Chetan Murthy

671 Barcelona Loop, Milpitas, CA, +1 408 250 0820, chetanmurthy@me.com

Work Experience

Innovium Inc, San Jose, California – *Principal Engineer* **Nov 2016 - Present**

- Designed and validated plugin based code generation framework to represent all the Innovium SDK modules abstractly as objects and packages using YAML notation (~70% SDK code is generated)
- Designed and Implemented plugins to generate Innovium SAI adapter layer, Innovium SDK API layer, SDK inter module layer for all the modules
- Designed and implemented framework to generate C code for data validation, type checking, object storage, logging, API replay, documentation, warm-boot
- Designed and architected the complete PI-PD API layer with two phase commit and post commit validation for all the Innovium SDK modules
- Designed and implemented code generation for REST access with CRUD on all Innovium SDK modules
- Designed, implemented and tested Innovium SDK's ACL, telemetry, and flexible packet field extraction modules

Cisco Systems, San Jose, California – *Technical Lead* **Dec 2013 – Oct 2016**

- Responsible for designing and implementing automatic code generation of C++ classes in python reading XML model that is used in SDK Hardware Abstraction Layer(HAL) to program and manage Cisco APIC ASIC
- Designed and implemented C API interface between apps and SDK HAL to communicate and perform parallel programming of multiple ASICS. Added support for basic and complex data types in the C API interface
- Implemented a multi-phase commit with rollback functionality in SDK. Added support for batching with inter or intra API commit. The generated C++ classes and the API modules extensively use shared pointers to minimize memory leak

Insieme Networks, Inc, San Jose - *Software Engineer* **Feb 2013 – Nov 2013**

- Designed and implemented device level diagnostics for testing asic memory, nvram, cpu, ssd, act2 etc and port level PRBS and loopback diagnostic tests for Cisco and Broadcom chipsets
- Responsible for designing and implementing collection and reporting of switch statistics of all the modules from Broadcom Trident 2 SDK, Cisco ACI chipsets (NorthStar, Alpine, Lacrosse and Sugarbowl)
- Designed and implemented atomic counters that is extensively used to debug fabric data path failures

Juniper Networks, Inc, Sunnyvale - *Software Engineer* **Jan 2009 – Feb 2013**

- Implemented and hand tuned hashing, packet-tap, DDOS protection for host path terminated packets in trinity microcode for better feature performance
- Implemented TCP/IP stack on PFE supporting IP fragmentation, reassembly and ARP resolution. Fine tuned the tcp performance to download 2 Million routes 30% faster than RDP

University of Florida - *Research Assistant* **Jan 2008 – Dec 2008**

- Devised an efficient bitstream compression and decompression accelerator for FPGA reconfiguration.
- Designed a novel multi dictionary compression technique for NISC architecture control words

Huawei Technologies, Bangalore - *Software Engineer* **Jun 2004 – Aug 2007**

- Inspect 2.0 – real time debugging tool for DORPA C, to manage and analyze crashes on multiple target nodes on VxWorks and Linux using DIFF, COFF object file formats (.NET managed VC++)
- Developed and implemented module system testing automation framework for DOPRA C reducing testing cycle by 40% of development cycle with 100% automation

Education

- 2007-2008: M.S. with Thesis in Computer Engineering, **University of Florida**. GPA: **3.81**/4.0
- 2000-2004: B.E. (Information Science), **Visvesvaraya Technological University**, Bangalore, India. **80.64**%

Skills & Interests

- Languages/Technologies: Proficient in C, Python, C++; familiar with javascript, sql, php, perl, objective C, html, css, xml, yaml, JSON, REST; experienced with git, aws, iphone/android, unix/linux
- Journals: "**Bitmask aware Compression of NISC Control Words**", Elsevier Integration, the VLSI Journal, 46(2), pages 131-41, March 2012, "**Decoding-aware Compression of FPGA Bitstreams**", IEEE Transactions on Very Large Scale Integration Systems, 19(3), pages 411-419, March 2011
- Patents: "**Lossless Data Compression and Real-time Decompression**", USPTO Patent Application 20100223237, 2010