

# Digital Logic Design Assignment 10 - EC2019-39

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## 1 EC2019 39

The state transition diagram for the circuit is

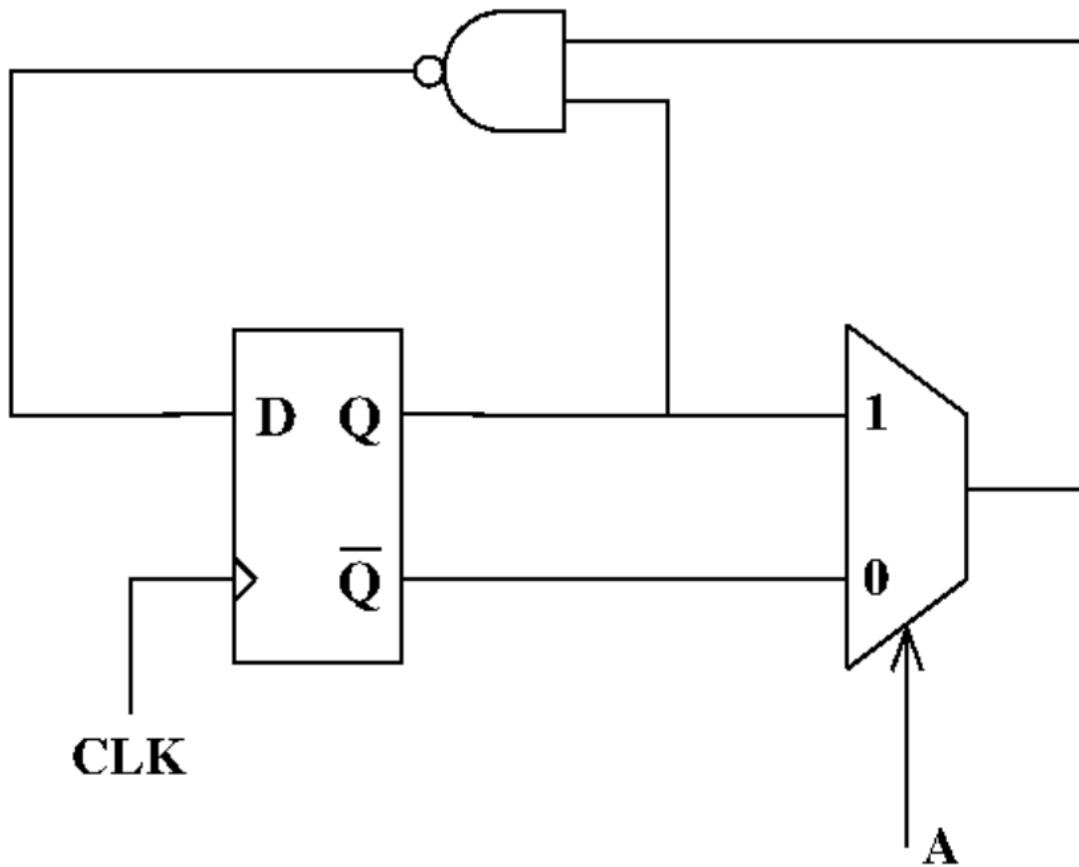


Figure 1

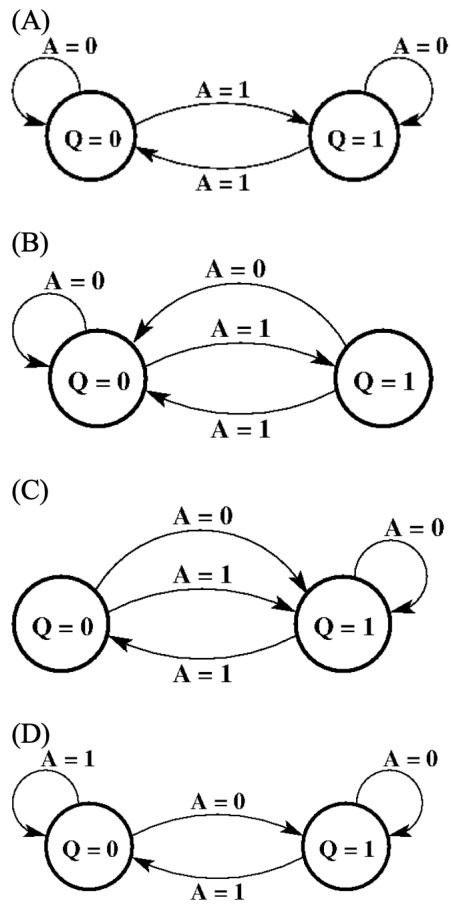


Figure 2

ANSWER.

The following circuit (figure 1) has one D flip flop, one 2\*1 multiplexer and one nand gate.

Now let us assume that output of the multiplexer as  $y$ .

if  $A=0$  then the output  $y=1$ .

$$D = \overline{Q} \cdot y.$$

$$D = \overline{Q} + \overline{y}.$$

the possible ways for output  $Q=0,1$ .

now let us assume that the output  $Q = 0$  then  $\overline{Q} = 1$ .

then  $D = 1 + 0$  .  $D = 1$ .

when  $A = 1$

then the output  $y = 0$ .

then  $D = \overline{Q \cdot y}$ .  
 $D = 1$ .  
 Now let us take  $Q = 1$ .  
 then when  $A = 0$ ,  $y = 1$ .  
 $D = \overline{Q} + \overline{y}$   
 $D = 0$   
 Similarly,  
 if  $A = 1$ ,  $y = 0$ .  
 then  $D = \overline{Q \cdot y}$   
 $D = 0 + 1$ .  
 $D = 1$ .  
 Therefore option (C) is correct.

TABLE 2		
Present state	input	Next state
0	0	0
0	1	1
1	0	0
1	1	1

