EC2017

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Figure I shows a 4-bit ripple carry adder realized using full adders and Figure II shows the circuit of a full-adder (FA). The propagation delay of the XOR, AND and OR gates in Figure II are 20 ns, 15 ns and 10 ns, respectively. Assume all the inputs to the 4-bit adder are initially reset to 0.

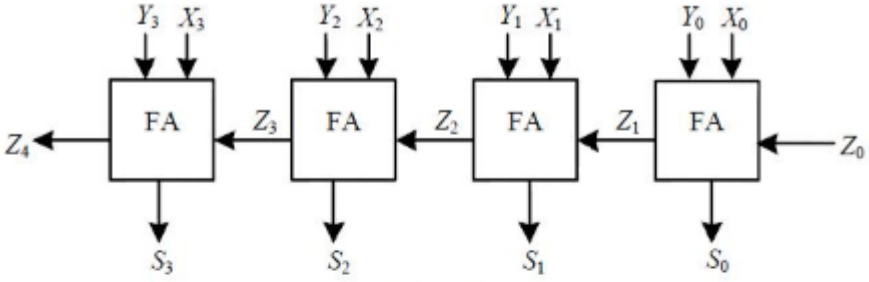


Figure I

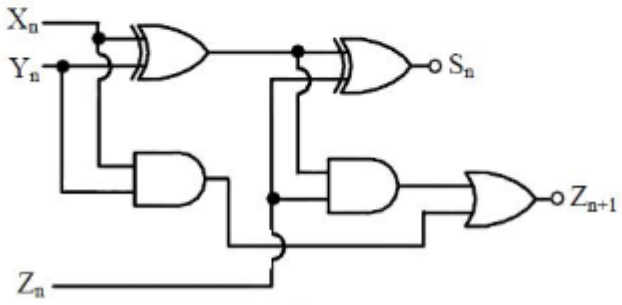
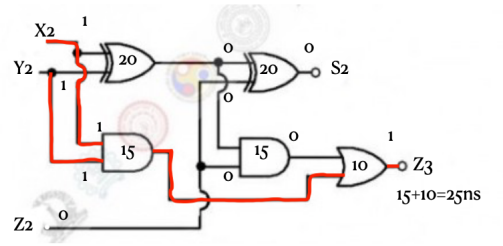


Figure II

At t = 0, the input to the 4-bit adder are changed to X3 X2 X1 Xo = 1100,

Y3 Y2 Y1 Yo = 0100 and Zo = 1. The output of the ripple carry adder will be stable at t (in ns)=

ANSWER



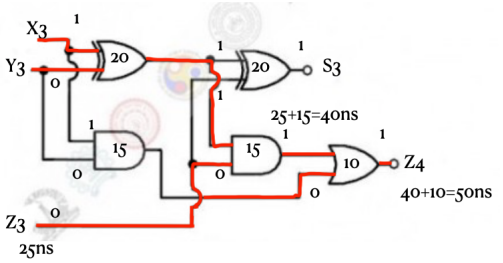


Table 1

n		3	2	1	0
	Z4 = 1	Z3 = 1	Z2 = 0	Z1 = 0	Z0 = 1
Xn		1	1	0	0
Yn		0	1	0	0
Sum		0	0	0	1

The delay in Z3 Output = 1 And+1 Or gate delay i.e 15 + 10 = 25 ns, the delay in Z4 Output = delay in Z3 input + 1 And + 1 Or gate i.e 25 + 15 + 10 = 50 ns. So the output of the ripple carry adder will be stable at t = 50 ns. (Full adder 1 is less significance so we did not considered that,and the reason why we did not considered XOR gate is because the delay of XOR gate is less than the delay of Z3 input). So the output of the ripple carry adder will be stable at t = 50 ns