CHETAN SOMANA

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Seasoned ASIC Verification Engineer with over 3 years of experience in high-paced environments. Aware of RTL to GDS II flow, with excellent coding and debugging skills in System Verilog and UVM. Demonstrated expertise in digital electronics, data structures, computer architecture design, and scripting. Proven track record of delivering high-quality verification solutions for complex ASIC designs.

WORK EXPERIENCE (3 Years)

Cyient LTD

APR 2022 – Present

ASIC Design Verification Engineer

SENT IP (INFINEON TECHNOLOGIES)

> Verifying two different flavours of SENT IP in two different environments.
> Extracting verification requirements for stimulus and coverage model development.
> Generated TB from scratch and integrated VIP's like CLOCK, RESET, AHB into generated bench.
> Integrated RAL model to facilitate register read/write transactions.
> Modelling SENT sensors.

AUTOMOTIVE PMIC (NXP)

> Hands on experience on all major ASIL-D PMIC digital blocks.
> Proactively engaged with the product definer, architects, designers and verification leads to develop vplans.
> Developed reusable sequences with constrained random stimulus and written assertions.
> Found the highest number of digital design bugs and later received an award from NXP R&D Vice President.
> Independently handled the design sign off checklist by meeting required Functional and Code coverage metrics.

QSPI (Internal)

> Responsible for writing the driver in STR and DTR mode which supports single, dual, and quad transfers.
> Developed testcases for both modes.

DPRAM (Internal)

> Implemented driver, monitor, scoreboard and coverage in the UVM environment.
> Provided stimulus using constraint random methods to cover various use cases.

Risetime Semiconductors

Aug 2021 – MAR 2022

Design Verification Engineer

16*16 router using SV and UVM

> Responsible for developing the testbench environment in system Verilog and UVM.
> Hands on experience on developing driver, monitor, interfaces, scoreboard, coverage.

Online Certified courses

>Cadence RTL to GDS II Flow v5.0: (completed)
>Multi-Core Computer Architecture IIT Guwahati(completed)

EDUCATION

Bachelor of Engineering / CGPA 7.29
Methodist College of Engineering and Technology

12 High School / 94%
Mac Arthur High School

10 SSC / CGPA 9.2
Bhashyam High School

SKILLS

System Verilog
UVM
TCL interactive debugger
Assertions
Micro architecture design
Leadership
Problem-solving
Rational Thinker
Coding in C & Python
ASIL D Functional Safety
Version Control System (GIT, SVN)
