Chetan Somana

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EDUCATION

North Carolina State University — Raleigh, NC
M.S. in Electrical Engineering — Apr 2027
Relevant Coursework: ASIC/FPGA design with Verilog 564, Microprocessor Architecture 563, UMV 748
Future Coursework: Advanced Comp Arch(CPU+GPU) 786, Parallel Comp Arch 506, Comp and Network Security 574

Osmania University — Hyderabad, India
B.S. in Electronics and Communication Engineering — Jun 2021
Coursework: Digital Electronics, Computer Organization, Digital Signal Processing

SKILLS

Programming: Verilog, System Verilog, UVM, Shell Scripting, Python, C++
Core Competencies: Verification planning, VIP integration, Testbench creation, RAL integration, Constrained Random Stimulus, Assertions, Coverage analysis
Protocols: I2C, QSPI, AHB, CSI, DSI, ASA-ML
Tools: Xcelium, Simvision, Vmanager, Questa Sim, VCS, Verdi, Version Control with SVN, GIT
Soft Skills: Accountability, Communication, Collaboration, Ownership

WORK EXPERIENCE

ACL DIGITAL — Bangalore, India
Senior Digital Verification Engineer — Jan 2025 – Jul 2025
ASA-Motion Link IP

- Accelerated ASA-ML SerDes verification by architecting a UVM-based camera sensor data generator that cut the stimulus development timeline, enabling earlier integration by four days.
- Owned the protocol analysis for the ASA-ML PHY layer, developing a timing reference that was adopted team-wide as the golden reference and eliminated the need for redundant calculations.
- Eliminated three weeks of redundant modeling effort by creating a SystemVerilog DPI framework to reuse golden C/Python reference models, enabling a deeper focus on corner-case bug hunting.
- Authored in-depth data-flow documentation for the SerDes PHY, enabling new engineers to contribute to projects one week sooner.

CYIENT — Hyderabad, India
ASIC Verification Engineer — Apr 2022 – Jan 2025
SENT Sensor IP – ODC Client: Infineon Technologies

- Rapidly generated a verification environment for a SENT protocol IP by mastering Infineon's proprietary tool flows to integrate standard AHB, clock, reset VIPs and validated register access on waveform within two weeks.
- Engineered a flexible, macro-based SystemVerilog framework to abstract differences between two chip flavors, cutting the bring-up time for both verification flows to under one month.
- Streamlined client communication by creating a reporting system that showcased regression results with detailed analysis and trend charts, reducing time spent in weekly meetings by 40% for 8 members involved.

Power Management IC – ODC Client: NXP

- Authored detailed verification plans for multiple digital blocks, consistently completing 2-3 days ahead of schedule, which allowed for contribution to other critical blocks to ensure collective team deadlines were met.
- Identified and resolved 52 critical design bugs by initiating a collaborative effort between analog, digital, and mixed-signal teams, earning a corporate award from the NXP R&D VP for the achievement
- Secured a critical tape-out by resolving all regression failures to achieve 100% coverage on the digital controller.

Armnok

- Developed and validated a reusable I2C VIP, including driver and monitor components, which was successfully integrated into a larger SoC project.
- Executed comprehensive verification of a QSPI VIP, developing test cases for single/dual/quad I/O lines in both single and double data rate.

RISETIME SEMICONDUCTORS — Hyderabad, India
Digital Verification Engineer — Aug 2021 – Mar 2022

- Developed a SystemVerilog testbench for a 16x16 switching router, implementing a driver, monitor, scoreboard, assertions and functional coverage from scratch while mastering Verdi and Simvision EDA tools.
- Designed and implemented a suite of fundamental digital IP blocks in SystemVerilog, including a watchdog timer, asynchronous FIFO, and packet decoder, successfully applying digital logic principles to create functional hardware.

ACADEMIC PROJECTS at NC State University

Cache and Memory Hierarchy Design Simulator (Completed)

- Architected a C++ simulator for a multi-level L1/L2 cache, which demonstrated an 8% reduction in Average Memory Access Time by implementing a stride-based prefetcher alongside LRU and write-back/write-allocate policies compared to FIFO.

16 Bit RISC based LC3 Microcontroller (Ongoing)

- Drove a pipelined LC3 processor to 100% functional coverage by developing a reusable UVM testbench from scratch. Authored 16 sequences to hit 50 unique instructions of LC3 ISA.

Branch Prediction Simulator (563 Future Project)
Out of Order Scalar/Superscalar Processor (563 Future Project)
Convolution Neural Network with DRAM interface (564 Future Project)
MEOSI based Cache Controller in Multi core CPU (506 Future Project)
Locality Aware L1D Cache Management (786 Future Project)
Secure Communication Using AES and PSK (574 Future Project)

LEADERSHIP & ACHIEVEMENTS

- Earned a spot as teaching assistant for the NIT Kurukshetra VLSI workshop, where I taught students to debug Linux environment issues, tool errors and guided them through their first VLSI design project.
- Received an award from NXP R&D VP for finding most design bugs.
- Mentored undergraduate interns at ACL Digital in their VIP development.
- Ranked in the top 5% (out of 224 participants) in a proctored national examination on Multi-Core Computer Architecture administered by IIT Guwahati.
- Recognized as the team's Top Contributor for two consecutive years (2023, 2024), earning the highest possible performance rating in each annual analysis.