

Chetan Somana

✉ chetan.somana@gmail.com [in linkedin.com/in/chetan-somana](https://www.linkedin.com/in/chetan-somana)

SUMMARY

A passionate engineer with excellent coding skills and good knowledge in digital electronics, Verilog, System verilog verification and data structures

EXPERIENCE

Design Verification Engineer

NXP Semiconductors

November 2022 – Present, Hyderabad, Telangana, India · Remote

Worked with NXP from verifying the design starting with scratch to the metal layer tapeout.

- > Gained experience in ASIL D automotive verification.
 - > Developed vplans from scratch.
 - > During the vplans development interacted with spec definer, DV lead to clear the ambiguity.
 - > Made vplan with summarized diagrams, tables, waveforms to save time during the review.
 - > Developed the mindset of reusing the existing code than to reinvent wheel for better future reusability and to save time.
 - > Developed sequences which deals with the signal level of digital i/o pins. Understood the base functionality of the complicated sequences, instead of modifying them, I've created a new sequences from the base sequence. Added required functionality.
 - > Tested the many blocks and reapplied previous learned verification concepts
 - > Constraint random verification. Add all the stimulus in the base test. Extend the base test and constraint to specific scenario so that metrics are easily measured.
 - > Sequence based stimulus. Exploited the sequence features as they can be used to any test at any point of time in the simulation.
 - > RAL.
 - > Developed writing assertions which mimics the design.
 - > Understand the use of vsif in the regression methodology. Able to do session compare, analyze failures, analyze metrics, modify vsif to target specific group with more seeds.
 - > Improved the functional coverage of the project by myself analysing the bins generated by the script. Provided feedback to the script to ignore RO bins to only read, truncated the maximum bins to a realistic case as its take larger cpu power/time to cover 8bit field.
- Created refinement file in case by basics.
- > Improved the code coverage of VAON, FCCU, BUCK, DEGLICTER. Applied HDL skills for quicker analysing the block, expression, toggle, FSM areas.
 - > Tools used for verification Cadence xcelium
 - > Project maintenance tools Bitbucket, Jira, Doors, Confluence, pipa

Asic design verification engineer

Cyient

April 2022 – Present, Hyderabad, Telangana, India

- > Worked on QSPI flash memory. Verified single, dual and quad in single edge transfer / double edge transfer. Written constraint for randomization. Learned to use Vmanager for regression.
- > Worked on propriety system bus protocol. Developed monitor, scoreboard. Took assistance from a senior engineer to develop assertions.
- > Good hands on experience in scripting.
- > Worked in cadence, synopsys, mentor graphics environments.

Design Verification Engineer

RiseTime Semiconductors

August 2021 – March 2022, Hyderabad, Telangana, India

- > Verified 16 * 16 router using UVM. Developed monitor and scoreboard to verify the payload between source and destination to 100% on every possible route on the router.
- > Worked on I2C protocol in 100KHz, 400KHz. Verified the multiple slave addressing, start/stop conditions, acknowledgement.

Trainee Embedded Hardware Engineer

Affluence Infosystems

March 2021 – June 2021, Hyderabad, Telangana, India

Coming up with a block diagram of a product and turning it into a schematic using OrCad Capture. Verifying the voltage levels of PMIC with the help of CRO according to component layout. My current project is on Infotainment systems.

Quality Analyst

Saia Water Tower

May 2019 – June 2019, Hyderabad, Telangana, India

Maintain machine tools in proper operational condition. Inspect, test, and adjust completed units to ensure that units meet specifications, durability, and customer order requirements.

PROJECTS

Face Detection

September 2019 - October 2019

Gathered data of family members. Created a positives and negatives of the faces to train the machine. Using openCV, a python image processing library developed face detection.

4*4*4 LED CUBE using Arduino

February 2018 - April 2018

Soldered the LED on 1 strand wire in 4 by 4 matrix with the base as veroboard. Underneath the board connected 100ohm resistor for every 4*4 LED. All the necessary connections are plugged into Arduino. After dumping the code into the microcontroller, LED glows based on code.

EDUCATION

Bachelor's degree, Electrical, Electronics and Communications Engineering

Methodist college of eng and tech · June 2021

COURSEWORK

Cisco IOT

Remote Sensing Applications in Agriculture by ISRO

SKILLS

Industry Knowledge: Code Coverage, SystemVerilog, Digital Electronics, Universal Verification Methodology (UVM), Data Structures, Mobile Electronics

Tools & Technologies: Python (Programming Language), Embedded Systems