Indian Institute of Technology (IIT-Kharagpur)

AUTUMN Semester, 2023
COMPUTER SCIENCE AND ENGINEERING

Computer Organization and Architecture Laboratory

Verilog Assignment 6

September 11, 2023

Instructions: *Make one submission per group in the form of a single zipped folder containing your source file(s). Name your submitted zipped folder as Assgn_1_Grp_GroupNo.zip and (e.g. Assgn_1_Grp_25.zip). Inside each submitted source files, there should be a clear header describing the assignment no., problem no., semester, group no., and names of group members. The file name should be of the format QuestionNo_Grp_GroupNo.s (e.g. Q1_Grp_25.s). Liberally comment on your code to improve its comprehensibility.*

1. Interface an 8x4 register bank to a 16x4 memory system, with suitable control signals for read and write operations. The following operations can be carried out:

(a) Read a 4-bit data and store it into a specified memory location with 4-bit address.

(b) Given a register number and a memory address, transfer data from register to memory.

(c) Same as above, but transfer data from memory to register.

(d) Given a memory address, display the contents of the memory location.