Verilog Assignment 6

GROUP 14

P. Chethan Krishna Venkat (21CS30036)
G . Vikhyath (21CS10028)

Description:

We have created a memory block with parameter:

- Depth =16
- Width = 4

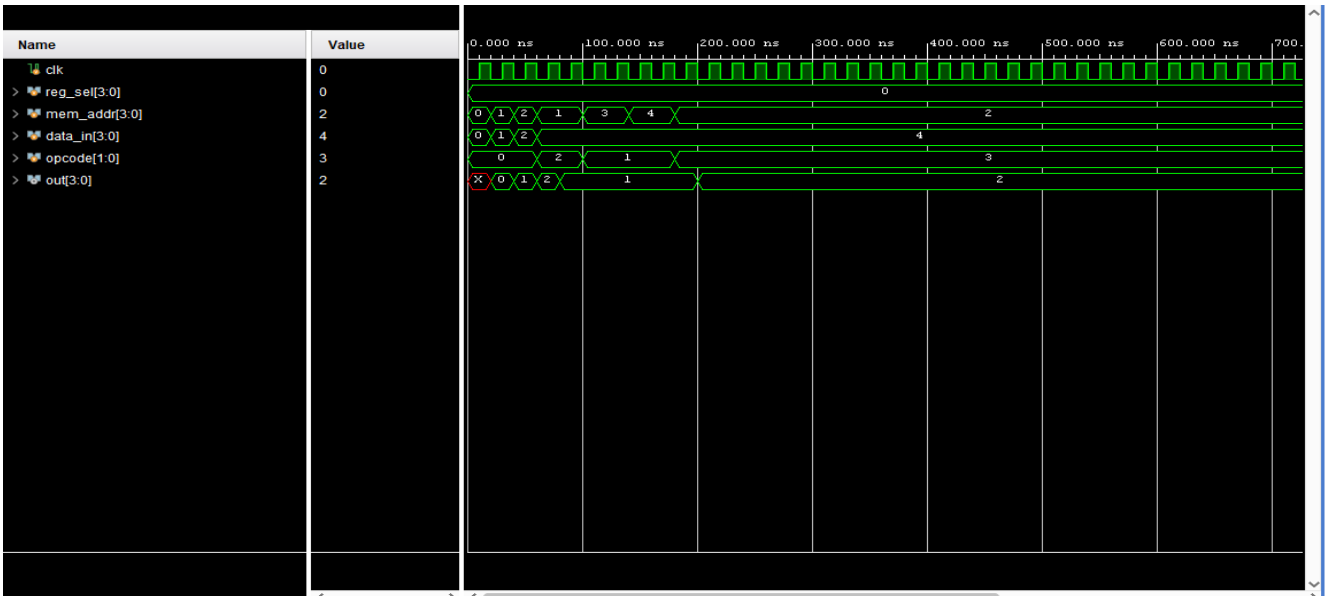
These are used to initialise 16 memory blocks each with 4 bits.

- Our main module is the "register_*memory_interface*", it has inputs: Clock - clk, register number - reg_adrs (3 bits), memory address – mem_addrs (4 bits), select operation - select (2 bits), data input - data_in (4 bits); Output: data output - data_out (4 bits).
- This module uses select to choose among the four options to perform: - 0 (00) = to read an input and store it in a memory address.
  - 1 (01) = to transfer data from a register to given memory address.
  - 2 (10) = to transfer data from a memory address to a given register. - 3 (11) = to display data in a memory address.
- This module also has an module instantation for the module "*blk_mem_gen_0*" which is an important module obtained using IP catalog. It takes inputs: clock, enable, write enable, memory address, data input ; output: data output.

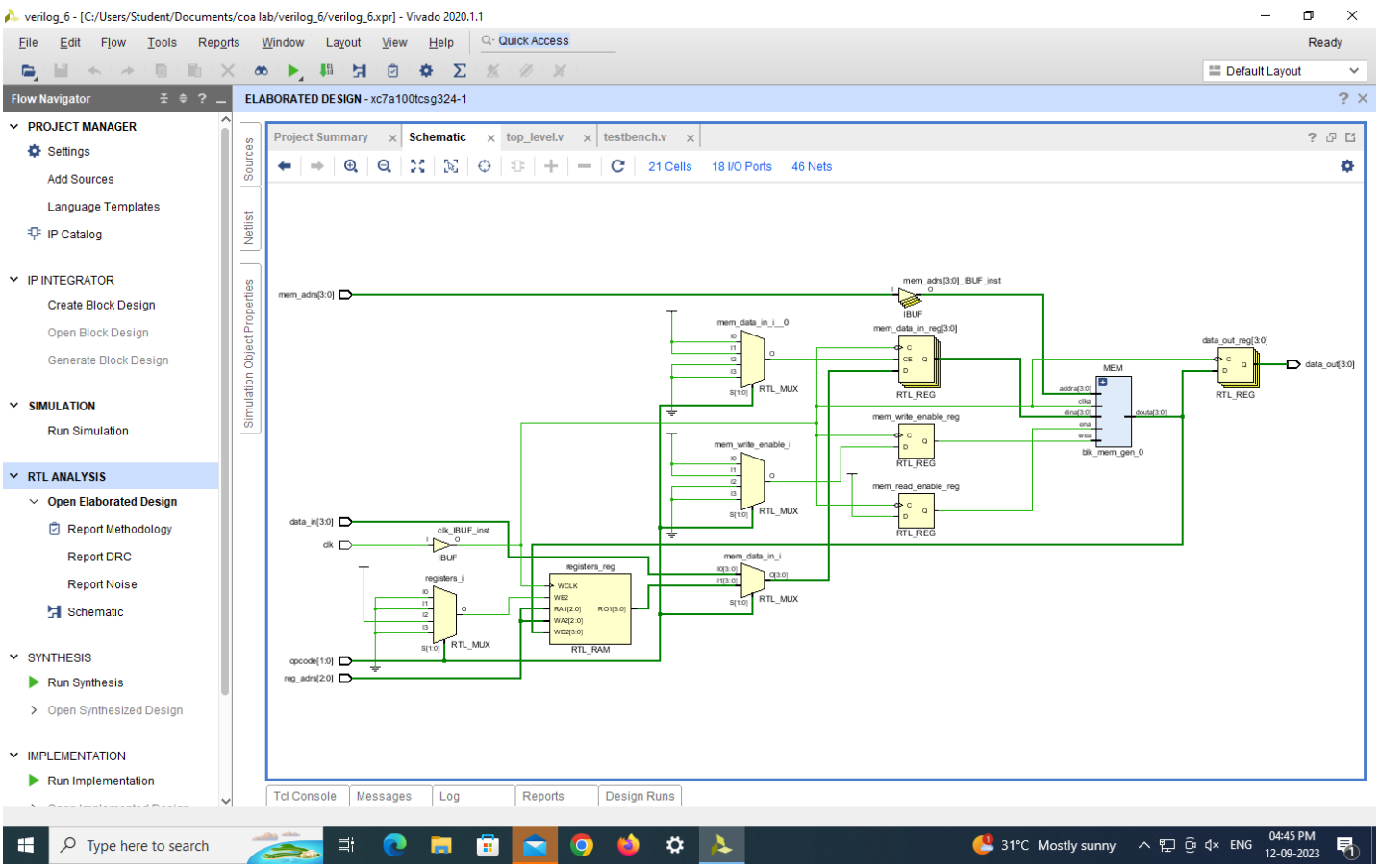
Explanation of test case used in test bench:

- for the operation 0: 1)pass in a data (0) to store in a memory address (0000).
  2) pass in a data (1) to store in a memory address (0001).
  3) pass in a data (2) to store in a memory address (0010).
- Then using operation 2: pass the data in this memory location (0001) into the register number (0).
- From here use operation 1: pass the data in the register number (0) into the memory address (0011).
- From here use operation 1: pass the data in the register number (0) into the memory address (0100).
- Finally , using operation 3: display the data in memory address (0010).
- Proper flow and display of the data indicates proper functioning of the module.

Simulation:



Schematic Diagram



Values in memory locations after all the testcases