Indian Institute of Technology (IIT-Kharagpur)

AUTUMN Semester, 2023

COMPUTER SCIENCE AND ENGINEERING

Computer Organization and Architecture Laboratory

Verilog Assignment 1

August 21, 2023

INSTRUCTIONS: Make one submission per group in the form of a single zipped folder containing your source file(s). Name your submitted zipped folder as Assgn_1_Grp_GroupNo.zip and (e.g. Assgn_1_Grp_25.zip). Inside each submitted source files, there should be a clear header describing the assignment no., problem no., semester, group no., and names of group members. The file name should be of the format QuestionNo_Grp_GroupNo.s (e.g. Q1_Grp_25.s). Liberally comment on your code to improve its comprehensibility.

1 Question 1

Design a 2-to-1 multiplexer module, and using it design a 4-to-1 multiplexer.

2 Question 2

Design a full adder module using structural description (i.e., netlist of gates using assign statements). Instantiate the full adder module six times to design a 6-bit ripple-carry adder.