Indian Institute of Technology (IIT-Kharagpur)

AUTUMN Semester, 2023

COMPUTER SCIENCE AND ENGINEERING

Computer Organization and Architecture Laboratory

Verilog Assignment 2

August 23, 2023

INSTRUCTIONS: Make one submission per group in the form of a single zipped folder containing your source file(s). Name your submitted zipped folder as Assgn_1_Grp_GroupNo.zip and (e.g. Assgn_1_Grp_25.zip). Inside each submitted source files, there should be a clear header describing the assignment no., problem no., semester, group no., and names of group members. The file name should be of the format QuestionNo_Grp_GroupNo.s (e.g. Q1_Grp_25.s). Liberally comment on your code to improve its comprehensibility.

1 Question 1

Write a Verilog module containing 8 registers, R0 to R7, each of size 16 bits. The registers must have parallel load facility, with synchronous LOAD, and output ENABLE facility. If the output is not enabled, all the output lines will be in the high-impedance state.

In the top-level module, there will be five input ports, (a) 3-bit source register number, (b) 3-bit destination register number, (c) control signals MOVE and IN, (d) a 16-bit data input port, and (e) CLOCK. The value of the source register selected will also be available on an 16-bit output port.

Write the necessary Verilog modules, write a suitable test bench to simulate the modules to verify the correctness.

2 Question 2

Write Verilog module(s) to compute the GCD of two 8-bit numbers A and B. Make relevant assumptions. Write a suitable test bench to test the module.