Indian Institute of Technology (IIT-Kharagpur)

AUTUMN Semester, 2023
COMPUTER SCIENCE AND ENGINEERING

Computer Organization and Architecture Laboratory

Verilog Assignment 3

August 28, 2023

Instructions: *Make one submission per group in the form of a single zipped folder containing your source file(s). Name your submitted zipped folder as Assgn_1_Grp_GroupNo.zip and (e.g. Assgn_1_Grp_25.zip). Inside each submitted source files, there should be a clear header describing the assignment no., problem no., semester, group no., and names of group members. The file name should be of the format QuestionNo_Grp_GroupNo.s (e.g. Q1_Grp_25.s). Liberally comment on your code to improve its comprehensibility.*

1. Design a 8-bit ALU with the following functionalities. Assume that the ALU is fed with two 8-bit inputs in1 and in2, and produces an 8-bit output result.

- $result = in1 + in2$
- $result = in1 - in2$
- $result = in1$
- $result = in1 << 1$
- $result = in1 >> 1$
- $result = in1$ AND $in2$
- $result = NOT\ in1$
- $result = in1$ OR $in2$

The ALU has eight functions, which is selected by a 3-bit input "func".

Write separate modules for each of the eight functions, which will be instantiated in the top-level ALU module. The addition amust be implemented using structural modeling using carry lookahead adder. Implement the subtractor using a complementer and an adder.

In the test bench, connect registers to the inputs and output of the ALU module, and feed various test inputs in synchronism with a clock.