

Verilog Assignment 6

GROUP 14

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Description:

We have created a memory block with parameter:

- Depth = 16
- Width = 4

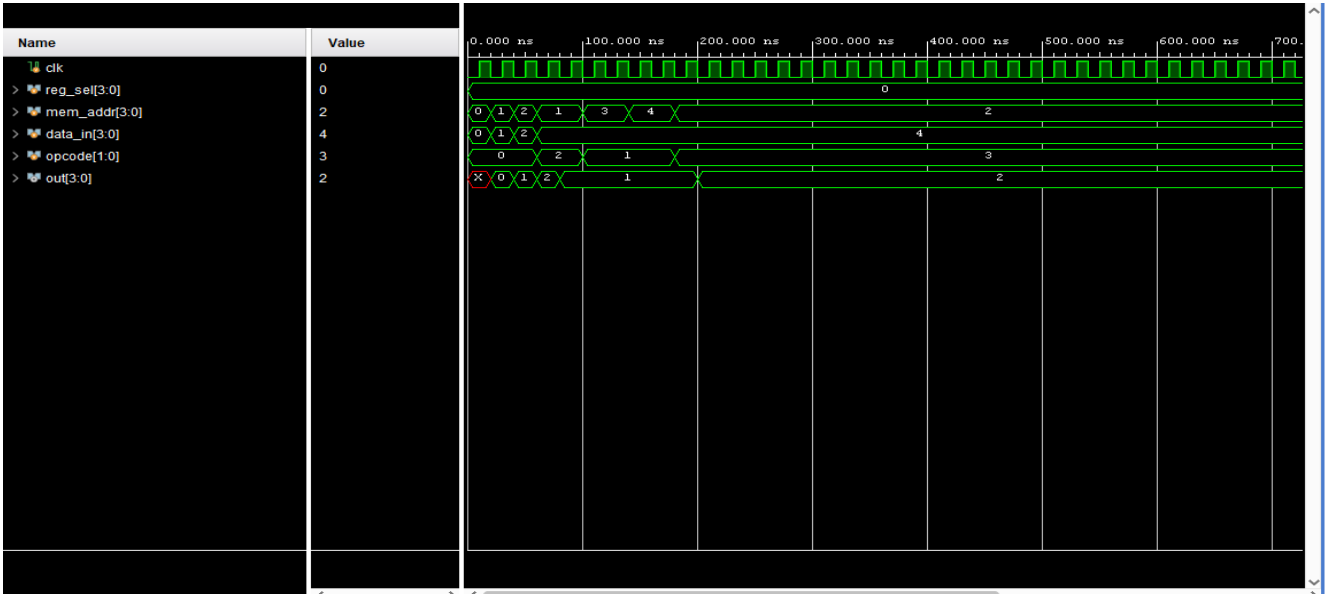
These are used to initialise 16 memory blocks each with 4 bits.

- Our main module is the “*register_memory_interface*”, it has inputs: Clock - *clk*, register number - *reg_adrs* (3 bits), memory address – *mem_adrs* (4 bits), select operation - *select* (2 bits), data input - *data_in* (4 bits); Output: data output - *data_out* (4 bits).
- This module uses *select* to choose among the four options to perform:
 - 0 (00) = to read an input and store it in a memory address.
 - 1 (01) = to transfer data from a register to given memory address.
 - 2 (10) = to transfer data from a memory address to a given register.
 - 3 (11) = to display data in a memory address.
- This module also has an module instantiation for the module “*blk_mem_gen_0*” which is an important module obtained using IP catalog. It takes inputs: clock, enable, write enable, memory address, data input ; output: data output.

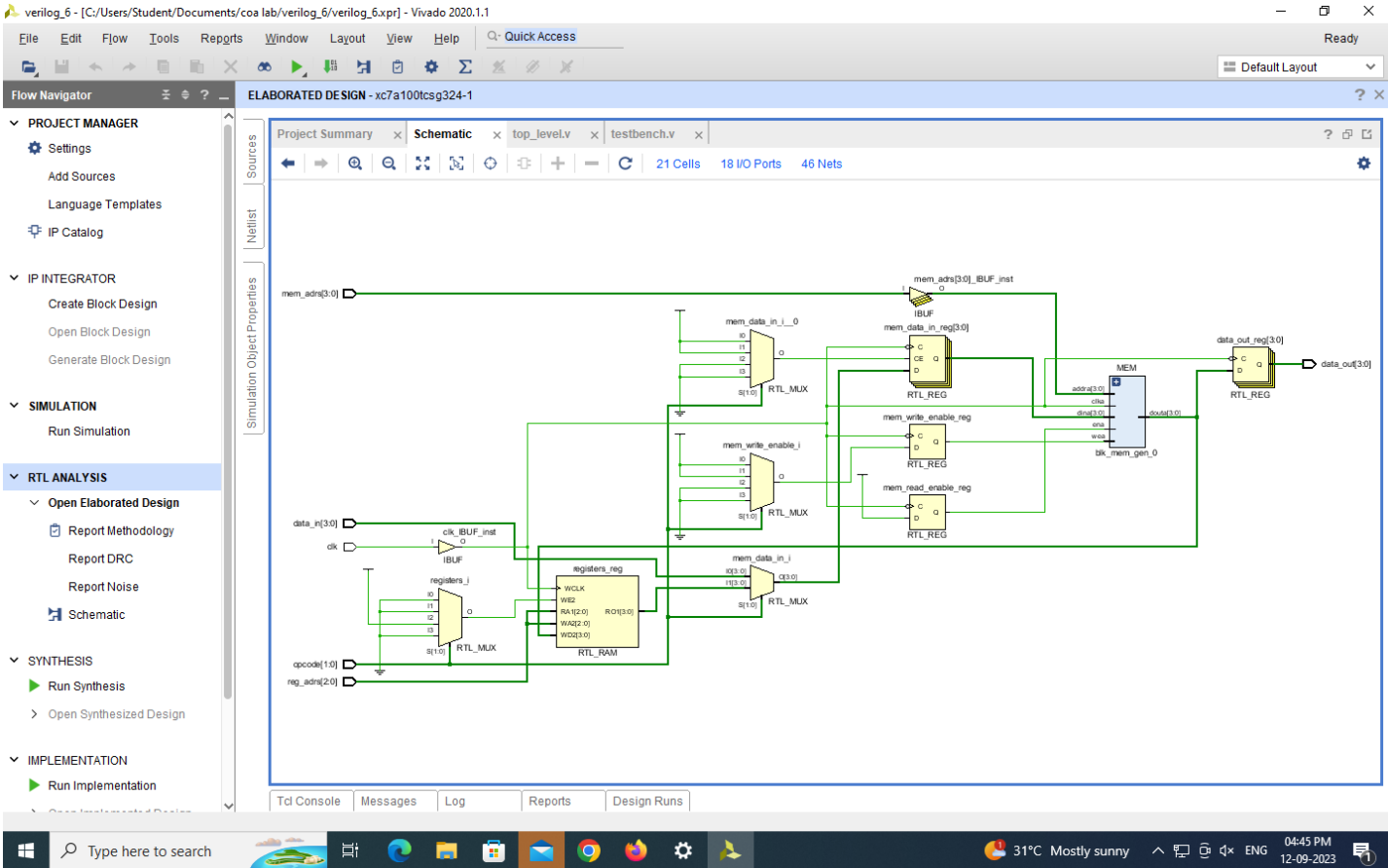
Explanation of test case used in test bench:

- for the operation 0: 1) pass in a data (0) to store in a memory address (0000).
2) pass in a data (1) to store in a memory address (0001).
3) pass in a data (2) to store in a memory address (0010).
- Then using operation 2: pass the data in this memory location (0001) into the register number (0).
- From here use operation 1: pass the data in the register number (0) into the memory address (0011).
- From here use operation 1: pass the data in the register number (0) into the memory address (0100).
- Finally , using operation 3: display the data in memory address (0010).
- Proper flow and display of the data indicates proper functioning of the module.

Simulation:



Schematic Diagram



Values in memory locations after all the testcases

verilog_6 - [C:/Users/Student/Documents/coa lab/verilog_6/verilog_6.xpr] - Vivado 2020.1.1

File Edit Flow Tools Reports Window Layout View Run Help Quick Access Ready

Flow Navigator

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

SIMULATION - Behavioral Simulation - Functional - sim_1 - TestBench

Scope Sources Objects Protocol Inst

Scope

Name	Design U...	Block T...
TestBench	TestBench	Verilog
top_module	register_me	Verilog
MEM	blk_mem_g	Verilog
inst	blk_mem_g	Verilog
native_r	blk_mem_g	Verilog
gbl	gbl	Verilog

Objects

Name	Value	Data Type
DBITE	0	Logic
RDAD	0	Array
mem	0,1,2,1,1,0,0	Array
[0]	0	Array
[1]	1	Array
[2]	2	Array
[3]	1	Array
[4]	1	Array
[5]	0	Array
[6]	0	Array
[7]	0	Array
[8]	0	Array
[9]	0	Array
[10]	0	Array
[11]	0	Array
[12]	0	Array
[13]	0	Array
[14]	0	Array

top_level.v testbench.v Untitled 20

Name Value

Name	Value
clk	0
reg_sel[3:0]	0
mem_addr[3:0]	2
data_in[3:0]	4
opcode[1:0]	3
out[3:0]	2

0.000 ns 100.000

Tcl Console Messages Log

INFO: [USF-XSim-96] XSim completed. Design snapshot 'TestBench_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:03 ; elapsed = 00:00:09 . Memory (MB): peak = 1413.188 ; gain = 0.000

Type a Tcl command here

Simulation Object memory

Windows Taskbar: 31°C Mostly sunny 04:44 PM 12-09-2023