Indian Institute of Technology (IIT-Kharagpur)

AUTUMN Semester, 2023
COMPUTER SCIENCE AND ENGINEERING

Computer Organization and Architecture Laboratory

Verilog Assignment 4

August 30, 2023

Instructions: *Make one submission per group in the form of a single zipped folder containing your source file(s). Name your submitted zipped folder as Assgn_1_Grp_GroupNo.zip and (e.g. Assgn_1_Grp_25.zip). Inside each submitted source files, there should be a clear header describing the assignment no., problem no., semester, group no., and names of group members. The file name should be of the format QuestionNo_Grp_GroupNo.s (e.g. Q1_Grp_25.s). Liberally comment on your code to improve its comprehensibility.*

1. Design an 8-bit multiplier as per the Booth's Multiplication Algorithm. The flowchart for the algorithm is shown in Figure 1. Consider the MSB of multiplier and multiplicand as sign-bit. The top-level module should be structural, and there must be separate modules for each block, such as adder, shifter, etc.

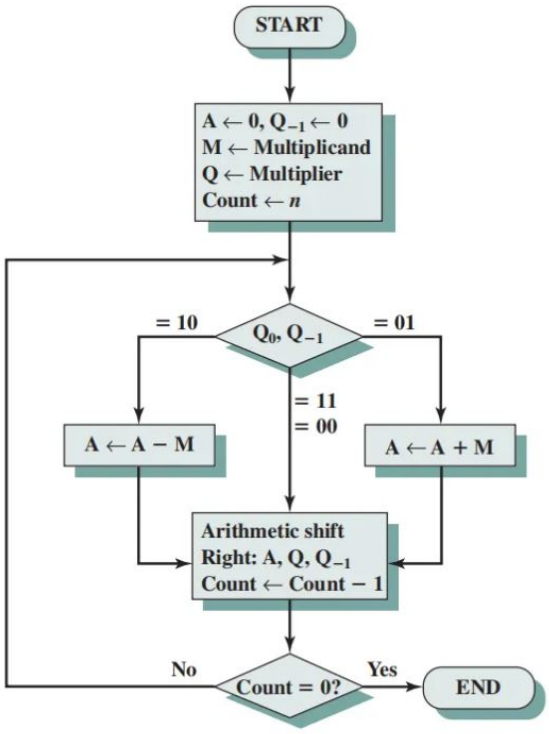

Figure 1: Booth's Algorithm Flowchart