Indian Institute of Technology (IIT-Kharagpur)

AUTUMN Semester, 2023
COMPUTER SCIENCE AND ENGINEERING

Computer Organization and Architecture Laboratory

Verilog Assignment 5

September 4, 2023

Instructions: *Make one submission per group in the form of a single zipped folder containing your source file(s). Name your submitted zipped folder as Assgn_1_Grp_GroupNo.zip and (e.g. Assgn_1_Grp_25.zip). Inside each submitted source files, there should be a clear header describing the assignment no., problem no., semester, group no., and names of group members. The file name should be of the format QuestionNo_Grp_GroupNo.s (e.g. Q1_Grp_25.s). Liberally comment on your code to improve its comprehensibility.*

Objective of the Project:

In this project, we would design a circuit which takes an input x which is of 32 bits (4 bytes), and computes the value of $y = x/255$, without using any multiplier or division unit. The circuit would comprise of only an 8-bit subtractor and shifters as the main data-path elements.

(Hint: Let, $y = x/255$, thus $y = 256y - x$)

For this proceed in the following steps:

1. Consider, x as a 4-byte element, x_3, x_2, x_1, x_0, where each x_i is a byte. Explain the circuitry of how to obtain y from x by a diagram. Note $256y$ is a byte-shift of y.

2. Write the verilog code Divby255 in the Xilinx tool for realizing the circuit. Also write the test-bench to simulate the verilog code. Note that the top-level of the design module Divby255 must be structural, while the internal modules, may be behavioral.

3. Download the bit-stream onto your FPGA device and demonstrate its working.