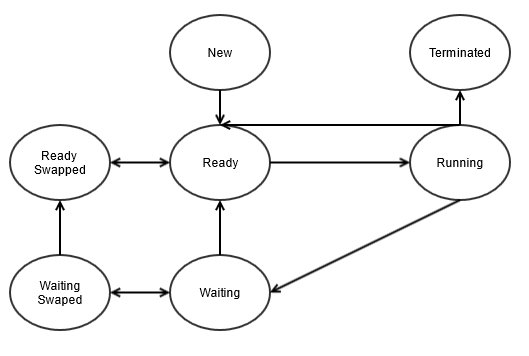
1. Caches are useful when the primary location of the data has a far slower response time then the processor that needs access to the information. Cache can also be used as a way to transfer data between different programs. The main thing a cache alleviates is waiting on the system IO to retrieve data from a slower device, allowing for higher CPU utilization. The largest problems when dealing with caches is ensuring all levels are kept synchronized when dealing with a multiprocessor environment. If not careful, multiple programs can interact with the same piece of data causing inconsistences in chances.
2. The purpose of an interrupt is to allow for a piece of hardware to stop the currently executing program and run instructions based on the specific hardware. A system call is a way for a user mode program to make use of privileged mode CPU instructions, by making a request though the operating system.
3. Monitor Mode, more commonly referred to as privileged mode, is allowed to execute special more powerful instructions on the CPU that a program in User Mode is unable to execute. This gives a basic safeguard to prevent a program from executing a command that could cause harm to the user if done unintentionally, such as deleting a file or restarting the system.
4. The two types of IPC are message passing, and using shared memory. Shared Memory tends to be faster on single core system then Message Passing due to Message Passing having to go through the kernel, but on a multiprocessor machine Message Passing will actually have a speed advantage due to not having to deal with data spread among multiple caches. Shared Memory also leads to an issue where multiple processes could attempt to access the same piece of data simultaneously, and Message Passing is normal limited in the size of the messages.
5. The main advantage to the Microkernel approach is it makes expanding system functionality easier. User and system mode services interact with the microkernel though the use of message passing. A major disadvantage to the microkernel approach is that performance may suffer due to a higher overhead.
6. The layered kernel structure and the modular kernel structure are similar in that they move core system functionality outside of the main system kernel into self-contained services that can be changed without recompiling the entire kernel. The modular structure main difference from layered is that any module can access any other module, but in a layered system layers can only access functions below them and not above.
7. Short Term Scheduling is used to regulate how long individual processes are running on the CPU and determine the order processes are run in. The Long Term Scheduling is used to determine which process to allow into execution, and is used to regulate the rate new processes are given to the short term scheduler.
8. A PCB is a Process Control Block, which hold the information about a specific process, such as its state, process number, and the program counter.
9. Medium Term Scheduling swaps a process in or out of main memory into a secondary memory location, commonly a hard drive disk.





|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Process | CPU burst time | Arrival time | Priority queue | Wait Time | Response Time | Turnaround Time |
| P1 | 10 | 0 | 2 | 26 | 0 | 36 |
| P2 | 7 | 3 | 1 | 0 | 0 | 7 |
| P3 | 6 | 4 | 2 | 21 | 4 | 29 |
| P4 | 5 | 12 | 1 | 0 | 0 | 5 |
| P5 | 8 | 18 | 1 | 0 | 0 | 8 |
|  |  |  | Average | 9.4 | 0.8 | 17 |



1. FCFS:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Process | Arrival time | CPU burst time | Wait Time | Response Time | Turnaround Time |
| P1 | 0 | 8 | 0 | 0 | 8 |
| P2 | 3 | 5 | 5 | 5 | 10 |
| P3 | 4 | 10 | 9 | 9 | 19 |
| P4 | 6 | 9 | 17 | 17 | 26 |
| P5 | 11 | 7 | 21 | 21 | 28 |
|  |  | Average | 10.4 | 10.4 | 18.2 |



SJF:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Process | Arrival time | CPU burst time | Wait Time | Response Time | Turnaround Time |
| P1 | 0 | 8 | 0 | 0 | 8 |
| P2 | 3 | 5 | 5 | 5 | 10 |
| P3 | 4 | 10 | 25 | 25 | 35 |
| P4 | 6 | 9 | 14 | 14 | 23 |
| P5 | 11 | 7 | 2 | 2 | 9 |
|  |  | Average | 9.2 | 9.2 | 17 |
|  |  |  |  |  |  |



RR(TQ5):

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Process | Arrival time | CPU burst time | Wait Time | Response Time | Turnaround Time |
| P1 | 0 | 8 | 20 | 0 | 28 |
| P2 | 3 | 5 | 2 | 2 | 7 |
| P3 | 4 | 10 | 19 | 6 | 29 |
| P4 | 6 | 9 | 22 | 9 | 31 |
| P5 | 11 | 7 | 21 | 9 | 28 |
|  |  | Average | 16.8 | 5.2 | 24.6 |

