Experiment No: 3

Name: Atharva Dhobale
Roll no: E43001
Division: BE 3 **Batch:** B9

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
useIEEE.STD_LOGIC_unsigned.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entitymodncount is
   Port ( clk : in  STD_LOGIC;
clr : in  STD_LOGIC;
q :inout  STD_LOGIC_VECTOR (2 downto 0));
endmodncount;

architecture Behavioral of modncount is
signal count: std_logic_vector(2 downto 0);
begin
process(clk)
begin
if (clr='1') then count <= "000";

elsif (rising_edge (clk)) then
if (count="100")
then  count<= "000";

else
count<=count+ 1;
end if;
end if;
end process;
q<=count;
end Behavioral;
```

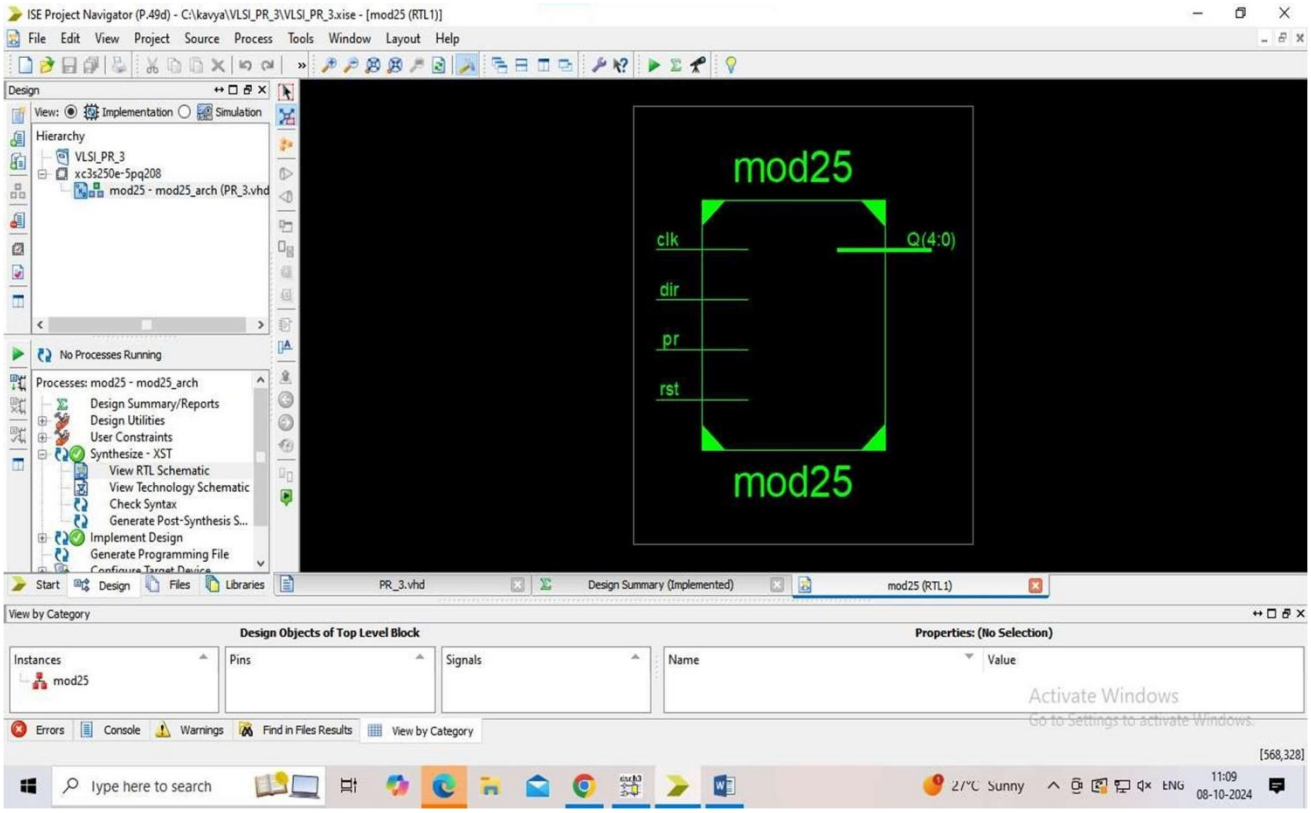
Testbench:

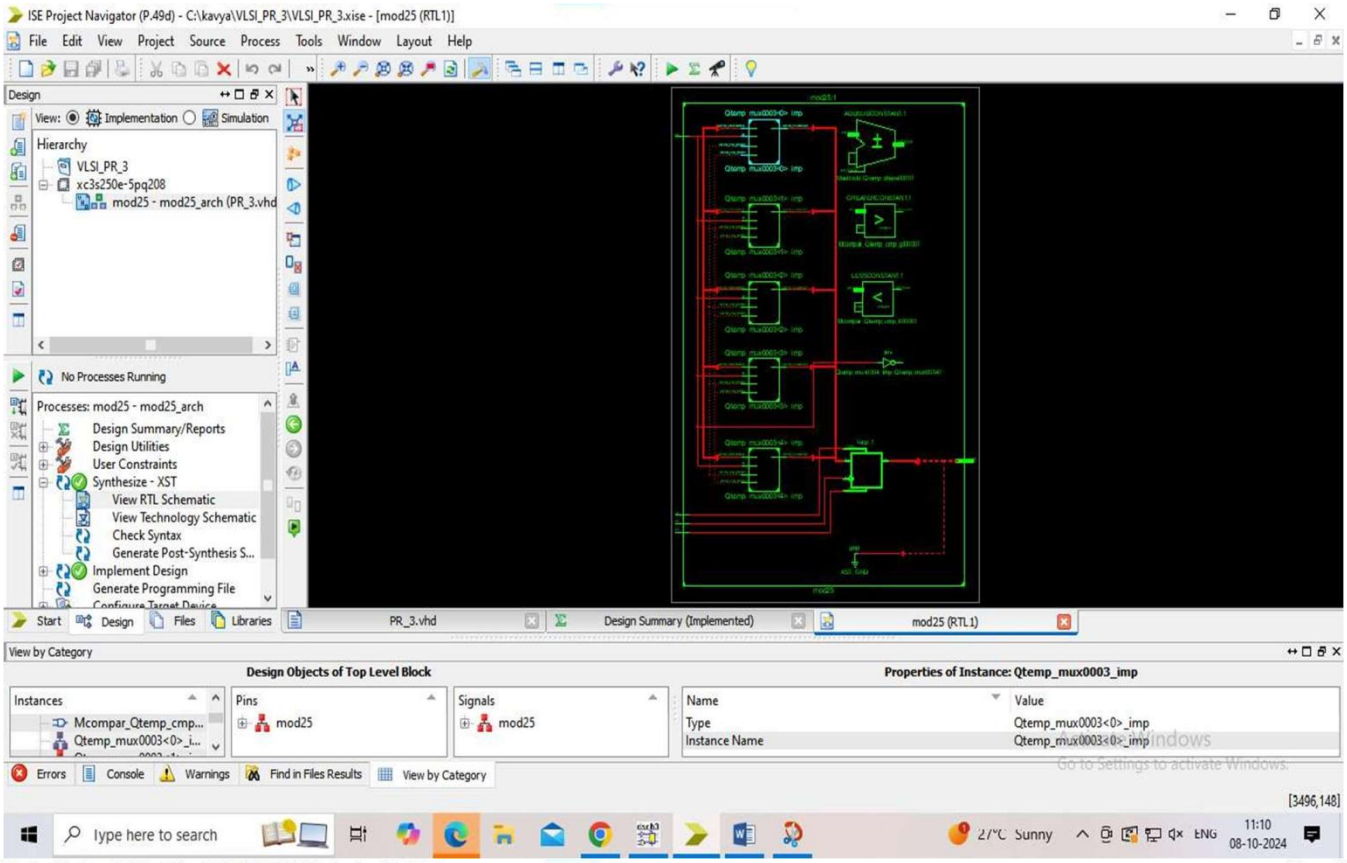
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY hhh IS
END hhh;

ARCHITECTURE behavior OF hhh IS

   -- Component Declaration for the Unit Under Test (UUT)

   COMPONENT modncount
PORT(
clk : IN  std_logic;
clr : IN  std_logic;
q : INOUT  std_logic_vector(2 downto 0)
      );
   END COMPONENT;


  --Inputs
signalclk : std_logic := '0';
signalclr : std_logic := '0';

  --BiDirs
signal q : std_logic_vector(2 downto 0);

  -- Clock period definitions
--   constantclk_period : time := 10 ns;

BEGIN

 -- Instantiate the Unit Under Test (UUT)
uut: modncount PORT MAP (
clk =>clk,
clr =>clr,
q => q
      );

  -- Clock process definitions
clk_process :process
begin
                    clk<= '0';
                    wait for 10 ns;
                    clk<= '1';
                    wait for 10 ns;
end process;


  -- Stimulus process
```

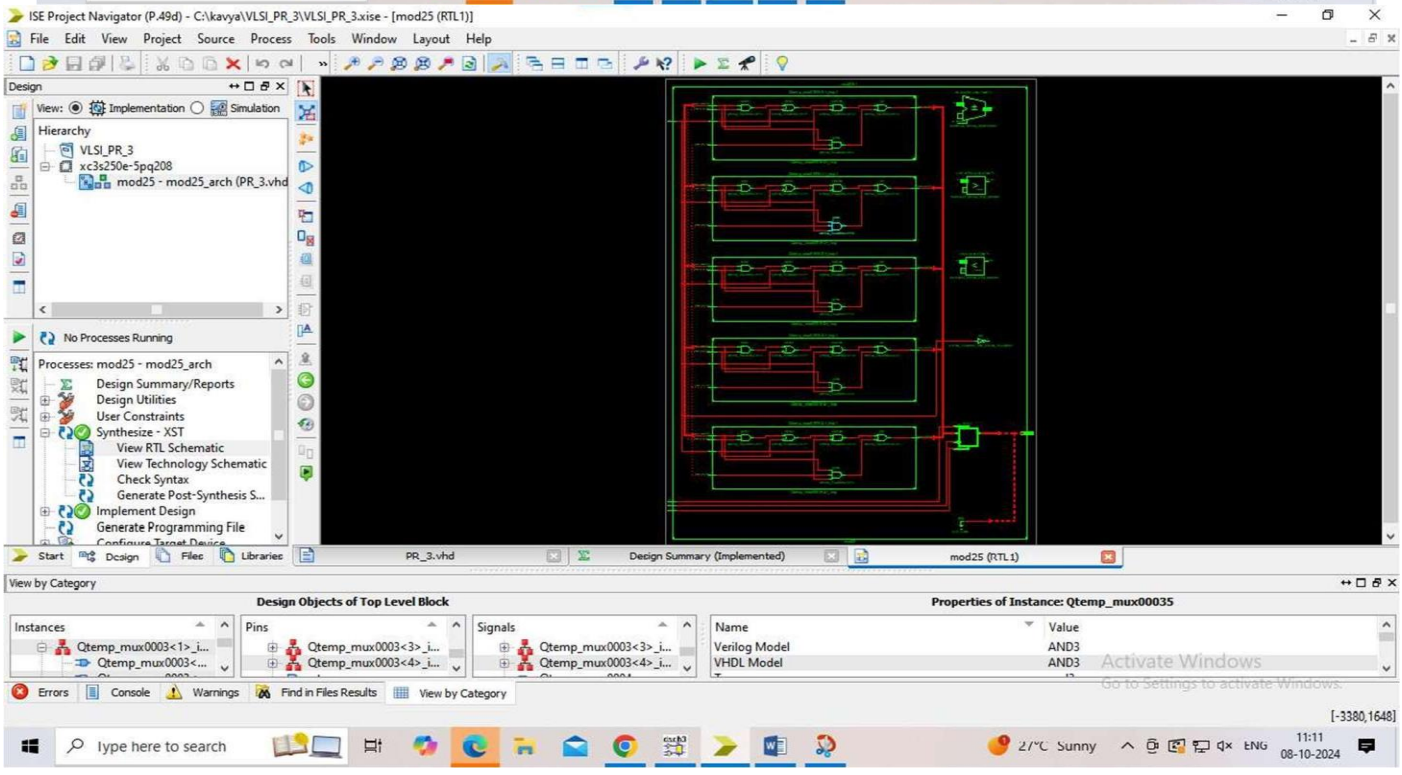
```
stim_proc: process
begin
        clr<='1';
    -- hold reset state for 100 ns.
wait for 20 ns;
                clr<='0';
    -- hold reset state for 100 ns.
wait for 20 ns;
    -- hold reset state for 100 ns.
--    wait for 100 ns;
--
--    wait for clk_period*10;

    -- insert stimulus here

wait;
end process;

END;
```

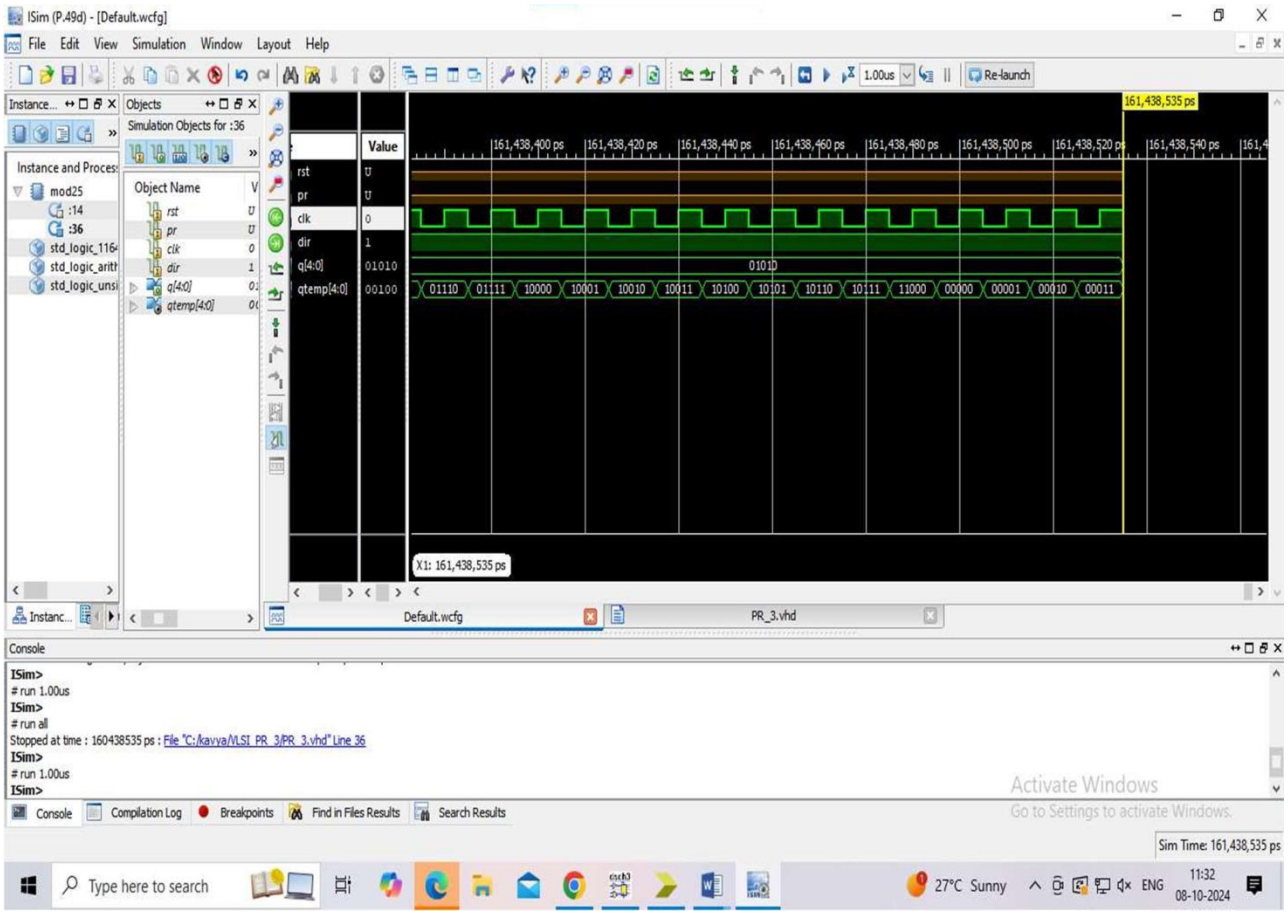
UCF

```
Net clkloc=”p182”;
Net clrloc=”p102”;
Net q(2) loc=”p165”;
Net q(2) loc=”p166”;
Net q(2) loc=”p167”;
```




ISE Project Navigator (P.49d) - C:\kavya\VLSI_PR_3\VLSI_PR_3.xise - [mod25 (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
VLSI_PR_3
xc3s250e-5pq208
mod25 - mod25_arch (PR_3.vhd
No Processes Running
Processes: mod25 - mod25_arch
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis S...
Implement Design
Generate Programming File
Start Design Files Libraries
PR_3.vhd
Design Summary (Implemented)
mod25 (RTL1)
View by Category
Design Objects of Top Level Block
Properties of Instance: Qtemp_mux0003_imp
Instances
Mcompar_Qtemp_cmp...
Qtemp_mux0003<0>_i...
Pins
mod25
Signals
mod25
Name
Value
Type
Qtemp_mux0003<0>_imp
Instance Name
Qtemp_mux0003<0>_imp
Errors Console Warnings Find in Files Results View by Category
[3496,148]
Type here to search
27°C Sunny
ENG
11:10
08-10-2024


ISE Project Navigator (P.49d) - C:\kavya\VLSI_PR_3\VLSI_PR_3.xise - [mod25 (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
VLSI_PR_3
xc3s250e-5pq208
mod25 - mod25_arch (PR_3.vhd
No Processes Running
Processes: mod25 - mod25_arch
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis S...
Implement Design
Generate Programming File
Start Design Files Libraries
PR_3.vhd
Design Summary (Implemented)
mod25 (RTL1)
View by Category
Design Objects of Top Level Block
Properties of Instance: Qtemp_mux00035
Instances
Qtemp_mux0003<1>_i...
Qtemp_mux0003<...
Pins
Qtemp_mux0003<3>_i...
Qtemp_mux0003<4>_i...
Signals
Qtemp_mux0003<3>_i...
Qtemp_mux0003<4>_i...
Name
Value
Verilog Model
AND3
VHDL Model
AND3
Errors Console Warnings Find in Files Results View by Category
[-3380,1648]
Type here to search
27°C Sunny
ENG
11:11
08-10-2024


ISim (P.49d) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Objects
Simulation Objects for :36
Object Name
rst
pr
clk
dir
q[4:0]
qtemp[4:0]
Value
161,438,535 ps
161,438,400 ps
161,438,420 ps
161,438,440 ps
161,438,460 ps
161,438,480 ps
161,438,500 ps
161,438,520 ps
161,438,540 ps
01010
01110 01111 10000 10001 10010 10011 10100 10101 10110 10111 11000 00000 00001 00010 00011
X1: 161,438,535 ps
Default.wcfg
PR_3.vhd
Console
ISim>
run 1.00us
ISim>
run all
Stopped at time : 160438535 ps : File "C:/kavya/VLSI_PR_3/PR_3.vhd" Line 36
ISim>
run 1.00us
ISim>
Activate Windows
Go to Settings to activate Windows.
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 161,438,535 ps
Type here to search
27°C Sunny
ENG
11:32
08-10-2024

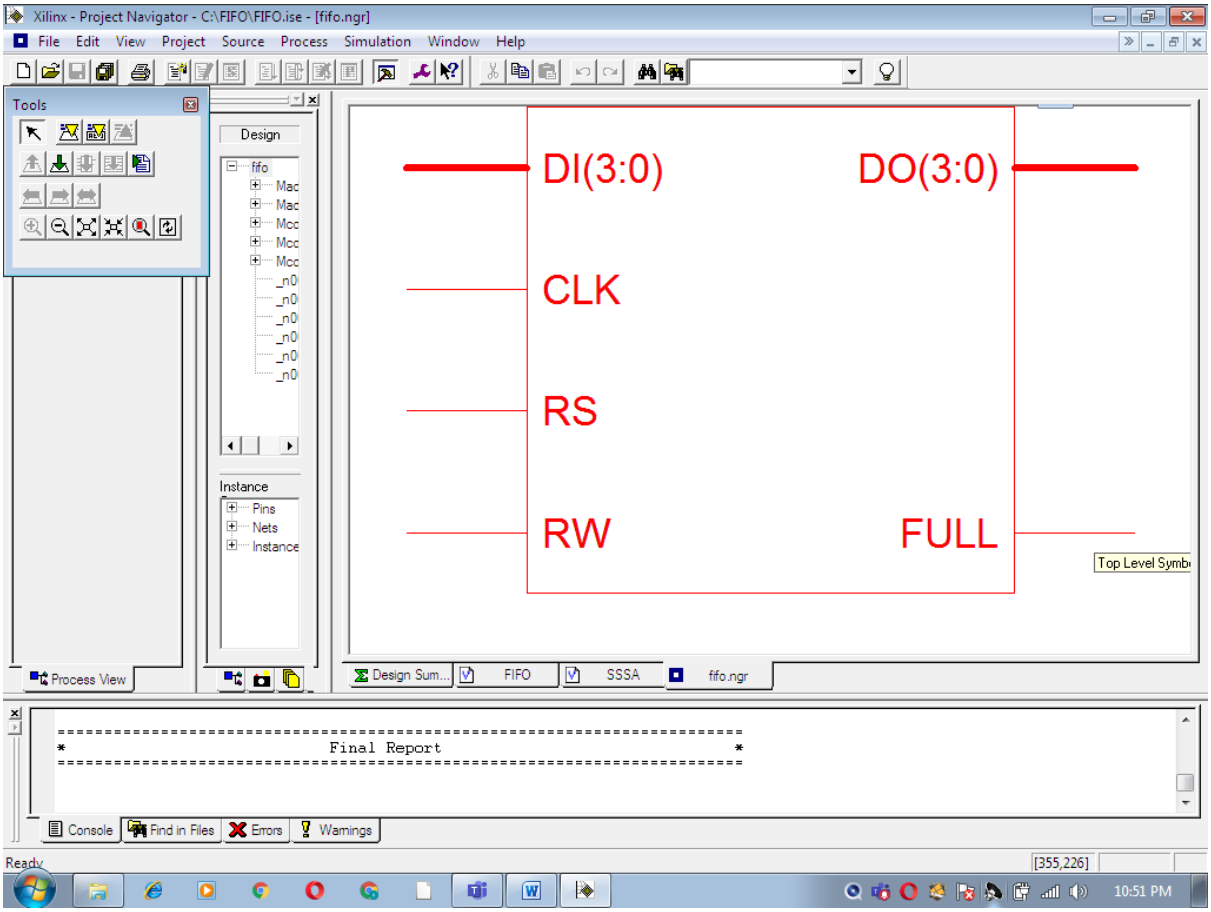
Experiment 4

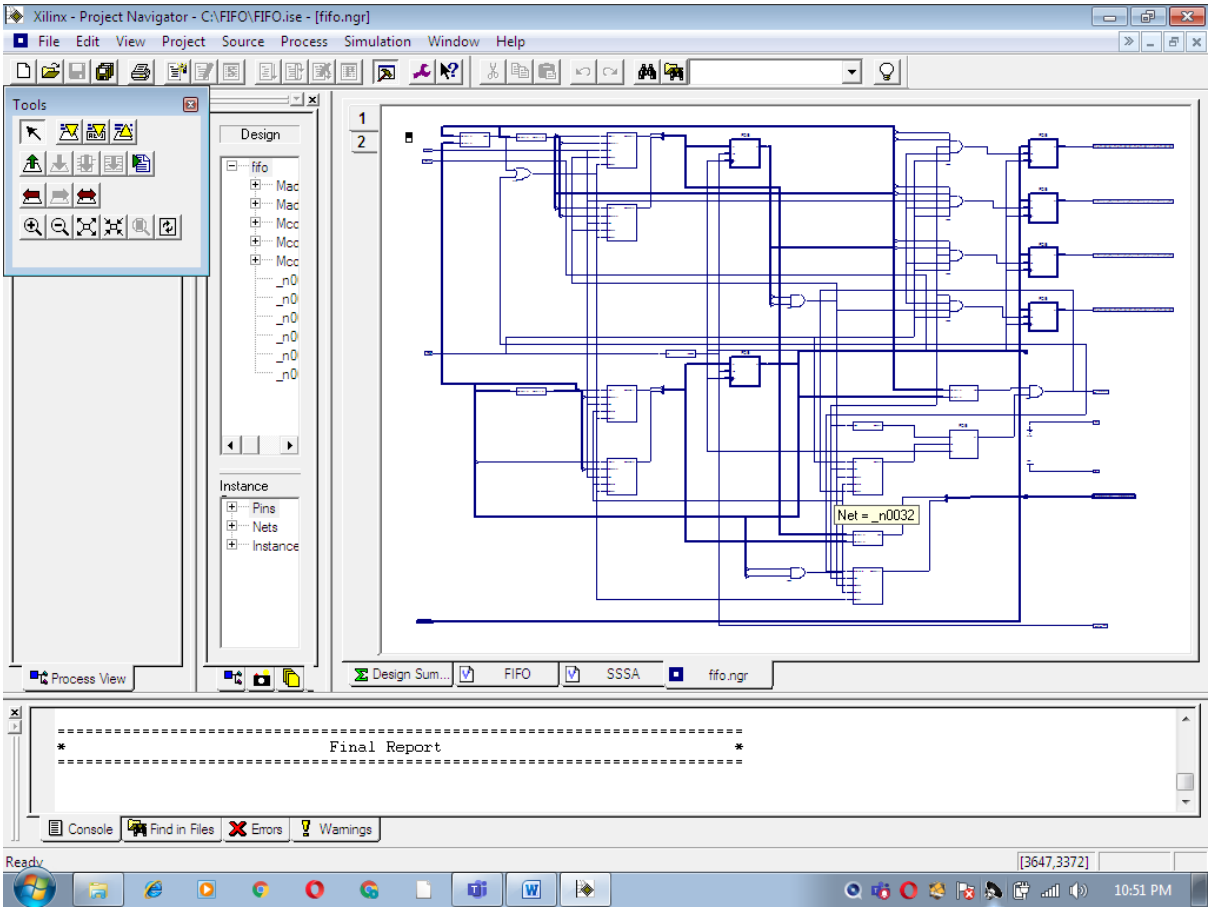
Name: Atharva Dhobale
Roll no: E43001
Division: BE 3 **Batch:** B9

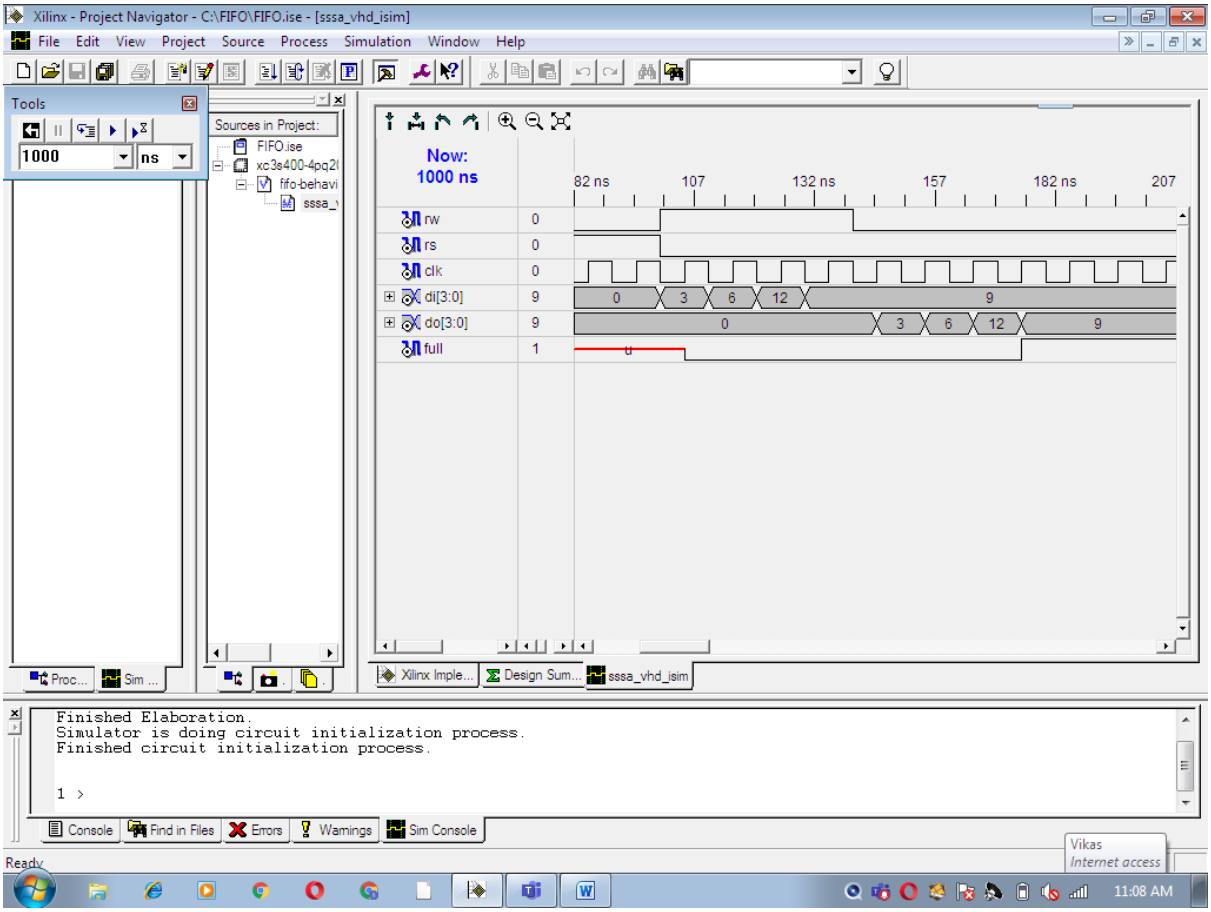
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity FIFO is
   Port ( DI : in std_logic_vector(3         downto 0);
DO : out std_logic_vector(3       downto 0);
RW : in std_logic;
FULL : out std_logic;
RS : in std_logic;
CLK : in std_logic);
end FIFO;

architecture Behavioral of FIFO is

begin

process(RS,CLK)
        type memory is Array( 0         to        3)of      std_logic_vector(3        downto 0);
                        variablemem: memory;

                        variable  r_p:integer range 0      to        3;
                        variable  w_p:integer range 0      to        3;
                        variable  overwrite :boolean;
begin
if RS='1' then
DO<="0000";
elsif(CLK'event and CLK='1') then
if  RW='1'then

                        if  (overwrite=False OR w_p/=r_p) then
                        mem (w_p):=DI;
                                ifw_p=3  then
                                        w_p:=0 ;
                                        else

                                        w_p:=w_p+1;
                                        overwrite:=False;
                                end if;
                                        end if;
elseif    RW='0' then

                                if        (overwrite=False OR w_p/=r_p) then
                DO<=mem(r_p);
                                if (r_p=3 ) then
                                        r_p:=0 ;
```

```
                                        overwrite:=true;
                                        else

                                        r_p:=r_p+1;

                                end if;
                        end if;
                        end if;

                        if      w_p=r_p         then

                        if overwrite=true then
                FULL<='1';

                        else
                                FULL<='0';

                        end if;

                                else
                                 FULL<='0';
                                end if;
                                end if;
                        end process;

end Behavioral;

ENTITY SSSA_vhd IS
END SSSA_vhd;

ARCHITECTURE behavior OF SSSA_vhd IS

        -- Component Declaration for the Unit Under Test (UUT)
        COMPONENT fifo
        PORT(
                DI : IN std_logic_vector(3 downto 0);
                RW : IN std_logic;
                RS : IN std_logic;
                CLK : IN std_logic;
                DO : OUT std_logic_vector(3 downto 0);
                FULL : OUT std_logic
                );
        END COMPONENT;


--Inputs
        SIGNAL RW :std_logic := '0';
        SIGNAL RS :std_logic := '0';
        SIGNAL CLK :std_logic := '0';
        SIGNAL DI :std_logic_vector(3 downto 0) := (others=>'0');

        --Outputs
        SIGNAL DO :std_logic_vector(3 downto 0);
        SIGNAL FULL :std_logic;
        constant        CLK_period : time := 10 ns;
```

```
BEGIN

	-- Instantiate the Unit Under Test (UUT)
	uut: fifo PORT MAP(
		DI => DI,
		DO => DO,
		RW => RW,
		FULL => FULL,
		RS => RS,
		CLK => CLK
	);
	process
	begin
		CLK<='0'	;
	wait for CLK_period/2;
			CLK<='1'	;
	wait for CLK_period/2;
	end process;



	tb : PROCESS
	BEGIN
		 RS<='1';
	wait for 100 ns;
	RS<='0';
	RW<='1';
	DI<="0011";
		-- Wait 100 ns for global reset to finish
		wait for 10 ns;
		RW<='1';
	DI<="0110";
		-- Wait 100 ns for global reset to finish
		wait for 10 ns;
                                                        RW<='1';
	DI<="1100";

		-- Wait 100 ns for global reset to finish
		wait for 10 ns;
		RW<='1';
	DI<="1001";

		-- Wait 100 ns for global reset to finish
		wait for 10 ns;
		-- Place stimulus here
                                        RW<='0';
		-- Wait 100 ns for global reset to finish
		wait for 10 ns;
		RW<='0';
		-- Wait 100 ns for global reset to finish
		wait for 10 ns;
		RW<='0';
		-- Wait 100 ns for global reset to finish
		wait for 10 ns;
		WAIT FOR CLK_period*10;
		wait; -- will wait forever
	END PROCESS;

END;
```


Xilinx - Project Navigator - C:\FIFO\FIFO.ise - [fifo.ngr]
File Edit View Project Source Process Simulation Window Help
Tools
Design
fifo
Instance
Pins
Nets
Instance
DI(3:0)
DO(3:0)
CLK
RS
RW
FULL
Top Level Symb
Process View
Design Sum...
FIFO
SSSA
fifo.ngr
Final Report
Console
Find in Files
Errors
Warnings
Ready
[355,226]
10:51 PM


Xilinx - Project Navigator - C:\FIFO\FIFO.ise - [fifo.ngr]
File Edit View Project Source Process Simulation Window Help
Tools
Design
fifo
Instance
Pins
Nets
Instance
1
2
Net = _n0032
Process View
Design Sum...
FIFO
SSSA
fifo.ngr
Final Report
Console
Find in Files
Errors
Warnings
Ready
[3647,3372]
10:51 PM



==========

* Final Report *

==========

Final Results
RTL Top Level Output File Name : fifo.ngr
Keep Hierarchy : NO

Design Statistics
IOs : 12

Cell Usage :
BELS : 2
GND : 1
VCC : 1
FlipFlops/Latches : 26
FDCE : 4
FDE : 22

==========

CPU : 5.92 / 8.26 s | Elapsed : 6.00 / 8.00 s

-->

Total memory usage is 122500 kilobytes

Number of errors : 0 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

Experiment 5

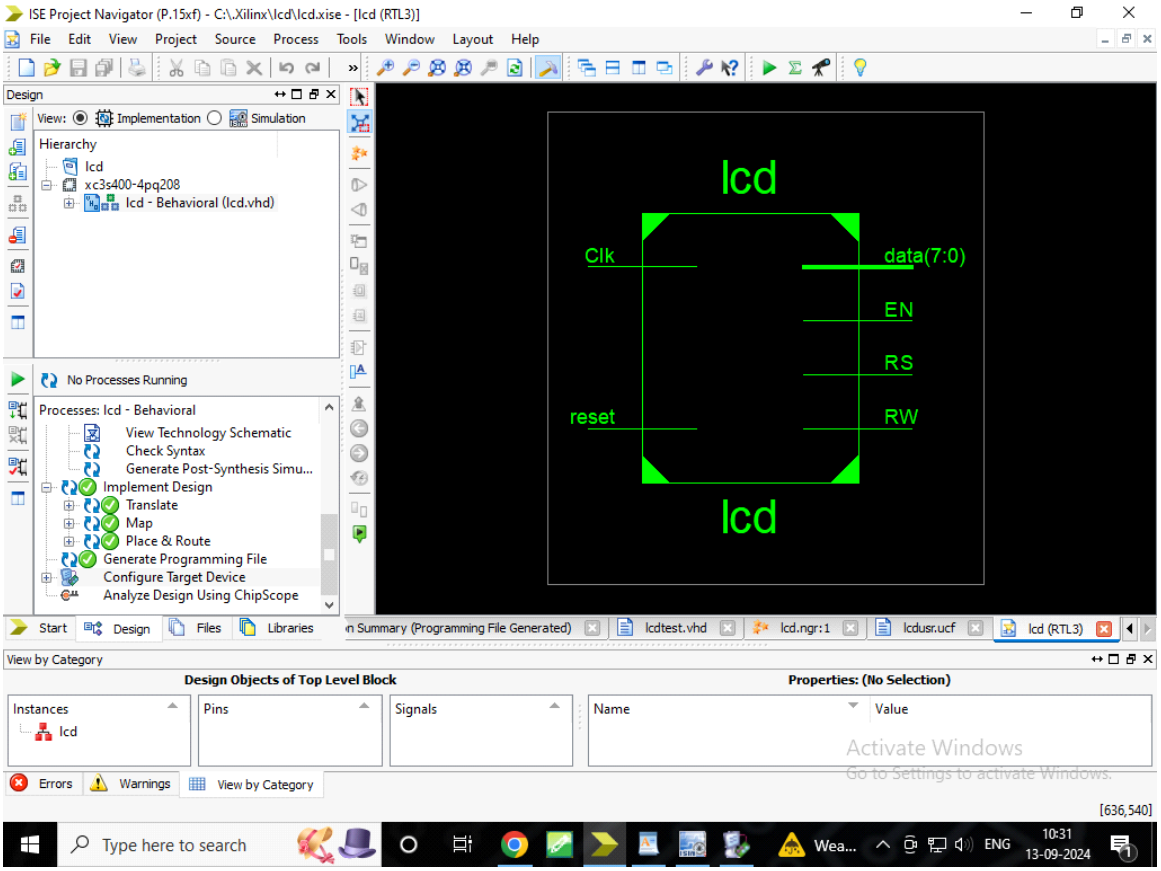
Name: Atharva Dhobale
Roll no: E43001
Division: BE 3 **Batch:** B9

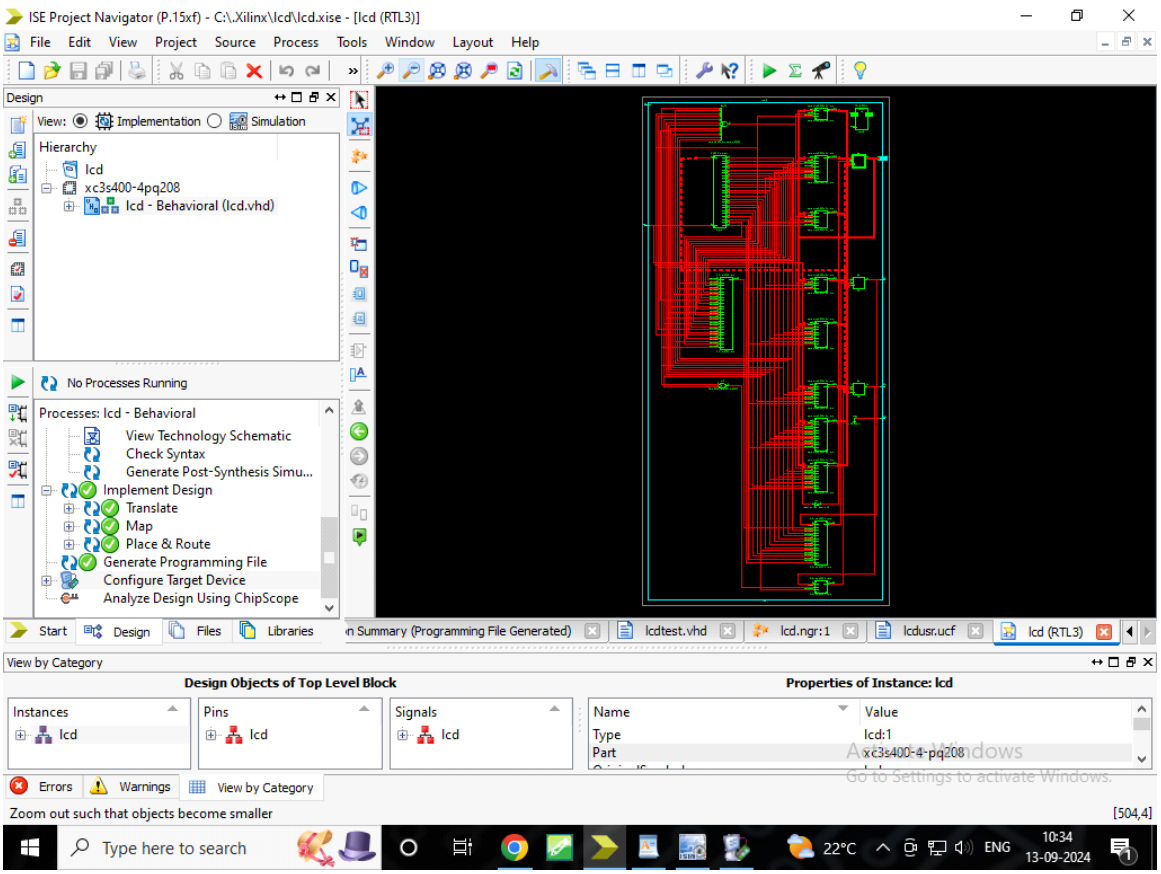
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity lcd is
   Port ( clk,reset : in std_logic;
        RS,EN,RW : out std_logic;
        data : out std_logic_vector(7 downto 0));
end lcd;
architecture Behavioral of lcd is
   type state_type is (s0,s1,s2,s3,s4,s5,s6,s7,s8,s9,s10,s11,
   s12,s13,s14,s15,s16,s17,s18,s19,s20,s21,s22,s23);
   signal state:state_type;
          SIGNAL count:std_logic_vector(22 downto 0);
   SIGNAL clk1:std_logic;
begin
process(Clk,Reset)
          begin
                    if(Clk' event AND Clk='1')then
                    count<=count+"0001";
                    end if;
                    clk1<=count(20);
                    end process;
RW<='0';
          process(clk1, reset)
          begin
            if reset = '1' then
                              state <= s0;
                    elsif rising_edge(clk1) then
                              if state = s0 then
                                        state <= s1;
                                        RS<='0'; -- Write commonds to LCD.
                                        EN <= '1';
                                        data <= "00110000"; -- Function set for 8 bit interface, 1 line mode and
5x7 dot matrix.
                              end if;
                              if state = s1 then
                                        state <= s2;
                                        EN <= '0';
                              end if;
                              if state = s2 then
                                        state <= s3;
```

```
                EN <= '1';
                data <= "00001111"; -- Display cursor and blinking ON.
        end if;
        if state = s3 then
                state <= s4;
                EN <= '0';
        end if;
        if state = s4 then
                state <= s5;
                EN <= '1';
                data <= "00000001";      -- Clear display.
        end if;
        if state = s5 then
                state <= s6;
                EN <= '0';
        end if;
        if state = s6 then
                state <= s7;
                EN <= '1';
                data <= "10000100"; -- Display address.
        end if;
        if state = s7 then
                state <= s8;
                EN <= '0';
        end if;
        if state = s8 then
                RS <= '1';  -- Write data to LCD.
                state <= s9;
                EN <= '1';
                data <= "00101010"; --(*)
        end if;
        if state = s9 then
                state <= s10;
                EN <= '0';
        end if;
if state = s10 then
                state <= s11;
                EN <= '1';
                data <= "01010011"; --S
        end if;
        if state = s11 then
                state <= s12;
                EN <= '0';
        end if;
        if state = s12 then
                state <= s13;
                EN <= '1';
                data <= "01001011"; --K
```

```
end if;
if state = s13 then
        state <= s14;
        EN <= '0';
end if;
if state = s14 then
        state <= s15;
        EN <= '1';
        data <= "01001110"; --N
end if;
if state = s15 then
        state <= s16;
        EN <= '0';
end if;
if state = s16 then
        state <= s17;
        EN <= '1';
        data <= "01000011"; --C
end if;
if state = s17 then
        state <= s18;
        EN <= '0';
end if;
 if state = s18 then
        state <= s19;
        EN <= '1';
        data <= "01001111"; --O
end if;
if state = s19 then
        state <= s20;
        EN <= '0';
end if;
if state = s20 then
        state <= s21;
        EN <= '1';
        data <= "01000101"; --E
end if;
if state = s21 then
        state <= s22;
        EN <= '0';
end if;
if state = s22 then
        state <= s23;
        EN <= '1';
        data <= "00101010"; --(*)
end if;
if state = s23 then
        EN <= '0';
```

```
                    end if;
                end if;
            end process;
end Behavioral;
```

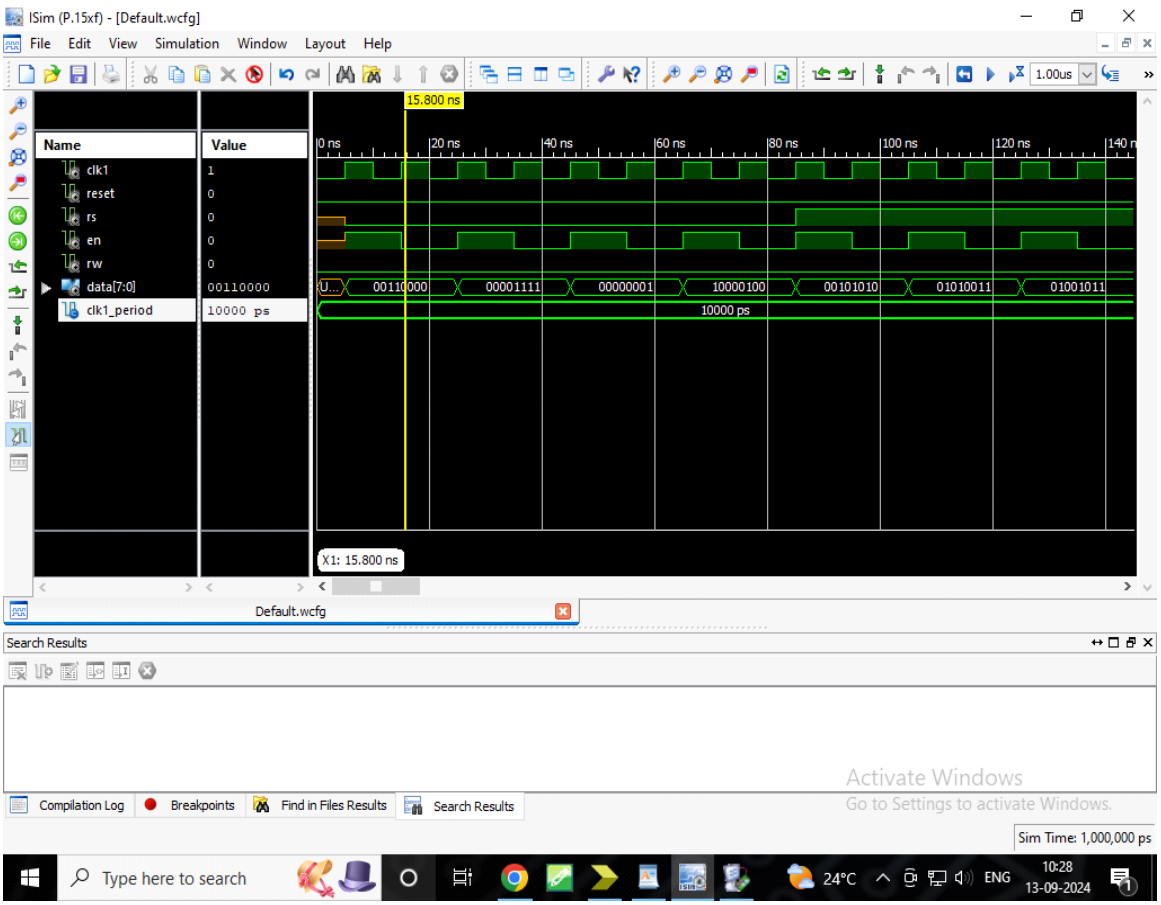




Testbench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;
ENTITY lcdtest IS
END lcdtest;
ARCHITECTURE behavior OF lcdtest IS
   -- Component Declaration for the Unit Under Test (UUT)
   COMPONENT lcd
   PORT(
        clk1 : IN  std_logic;
        reset : IN  std_logic;
        RS : OUT  std_logic;
        EN : OUT  std_logic;
        RW : OUT  std_logic;
```

```
        data : OUT  std_logic_vector(7 downto 0)
       );
   END COMPONENT;

  --Inputs
  signal clk1 : std_logic := '0';
  signal reset : std_logic := '0';
          --Outputs
  signal RS : std_logic;
  signal EN : std_logic;
  signal RW : std_logic;
  signal data : std_logic_vector(7 downto 0);
  -- Clock period definitions
  constant clk1_period : time := 10 ns;
BEGIN
          -- Instantiate the Unit Under Test (UUT)
  uut: lcd PORT MAP (
       clk1 => clk1,
       reset => reset,
       RS => RS,
       EN => EN,
       RW => RW,
       data => data
      );
  -- Clock process definitions
  clk1_process :process
  begin
                    clk1 <= '0';
                    wait for clk1_period/2;
                    clk1 <= '1';
                    wait for clk1_period/2;
  end process;
  -- Stimulus process
  stim_proc: process
  begin
    -- hold reset state for 100 ns.

                                reset<='0';
    wait for clk1_period*10;
    -- insert stimulus here
    wait;
  end process;
END;
```



UCF:

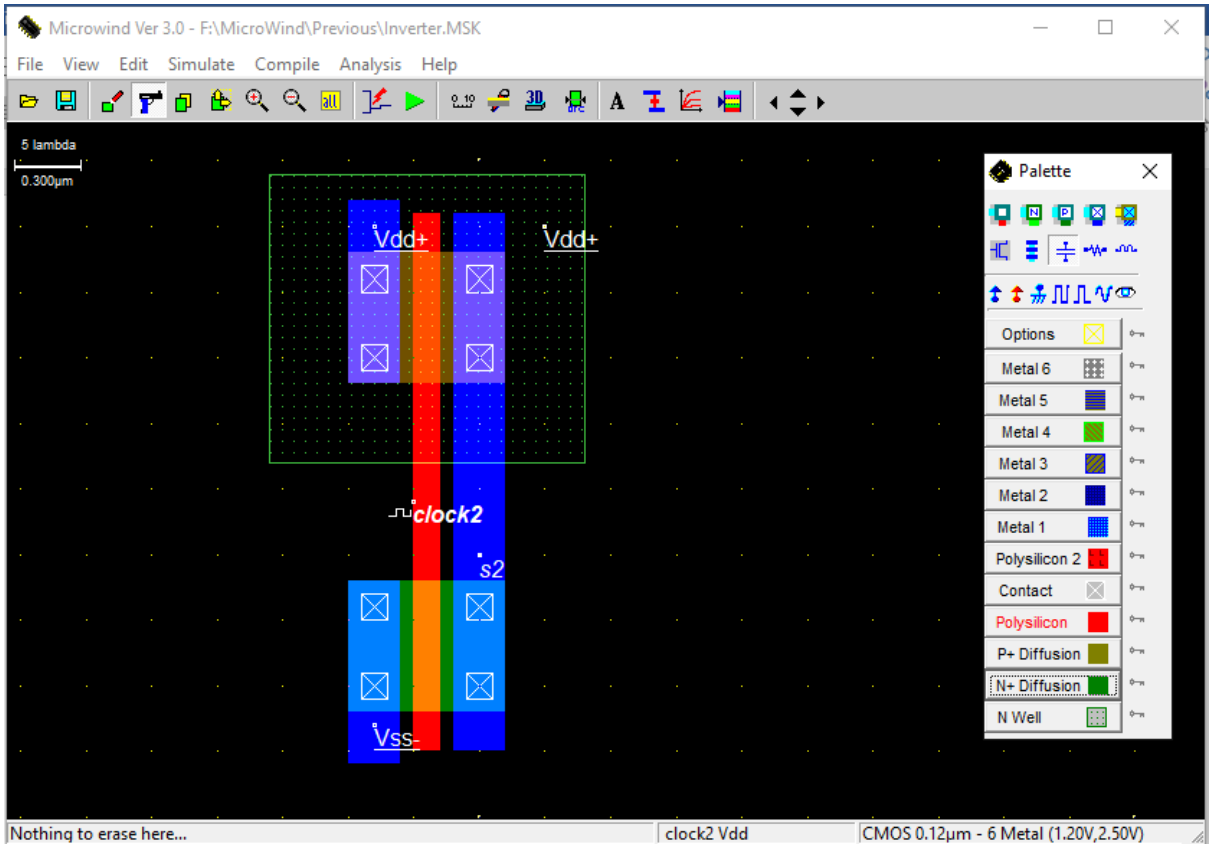
NET data(0) LOC =P62;
NET data(1) LOC =P63;
NET data(2) LOC =P64;
NET data(3) LOC =P65;
NET data(4) LOC =P67;
NET data(5) LOC =P68;
NET data(6) LOC =P71;
NET data(7) LOC =P72;
NET Clk LOC =P183;
NET reset LOC =P102;
NET RS LOC =P57;
NET EN LOC =P61;
NET RW LOC =P58;

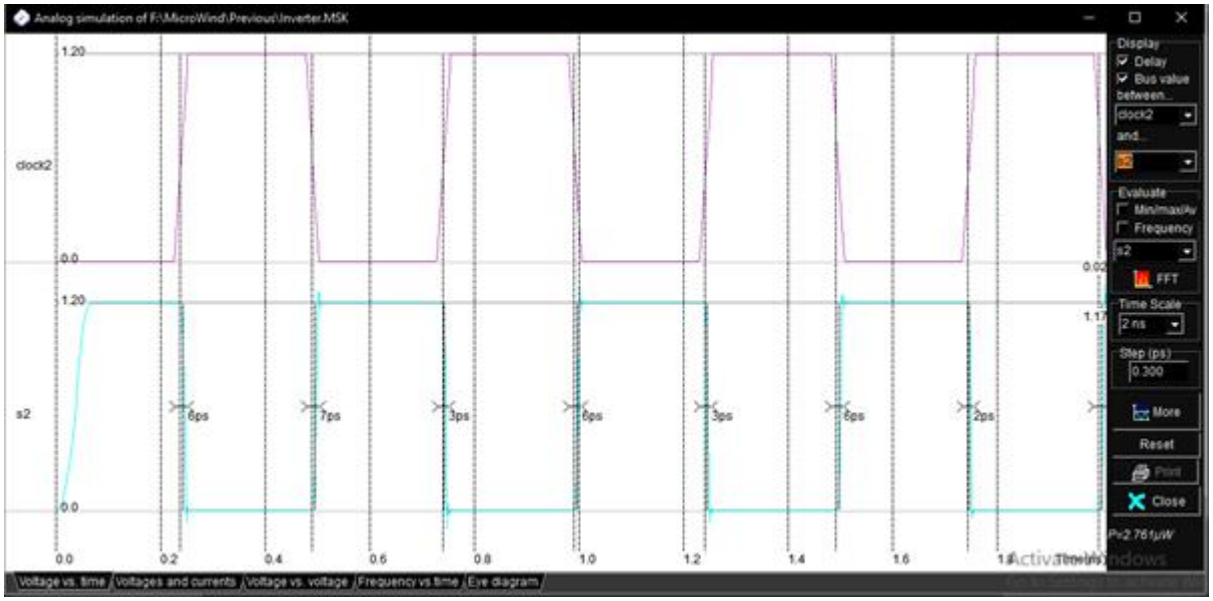
```
=========================================================================
*                      Final Report                     *
=========================================================================
Final Results
RTL Top Level Output File Name     : lcd.ngr
Top Level Output File Name         : lcd
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 13

Cell Usage :
# BELS                             : 92
#      GND                         : 1
#      INV                         : 2
#      LUT1                        : 20
#      LUT2                        : 1
#      LUT2_L                      : 3
#      LUT3                        : 3
#      LUT3_D                      : 1
#      LUT4                        : 14
#      LUT4_D                      : 1
#      LUT4_L                      : 4
#      MUXCY                       : 20
#      VCC                         : 1
#      XORCY                       : 21
# FlipFlops/Latches                : 55
#      FD                          : 21
#      FDC                         : 22
#      FDCE                        : 1
#      FDE                         : 10
#      FDP                         : 1
# Clock Buffers                    : 2
#      BUFG                        : 1
#      BUFGP                       : 1
# IO Buffers                       : 12
#      IBUF                        : 1
#      OBUF                        : 11
=========================================================================
Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 3.89 secs
-->
Total memory usage is 4509380 kilobytes
Number of errors   :    0 (   0 filtered)
Number of warnings :    3 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```

Name: Atharva Dhobale

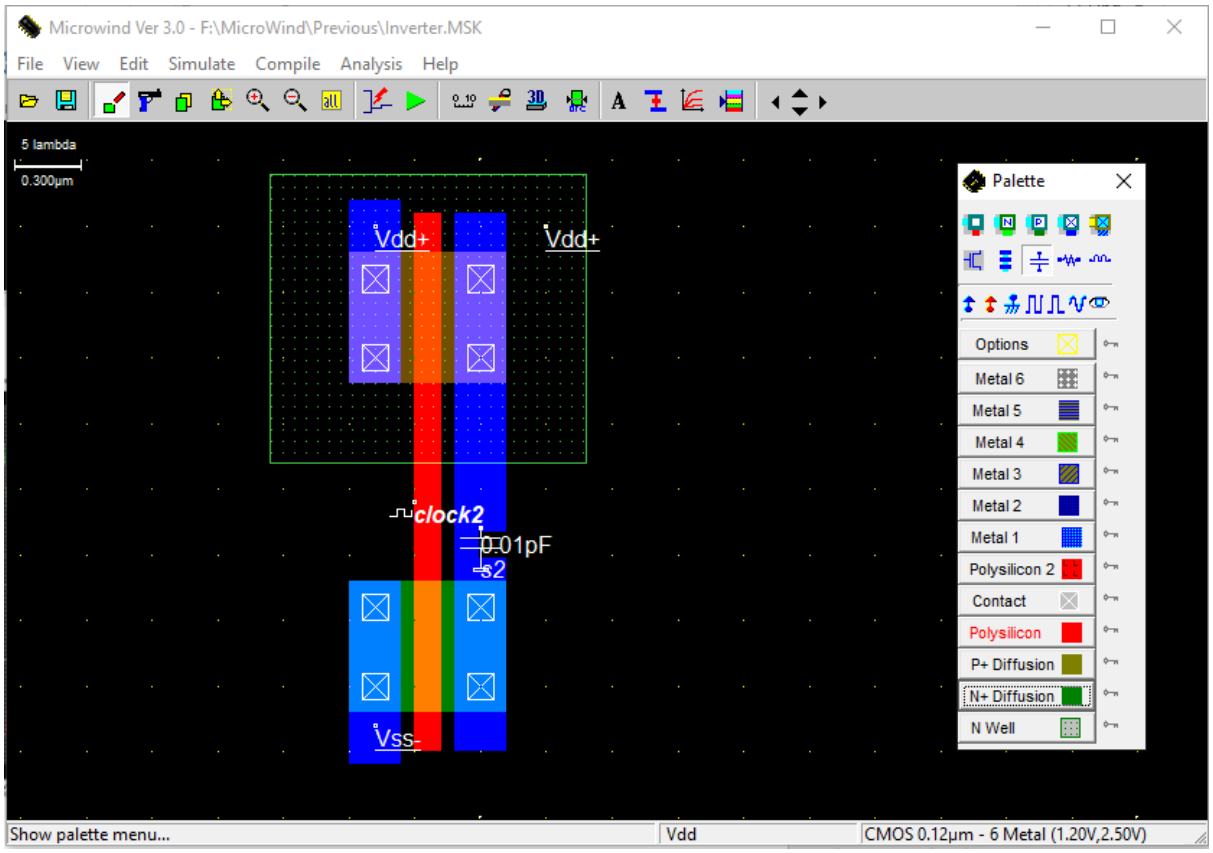
Roll No.: E43001 Batch: B9 Div: 3

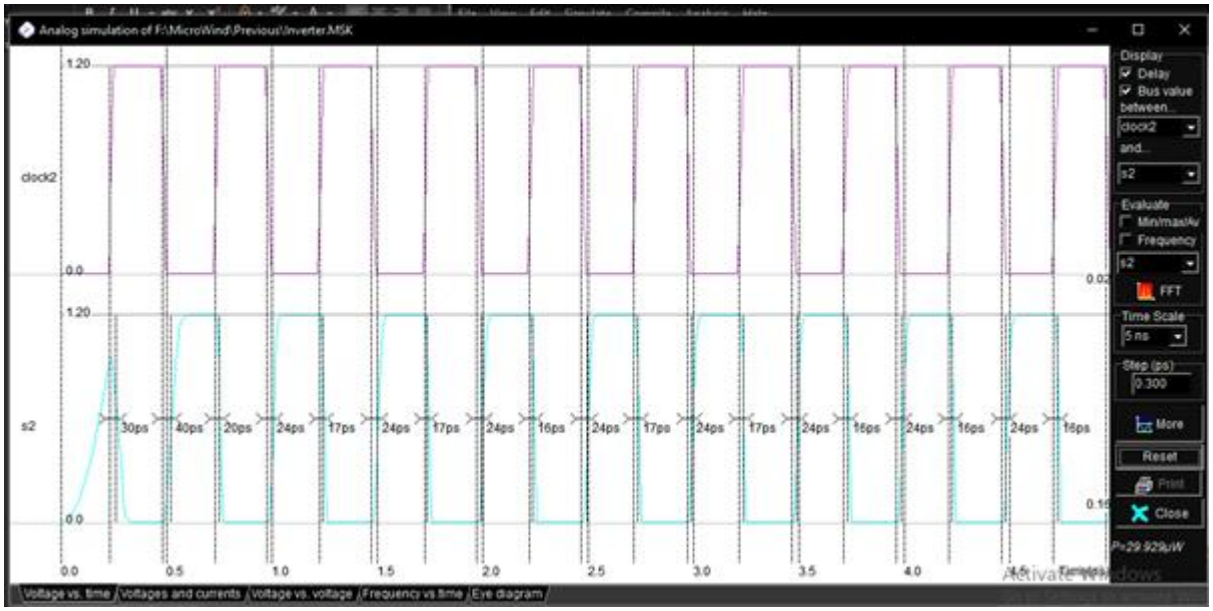
INVERTER





With Capacitor





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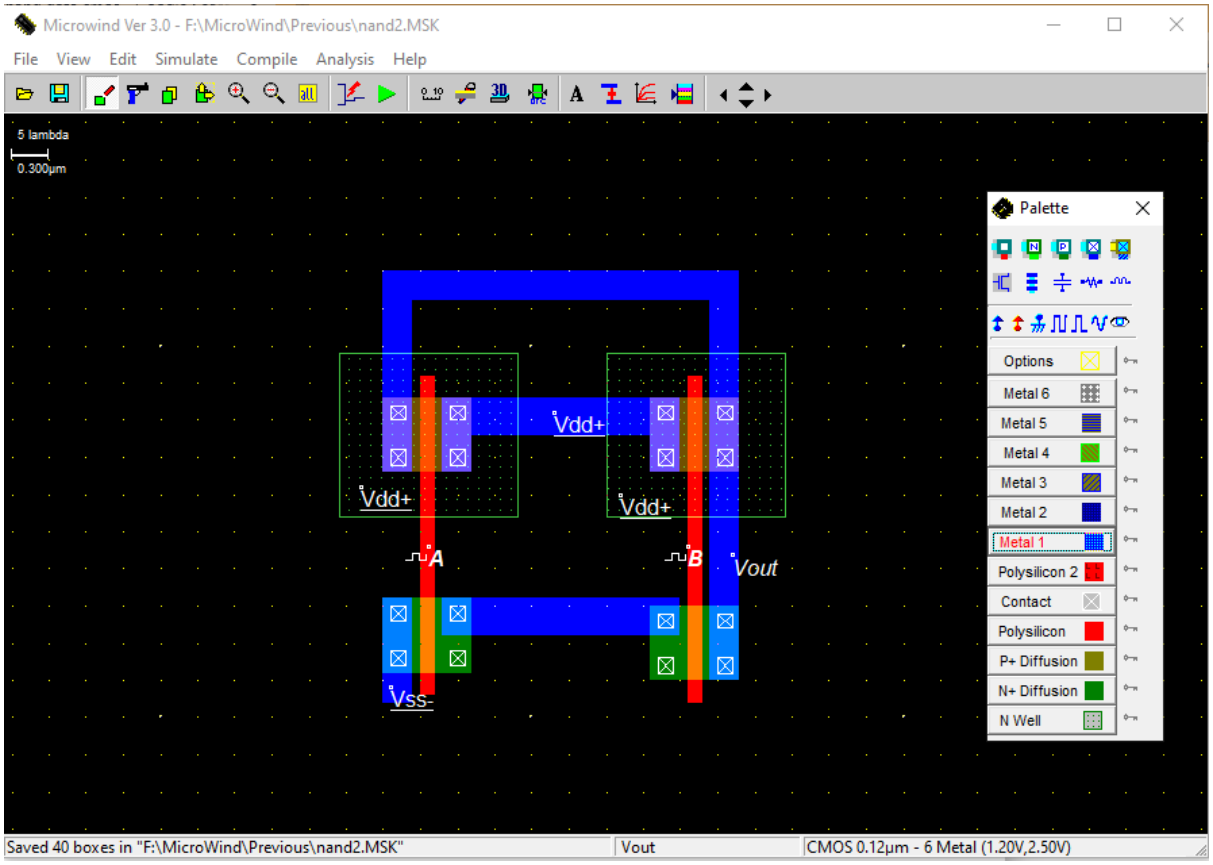
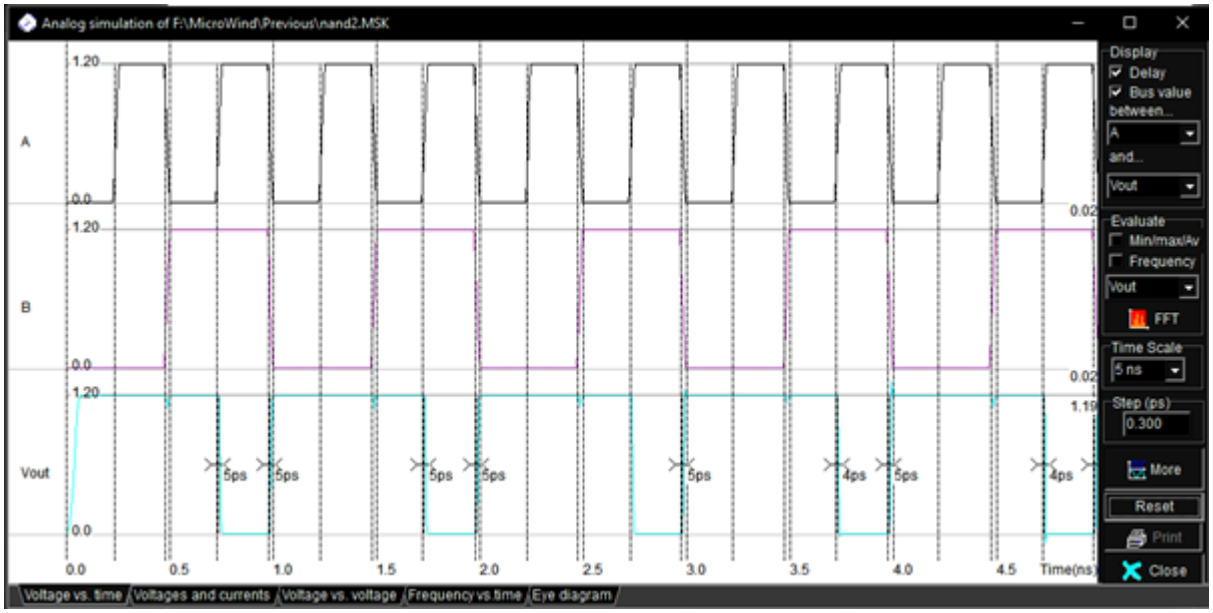
NAND





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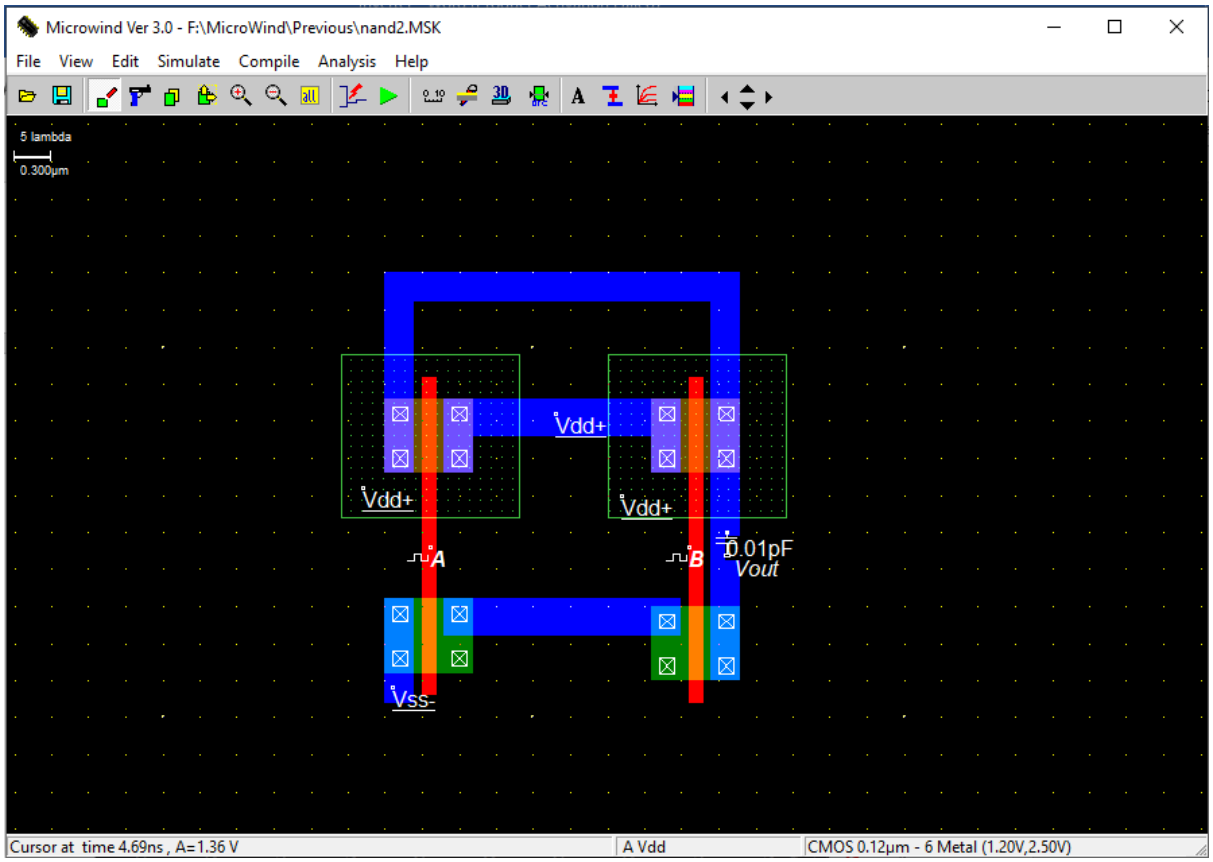

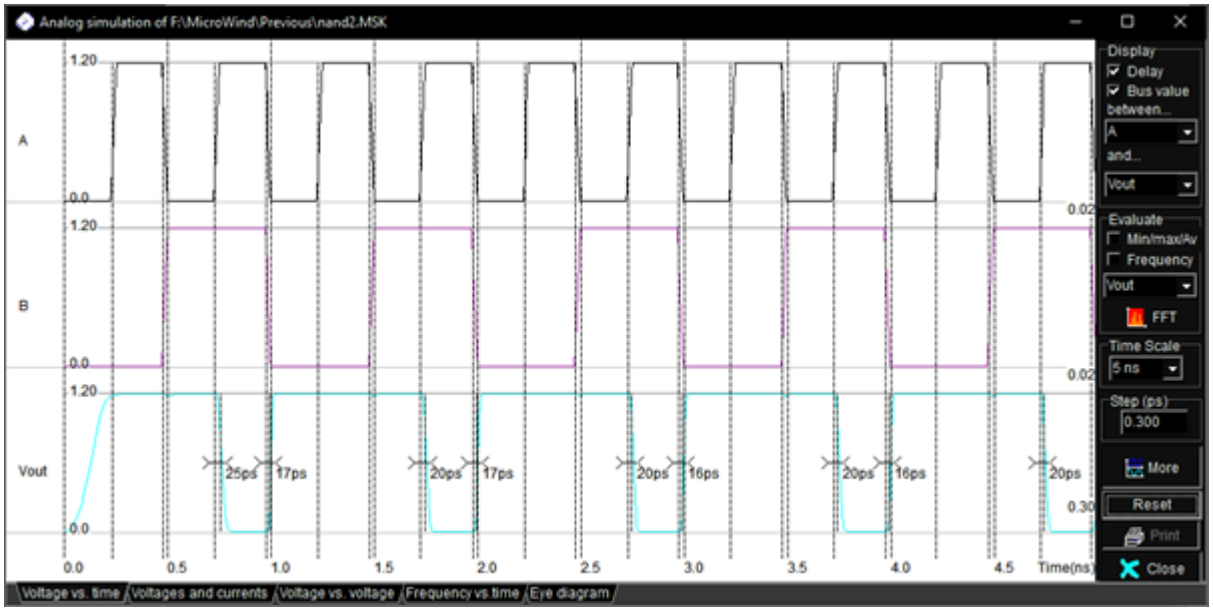

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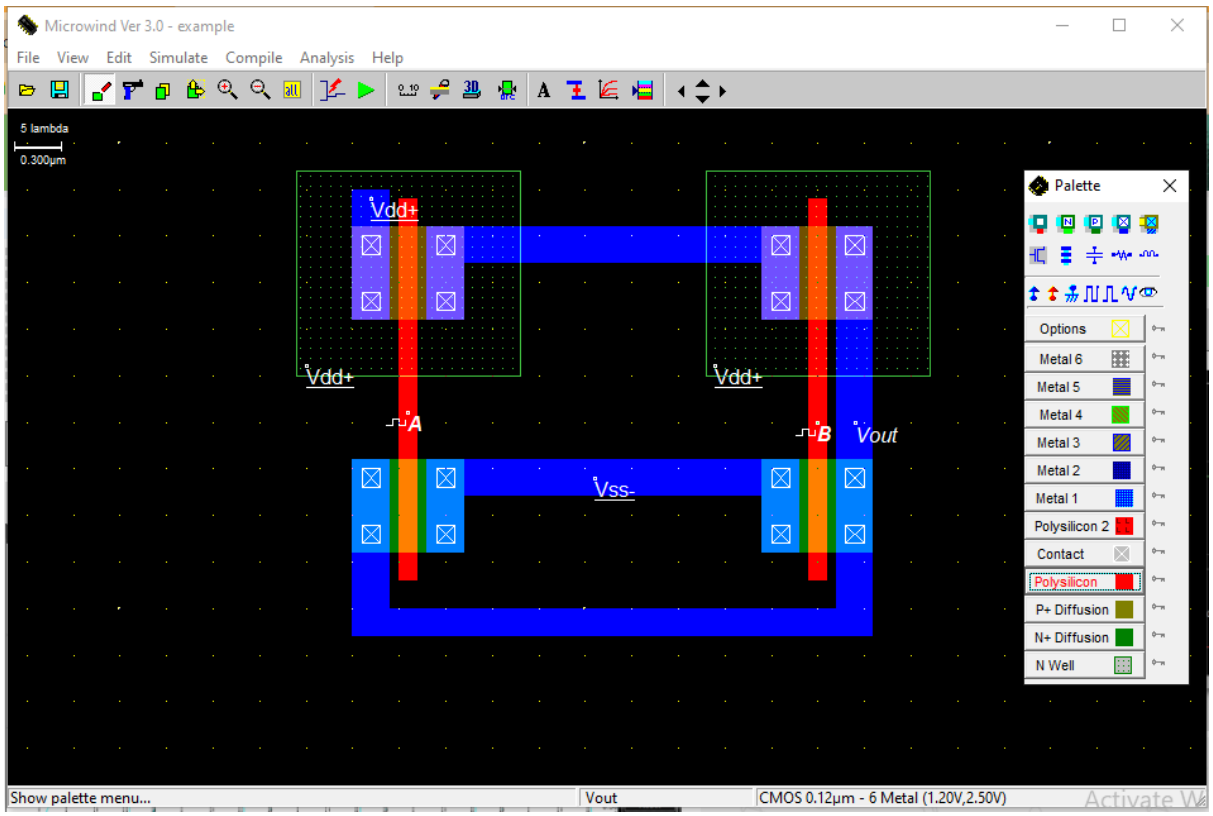
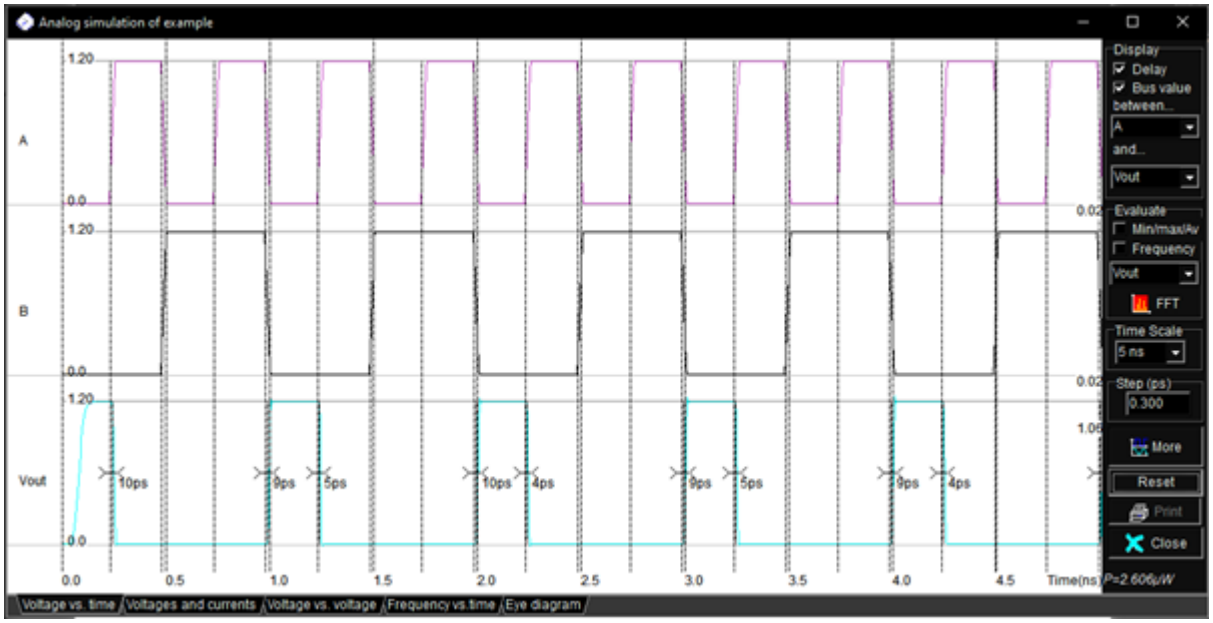
NOR





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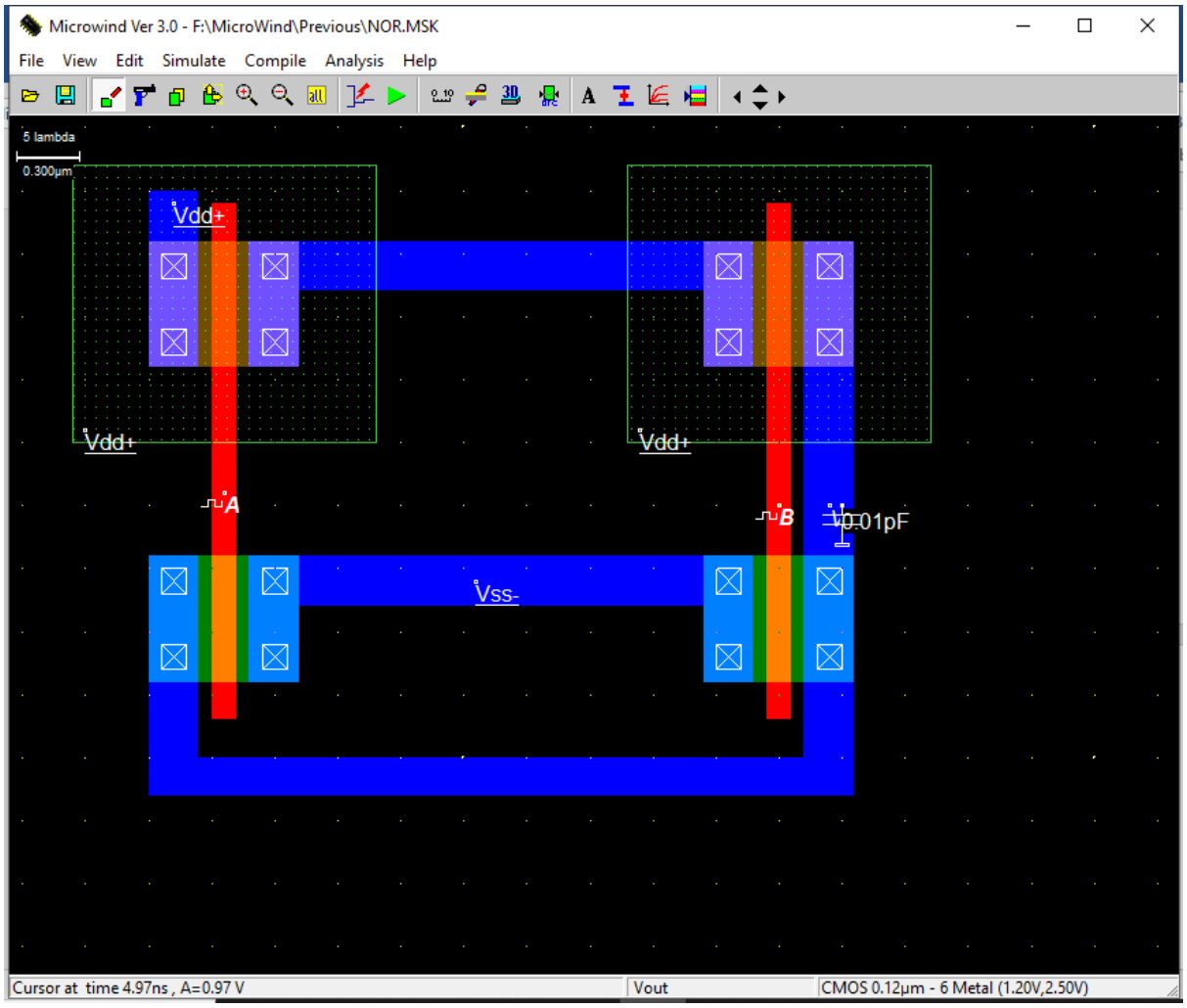

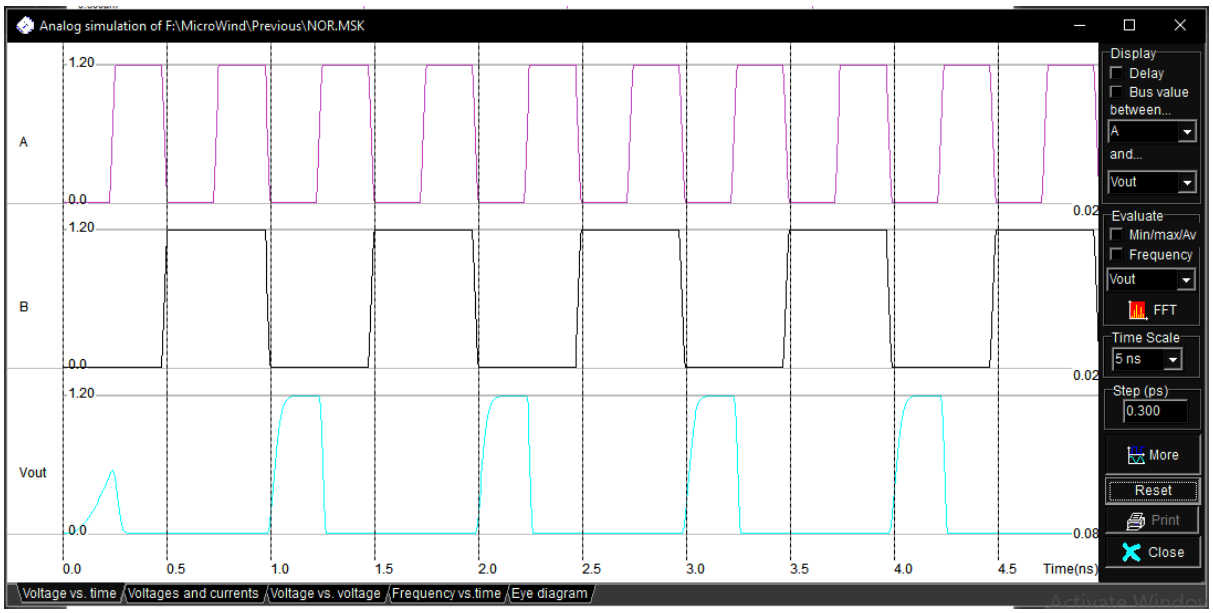

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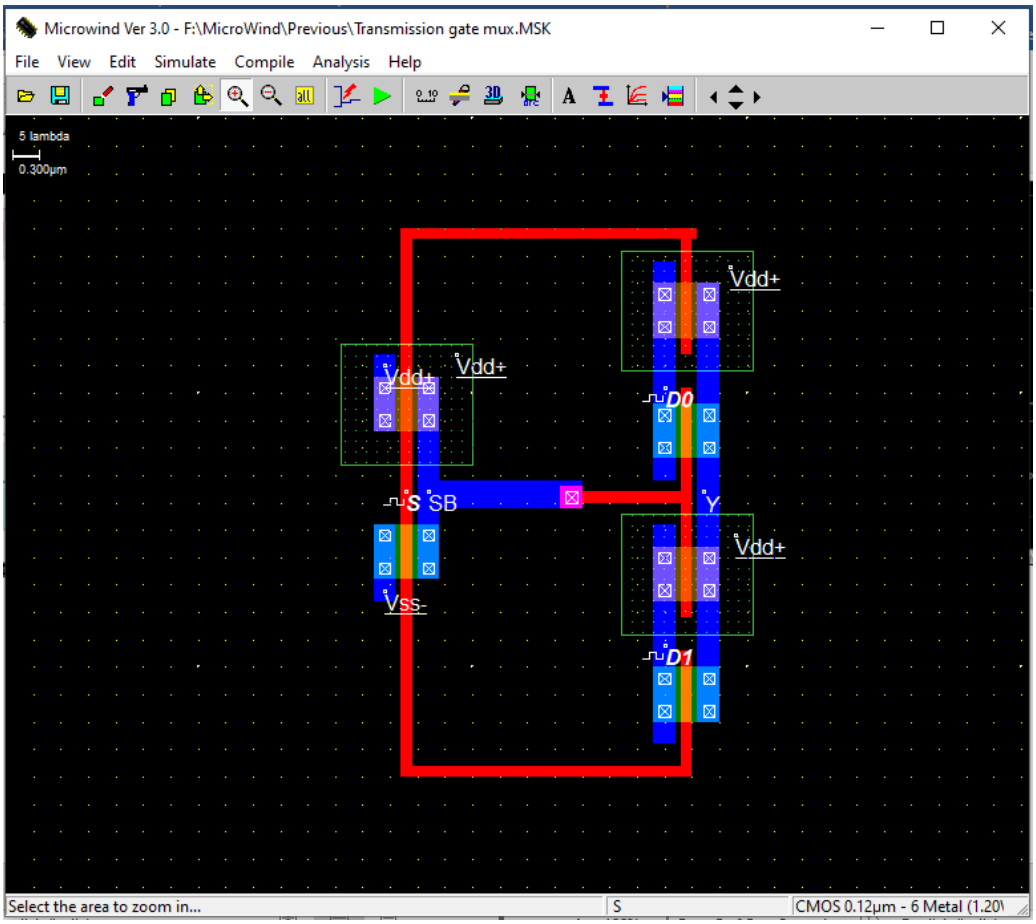
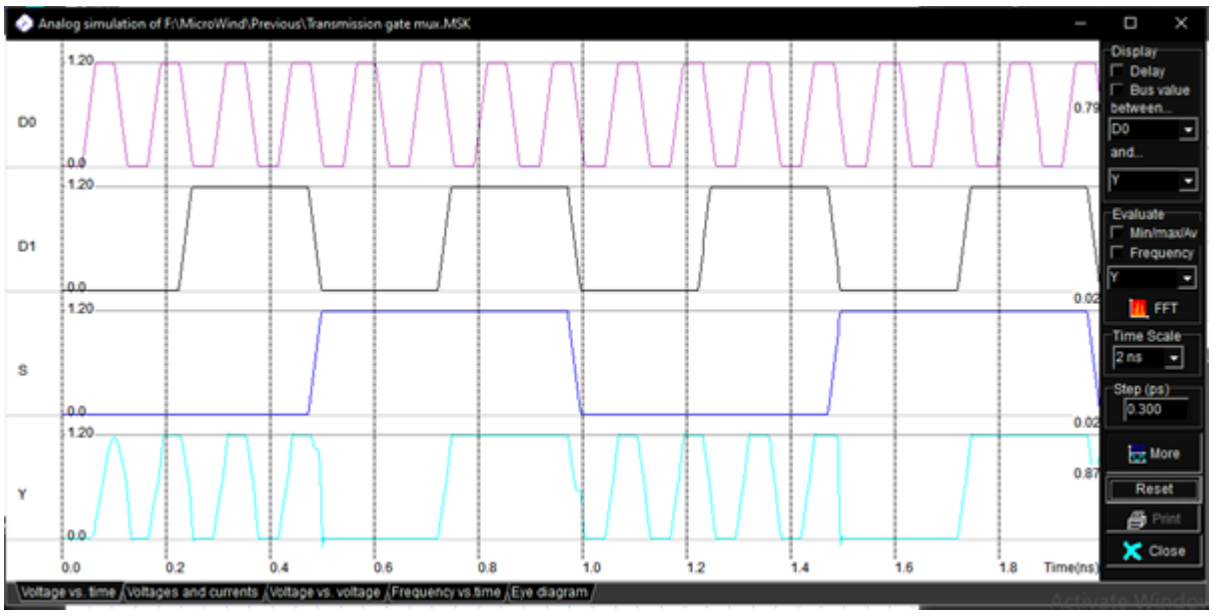
Mux 2:1 using Transmission gate





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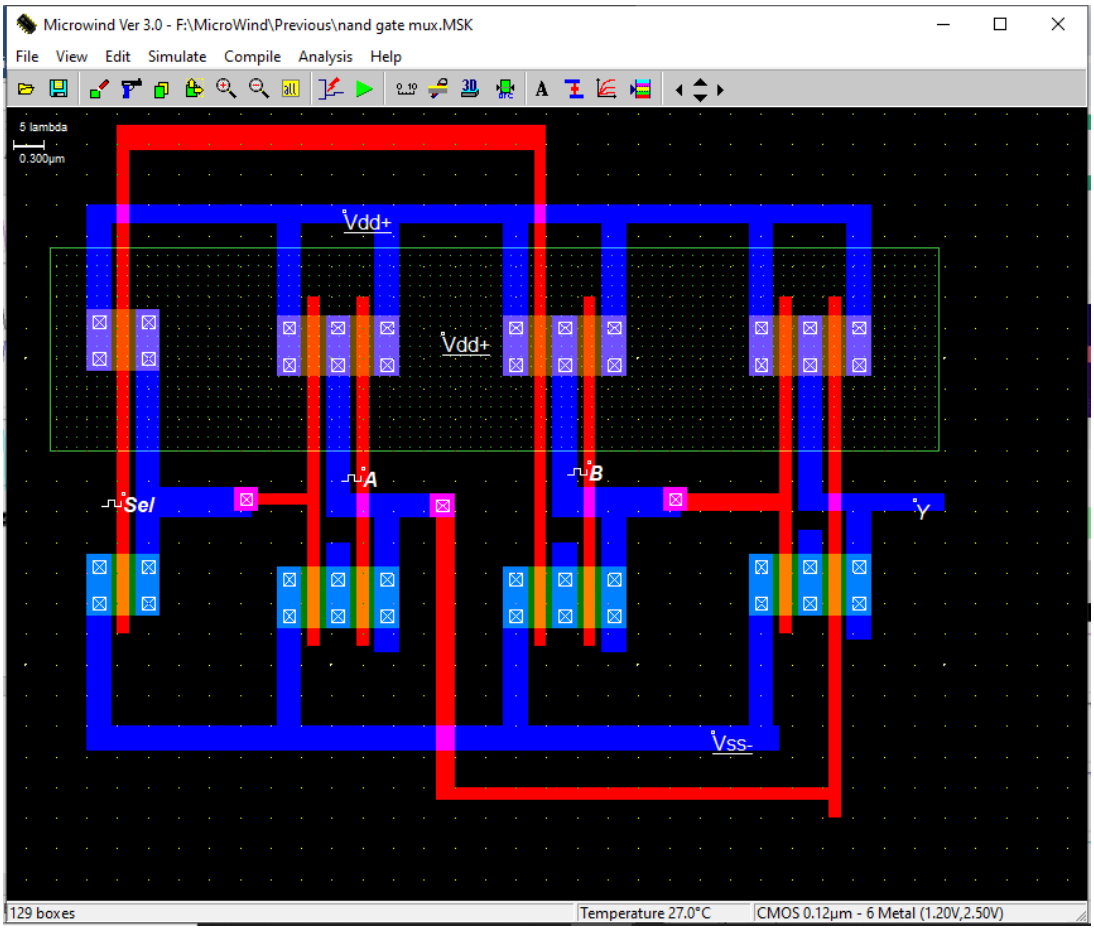
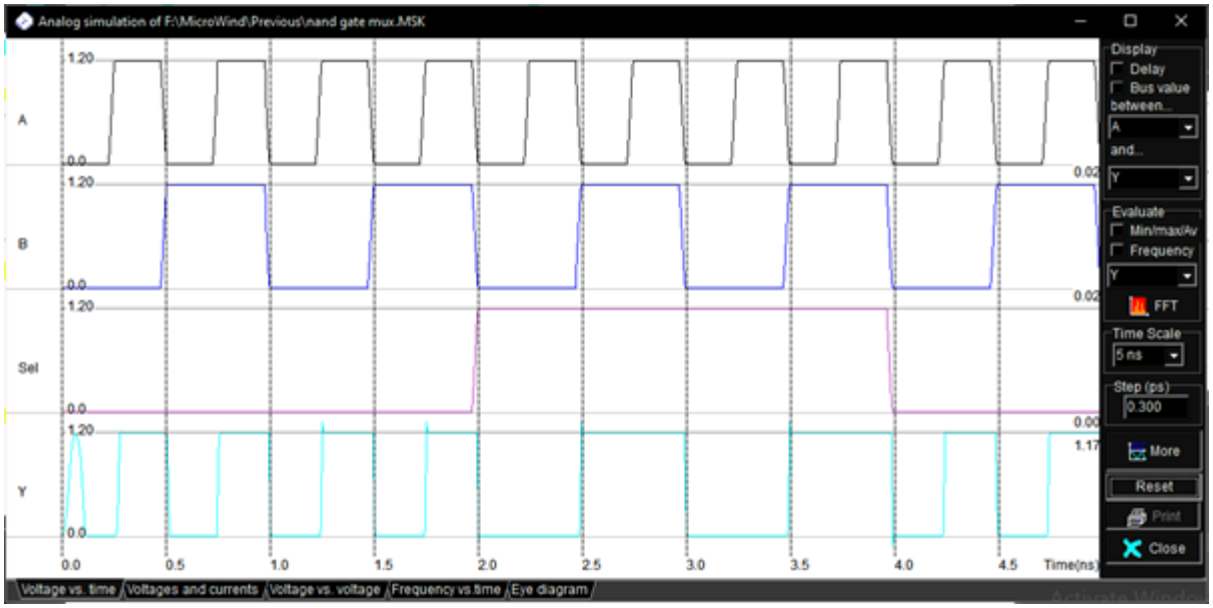
Mux 2:1 using Conventional gate (NAND gate)





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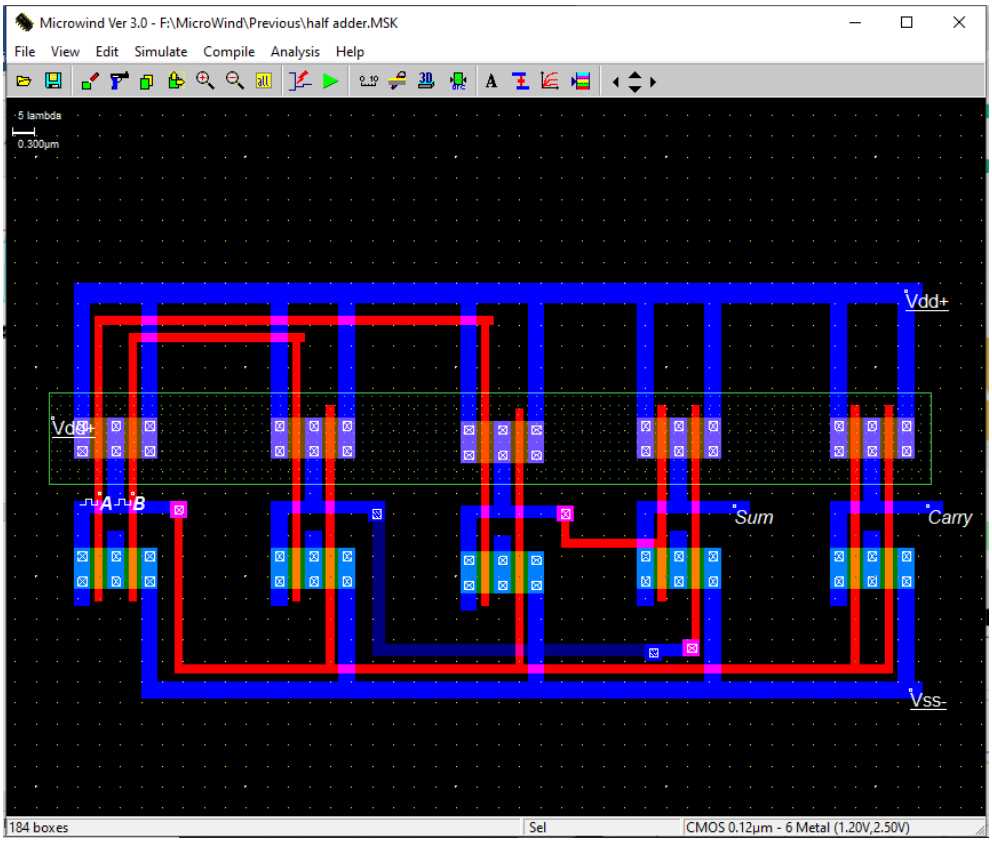
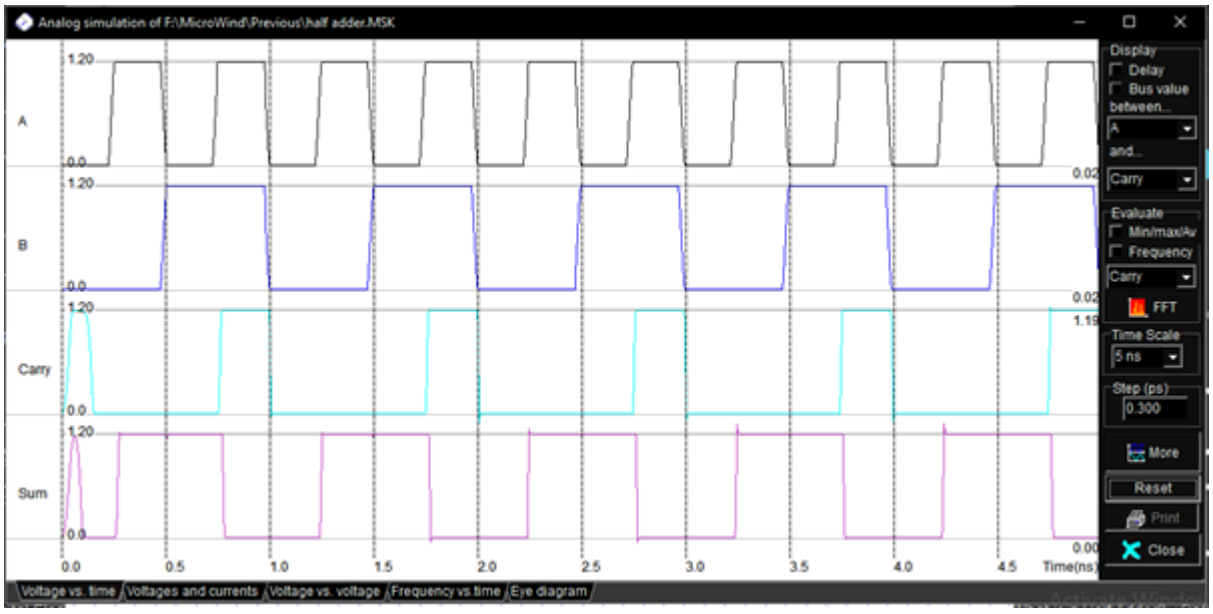
Half adder





Name: Atharva Dhobale

Roll No.: E43001 Batch: B9 Div: 3

SRAM