

## 2020 Digital IC Design Homework 5: Sobel

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<b>Simulation Result</b>																																							
Functional simulation	A	Gate-level simulation	A	Gate-level simulation time	15,728,808 (ns)																																		
<pre> ----- SUMMARY ----- Congratulations! Sobel X data have been generated successfully! The result is PASS!! Congratulations! Sobel Y data have been generated successfully! The result is PASS!! Congratulations! Sobel combine data have been generated successfully! The result is PASS!!  ** Note: ffinish   : C:/modeltech4_10.1c/MSB/testfixture.v(198)     Time: 15728760 ns  Iteration: 0  Instance: /testfixture         </pre>			<pre> ----- SUMMARY ----- Congratulations! Sobel X data have been generated successfully! The result is PASS!! Congratulations! Sobel Y data have been generated successfully! The result is PASS!! Congratulations! Sobel combine data have been generated successfully! The result is PASS!!  ** Note: ffinish   : C:/modeltech4_10.1c/MSB/testfixture.v(198)     Time: 15728808965 ps  Iteration: 0  Instance: /testfixture         </pre>																																				
<b>Synthesis Result</b>																																							
Total logic elements				619																																			
Total memory bit				0																																			
Embedded multiplier 9-bit element				0																																			
<div style="background-color: #0070c0; color: white; padding: 2px; font-weight: bold;">Flow Summary</div> <table border="1" style="width: 100%; border-collapse: collapse; font-size: 0.9em;"> <tr> <td style="background-color: #e0e0e0;"><b>Flow Status</b></td> <td>Successful - Mon Jun 22 22:57:07 2020</td> </tr> <tr> <td style="background-color: #e0e0e0;">Quartus II Version</td> <td>10.0 Build 262 08/18/2010 SP 1 SJ Full Version</td> </tr> <tr> <td style="background-color: #e0e0e0;">Revision Name</td> <td>SOBEL</td> </tr> <tr> <td style="background-color: #e0e0e0;">Top-level Entity Name</td> <td>SOBEL</td> </tr> <tr> <td style="background-color: #e0e0e0;">Family</td> <td>Cyclone II</td> </tr> <tr> <td style="background-color: #e0e0e0;">Device</td> <td>EP2C70F896C8</td> </tr> <tr> <td style="background-color: #e0e0e0;">Timing Models</td> <td>Final</td> </tr> <tr> <td style="background-color: #e0e0e0;">Met timing requirements</td> <td>N/A</td> </tr> <tr> <td style="background-color: #e0e0e0;">Total logic elements</td> <td>619 / 68,416 ( &lt; 1 % )</td> </tr> <tr> <td style="background-color: #e0e0e0;">  Total combinational functions</td> <td>600 / 68,416 ( &lt; 1 % )</td> </tr> <tr> <td style="background-color: #e0e0e0;">  Dedicated logic registers</td> <td>194 / 68,416 ( &lt; 1 % )</td> </tr> <tr> <td style="background-color: #e0e0e0;">Total registers</td> <td>194</td> </tr> <tr> <td style="background-color: #e0e0e0;">Total pins</td> <td>81 / 622 ( 13 % )</td> </tr> <tr> <td style="background-color: #e0e0e0;">Total virtual pins</td> <td>0</td> </tr> <tr> <td style="background-color: #e0e0e0;">Total memory bits</td> <td>0 / 1,152,000 ( 0 % )</td> </tr> <tr> <td style="background-color: #e0e0e0;">Embedded Multiplier 9-bit elements</td> <td>0 / 300 ( 0 % )</td> </tr> <tr> <td style="background-color: #e0e0e0;">Total PLLs</td> <td>0 / 4 ( 0 % )</td> </tr> </table>						<b>Flow Status</b>	Successful - Mon Jun 22 22:57:07 2020	Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version	Revision Name	SOBEL	Top-level Entity Name	SOBEL	Family	Cyclone II	Device	EP2C70F896C8	Timing Models	Final	Met timing requirements	N/A	Total logic elements	619 / 68,416 ( < 1 % )	Total combinational functions	600 / 68,416 ( < 1 % )	Dedicated logic registers	194 / 68,416 ( < 1 % )	Total registers	194	Total pins	81 / 622 ( 13 % )	Total virtual pins	0	Total memory bits	0 / 1,152,000 ( 0 % )	Embedded Multiplier 9-bit elements	0 / 300 ( 0 % )	Total PLLs	0 / 4 ( 0 % )
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<b>Description of your design</b>																																							
<p>讀 9 個 pixel 後算 SobelX、SobelY、SobelCombine，做 65536 個 round。</p> <p>上一次沒有用狀態機的方式寫，所以這次試著寫寫看，作法其實不難，但是因為不太會看時序，Debug 花了很多時間，還好最後有做出來。</p> <p>minimum CYCLE = 20</p>																																							

Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) × (gate-level simulation time in ns)