2020 Digital IC Design Homework 3: Approximate Average

NAME	李哲緯
Student ID	P76081297

Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	164410 (ns)

```
----------------------------------------------

All data have been generated successfully!

-------------------PASS-------------------

----------------------------------------------

** Note: $finish    : C:/modeltech64_10.1c/
   Time: 164410 ns  Iteration: 2  Instance:
1
```

```
----------------------------------------------

All data have been generated successfully!

-------------------PASS-------------------

----------------------------------------------

** Note: $finish    : C:/modeltech64_10.1c
   Time: 164410 ns  Iteration: 2  Instance
1
```

Synthesis Result

Total logic elements	486
Total memory bit	0
Embedded multiplier 9-bit element	0

Flow Summary

Flow Status	Successful - Tue May 05 12:33:02 2020
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	CS
Top-level Entity Name	CS
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	486 / 68,416 (< 1 %)
Total combinational functions	486 / 68,416 (< 1 %)
Dedicated logic registers	73 / 68,416 (< 1 %)
Total registers	73
Total pins	20 / 622 (3 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

用 72bit reg XS 存 9 個 8-bit number，clock 來時，取後 8 個數字及 input，計算 X_{avg}，接著根據公式找出 $X_{approximate}$，後面將 $X_{approximate}$ * 9 改成 ($X_{approximate}$ >> 3)+ $X_{approximate}$)，用 shift 代替乘法，最後在 shift right 3 bits 代替除以 8，得到 output

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*