2020 Digital IC Design Homework 2: Divider

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	6553610 ns

```
#       65519 data is correct
#       65520 data is correct
#       65521 data is correct
#       65522 data is correct
#       65523 data is correct
#       65524 data is correct
#       65525 data is correct
#       65526 data is correct
#       65527 data is correct
#       65528 data is correct
#       65529 data is correct
#       65530 data is correct
#       65531 data is correct
#       65532 data is correct
#       65533 data is correct
#       65534 data is correct
#       65535 data is correct
#       65536 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
# ** Note: $finish    : C:/modeltech64_10.1c/HW2/div_tb.v(62)
#    Time: 6553610 ns  Iteration: 0  Instance: /div_tb
```

```
#       65519 data is correct
#       65520 data is correct
#       65521 data is correct
#       65522 data is correct
#       65523 data is correct
#       65524 data is correct
#       65525 data is correct
#       65526 data is correct
#       65527 data is correct
#       65528 data is correct
#       65529 data is correct
#       65530 data is correct
#       65531 data is correct
#       65532 data is correct
#       65533 data is correct
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# --------------------PASS--------------------
# All data have been generated successfully!
# ** Note: $finish    : C:/modeltech64_10.1c/HW2/div_tb.v(62)
#    Time: 6553610 ns  Iteration: 0  Instance: /div_tb
```

Synthesis Result

Total logic elements	167
Total memory bit	0
Embedded multiplier 9-bit element	0

Flow Summary

Flow Status	Successful - Mon Apr 13 16:08:52 2020
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	div
Top-level Entity Name	div
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	167 / 68,416 (< 1 %)
Total combinational functions	167 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	25 / 622 (4 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

照著 hardware friendly division 的邏輯來做，但是不知道怎麼用 clock 跟 mux，所以就先用 for 迴圈做了。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*