

2020 Digital IC Design Homework 1: 4-bit binary adder-subtractor

NAME	李哲緯																																						
Student ID	P76081297																																						
Simulation Result																																							
Functional simulation	Pass or Fail	Gate-level simulation	Pass or Fail	Gate-level simulation time	simulation time (ns)																																		
<pre># 495 data is correct # 496 data is correct # 497 data is correct # 498 data is correct # 499 data is correct # 500 data is correct # 501 data is correct # 502 data is correct # 503 data is correct # 504 data is correct # 505 data is correct # 506 data is correct # 507 data is correct # 508 data is correct # 509 data is correct # 510 data is correct # 511 data is correct # 512 data is correct # -----PASS----- # All data have been generated successfully! # ** Note: \$finish : C:/modeltech64_10.1c/HW1/AS_tb.v(63) # Time: 25700 ns Iteration: 0 Instance: /AS_tb</pre>			<pre># 495 data is correct # 496 data is correct # 497 data is correct # 498 data is correct # 499 data is correct # 500 data is correct # 501 data is correct # 502 data is correct # 503 data is correct # 504 data is correct # 505 data is correct # 506 data is correct # 507 data is correct # 508 data is correct # 509 data is correct # 510 data is correct # 511 data is correct # 512 data is correct # -----PASS----- # All data have been generated successfully! # ** Note: \$finish : C:/modeltech64_10.1c/HW1/AS_tb.v(63) # Time: 25700 ns Iteration: 0 Instance: /AS_tb</pre>																																				
Synthesis Result																																							
Total logic elements				8																																			
Total memory bit				0																																			
Embedded multiplier 9-bit element				0																																			
<div style="background-color: #0070C0; color: white; padding: 2px; font-weight: bold;">Flow Summary</div> <table border="1" style="width: 100%; border-collapse: collapse; font-size: 0.9em;"> <tr> <td>Flow Status</td> <td>Successful - Mon Apr 13 16:25:40 2020</td> </tr> <tr> <td>Quartus II Version</td> <td>10.0 Build 262 08/18/2010 SP 1 SJ Full Version</td> </tr> <tr> <td>Revision Name</td> <td>AS</td> </tr> <tr> <td>Top-level Entity Name</td> <td>AS</td> </tr> <tr> <td>Family</td> <td>Cyclone II</td> </tr> <tr> <td>Device</td> <td>EP2C70F896C8</td> </tr> <tr> <td>Timing Models</td> <td>Final</td> </tr> <tr> <td>Met timing requirements</td> <td>Yes</td> </tr> <tr> <td>[-] Total logic elements</td> <td>8 / 68,416 (< 1 %)</td> </tr> <tr> <td> Total combinational functions</td> <td>8 / 68,416 (< 1 %)</td> </tr> <tr> <td> Dedicated logic registers</td> <td>0 / 68,416 (0 %)</td> </tr> <tr> <td> Total registers</td> <td>0</td> </tr> <tr> <td> Total pins</td> <td>14 / 622 (2 %)</td> </tr> <tr> <td> Total virtual pins</td> <td>0</td> </tr> <tr> <td> Total memory bits</td> <td>0 / 1,152,000 (0 %)</td> </tr> <tr> <td> Embedded Multiplier 9-bit elements</td> <td>0 / 300 (0 %)</td> </tr> <tr> <td> Total PLLs</td> <td>0 / 4 (0 %)</td> </tr> </table>						Flow Status	Successful - Mon Apr 13 16:25:40 2020	Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version	Revision Name	AS	Top-level Entity Name	AS	Family	Cyclone II	Device	EP2C70F896C8	Timing Models	Final	Met timing requirements	Yes	[-] Total logic elements	8 / 68,416 (< 1 %)	Total combinational functions	8 / 68,416 (< 1 %)	Dedicated logic registers	0 / 68,416 (0 %)	Total registers	0	Total pins	14 / 622 (2 %)	Total virtual pins	0	Total memory bits	0 / 1,152,000 (0 %)	Embedded Multiplier 9-bit elements	0 / 300 (0 %)	Total PLLs	0 / 4 (0 %)
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Description of your design																																							
Full adder 用兩個 half adder、一個 or 做出，接著照著作業要求給的圖接線																																							

Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)