2020 Digital IC Design Homework 1: 4-bit binary adder-subtractor

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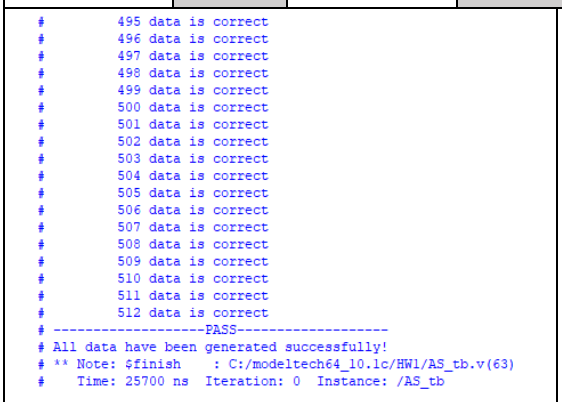
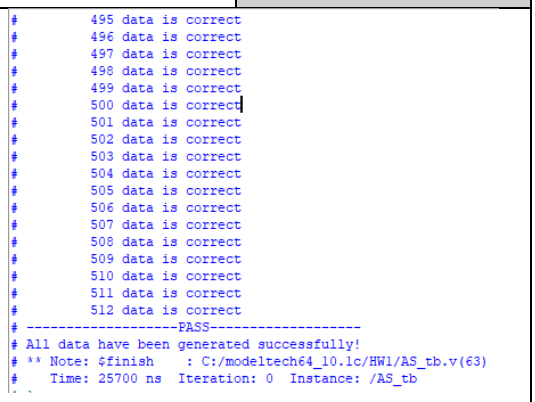
Simulation Result

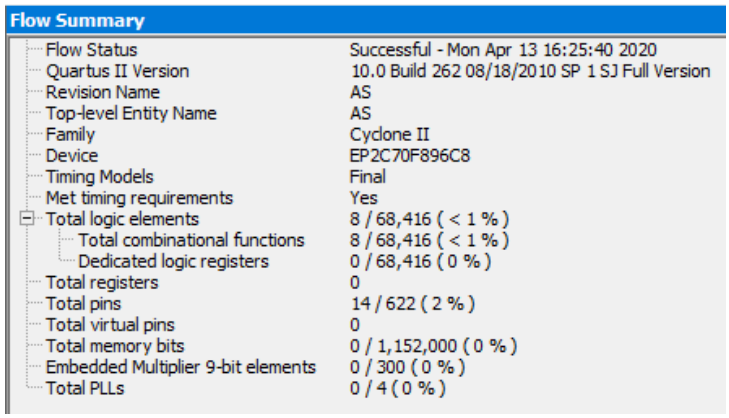
Functional simulation	Pass or Fail	Gate-level simulation	Pass or Fail	Gate-level simulation time	simulation time (ns)





Synthesis Result

Total logic elements	8
Total memory bit	0
Embedded multiplier 9-bit element	0



Description of your design

Full adder 用兩個 half adder、一個 or 做出，接著照著作業要求給的圖接線

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*