2020 Digital IC Design Homework 2: Divider

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| NAME | | 李哲緯 | | | | | | |
| Student ID | | P76081297 | | | | | | |
| **Simulation Result** | | | | | | | | |
| Functional simulation | Pass | | Gate-level simulation | Pass | | | Gate-level simulation time | 6553610 ns |
|  | | | | | |  | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | | 167 | | | |
| Total memory bit | | | | | 0 | | | |
| Embedded multiplier 9-bit element | | | | | 0 | | | |
|  | | | | | | | | |
| **Description of your design** | | | | | | | | |
| 照著hardware friendly division的邏輯來做，但是不知道怎麼用clock跟mux，所以就先用for迴圈做了。 | | | | | | | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (gate-level simulation time in ns)*