2020 Digital IC Design Homework 4: RC4 Encrypt

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| **Simulation Result** | | | | | | | | |
| Functional simulation | Pass | | Gate-level simulation | Fail | | | Gate-level simulation time |  |
|  | | | | | | (your post-sim result) | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | |  | | | |
| Total memory bit | | | | |  | | | |
| Embedded multiplier 9-bit element | | | | |  | | | |
|  | | | | | | | | |
| **Description of your design** | | | | | | | | |
| Key\_valid等一個cycle後開始讀32個key，初始化sbox並且打亂，plain\_read設為1，下一個cycle開始加密明文並且輸出，加密完  重新初始化並打亂sbox，將cipher\_read設為1，下一個cycle開始將密文解密並輸出，作完之後將done設為1 | | | | | | | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (gate-level simulation time in ns)*