2020 Digital IC Design Homework 5: Sobel

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| **Simulation Result** | | | | | | | | |
| Functional simulation | A | | Gate-level simulation | A | | | Gate-level simulation time | 15,728,808 (ns) |
|  | | | | | |  | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | | 619 | | | |
| Total memory bit | | | | | 0 | | | |
| Embedded multiplier 9-bit element | | | | | 0 | | | |
|  | | | | | | | | |
| **Description of your design** | | | | | | | | |
| 讀9個pixel後算SobelX、SobelY、SobelCombine，做65536個round。  上一次沒有用狀態機的方式寫，所以這次試著寫寫看，作法其實不難，但是因為不太會看時序，Debug花了很多時間，還好最後有做出來。  minimum CYCLE = 20 | | | | | | | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (gate-level simulation time in ns)*