AiP650E
2-line Serial Interface/Common Cathode 8Seg 4Grid LED Controller/Driver with 7*4 Keyboard Scan Ports and Partial Combined Key Function

Product Specification

Specification Revision History:

Version	Date	Description
2015-01-A1	2015-01	New
2019-09-A2	2019-09	Replace the new template and add Ordering Information
2021-12-A3	2021-12	Modify Ordering Information

1、General Description

AiP650E is a LED driver with interface of keyboard scanning circuit. It integrates on-chip circuits of MCU input/output controller interface, data latch, LED driver, keyboard scanning, brightness modulation etc. Stable performance, reliable quality, and strong capacity of resisting disturbance are advantages of this chip, which guarantees it to be applied in a 24-hours continuous working occasion.

Features:

- Display mode: 8 SEG×4 DIG
- The output current of one Seg is no less than 25mA, and the output current of one Dig is no less than 150mA.
- 8-stage brightness modulation
- Keyboard scanning: 7×4bit with 4 groups of key combinations
- High-speed serial interface of two-line
- Built-in RC oscillator
- Built-in power-on reset circuit
- Supply voltage: 3V~5.5V
- It is suggested to add a capacitor whose value is 100nF while using the ICs, and the capacitor need to be connect to the VDD port of AiP650E as near as possible (suggested less than 2cm)
- Package: DIP16/SOP16

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP650EP DA16.TB	DIP16	AiP650EP	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing:2.54mm
AiP650EO SA16.TB	SOP16	AiP650EO	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm

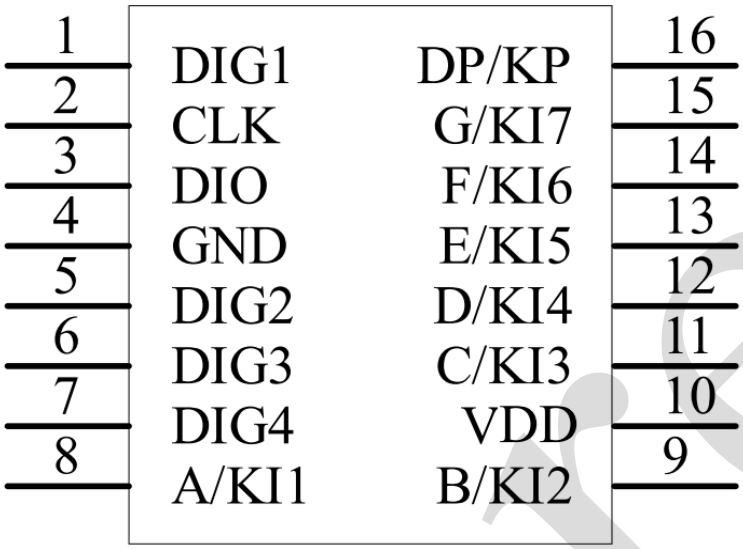
Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP650EO SA16.TR	SOP16	AiP650EO	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Pin Configurations



2.2、Pin Description

Pin No.	Pin Name	Description	Function
1	DIG1	Grid /Key Scan output Pin	LED Grid Output Pin, also acts as the key scan output pin.
2	CLK	Clock input Pin	The clock input pin, built-in pull-up resistors.
3	DIO	Data input/output Pin	The data input/output pin.(N-Channel, Open-Drain)
4	GND	Ground Pin	Ground Pin
5	DIG2	Grid /Key Scan output Pin	LED Grid Output Pin, also acts as the key scan output pin.
6	DIG3	Grid /Key Scan output Pin	LED Grid Output Pin, also acts as the key scan output pin.
7	DIG4	Grid /Key Scan output Pin	LED Grid Output Pin, also acts as the key scan output pin.
8	A/KI1	Segment output Pin/ Key Scan input Pin	LED Segment Output Pin, also acts as the key scan input，built-in pull-down resistors.
9	B/KI2	Segment output Pin/ Key Scan input Pin	LED Segment Output Pin, also acts as the key scan input，built-in pull-down resistors.
10	VDD	Power Supply	Add a 104 capacitance between VDD and GND, as close as possible to power supply pin.
11	C/KI3	Segment output Pin/ Key Scan input Pin	LED Segment Output Pin, also acts as the key scan input，built-in pull-down resistors.
12	D/KI4	Segment output Pin/ Key Scan input Pin	LED Segment Output Pin, also acts as the key scan input，built-in pull-down resistors.

13	E/KI5	Segment output Pin/ Key Scan input Pin	LED Segment Output Pin, also acts as the key scan input，built-in pull-down resistors.
14	F/KI6	Segment output Pin/Key Scan input Pin	LED Segment Output Pin, also acts as the key scan input，built-in pull-down resistors.
15	G/KI7	Segment output Pin/Key Scan input Pin	LED Segment Output Pin, also acts as the key scan input，built-in pull-down resistors.
16	DP/KP	Segment output	LED Segment output pin

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, All voltage referenced to Vss, unless otherwise specified.)

Characteristic	Symbol	Conditions		Value	Unit
Power Supply Voltage	VDD	-		-0.5～+6.5	V
Input voltage	VIN	-		-0.5～VDD+0.5	V
Segment drive output current	I_{O1}	-		0～30	mA
Grid drive output current	I_{O2}	-		0～150	mA
Sum driving current of all pins	I_O	-		0～150	mA
Ambient Temperature	T_{amb}	-		-40～+85	℃
Storage Temperature	T_{stg}	-		-55～+125	℃
Soldering Temperature	T_L	10s	DIP	245	℃
			SOP	250	℃

3.2、Electrical Characteristics

(T_{amb}=25℃, VDD=5V, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
DC Characteristics					
Power Supply Voltage	VDD	3	5	5.5	V
Power Supply Current	I_C	0.2	80	230	mA
Quiescent Current	I_{Cs}	-	0.3	0.6	mA
Sleep Current	I_{Cslp}	-	0.05	0.1	mA
CLK and DIO Low-level input voltage	V_{IL}	-0.5	-	0.8	V
CLK and DIO High-level input voltage	V_{IH}	2.0	-	VDD+0.5	V
KI Low-level input voltage	V_{ILki}	-0.5	-	0.5	V
KI High-level input voltage	V_{IHki}	1.8	-	VDD+0.5	V
DIG Low-level output voltage（-200mA）	V_{OLdig}	-	-	1.2	V
DIG Low-level output voltage（-100mA）	V_{OLdig}	-	-	0.8	V
DIG Low-level output voltage（50mA）	V_{OHdig}	4.5	-	-	V
KI Low-level output voltage（-20mA）	V_{OLki}	-	-	0.5	V

KI Low-level output voltage（20mA）	V_{OHki}	4.5	-	-	V
All other pins Low-level output voltage（-4mA）	V_{OL}	-	-	0.5	V
All other pins High-level output voltage（4mA）	V_{OH}	4.5	-	-	V
KI input pull-down current	I_{DN1}	-30	-50	-90	uA
CLK input pull-up current	I_{UP1}	10	200	300	uA
DIO input pull-up current	I_{UP2}	150	300	400	uA
KP input pull-up current	I_{UP3}	500	2000	5000	uA
The voltage of power on reset	V_R	2.3	2.6	2.9	V
AC Characteristics					
● Internal timing parameters					
Power on reset time	T_{PR}	10	25	60	ms
Display scan cycle	T_P	4	8	20	ms
Key scan interval	T_{KS}	20	40	80	ms
●Interface timing parameters					
DIO falling edge of the start signal setup time	T_{SSTA}	100	-	-	ns
DIO falling edge of the start signal hold time	T_{HSTA}	100	-	-	ns
DIO rising edge of the stop signal setup time	T_{SSTO}	100	-	-	ns
DIO rising edge of the stop signal hold time	T_{HSTO}	100	-	-	ns
CLK low level width	T_{CLOW}	100	-	-	ns
CLK high level width	T_{CHIG}	100	-	-	ns
Setup time between DIO input and CLK	T_{SDA}	30	-	-	ns
hold time between DIO input and CLK	T_{HDA}	10	-	-	ns
Delay time between DIO output valid and CLK failing edge	T_{AA}	2	-	30	ns
Delay time between DIO output invalid and CLK failing edge	T_{DH}	2	-	40	ns
Data transmission rate	Rate	0	-	4M	bps

4、Function Description

4.1、Display Mode And RAM Address

When the LED display data is written,the operation is performed in the order of the display address from the high to the low and the data byte from the high to the low.The address assignment is as follows:

A	B	C	D	E	F	G	DP	
B0	B1	B2	B3	B4	B5	B6	B7	
68H								DIG1
6AH								DIG2
6CH								DIG3
6EH								DIG4

Note: When power up, transfer data to RAM first, and then setup display on.

4.2、Control Instruction

The system instruction must be input before sending display instructions,that is,input byte 1 is the system instruction,and input byte 2 is the display instruction.

4.2.1、System Instruction

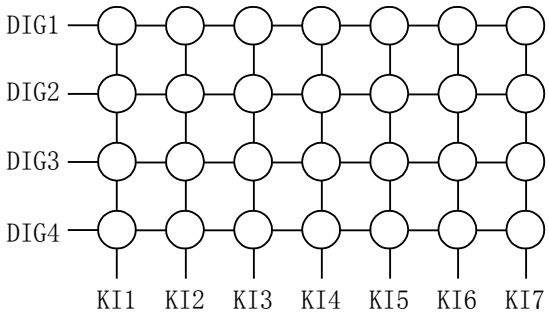
Instruction	Instruction code								Instruction description
	B7	B6	B5	B4	B3	B2	B1	B0	
System Instruction	0	1	0	0	1	0	0	0	Set system parameters

4.2.2、Display Instruction

Instruction	Instruction code								Instruction description
	B7	B6	B5	B4	B3	B2	B1	B0	
Display mode	X	X	X	X	X	X	X	**D**	D=1, display on D=0, display off
Sleep mode	X	X	X	X	X	**W**	X	X	W=0, sleep mode disable W=1, sleep mode enable
SEG control	X	X	X	X	**S**	X	X	X	S=1, seven segment S=0, eight segment
Brightness setting	X	**BR[2:0]**			X	X	X	X	BR[2:0]= 000: 8 levels of brightness 001: 1 levels of brightness 010: 2 levels of brightness 011: 3 levels of brightness 100: 4 levels of brightness 101: 5 levels of brightness 110: 6 levels of brightness 111: 7 levels of brightness

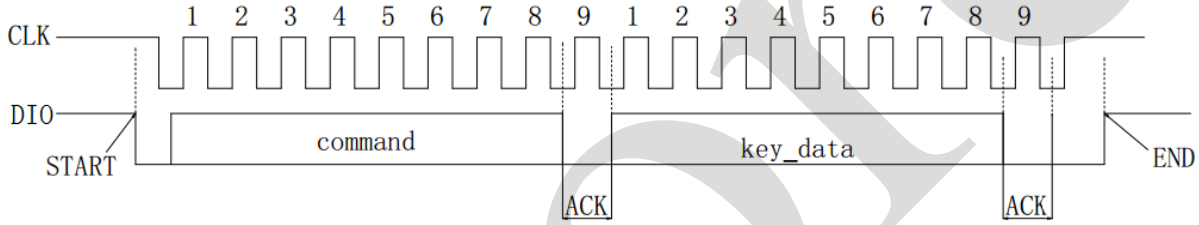
4.3、Key Scan Matrix And Key Scan Data Register

Key Scan Matrix



Key Scan Data

The data format of the key values in this circuit includes a command with 9bit clock period and data with 9bit clock period. The ninth bit of the command is ACK=0 and the ninth bit of data is ACK=1. The diagram is as the image below.



command: Get_key command
key_data: Get_key data (1 byte)

Instruction	Instruction code								Instruction description
	B7	B6	B5	B4	B3	B2	B1	B0	
Get key	0	1	0	0	1	X	X	1	Read the key data

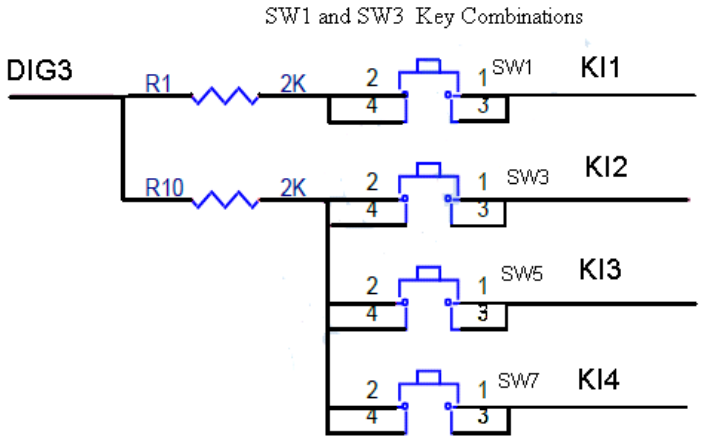
Different key values read can be achieved via logic coding. The according table is shown below:

	DIG1	DIG2	DIG3	DIG4
NO KEY	00_101_110:2E			
KI1	01_000_100	01_000_101	01_000_110	01_000_111
KI2	01_001_100	01_001_101	01_001_110	01_001_111
KI3	01_010_100	01_010_101	01_010_110	01_010_111
KI4	01_011_100	01_011_101	01_011_110	01_011_111
KI5	01_100_100	01_100_101	01_100_110	01_100_111
KI6	01_101_100	01_101_101	01_101_110	01_101_111
KI7	01_110_100	01_110_101	01_110_110	01_110_111
KI1+KI2	01_111_100	01_111_101	01_111_110	01_111_111

The key press can only be identified only when it lasts two key scan periods at least.

AiP650E supports key combination of KI1 and KI2 with the same DIGX pin. Key combination has the highest priority. In addition, key with smaller code has the high priority if multiple keys are pressed at the same time. For instance, two keys both connecting DIG3\KI1 and DIG3\KI2 can be a key combination. In key combination application, the block processing between KI1 and KI2 with key combination function is

as follows:



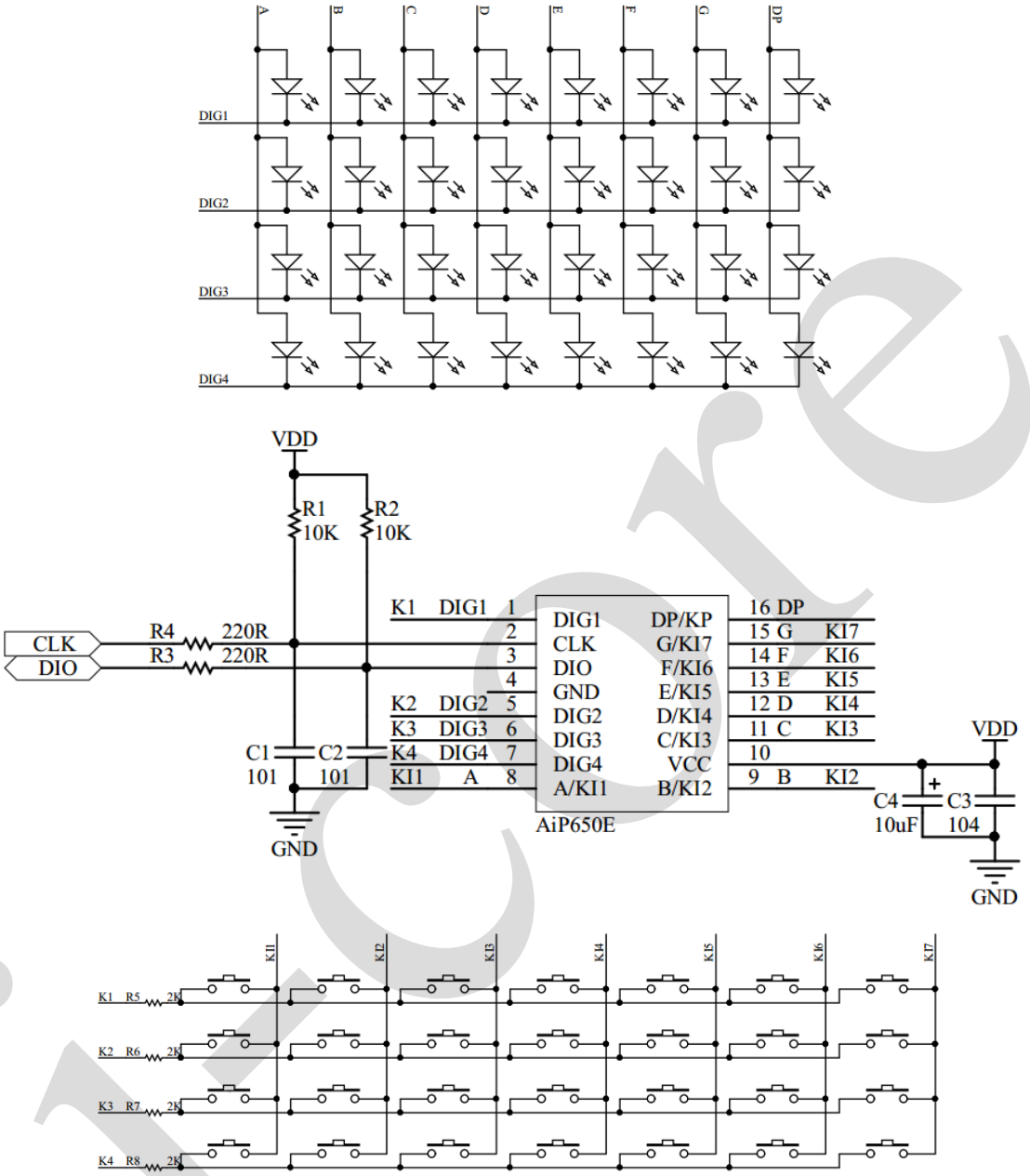
4.4、Communication Port Instruction

This circuit applies a communication like I^2C. Data of MPU communicate via interfaces of two-line bus with this circuit. While inputting data, the circuit latches data in the rising edge of CLK. As a result, signals on DIO must stay unchanged when CLK is high level, in addition, signals on DIO can be changed only when the clock signal of CLK is low and DIO can't change in the trailing edge of CLK. The start condition of inputting data is CLK keep its high level and DIO changing from high to low, and the end condition is CLK to be of its high level and DIO changing from low to high.

The data transmission of this circuit has answer-back signal ACK. Inside the ninth clock signal on CLK , it will generate an ACK with a logic 0 on DIO in the processing of data transmission. No matter it is command writing, data reading or writing, ACK signal outputs on the ninth CLK signal.

The mode of instruction transmission is 16bit. The procedure of instruction transmission is shown as follows. While transmitting data and command, MSB is transmitted first and the LSB is transmitted last. The circuit latch data in the rising edge of CLK and DIO cannot change when CLK is keep high level, also, it cannot vary in the trailing edge of CLK, but it can be changed when CLK is low level.

5、Typical Application Circuit And Application Note

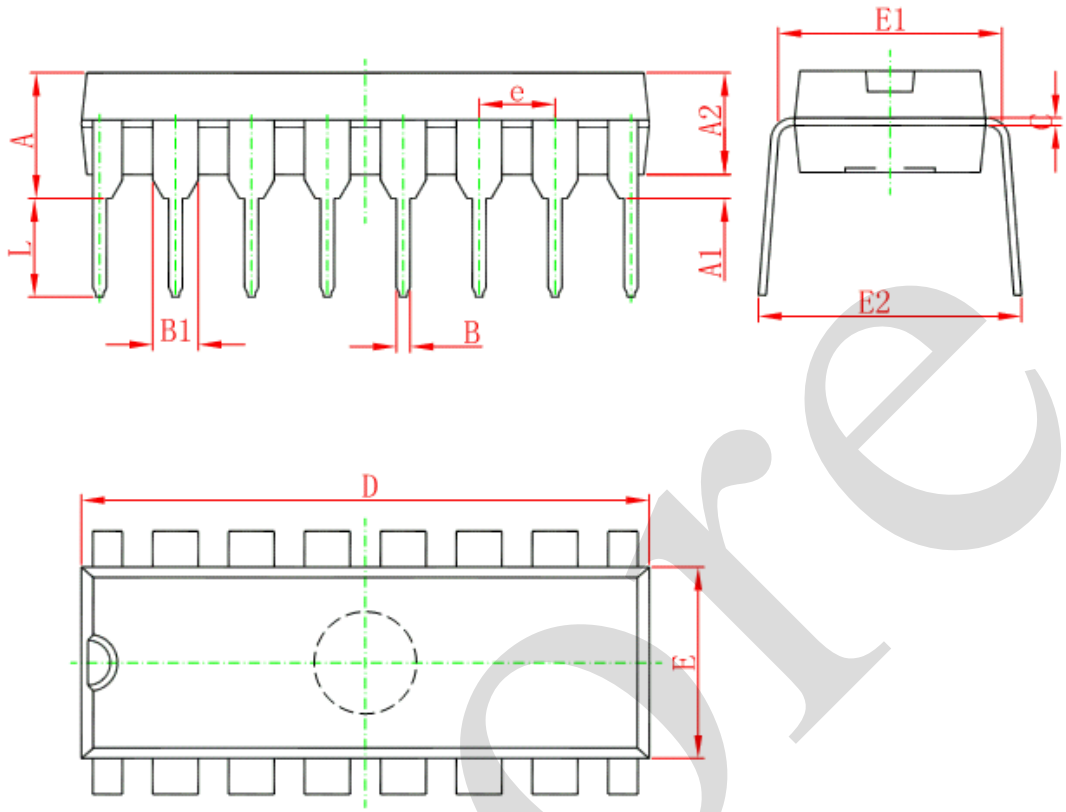


Note:

1. The circuit between filter capacitor and VDD, GND is as short as possible to enhance the filter effect.
2. In order to improve the anti-interference ability of the circuit, the communication port is recommended to be connected according to the above figure. The specific parameter values can be adjusted according to actual needs.
3. In order to prevent the influence of keys on the display effect,the resistor of 2KΩ(R5/R6/R7/R8)should be connected in series between DIG1~DIG4 in the key matrix.

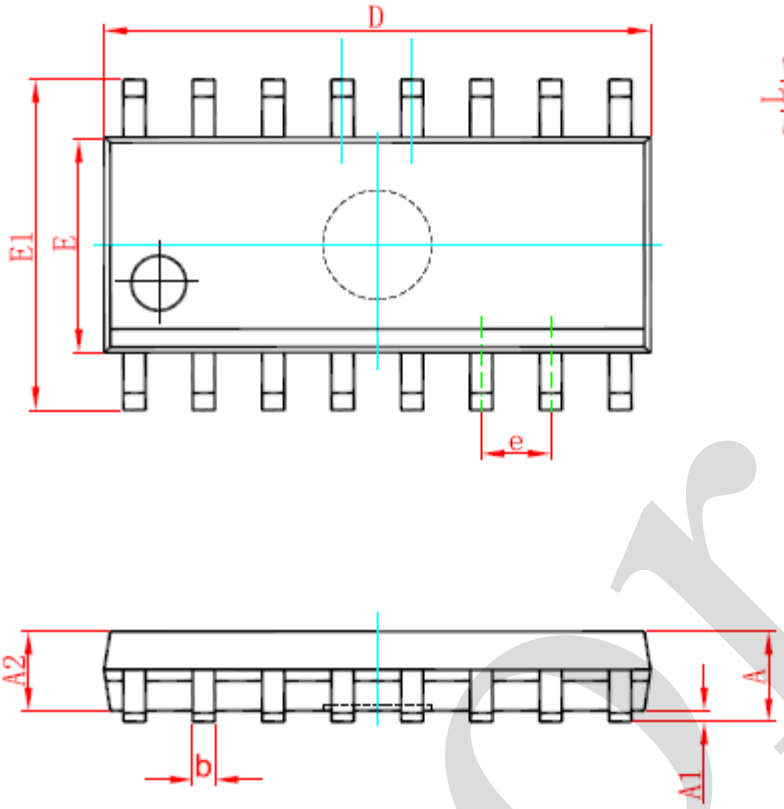
6、Package Information

6.1、DIP16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

6.2、SOP16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notion

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