POWER, ENERGY AND DELAY ANALYSIS OF A SUB-THRESHOLD MOS CIRCUIT INCLUDING VARIOUS LOGIC STYLES

A MAJOR PROJECT REPORT
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CERTIFICATE

This is to certify that the project report titled " **POWER, ENERGY AND DELAY ANALYSIS OF A SUB-THRESHOLD MOS CIRCUIT INCLUDING VARIOUS LOGIC STYLES** " submitted by **Animesh Mukherjee(B110826EC), Amal Roshan(B110511EC), C. Haranadh(B110391EC) and Jithin VJ(B110011EC)** as the record of the project work carried out by them is accepted in partial fullfillment of the requirement for the award of the degree of Bachelor of Technology in Electronics and Communication Engineering at the National Institute of Technology Calicut.

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Chapter 1

Introduction to Work

Low power design methodology is one of the pioneering fields in VLSI design. There are many low power techniques such as source biasing, power gating, clock gating, multi-V_{th} design. Along with it there has been immense research in sub threshold design. The most advantageous feature of sub-threshold design is reduction in leakage power. The sub-threshold currents are a few order larger than the leakage currents. This work emphasises on study, design and analysis of digital circuits (ex- adders) in sub-threshold region. It is preceded by a detailed work on logical Effort (for High Performance) and sleepy circuits (for low energy consumption).

1.1 Organization of work

This report is broadly divided into four chapters.

Chapter one deals with basics of power and delay. It explains why a low energy design is same as low power design. It is followed by simultaional analysis of adder circuits using static CMOS and Pass Transistor Logic.
Chapter two deals with logical effort approach. The concept of logical effort is explained thoroughly and a sum section of a full adder is designed using it. Limitations of logical effort due to interconnects has also been discussed.
Chapter three deals with sleepy keeper approach. It is a method of power gating and it results in low static dissipation of power. Simulational results about sleepy keeper approach have been included.
Chapter four deals with sub-threshold design. It begins with the modelling of sub-threshold current followed by a design methodology that is based on the parameters of the application circuit. Simulations of full adder using static CMOS and Pass Transistor Logic have been performed in the sub-threshold region. Finally the pros and cons of the sub-threshold design has been discussed.

Chapter 2

Power and Energy

2.1 Introduction to power and energy

The design of electronic circuits has been dominated by the likes of processors, semiconductor memories, separate graphic processing units, rapid execution engines, multi-stage pipelined processors and many more, until the 21st century.
In the 21st century, portability became an important requirement for all electronic circuits. Hand held devices, cell phones, calculators, tablets, PDAs and any more small gadgets came into existence and the need for low energy consumption became more prominent as these devices do not have a serious performance requirements [1]. In certain emerging applications, such as sensor nodes, bio-medical and implant devices, wearable computing etc energy efficiency concerns supersede traditional emphasis on performance or speed. These systems are smaller in size and energy efficiency is a major concern that is primarily achieved by scaling down the voltage in most cases. Many such energy efficient systems use minimum energy in the sub-threshold region, where the power supply voltage is below the device threshold voltage. Hence, sub-threshold circuit behavior and design methodologies plays an integral role in designing energy efficient low power electronic devices. This work mainly focuses on the various design paradigms and approaches adopted in modern day sub-threshold VLSI design that are used in designing energy efficient devices.
We face a myriad of problems while designing sub-threshold circuits like leakage current, lower performance, design complexity etc. Moreover many of the design paradigms employed in above threshold region are not applicable in the sub-threshold domain. This project aims at design and analysis of sub-threshold circuits, and understanding the limitations and opportunities of this deisgn [2].
The work done in this project has been motivated by the need for low-energy consuming circuits that have a higher performance. But our studies show that there are certain well-established boundaries that define the limits of sub-threshold design in terms of performance and power consumption.

2.2 Equivalence of Low Power and Low Energy

The low power design is by default a low energy design. It needs to be clarified that power is rate of consuming/delivering energy, so in essence there is no shortage of power as the rate of using energy depends on the user. On the other hand energy is a scarce quantity as it is an independent variable unlike power. So low energy design is intuitively a low power design with a fixed operating frequency as per the requirement by the application.

2.3 Power

Power is the single most important design metric in modern day electronic design. The increasing power density of electronic circuits was rightly pointed out by Gordon Moore (Co-founder Intel Semiconductor Corp) through his famous Moore's law. Moore's law states that "The number of transistors per square inch on integrated circuits had doubled every year since the integrated circuit was invented and the data density has almost doubled every 18 months ". Experts believe the Moore's law to be valid for another 2-3 decades and this points out the enormous amount of data and power that is transmitted across various devices per day [3].

2.3.1 Terminology

Average power

The instantaneous power (P=VI) of alternating current (AC) circuit vary continuously, so unlike the DC circuits, a proper measure of power is the average power.The average power is expressed as

$$P = \Delta W/\Delta t \tag{2.1}$$

From the above equation average power is equal to the average amount of work done or energy converted (ΔW) per unit of time(Δt). From the electrical point of view the equations can be remodelled as

$$P = I \times V = I^2 \times R = \frac{V^2}{R} \tag{2.2}$$

Here R is resistance measured in ohms, I is current in amperes and V is voltage or potential difference measured in volts.

Instantaneous Power

The instantaneous power as the name indicates is the power of the system at that particular instant (Δt approaches zero).

$$P_{instantaneous} = \lim_{\Delta t \to 0} (\Delta W/\Delta t) \tag{2.3}$$

It can also be written as the product of $V(t)$ (potential difference or voltage drop across the component) and $I(t)$ (instantaneous current).

$$P(t) = I(t) \times V(t) \tag{2.4}$$

Peak Power and Duty Cycle

In the case of an AC power source, an important parameter that needs to be considered is the peak power or the maximum power that the device draws from the source during a given period of time. This is an important parameter that plays a major role in the reliability of circuit operation and also helps in designing the circuits in such a way that it does not cause soft errors. Peak power can simply be defined as

$$P_0 = Max[P(t)] \tag{2.5}$$

If the energy per pulse is denoted as E_{pulse} ,then we can define the pulse length τ as

$$E_{pulse} = P_0 \times \tau \tag{2.6}$$

The ratio of average power to the peak power is equal to the ratio of pulse length to the period T of the periodic fucnction and is called duty cycle i.e

$$\frac{P_{avg}}{P_0} = \frac{\tau}{T} \tag{2.7}$$

2.3.2 Power Dissipation in CMOS Circuits

Generally,we require a very large number of transistors while designing VLSI circuits and it leads to a wide variety of ways in which power is dissipated. Most of the major sources of power dissipation in VLSI circuits can be classified as static and dynamic types [4].

$$P_{total} = P_{static} + P_{dynamic} \tag{2.8}$$

Dynamic Power Dissipation

- Switching Power Dissipation
  As nodes transit between two logic levels parasitic capacitances get charged and discharged,current flows through the channel resistance of transistors and power is dissipated. This component depends upon supply voltage,node voltage swing,average switching capacitance per cycle.The power dissipated depends upon the signal probabilities and thus are expressed in terms of an activity factor.The power dissipated is given by :

  $$P = \alpha C_{load} f V_{DD}^2 \tag{2.9}$$

  where α is switching activity factor, C_{load} is load capacitance, f is frequency and V_{DD} is supply voltage.
  The activity factor is the probability that the circuit node transitions from 0 to 1, because that is the only time the circuit consumes power. A clock has an activity factor of one because it rises and falls every cycle. Most data has a maximum activity factor of 0.5 because it transitions only once each cycle. Truly random data has an activity factor of 0.25 because it transitions every other cycle. Static CMOS logic has been empirically determined to have activity factors closer to 0.1 because some gates maintain one output state more often than another and because real data inputs to some portions of a system often remain constant from one cycle to the next [5]. The switching power dissipation forms a large portion of dynamic power dissipation as output capacitance C_{load} is charged or discharged dynamically as shown in Figure 1.1

- Short-Circuit power dissipation
  Short-Circuit Current is the current due to the creation of a DC path between the supply and ground terminals of a cmos circuit. This type of power dissipation takes place even when there is no load or parasitic capacitance due to the slow input change. This results in both p-sub network and n-sub network conducting simultaneously. This happens when the output of a gate is changing with response to the input(s). This power dissipation occurs due to simultaneous saturation of both pull-up and pull-down networks [6] as shown in Figure 1.2 .

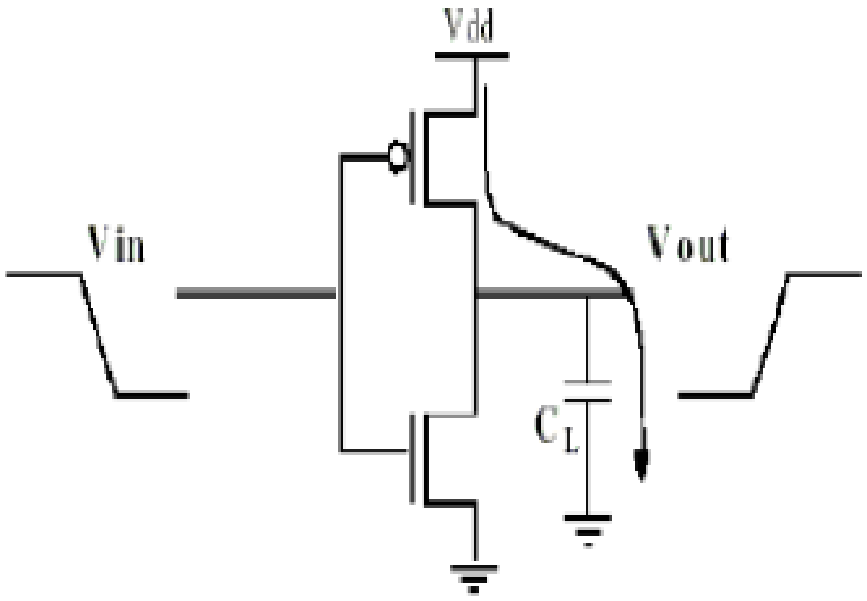

Figure 2.1: Switching power dissipation due to the charging and discharging of parasitic capacitance

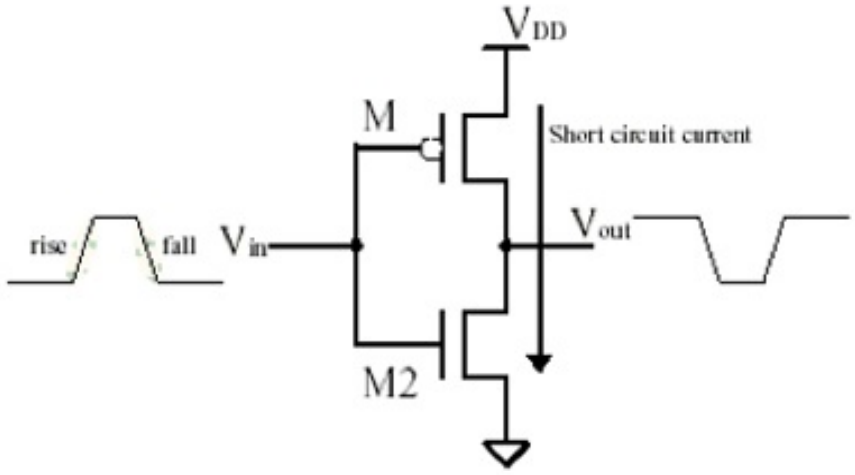

Figure 2.2: Short-circuit power dissipation due to flow of short-circuit current from V_{DD} to ground

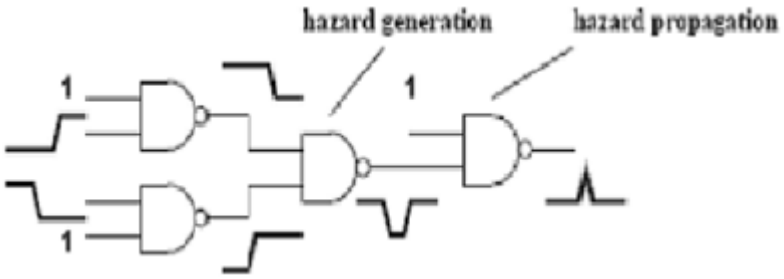

Figure 2.3: Glitching Power Dissipation

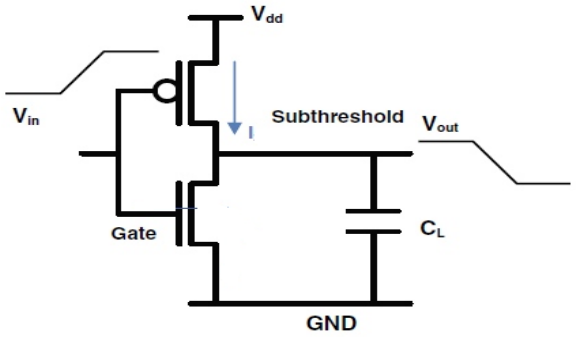

Figure 2.4: Power Dissipation due to Sub-threshold leakage

- Glitching Power Dissipation
  Glitching power dissipation occurs mainly due to the finite delay of gates used in the CMOS circuit. Finite delay of gates results in the output becoming high for a very small duration and this phenomenon is called a glitch. So glitches are in short, temporary changes in the output due to skewed input and account for about 15 - 20 percentage of total power dissipation in VLSI circuits. The glitching power dissipation is mainly determined by the output load, input pattern and the slope of the input [7]. Figure 1.3 shows an example of glitching power consumption.

Static Power Dissipation

Even when the CMOS circuit is in an idle state there is a power dissipation due to the leakage and sub-threshold current that has a huge impact on design of ultra low-power systems.The static power dissipation types can be broadly classified as follows

- Sub-threshold leakage
  It is caused by minority carriers drift from drain to source in the transistor weak-inversion region of operation ($V_{GS} < V_{th}$). It is the major source of static power dissipation in VLSI circuits. Sub-threshold leakage current flows when a transistor is supposed to be OFF [6]. For V_{DS} exceeding a few multiples of the thermal voltage (e.g. $V_{DS} > 50mV$), it can be simplified to

$$I_{sub} = I_0 \left[1 - exp\frac{qV_{DS}}{kT} \right] exp\left[q\frac{V_{GS} - V_{th} - V_{off}}{\eta kT} \right] \tag{2.10}$$

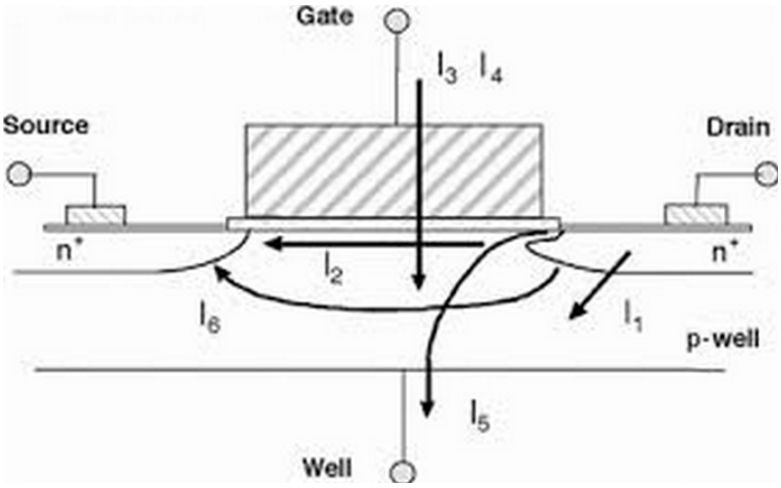

Figure 2.5: Components of Leakage Power

- Junction Leakage
  Junction leakage occurs when the source or drain diffusion region is at a different potential from the substrate. Although the ordinary leakage of reverse-biased diodes is usually negligible, BTBT(band to band tunnelling) and GIDL(gate induced drain leakage) can result in leakage currents that approach sub-threshold leakage levels in high-V_{th} transistors.

- Gate Leakage
  Gate leakage occurs when carriers tunnel through a thin gate dielectric when a voltage is applied across the gate (e.g., when the gate is ON). Gate leakage is an extremely strong function of the dielectric thickness.

There are different types of currents genrated due to different types of mechanisms. As shown in Figure 2.5, I_1 is diode leakage current, I_2 is sub-threshold leakage, I_3 is gate oxide tunnelling current, I_4 is gate current due to hot-carrier injection, I_5 is gate induced drain leakage current andI_6 is channel punch through current.

2.4 Energy

The power-delay product (PDP) is simply the energy. The minimum energy point is the least energy that an operation could consume if delay were unimportant [4]. It occurs in sub-threshold operation where $V_{DD} < V_t$. The minimum energy point typically consumes an order of magnitude less energy than the conventional operating point, but runs at least three orders of magnitude more slowly. John von Neumann first asserted that the "thermodynamic minimum of energy per elementary act of information" was $kTln2$ [27]. It was proved for CMOS by considering the minimum allowable voltage at which an inverter could operate. To achieve non zero noise margins, an inverter must have a slope steeper than -1 at the switching point, V_{inv},ie where $V_{out} = V_{in}$. For an ideal inverter with n = 1 in the sub-threshold characteristics, this occurs at a minimum operating voltage of 36mV at 300K. The energy consumed per cycle is

$$E_{switching} = C_{eff}V_{DD}^2 \tag{2.11}$$

where C_{eff} is the effective capacitance.

$$E_{leakage} = I_{sub} V_{DD} t_{cycle} \tag{2.12}$$

2.4.1 Energy Optimization and Performance

The total energy consumed in a digital circuit is the sum of leakage and dynamic energies ie

$$E_{total} = E_{dynamic} + E_{leakage} \tag{2.13}$$

The dynamic energy is associated with the computational power consumption of the circuit, while the leakage energy is the unwanted dissipated energy. For energy optimisation, we need to minimise the leakage energy as it is being wasted.

2.5 Controlling Power Dissipation:Design Idea

2.5.1 Logic Transitions

Due to dynamic power dissipation, the power mostly varies as V_{DD}^2 and one way of reducing it is to scale down the threshold voltage otherwise poor noise margins will occur. The sub threshold leakage current rises exponentially as the threshold voltage is reduced. The devices need to be designed to have threshold voltage that maximize the net reduction in dissipation[5]

2.5.2 Short Circuit Current

Transition component depends on the frequency or probability of the transition. This accounts for the power loss due to short circuit current.

2.5.3 Leakage Current

The static power dissipation is heavily dependant on gate leakage current. The ultra thin gate oxide layer leads to high gate oxide capacitance, which is the direct reason for improvement in the drive current and sub-threshold leakage. It requires the oxide layer to be electrically thin then the oxide layer can store charges and induce an electric field easily as a great capacitor of high value. On the other hand, the gate leakage current is mainly due to a quantum mechanical tunnelling of electrons which has nothing to do with an electrical issue but mainly to do with a wave-particle duality. Therefore, a physical thick layer could function as a barrier for tunnelling effectively. Hence, the gate oxide layer has to be electrically thin but physically thick in order to maintain the improvement introduced by an ultra thin oxide and to minimize the tunnelling effect as well.

As the supply voltage is reduced the power-delay product of the circuit decreases and delay increases monotonically. One way to change the delay of CMOS circuit is changing the W/L ratios, of the device in the circuit. If the interconnect capacitance is not significant then the power-delay product of an inverter driving another inverter varies with W/L. Hence there exists a combination of supply voltage and W/L ratio to provide optimal power delay product. The system level throughput can be kept satisfactory even after the scaling of supply voltage only by pipelining and parallelism. It compensates the increased delay but at the same time, introduces latency [the delay between cause and effect]. Overhead of control circuitry is also required to maintain such architectures and this again increase power consumption. In a dynamic circuit, energy per transition is given by $C_{load} V_{DD}^2$.
So power is energy per transition times the number of transition.
The number of transition depends on the probability of occurrence of an output from a given set of input.

2.6 Logic Styles

2.6.1 CMOS Logic Style

Logic gates in conventional or complementary CMOS (also simply referred to as CMOS in the sequel) are built from an NMOS pull-down and a dual PMOS pull-up logic network. In addition, pass gates or transmission gates (i.e., the combination of an NMOS and a PMOS pass-transistor) are often used for implementing multiplexers, XOR-gates, and flip-flops efficiently. Any logic function can be realized by NMOS pull-down and PMOS pull-up networks connected between the gate output and the power lines.

2.6.2 Pass Transistor Logic

The basic difference of pass-transistor logic compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines. The advantage is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation, which results in a smaller number of transistors and smaller input loads, especially when NMOS networks are used. However, the threshold voltage drop through the NMOS transistors while passing a logic "1" makes swing (or level) restoration at the gate outputs necessary in order to avoid static currents at the subsequent output inverters or logic gates. Adjusting the threshold voltages as a solution at the process technology level is usually not feasible for other reasons. In order to decouple gate inputs and outputs and to provide acceptable output driving capabilities, inverters are usually attached to the gate outputs [1].

2.6.3 Impact of Various Logic Styles

Based on a series of simulation studies it was concluded that the logic style used in logic gates basically influences the following:

- Delay: The circuit delay is determined by the number of inversion levels, the number of transistors in series, transistor sizes (i.e., channel widths), and intra- and inter cell wiring capacitances.
- Size: Circuit size depends on the number of transistors and their sizes and on the wiring complexity.
- Power dissipation: Power dissipation is determined by the switching activity and the node capacitances (made up of gate, diffusion, and wire capacitances), the latter of which in turn is a function of the same parameters that also control circuit size.
- Wiring complexity: Wiring complexity is determined by the number of connections and their lengths and by whether single-rail or dual-rail logic is used.

All these characteristics may vary considerably from one logic style to another and thus make the proper choice of logic style crucial for circuit performance.

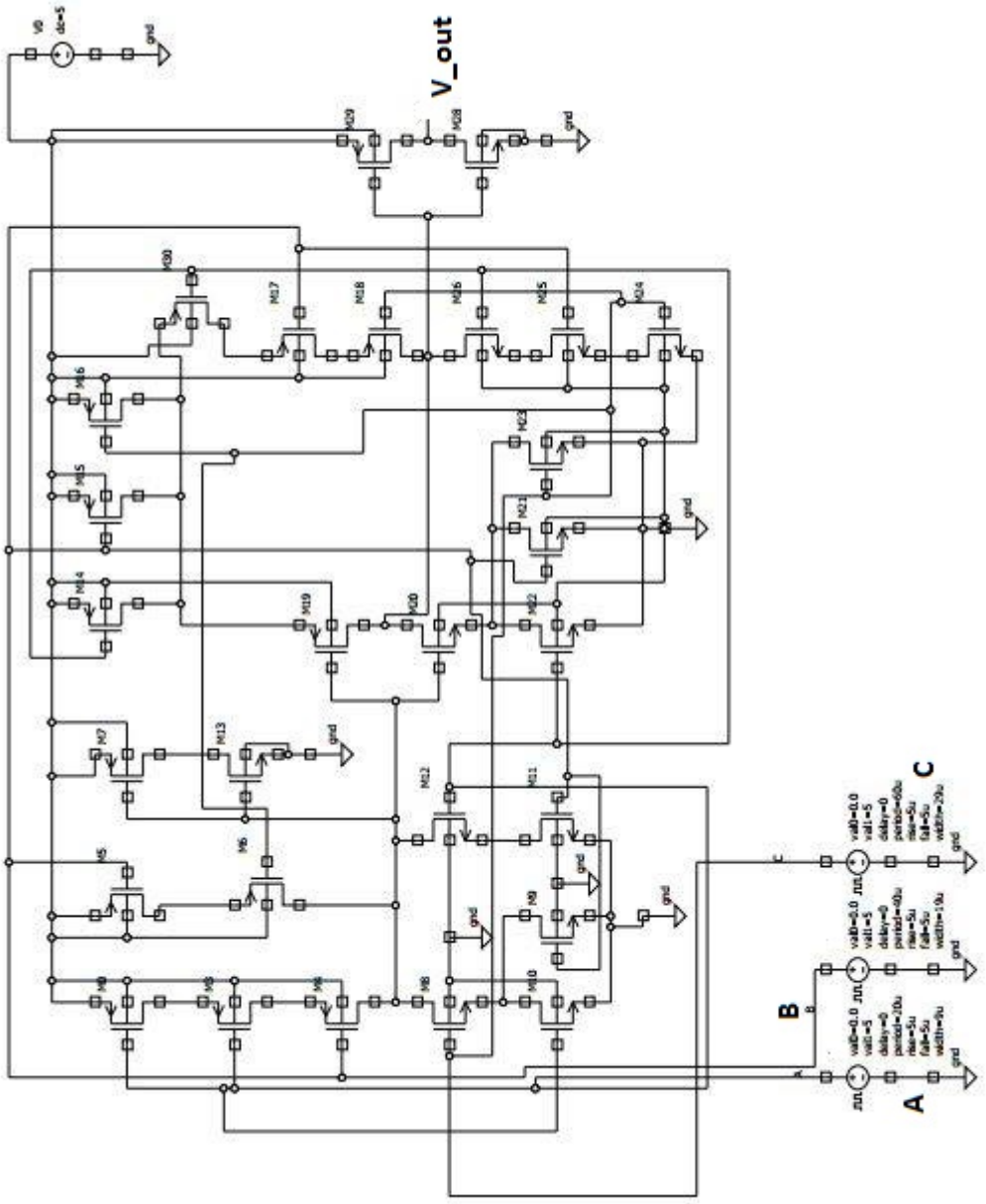

Figure 2.6: Circuit diagram of CMOS 3-bit adder

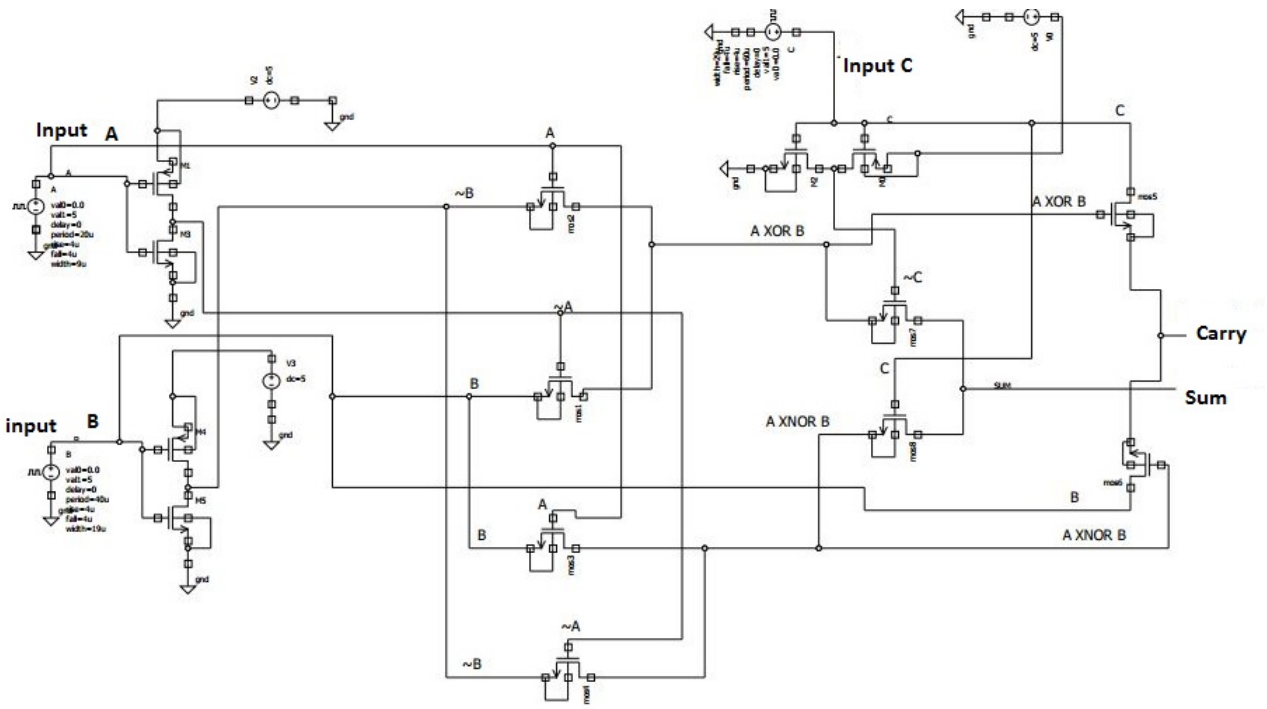

Figure 2.7: Circuit diagram of Pass Transistor 3-bit adder

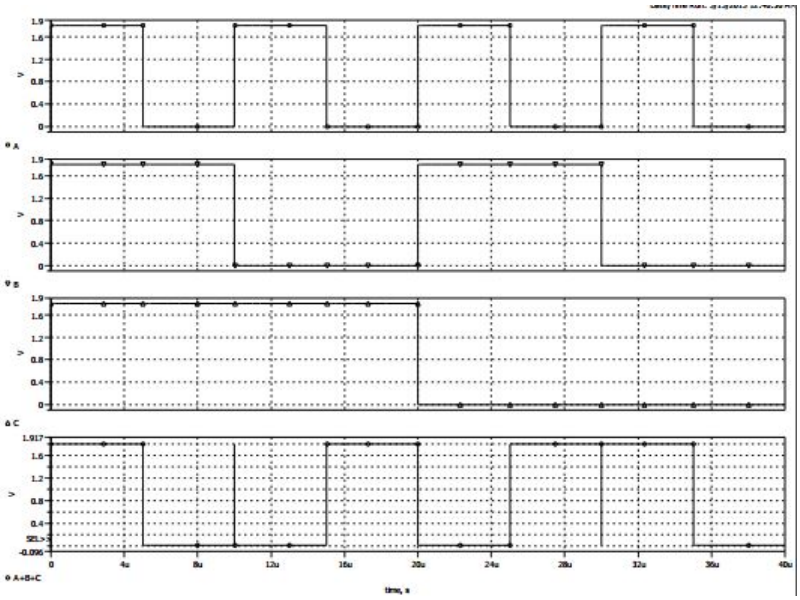

Figure 2.8: output of 3 bit adder in CMOS logic style

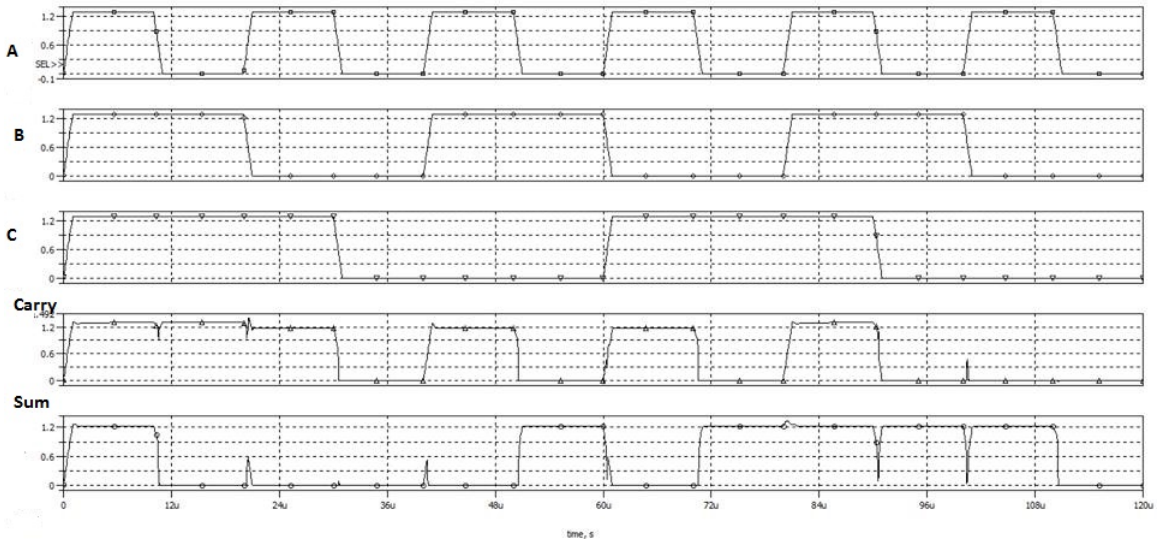

Figure 2.9: output of 3 bit adder in Pass transistor logic style

Table 2.1: Variation of rise time,fall time and propagation delay of Pass Transistor logic 3 bit adder SUM. All delay measurements are in μs. Here $t_p = (t_{PLH} + t_{PLH})/2$

For all ips(A,B,C)	Rise time t_r	Fall Timet_f	$(t_r + t_f)/2$	t_{PLH}	t_{PHL}	t_p
1	0.29	0.35	0.32	0.14	0.054	0.097
2	0.57	0.83	0.7	0.275	0.056	0.17
3	0.86	1.29	1.075	0.412	0.018	0.215
4	1.14	1.77	1.455	0.55	0.020	0.285
5	1.43	2.26	1.846	0.685	0.026	0.36

2.6.4 Results

The data in Table 2.1 is given for Pass Transistor logic.
ANALYSIS:
INPUT A $period = 20\mu s, Risetime = T_r, Falltime = T_f$
INPUT B $period = 40\mu s, Risetime = T_r, Falltime = T_f$
INPUT C $period = 60\mu s, Risetime = T_r, Falltime = T_f$
Output Sum $-V_H = 1.3V, V_L = 4nV \approx 0V, V(90\%) = 1.17V, V(10\%) = 0.13V, V(50\%) = 0.65V, t_r, t_f, t_{pLH}, t_{pHL}, t_p$
All time is in microseconds The data in Table 2.2 for is given for static CMOS logic.

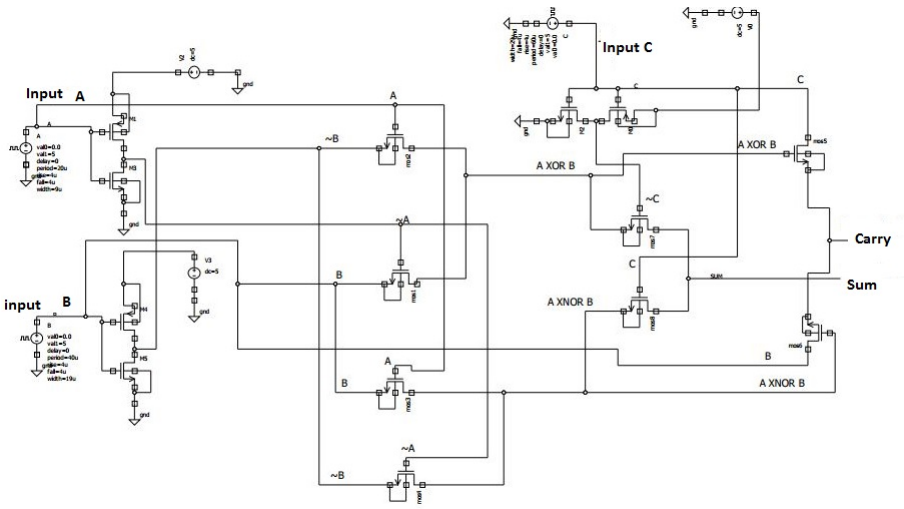

Figure 2.10: Circuit diagram of Pass Transistor 3-bit adder

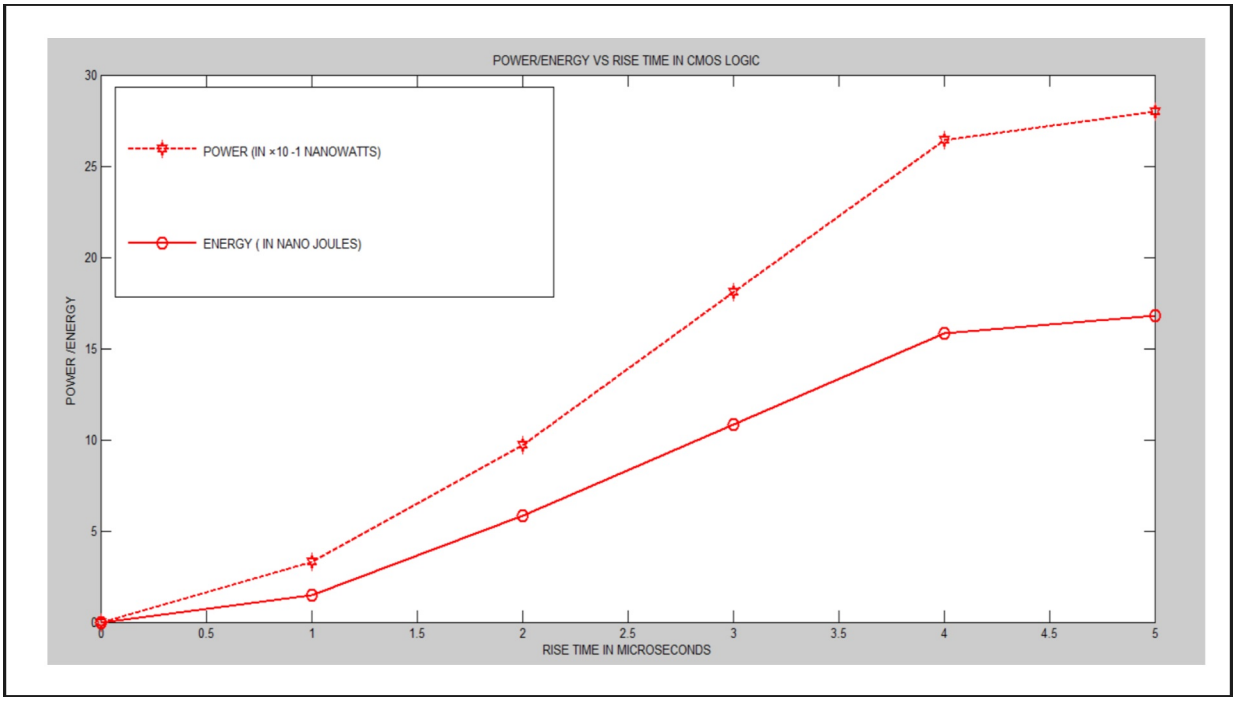

Figure 2.11: Power and Energy vs input rise time in CMOS adder

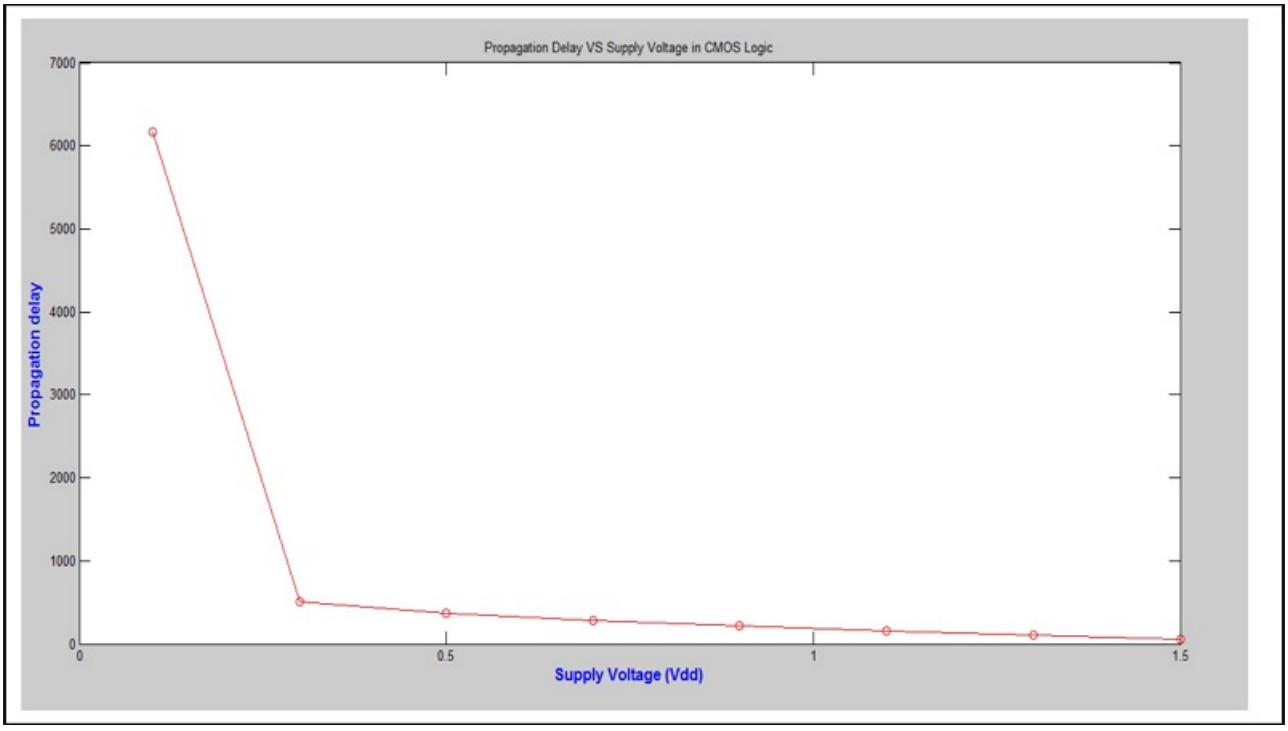

Figure 2.12: Delay vs V_{DD} in CMOS 3 bit adder

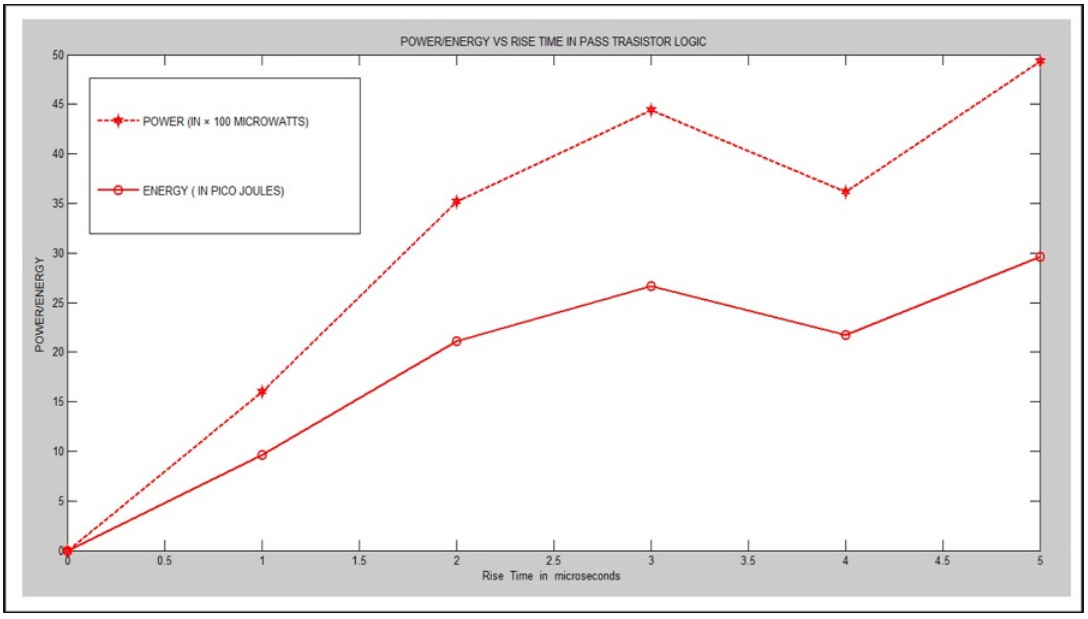

Figure 2.13: Power and Energy vs input rise time in pass transistor adder

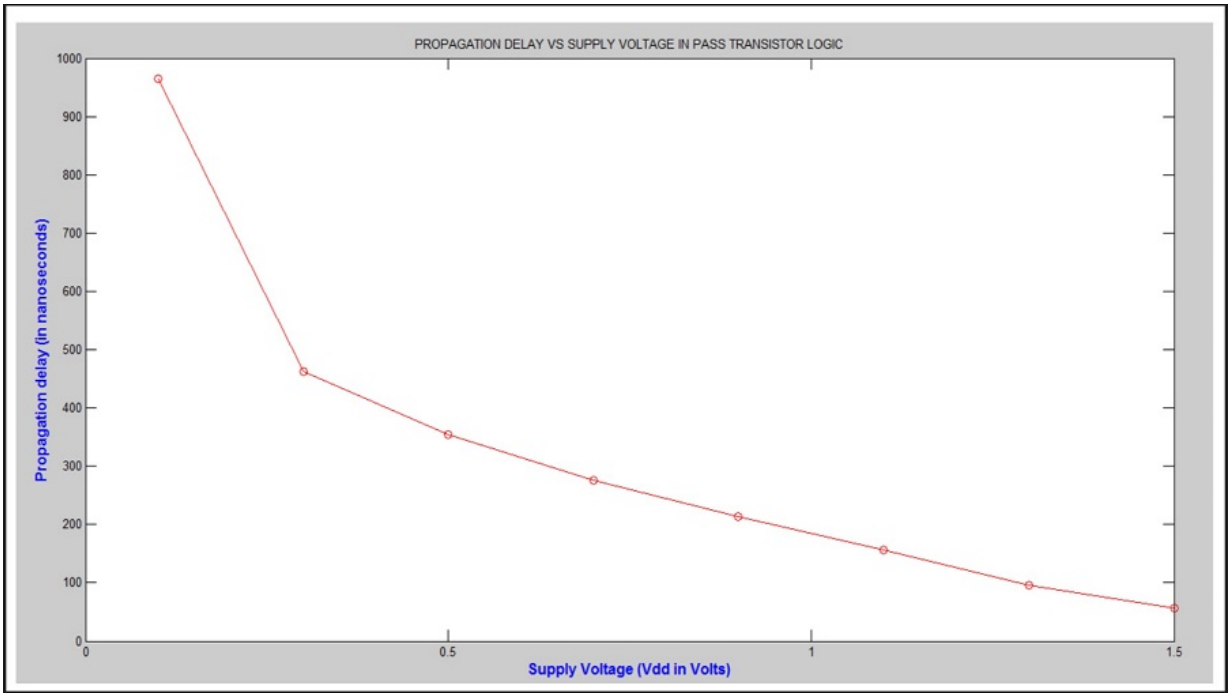

Figure 2.14: Delay vs V_{DD} in Pass Transisitor 3 bit adder

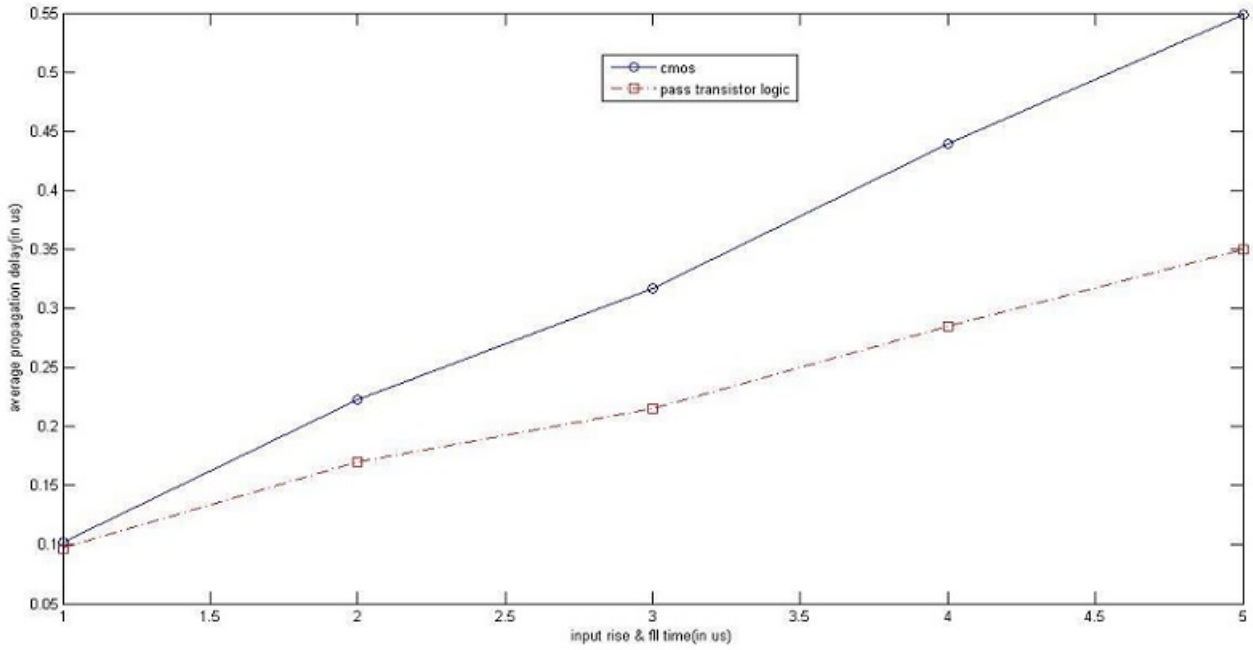

Figure 2.15: Dependence of output propagation delay on input rise and fall time

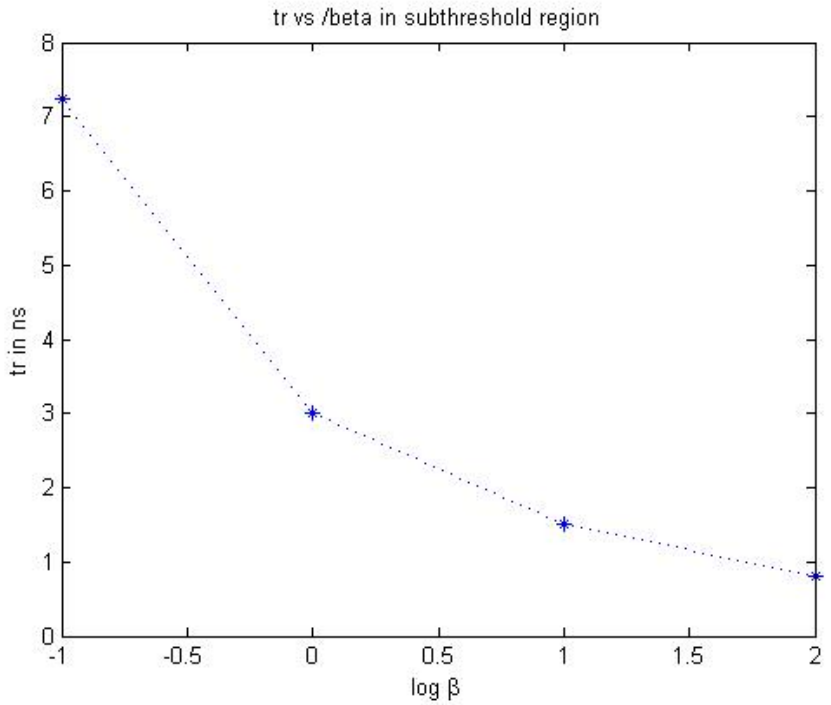

Figure 2.16: Variation of rise time with change in β in sub treshold region

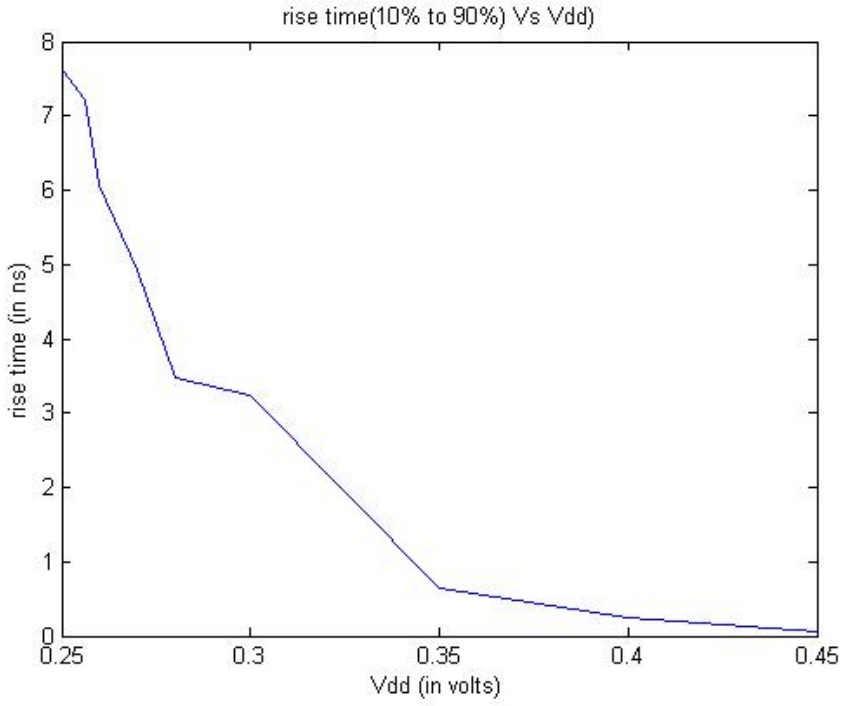

Figure 2.17: Variation of rise time with change in V_{DD} in sub treshold region

Table 2.2: Variation of rise time,fall time and propagation delay of CMOS logic 3 bit addder SUM

For all ips(A,B,C)	Rise time t_r	Fall Timet_f	$(t_r + t_f)/2$	t_{PLH}	t_{PHL}	$t_p = (t_{PLH} + t_{PLH})/2$
1	0.57	6.11	3.34	138.72	66.40	102.55
2	0.97	12.14	6.55	295.20	151.36	223.28
3	1.35	18.49	9.92	442.89	191.83	317.36
4	1.65	24.31	12.99	582.33	295.60	438.92
5	2.01	30.32	16.16	721.71	374.88	548.30

Table 2.3: Variation of Power , Energy and Delay with respect to change in Rise and Fall time in CMOS 3 bit adder

Rise time (μs)	Power (mW)	Energy(nJ)	Delay(μs)	Power Delay Product (pJ)
1	0.033	1.98	0.103	3.201
2	0.097	5.82	0.223	21.63
3	0.181	10.86	0.317	57.377
4	0.264	15.84	0.439	115.89
5	0.28	16.8	0.548	153.44

2.6.5 Observations

As the Input rise and fall times(rise time = fall time) increases Power, energy and power delay product also increases.
Also with the increase in rise and fall times of the input, the output(SUM) Propagation delay increases. These are the cases in CMOS and Pass Transistor Logics. Supply voltage(V_{DD}) was also varied. As the supply voltage increases, the propagation delay decreases and for small V_{DD} values in the decrease were exponential.
The Subthreshold Region was also explored in the simulation. The transfer characteristics of CMOS inverter in Subthreshold region was obtained.As the Drain voltage increased, the curve is more steeper showing the decrease in Transition width. As the Supply voltage was varied, the output rise time decreases. As the ratio of the Channel lengths of NMOS to PMOS (β) increased, the rise time of the output decreased.

Table 2.4: Variation of Power , Energy and Delay with respect to change in Rise and Fall time in Pass Transistor 3 bit adder

Rise time (μs)	Power (mW)	Energy(nJ)	Delay(μs)	Power Delay Product (fJ)
1	0.16	9.6	0.097	15.52
2	0.352	21.12	0.17	59.84
3	0.444	26.64	0.215	95.46
4	0.362	21.72	0.285	103.17
5	0.493	29.58	0.36	177.48

V_{DD} (V)	t_{PLH}(ns)	t_{PHL}(ns)	Propagation dalay $t_p = \frac{t_{PLH}+t_{PHL}}{2}$ (ns)
1.5	34.86	79.3	57.08
1.3	54.23	138.2	96.215
1.1	131.8	181.47	156.63
0.9	197.83	230.3	214.06
0.7	265.1	285.42	275.26
0.5	346.7	360.45	353.57
0.3	453.7	472.40	463.05
0.1	1080	849.5	964.5

Table 2.5: Variation of Propagation delay with the change in V_{DD} in Pass Transistor logic 3 bit adder

Table 2.6: Variation of Propagation delay with the change in V_{DD} in CMOS 3 bit adder

V_{DD} (V)	t_{PLH}(ns)	t_{PHL}(ns)	Propagation dalay $t_p = \frac{t_{PLH}+t_{PHL}}{2}$ (ns)
1.5	1.33	102.85	52.09
1.3	66.4	138.72	102.55
1.1	149.7	155.1	152.35
0.9	213.7	233.68	223.44
0.7	276.6	299.88	288.24
0.5	357.6	387.02	372.31
0.3	478.99	541.7	510.345
0.1	2570	9770	6170

Table 2.7: Variation of output rise time with change in NMOS to PMOS ratio (β) in sub threshold region

β	t_r(ns)
0.1	7.223
1	3
10	1.5
100	0.798

2.7 Summary

Based on the above simulation experiments, the relation between Power,Energy and delay can be inferred. The problem of power dissipation is due to switching activity and leakage current.

Table 2.8: Variation of t_r with respect to change in V_{DD} in sub threshold region

V_{DD} (V)	t_r (ns)
0.25	7.62
0.256	7.22
0.26	6.06
0.27	4.93
0.28	3.474
0.3	3.23
0.35	0.636
0.4	0.254
0.45	0.05

Switching activity accounts for 80% of power dissipation in modern MOS circuits.Power can be estimated by statistical or simulational methods. While statistical methods require intensive computation for a large model, the simulational methods are slow and expensive for large circuits. Further power optimisation should not offset other aspects of circuit like noise margins. Switching power is due to logical transitions and glitching activities. Glitches arise when there are two paths with different delay as input to some other gates. This analysis assumes negligible gate capacitances so the dynamic power dissipation can be given by $\alpha V_{dd}^2 C_L f$. The transition component of the dissipation depends upon signal probabilities or the probability of occurrence of transitions.
While simulating different logic styles static is preferred over dynamic because the dynamic designs require a clock overhead and are mostly high speed in nature so they exhibit a high power dissipation due to high signal transition activities due to pre-charging mechanisms.
Sub-threshold operation of inverters show that the operating current is equivalent to the leakage current,so power dissipation is low. Pass transistor Logic performs better in terms of propagation delay in terms of static CMOS due to smaller input loads, that can be verified in simulations. Less power is consumed by Pass Transistor logic style with respect to CMOS with variation in input rise and fall time. The power delay product of the Pass Transistor Logic is less in 3 orders of magnitude than CMOS.
Delay estimation is a prime concern while designing low power circuits because performance has to be quantified. While the rigorous mathematical models do give a very accurate result, yet simpler delay calculation model like logical Effort, is more popular as a back of an envelope design. The next chapter describes the details of logical effort.

Chapter 3

Logical Effort Approach

3.1 Introduction to Logical Effort

Delay estimation in a circuit is a very onerous task. First hand delay approximation provides an insight in the performance of the circuit. There are many models for delay approximation but among all of them Logical Effort method is the most simplest and widely used. It is not extremely accurate but designs based on logical effort are far more closer to the desired performance. Further modifications have been incorporated in basic Logical Effort design in order to make it more accurate. Calculation of delay by the method of Logical Effort gives a process independent estimate of delay

$$d_{abs} = \tau d \tag{3.1}$$

Here d is the delay calculated through logical effort which is independent from a particular technology of MOSFETs. To calculate the delay corresponding to a particular manufacturing technology it is multiplied with τ_0 which is the delay of a inverter driving an identical inverter of the same process. [7].

3.1.1 Basic Definition

Different definitions of Logical Effort have been summarized below. Each definition explains a different perspective for the term.

- The logical effort of a logic gate is defined as the number of times worse it is at delivering output current than would be an inverter with identical input capacitance. It is based on the fact that as the gates become more complex the input capacitances increase, because of network of PMOS and NMOS that are connected in series, parallel or mixed. Also a series combination of MOSFETS conduct poorly as compared to a single MOSFET (the analogy between a complex gate and an inverter, because in charging/discharging of an inverter only one transistor is involved in conducting current, while a possible series combination may conduct in the complex gate). Hence Logical Effort quantifies the effect of complex gates in terms of the output current.

- The logical effort of a logic gate is defined as the ratio of its input capacitance to that of an inverter that delivers equal output current. This definition is used to numerically calculate logical effort of a gate. It provides an insight in the input capacitance of a gate thus the overall complexity of the gate is quantified.

- The logical effort of a gate is defined as the slope of the gates delay vs. fanout curve divided by the slope of an inverters delay vs. fanout. This is the graphical interpretation of logical effort. The slope of delay vs fan-out curves are positive because as the fanout

increases the delay also rises. This ration determines the rate of rising of this slope with that of a characteristic inverter. curve [7].

3.1.2 Elements of Logical Effort

The logical effort expression is:

$$d = f + p \tag{3.2}$$

The delay of a gate is the sum of effort delay (f) and parasitic delay (p). The effort delay depends on the characteristics of the gate. The parasitic delay is directly proportional to the number of inputs of the gate. The stage effort can be further expressed as the product of logical effort(g) and electrical effort(h).

$$d = (g \times h) + p \tag{3.3}$$

The electrical effort is the ratio of the output capacitance of the gate to that of input capacitance.

$$h = \frac{C_{out}}{C_{in}} \tag{3.4}$$

The input capacitance is calculated for an individual input signal, by adding the widths of

Table 3.1: Logical effort(g) for standard CMOS gates with varying input an $\gamma = 2$. $\gamma = \frac{\mu_n}{\mu_p}$,the ratio of mobility of electron to hole.

Gate Type	1	2	3	4	5	n
Inverter	1					
NAND		4/3	5/3	6/3	7/3	(n+2)/3
NOR		5/3	7/3	9/3	11/3	(2n + 1)/3
Multiplexer		2	2	2	2	2
XOR (parity)		4	12	32		

the transistor, that it is connected to. In a same way input capacitance can be calculated for a bundle of signal or the entire circuit.
In a multi -stage circuit the output capacitance of a gate acts as a input capacitance for the next stage gate. These loads also include the stray capacitance of wires, drain regions of transistors, etc. Capacitance of a transistor is directly proportional to the area of the gate. In any technology the length is always fixed. As a result of this the capacitance becomes directly proportional to the width of the transistor. Hence the electrical effort can also be expressed as width ratio.
The parasitic delay corresponding to a gate is always fixed. It is independent of size of logic gate and load capacitance it drives. The primary reason behind this is that wider transistors have diffusion capacitance [8]. The major contributor in the parasitic delay is the the source/drain regions capacitance of the transistors that drive the gate of the output.

3.1.3 Logical Effort in Multi Sage Circuits

A multi-stage circuit consists of different type of logical functional units either connected in series or parallel. To calculate the logical effort in a multi stage circuit first a critical path is chosen. Critical path is the path along which the delay is assumed to be highest theoretically. Once the maximum delay is known the circuit can be calibrated with respect to this delay. The delay in a multi stage circuit is given by [7]

$$\hat{D} = NF^{\frac{1}{N}} + P = \sum(g_i h_i + p_i) \tag{3.5}$$

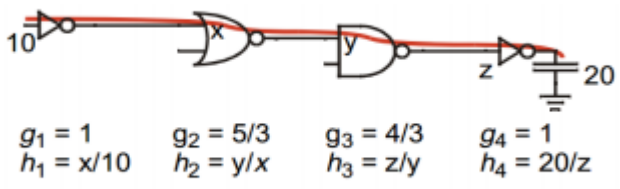

Figure 3.1: A multi stage circuit

where F is the effort of a single gate is given by:$F = G \times B \times H$.
G, B and H are path logical effort, branching effort and path electrical effort respectively.

Path Logical Effort:$\mathbf{G} = \prod g_i$
Path Electrical Effort: $\mathbf{H} = \frac{C_{out}}{C_{in}}$
Branching Effort: $\mathbf{B} = \frac{C_{on-path}+C_{off-path}}{C_{on-path}}$
The concept of logical effort helps to find the optimal number of stages in a complex circuit [8]. Once effort by each stage is equalized the delay can be further minimized by optimization of number of stages.
considering a circuit performing a logical function has n_1 stages and there is another path consisting of inverter chain containing n_2 gates. The total number of gates is $N = n_1 + n_2$. The minimum delay of the N stages is the sum of the delay in the logic stages and in the inverter stages:

$$\hat{D} = NF^{\frac{1}{N}} \left(\sum_{i=1}^{n_1} p_i \right) + (N - n_1)p_{inv} \tag{3.6}$$

This expression consists of three terms. the first term is delay across N stages obtained by distributing effort equally. The second term is the parasitic delay of the logic stages. Similarly the third term is the parasitic delay of the inverters. Differentiating it with respect to N and setting to Zero.

$$\frac{\partial \hat{D}}{\partial N} = -F^{\frac{1}{N}} ln(F^{\frac{1}{N}}) + F^{\frac{1}{N}} + p_{inv} = 0 \tag{3.7}$$

The solution of the equation $\hat{N}$ gives the number of stages to use to obtain least delay.

3.2 Model of a Logic Gate

An electrical model of an gate approximates the behaviour of a gate as as static circuit. Figure 5.2 shows an input signal loaded by a capacitance C_{in}, the capacitance of the transistor gates connected to the input terminal. The voltage at the input terminal will decide whether transistor is in on condition or off condition. If the upper switch conducts then the output voltage will be high through R_{ui}. R_{ui} is the pull-up modelled resistance [10]. If the lower switch conducts then the output will be low though R_{di}. Here R_{di} is the pull-down transistor modelled resistance. The output capacitance is the sum of two different capacitances. C_{pi} is a parasitic capacitance associated with the internal characteristics of the gate. C_{out} is the load capacitance associated with the gate is to drive. C_{in}, C_{pi}, R_{ui} and R_{di} are used to model

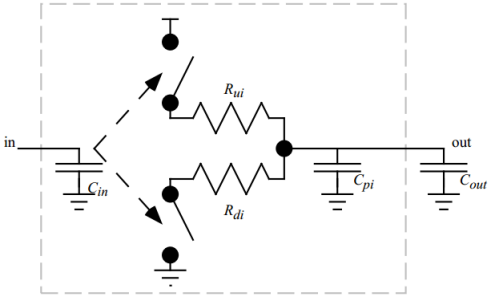

Figure 3.2: A simple model for a 1 input gate driven either HIGH or LOW

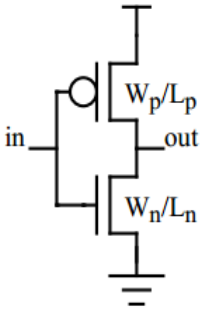

Figure 3.3: A sample inverter gate

a logic gate and these elements depends on the logic function also. To obtain a particular logic gate the width of all transistors are scaled with a sample inverter gate (Figure 3.3). This scaling factor (α) is used to model the parameters of transistors.

$$C_{in} = \alpha C_t \tag{3.8}$$

$$R_i = R_{ui} = R_{di} = R_t/\alpha \tag{3.9}$$

$$C_{pi} = \alpha C_{pt} \tag{3.10}$$

Here C_t, C_{pt} and R_t are the input capacitance, parasitic capacitance and equal pull-up and pull-down resistors of the sample gate respectively. The scaling of the template increases the widths of all transistors by the factor α leaving the transistor lengths unchanged.

The proposed model gate for logic gate easily relates with the the inverter.The n type pull-down transistor with width W_n and length L_n is modelled by the switch and resistor R_{di}. Similarly p type pull-up transistor is modelled by the switch and the resistor R_{ui} connecting to positive power supply. The input signal is loaded by the capacitance formed by the gates of both transistors, which is proportional to the area of the transistor gates:

$$C_t = k_1 W_n L_n + k_1 W_p L_p \tag{3.11}$$

where k_1 depends on the fabrication process. The resistances are determined by

$$\frac{1}{R_t} = \frac{k_2 \mu_n W_n}{L_n} + \frac{k_2 \mu_p W_p}{L_p} \tag{3.12}$$

where k_2 is a fabrication dependent variable. μ indicates the mobilities of p and n type transistors. This model can be easily related to other type of gates rather than only inverter.

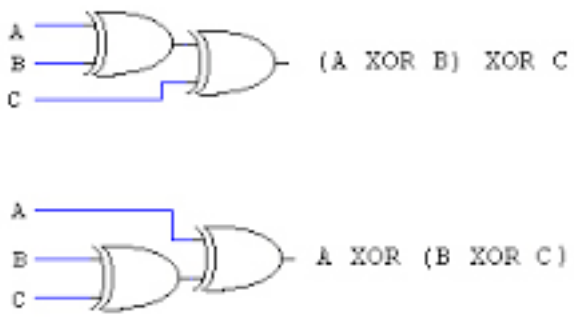

Figure 3.4: 1 Bit Adder Logic Gate

The circuit of the logic gate is a network of source-to-drain connections of transistors such that the output of the logic gate can be connected either to the power supply or to ground, depending on the voltages present on the input signals that control the transistors in the network. The pull-up and pull-down resistances shown in the model are the effective resistances of the network when the pull-up or pull-down path is active [7]. Hence the delay in a logic gate can be assumed to be only RC delay contributed by charging and discharging the capacitance attached to the output node.

$$\begin{aligned} d_{abs} &= \kappa R_i(C_{out} + C_{pi}) \\ &= \kappa(R_t/\alpha)C_{in}(C_{out}/C_{in}) + \kappa(R_t/\alpha)(\alpha C_{pt}) \\ &= (\kappa R_t C_t)(C_{out}/C_{in}) + \kappa R_t C_{pt} \end{aligned}$$

Here κ is fabrication dependent parameter. From the above equations all the logical effort parameters can be obtained.

$$\begin{aligned} d_{abs} &= \tau(gh + p) \\ \tau &= \kappa R_{inv} C_{inv} \\ g &= \frac{R_t C_t}{R_{inv} C_{inv}} \\ h &= \frac{C_{out}}{C_{in}} \\ p &= \frac{R_t C_{pt}}{R_{inv} C_{inv}} \end{aligned}$$

where C_{inv} and R_{inv} are the capacitance and resistance of the pull-up or pull-down transistor in sample gate.

3.3 DESIGN of SUM section in 1 bit adder using Logical Effort

The logical effort of a 2-in XOR gate is 4,while its parasitic delay is 4. from Figure 5.4 the parasitic delay including two stages is given as $4 + 4 = 8$. The logical effort of path is G= 4×4. The branching effort B is 1, and the electrical effort depends on the output load of the circuit. So the total stage effort is obtained as $F = GBH = 16H$. The optimal stage

effort is obtained as $\sqrt{F} = \sqrt[4]{H}$ as the total number of stages is 2. Total delay is obtained as $\hat{D} = N.F^{1/N} + P$ where $N = 2$ and $P = 8$. Delay is $\hat{D} = 8(\sqrt{H} + 1)$. The parameter H is a design specification and it is the pre-layout Load capacitance for a first approximation.This may be input capacitance of next stage or final output load.

$H = C_{out}/C_{in}$	d (normalized delay)
1	8
10	33.29
100	88
1000	260

Table 3.2: Variation of delay with change in Electrical effort(H)

The values of delay for different values of H (total electrical effort) are shown in Table 3.2

3.4 Expression for capacitance of second stage

The capacitance at first stage i.e. input and at the output is denoted as $C_{in1} and C_{in2}$ respectively. The value of optimal stage effort is $f = (GBH)^{1/N}$. Also,
$g.h_{opt} = f$ i.e.

$$\begin{aligned} g.h_{opt} &= f \\ h_{opt} &= 4(\sqrt{C_{out}/C_{in1}})/4 \\ h_{opt} &= \sqrt{C_{out}/C_{in1}} \\ C_{out}/C_{in2} &= \sqrt{C_{out}/C_{in1}} \\ C_{in2} &= \sqrt{C_{out}.C_{in1}} \end{aligned}$$

Thus, the input capacitance of second stage is the geometric mean of the output and input capacitances of the sum section respectively.

3.5 Design Using Buffers:

The delay obtained in previous design can be further reduced at the cost of inserting an even number of inverters as a buffer to drive loads better.
In this stage the number of stages becomes $N_b = 2 + 2n$ where $2n$ is the number of inverters inserted.In this case
Total logical effort $G = 16$ (inverter has LE=1).
The Branching effort is also ie B=1.
The parasitic delay is $p_{buffer} = 8 + 2n$. Let N_b be the total number of stages in this case.
Then total delay is given as
$d_{buffer} = N_b.(GBH)^{1/N_b} + p_{buffer}$. H is the design specification and now there is a control parameter namely N_b to reduce the delay.
The total delay is calculated as
$d_{buffer} = (2+2n).(GBH)^{1/2+2n} + p_{buffer}$. i.e. $d_{buffer} = (2+2n).(16H)^{1/2+2n} + 8 + 2n$ Delay for different values of H and n has been calculated.

3.5.1 Expression for capacitance of second stage:

A similar analysis as presented before gives the expression for the capacitance of the second stage as follows

$$C_{in2} = 4C_{out}.(16C_{out}/C_{in})^{-(2+2n)} \tag{3.13}$$

No of stages	d(Normalized Delay)			
n	d(H=1)	d(H=10)	d(H=100)	d(H=1000)
1	18	24.22	35.298	41.809
2	21.52	25.27	32.51	35.90
3	25.31	29.08	34.11	36.55

Table 3.3: Delay variation with number of stages and Electrical Effort (H)

Table 3.3 shows the value of delay for different values of H, with a inverter buffer design. A similar analysis can be found on the carry section of the static adder if implemented as a two stage NAND gate implementation [10] .
In order to check the parasitic elements associated with the 28T adder circuit, its layout was implemented in Cadence Layout Editor. Both pre layout simulation and and post layout simulation was performed to check the deviation from the ideal schematic conditions.

3.6 Limitation of Logical Effort

Logical effort is a very simple model. It does not take into account any type of flaws or non ideal behaviour in the model. But this model has many limitations. The RC model approach is very simple in nature. It does not take into account effects of variable rise times and velocity of saturation. Fortunately , rise times tend to be about equal in well-designed circuits with equal effort delays and velocity saturation can handled by characterizing logical effort of gates with simulation. Logical effort approach only takes into account delay. It does not considers other design parameters such as power, design area, power delay product. It also does not provide closed form solution in case of branching and multiple number of stages. In such cases many iterations are required to get the correct approximate value. Iterations are also required in all those cases in which interconnect capacitance is comparable to gate capacitance [11]. In many cases the complexity of circuit creates problem and it is difficult to find a accurate approximate. In a general case a path is needed to calculate the path logical effort i.e. G, but without calculating G number of stages is not known [8]. This problem is also known as Chicken and Egg problem. But the biggest problem related with Logical effort approach is that it neglects the delay due to interconnects. Interconnects also play a very big role in delay in circuits. In the modern era when there are billions of transistors on a chip, interconnect delay is a important parameter and cannot be neglected [10]. To overcome these problems logical effort model is developed further. The given figure models interconnects as $\pi-$model.

According to this improved model, propagation delay

$$t_p \propto L\sqrt{(R_dC_d)(r_wc_w)} \tag{3.14}$$

with R_dC_d and r_wc_w intrinsic delays of inverter and wire, respectively. The study and simulation of effect of interconnect length on propagation delay was done. A drastic effect of interconnect was found on propagation delay. The observations has been shown in Table 3.4. The output changes in a vary uneven manner with increase in interconnect length.

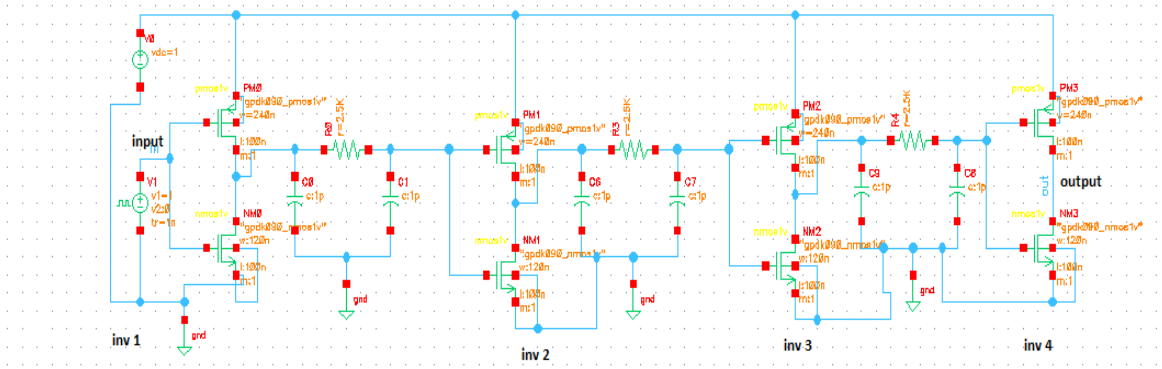

Figure 3.5: A 4 inverter chain with interconnects modelled as $\pi-$model [10]

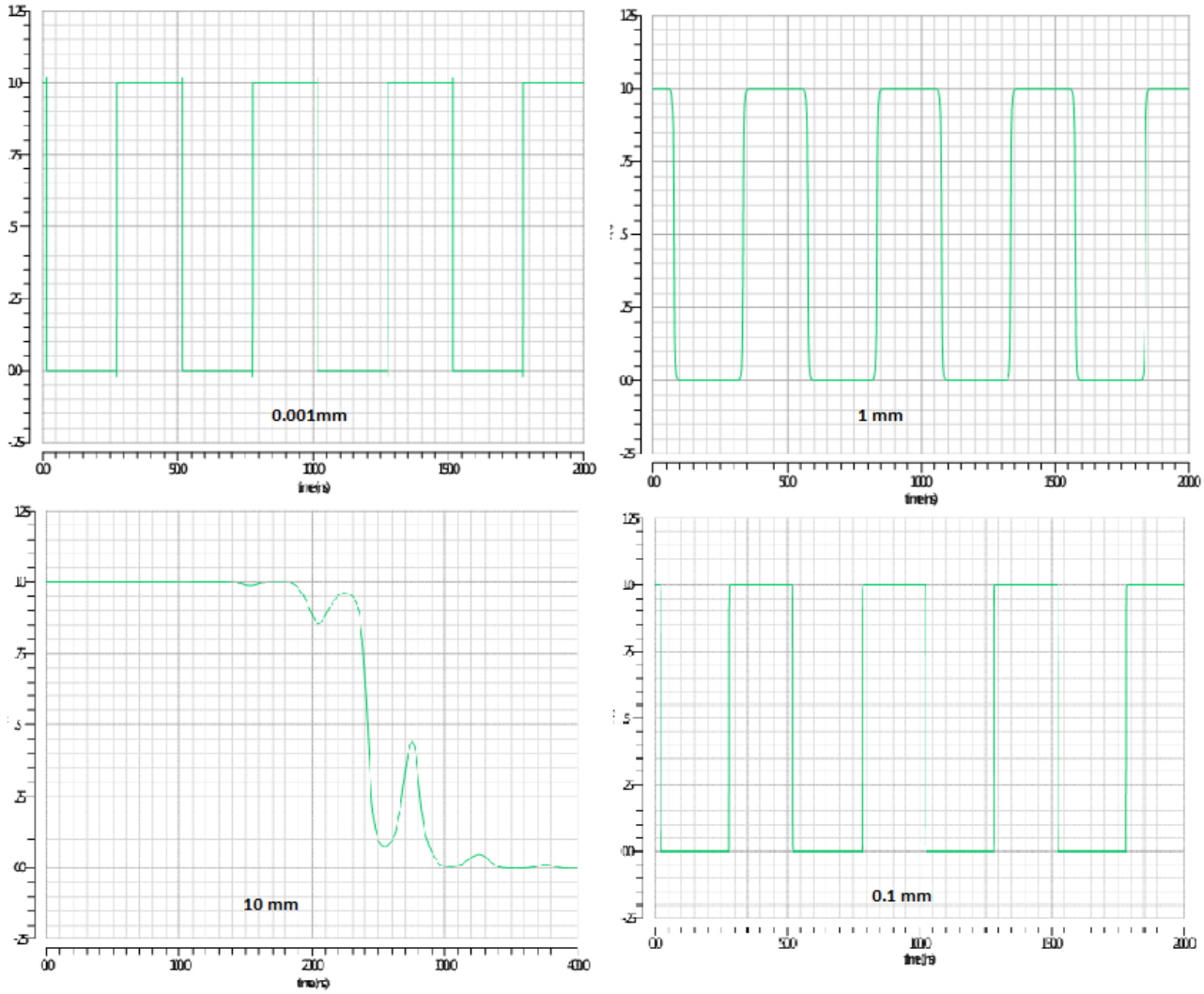

Figure 3.6: The output of a 4 chain inverter gate with variation in interconnect length. The interconnect lengths from top left are 0.001mm, 1mm, 10mm and 0.1mm respectively.

Length of interconnect (mm)	Propagation Delay,t_p (ns)
0 (ideal)	0.13
0.001	0.14
0.01	0.22
0.1	0.83
1	6.12
10	240.20

Table 3.4: Propagation delay variation with interconnect length. The readings were taken four a 4 inverter chain shown in figure in 90nm technology where $r_w = 250\Omega/mm$; $c_w = 200fF/mm$ and $t_p = 0.69 r_w c_w L^2$ [9]

3.7 Summary

Logical effort is a novel technique employed to size circuits in order to drive loads that are relatively large than the usual input capacitances. This requires the calculation of logical effort that is defined as the ratio of the input capacitance of a gate with respect to that of an inverter The method of logical effort was coined by Ivan Sutherland and Bob Sproull in 1991. It establishes a link to design circuits on the basis of the varying output capacitances. A 1 bit adder was implemented using two XOR gates and their respective capacitances were calculated using the Logical Effort approach. In the above sections it was also established that delay increases due to increase in output load.

The conventional method of logical effort fails as the size of the devices continue to shrink and the length of interconnects scales to the device parameters. The conventional Logical Effort fails to account for the reactances in the wire and it leads to an unsuitable estimation. It was shown via simulation that that logical effort is not an acceptable solution where interconnect length is taken in account. It was clearly shown through various graphs which show high deviation under high interconnect length.
Since logical effort only deals with delay parameter, it cannot be used alone to design a low power circuit. For a low power circuit the leakage currents should be minimized. These topics will be covered in next chapter. Design of low power can be accomplished by power gating. In this method we provide power supplies (ie V_{DD} and ground) to the pull-up and pull-down circuits via a switch which is itself a PMOS or NMOS. This ensures that when the circuit has no operations to perform, the switch can be turned off and hence static power dissipation can be reduced. There are delay penalties and also the sizing of the switch is to be done so that it sources/sinks required current even in the worst case. The next chapter, elucidates more about the idea of power gating.

Chapter 4

Sleepy Keeper Approach

4.1 Introduction to Sleepy Keeper approach

This is a new technique for providing low leakage in the circuit design. In this approach, the output logic state remains exact while minimizes the leakage current. Sleepy Keeper circuit has two additional transistors with the Normal Sleep Transistors. Also two values of V_{th} can be used in the sleepy keeper circuit which decreases the Sub-threshold leakage current significantly [12].

4.2 Various Approaches:

4.2.1 Sleep approach

The traditional method for low sub-threshold leakage power is Sleep approach. In this configuration, two transistors are used as shown in figure. One Sleep PMOS transistor is placed between V_{DD} and the pull-up network and an additional Sleep NMOS transistor is between pull down network and Ground. The sleep transistors are in ON state when the circuit is Active and are in OFF state when the circuit is idle.

This reduces the power due to leakage when circuit is in off or stand by mode. But the disadvantage is that the Output node is still floating and results in false results.

4.2.2 Leakage feedback approach

In this technique two extra transistors are used to maintain the logic state during Sleep mode [14]. The transistors are connected to the output of an inverter which is ridden by Output of the circuit as shown in figure. Also a PMOS transistor and a NMOS transistor are placed

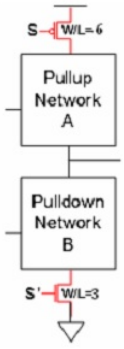

Figure 4.1: Leakage feedback approach

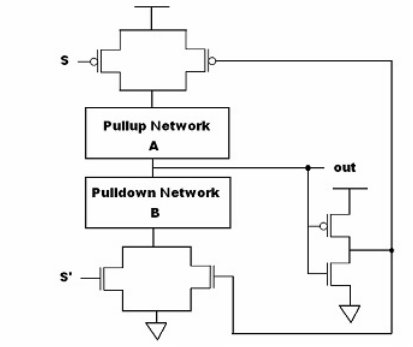

Figure 4.2: Leakage feedback approach

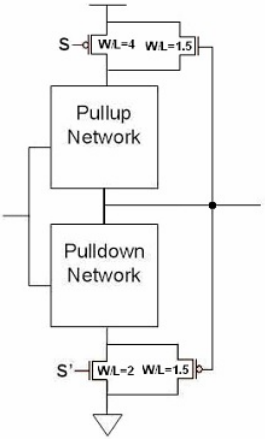

Figure 4.3: Sleepy keeper approach

parallel to the Sleep transistors.Under Sleep mode, sleep transistors are turned off and one of the transistors in parallel to the sleep transistors stay connected with the power supply line. Dual V_{th} technology can be used to get greater power reduction.

Large V_{th} is applied to leakage reduction transistors (Sleep transistors) , and to transistors in parallel. Low- V_{th} is applied to the remaining transistors to maintain output logic levels.

4.2.3 Sleepy Keeper approach

The issue with traditional CMOS is that the transistors are used only in their inverting way: namely, PMOS transistors connect to V_{DD} and NMOS transistors connect to GND. It is well known that PMOS transistors are inefficient at passing GND. Similarly the case with NMOS transistors which are not efficient at passing V_{DD}. However, in order to maintain a value of 1 in sleep mode, the sleepy keeper approach uses the output value of 1 and the NMOS transistor connected to V_{DD} to maintain output value equal to 1 when in sleep mode [12].

An additional single NMOS transistor placed in parallel to the pull-up Sleep transistor joins V_{DD} to the pull-up network. In the Sleep mode, this NMOS transistor is the only source of V_{DD} to the pull-up network since the sleep transistor is off.

Similarly, to hold a value of 0 in sleep mode, the sleepy keeper approach uses the output value of 0 and a PMOS transistor connected to GND to maintain output value equal to 0 when in Sleep mode. As shown in Figure.

Here, An additional single PMOS transistor placed in parallel to the pull-down sleep transistor is the only source of GND to the pull-down network.

For this approach to work, the NMOS connected to V_{DD} and the PMOS connected to GND

Type	Static Power (nW)
Sleep approach	0.44
Leakage feedback approach	0.53
Sleepy Keeper approach	0.13

Table 4.1: Static Power Dissipation in various modes. Low leakage power in the case of Sleepy Keeper approach

Type	Dynamic Power (nW)
Sleep approach	5.1
Leakage feedback approach	45
Sleepy Keeper approach	5.2

Table 4.2: Dynamic Power Dissipation in various modes. High power dissipation in Leakage feedback compared to Sleep and Sleep keeper.

be able to maintain proper logic state. Also sleepy keeper transistors (the NMOS connected to V_{DD} and the PMOS connected to GND) are emphatically not used to dynamically change the output voltage but instead only use them to maintain an already calculated output voltage. Intuitively,only a few clock cycles after entering sleep to a few clock cycles prior to exiting sleep. The sleepy keeper transistors acts as the sole connection to keep the output voltage unchanged.

4.3 Methodology and Observations

A 28T 3 bit adder was implemented and power leakage was studied in it with the sleep circuit approach, leakage feedback approach and sleepy keeper approach. Propagation delay, static power consumption and dynamic power consumption were measured. The results were compared and performance of the three approaches was analysed. Graphs are plotted. In this approach more number of circuits are used that take extra space in the layout. But this extra area effect minimizes as the complexity of circuits increases because in complex circuits having some extra space for two three transistors does not have much difference.The Static Power is reduced in Sleepy Keeper approach compared to other.

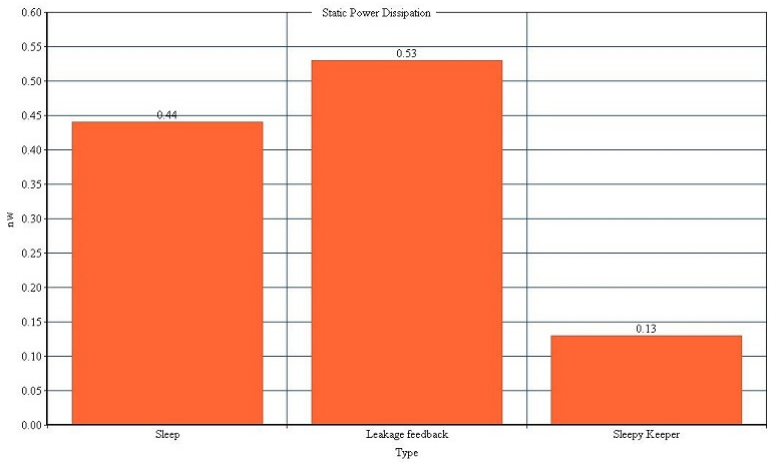

Figure 4.4: Static Power Dissipation-28TCMOS 1 Bit Adder

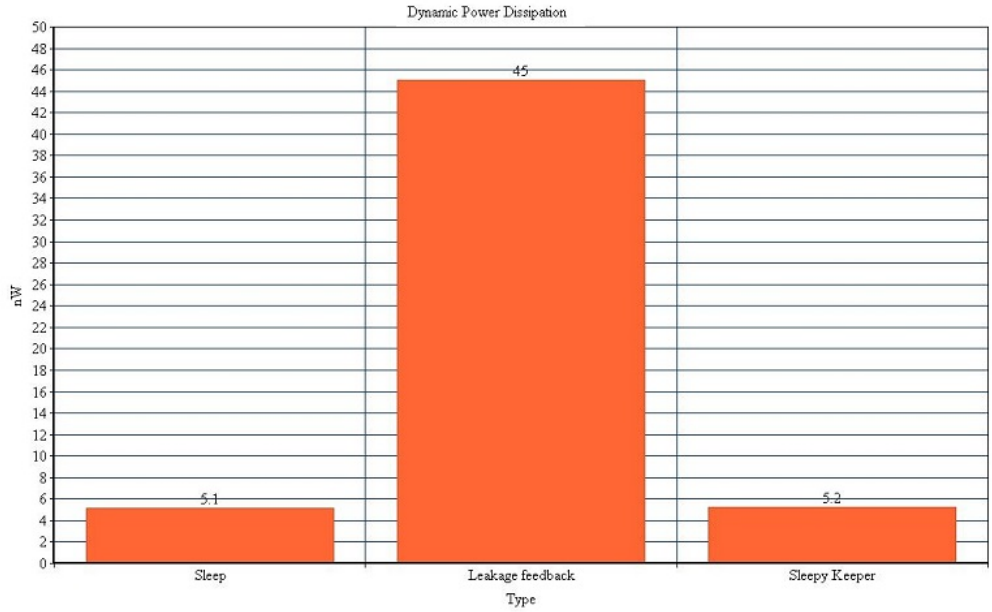

Figure 4.5: Dynamic Power Dissipation-28TCMOS 1 Bit Adder

4.4 Summary

The method of power gating has been demonstrated by this work. In this method the leakage power dissipation is low due to less access of the pull-up/pull-down networks to V_{DD} or ground.
The results of power gating are an increase in area and also a speed penalty. Therefore, the design of the switch requires a lot of pre-estimation with standard cell libraries which is a not a trivial task.
The next chapter illustrates the intricacies of sub-threshold design. This design is applicable for circuits that do not have a severe performance criterion, and are mostly concerned with low energy consumption. There are drawbacks to this method in terms of robustness to different logic styles, driving large loads, and high susceptibility to noise.

Chapter 5

Sub-Threshold Design

5.1 Introduction to Sub Threshold Design

In the personal computer design era VLSI circuits primarily focused on enhancing speed to execute complex instructions and support highly computational applications such as video, gaming, graphics etc. As a result complex signal processing applications and graphics processing units were integrated conventionally via an IC. These solutions though did not address the demand for portable operation as required by the advent of PDAs, mobile phones etc.
From here the power consumption became a prominent issue in design of smaller applications like watches, hand-held computers, PDAs, cell phones etc. All these applications require low power consumption more than a highly critical performance.
The need for low power design for non-critical performance is delivered by sub- threshold design of circuits. In these circuits the MOS transistor operates with a supply voltage less than the sub threshold voltage (denoted as V_{th}). This region of operation (known as sub-threshold region or sub-V_{th} operation) has driving currents as exponential functions of the applied gate voltages as compared to the square law dependence of driving current in linear or saturation regions. This current is similar to BJT driving current. They have strong variations with temperature and changes in bias as compared to super- V_{th} operations.
The total power consumption comprises of two terms, dynamic power and static power. Dynamic power depends on the square of supply voltage. Reducing supply voltage reduces the dynamic power. With shrinking technologies the static power is scaling close to the dynamic power due to increase in dominance of different leakage mechanisms. This is controlled by circuit techniques (source biasing, sleepy approach) as well as process techniques.
Some of the challenges in sub-V_th designs are designing an equal delay pull-up and pull-down network, finding a proper model to extract parameters from the sub-threshold currents. The biggest disadvantage of a sub-threshold circuit is the degradation in the output waveforms i.e. the are unsuitable for driving a high output load, or a next stage. Though sizing of gates is possible and gives an improvement in the performance yet unlike the conventional logical effort there is a parameter dependant sizing strategy through which wider gates are obtained. Sub-threshold circuits can be used for a low frequency of operation.

Applications of Sub-threshold circuits include

- Micro Sensor Networks: A micro sensor network refers to a signal processing circuit that has sensing,computation and communication facility. It does not require a very high performance and mostly they depend on the higher battery life, as it is not possible to replace the battery regularly. This is where low performance and low power sub-V_t design comes in picture

- RFID (Radio Frequency Identification): This application involves automatic identification of objects via RFID tags attached to them, that transmit and receive information wirelessly using radio frequencies. This is also an area of application of sub-threshold design.

5.2 Theory of Sub threshold MOS Design

5.2.1 Origin of weak inversion current

The weak inversion region was first studied on a metal insulator surface by Garett and Brattain [17]. In the weak inversion region, the majority carriers below the gate have been repelled leaving a depletion charge of fixed atom. The density of minority carriers is greater than bulk but not enough to affect the Capacitance vs Voltage charecteristics of MIS diode. They are mobile carriers and as soon as some voltage is applied across source and drain, a small diffusion current begins to flow.

5.2.2 Modelling of sub-threshold current

The sub-threshold current was modelled via numerous papers. In 1972, Barron [18] showed that the sub-threshold current depends exponentially on the surface potential. It was followed by works from [19],[20] and an exponential model for the sub-threshold current was chosen as

$$I_{sub-threshold} = I_0 e^{\left(\frac{V_{GS}-V_t}{nV_T}\right)} \tag{5.1}$$

With low V_{DS} roll off the model was re-fabricated as [19],[20],[21]

$$I_{sub-threshold} = I_0 e^{\frac{V_{GS}-V_t}{nV_T}} \left(1 - e^{\frac{-V_{DS}}{V_T}}\right) \tag{5.2}$$

where I_0 is

$$I_0 = \mu_0 C_{ox} \frac{W}{L} (\eta - 1) V_T^2 \tag{5.3}$$

Including DIBL the equation becomes

$$I_{sub-threshold} = I_0 e^{\frac{V_{GS}-V_t+\eta V_{DS}}{nV_T}} \left(1 - e^{\frac{-V_{DS}}{V_T}}\right) \tag{5.4}$$

where η is DIBL coefficient.

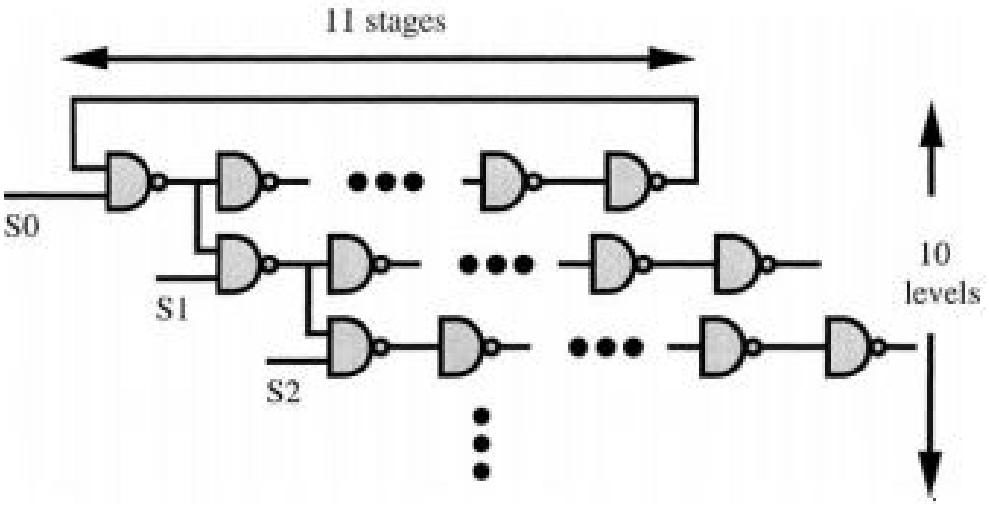

Figure 5.1: Variable Activity Factor Circuit,2002 IEEE

5.2.3 Minimum Energy Point

Low power design directly implies a low energy design. Energy is affected by many parameters but mainly power supply voltage and threshold voltage play a key role in determining total energy. A minimum energy point is found such that, when the circuit operates at this point the energy per operation is minimum as compared to any other point in the V_{DD}, V_t space.

Variable Activity Factor circuit

A simulation of variable activity factor circuit (Figure 5.1) is used to determine the optimal energy point.

A variable activity factor is gained by placing nine additional delay chains in parallel which are driven by the oscillator and run at the same frequency. The delay chains are enabled/disabled using selector inputs (S0-S9) to vary the activity factor.

The total energy is sum of dynamic and static energy consumption. The dynamic energy is given by

$$E_{dynamic} = \alpha C_{out} V_{DD}^2 \tag{5.5}$$

Propagation delay of a characteristic inverter in sub-threshold region is given as (from [23])

$$t_d = \frac{K C_{out} V_{DD}}{I_{0,g}} exp - \left(\frac{V_{DD} - V_{t,g}}{n V_T} \right). \tag{5.6}$$

The parameters $K, V_{t,g}, I_{0,g}$ are fitting parameters and they do not correspond to actual MOSFET parameters.
The operating frequency is given as

$$f = \frac{1}{t_d L_{DP}} \tag{5.7}$$

where L_{DP} is the depth of critical path. The total delay in the critical path is given as $T_D = \frac{1}{f}$.
The leakage energy is given as

$$E_{leak} = I_{leak} V_{DD} T_D = W_{eff} I_{0,g} V_{DD} t_d L_{DP} e^{\frac{-V_{t,g}}{nV_T}} = W_{eff} K C_{out} V_{DD}^2 t_d L_{DP} e^{\frac{-V_{DD}}{nV_T}} \quad (5.8)$$

The total energy is given as

$$\begin{aligned} E_{total} &= E_{dynamic} + E_{leak} \\ &= V_{DD}^2 \left(C_{eff} + W_{eff} K C_{out} L_{DP} e^{\frac{-V_{DD}}{nV_T}} \right) \end{aligned} \quad (5.9)$$

$$\frac{\partial E_{total}}{\partial V_{DD}} = 2 C_{eff} V_{DD} + \left(2 - \frac{V_{DD}}{nV_T} \right) W_{eff} K C_{out} L_{DP} V_{DD} e^{\frac{-V_{DD}}{nV_T}} \quad (5.10)$$

Setting $\frac{\partial E_{total}}{\partial V_{DD}}$ equal to zero,

$$(2 - \frac{V_{DD}}{nV_T}) e^{\frac{-V_{DD}}{nV_T}} = \frac{-2 C_{eff} e^2}{W_{eff} K C_{out} L_{DP}} \quad (5.11)$$

From this the analytical solution for the optimum supply voltage is given as

$$V_{DD_{opt}} = nV_T \left(2 - lambertW \left(\frac{-2 C_{eff} e^2}{W_{eff} K C_{out} L_{DP}} \right) \right) \quad (5.12)$$

and the optimum threshold voltage is given as

$$V_{T_{opt}} = V_{DD_{opt}} - nV_T ln \left(\frac{f K C_{out} L_{DP} V_{DD_{opt}}}{I_{0,g}} \right) \quad (5.13)$$

Lambert Function

The lambertW function appearing in the expressions above is inverse of the function $f(x) = xe^x$.
In other words the general form of lambertW function is the solution to the equations as

$x = W(x)e^{W(x)}$.
The domain of the Lambert W function is $[\frac{1}{e}, \infty)$ and the range is $(-\infty, \infty)$. However, when x is in the interval (-1/e, 0), the function returns two values of W(x), so the complete Lambert function is not a true function in the strictest sense.

5.3 Design of an inverter in sub-threshold region

An inverter is the simplest CMOS circuit that can be realized. Its performance is used as a scale to measure the performance of other complex gates. One of the biggest problem in designing an inverter lies in the sizing of pull up and pull down networks for the operation . Unlike the conventional CMOS design a simple relation like $\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p}$ cannot be used to determine the sizes of the respective widths as the current equation is not a square-law. Using Symica IDE and channel length of 130 nm, the simulation results agree for a $\frac{W_p}{W_n} = 6.54$. Smaller width of devices produce poor output waveforms as can be ascertained by the smaller time spent in the constant V_{DD} or ground (denoted as t_{const}).

$V_{DD}(mV)$	$\tau_{const}(ps)$	$\tau_{rise}(ns)$	$\tau_{fall}(ns)$	$\tau_{delay}(ns)$	$P_{tot}(nW)$
320	9	2.5	2.88	4.73	53
340	110	2.3	2.48	3	78
360	500	2.18	2.32	1.92	113
380	2000	1.43	1.45	1.26	153
400	3000	0.94	0.97	0.8	207

Table 5.1: Inverter charecteristic with $\frac{W_p}{W_n} = 6.54, W_n = 550nm, V_{T0} = 432mV$

$W_n(nm)$	$\tau_{const}(ps)$	$\tau_{rise}(ns)$	$\tau_{fall}(ns)$	$\tau_{delay}(ns)$	$P_{tot}(nW)$
520	1980	1.45	1.48	1.27	145
260	1140	1.9	2	3.45	78
130	37	2.95	3.04	9	43

Table 5.2: Performance of inverter with $\frac{W_p}{W_n} = 6.54$,$V_{DD} = 0.38$ V

5.3.1 Evaluating the model of sub-threshold design

For designing the CMOS inverter in sub-threshold region we choose the $C_{load} = 9C_{in}$.
Our $C_{in} = C_{ox}WL$ so $C_{load} = 9C_{ox}WL$. This value is calculated for $L = 130nm$ and $t_{ox} = 3.3nm$, and so $C_{load} = 0.2pF$. C_{load} is chosen as $1pF$.
The nominal threshold voltage of the transistor is found to be $V_{th0} = 0.432V$, and the leakage current is observed to be $I_{leak} = 212pA$. Then using an assumption that $I_{leak} = I_{0,g}e^{\frac{-V_{th0}}{V_T}}$ we estimate $I_{0,g} = 3.76 \times 10^{-3}A$
From equation 5.8 we evaluate K as K=$\frac{\tau_d I_{0,g}}{C_{load}V_{DD}} = 8 \times 10^4 units$.
$C_{eff} = C_{in}$ and $W_{eff} = W_p + W_n$.
From all these values we calculate $\beta = \frac{-2C_{eff}e^2}{W_{eff}KC_{load}L_{DP}}$.
Now using this we calculate $lambertw(\beta) = -7.4 and -0.0045$. Using equations, 5.11 and 5.12 we get $V_{DD_{opt}} = 300mV$ and $V_{t_{opt}} = 422mV$. But to improve the τ_{const} we choose $V_{DD_{opt}} = 380mV$ and the performances are tabulated.

Tables 5.1 and 5.2 denote the performance of a inverter operating in sub-threshold region. The parameter τ_{const} denotes the time spent by the output waveform in constant V_{DD} or ground. A smaller time indicates a poor shaped waveform, unsuitable for driving large loads.Frequency of operation was chosen as $10kHz$.

5.3.2 Matching the delay in pull-up and pull down networks

The sizing of the MOSFET in sub-V_t region is more important than in super-V_t region as sub-V_t design is not strictly ratio-less as the super-V_t design is.
As can be seen from equations, 5.3 and 5.4 (if $V_{GS} = V_{DD}$, and $V_{DS} = V_{DD}$)

$$I_{sub-threshold} = I_0 e^{\frac{V_{DD} - V_t + \eta V_{DD}}{nV_T}} \left(1 - e^{\frac{-V_{DD}}{V_T}}\right) \tag{5.14}$$

$$\frac{\partial I_{sub-threshold}}{\partial V_{DD}} = \mu C_{ox}\frac{W}{L}(n-1)V_T^2\left[e^{\frac{V_{DD}(1+\eta)-V_t}{V_T}}\left(\frac{1+\eta}{V_T}\right)\left(1-e^{\frac{-V_{DD}}{V_T}}\right)-e^{\frac{V_{DD}(1+\eta)-V_t}{V_T}}\left(\frac{e^{\frac{-V_{DD}}{V_T}}}{V_T}\right)\right] \tag{5.15}$$

$$= \mu C_{ox}\frac{W}{L}(n-1)V_T^2 f(V_{DD}) \tag{5.16}$$

So to equate the corresponding resistances of NMOS and PMOS (for a equal pull-up and pull-down network)

$$\mu_p C_{ox}\frac{W_p}{L}(n-1)V_T^2 f_p(V_{DD}) = \mu_n C_{ox}\frac{W_n}{L}(n-1)V_T^2 f_n(V_{DD}) \tag{5.17}$$

$$\Rightarrow \frac{W_p}{W_n} = \left(\frac{\mu_n f_n(V_{DD})}{\mu_p f_p(V_{DD})}\right)$$

Thus the ratio of widths of PMOS and NMOS depends on the supply voltage and the matching of parameters in the both MOSFETS. So, this is one of the limitations of the sub-V_t design.

5.4 Design of a Full Adder in sub-threshold region

Design of full adder involves designing the sum section and the carry section. One of the biggest disadvantages of a sub-threshold design is that it cannot be used to drive a chain of stages or larger loads. So as a result the circuits need to attain their functionalities in least number of stages. CMOS conventional static logic style was used initially and the half adder using this was simulated. It gave convincing results but a full adder could not be designed properly using the sub-threshold design for static CMOS because it had too many stages to drive.

Instead, we choose a Pass transistor logic and use it to design a full adder and simulate to obtain the results. This circuit is far more convincing in terms of output waveform quality, which can be further improved using a level restorer or a threshold detection circuit. Nevertheless, the pass transistor logic has disadvantages that it requires input in both original and complimentary form thus an overhead.

5.4.1 Evaluating sub-threshold model for sum section of full adder

In this case we select a frequency of operation as 10kHz. Proceeding as the design we extract parameter values as follows

- $I_{leak} = 668pA$
- $I_{0,g} = 2.34 \times 10^{-4}A$
- $\tau_d = 9.73ns$
- K=18070
- $W_{eff} = 18W = 320 \times 10^{-4}cm$
- $C_{eff} = 48C_{ox}WL = 1.848 \times 10^{-16}F$
- $C_{load} = 18C_{ox}WL = 7 \times 10^{-17}F$

	Static CMOS SUM section	Pass Transistor SUM section
Power (μW)	3.53	1.16
Delay (ns)	2.2	0.4
$t_r(ns)$	0.9	1.5139 (best case)
$t_f(ns)$	1.875	4.6852 (best case)
$t_{const}(ps)$	4500	1197
threshold (mV)	0	130
Noise Margin(mV)	86-190 mV	NA
Voltage swing (mV)	380	237
Output rms value(V)	0.27	0.29
$V_{out_{max}}$ (mV)	387	500
$V_{out_{min}}$(mV)	0	0
MOSFET count	20	8

Table 5.3: Comparison of SUM section in sub-threshold design, $SUM = A \oplus B \oplus C$,$V_{DD} = 0.38V, V_{th} = 0.42V$

	Static CMOS CARRY section	Pass Transistor CARRY section
Power (μW)	4.62	0.06
Delay (ps)	350	40
$t_r(ns)$	1	5 (best case)
$t_f(ns)$	0.6	5.156 (best case)
$t_{const}(ps)$	4539	947
threshold (mV)	0	65
Noise Margin(mV)	190 mV	NA
Voltage swing (mV)	380	315
Output rms value(V)	0.28	0.23
$V_{out_{max}}$ (mV)	400	490
$V_{out_{min}}$(mV)	-100	-33
MOSFET count	18	8

Table 5.4: Comparison of Carry section in sub-threshold design, $Carry = AB + BC + AC$,$V_{DD} = 0.38V, V_{th} = 0.42V$

- $V_{DD} = 1.8V$
- $\beta = 0.28642$
- $lambertw(\beta) = -1.896$
- $V_{DD_{opt}} = 316mV$
- $V_{th_{opt}} = 426mV$

Using these value we first design a static CMOS half adder and tabulate its performance in 5.3. After that we design a Pass Transistor logic full adder and tabulate its performance in 5.4.

5.5 Observations

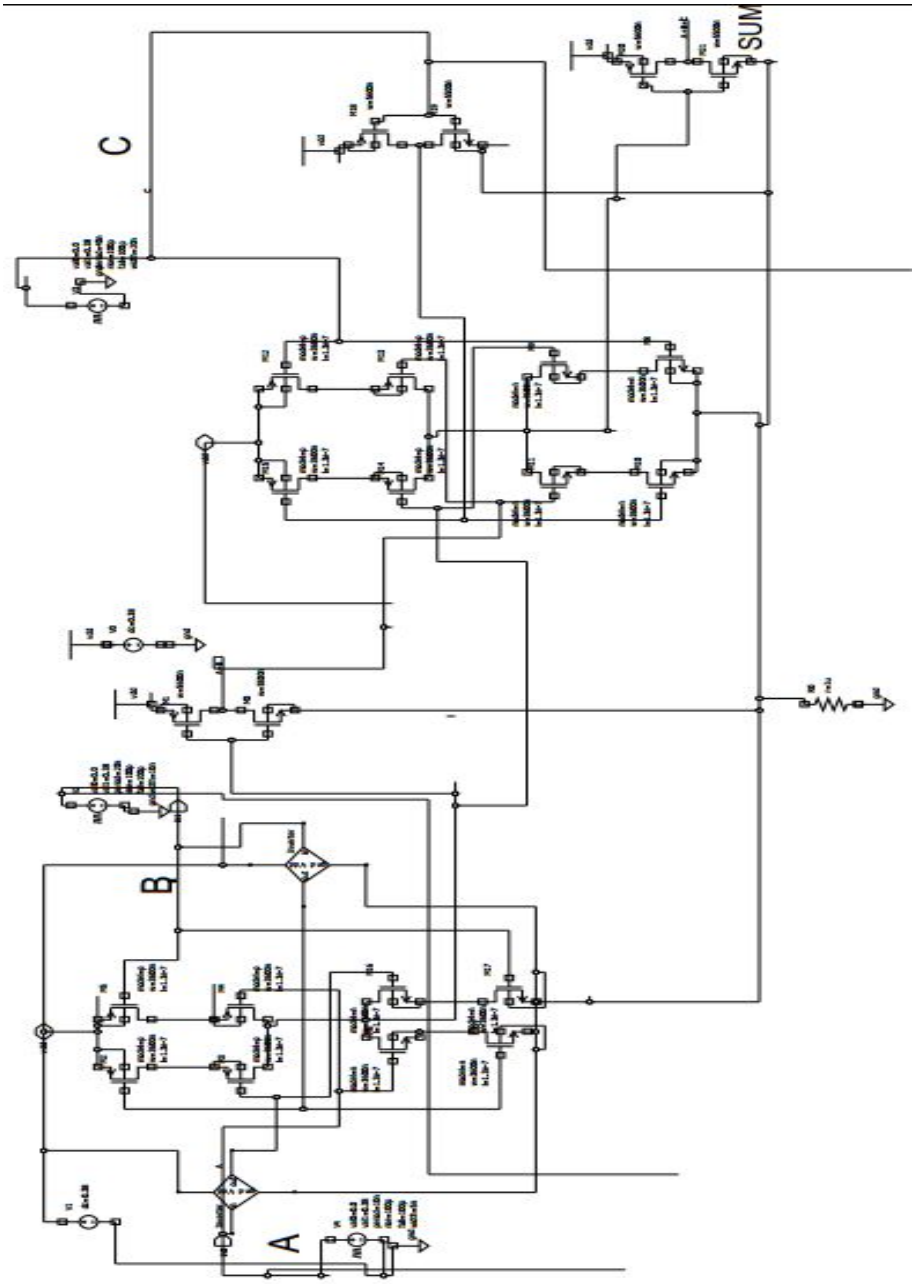

Figure 5.2: SUM section of a full adder using Static CMOS logic

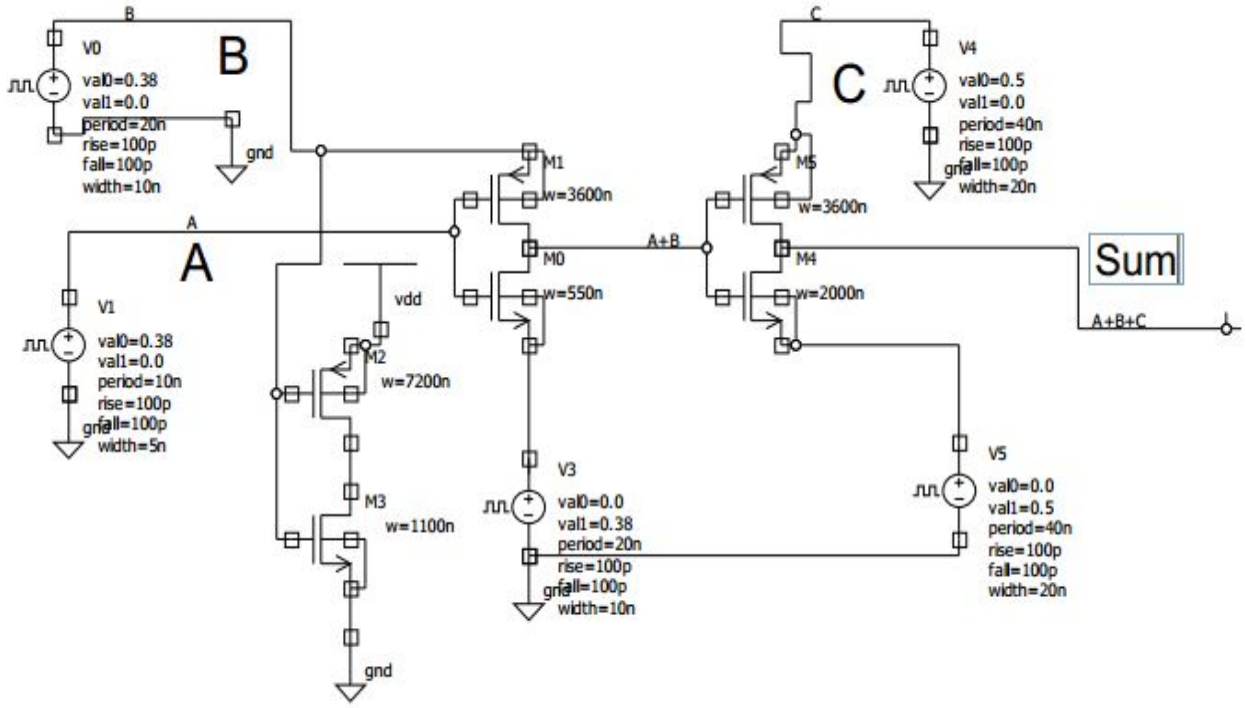

Figure 5.3: SUM section of a full adder using Pass Transistor logic

Some comments about the sum and carry sections designed by static CMOS and Pass Transistor Logic :

- Figure 5.6 shows the output of the sum section of a full adder with static CMOS design. It is very much similar to the super-V_{th} design. When all the inputs are zero, the output of adder is 130 mV. The all zero case is considered to be a trivial input and the circuit is designed to provide faithful output to all other input conditions, without compromising on any other input combination.

- Figure 5.7 shows the output of the sum section using Pass Transistor Logic. It suffers from poor noise margin so it is NA in the Table 5.3. Also the effect of feedback capacitance from Drain to Gate, is more prominent as the voltage spikes up.

- Figure 5.8 and 5.9 show the output of carry section for static and pass transistor logic. The implementation of Pass Transistor Logic requires less number of transistors but suffers heavily from poor noise margin as compared to that of the static CMOS.

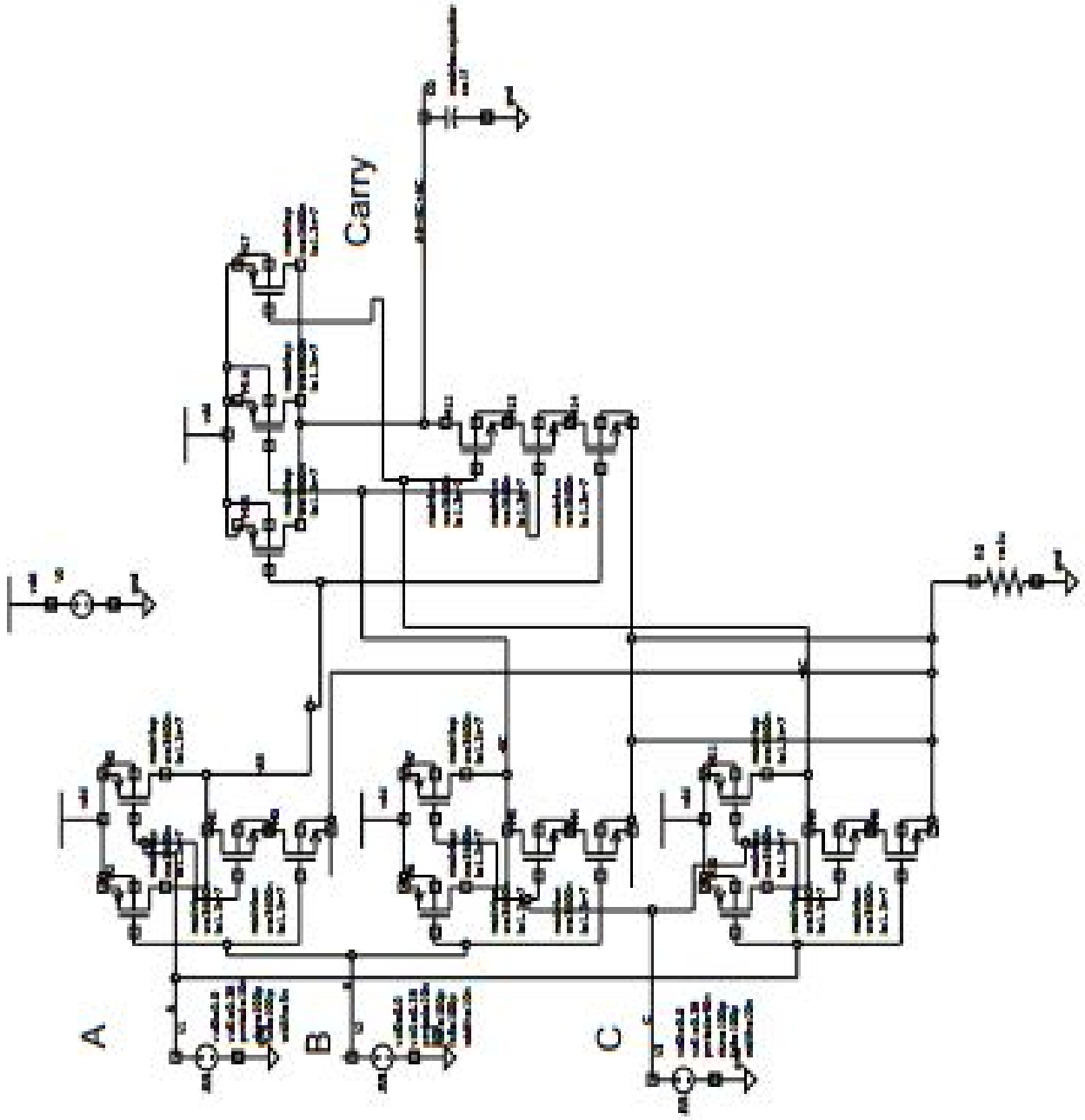

Figure 5.4: CARRY section of a full adder using Static CMOS logic

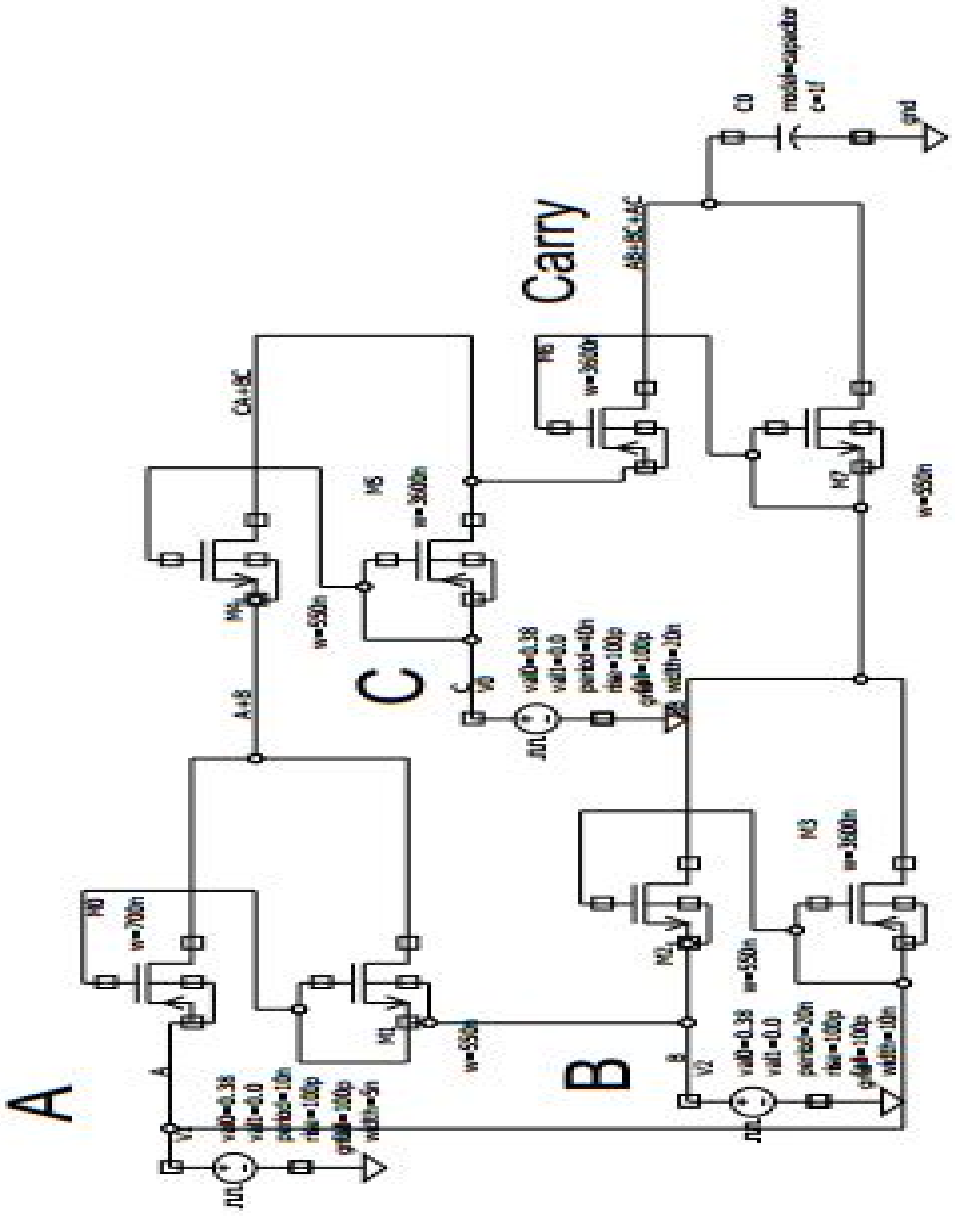

Figure 5.5: CARRY section of a full adder using Pass Transistor logic

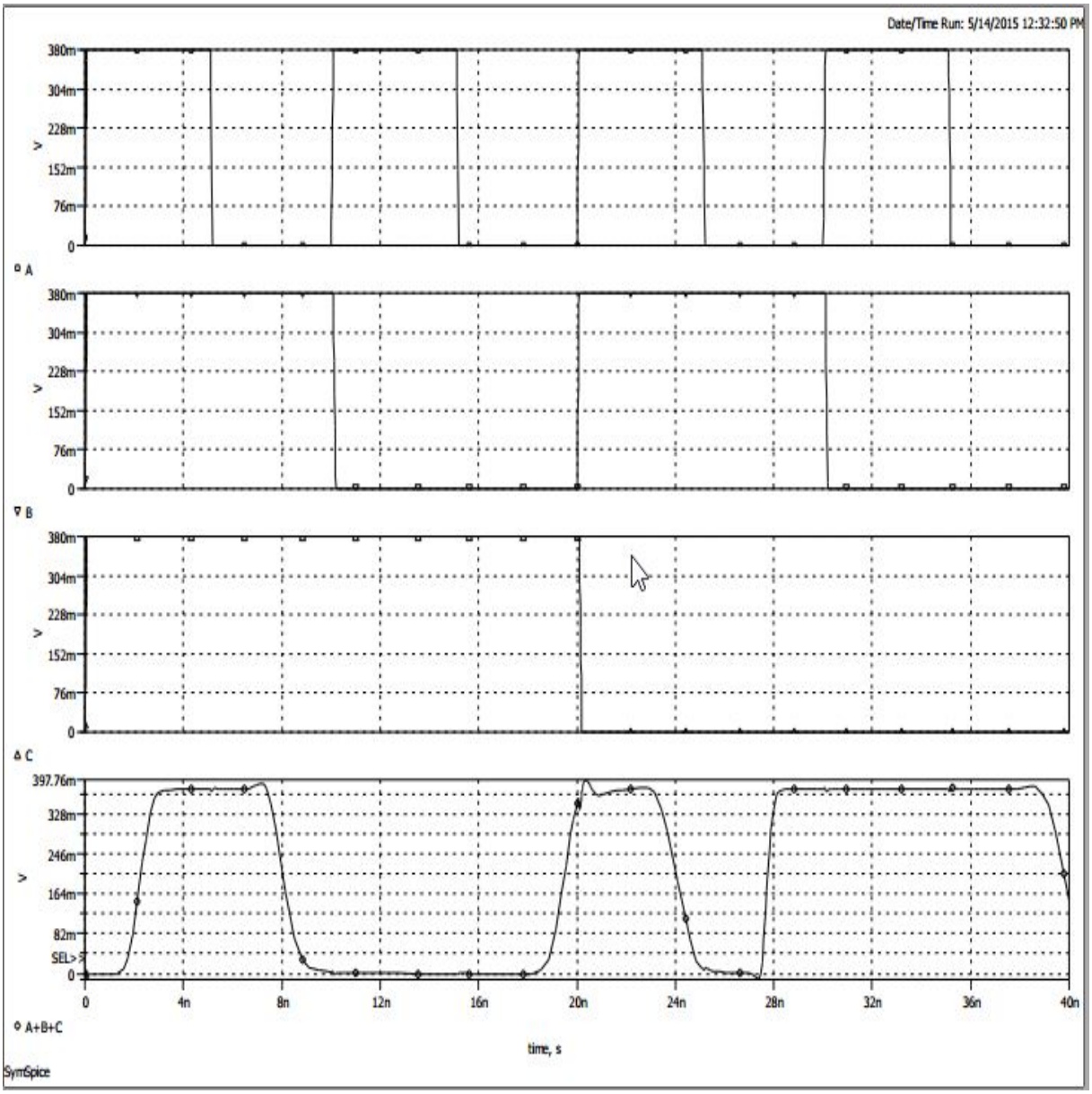

Figure 5.6: Output of SUM section of a full adder using Static CMOS logic

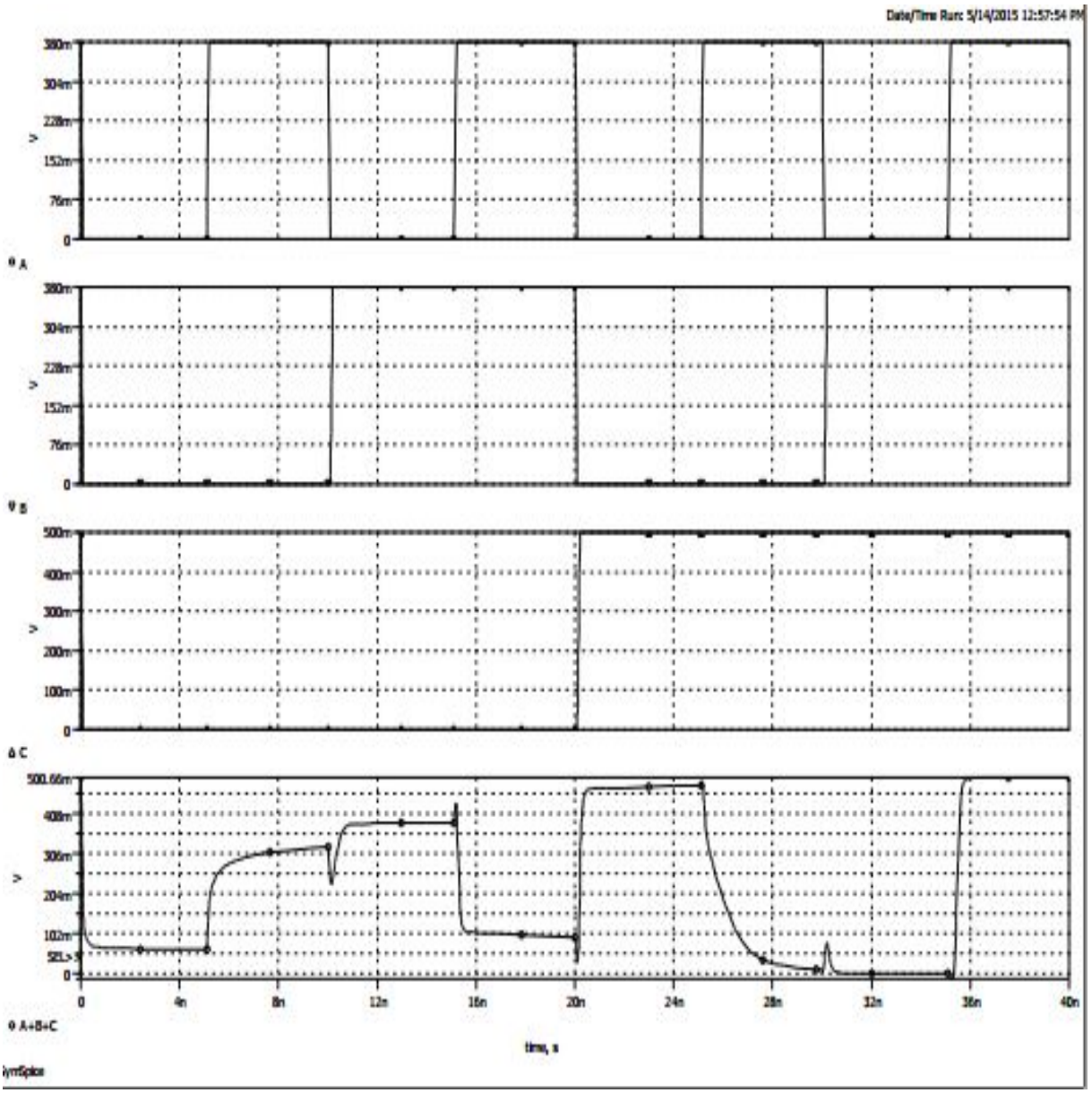

Figure 5.7: Output of SUM section of a full adder using Pass Transistor logic

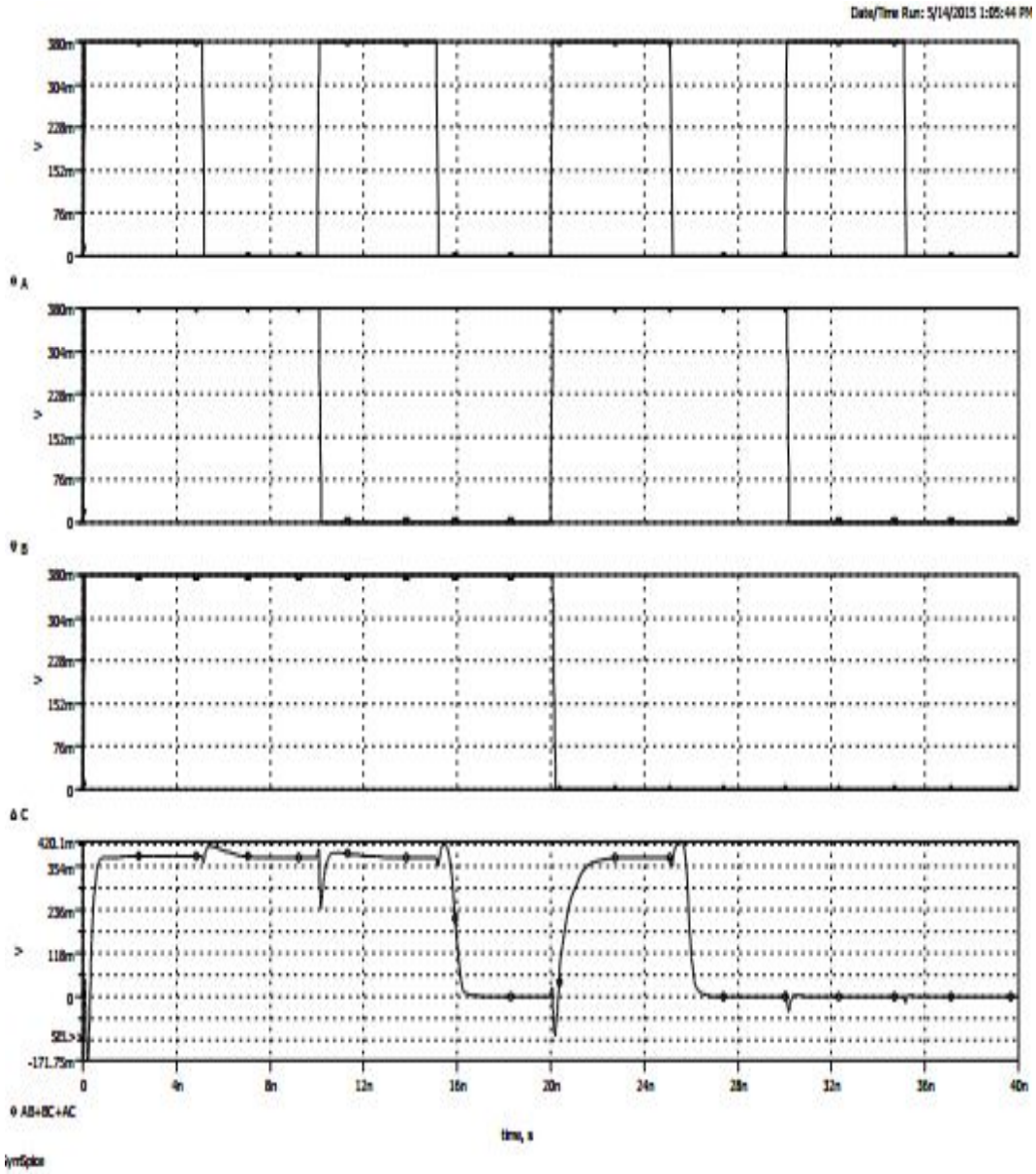

Figure 5.8: Output of Carry section of a full adder using Static CMOS logic

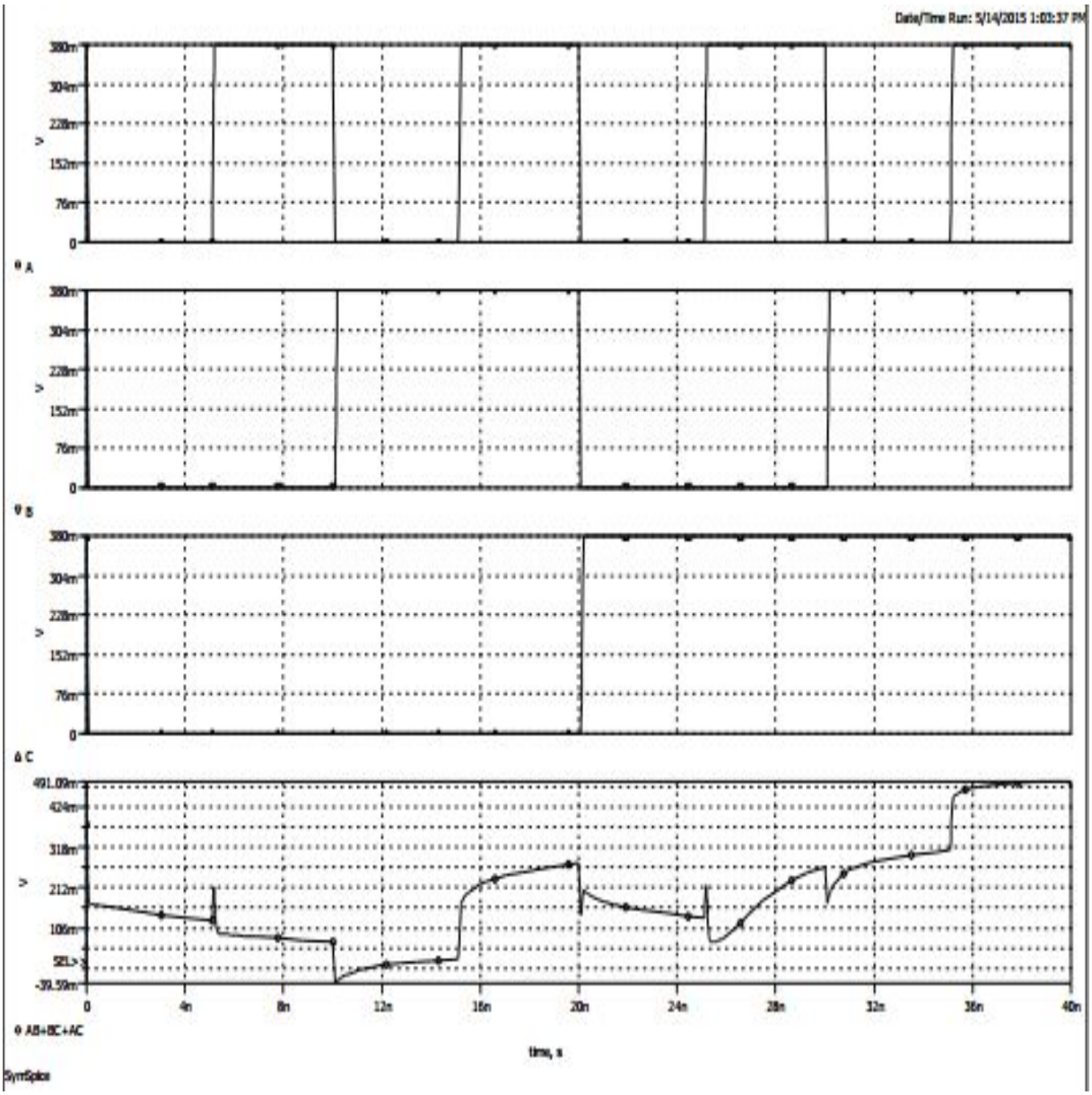

Figure 5.9: Output of Carry section of a full adder using Pass Transistor logic

5.5.1 Summary:

The method of Sub-threshold design is a trade-off between the high performance and low power consumption. Though it has some advantages yet its subtle limitations inhibit its large scale usage. The major advantage of the sub-threshold design are as follows:

- This leakage power is considerably reduced by in this case, as the ON state currents are a few order different from the leakage power.
- the calculation of $V_{DD_{opt}}$ involves the use of Lambert function. A change of order 1000 in the input results in a change of order 10 in the output. This formulates that sub-threshold design can be used for a wide variety of output load. The limitation to this robustness comes from the trouble of estimating fitting parameters accurately, for different load capacitances.
- The dependence of C_{eff} on $V_{DD_{opt}}$ (which is less by 20-30 % to conventional C_{ox}) makes it less dependable on circuit parasitics.

This method has several limitations that make it unsuitable for many applications. Some of its limitations are listed as follows :

- The exponential dependence of sub-threshold current on gate voltage makes it difficult to design equal pull-up and pull-down MOS networks. Several formulations have been proposed in [25] and [26] yet the sub-V_{th} is not characterized for equal pull-up and pull-down.
- The variation in output is very susceptible to temperature as compared to super-V_{th} design.
- The value of fitting parameters such as V_{th0}, I_0 and K are estimated on the basis of leakage current or delay of a circuit. So it is a tedious, iterative process to estimate the actual values. A lot of standard cell characterization and estimation is required to accurately tabulate different values of these fitting parameters.
- The design of load capacitance is also an iterative process, the sub-threshold circuits are very poor at delivering current to large loads, unless the widths are increased. This increases the dynamic power consumption but leakage power is still low.
- An exact design needs an iteration in terms of fitting parameters, $V_{DD_{opt}}, V_{th_{opt}}$, so it is unsuitable for one-step designs.

As a conclusive remark, the sub-threshold design is an iterative process, the results obtained are indicative but not exact.

Chapter 6

Conclusions

This work aimed at establishing a design and verifying the validity of the design in sub-threshold region. The notion of power and energy, and the subtle difference between them has led to the idea of low performance design such as sub-threshold design. This is motivated by the low energy design (ie that finds an operating point to minimize energy) using a variable activity circuit. (Figure 4.1).
The delay analysis and improvement in delay by sizing the transistors is demonstrated in Chapter 2. Logical effort has been used to size transistors to optimise the delay for a sum section of an adder.
Power gating is also an important technique to effectively reduce power by shutting down a part of a circuit which is not operating. This idea reduces the leakage power and those results have been mentioned as Figure 3.4 and Figure 3.5.
Finally sub-threshold design has been dealt in the last chapter. It shows the different parameters involved with the sub-threshold current, model of the sub-threshold design and the performance(Figure 4.6, Figure 4.7, Figure 4.8 and Figure 4.9). The advantages and limitations of the sub-threshold design have been also mentioned.
Low power design is a balance between circuit techniques and process techniques. It depends on the application as well as the process technology available. Nevertheless, sub-threshold design is not suitable for driving large loads for long time. The performance can be improved by applying logical effort, power gating and minimum energy model design. The entire process in iterative, and the results are indicative but not exact.

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