24RE TRIBHUVAN UNIVERSITY INSTITUTE OF ENGINEERING

Examination Control Division 2070 Chaitra

Exam,		Regular	
Level	BE	Full Marks	80
Programme	BEL,BEX,BCT	Pass Marks	32
Year / Part	11/1	Time	3 hrs.

Subject: - Digital Logic (EX502)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ Attempt <u>All</u> questions.
- ✓ The figures in the margin indicate Full Marks.
- ✓ Assume suitable data if necessary.

•	Assume suitable data if necessary.	
1.	Define digital signal and explain Gray code with example.	[1+5]
2.	Prove that positive X-OR is equivalent to negative X-NOR.	[5]
3.	a) Convert the following term into standard min term. A: B'C.	[3]
	b) Use K-map method to implement the following function and also draw the reduced circuit using NOR gate.	[5]
	$F(A, B, C, D) = \Sigma_{m}(0, 2, 4, 6, 8, 10, 15)$ and	
	$d = \Sigma_m (3, 11, 14)$	
4.	a) Realize the logic circuit of the following using 8:1 MUX.	[4]
	$F(W, X, Y, Z) = \Sigma_m (1, 2, 5, 7, 8, 10, 12, 13, 15)$	
	b) When FF _H is ANDed with CO _H what will be the resulting number? Subtract (26) 10 from (16) 10 using 2's complement binary method.	[2+2]
5.	a) Differentiate between level and Edge triggering?	[3]
	b) Explain the operation of two bit magnitude comparator with truth table and circuit diagram.	[5]
6.	a) Describe different typerof registers with diagram.	[8]
	b) Illustrate how 1011 data can be stored and retrieve in parallel in serial out shift register with neat timing diagram and truth table.	[8]
7.	Differentiate synchronous and asynchronous sequential circuits. Explain the operation of mod-12 synchronous counter with timing diagram.	[2+6]
8.	a) Define state diagram and state table with example.	[2]
	b) Design a sequential machine that has one serial input and one output z . The machine is required to give an output $z=1$ when the input X contains the message 110.	[8]
9.	Draw the schematic diagram of TTL two input NOR Gate.	[6]
10.	Explain briefly the block diagram of an instrument to measure frequency.	[5]
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Exam.		Regular	
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Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic (EX502)

- Candidates are required to give their answers in their own words as far as practicable.
- ✓ Attempt <u>All</u> questions.
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1.	Define digital IC signal levels. What is Gray Code? Explain with example.	[3+3]
2,	Construct the given Boolean function: $F = (A+B) (C+D) E$ using NOR gates only.	[4]
	Simplify F (A,B,C,D) = π (0,2,5,8,10) + d(7,15). Write its standard SOP and implement the simplified circuit using NOR gates only.	[4+4]
4.	a) What is priority Encoder? Design octal to binary priority encoder.	[2+4]
	b) Design a 2 bit magnitude comparator.	[4]
5.	Design a combinational logic that performs multiplication between two 4 bit numbers using binary parallel adder and other gates.	[8]
6.	Draw the circuit diagram and explain the operation of positive edge triggered JK flip-flop, What are the drawbacks of JK flip-flop?	[7+1]
7.	Explain the Serial in Serial out (SISO) shift register with timing diagram.	[4]
8.	Design the synchronous decade counter and also show the timing diagram.	[8]
9.	Design a sequential machine that detects three consecutive zeros from an input data stream X by making output, $Y \equiv 1$.	[12]
10.	Draw the schematic circuit for CMOS NAND gates. What do you mean by totem-pole output?	[4+4]
11.	Describe the operation of a frequency counter.	[4]

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Exam.		Regular	
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Year / Part	П/1	Time	3 hrs.

[2+6]

[4]

Subject: - Digital Logic (EX 502)

 Candidates are required to give their answers in their own words as far as practicable. Attempt All questions. ✓ The figures in the margin indicate Full Marks. ✓ Assume suitable data if necessary. 1. List out the name of universal gates and why they are called universal gate? Relise Ex- OR Gate using only NAND gates. [2+2]Explain Excess 3 code with suitable examples. [6] 3. Simplify the function using K-map $F = \sum (0.1.4.8, 10.11.12)$ and $D = \sum (2.3.6.9, 15)$. Also convert the result into standard minterm. [3+5] Design a 32 to 1 multiplexer using 16 to 1 and 2 to 1 multiplexers. [5] Design a 3-bit even parity generator and 4-bit even parity checker circuit. [5] Draw the block diagram of n-bit full adder and explain its operation. [8] 7. Write down the drawbacks of SR flip flop. Explain the operation of data flip flop with timing diagram and truth table. [1+7] 8. With clear circuit and timing diagram, explain the operation of Serial in - Serial out shift register. [4] Define ripple counter. Explain the operation of mode-10 ripple counter with timing diagram. [1+7]10. Design a sequential machine that has one serial input and one output z. The machine is required to give an output z = 1 when the input x contains the message 1010. [12]

11. Describe the voltage profile of TTL. Explain the operation of TTL to CMOS interface.

12. What is frequency counter? Explain with block diagram.

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12. Design a two bit magnitude comparator.

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[6]

[6]

	Subject: - Digital Logic	
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1.		1+2]
2.	Why NAND and NOR gates are called Universal gates? Illustrate with examples.	[4]
3.	What do you mean by HDL? Design a 2 to 4 line decoder circuit using HDL.	2+3]
4.	Simplify $\pi(0, 4, 5, 8, 9, 11, 15)$ using K-Map and write its standard SOP expression.	4+2]
5.		2÷2]
6.	Draw the schematic diagram of TTL NOR gate, Discuss the characteristics of TTL 74XX series gates.	[6]
7.	Draw the circuit diagram of edge triggred JK flip flop and explain it.	[5]
8.	and the state of t	2:16]
9.	What is a counter? Design a MOD - 6 synchronous counter. Draw its timing diagram.	
10	Design a synchronous state machine with the following specification:	[12]
	 a) No. of input: 1 b) No. of output: 1 c) The output of the machine is to be set high when the data in the input is 110 in sequence, starting from the MSB (Use SR flip - flop). 	

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11. With an example, state and explain the problems associated in the design of asynchronous sequential circuit.

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Exam.	Regular/Back		
Level ·	BE	Full Marks	80
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Year / Part	1[/]	Time	3 hrs.

Subject: - Logic Circuits

- Candidates are required to give their answers in their own words as far as practicable.
- ✓ Attempt All questions.
- ✓ The figures in the margin indicate Full Marks.
- ✓ Assume suitable data if necessary.
- 1. Convert the following numbers from the given base to the bases indicated:

 $[1\times6]$

- a) Octal 623.77 to detamal, binary and hexadecimal
- b) Hexadecimal 2AC5 D to decimal, octal and binary
- Perform the subtraction with the following decimal and binary numbers using 9's and 1's
 complement respectively. [2+2]
 - a) 3570-2100 (Using 9's complement)
 - b) 10010-10011 (Using 1's complement)
- 3. Prove the following Boolean expression:

[4+4+2]

$$AB + A\overline{B}C + \overline{A}BC = AB + AC + BC$$

And simplify $\Sigma 1, 2, 3, 8, 9, 10, 11, 14$) and d(0,4,12) by using K-map and write its standard product of sum (POS) expression.

[8]

5. State De-Morgan streeter. Why NAND and NOR gates are called an universal logic gates.

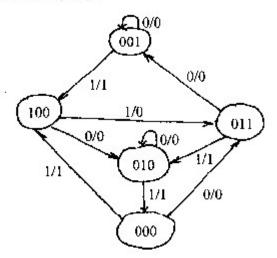
[3+6]

6. Explain about Jik-flip-flop along with their truth table and characteristic equation.

[6]

- 7. Design a mod-10 synchronous counter showing its state circuit diagram and output waveforms.
- [6]
- 8. Describe briefly the operation of a 4-bit serial in-parallel out register with a clear circuit diagram.
- [5]
- A sequential circuit has one input and one output. The state diagram is shown in figure. Design
 the sequential circuit with RS-flip-flops.

[10]



- 10. Explain with wave diagram how can you display a letter E in a CRT under 5×7 matrix format.
- 11. Write short notes on: (any two)

[6] [5×2]

- a) Multiplexing and demultiplexing.
- c) Fan-in and fan-out, propagation delay
- b) Gray code
- d) Parity generator
