DIGITAL LOGIC | SYLLABUS | IOE | 2066

DIGITAL LOGIC

EX 502

Lecture : 3
Year : II
Tutorial : 0
Part : I
Practical : 3

Course Objective:

To introduce basic principles of digital logic design, its implementation and applications.

1. Introduction (3 hours)

1.1. Definitions for Digital Signals
1.2. Digital Waveforms
1.3. Digital Logic
1.4. Moving and Storing Digital Information
1.5. Digital Operations
1.6. Digital Computer
1.7. Digital Integrated Circuits
1.8. Digital IC Signal Levels
1.9. Clock wave form
1.10. Coding
1.10.1. ASCII Code
1.10.2. BCD
1.10.3. The Excess – 3 Code
1.10.4. The Gray Code

2. Digital Logic (1 hours)

2.1. The Basic Gates – NOT, OR, AND
2.2. Universal Logic Gates – NOR, NAND
2.3. AND-OR-INVERT Gates
2.4. Positive and Negative Logic
2.5. Introduction to HDL

3. Combinational Logic Circuits (5 hours)

3.1. Boolean Laws and Theorems
3.2. Sum-of-Products Method
3.3. Truth Table to Karnaugh Map
3.4. Pairs, Quads, and Octets
3.5. Karnaugh Simplifications
3.6. Don't Care Conditions
3.7. Product-of-Sums Method
3.8. Product-of-Sums Simplification
3.9. Hazards and Hazard Covers
3.10. HDL Implementation Models

4. Data Processing Circuits (5 hours)

4.1. Multiplexetures
4.2. Demultiplexetures
4.3. Decoder
4.4. BCD-to-Decimal Decoders
4.5. Seven-Segment Decoders
4.6. Encoder
4.7. Exclusive-OR Gates
4.8. Parity Generators and Checkers
4.9. Magnitude Comparator
4.10. Read-Only Memory
4.11. Programmable Array Logic

4.12. Programmable Logic Arrays
4.13. Troubleshooting with a Logic Probe
4.14. HDL Implementation of Data Processing Circuits

5. Arithmetic Circuits (5 hours)

5.1. Binary Addition
5.2. Binary Subtraction
5.3. Unsigned Binary Numbers
5.4. Sign-Magnitude Numbers
5.5. 2's Complement Representation
5.6. 2's Complement Arithmetic
5.7. Arithmetic Building Blocks
5.8. The Adder-Subtracter
5.9. Fast Adder
5.10. Arithmetic Logic Unit
5.11. Binary Multiplication and Division
5.12. Arithmetic Circuits Using HDL

6. Flip Flops (5 hours)

6.1. RS Flip-Flops
6.2. Gated Flip-Flops
6.3. Edge-Triggered RS Flip-Flops
6.4. Egde Triggered D Flip-Flops
6.5. Egde Triggered J K Flip-Flops
6.6. Flip-Flop Timing
6.7. J K Mater- Slave Flip-Flops
6.8. Switch Contacts Bounds Circuits
6.9. Varius Representation of Flip-Flops
6.10. Analysis of Sequencial Circuits

7. Registers (2 hours)

7.1. Types of Registers
7.2. Serial In – Serial Out
7.3. Serial In – Parallel Out
7.4. Parallel In – Serial Out
7.5. Parallel In – Parallel Out
7.6. Applications of Shift Registers

8. Counters (5 hours)

8.1. Asynchronous Counters
8.2. Decoding Gates
8.3. Synchronous Counters
8.4. Changing the Counter Modulus
8.5. Decade Counters
8.6. Presettable Counters
8.7. Counter Design as a Synthesis Problem
8.8. A Digital Clock

9. Sequential Machines (8 hours)

9.1. Synchronous machines
9.1.1. Clock driven models and state diagrams
9.1.2. Transition tables, Redundant states
9.1.3. Binary assignment
9.1.4. Use of flip-flops in realizing the models
9.2. Asynchronous machines
9.2.1. Hazards in asynchronous system and use of redundant branch
9.2.2. Allowable transitions
9.2.3. Flow tables and merger diagrams
9.2.4. Excitation maps and realization of the models

10. Digital Integrate Circuits (4 hours)

10.1. Switching Circuits

10.2. 7400 TTL
10.3. TTL parameters
10.4. TTL Overvew
10.5. Open Collecter Gates
10.6. Three-state TTL Devices
10.7. External Drive for TTL Lods
10.8. TTL Driving External Loads
10.9. 74C00 CMOS
10.10. CMOS Characteristics
10.11. TTL- to –CMOS Interface
10.12. CMOS- to- TTL Interface

11. Applications (2 hours)

11.1. Multiplexing Displays
11.2. Frequency Counters
11.3. Time Measurement

Practical:

1. DeMorgan's law and it's familiarization with NAND and NOR gates
2. Encoder, Decoder, and Multiplexer
3. Familiarization with Binary Addition and Subtraction
4. Construction of true complement generator
5. Latches, RS, Master-Slave and T type flip flops
6. D and JK type flip flops
7. Ripple Counter, Synchronous counter
8. Familiarization with computer package for logic circuit design
9. Design digital circuits using hardware and software tools
10. Use of PLAs and PLDs

References:

1. Donald P. Leach, Albert Paul Malvino and Goutam Saha, " Digital Principles and

Applications", 6th edition , Tata McGraw-Hill, 2006
2. David J Comer "Digital Logic And State Machine Design" 3rd edition, Oxfored University Press, 2002
3. William I. Fletcher "An Engineering Approach to Digital Design" Printice Hall of India, New Delhi 1990
4. William H. Gothmann, "Digital Electronics, An Introduction to Theory and Practice", 2nd edition, PHI, 2009

Evaluation Scheme:

The questions will cover all the chapters of the syllabus. The evaluation scheme will be as indicated in the table below
Chapters Hours Marks distribution*

Chapters	Hours	Marks distribution*
1	3	6
2	1	4
3	5	8
4	5	10
5	5	8
6	5	8
7	2	4
8	5	8
9	8	12
10	4	8
11	2	4
Total	**45**	**80**

* There could be a minor deviation in the marks distribution.