36 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2071 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. What are the major differences between computer architecture and computer organization? What does the width of data bus and address bus represent in a system? Why is bus hierarchy required? [2+2+2]
2. Explain the general organization of register in CPU. Describe the operation of LD (load) instruction under various addressing modes with syntax. [6+4]
3. What are the different types of instructions? How can you perform X = (A+B) × (C+D) operation by using zero, one, two and three address instruction format. Assume A, B, C, D, X are memory address. [3+5]
4. What is address sequencing? Explain the selection of address for control memory with its block diagram. [3+7]
5. Explain the Arithmetic pipeline and instruction pipeline with example. [10]
6. Draw the flowchart for floating point Division. [4]
7. Design a booth multiplication algorithm hardware. Multiply 5 and -6 using booth multiplication algorithm. [4+4]
8. Explain cache organization. Explain the cache mapping techniques with example. [4+6]
9. Highlight the role of I/O interface in a computer system. Describe the drawbacks of programmed I/O and interrupt driven I/O and explain how DMA overcomes their drawbacks. [4+6]
10. How can multiprocessor be classified according to their memory organization? Explain. [4]

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36 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2072 Kartik

Exam.	New Back (2066 & Later Batch)		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Differentiate between computer architecture and computer organization. Explain the computer functions with different cycles. [3+5]
2. Write a code for Y = (A+B)*(C+D)+G/E*F using three address, two address one address and zero address instruction format. [8]
3. Mention the different types of addressing mode and compare each other. [10]
4. Explain the address sequencer with the help of a block diagram. Explain about microinstruction format in detail. [5+5]
5. Define pipeline and explain its types. Describe different pipeline hazards with example. [4+6]
6. Draw the flowchart for restoring division method. [4]
7. Explain Booth multiplication algorithm. Multiply -6×12 using Booths algorithm. [4+6]
8. Draw the memory hierarchy. Explain Associative Cache Mapping with example. [2+6]
9. What are the different types of priority interrupt? Explain the communication between CPU and IOP with necessary block diagram. [4+6]
10. Explain about multiprocessor and multiprocessing in brief. [4]

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INSTITUTE OF ENGINEERING
Examination Control Division
2071 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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37 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2071 Shawan

Exam.	New Back (2066 & Later Batch)		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
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1. What do you understand by Bus Interconnection? What are the driving factors behind the need to design for performance? [2+4]

2. Explain Instruction Format with its types? Illustrate the code to evaluate to evaluate: Y = (A+B) * (C+D) using three address, two address, one address and zero address instruction formats. [2+6]

3. Describe the instruction cycle state diagram? Design a 2-Bit ALU that can perform addition, AND, OR operations. [3+3]

4. Explain the organization of a control memory. Discuss the microinstruction format with the help of a suitable example. [4+6]

5. Discuss about parallel processing? How parallel processing can be achieved in pipelining, explain it with time-space diagram for four segments pipeline having six tasks. [4+6]

6. Write down the detail algorithm of Booth Multiplication. Illustrate the multiplication of (9) and (-3) using 2's complement method. [5+5]

7. What is Memory Hierarchy and why it is formed in computer system? Explain the Direct cache memory mapping technique using organization diagram and appropriate example. [3+6]

8. What are the functions of I/O Module? What is the purpose of priority interrupt; explain priority interrupt types with key characteristics. [3+7]

9. Differentiate the following [4x3]

   a. RISC and CISC
   b. Restoring and Non-Restoring Division
   c. Crossbar Switch and Multistage Switching Network

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2071 Chaitra

Exam.	Regular		
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Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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- ✓ *Assume suitable data if necessary.*

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2. Explain the general organization of register in CPU. Describe the operation of LD (load) instruction under various addressing modes with syntax. [6+4]
3. What are the different types of instructions? How can you perform X = (A+B) × (C+D) operation by using zero, one, two and three address instruction format. Assume A, B, C, D, X are memory address. [3+5]
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9. Highlight the role of I/O interface in a computer system. Describe the drawbacks of programmed I/O and interrupt driven I/O and explain how DMA overcomes their drawbacks. [4+6]
10. How can multiprocessor be classified according to their memory organization? Explain. [4]

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37 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2070 Ashad

Exam.	New Back (2066 & Later Batch)		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. What is performance balance and why is it required? Explain different elements of bus design. [6]
2. Define the addressing mode and explain the different types of addressing modes with example. [10]
3. What are the stages of ALU design? Explain with the example of 2-bit ALU performing addition, subtraction, OR and XOR. [8]
4. What are the differences between hardwired implementation and micro-programmed implementation of control unit? Explain with steps involved when you are designing micro-program control unit. [4+6]
5. What is instruction hazard in pipeline? What is the four segment instruction pipeline? Explain with example. [2+8]
6. How division operation can be performed? Explain with its hardware implementation. [10]
7. Draw a flowchart of floating point subtraction. [4]
8. What are the major differences between different cache mapping techniques? Suppose main memory has 32 blocks and Cache memory has 8 blocks when 10 blocks of main memory are used, show how mapping is performed in direct mapping technique. [6+2]
9. Differentiate between programmed I/O, interrupt-driven I/O and direct memory access (DMA). [10]
10. Explain the interprocessor synchronization with example. [4]

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36 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2070 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Explain the interconnection of CPU with Memory and I/O devices along with different operations over them. [3+3]
2. Write down the Y = A/B+(C×D) + F(H/G) equation in three address, two address, one address and zero address instruction. [8]
3. Mention the different types of addressing modes. Compare each of them with algorithm as well as advantages and disadvantages. [10]
4. Differentiate between hardwired and micro-programmed control unit. How does a sequencing logic work in micro-programmed control unit to execute a micro-program? [4+6]
5. Explain the arithmetic pipeline and instruction pipeline with example. [10]
6. Explain the non-restoring division along with its algorithm, flowchart and example. [8]
7. Explain the Booth algorithm and multiply Y = 8×9 using Booth algorithms. [6]
8. Mention the characteristics of computer memory. Differentiate between associative mappings and set associative mapping with example. [3+5]
9. How does DMA overcome the problems of programmed I/O and interrupt-driven I/O techniques? Explain. [5]
10. Why IOP is use in I/O organization? Explain. [5]
11. Explain the characteristics of multiprocessors. [4]

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36 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2068 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: -Computer Organization and Architecture *(CT 603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Explain the functional view and four types of operations used in computer. [6]
2. What are most common fields in an instruction? How can you perform X=(E+F)*(G+H) operation by using zero, one, two and three address instruction format. Assume that E, F, G, H and X are memory addresses. [8]
3. Define addressing mode. Explain different types of addressing modes with example. [10]
4. Explain various fields in micro-instruction format with neat and clean block diagram. Describe how address of control memory is selected. [3+7]
5. What are the hazards in instruction pipelining? How can they be resolved? Explain. [10]
6. Explain Booth algorithm. Use the Booth algorithm to multiply 23(multiplicand) by –21(multiplier), where each number is represented using 6 bits. [8]
7. Explain floating point division algorithm. [6]
8. Explain cache read operation. What are the demerits of direct mapping technique used in cache design and describe in details any one of the mapping technique that solves these problems. [8]
9. Why input-output processor is needed in an input-output organization? Explain with block diagram. [10]
10. Define the multiprocessor and its characteristics. [4]

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42 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2068 Baishakh

Exam.	Regular / Back		
Level	BE	Full Marks	80
Programme	BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Architecture and Design

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Write down the following equation in three addresses, two addresses, one address and zero address instruction. If necessary, use temporary location T to store intermediate result. Y = A + (B*C) + D. [8]
2. What are the different types of addressing modes? Compare each of them with algorithm as well as advantages and disadvantages. [8]
3. Differentiate between restoring division and non restoring division with example. [8]
4. What are the three types of control signals? Explain the key steps of hardware implementation of control unit. [3+7]
5. What do you mean by mapping process? Differentiate between direct, associative and set associative mapping. [2+8]
6. Explain the key characteristics of computer memory systems. [8]
7. Explain the input/output interface with example. [6]
8. Compare between program I/O, interrupt driven I/O and Direct Memory Access (DMA). [8]
9. What are the steps to configure the plug and play device? Explain. [6]
10. What are the main goals of the plug and play BIOS specification? Explain. [8]

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42 TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2067 Ashadh

Exam.	Regular/Back		
Level	BE	Full Marks	80
Programme	BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Architecture and Design

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Write down the Y=AB÷ (F/G) +CD equation in three-address, two address, one address and zero address instruction. (8)
2. What are the three types of data manipulation instructions used in computer? Explain. (8)
3. Explain the Booth algorithm and its hardware implementation. Multiply the 6×7 using Booth algorithm. (4+4)
4. What do you mean by address sequencing? Explain the address sequencing capabilities required in a control memory. (3+5)
5. Why replacement algorithm is used when designing the cache? Explain with example. (8)
6. Why cache management is necessary in mapping process? Differentiate between direct mapping address structure and associative mapping address structure. (2+6)
7. What are the four types of I/O commands that an interface receive during the communication link between the processor and peripherals? Explain the I/O bus and interface modules. (4+4)
8. Mention the three possible configurations of DMA and compare them. (8)
9. Explain the PnP device configuration with example. (8)
10. Define the terms. (4×2=8)
    a) ISA
    b) PnP Post

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