UController/CPLD/FPGA Register Transfer Bus

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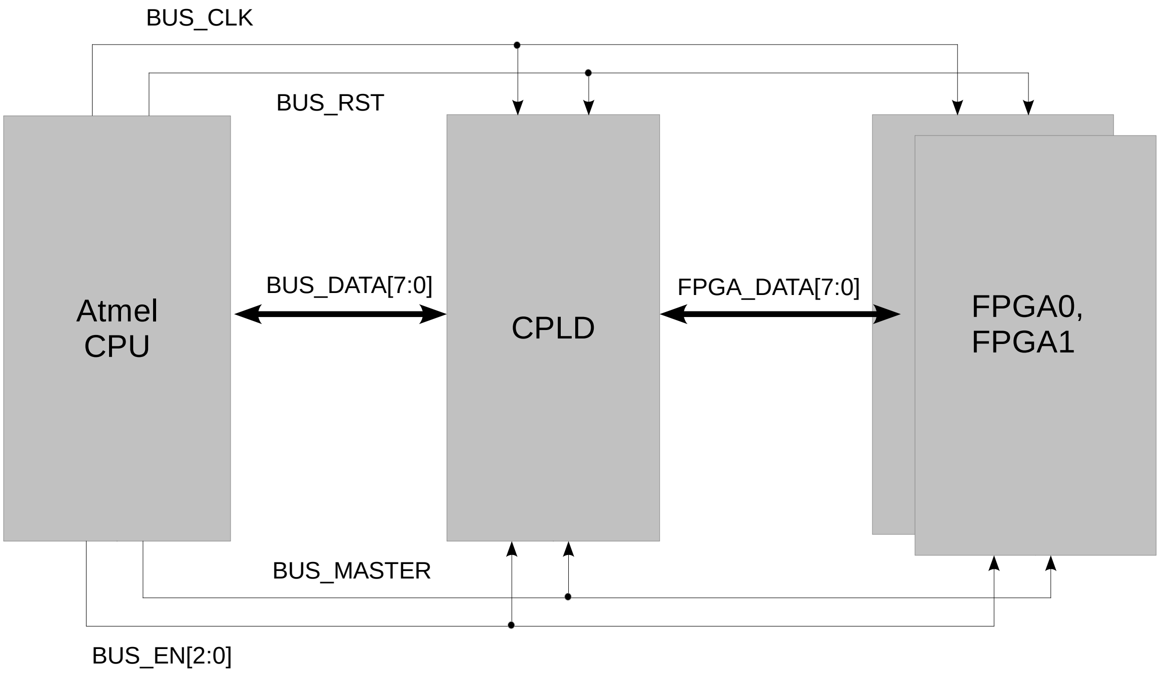
Overview

The uC register transfer bus is used to update and read control registers in the CPLD and two FPGAs. The toplogy is shown in the below diagram.



The uController (uC) serves as the master and drives control and data/address signals to three slave devices (CPLD and the two FPGAs). The interface between all devices is asynchronous. The uC bit bangs GPIOs to drive voltage levels. The CPLD and FPGAs capture data based on a strobe (BUS_CLK) and synchronizes data/address to internal clock domains. The uC identifies the target device through BUS_EN[2:0]. In the event the target is one of the FPGAs, the CPLD acts as a pass through device which connects BUS_DATA[7:0] to FPGA_DATA[7:0].

Each beat of data or address is 8b in size. Write data from uC to CPLD/FPGAs can be bursted with no limit in the number of data beats – however the data must be 4B aligned. Target devices accumulate write data in 4B chunks and continue incrementing the initial base address until the write operation is terminated. Read data transfers from CPLD/FPGAs are fixed at up to 4B in size (the current protocol does not specify read data size). On reads of data quantities less than 4B (i.e. on a 1B read), the uC can negate BUS_EN to terminate the transaction early. All transactions must be terminated by negating BUS_EN before starting the next transaction, allowing hardware state machines to identify the end of an operation.

The uC utilizes an asynchronous reset (BUS_RST) which is used to reset all state back to the reset state. In the unexpected condition of an error or hang, the reset signal can be used to recover the UC register transfer interface.

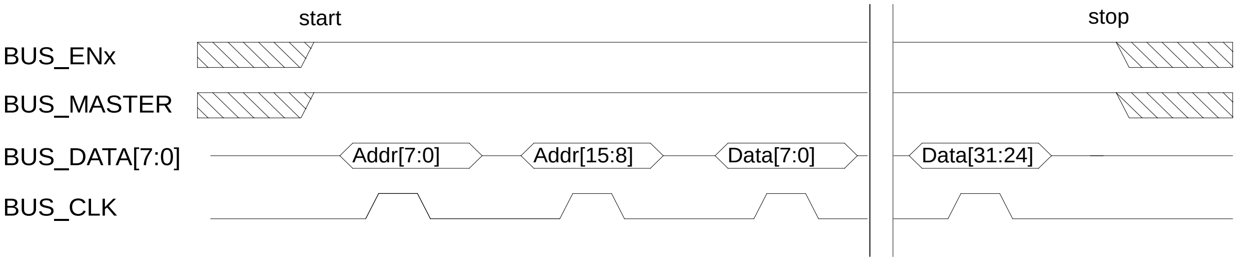
Interface Signal Description

uController to CPLD/FPGA Asynchronous Interface

Signal	Source	Description
BUS_DATA[7:0] (FPGA_DATA[7:0])	Bi-directional –CPLD or slave master	Contains either control register addresses or data. Driven by the UC on writes with two beats of address and multiple beats of data. Driven by slave devices in response to master read requests to return read data. Connected to FPGA_DATA[7:0] by the CPLD in the event the target device is one of the FPGAs.
BUS_CLK	uC master	Strobe to indicate data on BUS_DATA[7:0] is valid. Asserted by the uC on writes to strobe address and write data beats. Asserted by the uC on reads to strobe addresses. Asserted by the uC when read data returns from the slave device to indicate the current beat of data has been received and the next beat of data can be driven by the slave device.
BUS_MASTER	uC master	Driven by uC to indicate it has ownership of BUS_DATA[7:0]. Slave devices must wait for negation of BUS_MASTER before driving data on BUS_DATA[7:0]/FPGA_DATA[7:0].
BUS_EN[2:0]	uC master	Per target chip select. - BUS_EN[0] : FPGA0 - BUS_EN[1] : FPGA1 - BUS_EN[2] : CPLD Asserted to initiate a transaction to the specific target. Must be held through the operation. Negation indicates termination of the transaction. If negated during the middle of a transaction, the current transaction should be immediately terminated. ***Must be negated at the end of every transaction to reset FPGA/CPLD state machines.*** This must be a one-hot signal – only one enable can be asserted at a time.
BUS_RST	uC master	Global asynchronous reset used to reset the UC / PLD / FPGA register transfer interface. Must be held constant by the UC for 1us(?).

Write Operations

Control register writes to either the CPLD or FPGA are initiated by the uC on the asynchronous BUS_.... interface. The uC first asserts BUS_EN{0,1,2} to indicate the target. BUS_MASTER is also asserted to indicate the uC is the master of the BUS_DATA[7:0] bus. Generally, the uC should assert BUS_MASTER except when waiting for control register read responses. The uC drives two beats of address to indicate the control register write address, followed by multiple beats of write data. The msb bit (Addr[15]) is asserted to indicate a write. Data is strobed by BUS_CLK to indicate the data is valid. Slave devices perform an edge detect on the low to high transition of BUS_CLK to capture address or data.



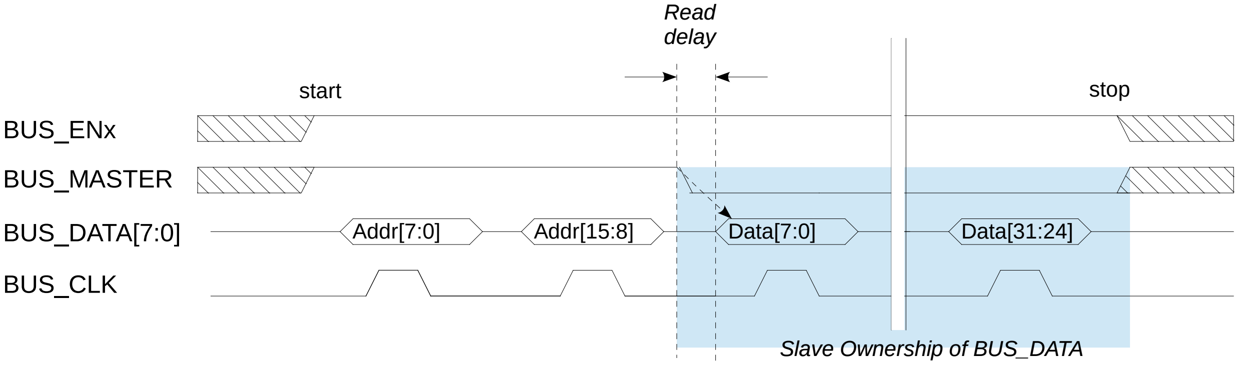
Address and data beats are driven in little endian order with low order bytes driven first. On writes, the uC is allowed to continue bursting write data in 32bit chunks. Slave devices accumulate write data in one byte beats, and when 4 beats of write data have been accumulated, the slave device performs the write. Slave devices automatically increment the initial base address for each double word write.

In the event the device target is one of the FPGAs, the CPLD connects BUS_DATA and FPGA_DATA, providing point to point communication between the uController and the FPGA. Whether the target is the CPLD or FPGA, the write protocol operates exactly the same.

Slave devices perform an address check to determine the validity of the write addresses. In the event of a bad address, the write operation is dropped and an error is logged. The protocol has been kept simple and does not currently support acknowledgement of writes.

Read Operations

Similar to control register writes, control register reads are initiated by the uC on the asynchronous BUS_.... interface. The uC first asserts BUS_EN{0,1,2} to indicate the target. BUS_MASTER is also asserted to indicate the uC is the master of BUS_DATA[7:0]. The uC drives two beats of address to specify the control register address – the msb bit (Addr[15]) must be zero to indicate a read operation. After the second beat of address has been strobed, the uC negates BUS_MASTER to relinquish control of BUS_DATA. Prior to negating BUS_MASTER the UC must stop driving BUS_DATA. After a read-delay which is determined by the time it takes the slave device to perform the control register read, the slave device drives read data onto the BUS_DATA/FPGA_DATA bus.



To receive multiple beats of read data, the uC uses BUS_CLK as a handshake back to the slave device to indicate the read data has been received. After driving read data, the slave device waits for a low to high transition of BUS_CLK before driving the next beat of read data. This handshake continues until all 4 beats of read data (4x8bits) have been transferred. Read data is currently fixed at 32bits – the protocol does not specify read data sizes.

The slave devices operate much faster than the uController. The expectation is that by the time the uController starts to read the data off its GPIOs, the slave devices have already driven the data and it is stable. If required, the uController can wait a pre-defined period of time before access the read data on its GPIOs.

Slave devices perform a valid address check. All reads return data. If an invalid address or error occurs, the slave devices returns 0xDEADBEEF as data.

Implementation Details

After updating all SFPs, the uC **must** indicate interval done (check FPGA stats address map) to release a bank select lock. Assertion of interval done promotes the recently written bank for reading by the link engine.

Register Address Map

The FPGA UC address space is 16b. The addresses point to double word sized quantities (*e.g.* address 0x0 points to 32b of data, address 0x1 points to next 32b of data). The addresses are mapped as shown below:

[15]	[14:12]	[11:10]	[9:0]
1b – rd/wr control 0=read 1=write	3b - Reserved Unused control fields	2b – Address Space ID 2'b00 : SFP stats 2'b01 : FPGA stats 2'b10 : reserved 2'b11 : reserved	10b - per address space offset

- [15:12] : The upper 4b are used as control fields to specify operation type. Currently, only bit[15] is used to indicate read or write operation. Bits [14:12] are reserved.
- [11:10] : Address space ID. Indicates address space type.
- [9:0] : Per address space offset

Generally, writes to reserved space are dropped while reads to reserved space return 0xDEADBEEF. Refer to the following sections for more details of reserved space operation.

SFP Stats Address Map

The address space for SFP stats is located at Addr[11:9]=2'b00. Bits [9:5] specify the SFP – up to 32 total SFPs per FPGA. Bits [4:0] specify per SFP stats.

[15]	[14:12]	[11:10]	[9:5]	[4:0]
1b – rd/wr control 0=read 1=write	= 3'b000	= 2'b00	5b – SFP selector	5b - Per SFP stats 32-double words (128B total)

Per SFP, the address map is shown below:

Addr [4:0]	**Byte 3 (MSB)**	**Byte 2**	**Byte 1**	**Byte 0 (LSB)**	**Description**
0x0	Vendor OUI Byte 2	Vendor OUI Byte 1	Vendor OUI Byte 0	SFP Present	Contains two fields: - Vendor OUI : 3 Byte vendor IEEE Company identifier, all zero indicates OUI is unspecified. Finisar transceivers contain values 00h, 90h, and 65h. This field consists of a character string where byte 0 corresponds to the first character in the string. - SFP Present : 00h indicates not present 01h indicates present FFh reset state, indicates unknown
0x1	Vendor Part Number Byte 3	Vendor Part Number Byte 2	Vendor Part Number Byte 1	Vendor Part Number Byte 0	Vendor part number (PN). 16 byte field that contains ASCII characters, left aligned, and padded on the right with ASCII spaces (20h). Defines the vendor part number or product name. All zeros indicates Vendor PN is unspecified. This field consists of a character string where byte 0 corresponds to the first character in the string.
0x2	Vendor Part Number Byte 7	Vendor Part Number Byte 6	Vendor Part Number Byte 5	Vendor Part Number Byte 4	
0x3	Vendor Part Number Byte 11	Vendor Part Number Byte 10	Vendor Part Number Byte 9	Vendor Part Number Byte 8	
0x4	Vendor Part Number Byte 15	Vendor Part Number Byte 14	Vendor Part Number Byte 13	Vendor Part Number Byte 12	
0x5	Vendor Serial	Vendor Serial	Vendor Serial	Vendor Serial	

	Number Byte 3	Number Byte 2	Number Byte 1	Number Byte 0	The vendor serial number (vendor SN) is a 16 character field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor's serial number for the transceiver. A value of all zero in the 16-byte field indicates that the vendor PN is unspecified. This field consists of a character string where byte 0 corresponds to the first character in the string.
0x6	Vendor Serial Number Byte 7	Vendor Serial Number Byte 6	Vendor Serial Number Byte 5	Vendor Serial Number Byte 4	
0x7	Vendor Serial Number Byte 11	Vendor Serial Number Byte 10	Vendor Serial Number Byte 9	Vendor Serial Number Byte 8	
0x8	Vendor Serial Number Byte 15	Vendor Serial Number Byte 14	Vendor Serial Number Byte 13	Vendor Serial Number Byte 12	
0x9	Vendor Revision Number Byte 3	Vendor Revision Number Byte 2	Vendor Revision Number Byte 1	Vendor Revision Number Byte 0	The vendor revision number (vendor rev) is a 4-byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor's product revision number. A value of all zero in the 4-byte field indicates that the vendor rev is unspecified. All legacy Finisar transceivers contain zero in all 4 bytes or ASCII space (20h) in all four bytes or one of two place holders: "X1—" or "1A—".
0xA	Reserved (reads return indeterminate value))	Nominal Bit Rate	SFP Temperature Byte 1 (MSB)	SFP Temperature Byte 0 (LSB)	SFP Temperature : Internally measured transceiver temperature. Represented as a 16 bit signed twos complement value in increments of 1/256 degrees Celsius, yielding a total range of – 128°C to +128°C. Temperature measurement is valid from –40°C to +125°C with an accuracy of ± 3°C. The temperature sensor is located in the center of the module and is typically 5 to 10 degrees hotter than the module case. Nominal Bit Rate: 1 Byte field – specifies nominal bit rate in units of 100 Megabits/sec, rounded off to the nearest 100 Megabits/sec. The bit rate includes those bits necessary to encode and delimit the signal as well as those bits carrying data information. A value of 0 indicates that the bit rate is not specified.
0xB	SFP TX Power Byte 1 (MSB)	SFP TX Power Byte 0 (LSB)	SFP RX Power Byte 1 (MSB)	SFP RX Power Byte 0 (LSB)	TX Power : Measured TX output power in mW. Represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0 – 65535) with LSB equal to 0.1 µW, yielding a total range of 0 to 6.5535 mW (~ -40 to +8.2 dBm). Data is factory calibrated to absolute units using the most representative fiber output type. Accuracy is ±3dB. Data is not valid when the transmitter is disabled. RX Power : Measured RX received average optical power in mW. Represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0 – 65535) with LSB equal to 0.1 µW, yielding a total range of 0 to 6.5535 mW (~ -40 to +8.2 dBm). Absolute accuracy is dependent upon the exact optical wavelength. For the specified wavelength, accuracy is ±3dB.
0xC	Warning Flags				Warning flags. Once set, remains set until link engine read and UC write to zero. refer to Finisar spec for more details: http://www.finisar.com/sites/default/files/pdf/appnotes/ylZNRYapp%20note%201.pdf
0xD	Alarm Flags				Alarm flags. Once set, remains set until link engine read and UC write to zero. refer to Finisar spec for more details: http://www.finisar.com/sites/default/files/pdf/appnotes/ylZNRYapp%20note%201.pdf
0xE	Reserved (reads return indeterminate value)	Reserved (reads return indeterminate value)	Reserved (reads return indeterminate value)	SFP Number	SFP Number : hardcoded SFP number. Used to debug and test interface. Upper 3 bytes are reserved and always return zero. This location is read-only.
0xF – 0x1F	Reserved				Reserved for future use. Can be read and written and used as scratch space.

FPGA Stats Address Map

The address space for FPGA stats is located at Addr[11:10]=2’b01.

[15]	[14:12]	[11:10]	[9:0]
1b – rd/wr control 0=read 1=write	= 3’b000	= 2’b01	10b - per address space offset

The address map is shown below:

Addr [9:0]	Byte 3	Byte 2	Byte 1	Byte 0	Description
0x0	Reserved (reads return indeterminate value)	Reserved (reads return indeterminate value)	Reserved (reads return indeterminate value)	FPGA Temperature	FPGA temperature using on chip temperature sensing junction diode. 8-bit signal that contains the analog-to-digital-conversion temperature value. The 8-bit value maps to a unique temperature value. Temperature range is -70C to +127C. During device power-up or before the temperature value is valid, this field is set to 11010101 Refer to Altera documents (Table 3-2) for more details: http://www.altera.com/literature/ug/ug_alttemp_sense.pdf This location is read-only.
0x1	0x1 – indicates UC write interval done All other fields are reserved.				UC write interval done. Writing a 0x1 indicates the current uC SFP stat write interval has been completed. On writes to SFP stat space, the FPGA locks the SFP RAM bank select and waits for the uC to indicate all writes are done before promoting the current write bank for reads by the link engine.
0x2	Reads return 0xC001C0DE				Read-only C001C0DE register. Returns static value which can be used to test the UC register transfer interface. Writes do not work.

0x3	PCIE status	PCIE status register. Monitored to identify PCIE issues. [7:0] – Current LTSSM state [4:0] : LTSSM state [7:5] : hardwired to 3’b00 [11:8] – Negotiated speed of PCIE interface 0001 : Gen1 0010 : Gen2 0011 : Gen 3 All other encodings reserved [15:12] – Negotiated width of PCIE interface 0000 : lanes x1 0001 : lanes x2 0010 : lanes x4 0011 : lanes x8 All other encodings reserved [31:16] – PCIE Misc Status [16] : PIN_PERST_n [17] : hip_rst_pld_clk_inuse (1 indicates good) [18] : hip_rst_pld_core_ready (1 indicates good) [19] : hip_rst_serdes_pll_locked (1 indicates good) [20] : hip_rst_reset_status (0 indicates good [21] : reconfig_busy (0 indicates good) [22] : hip_status_dlup (pulses 1-0-1 on exit from data link up) [23] : hip_status_l2_exit (1 indicates good) [24] : hip_status_hotrst_exit (1 indicates good) [25] : hip_status_dlup_exit (1 indicates good) [26] : APP_RST_n_STATUS [27] : rst_controller_out_reset [28] : iRST_NPOR_n [29] : heart_beat – toggles at PCIE clock rate [31:30] : reserved – set to zero
0x4	PCIE Reset	Writing any value to this register initiates a PCIE reset through the PERST_n pin.
0x5	FPGA Version 0	Bits [31:0] of FPGA Version register: [7:0] : BitfileRev[7:0] [15:8] : Author[7:0] [31:16] : RepoRev[15:0]
0x6	FPGA Version 1	Bits [63:32] of FPGA Version register: [7:0] : RepoRev[23:16] [31:8] : yymmdd[15:0]
0x7 0x3FF	Reserved – read return 0xDEADBEEF	Reserved for future use. Cannot be written. Reads return 0xDEADBEEF.