Chia-Ho Lin

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Area of Interest

Topics: Computer vision, Deep Learning, Image/Video processing, Multimedia Algorithm

Skills: Digital IC design, DSP in VLSI, Architectural design

Jobs: Algorithm & Architecture, Digital IC design, Software Engineering

Education

National Taiwan University (NTU), Taiwan 09/2016 – Present
M.S. in Electronics Engineering ● GPA: 4.15/4.3
Advisor: Prof. Liang-Gee Chen

09/2012 – 06/2016
National Taiwan University (NTU), Taiwan
B.S. in Electronics Engineering ● GPA: 3.97/4.3 ● Ranking: 36/190

Research Project

Deep Learning and Its Applications:

- Master's Thesis: Low-power DNN algorithm for egocentric Human-Object Interaction 07/2017 – Present
  Advised by Prof. Liang-Gee Chen
  - Design an CNN-based algorithm to recognize interplay between human and object
  - Specification: given a video, produce <verb,object> recognition
  - Feature: better late fusion for deep feature aggregation
  - Contribution: zero-shot learning for unseen verb-object pair

Computer Vision:

- Improved Trajectories with better optical flow engine 02/2016 – 06/2017
  Advised by Prof. Liang-Gee Chen
  - Proposed a hardware-friendly algorithm and better dataflow for optical flow engine
- Image Detail Enhancement Using CUDA/OpenCL 02/2015 – 01/2016
  Advised by Prof. Shao-Yi Chien
  - Performance optimization for gaussian, bilateral and guided filter by CUDA parallel implementation
  - 100x speedup compared to original one
- Image Segmentation algorithm implementation 02/2015 – 06/2015
  Advised by Prof. Jian-Jiun Ding
  - Superpixel algorithm implementation

Wireless Communications:

- Device-to-Device Communication & 4G LTE 09/2014 – 01/2015
  Advised by Prof. Hung-Yu Wei
  - Resource allocation simulation and analysis

Course Project

Deep Learning and Its Applications:

- Machine Learning and having it deep and structured
  - Project: A label classifier by deep neuron network for Cyber Security Attack Defender (~200 lines Python code by keras)
  - Ranked 20% in Kaggle competition of the class

Digital IC Design / DSP in VLSI:

- Computer-aided VLSI System Design
  - Project: LZSS Compression Encoder (~500 lines Verilog code)
  - Be familiar with IC Design flow (RTL, Design Compiler, SOC Encounter)
- Multimedia System-on-chip Design
  - Project: Zynq Video Denoise System
  - Learned to improve FPS by DMA, bus and IPs in FPGA system
- Digital System Design
  - Project: Pipelined MIPS processor by Verilog (~700 lines Verilog code)
- Electrical Engineering Lab (digital Circuit)
  - Project: Dynamic object remover capable of removing moving object in several continuous shooting photographs on FPGA processor

Algorithm:

- Digital Visual Effects
  - Project: Image stitching implementation (~1000 lines Matlab code)
  - Learned to survey and implement parts of DSP-related paper
- Data Structure and Programming
  - Project: C++ program to functionally reduce And-Inverter graph to improve the product of cycle time and area of a schematic diagram (2000~3000 lines C++ code)
- GPU Programming
  - Project: CUDA implementation for state-of-the-art image stitching algorithm
- Algorithm
  - Project: Color Balancing for Double Patterning (can be mapped to IC layout design problem)
  - Participated in The 2015 CAD contest at ICCAD (domestic tournaments)

Mobile/Web Application Development:

- Intelligent Devices and Cloud Computing
  - Project: Smart Google Scholar searching system
  - Developed a back-end paper ranking system (Apache Spark) and front-end app/web interface (ReactJS).

Technical Skills

Programming:

Proficient: C/C++, Verilog. Python, Matlab, CUDA/OpenCL
Basic: HTML/CSS/Javascript

Tool:

Keras/Tensorflow, Verdi, NC-verilog, Design Compiler, SoC encounter, ReactJS

Publications

- **Chia-Ho Lin**, Yuhsiang M. Tsai, Weichung Wang and Liang-Gee Chen, "GPU-Accelerated High-Resolution Image Stitching with Better Initial Guess", in IEEE International Conference on Consumer Electronics (ICCE), Las Vegas, USA, Jan 2018.
- Chun-Wei Yu, **Chia-Ho Lin**, Yu-Sheng Wu, and Liang-Gee Chen, "Architecture and Algorithm Design of High Frame Rate Optical Flow Engine", in VLSI design/CAD symposium, Kaohsiung, Taiwan, Aug 2016.

Language Proficiency

English:

TOEIC: 900/990 (L: 440/495; R:460/495)
GEPT: High-Intermediate passed (L: 99/120; R:112/120; W:80/100; S:80/100)

Chinese: Native Speaker
Japanese: Basic