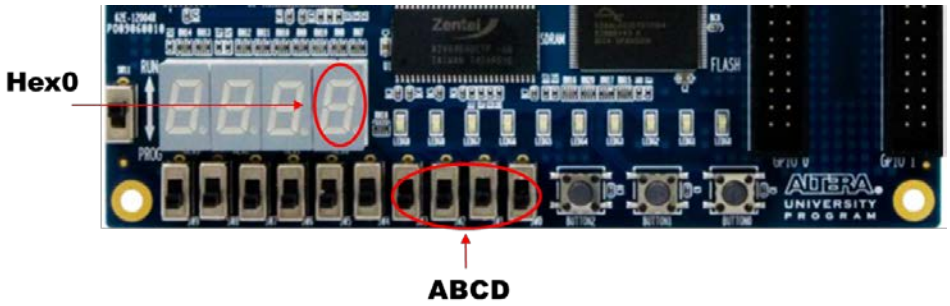
Lab 2- VHDL Design Using Dataflow Architectural Style

In this lab we will design a 4-input prime number detector in VHDL. We also practice making the required pin assignments via the DE0_pin_assignments.qsf for the DE0 board.

Lab 2.1:

Design a 4-input 7-segment display decoder:

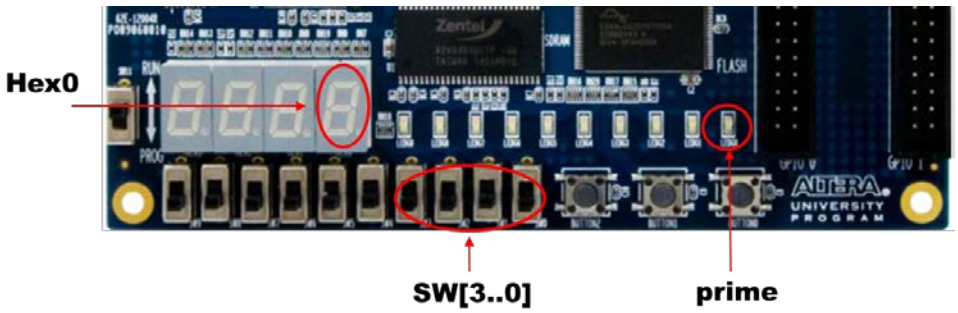
The display will show characters 0_{16} to F_{16} corresponding to the 4-bit input as shown on page 14 of "lab2_instruction.ppt".



Lab 2.2:

Design a 4-Input Prime Number Detector:

- We will design a 4-input prime number detector, taking in numbers between 0_{10} and 15_{10}. This requires your detector to have four binary inputs (0000_2 to 1111_2).
- The definition of a prime number is: "A Prime Number can be divided evenly only by 1 or itself and it must be a whole number greater than 1." By this definition, the prime numbers between 0_{10} and 15_{10} are: 2, 3, 5, 7, 11 and 13.
- The assertion of prime number is shown on $LEDG_0$, and the input number is shown on HEX_0.



Lab-report:

Submit a lab report on **ilearn** by 11:59pm the day before of next lab. (The lab report must be a **PDF** file.) Your Lab report should include the following items:

1) VHDL code for the 4-input 7-segment display decoder.

2) VHDL code and its functional simulation for the 4-Input Prime Number Detector.

3) observations and comments.