Lab 3- Combinational Circuits(I): Using VHDL

The goal of this lab is to design combinational circuits using VHDL's concurrent statements.

Lab 3.1:

Design a customized 7-segment decoder:

Figure 1 shows a customized 7-segment decoder module that has two-bit input c_1c_0. This decoder produces seven outputs that are used to display a character on a 7-segment display. Table 1 lists the characters that should be displayed for each valuation of c_1c_0. ("blank" character is selected for c_1c_0 =11). Each segment in the display is illuminated by driving it to the logic value 0.

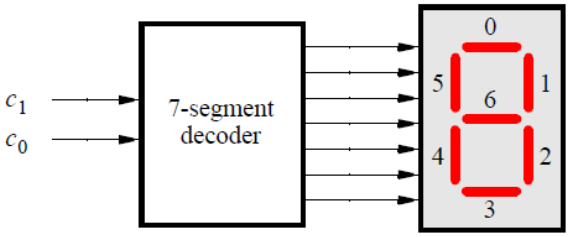
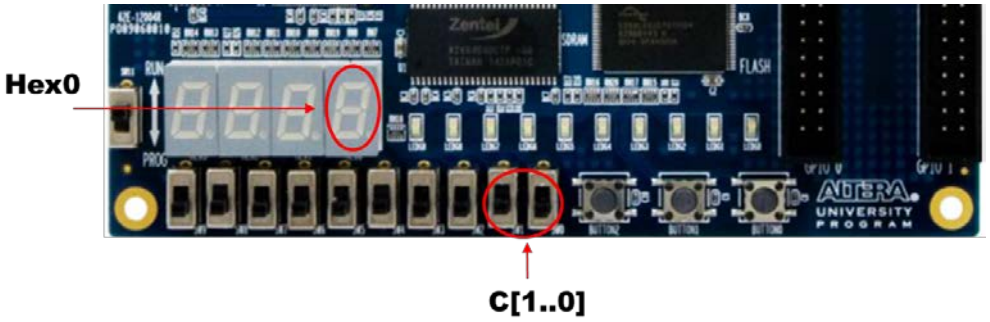


Figure 1.

c_1c_0	Character
00	d
01	E
10	0
11	

Table 1. Character codes

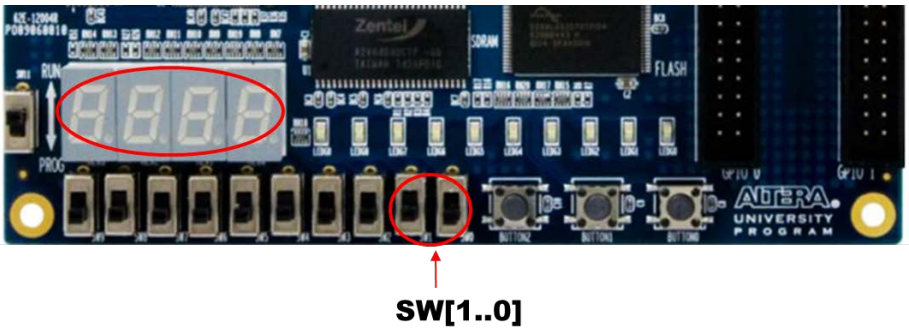
- Write a VHDL code for the customized 7-segment decoder. Connect the c_1c_0 inputs to switches SW_{1-0}, and connect the outputs of the decoder to the HEX0 display on the DE0 board.



Lab 3.2:

Display specified characters on four 7-segment displays:

This time, design a circuit that will display characters d, E, 0, and "blank" on four displays (HEX3, HEX2, HEX1, and HEX0), depending on the setting of SW_{1-0}, respectively. That is when SW_{1-0} = 00, Hex3 shows character 'd' and others are blank; when SW_{1-0} = 01, Hex2 shows character 'E' and others are blank; when SW_{1-0} = 10, Hex1 shows character '0' and others are blank; when SW_{1-0} = 11, all Hex's are blank.



Lab-report:

Submit a lab report on **ilearn** by 11:59pm the day before of next lab. (The lab report must be a **PDF** file.) Your Lab report should include the following items:

1) VHDL code for Lab 3.1.

2) VHDL code for Lab 3.2.

3) Observations and comments.