Lab 4- Combinational Circuits (II): Using VHDL

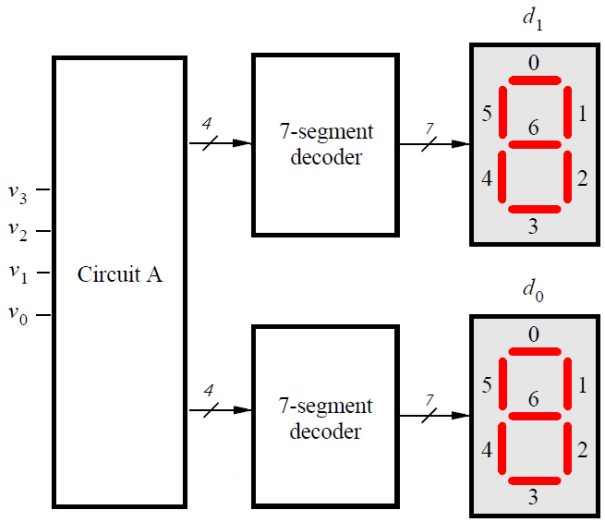
The goal of this lab is to design combinational circuits using VHDL's sequential statements, such as if-then-else and case-when.

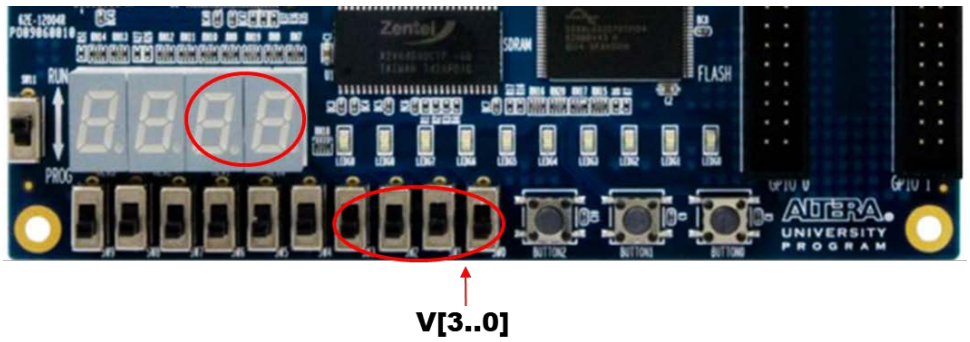
Lab 4.1:

A binary-to-decimal converter:

You are to design a circuit that converts a four-bit binary number V = $v_3v_2v_1v_0$ into its two-digit decimal equivalent D = d_1d_0. Table 1 shows the required output values. A partial design of this circuit is given in the following figure. Circuit A must check when the value of V is greater than 9, and use the outputs in the control of the 7-segment displays.

Binary value	Decimal digits	
0000	0	0
0001	0	1
0010	0	2
...	...	...
1001	0	9
1010	1	0
1011	1	1
1100	1	2
1101	1	3
1110	1	4
1111	1	5





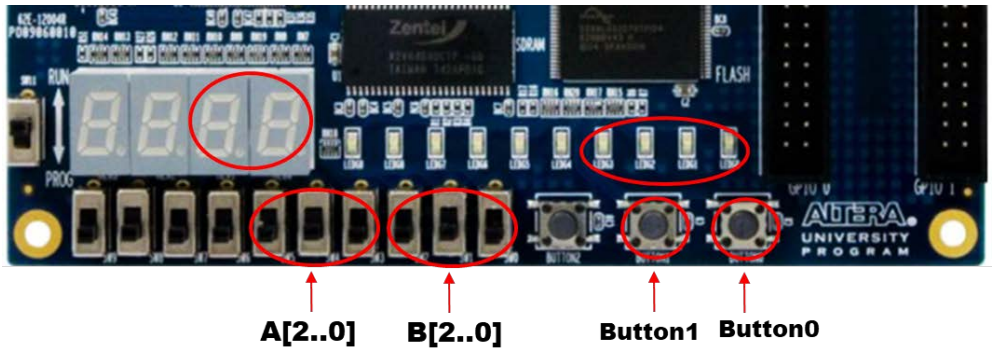
Lab 4.2:

A key-controlled displayed circuit:

DE0提供三個 push-buttons 按鈕開關,分別為Button2, Button1, Button0. 當開關按下後輸出低電位0V, 未按下時其輸出為高電位3.3V.

Given two 3-bit unsigned binary numbers A and B, a key-controlled displayed circuit is operated as follows,

- When Button0 is pushed, decimal value of A+B is shown on 7-segment displays.
- When Button1 is pushed, binary value of A+B is shown on leds.
- For other cases, nothing is displayed.



Lab-report:

Submit a lab report on **ilearn** by 11:00pm the day before of next lab. (The lab report must be a **PDF** file.) Your Lab report should include the following items:

1) VHDL code and 4-bit binary-to-decimal simulation for Lab 4.1.

2) VHDL code and A+B simulation for Lab 4.2.

3) observations and comments.