NCTU-EE DCS – 2017

Lab04 Exercise

Design: Tic-Tac-Toe

Data Preparation

1. Extract test data from TA's directory:

   % tar xvf ~dcsta02/LAB04.tar

2. The extracted LAB directory contains:

   a. EXERCISE/ : Exercise

Pattern Description

In this lab, you have to complete your test pattern and use it to check whether the design of LAB03 is passing or not. You are limited to using Random function to generate your test pattern which should be more than 2,000 test patterns. Once your PATTERN find out the error of the design, you should print out "initial_position", "input_sequence", and "Line_O/X" of both design and the correct value. Figure1 and Figure2 are the examples.

(This lab we are not going to provide the design file (.sv) for you, so you should use your own design of LAB03)

Figure 1.

```
------------------------------------------------------------------
      at initial_pos = #          2 and seq = #          0
                  Error !! The answer is wrong!
Your answer is  Line_X =  1 Line_O =  8  The Correct answer is X = 0 O =  8
------------------------------------------------------------------
```

Figure 2.

```
------------------------------------------------------------------
      at initial pos = #          6 and seq = #          0
                  Error !! The answer is wrong!
Your answer is  Line_X =  0 Line_O =  7  The Correct answer is X = 0 O =  8
------------------------------------------------------------------
```

Random Function Example:

(a)

temp = $urandom_range(511,0); //The value of temp is from 0 to 511

(b)

integer seed = 20; //You could change seed number to change the random number

temp = {$random(seed)} % 512; //The value of temp is from 0 to 511

Design Inputs

The signal ORIGIN is *unsigned 4 bits* input, which indicates initial position (it's range is 1~9). The signal SEQUENCE is *unsigned 9 bits* input and define state of sequence sheet "O" or "X" (0 indicates "O", 1 indicates "X").

Design Outputs

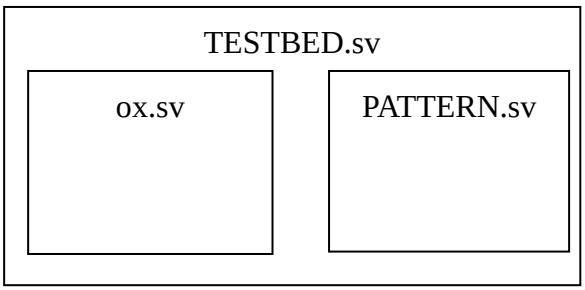
The signal Line_O is *unsigned 4 bits* input, outputs "O" bingo line number.

The signal Line_X is *unsigned 4 bits* input, outputs "X" bingo line number.

Design Specifications

1. Top module name : ox (File name: ox.v)
2. Input pins: Original_pos[3:0], Sequence[8:0].
3. Output pins: Line_O[3:0], Line_X[3:0].
4. **We will get back your code and do code checking with computer tool (No** plagiarism**)**

Block Diagram



Grading Policy

1. Run the RTL simulation and find out the error of our design
2. Use "Random" function to generate your test pattern
3. Generate more than 2,000 test patterns

Note

Template folders and reference commands:

1. 01_RTL/ (RTL simulation) **./01_run**
2. Upload **PATTERN.sv** to e3

Sample Waveform