NCTU-EE DCS – 2017

Lab02 Exercise

Design: Arithmetic Logic Unit (ALU)

Data Preparation

1. Extract test data from TA's directory:
   % tar xvf ~dcsta02/LAB02.tar
2. The extracted LAB directory contains:
   a. Exercise/ :your design

Design Description and Example Wave

An arithmetic logic unit (ALU) is a digital electronic circuit that performs arithmetic and bitwise logical operations on integer binary numbers. In this exercise, a string of instructions will be given. Your job is to decode these instructions and execute.

The following is the definition of the instruction.

instruction [10:8]	**instruction** [7:4]	**instruction** [3:0]
Mode	Data of Rs	Data of Rt
3-bit	4-bit	4-bit

Register (Rs) and Register (Rt) represent the data of registers. The instruction takes 3 bits to store the mode bit and takes 8 bits to store the data. Rs and Rt reserve 4 bits to store data.

e.g. Rs = 4'b0000 means the data of Rs is 0. Rt = 4'b0001 means the data of Rt is 1, and so on.

The following is the definition of the mode.

Mode[2:0]	Operation	Note
3'b000	Rs + Rt	Addition
3'b001	|Rs – Rt|	Absolute value after Subtraction
3'b010	Rs * Rt	Multiplication
3'b011	((Rs + Rt + 4'd15))/7	Division (accurate to the sixth digit after the decimal point)
3'b100	(Rs + Rt)<<2	Shift 2 bits

e.g. Mode = 3'b000、Rs = 4'b0010 and Rt = 4'b0001，
the result is out = 8'b00000011.

Inputs

I/O	Signal name	Description
Input	**Instruction[10:0]**	Described above

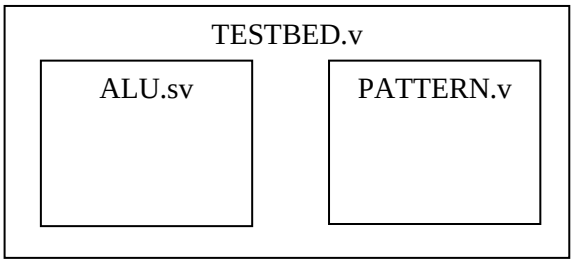
Outputs

I/O	Signal name	Description
output	**Out[8:0]**	Calculation result

Specifications

1. Top module name : ALU (File name : ALU.sv)
2. Input pins : **instruction[10:0]**
   Output pins : **out[8:0]**
3. All data in registers are unsigned number, including **out[8:0]**.
4. The maximal delay is 30ns.

Block Diagram



Upload File

1. ALU.sv (If renew, the original file should be replaced)

Grading Policy

1. Pass the RTL simulation.
2. Synthesis successful (no error)

Note

Template folders and reference commands:

1. 01_RTL/ (RTL simulation) **./01_run**
2. 02_SYN/ (Synthesis) **./01_run_dc**

Example Waveform