2023 Digital IC Design Homework 4

NAME	NAME 江坤諦					
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Simulation Result						
Functional		100			100	
simulation				simulation		
# Congratulations! Layer 0 data have been generated successfully! The result : # Congratulations! Layer 1 data have been generated successfully! The result : # terminate at 50184 cycle # *** Note: 5finish : C:/Users/Aaron/Desktop/dic-2023/BW4/file/testfixture.* # Time: 2509207454 ps Iteration: 0 Instance: /testfixture			PASS!!	S U M M A R Y Congratulations! Layer 0 data have been ger Congratulations! Layer 1 data have been ger terminate at 50125 cycle ** Note: Ofinish : testfixture.v(178) Time: 2509250 ns Iteration: 0 Instance	nerated successfully! The result is PASS!!	
Synthesis Result						
Total logic elements			448			
Total memory bits			0			
Embedded multiplier 9-bit elements			0			
Total cycle us	Total cycle used		50184			
		Flow Summary < <fiiter>> Flow Status Quartus Prime Version Revision Name Top-level Entity Name Family Device Timing Models Total logic elements Total registers Total pris Total virtual pins Total virtual pins Total PLLs Total PLLs</fiiter>	20.' ATC ATC Cyc EP4 Fin: 448 102 82 , 0	3 / 55,856 (< 1 %)		
		Descript	ion o	of your design		

In my design, the difficult point is about 'iaddr' signal control, I give several boundary conditions to decide the padding algorithm. In the convolution procedure, according to the homework description, construct a 2's complement method case by case to calculate the convolution layer kernel.

Next, another two stage "RDANDMAXPOOL" and "CEILANDSTR1" handle the reading operation from layer 0 memory and do the max-pooling operation and store

to layer 1 memory. Finally, when layer 1 memory is filled with value (use counter), "DONE" stage is active and pull down the "busy" signal to let testbench test the results.

Note: https://hackmd.io/@chiangkd/dic-2023-hw4

 $Scoring = (Total\ logic\ elements + Total\ memory\ bits + 9*Embedded\ multipliers\ 9-bit\ elements)\ X\ Total\ cycle\ used$

* Total logic elements must not exceed 1000.

Total logic elements	448	
Total memory bits	0	
Embedded multipliers 9-bit elements	0	
Total cycle used	50184	
Scoring	22482432	