2023 Digital IC Design Homework 1

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Functional Simulation Result

Stage 1	Pass	Stage 2	Pass	Stage 3	Pass	Stage 4	Pass

Stage 1

```
# -------------Stage 1 : Maximum selection with 4-input MMS-------------
#
# -------------Stage 1 :              Pass!                 -------------
```

Stage 2

```
# -------------Stage 2 : Minimum selection with 4-input MMS-------------
#
# -------------Stage 2 :              Pass!                 -------------
```

Stage 3

```
# -------------Stage 3 : Maximum selection with 8-input MMS-------------
#
# -------------Stage 3 :              Pass!                 -------------
```

Stage 4

```
# -------------Stage 4 : Minimum selection with 8-input MMS-------------
#
# -------------Stage 4 :              Pass!                 -------------
```

Description of your design

I simply write the code by intuition with homework description. In homework description, Table II provide the selection case of the multiplexer. Back to the code, I give a variable name `cmp` represent all the MUX output. So, in `MMS_4num.v`, there are three MUXs description with always block. Similar in `MMS_8num`, a MUX description with always block.