2023 Digital IC Design Homework 5

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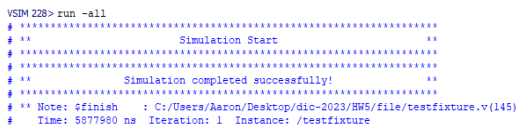
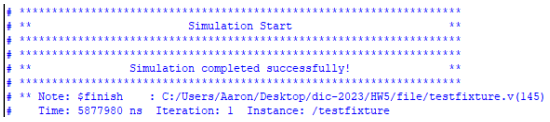
Simulation Result			
Functional simulation	Completed	Gate-level simulation	Completed





Evaluation Results			
test1.png	25.32	test2.png	24.82
test3.png	29.12	test4.png	20.95
test5.png	21.94	test6.png	25.21

Description of your design

In my design, I use four state to solve the problem. First of all, `WRITE_IN_RAW` store the `data_in` signal to memory, means that that are all raw data without demosaicing. And the other 3 states handle to fill in three color (RGB) memory with bilinear interpolation. In homework description, edge pixels will not be included in the PNSR evaluation for convenience. So, I decide to use a simple condition to change state. The condition for the end of filling up each memory can be no so rigorous because of the description. At `PAD_BLUE` stage, similarly use a condition of `data_idx` equals a specific value to pull up `done` signal and end the simulation.

Scoring = average PSNR of the six test images

*** PSNR of all interpolation results should meet at least the baseline.**