VLSI DSP Design 2018 Fall 期中考

NCHU Department of Electrical Engineering Total score 110

Part A. 簡答題 (38)

A1. What is the meaning of up sampling

A2. Pseudo inverse of a matrix A

A3. Coefficient update equation of LMS adaptive filters

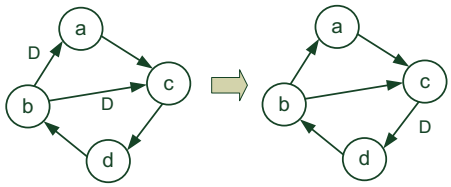
A4. L-slow delay in block processing of size L

A5. 2×2 Givens rotation matrix to convert $[4\ 3]^t$ to $[5\ 0]^t$

A6. What is decimation in frequency (DIF) in Fast Fourier Transform

A7. (8) Please draw the tree-structured analysis filter bank design for DWT with 3 octaves

A8. (6) please derive the node delay transfer values for each node in the DFG to achieve the retiming



Part B. 計算與設計題 (72)

B1. (10) Consider a direct form implementation of the FIR filter

$$y(n) = a_0x(n) + a_1x(n-1) + a_2x(n-2) + a_3x(n-3),$$

Assume that the time required for 1 multiply-add operation is $T=T_m+T_a$,.

a) draw a block filter architecture for a block size of 3

b) Pipeline this block filter such that the critical path delay is equal to T.

B2. (10) Consider the 4-tap FIR given in B1, please derive a transpose form block filter design for a block size of 2

Hint: Since two inputs are available every clock cycle, two multiply & add computations can be computed in each pipeline stage

B3. (12) consider the DFG shown in Fig. 1, assume addition and multiplication require 1 u.t. and 2 u.t., respectively

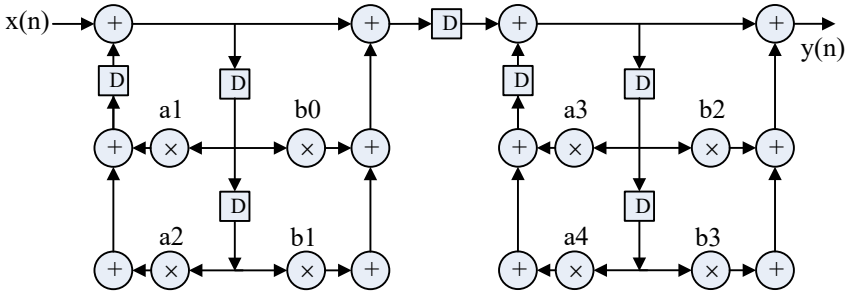


Fig. 1

a) what is the critical path of the design?

b) What is the iteration bound of the design?

c) Retime the design so that critical path equal to the iteration bound

VLSI DSP Design 2018 Fall 期中考

NCHU Department of Electrical Engineering Total score 110

B4. (12) For a 7-tap linear filter shown in Figure 2, assume the delays of multiplier and adder are T_m=5, T_a=1, respectively. Assume V_{dd} = 3V and V_t = 0.6V. Also assume the input capacitance relationship between multiplier and adder is $C_m = 5C_a$. If we divide the multiplier into 3 pipeline stages for power saving, and let T_{m1}=2, T_{m2}=2, T_{m3}=1, $C_{m1} = C_{m2} = 2C_a$, $C_{m3} = C_a$, after pipelining, please calculate

a) the voltage scaling factor β

b) the percentage of power saving

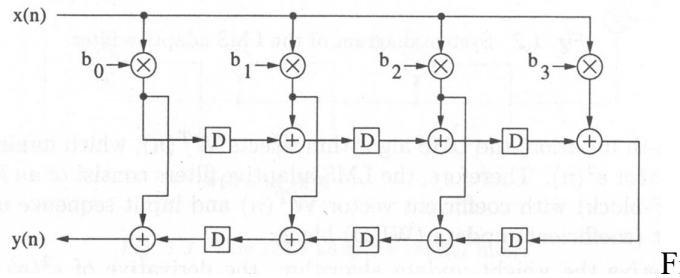


Fig 2.

B5. (16) For the DFG shown in Fig. 3, assume addition and multiplication require 1 u.t. and 3 u.t., respectively

a) please derive its transfer function

b) please derive its iteration bound

c) use the flow graph traversal scheme to derive its transpose form

d) use time scaling factor 2 and cut set retiming to reduce the critical path delay to 3 u.t.

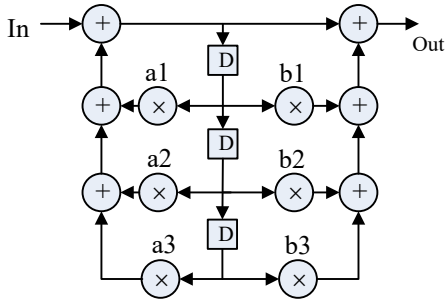


Fig. 3

B6. (12) Consider a 4-level pipelined all pass 8th order IIR digital filter shown in Fig 5. Assume multiplication and addition require 2 u.t. and 1 u.t., respectively.

a) calculate the iteration period bound of the filter

b) what is the critical path

c) apply cut set retiming to achieve a filter design with its critical path delay equal to 2u.t.

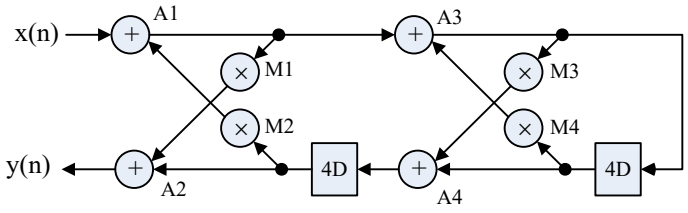


Fig. 5