VLSI DSP Design 2019 Fall 期中考範例

NCHU Department of Electrical Engineering

Part A. 簡答題 (38)

A1. What is the meaning of down sampling

A2. L-slow delay in block processing of size L

A3. 2×2 Givens rotation matrix to convert $[4\ -3]^t$ to $[5\ 0]^t$

A4. What is a Toeplitz matrix

A5. What is a dependence vector

Part B. 計算與設計題

B1. Consider a direct form implementation of the FIR filter

$$y(n) = a_0 x(n) + a_1 x(n-1) + a_2 x(n-2) + a_3 x(n-3),$$

Assume that the time required for multiply and add operation are T_m and T_a, respectively.

a) draw a block filter architecture for a block size of 3

b) what is the critical path delay of the design.

B2. Please draw the dependence graph of a matrix-vector multiplication $\mathbf{c}_{3\times1} = \mathbf{A}_{3\times3} \cdot \mathbf{b}_{3\times1}$

B3. consider the DFG shown in Fig. 1, assume addition and multiplication require 1 u.t. and 2 u.t., respectively

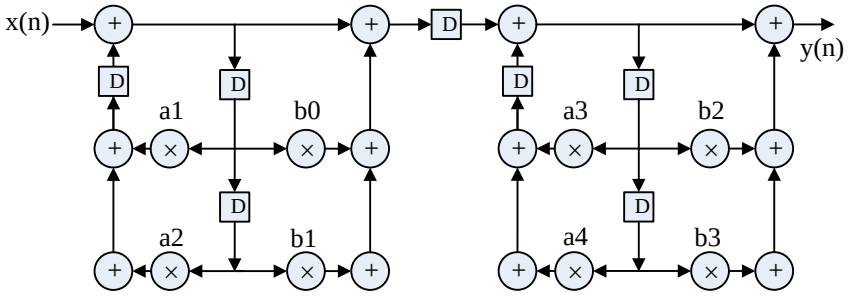

Fig. 1

a) what is the critical path of the design?

b) What is the iteration bound of the design?