Deliverable 2.2

Description of approach used for compact modelling of Fe-SBFET

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Name of researcher: Chiara Rossi
Name of supervisor: David Esseni

Department: DPIA – University of Udine

Summary

This report presents a compact model for SPICE-compatible simulations of ferroelectric-modulated Schottky junctions. The model has been coded in Verilog-A and verified using TCAD simulations. The compact model has been developed so that, by connecting it with a FET or FeFET compact model, it can be used to simulate ferroelectric Schottky barrier field effect transistors (Fe-SBFET) in a conventional architecture or ferroelectric-modulated diode (FMD) architecture. In particular, the compact model can be applied for the simulation of the Fe-SBFET used as artificial synapse. The model, given as an input the ferroelectric state, predicts the ferroelectric-modulated Schottky resistance. Thus, for offline trained neuromorphic chips, i.e. where optimal conductance of memory cells for a specific task is extracted externally and then transferred to the artificial synapses, the synaptic weights in the form of ferroelectric states can be directly passed to the compact models and kept fixed. For online training, i.e. training carried out directly in the neuromorphic chip, the synaptic weights are updated while learning. In this case, an additional compact model to simulate the ferroelectric switching kinetics should be connected to the ferroelectric-modulated Schottky resistance compact model presented here.
The Verilog-A code of the model can be found in open source, under the MIT license, on GitHub (https://github.com/chiara-rossi/CompactModel_P-modulated-Schottky-junction).

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1. Introduction

The compact model presented here focuses on the description of the ferroelectric polarization induced Schottky barrier modulation. In particular, it has been chosen to develop a compact model that simulates the polarization-dependent Schottky contact resistance, rather than a compact model for a *full* Fe-SBFET. The symbol of the compact model is reported in Fig. 1. As Fe-SBFETs can be fabricated in two different architectures, i.e. conventional, shown in Fig. 2, and ferroelectric-modulated diode (FMD), shown in Fig. 3, a compact model of the sole Schottky resistance is more flexible because it can be used for both architectures. It has to be noted that such a model describes only the Schottky contacts and thus it needs to be connected to a compact model of a FeFET[1] or FET in order to obtain a complete model for the conventional and FMD Fe-SBFET, respectively.

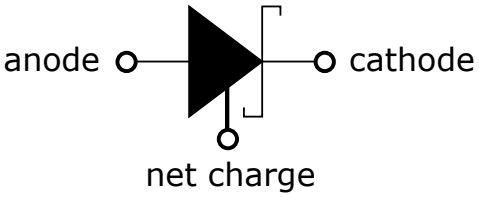

Fig. 1 – Symbol of the polarization-dependent Schottky contact resistance.

The compact model has been developed for the simulation of the Fe-SBFET used as artificial synapse, i.e. employed to store synaptic weights. In particular, the model simulates the ferroelectric-modulated Schottky resistance after a write pulse, thus for a known, previously set, ferroelectric state. Compact modelling of ferroelectric switching kinetics has already been addressed and some implementations can be found in literature[2]. Thus, the ferroelectric-modulated Schottky resistance compact model presented here needs as an input the net charge in the ferroelectric-dielectric stack placed above the Schottky contact, i.e. the ferroelectric polarization plus the trapped charge in the stack. In fact, previous experimental and simulation works have shown that ferroelectric-dielectric stacks, in particular HZO-SiO_2 stacks, are characterized by a large density of traps, with a concentration of about $\sim 10^{14}$ cm^{-2}, leading to a trapped charge comparable to the polarization charge[3]. Such trapped charges have a crucial role in the stabilization of the polarization, as they reduce the otherwise very large depolarization field in the ferroelectric layer[4]. The total net charge, i.e. the ferroelectric polarization compensated by the trapped charge, is in the range of some μC/cm.

[1] C.-T. Tung *et al.,* "A Compact Model of Ferroelectric Field-Effect Transistor", IEEE Electron Device Letters, vol. 43, n. 8, 2022, doi: 10.1109/LED.2022.3182141; J.-M. Sallese and V. Meyer, "The Ferroelectric MOSFET: A Self-Consistent Quasi-Static Model and its Implications" IEEE Transactions On Electron Devices, vol. 51, no. 12, 2004, doi: 10.1109/TED.2004.839113

[2] C. Peng *et al.,* "Nucleation-limited-switching based compact models for Hf-based ferroelectric devices and their applications in memory arrays", in 2025 14th International Conference on Modern Circuits and Systems Technologies (MOCAST), doi: 10.1109/MOCAST65744.2025.11083922; M. Lederer *et al.,* "SPICE compatible semi-empirical compact model for ferroelectric hysteresis", Solid-State Electronics, Vol. 199, 2023, doi: 10.1016/j.sse.2022.108501; https://cordis.europa.eu/project/id/871737/results/it

[3] K. Toprasertpong *et al.*, "Direct Observation of Interface Charge Behaviors in FeFET by Quasi-Static Split C-V and Hall Techniques: Revealing FeFET Operation," in 2019 IEEE International Electron Devices Meeting (IEDM), 2019, pp. 23.7.1– 23.7.4, doi:10.1109/IEDM19573.2019.8993664; S. Zhao, *et al.*, "Experimental Extraction and Simulation of Charge Trapping During Endurance of Fe- FET With TiN/HfZrO/SiO2/Si (MFIS) Gate Structure," IEEE Transactions on Electron Devices, vol. 69, no. 3, pp. 1561–1567, 2022, doi:10.1109/TED.2021.3139285; S. Deng, *et al.*, "Examination of the interplay between polarization switching and charge trapping in ferroelectric FET" in 2020 IEEE International Electron Devices Meeting (IEDM), 2020, pp. 4.4.1–4.4.4, doi:10.1109/IEDM13553.2020.9371999.

[4] Fontanini, *et al.*, "Modeling and Design of FTJs as Multi- Level Low Energy Memristors for Neuromorphic Computing," IEEE Journal of the Electron Devices Society, vol. 9, pp. 1202–1209, 2021, doi:10.1109/JEDS.2021.3120200

The maximum net charge depends on the minimum trapped charge needed to stabilize the ferroelectric polarization and, for a MFIS stack, it can be calculated with analytical expressions[5].

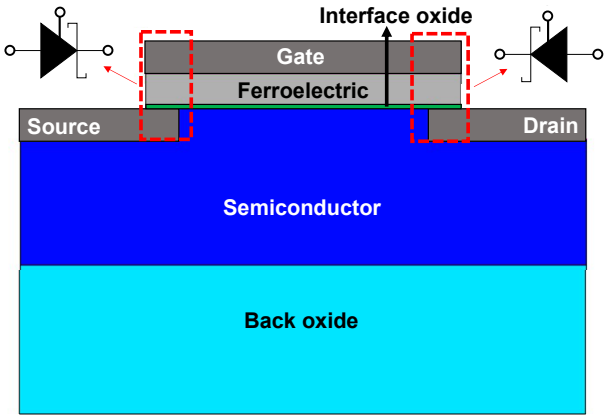

Fig. 2 – Conventional Fe-SBFET. The red rectangles indicate the Schottky diodes modulated by the ferroelectric polarization and described by the compact model.

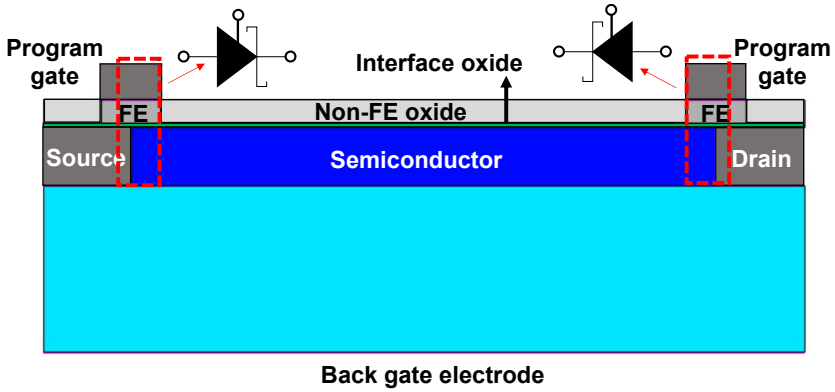

Fig. 3 - FMD Fe-SBFET. The red rectangles indicate the Schottky diodes modulated by the ferroelectric polarization and described by the compact model.

It has to be also noted that the model has been developed and tested for Schottky diodes featuring semiconductors with relatively low doping concentrations (10^{15} -10^{16} cm^{-3}), typically employed in Fe-SBFET. Thus, the usage of the model for Schottky contacts to semiconductors with higher doping will impact its accuracy.

The compact model has been implemented in Verilog-A language, which is a hardware description language and is the *de facto* standard language that the semiconductor industry uses for the implementation of compact models[6]. Verilog-A compact models can be simulated in the most popular SPICE circuit simulators.

[5] C. Rossi, D. Lizzit and D. Esseni, "Multilevel Operation in Scaled Back-End-of-Line Ferroelectric FETs With a Metal Interlayer," in IEEE Access, vol. 13, pp. 68525-68535, 2025, doi: 10.1109/ACCESS.2025.3561255
The paper above reports analytical expressions for a ferroelectric-metal interlayer-dielectric gate stack, however the same expressions can be used, as trapped charge at ferroelectric/dielectric interface are equivalent to the charge in the metal interlayer. In that work, we extracted a maximum net charge (positive and negative) of 3.8 $\mu C/cm^2$ and -3.9 $\mu C/cm^2$ for a MFMIS stack featuring 10 nm HZO layer and 5 nm SiO_2 layer and of 4.12 $\mu C/cm^2$ and -4.35 $\mu C/cm^2$ for a stack with the same HZO layer but 5 nm Al_2O_3 layer as dielectric. If we consider a 10 nm HZO layer and a 1 nm SiO_2 layer, the net charge increases to 5.26 and -6.01 $\mu C/cm^2$.

[6] C. C. McAndrew *et al.,* "Best Practices for Compact Modeling in Verilog-A," in IEEE Journal of the Electron Devices Society, vol. 3, no. 5, pp. 383-396, Sept. 2015, doi: 10.1109/JEDS.2015.2455342

The model has been run and tested using Cadence Spectre simulator[7].

2. Analytical model

The compact model is based on the analytical formulation of the field and thermionic-field emission is Schottky barriers by Padovani and Stratton[8]. The analytical expressions derived by Padovani and Stratton for the current due to field emission and thermionic-field emission describe a *regular* Schottky diode and have been also used to derive ohmic contact resistance in Schottky barriers for highly doped semiconductors. The detailed derivation of the model can be found in [7]. The Padovani-Stratton model has been here extended to model polarization-induced Schottky barrier modulation. In fact, the polarization-induced Schottky barrier modulation can be also interpreted as an electrostatic doping of the semiconductor at the Schottky junction due to the net charge in the ferroelectric-dielectric stack. In the Padovani-Stratton formulation, the doping concentration appears as a parameter. In our model, the doping is modified to a *net doping* that is equal to the impurity concentration plus an *equivalent electrostatic doping,* which is computed from the net charge (net compensated polarization given as an input to the compact model, as explained in the previous section). As a result, the Schottky diode current depends on the net charge.
The Padovani-Stratton model provides I-V relationships for field emission and thermionic-field emission in forward and reverse bias. Our compact model uses the analytical expressions for field emission and thermionic-field emission in reverse bias and for thermionic-field emission in forward bias. The expression for field emission in forward bias is not used as it is only relevant for highly doped semiconductor, which are not of interest in our model[9].
The current density due to thermionic-field emission in forward bias is expressed as[10]:

$$J_{TFE,F} = \frac{A^* T \sqrt{\pi E_{00,imp} q(\phi_{Bn} - \phi_n - V_F)}}{k \cosh\left(E_{00,imp}/kT\right)} \exp\left[-\frac{q\phi_n}{kT} - \frac{q(\phi_{Bn} - \phi_n)}{E_0}\right] \exp\left(\frac{qV_F}{E_0}\right)$$

where

$$E_{00} \equiv \frac{q\hbar}{2}\sqrt{\frac{N_{net}}{m^* \varepsilon_s}}$$

$$E_{00,imp} \equiv \frac{q\hbar}{2}\sqrt{\frac{N_{imp}}{m^* \varepsilon_s}}$$

$$E_0 \equiv E_{00} \coth\left(\frac{E_{00}}{kT}\right)$$

and A^* is the effective Richardson constant, computed as $A^* = 4\pi q m^* k^2/h^3$, where q is the electron charge, m^* is the electron effective mass, k is Boltzmann's constant, h is the Planck's constant ($\hbar$ is the reduced Planck constant). ϕ_{Bn} is the Schottky barrier to the semiconductor conduction band (difference between the metal work function and the electron affinity of the semiconductor), ϕ_n is the energy difference between the conduction band and the Fermi level and V_F is the diode forward voltage (V_R is the reverse voltage). T is the temperature, ε_s is the

[7] https://www.cadence.com/en_US/home/resources/datasheets/spectre-simulation-platform-ds.html
[8] F. A. Padovani and R. Stratton, "Field and thermionic-field emission in Schottky barriers", Solid-State Electronics, vol. 9, pp. 695-707, 1966, doi: 10.1016/0038-1101(66)90097-9
[9] The inclusion of the forward bias-field emission expression caused convergence problems in SPICE simulations. This issue has not been addressed as the use of such expression is out of the scope of this work.
[10] S. Sze, "Physics of Semiconductor Devices", New York: John Wiley & Sons, 2nd ed., 1981

semiconductor permittivity, N_{imp} is the impurity concentration, $N_{net} = N_{imp} + N_{el}$ is the *net doping* and N_{el} is the equivalent electrostatic doping, whose derivation will be detailed later.
The current density due to thermionic-field emission in reverse bias is expressed as[9]:

$$J_{TFE,R} = \frac{A^* T}{k}\sqrt{\pi E_{00} q\left[V_R + \frac{\phi_{Bn}}{\cosh^2(E_{00}/kT)}\right]}\exp\left(-\frac{q\phi_{Bn}}{E_0}\right)\exp\left(\frac{qV_R}{E_{00,kT}}\right)$$

where

$$E_{00,kT} \equiv \frac{E_{00,imp}}{\left(\frac{E_{00,imp}}{kT}\right) - \tanh\left(\frac{E_{00,imp}}{kT}\right)}$$

The current density due to field emission in reverse bias is expressed as[9]:

$$J_{FE,R} = A^*\left(\frac{E_{00}}{k}\right)^2\left(\frac{\phi_{Bn} + V_R}{\phi_{Bn}}\right)\exp\left(-\frac{2q\phi_{Bn}^{3/2}}{3E_{00}\sqrt{\phi_{Bn} + V_R}}\right)$$

The total current is thus computed as:

$$I_{tot} = A * (J_{TFE,F} - J_{TFE,R} - J_{FE,R})$$

where A is the Schottky junction area.
For $kT \gg E_{00}$, thermionic emission dominates, whereas when $kT \ll E_{00}$, tunneling dominates[10]. To avoid convergence issues in SPICE simulations, the thermionic-field emission current in reverse bias is computed with the above formula only for $E_{00} \leq kT$ (the implementation is done with an if-statement).
The above expressions are valid for electrons (they have been derived for majority carriers in n-type semiconductors). Similar expressions are used to describe field and thermionic-field emission currents due to holes. The Schottky barrier to valence band is computed as $\phi_{Bp} = E_g - \phi_{Bn}$, where E_g is the semiconductor band gap.
Our compact model for the ferroelectric-modulated Schottky resistance consists of two submodels: one for electrons and one for holes. The two submodels should be connected in parallel to obtain the complete model (as their current should be summed). A positive net charge in the ferroelectric-dielectric stack results in an enhanced tunneling of electrons (n-type branch of a Fe-SBFET), whereas a negative net charge results in an enhanced tunneling of holes (p-type branch of a Fe-SBFET). Thus, in the *electron submodel,* N_{el} (the equivalent electrostatic doping) is different from zero only when the net charge (Q_n) is positive. On the other hand, in the *hole submodel,* N_{el} is different from zero only for negative net charge.
In the *electron submodel,* for positive net charge, N_{el} is given by:

$$N_{el} = \frac{Q_n}{q\ t_s} f_{Q,n} * Q_n^{fe,n}$$

And in the *hole submodel,* for negative net charge, N_{el} is given by:

$$N_{el} = \frac{Q_n}{q\ t_s} f_{Q,p} * Q_n^{fe,p}$$

where $f_{Q,n}$, $f_{Q,p}$, $f_{e,n}$, $f_{e,p}$ are fitting parameters and t_s is the semiconductor thickness in case of a FMD FeSBFET, whereas is an additional fitting parameter for the conventional Fe-SBFET. It has to be noted that, except for these fitting parameters related to the equivalent electrostatic doping, the other parameters present in the model are physical parameters.

The net charge Q_n is not a simple parameter of the compact model: its value is given as an input through a third electrode ("net charge" in Fig. 1). This third pin, in fact, is only used to pass the value of the net charge to the model, thanks to the definition of an *equivalent voltage* V (net charge), i.e. the voltage at the "net charge" electrode, which is equal to the net charge expressed in C/cm^2. In the compact model implementation, the "net charge" electrode is not connected to any branch, namely there is no expression linking the net charge Q_n to any current flow, so the "net charge" electrode behaves like an open circuit node. Thanks to this implementation, the net charge can be computed with other compact models (described above) and directly connected to this ferroelectric-modulated Schottky resistance compact model. Moreover, the net charge can be more easily handled in circuit simulations compared to an approach where the net charge is an internal parameter of the compact model.

3. Verilog-A implementation

The compact model, based on the analytical equations presented in the previous section, has been coded in Verilog-A. As described in the previous section, the model is composed by two sub-models, one that simulates the n-type branch of a Fe-SBFET and one that simulates the p-type branch of a Fe-SBFET, according to the net charge stored in the control gate ferroelectric-dielectric stack. The Verilog-A codes of the sub-models are reported in the following paragraphs.

3.1 Verilog-A code of Schottky Gated diode - n-type branch

```
`include "constants.h"
`include "disciplines.vams"

(*compact_module*)
module SchGDiode_e_v2(cathode,anode,netcharge);
inout      cathode,anode,netcharge;
electrical cathode,anode,netcharge;

//Technology parameters
parameter real  A=20e-11;        //[cm^2]     Diode Area
parameter real  SBH_n=0.6;       //[eV] Schottky Barrier Height for electrons
parameter real  A_re_n=110;      //[A/(cm^2K^2)]   reduced   effective   Richardson
constant for electrons
parameter real  N=1e15;          //[cm^-3] doping concentration
parameter real  Nc=3.2e19;       //[cm^-3]  Effective  conduction  band  density  of
states
parameter real  m_0=9.11e-31;    //[kg] m0 free electron mass
parameter real  m_eff=0.2;       //[] prefactor that multiplies m0 to obtain the
effective mass
parameter real  eps_s =11.7;     //[] semiconductor dielectric constant
parameter real  fQ =1.5e2;       //fitting factor used for equivalent electrostatic
doping
parameter real  fe =0.5;         //fitting factor used for equivalent electrostatic
doping

//Internal Parameters
real     E_00,E_00_dop,E_0,E_0_dop,E_00_KT,Nel;
real  phi_n,N_m3;
real  eps,A_re_n_t;
```

```
real  K,KT;
real  m_star,h_bar,c1;
real  J_FE_R,J_TFE_F,J_TFE_R,Jtot;
real  f0,f1,f2,f3,f4;
real  Qs, Ntot;

analog begin
      @(initial_step) begin
            f0=1;        //Debug multipliers
            f1=1;
            f2=1;
            f3=1;
      end
//*******************************************************//
//     Equivalent electrostatic doping                   //
//*******************************************************//
      if (V(netcharge)>=0) begin
      Qs=V(netcharge)/(`P_Q*20e-7); //[cm^-3] -> V(netcharge) in C/cm2
      Nel=Qs*fQ*pow(V(netcharge),fe);
      end else begin
      Nel=0;
      end
      Ntot=N+Nel;   //[cm^-3]

//*******************************************************//
//     Parameters                                        //
//*******************************************************//
      h_bar=`P_H/(2*`M_PI*`P_Q);//[eV s]
      eps=eps_s*`P_EPS0;        // [farads/meter]
      N_m3=Ntot*1e6;                  // [m^-3]
      m_star=m_0*m_eff;         //[kg]
      K=`P_K/(`P_Q);
      E_00=(`P_Q*h_bar/2)*sqrt(N_m3/(m_star*eps));
      E_00_dop=(`P_Q*h_bar/2)*sqrt(N*1e6/(m_star*eps));
      E_0=E_00*cosh(E_00/(K*$temperature))/sinh(E_00/(K*$temperature));
      J_FE_R=0;
      J_TFE_F=0;
      J_TFE_R=0;
      phi_n=-K*$temperature*ln(Nc/N);
      KT=K*$temperature;
      A_re_n_t=4*`M_PI*`P_Q*m_star*pow(`P_K,2)/(pow(`P_H,3))*1e-4;
//[A/(cm^2K^2)]

//*******************************************************//
// Thermionic-Field emission current (forward bias)     //
//*******************************************************//
      J_TFE_F=f1*A_re_n*$temperature*sqrt(`M_PI*E_00_dop*(SBH_n-phi_n-
V(anode,cathode)))/(K*cosh(E_00_dop/(K*$temperature)))*limexp(-
phi_n/(K*$temperature)-(SBH_n-phi_n)/E_0)*limexp(V(anode,cathode)/E_0);

//*******************************************************//
// Field emission current (reverse bias)                //
//*******************************************************//
      J_FE_R=f2*A_re_n_t*pow((E_00/K),2)*((SBH_n+V(cathode,anode))/SBH_n)*limexp(
-(2*pow(SBH_n,(3/2)))/(3*E_00*sqrt(SBH_n+V(cathode,anode))));
//*******************************************************//
// Thermionic-Field emission current (reverse bias)     //
```

```
//*******************************************************//
      E_00_KT=E_00_dop/((E_00_dop/(K*$temperature))-
tanh(E_00_dop/(K*$temperature)));
      if (E_00<=KT) begin
      J_TFE_R=f3*A_re_n*$temperature/K*sqrt(`M_PI*E_00*(V(cathode,anode)+SBH_n/(p
ow(cosh(E_00/(K*$temperature)),2))))*limexp(-
SBH_n/E_0)*limexp(V(cathode,anode)/E_00_KT);
      end else begin
      J_TFE_R=0;
      end

//*******************************************************//
// Total current                                         //
//*******************************************************//
      Jtot=(-J_FE_R+J_TFE_F-J_TFE_R);
      I(anode,cathode) <+ A*Jtot;

      //Maximum current density 1mA/um2
      if (abs(I(cathode,anode)/(A*1e12))>=1e-3) begin
            $strobe("**FAILURE DETECTED** %M limit current exceeded!");
      end
end
endmodule
```

3.2 Verilog-A code of Schottky Gated diode - p-type branch

```
`include "constants.h"
`include "disciplines.vams"

(*compact_module*)
module SchGDiode_h_v2(cathode,anode,netcharge);
inout      cathode,anode,netcharge;
electrical cathode,anode,netcharge;

//Technology parameters
parameter real  A=20e-11;        //[cm^2]     Diode Area
parameter real  SBH_n=0.6;       //[eV] Schottky Barrier Height for electron
parameter real  Eg=1.12;         //[eV] semiconductor band gap
parameter real  A_re_p=30;       //[A/(cm^2K^2)]   reduced   effective   Richardson
constant for holes
parameter real  N=1e15;          //[cm^-3] doping concentration
parameter real  Nv=1.8e19;       //[cm^-3] Effective valence band density of states
parameter real  m_0=9.11e-31;    //[kg] m0 free electron mass
parameter real  m_eff=0.6;//[] prefactor that multiplies m0 to obtain the effective
mass
parameter real  eps_s =11.7;     //[] semiconductor dielectric constant
parameter real  fQ =1e3;         //fitting factor used for equivalent electrostatic
doping
parameter real  fe =0.6;         //fitting factor used for equivalent electrostatic
doping

//Internal Parameters
real  E_00,E_00_dop,E_0,E_00_KT;              //
real  phi_p,SBH_p,N_m3;                 //
real  eps,A_re_p_t;              //
real  K,KT;               //
```

```
real  m_star,h_bar,c1;                  //
real  J_FE_R,J_TFE_F,J_TFE_R,Jtot;      //
real  f0,f1,f2,f3,f4;
real  Qs, Nel, Ntot;

analog begin
      @(initial_step) begin
            f0=1;        //Debug multipliers
            f1=1;
            f2=1;
            f3=1;
      end

//*****************************************************//
//     Equivalent electrostatic doping                 //
//*****************************************************//
      if (V(netcharge)<=0) begin
      Qs=-V(netcharge)/(`P_Q*20e-7);   //[cm^-3] -> V(netcharge) in C/cm2
      Nel=Qs*fQ*pow(-V(netcharge),fe);
      end else begin
      Nel=0;
      end
      Ntot=N+Nel;   //[cm^-3]

//*****************************************************//
//     Parameters                                      //
//*****************************************************//
      SBH_p=Eg-SBH_n;                   //[eV] Schottky Barrier Height for electron
      h_bar=`P_H/(2*`M_PI*`P_Q);        //[eV s]
      eps=eps_s*`P_EPS0;                // [farads/meter]
      N_m3=Ntot*1e6;                    // [m^-3]
      m_star=m_0*m_eff;                 //[kg]
      K=`P_K/(`P_Q);
      E_00=(`P_Q*h_bar/2)*sqrt(N_m3/(m_star*eps));
      E_00_dop=(`P_Q*h_bar/2)*sqrt(N*1e6/(m_star*eps));
      E_0=E_00*cosh(E_00/(K*$temperature))/sinh(E_00/(K*$temperature));
      J_FE_R=0;
      J_TFE_F=0;
      J_TFE_R=0;
      phi_p=-K*$temperature*ln(Nv/N);
      KT=K*$temperature;
      A_re_p_t=4*`M_PI*`P_Q*m_star*pow(`P_K,2)/(pow(`P_H,3))*1e-4;
//[A/(cm^2K^2)]

//*****************************************************//
// Thermionic-Field emission current (forward bias)    //
//*****************************************************//
      J_TFE_F=f1*A_re_p*$temperature*sqrt(`M_PI*E_00_dop*(SBH_p-phi_p-
V(anode,cathode)))/(K*cosh(E_00_dop/(K*$temperature)))*limexp(-
phi_p/(K*$temperature)-(SBH_p-phi_p)/E_0)*limexp(V(anode,cathode)/E_0);

//*****************************************************//
// Field emission current (reverse bias)               //
//*****************************************************//
      J_FE_R=f1*A_re_p_t*pow((E_00/K),2)*((SBH_p+V(cathode,anode))/SBH_p)*limexp(
-(2*pow(SBH_p,(3/2)))/(3*E_00*sqrt(SBH_p+V(cathode,anode))));
```

```
//*******************************************************//
// Thermionic-Field emission current (reverse bias)     //
//*******************************************************//
       E_00_KT=E_00_dop/((E_00_dop/(K*$temperature))-
tanh(E_00_dop/(K*$temperature)));
       if (E_00<=KT) begin
       J_TFE_R=f3*A_re_p*$temperature/K*sqrt(`M_PI*E_00*(V(cathode,anode)+SBH_p/(p
ow(cosh(E_00/(K*$temperature)),2))))*limexp(-
SBH_p/E_0)*limexp(V(cathode,anode)/E_00_KT);
       end else begin
       J_TFE_R=0;
       end

//*******************************************************//
// Total current                                        //
//*******************************************************//
       Jtot=(-J_FE_R+J_TFE_F-J_TFE_R);
       I(anode,cathode) <+ A*Jtot;

       //Maximum current density 1mA/um2
       if (abs(I(cathode,anode)/(A*1e12))>=1e-3) begin
              $strobe("**FAILURE DETECTED** %M limit current exceeded!");
       end
end
endmodule
```

4. Verification by TCAD simulations

The compact model has been verified by comparisons to TCAD simulations, carried out by using Synopsys Sentaurus TCAD[11].
First, a simple Schottky diode, with zero net charge, is simulated. The structure we consider is a simple silicon slab with an n-type doping concentration of 10^{15} cm^{-3} (with an area of 1 µm x 1 µm and a length of 0.5 µm) contacted by two electrodes, featuring an Ohmic contact at one electrode and a Schottky contact at the second electrode. We considered a silicon-aluminum junction for the Schottky electrode, corresponding to a Schottky barrier of 0.6 eV, as we have

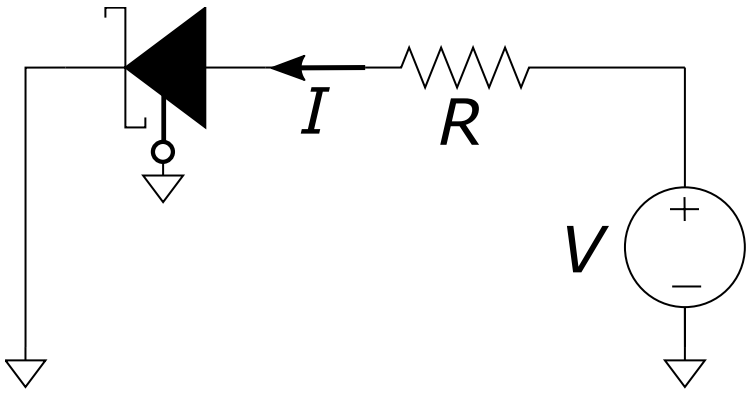

Fig. 4 – Circuit for SPICE simulation of a simple Schottky diode (zero net charge).

[11] Sentaurus Device of Synopsys TCAD, User Guide, V-2023.12

extracted in a previous work[12]. We have simulated such structure in TCAD Sentaurus. More details about the performed TCAD simulations are reported here: 10.5281/zenodo.17236834[13]. Then, we have constructed an equivalent circuit for SPICE simulation of such simple structure, which is sketched in Fig. 4. The structure features the Schottky junction compact model (n-type branch), a resistor and a voltage source. The circuit has been simulated using Spectre circuit simulator. We have set the compact model parameters to the same values as the TCAD model parameters. In this case, in fact, as the net charge is zero, the fitting parameters did not have an effect. All the other compact model parameters have a physical meaning and are also parameters for the TCAD simulations. The resistance in the circuit is the resistance of the silicon slab, computed from silicon resistivity value for a phosphorus doping of 10^{15} cm^{-3}.

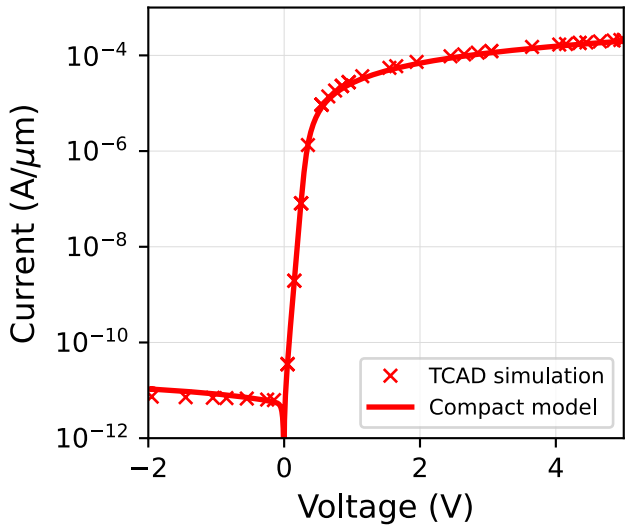

Fig. 5 – Current vs voltage characteristic of the Schottky diode simulated with the compact model (equivalent circuit in Fig. 4: the current reported here is indicated with *I* and the voltage with *V*) compared to TCAD simulations.

The current-voltage characteristics of the Schottky diode simulated with the compact model is compared to TCAD simulations in Fig. 5. The results obtained with the compact model agrees very well with TCAD results. A slight deviation is found for the reverse current: the compact model predicts a higher value with respect to TCAD simulations.
Next, we have simulated two back-to-back Schottky diodes: in Fe-SBFETs, in fact, the source and drain metallic contact to the semiconductor gives rise to such a configuration. The equivalent circuit for SPICE simulations with compact models is reported in Fig. 6. For any voltage *V* applied through the voltage source, one of the two Schottky diode is in reverse bias. In TCAD simulations, a silicon slab with an area of 1 µm x 1 µm and a length of 10 µm has been simulated. In this case, the two electrodes contacting the semiconductor are both Schottky contacts, with a barrier height of 0.6 eV. Simulations have been performed for n-type doping

[12] 10.5281/zenodo.17236834; D. Nazzari *et al.*, "Non-Volatile Reconfigurable Transistor via Ferroelectric Modulation: Fabrication Strategy and TCAD Simulations," *2025 International Semiconductor Conference (CAS)*, Sinaia, Romania, 2025, pp. 3-11, doi: 10.1109/CAS66707.2025.11222346
[13] The document in 10.5281/zenodo.17236834 reports about TCAD simulations of more complex devices, including SBFET, however the main information, models, physical parameters apply also for TCAD simulations reported here for simpler devices.

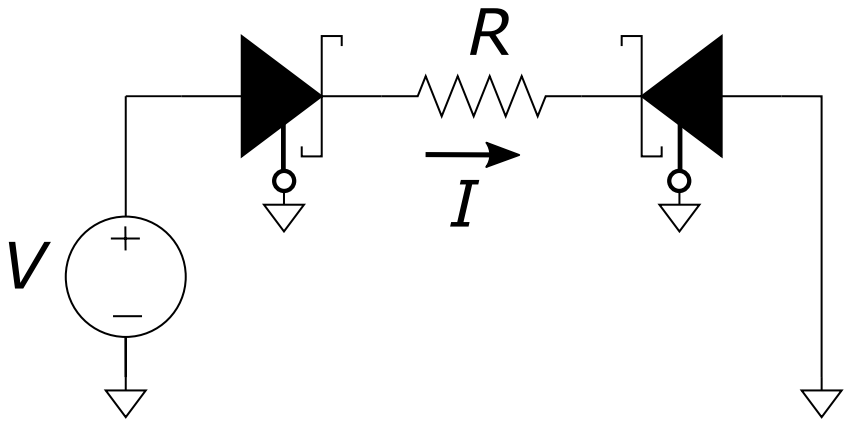

Fig. 6 – Circuit for SPICE simulation of two back-to-back Schottky diode (zero net charge).

concentrations of 10^{15} cm^{-3} and 10^{16} cm^{-3}. The resistance value *R* has been changed according to the resistivity value for the corresponding doping. Higher doping concentrations for the semiconductor are out of the scope of this work. Simulation results, using TCAD and the compact model, are reported in Fig. 8 and Fig. 7, for a doping concentrations of 10^{15} cm^{-3} and of 10^{16} cm^{-3}, respectively. A good fit to TCAD simulations could be obtained with the compact model. The main deviation from TCAD results is for negative voltages, where compact model results overestimate the current.

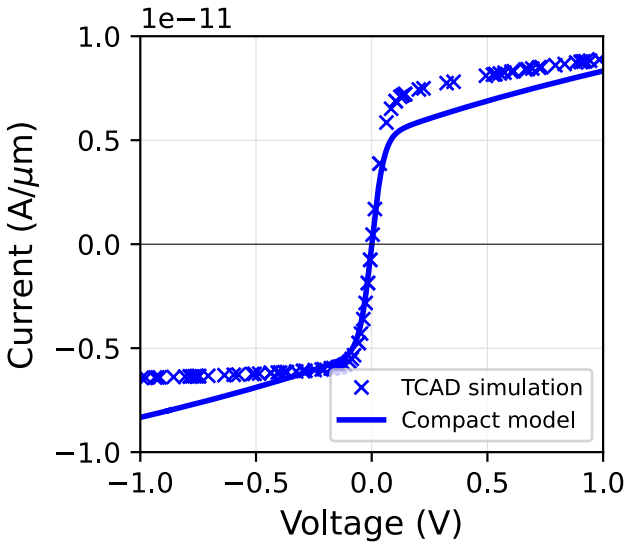

Fig. 8 - Current vs voltage characteristic of two back-to-back Schottky diodes, silicon doping of 10^{15} cm^{-3}, simulated with the compact model (equivalent circuit in Fig. 6: the current reported here is indicated with *I* and the voltage with *V*) compared to TCAD simulations.

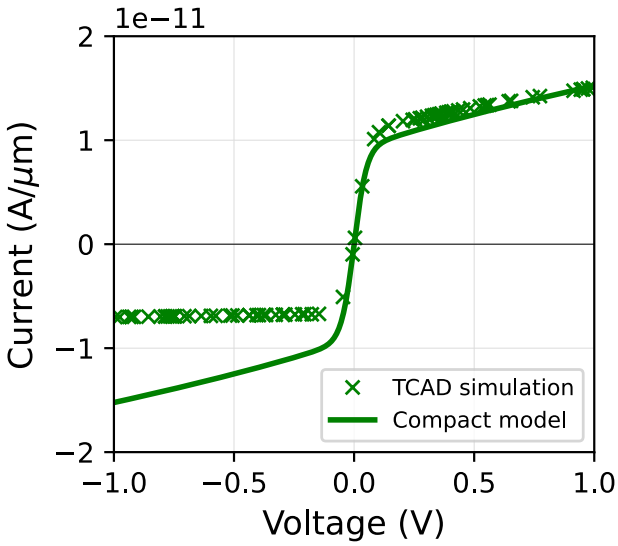

Fig. 7 - Current vs voltage characteristic of two back-to-back Schottky diodes, silicon doping of 10^{16} cm^{-3}, simulated with the compact model (equivalent circuit in Fig. 6: the current reported here is indicated with *I* and the voltage with *V*) compared to TCAD simulations.

Then, we have addressed the verification of the compact model using a non-zero net charge. A similar circuit with two back-to-back Schottky diodes connected by a resistance has been used also in this case. We decided not to use a FET or FeFET model connecting the two Schottky junctions. Even though with a FET or FeFET model we would have obtained a circuit more

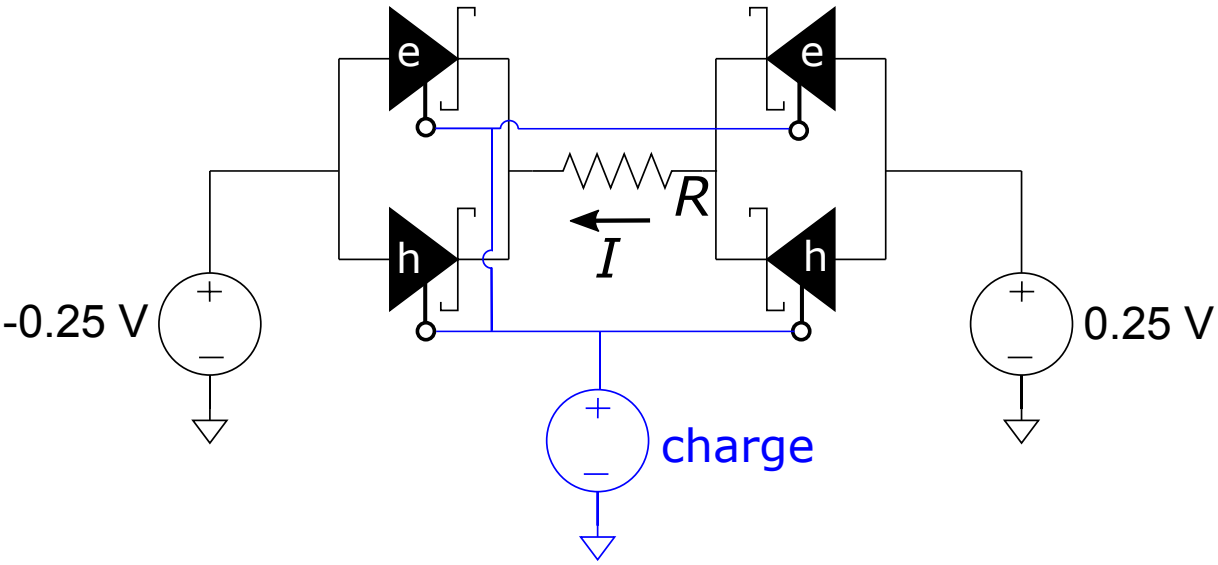

Fig. 9 - Circuit for SPICE simulation of two back-to-back Schottky diode with non-zero net charge. The letters e and h in the Schottky diode symbol refer to the electron submodel (n-type branch) and hole submodel (p-type branch), respectively.

similar to the one that should be used to model a complete Fe-SBFET, the insertion of such FET/FeFET models would have required an additional fitting of the FET/FeFET-compact model parameters to TCAD simulations. To avoid the inclusion of additional fitting parameters, we decided to simplify the structure to be simulated in order to keep the focus on the validation of the polarization-dependent Schottky resistance. The simulated equivalent circuit is shown in Fig. 9. The resistance is set to 40 kΩ. As we have a non-zero net charge, we should use the full model composed by the electron submodel and hole submodel connected in parallel, as it can be seen in Fig. 9. The net charge electrodes of the four submodels are connected to the same voltage source that gives the value of the net charge. In SPICE simulations the bias voltages have been kept constant and the *charge* voltage source value has been swept from -10 μC/cm^2 to 10 μC/cm^2, an interval which includes typical values for the net charge in Fe-SBFET, as explained in the introduction section. TCAD simulations have been performed with a mixed-mode approach: the two gated Schottky junctions have been simulated with numerical simulations but have been interconnected with an external resistor of 40 kΩ. The gated junctions, sketched in Fig. 10, are composed by a silicon layer (thickness of 20 nm and width of 1 μm) with a Schottky junction (barrier height of 0.6 eV) placed below an oxide layer contacted by an electrode, where a charge is specified instead of a voltage. Finally, an Ohmic electrode contact the other side of the silicon layer: this electrode is connected to the external resistor.

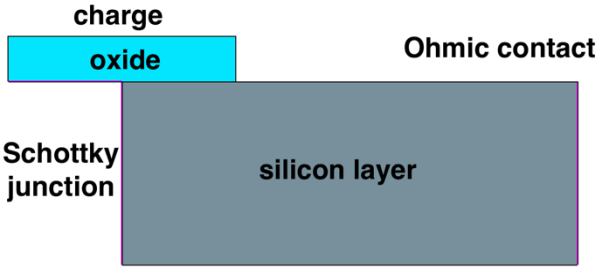

Fig. 10 – Gated polarization-modulated Schottky junction simulated in TCAD.

The results obtained with the compact model are compared to TCAD simulations in Fig. 11. The fitting parameters $f_{Q,n}$, $f_{Q,p}$, $f_{e,n}$, $f_{e,p}$ for the equivalent electrostatic doping have been calibrated in order to get a good agreement between compact model and TCAD simulations.

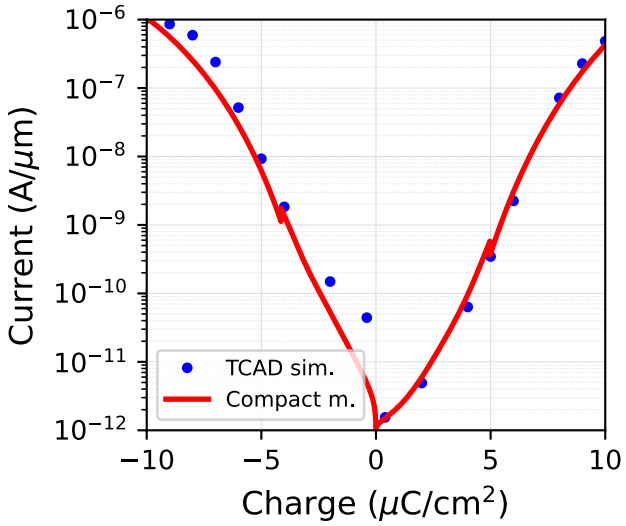

Fig. 11 – Current (*I* in Fig. 9) versus net charge simulated with compact model (line) and TCAD (symbols). The SPICE circuit for the simulation of compact model is shown in Fig. 9. The electrons tunneling mass is $0.3m_0$, the holes tunneling mass is $0.2m_0$.

The parameter t_s has been set to 20 nm, i.e. the silicon thickness. The TCAD parameters and model used for simulations in Fig. 11 are described in details in previous works[12], as mentioned above. In particular, the electrons tunneling mass has been set to 0.3m$_0$ and the holes tunneling mass has been set to 0.2m$_0$ in both TCAD and compact models. The fitting parameters used in Fig. 11 are: $f_{Q,n}$ = 190, $f_{Q,p}$ =14, $f_{e,n}$ =0.5, $f_{e,p}$ =0.3. Using these parameters, the compact model gives a quite good match to TCAD data, with a small deviation for negative net charge below -2 μC/cm^2, where the compact model underestimates the current. The small discontinuities in the curve of the compact model results, at about -5 μC/cm^2 and 5 μC/cm^2, are due to the if-statements used to enable or disable the computation of the thermionic-field emission current. This discontinuity does not affect convergence of SPICE simulations because the if-statement depends on the net charge and doping levels, but it does not depend on quantities like voltages and currents. The two sub-branches created by the if-statement refer to

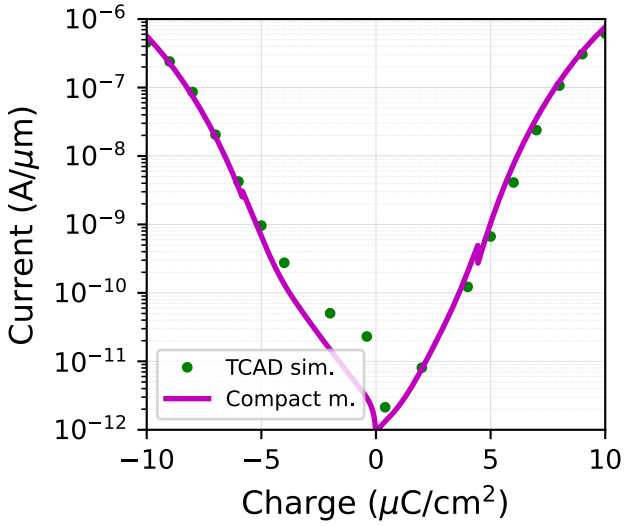

Fig. 12 - Current (*I* in Fig. 9) versus net charge simulated with compact model (line) and TCAD (symbols). The SPICE circuit for the simulation of compact model is shown in Fig. 9. The electrons tunneling mass is $0.2m_0$, the holes tunneling mass is $0.6m_0$.

different physical states of the device, which cannot coexist in a single SPICE simulation at a fixed charge/doping/temperature. Finally, simulations are performed also for different tunneling masses values, namely $0.2m_0$ for electrons and $0.6m_0$ for holes, in order to validate the model also in different conditions. The results are shown in Fig. 12. The fitting parameters are: $f_{Q,n} = 150$, $f_{Q,p} = 1100$, $f_{e,n} = 0.5$, $f_{e,p} = 0.6$. Also in this case, a good fit to TCAD data could be obtained, with a slight deviation for small values of negative net charge.

5. SPICE simulations of a FMD-FeSBFET

The compact model has been used to simulate a FMD-FeSBFET by interconnecting the ferroelectric-modulated Schottky resistance compact models to a FET model. Here, a MOS level 3 has been used for simplicity. The full circuits for the simulation of a FeSBFET employing n-type and p-type semiconductor are reported in Fig. 13 and Fig. 14, respectively. The circuits have been simulated in SPICE to obtain drain current-gate voltage characteristics, varying the net charge. The simulation results of the FMD-FeSBFETs transfer characteristics for different net charges are plotted in Fig. 15 and Fig. 16. The simulated transfer characteristics show the expected characteristics, as found in experiments, considering a single n-type or p-type branch. As a conventional FET model has been used, the ambipolar behaviour of the FeSBFET is not simulated. The absence of ambipolar behaviour is not detrimental for the employment of the compact model for simulation of artificial synapses, as usually only one branch is employed (the two branches provide the same levels of current, thus no additional conductance levels can be obtained by exploiting the ambipolar behaviour). However, if such behaviour should be modelled, the simple FET compact model can be changed to a more complex model that can simulate the ambipolar behaviour of a SBFET.

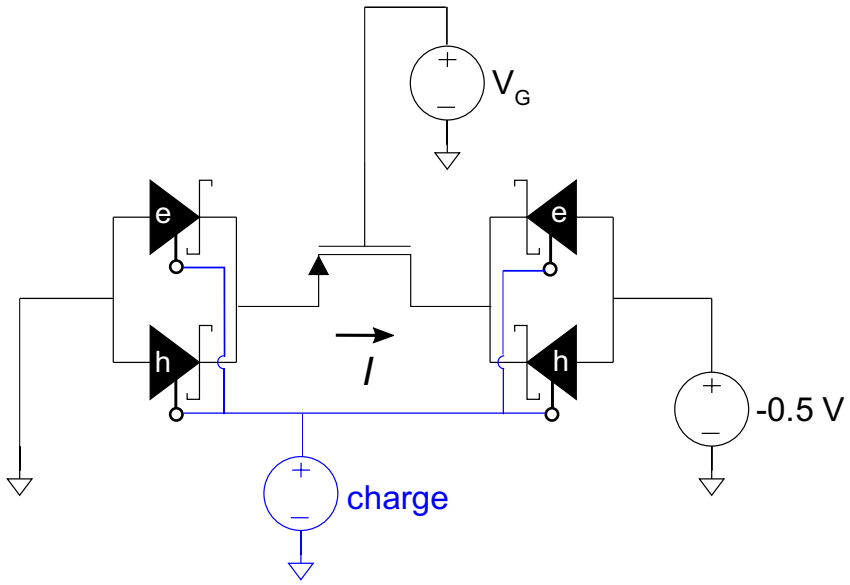

Fig. 13 - Circuit for SPICE simulation of a FMD-FeSBFET (n-type semiconductor). The letters e and h in the Schottky diode symbol refer to the electron submodel (n-type branch) and hole submodel (p-type branch), respectively.s

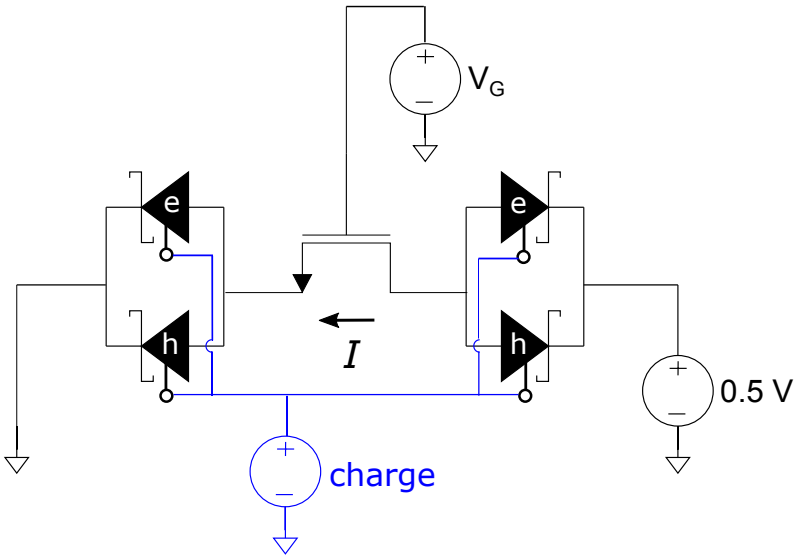

Fig. 14 - Circuit for SPICE simulation of a FMD-FeSBFET (p-type semiconductor). The letters e and h in the Schottky diode symbol refer to the electron submodel (n-type branch) and hole submodel (p-type branch), respectively.

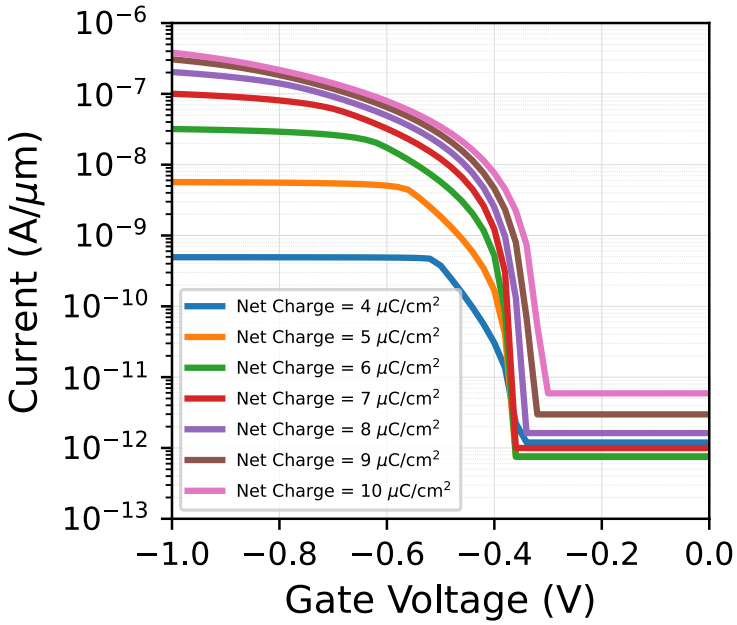

Fig. 15 – Transfer characteristics of the FMD-FeSBFET (p-type semiconductor) simulated with the compact model using the equivalent circuit in Fig. 13 (Current is I and gate voltage is V_G in Fig. 13). The electrons tunneling mass is 0.3 m_0 and the holes tunneling mass is 0.2m_0.

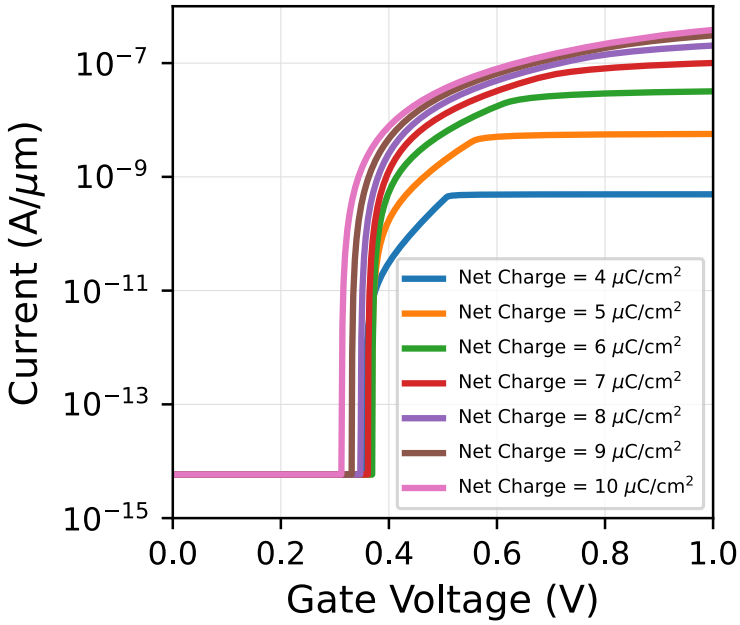

Fig. 16 - Transfer characteristics of the FMD-FeSBFET (p-type semiconductor) simulated with the compact model using the equivalent circuit in Fig. 14 (Current is I and gate voltage is V_G in Fig. 14). The electrons tunneling mass is 0.3 m_0 and the holes tunneling mass is 0.2m_0.

Conclusion

We have reported about the ferroelectric-modulated Schottky resistance compact model developed during the EASIFeT project. We have detailed the analytical equations used and presented the Verilog-A implementation of the compact model. The verification of the model has been carried out using TCAD Sentaurus simulations. We have shown how this model can be employed to simulate the Schottky barrier modulation by ferroelectric polarization in a Fe-SBFET. The Verilog-A code and the netlist, dataset and further information about the test cases presented here can be found on GitHub: https://github.com/chiara-rossi/CompactModel_P-modulated-Schottky-junction.