



Twocryst Fiber Tracker (TFT) Status

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CERN BE-ABP-NDC

17/10/2024

TWOCRIST detectors

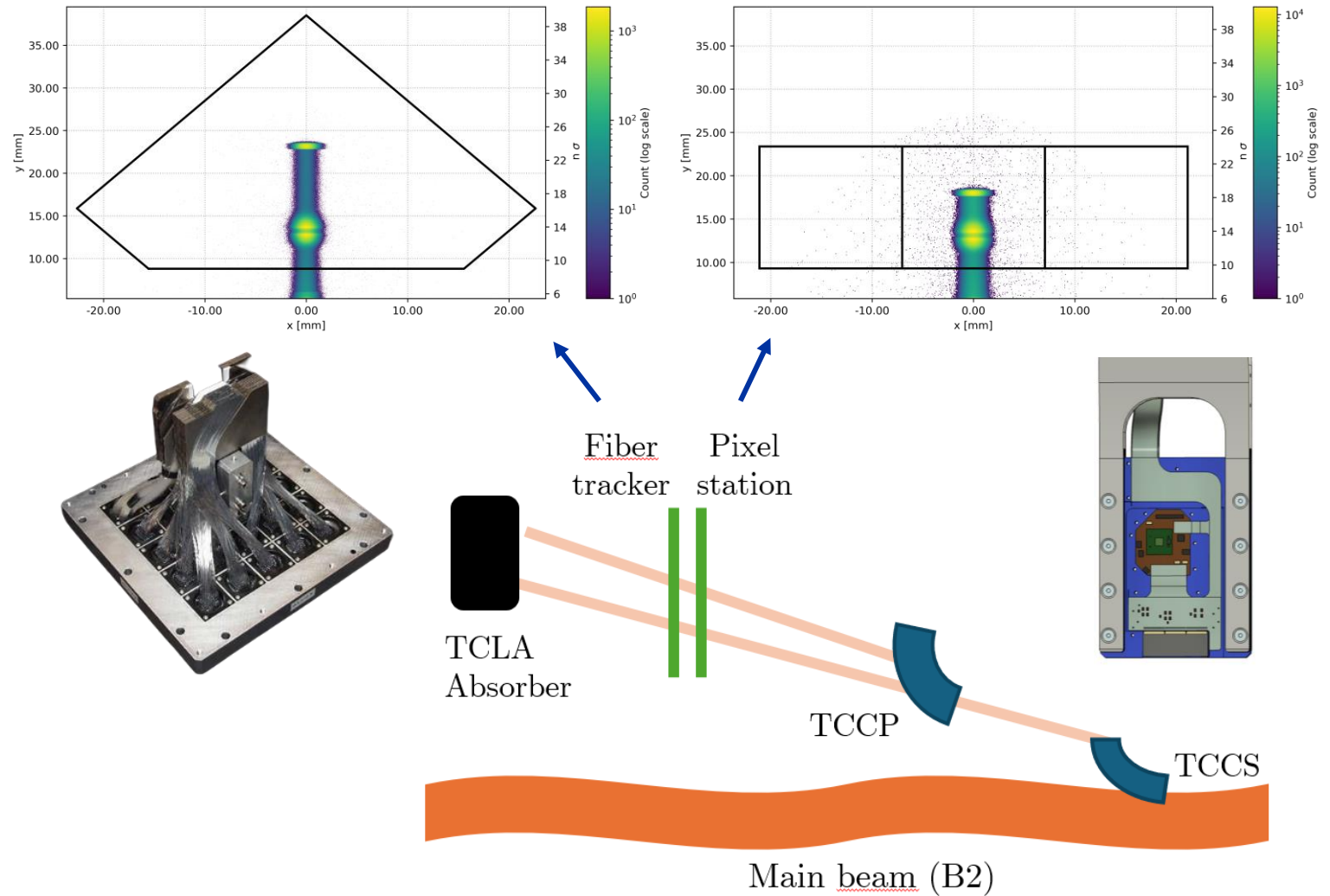
Pixel Detector

→ currently under beam test
(16 - 31 October)

Fiber Tracker (TFT)

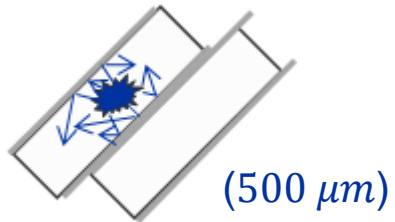
former ATLAS-ALFA detector
(uninstalled in Nov 2023)

→ needs to be tested and adapted
to TWOCRIST purposes

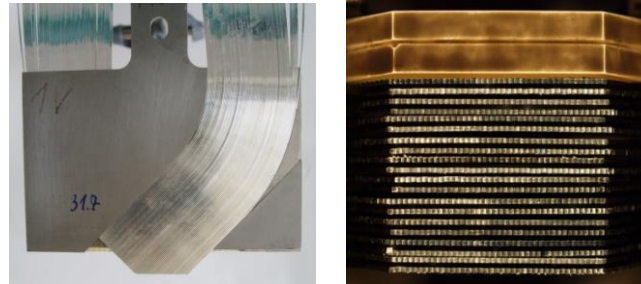


TFT Detector

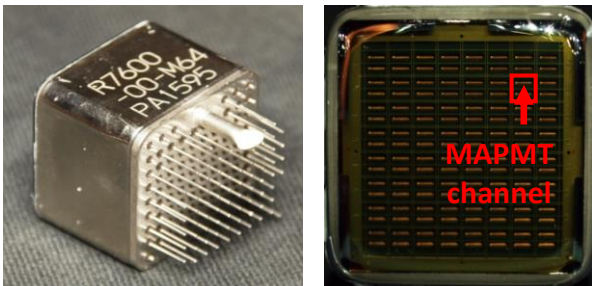
- Scintillating **fibers**



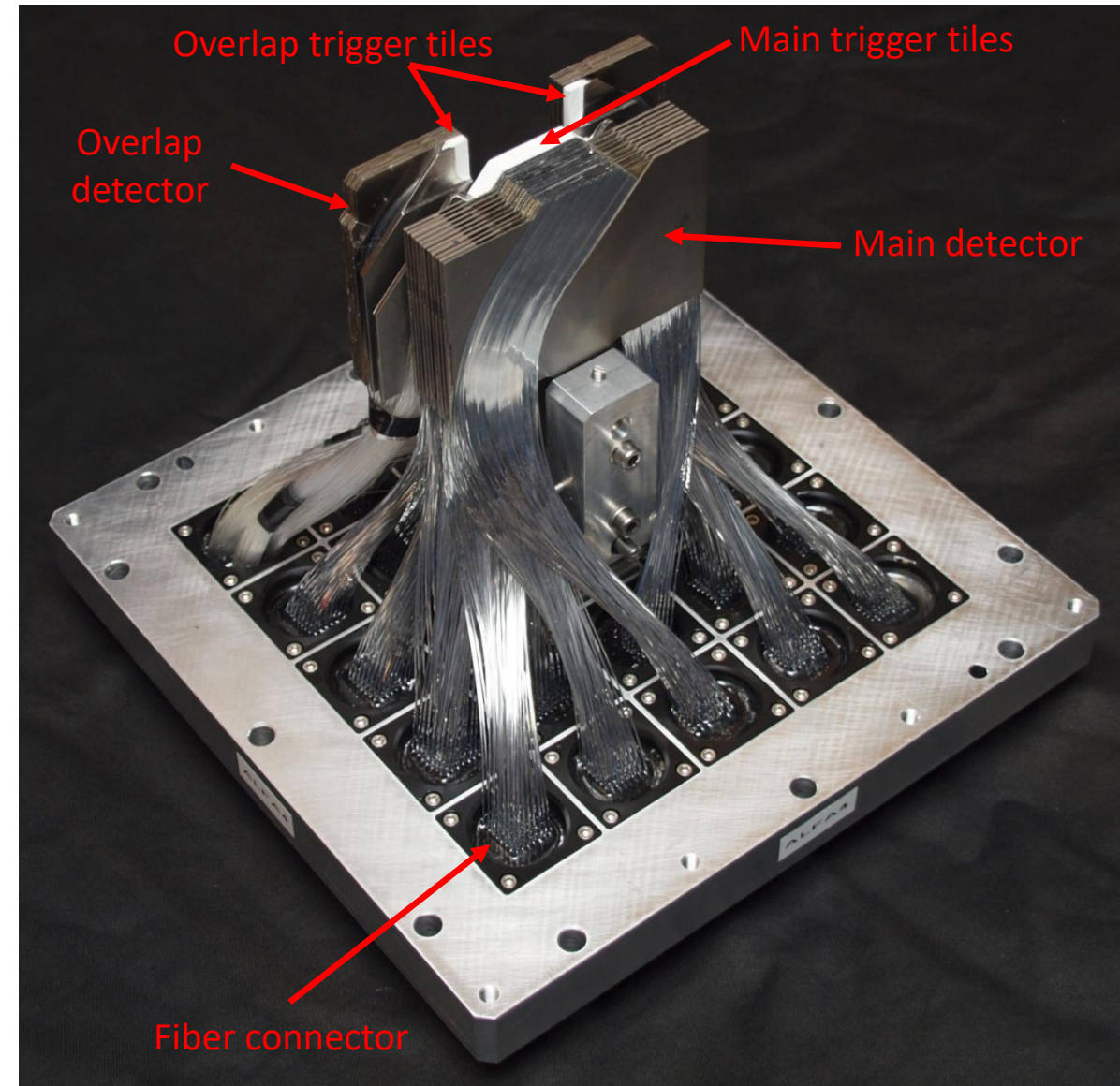
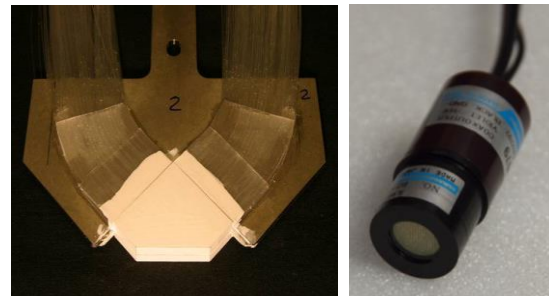
- Main detector plate



- MultiAnode PhotoMultiplier Tube (**MAPMT**)

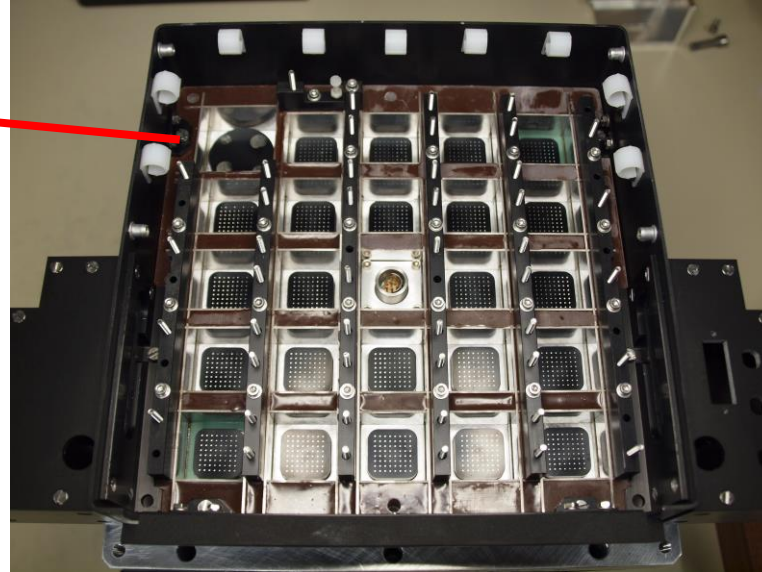


- Main **trigger** scintillator tile



TFT Detector – Blackbox

Trigger PMTs

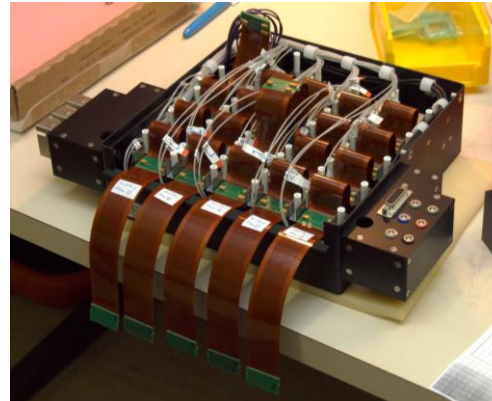


23 MAPMTs (64 channels)
→ 1472 channels

PhotoMultiplier FrontEnd (PMFs)



Kapton cables



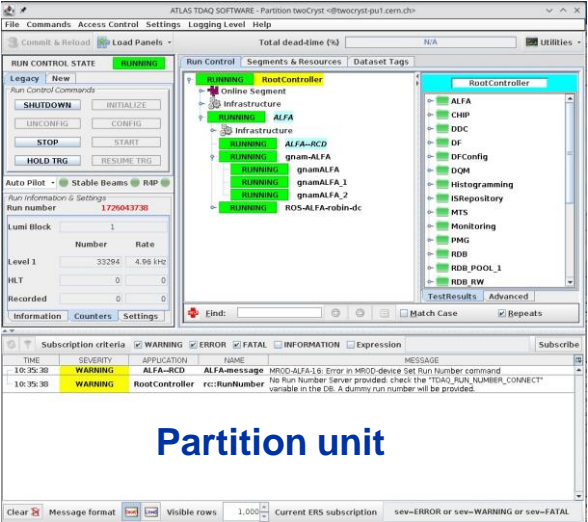
Motherboard



TFT Detector – Motherboard

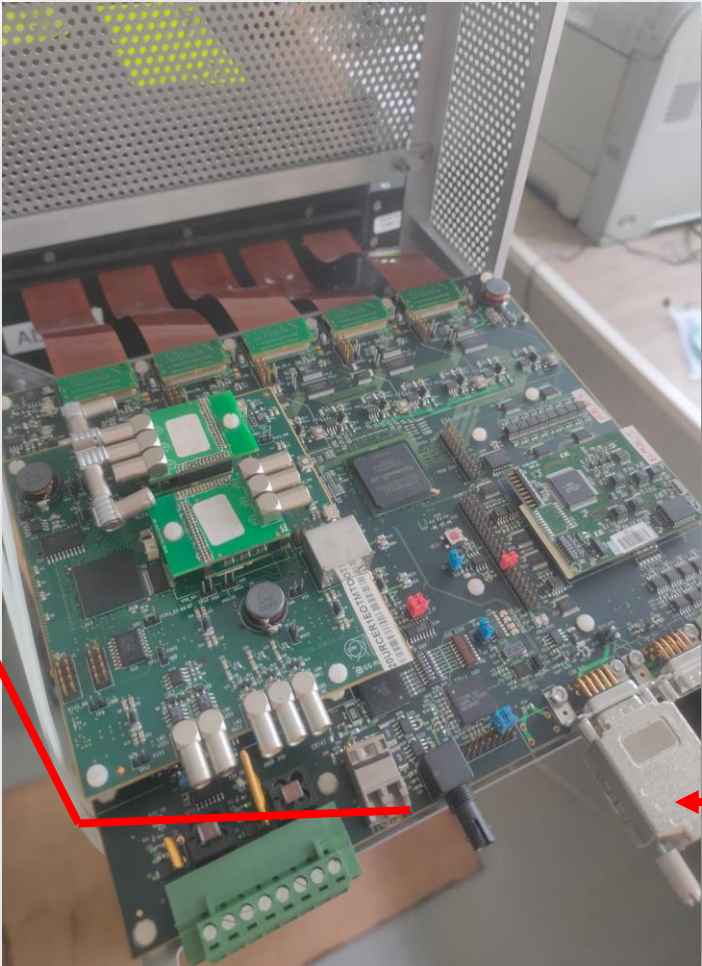
DAQ system

- **BOBR**
(LHC clock)
- **Timing / Trigger**
system
- **Readout** (mROD)



Partition unit

→ Histograms!

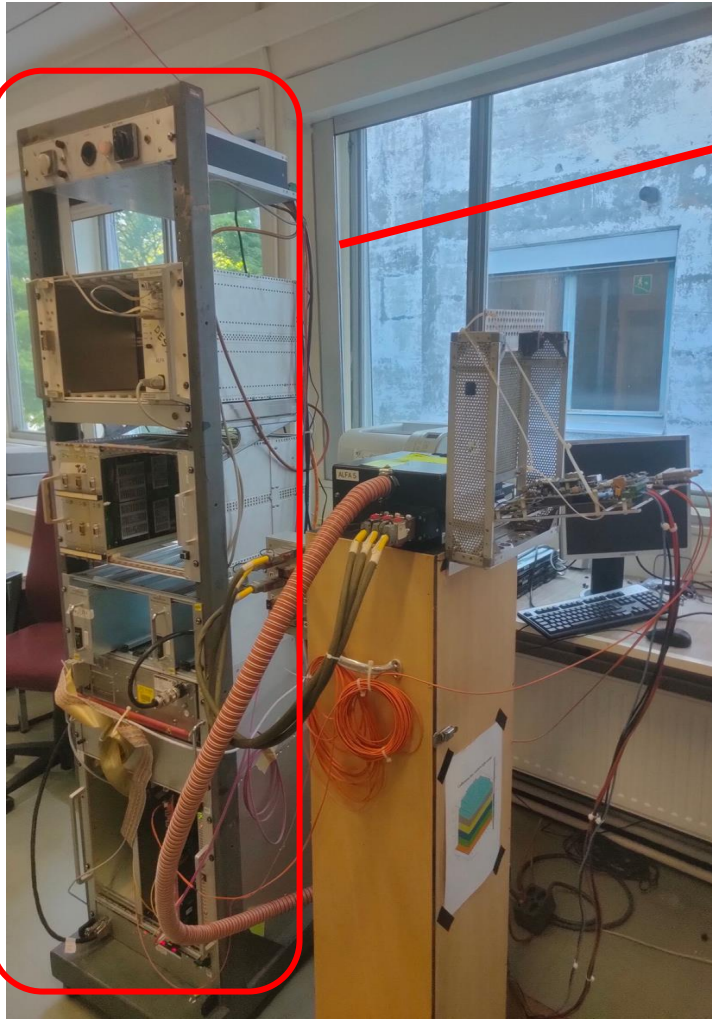


Detector control system (DCS)

- Set MAPMTs high voltages (HV)
- Configure **PMF**
- Monitor motherboard
- Monitor movement

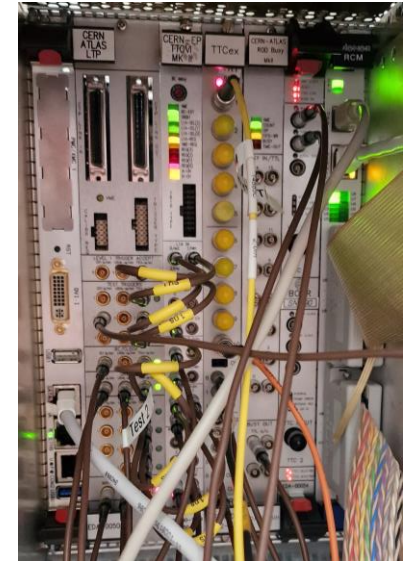


TFT Test Stand



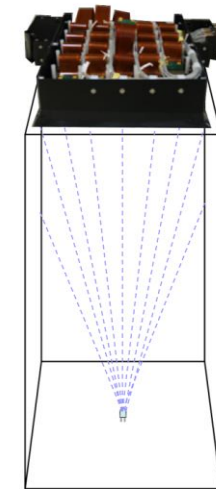
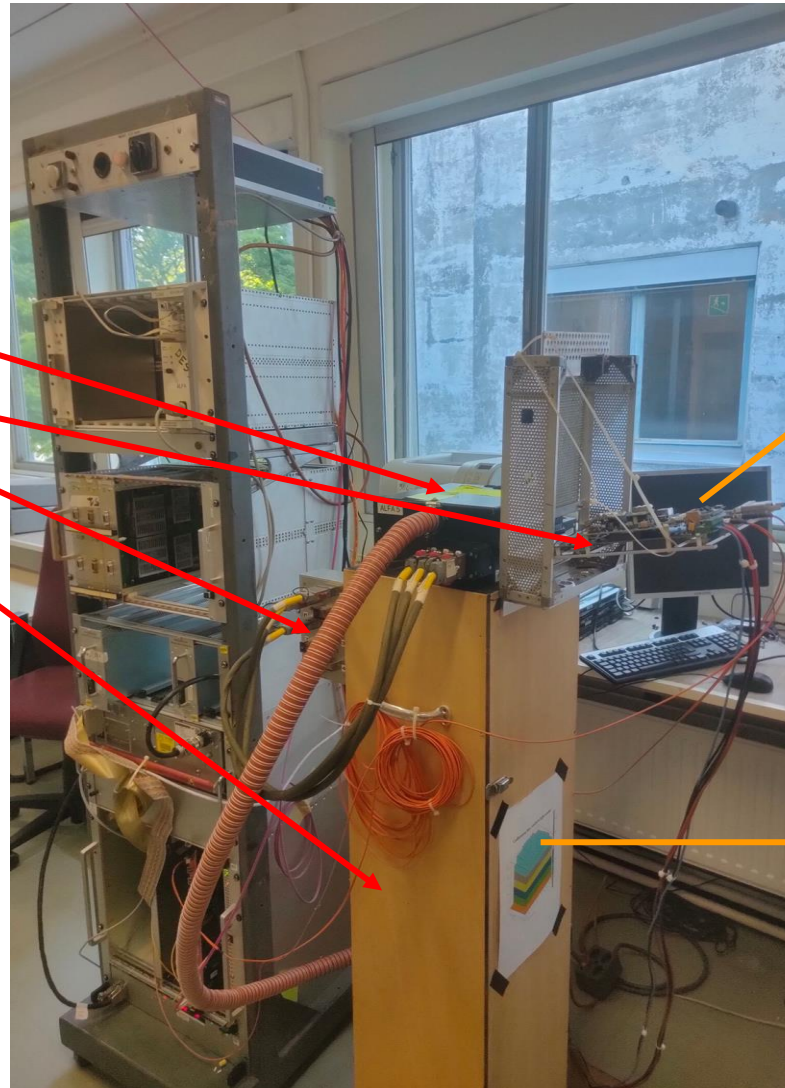
- **Power suppliers units (PSU)**
 - High Voltage PSU
 - CANbus PSU
 - Low Voltage PSU (Maraton)

- **DAQ VME crate**
 - Timing system
 - Readout



TFT Test Stand

- Power suppliers units (PSU)
- DAQ VME crate
- **Blackbox** containing photomultipliers
- **Motherboard**
- Air cooling for sensors and electronics
- Wooden box with **LED** at the bottom



Detector Timing

Tests with **pulsed LED light** ($f = 1\text{ KHz}$, $V_h = 3.3\text{ V}$, $w = 20\text{ ns}$)
→ find correct latency to time-in the detector wrt LED light

Slot 0	0
Slot 1	0
Slot 2	0
Slot 3	0
Slot 4	DATA!
Slot 5	0
Slot 6	0
...	...

TRIGGER

Latency

RP5 - Trigger logic setup

T1

T2

T1T2

Tol1

Tol2

Tled

Tsp1

Tsp2

RP5 - LED bias setup

Mode

1 kHz Clock

LED_ED1

Bias voltage (step)

255

Pulse width (ns)

60

APPLY

CANCEL

RP5 - Latency configuration

PMFs latency

47

SET

TRIGGER latency

138

SET

T charge latency

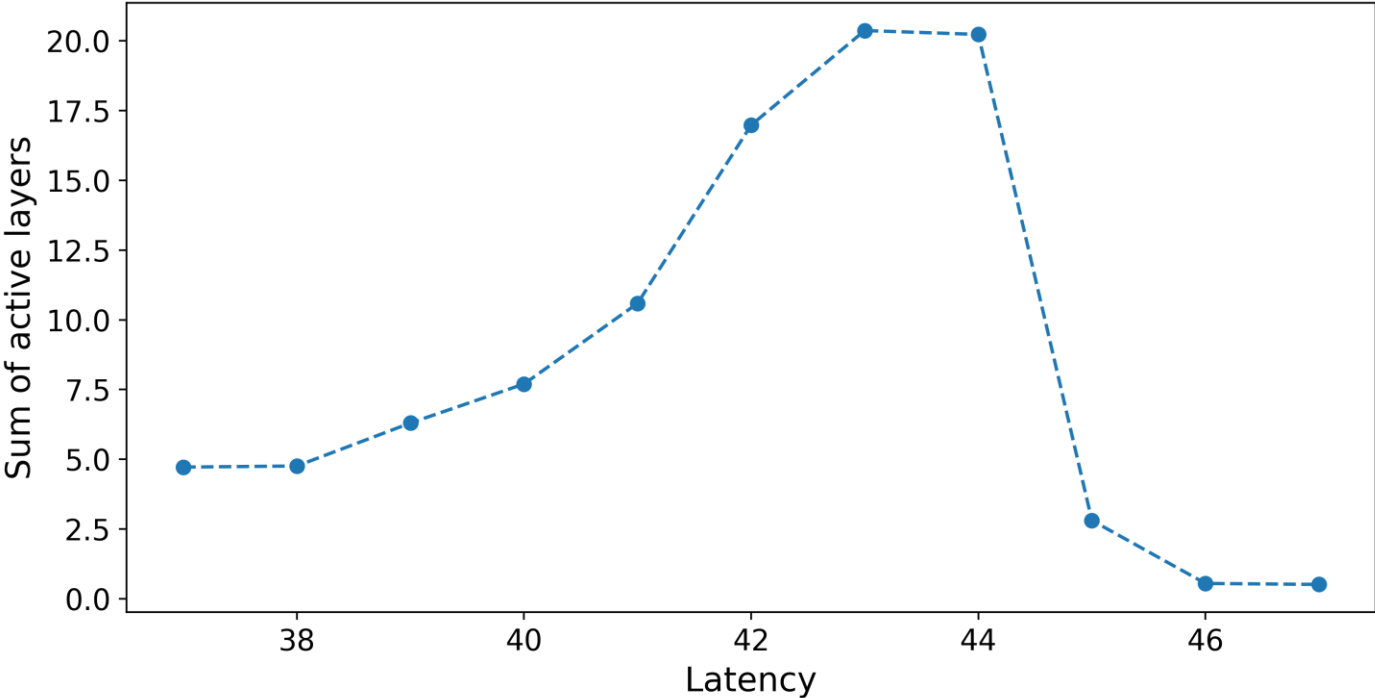
46

SET

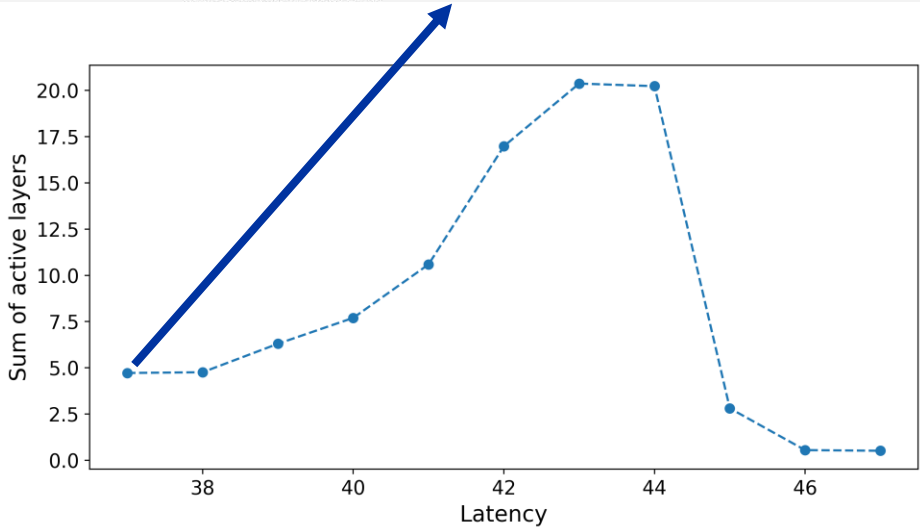
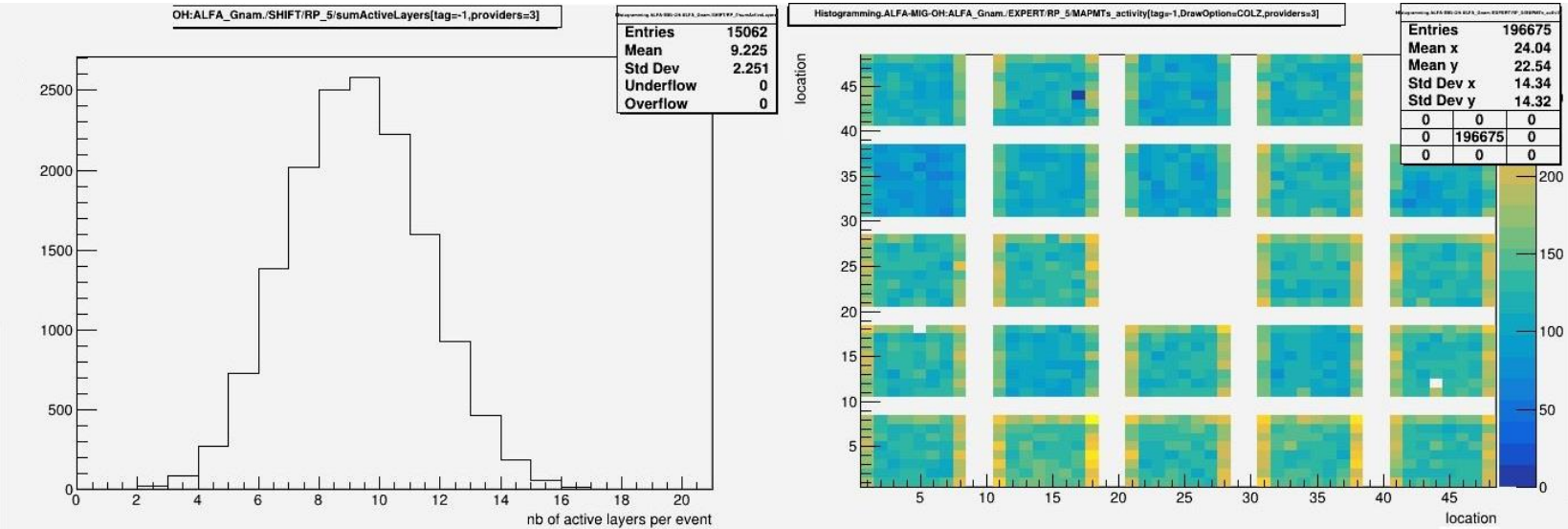
READ BACK

PMF

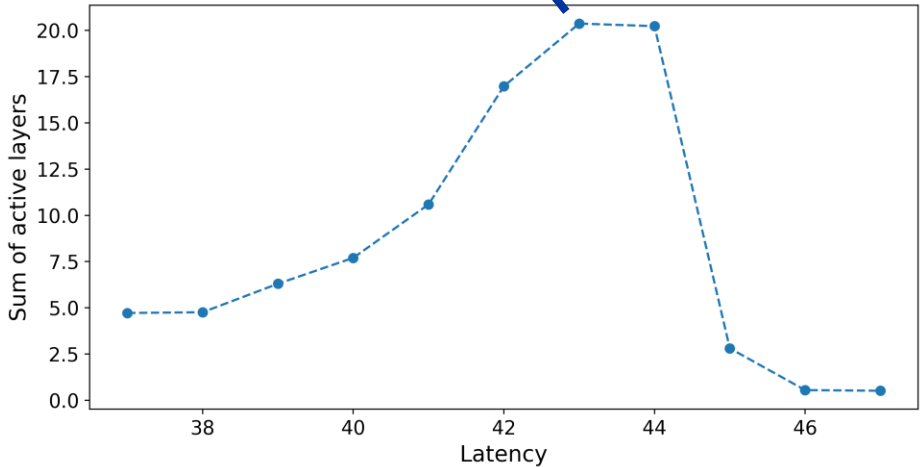
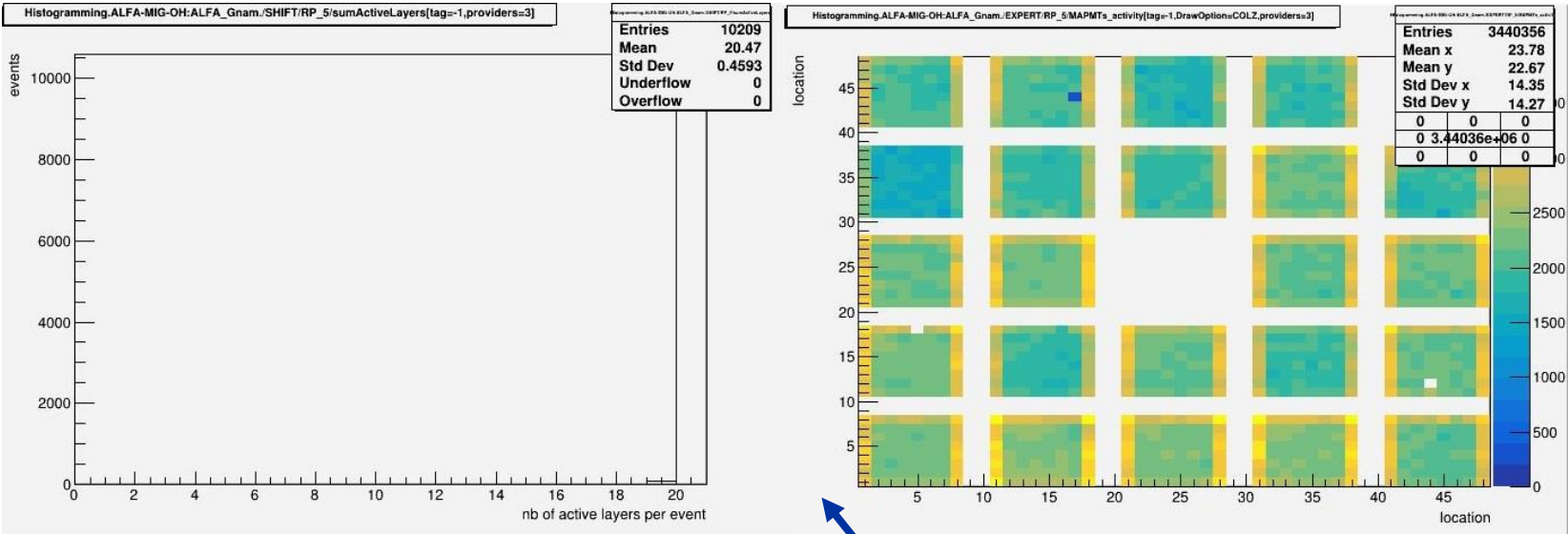
Depth read bac



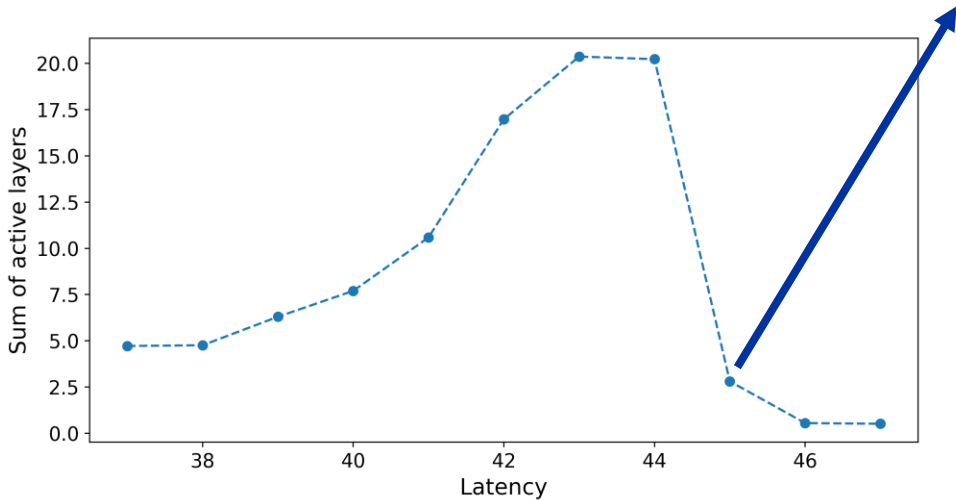
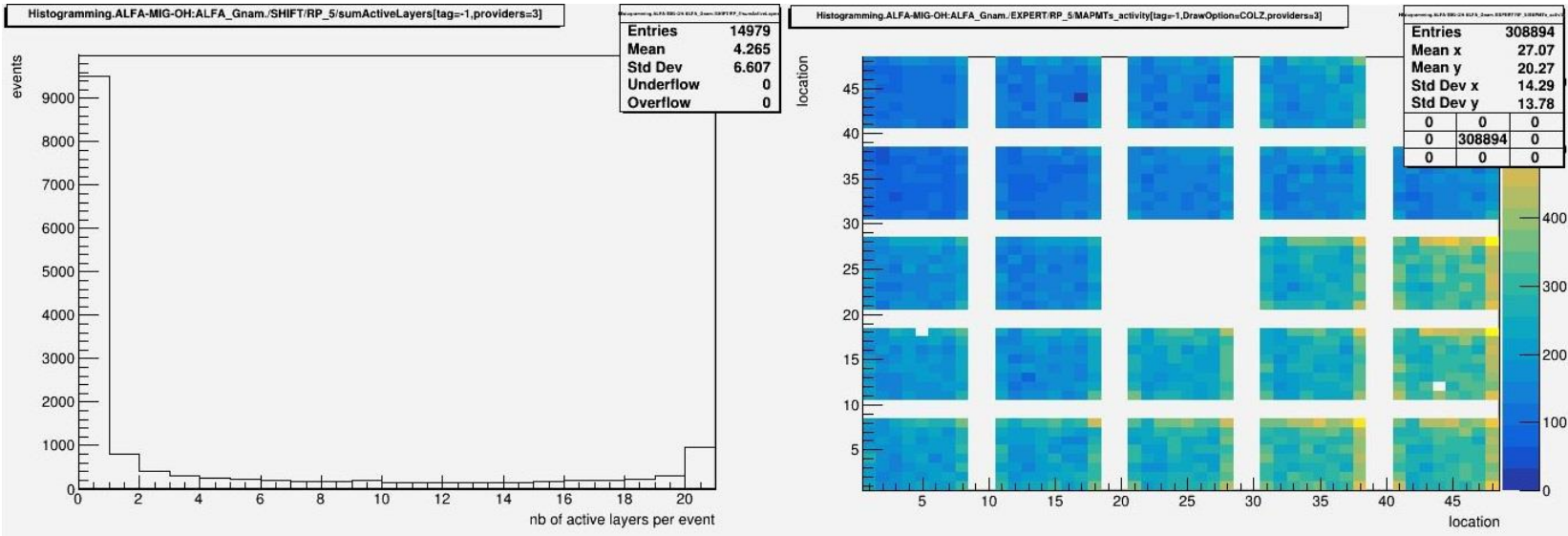
Detector Timing - Latency Scan



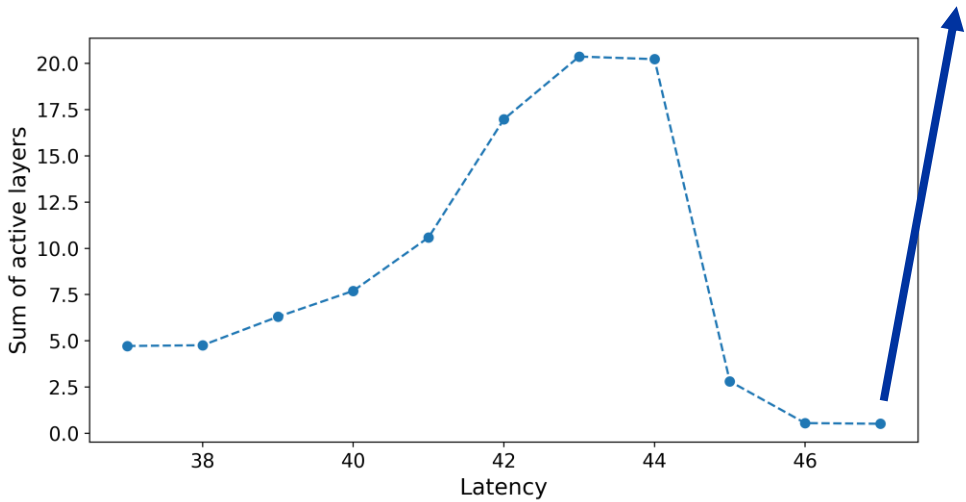
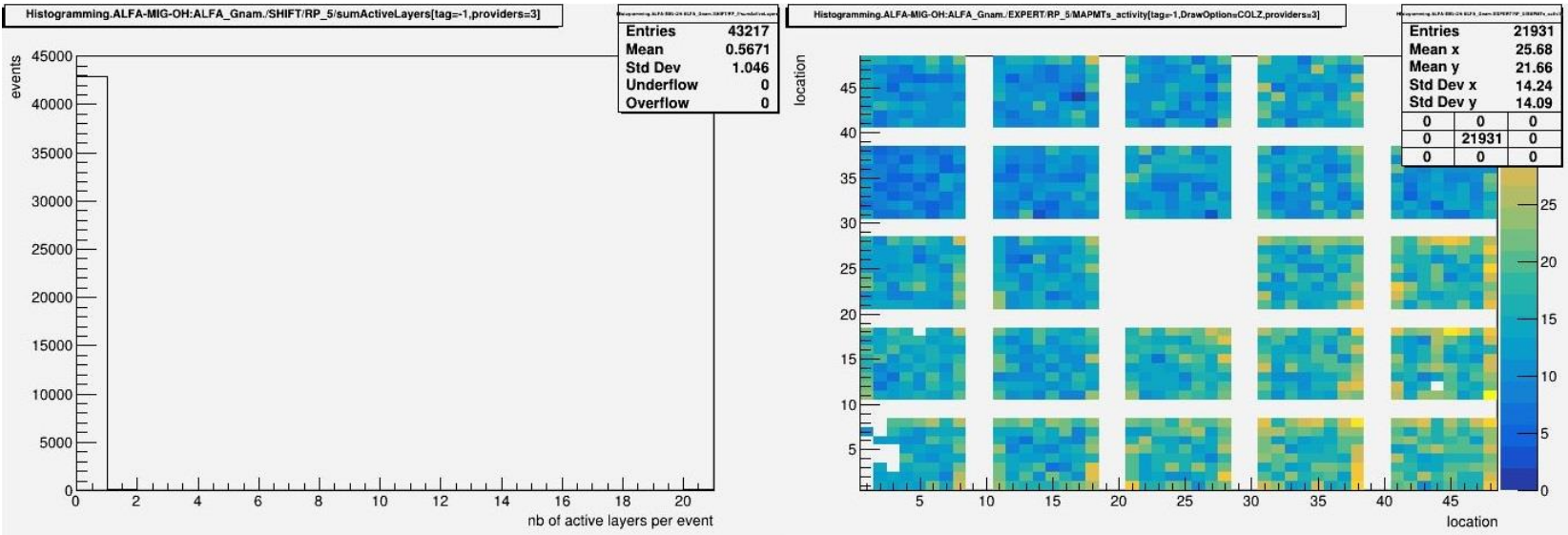
Detector Timing - Latency Scan



Detector Timing - Latency Scan

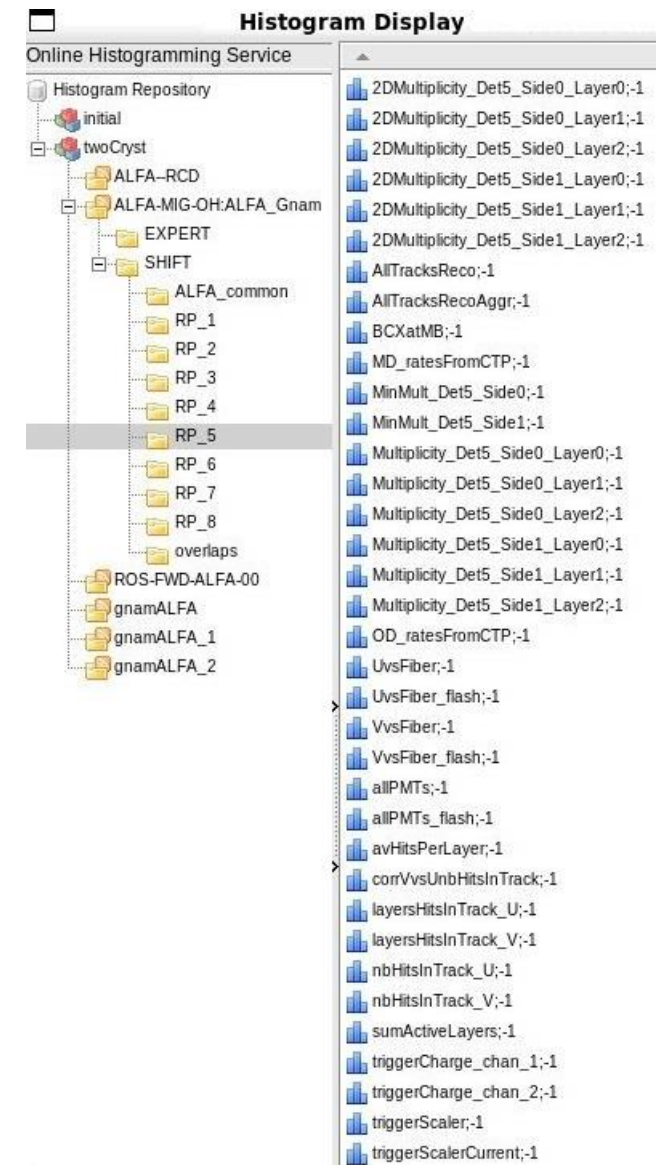


Detector Timing - Latency Scan



Next Steps

- Connection of DCS to Low Voltage (Ongoing)
- Check DAQ up to 50 kHz readout (maybe higher)
- Stability checks
- New implementation of using LHC clocks for the setup
- Finalize High voltage implementation in the Detector Control System
- Clean up the Detector Control System
- Minor hardware preparations for installation
- Adapt online histograms to TWOCRIST purposes





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