JAE-WON JANG

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EDUCATION

DOCTOR OF PHILOSOPHY STUDENT IN COMPUTER ENGINEERING (2016-PRESENT), PENNSYLVANIA STATE UNIVERSITY

Thesis Topic: Hardware Security – Using Emerging Memory Technologies, Threshold-Defined Transistors, and FPGA

DOCTOR OF PHILOSOPHY STUDENT IN COMPUTER ENGINEERING (2015-2016), UNIVERSITY OF SOUTH FLORIDA

Thesis Topic: Hardware Security – Using Emerging Memory Technologies

MASTERS OF SCIENCE IN COMPUTER ENGINEERING (2013-2015), UNIVERSITY OF SOUTH FLORIDA

Thesis Title: Security of Non-Volatile Memories – Attack Models, Analyses, and Counter-Measures

G.P.A: 3.76 / 4.00

BACHELOR OF SCIENCE IN COMPUTER ENGINEERING (2009 – 2013), UNIVERSITY OF SOUTH FLORIDA

G.P.A: 3.69 / 4.00 OVERALL ENGINEERING G.P.A: 3.83 / 4.00

RESEARCH INTEREST

Computer Architecture, Hardware Security, Emerging Technology, Cache Design

WORK EXPERIENCE

Summer 2013, **Intel Corporation** Internship, Hillsboro, OR

Collaborative work with **Taller Technologies** to create a new type of innovation called Shelf Edge Technology (http://newsroom.intel.com/community/intel_newsroom/blog/2013/06/25/intel-labs-looks-inside-the-future). Primary job was to debug the memory overload issues of Intel Android application. Secondary job was to utilize Intel facial recognition software called AIMSuite's API on Java language to validate the functionality using wireless cameras.

Fall 2013 to Summer 2016, **University of South Florida** Research Assitantship**,** Tampa, FL

At USF, my research focused on employing CMOS and emerging memory technology.

- Developed the 7-T SRAM Physically Unclonable Function (PUF) using Magnetic Tunnel Junction (MTJ) and showed improved stability and robustness using HSpice, VerilogA, and Matlab.
- Designed layouts (utilized up to Metal8 layer) of non-volatile sequential elements and schematics using 65nm library on Virtuoso
- Modeled the STT-RAM using Objective Oriented Micromagnetic Framework (OOMMF) software to analyze the vulnerabilities and simulate the impact of different form of attack.

Spring 2014 to Spring 2015, **University of South Florida** Tutor, Tampa, FL

At USF INTO program, I tutored students on graduate-level Computer Engineering core courses (Operating Systems, Algorithm, and Computer Architecture).

Fall 2016 to Summer 2017, **Penn State University** Research Asssistantship, State College, PA

Research assisting my advisor on the topic of hardware security

Fall 2017 to Present, **Penn State University** Teaching Assistantship, State College, PA

Working as an instructor for the course CMPSC 122 – Intermediate Programming (course related to data structure using the Python language) -

PUBLICATIONS

JOURNALS

J1. Jae-Won Jang, Asmit De, Deepak Vontela, Ithihasa Nirmala, Swaroop Ghosh, and Anirudh Iyengar, "Threshold-defined Logic and Interconnect for Protection against Reverse Engineering", Transactions on Information Forensics and Security (TFIS). (Impact Factor: 4.3) – Submitted For Review -

J2. Anirudh Iyengar, Swaroop Ghosh, and **Jae-Won Jang**, "MTJ-based State Retentive Flip-Flop with Enhanced-Scan Capability to Sustain Sudden Power Failure", Transactions on Circuits and Systems I (**TCAS-I**). (Impact Factor: 2.3)

J3. Swaroop Ghosh, Anirudh Iyengar, Seyedhamidreza Motaman, Rekha Govindaraj, **Jae-Won Jang**, Jinil Chung, Jongsun Park, Xin Li, Rajiv Joshi, and Dinesh Somasekhar, "Overview of Circuits, Systems, and Applications of Spintronics", IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS). (Impact Factor: 1.6)

J4. Anirudh Iyengar, Kenneth Ramclam, Swaroop Ghosh, **Jae-Won Jang** and Cheng-Wei Lin, "Spintronic PUFs for Security, Trust and Authentication", ACM Journal of Emerging Topics Computing Systems (**JETC Special Issue**). (Impact Factor 0.83)

CONFERENCES:

C1.**Jae-Won Jang**, Jongsun Park, Swaroop Ghosh, and Swarup Bhunia, "Self-Correcting STTRAM under Magnetic Field Attacks", Design Automation Conference (**DAC**), 2015.

C2.**Jae-Won Jang** and Swaroop Ghosh, "Performance Impact of Magnetic and Thermal Attack on STTRAM and Low-Overhead Mitigation Techniques", The International Symposium on Low Power Electronics and Design (**ISLPED**), 2016. Acceptance Rate = ~25%

C3.**Jae-Won Jang** and Swaroop Ghosh, "Design and Analysis of Novel SRAM PUFs with Embedded Latch for Robustness", International Symposium on Quality Electronic Design Conference (**ISQED**), 2015.

C4.**Jae-Won Jang,** Asmit De and Swaroop Ghosh, "Recent Trends in Intellectual Property (IP) Protection from Reverse Engineering", Microprocessor Test and Verification Conference (MTV), 2016 (Invited Paper).

C5.**Jae-Won Jang** and Swaroop Ghosh, "Security of Magnetic Memories: Vulnerabilities, Attack Models, Analyses, and Prevention", **SRC TECHCON** 2015.

C6.**Jae-Won Jang** and Swaroop Ghosh, "Improving Robustness of STTRAM Under Magnetic and Thermal Attack", **SRC TECHCON** 2016.

C7.**Jae-Won Jang,** Deepak Reddy Vontela, Ithihasa Reddy Nirmala, and Swaroop Ghosh, "A Novel Threshold Voltage Defined Multiplexer for Interconnect Camouflaging", Government Microcircuit Applications and Critical Technology (**GOMATech-17**), 2017.

C8.**Jae-Won Jang** and Swaroop Ghosh, "Security of Magnetic Memories: Vulnerabilities, Attack Models, Analyses and Preventions", Government Microcircuit Applications and Critical Technology (**GOMATech-16**), 2016.

C9.Cheng-Wei Lin, **Jae-Won Jang,** and Swaroop Ghosh, "Schmitt-Trigger-Based Recycling Sensor and Robust and High-Quality PUFs for Counterfeit IC Detection", Government Microcircuit Applications and Critical Technology (**GOMATech-15**), 2015.

C10.Alexander Holst, **Jae-Won Jang** and Swaroop Ghosh, "Investigation of Magnetic Field-Based Attacks on Magnetoresistive Random-Access Memory", International Symposium on Quality Electronic Design Conference (**ISQED**), 2017.

C11. Swaroop Ghosh, Nasim Khan, Asmit De, **Jae-Won Jang**, "Security and Privacy Threats to On-Chip Non-Volatile Memories and Countermeasures", Proceedings of the 35th International Conference on Computer-Aided Design (**ICCAD '16**), 2016 (Invited Paper).

WORK-IN PROGRESS | DEMONSTRATION:

X1. **Jae-Won Jang** and Swaroop Ghosh, "Data Integrity of STTRAM Vulnerabilities, Attack Models and Preventions", Design Automation Conference (**DAC**), 2016 (WIC).

X2. Alexander Holst, Swaroop Ghosh, and **Jae-Won Jang,** "Investigation of Magnetic Field-Based Attacks on Magnetoresistive Random-Access Memory (Demo Proposal)", IEEE International Symposium on Hardware Oriented Security and Trust (**HOST**), 2016.

X3. Anirudh Iyengar, Kenneth Ramclam, **Jae-Won Jang** & Cheng Wei Lin, Spintronic PUFs for Security, Trust and Authentication, Cyber Security Awareness Week Conference (CSAW), 2014. (3rd Place)

INVENTION DISCLOSURES

P1. Non-Volatile Flip-Flop with Enhanced-Scan Capability to Sustain Sudden Power Failure, Swaroop Ghosh, Anirudh Iyengar, and Jae-Won Jang (filed March 2015).

RESEARCH EXPERIENCES

- Security of Non-Volatile (NV) Memories
  - Research focused on the exploration of Spintronics for the new type of PUF [J2]
  - Demonstrated the novel vulnerabilities of emerging memory technology (STT-RAM) [C2] using OOMMF. This research is also published n **SRC TECHCON 2015 / 2016** [C4,5].
  - Explored the improved robustness of hardware security by implementing MTJ onto SRAM PUF [C1, C4] and published research paper in **GOMATech** and **ISQED.**
- Energy-Efficient Sequential Circuit Design
  - Employed Spintronics for energy-efficient circuit [J1]
- IC Design
  - Completed 1 tapeout. Experienced in padframe design using standard cmos065 library

CLASS PROJECTS

- Foundation of Software Security Project
  - Extensively studied **Buffer-Overflow Attacks** and **implemented it** on iOS. Demonstrated such attack on an iTouch 4th generation using Objective-C language.
- Emerging Topics in Network Security Project
  - Wrote a paper in regards to biometric authentication methods titled "Using User's Voice as the Catalyst for Biometric Authentication".
  - **Voice verification system** was researched upon and have implemented many different classifiers such as Gaussian Mixer Model (GMM), Hidden Markov Model (HMM), Fast Fourier Transform (FTT), and Dynamic Time Warp (DTW) to compare the effectiveness.
- CMOS Design Project
  - Designed, simulated, verified, and extracted IC layouts of basic gates, full adders, multiplexers, comparators, decoders, them using Virtuoso, Calibre, and DRC.
  - Designed thermometer semiconductor chip on the PadFrame using Virtuoso.
- Computer System Design Project
  - Programmed digital voice recorder using a ML505 FPGA board using Verilog language and MIPS Assembly Code. Recorder was able to record/play/pause/delete message.

AWARDS, HONORS AND GRANTS

- HOST 2016 Student Grant
- Thomas E. and Ann C. Wade Scholarship

AFFILIATION AND LEADERSHIP

- Former-Semiconductor Research Corporation **(SRC)** Member
- Association for Computing Machinery **(ACM)** Member
- IEEE-CS Society Member
- Tau Beta Pi (National Engineering Honor Bachelor Society) Member

SKILLS (Highlighted = Comfortable)

- Programming Language: **C**, **C++**, **Java**, **Javascript**, **Matlab**, **Objective-C**, Perl, **Python**
- Database-related: Currently learning Memcached / Redis; Also looking into Hadoop
- IDE: Visual Studio, NetBeans, **Eclipse**, **Github**, Xilinx ISE, and SimpleScalar
- Proficient at using GNU / Linux distribution.