Computer Architecture Homework 4

Spring 2022, April

1 Boolean Algebra and Logic Gates

Question 1.1

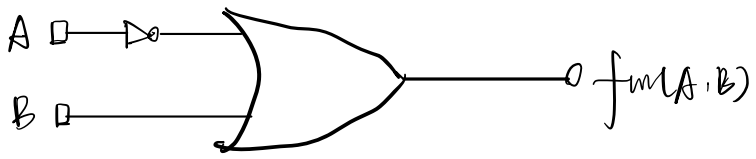
For the following function:
bool fun(bool A, bool B) return (A == B) ? true : B;
a. Write the Truth Table of it.(5 pts)
b. Write the Boolean Expression of it and simplify it (as simple as possible).(10 pts)
c. Draw the gate diagram that implements the boolean expression in b.(5 pts)

a.

A	B	fun(A, B)
0	0	1
0	1	1
1	0	0
1	1	1

b. $fun(A,B) = \bar{A}\bar{B} + \bar{A}B + AB = \bar{A} + AB = \bar{A} + B$

c.



Question 1.2

a. Simplify the following Boolean Expressions (as simple as possible and show enough steps please).(15 pts)

$B(AB + A\overline{B})(\overline{AC} + C) + \overline{CC} + (A + \overline{B})(\overline{CD})$

$= (AB + A\bar{B})(\bar{A} + C) + \bar{C} + A\bar{C}\bar{D} + \bar{B}\bar{C}\bar{D}$

$= AB(\bar{A}C + C) + \bar{C} + A(\bar{C} + \bar{D}) + \bar{B}(\bar{C} + \bar{D})$

$= AB(\bar{A} + \bar{C} + C) + \bar{C} + A\bar{C} + A\bar{D} + \bar{B}\bar{C} + \bar{B}\bar{D}$

$= AB(\bar{A} + 1) + \bar{C} + A\bar{C} + A\bar{D} + \bar{B}\bar{C} + \bar{B}\bar{D}$

$= AB + \bar{C} + A\bar{C} + A\bar{D} + \bar{B}\bar{C} + \bar{B}\bar{D}$

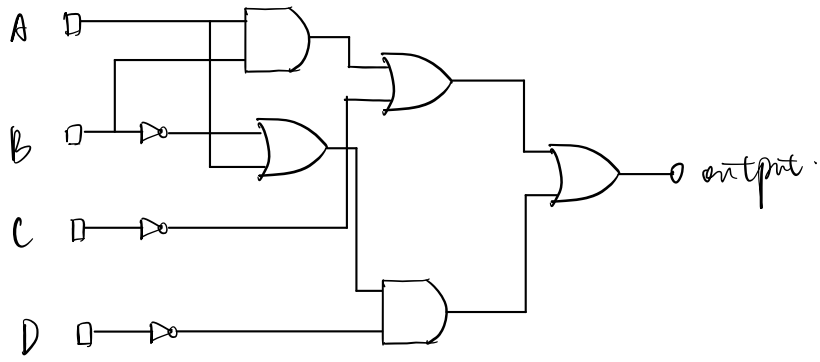
$= AB + (\bar{C} + A\bar{C} + \bar{B}\bar{C}) + (A + \bar{B})\bar{D}$

$= AB + \bar{C} + (A + \bar{B})\bar{D}$

$AB + \bar{C} + A\bar{D}(B + \bar{B}) + \bar{B}\bar{D}$ $AB + \bar{C} + \bar{B}\bar{D}$

$AB + \bar{C} + A\bar{D}B + A\bar{D}\bar{B}$

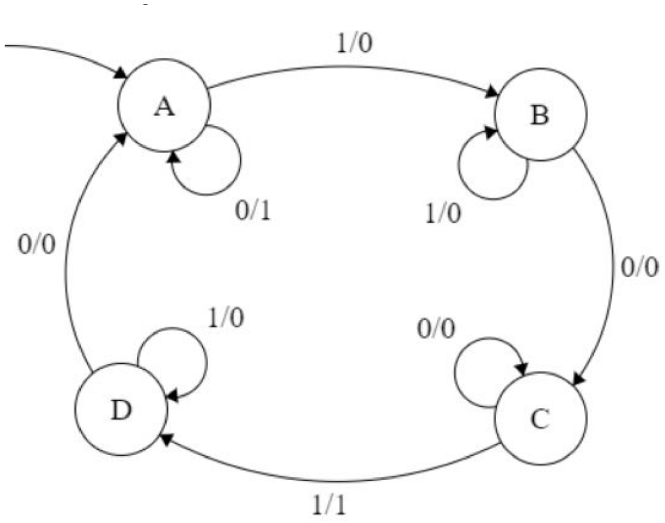
b. Draw the circuit according to the simplified boolean expression in (a) . (10 pts)



2 FSM

Question 2

For the following Finite State Machine, fill out the remainder of the table. (15 pts)



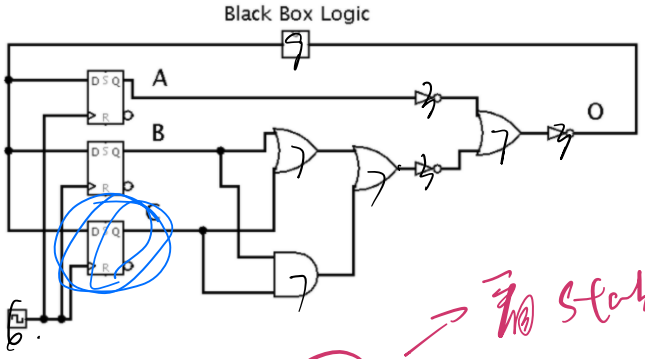
Input	-	1	0	0	1	1	0	0	0
Next State	A	B	C	C	D	D	A	A	A
Output	-	0	0	0	1	0	0	1	1

Table 1: Write Answer Here

3 SDS

Question 3

In the following circuit, NOT gates have a delay of 3ns, AND and OR gates have a delay of 7ns, and the "Black Box" logic component has a delay of 9ns. The registers have a clk-to-q delay of 6ns and setup times of 5ns.



a. What is the maximum allowable hold time of the registers? (please include enough explanation) (20 pts)

To determine the maximum allowable hold time, we have to find the shortest path. The hold time ≤ time of the shortest path. So.
maximum allowable hold time = time of the shortest path, which is from A to O, containing one clk-to-q delay, one OR gate, two NOT gates and a Black Box Logic.
So. Maximum hold time = 6+7+3+3+9 = 28 ns

b. What is the minimum acceptable clock period for this circuit? (please include enough explanation) (20 pts)

The minimum clock period is determined by the longest path, which can be CO or BO, either containing one clk-to-q delay, three OR gates (or two OR gates and one AND gate), two NOT gates and a Black Box Logic, and the set up time.

minimum clock period = 6+3×7+2×3+9+5 = 47 ns