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M40PF uciaprln0044 Specification

Ver01.01

Corresponding Requirement Specification
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Renesas Electronics Corporation

Approved	Checked	Prepared
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Version History Overview

Version	Refer	Modification	Approved	Checked	Prepared
V0.01	All	Copy from "M40PF uciaprln0043 Specification Ver. 01.00" and modified for uciaprln0044.			2017/05/25 ETD1-PC-DP1 K.Ishimi
V00.02	All	Feedback from IPS peer review (1st).			2017/06/06 ETD1-PC-DP1 K.Ishimi
V00.03	3.11.2.1.4 4.27&4.28	"Table 3-7 Baud Rate and Tolerance" was corrected. Fixed typo.			2017/06/23 ETD1-PC-DP1 K.Ishimi
v00.04	Cover 4.30	- Add document(ID&Name) of Corresponding Requirement Specification - Copyright is corrected.(RSD -> REL) - LRSS.RSDD: description was corrected.			2017/07/18 PCDD-DPDS1 K.Ishimi
v01.00	All	Feedback from IDR1.			2017/08/25 PCDD-DPDS1 K.Ishimi
v01.01	All	Feedback from IDR3 peer review.			2017/09/26 PCDD-DPDS1 K.Ishimi

1 ABSTRACT

The RLIN3 module has been developed to support LIN Master mode, LIN slave mode as well as UART mode communication. This document describes the registers and functionality of the RLIN3 module ported to various products.

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Glossary

Use of Words

Use of the words "shall", "should", "must", "will", and "may" within this Specification observe the following rules:-

- The word SHALL in the text expresses a mandatory requirement of the Specification.
- The word SHOULD in the text expresses a recommendation or advice on implementing such a requirement of the Specification, RSD expects such recommendations or advice to be followed unless good reasons are stated for not doing so.
- The word MUST in the text is used for legislative or regulatory requirements (e.g. Health and Safety) with which both
  RSD and the Supplier shall comply. It is not used to express a requirement of the Specification.
- The word WILL in the text expresses a provision or service by RSD or an intention by RSD in connection with a requirement of the Specification. The Supplier is implicitly authorised to rely on such service or intention.
- The word MAY in the text expresses a permissible practice or action. It does not express a requirement of the Specification.

Color of Tests

Use of the color "PURPLE", "GREEN" within this Specification observe the following rules:-

- The color PURPLE is specification of Secret function.
- The color GREEN is designer's information. (It should not be published to users)

2 ABBREVIATIONS

RSD	Renesas System Design Corporation
LIN	Local interconnect network protocol
RLIN	Renesas LIN IP
Tbit	Transmission bit
BPS	Bits per Second
BRG	Baud rate generator
SW	Software
MCU	Microcontroller unit
RxD	Reception pin
UART	Universal asynchronous reception transmission protocol
RS	Response Space
IBS	Inter-Byte Space
IBHS	Inter-Byte Header Space
HOCO	High speed On Chip Oscillator

3 OVERVIEW

This section describes the RLIN3 module. This module can be used as a LIN master node or LIN slave node to perform LIN communications (LIN frames and LIN Wakeup signals) complying with LIN protocol spec versions 1.3, 2.0, 2.1, 2.2 and SAE J2602 with a limited SW support. It also supports UART mode (half-duplex as well as full-duplex communication).

3.1 LIN COMMUNICATION FUNCTION

- Variable data byte count in the response 0 ~ 8byte
- Selectable Checksum type - automatic transmission, automatic judgement
  - Classic
  - Enhanced
- Three points majority sampling Enable / Disable for received bits
- Possibility to read Checksum generated by IP after completion of response transmission & received checksum after response reception.
- LIN Response transmission or reception with number of data bytes more than or equal to 9 is supported
- For data group response TX or RX, the total number of Response data bytes can be more than or equal to 9. The number of data bytes in each data group should only be configured to be between 1 and 8.
- Self-Test Mode.
- Status Flag write control mode (not open to customers)

3.2 LIN MASTER MODE

- Baud Rate Select Function
  - 2400, 4800, 9600, 10417, 19200, 38400 and 115200 bps can be generated from the BRG.
  - Supports bit rates from 1 to 115.2 Kbits/s
    - For supporting 115.2 Kbits/s, users should set LIN communication clock to multiple of 24 MHz. In this case LWBR.PRS[2:0] should be configured as "000b".
    - 38.4Kbps and 115.2Kbps are outside a LIN standard. This function should check an operating condition by the product side.
- Variable frame structure
  - Break Low transmission length 13 ~ 28Tbit
  - Break Del (delimiter) 1 ~ 4Tbit
  - Inter-byte Header Space(IBHS) 0 ~ 7Tbit
  - Response Space (RS) 0 ~ 7Tbit
  - Inter-byte Space (IBS) 0 ~ 3Tbit
- Transmission mode selection. Two modes are selectable:
  - Mode that transmits Header + Response with single Start Command.
  - Mode that transmits Header and Response by individual Start Commands.
- Wake-up transmission/reception
  - Transmission (1 to 16Tbit selectable by software) / Reception of Wake-up possible in LIN Wake-up State.
  - Automatic baud rate selection possible for Wake up mode
- Status
  - Successful Transmission
  - Header Transmission
  - Successful Reception
  - One Byte Reception
  - Error SUM
  - LIN Mode Status
    - Reset
    - Normal
    - Wakeup
- Error status, detection can be enabled or disabled (except Checksum Error and Response Preparation Error)
  - Bit error
  - Physical Bus error

- Framing error
- Frame Timeout error / Response Timeout error
- Checksum error
- Response Preparation Error

3.3 LIN SLAVE MODE

- Baud Rate Select Function
  - 2400, 4800, 9600, 10417, 19200, 38400 and 115200 bps can be generated from the BRG.
  - Supports bit rates from 1 to 115.2 Kbits/s
    - For supporting 115.2 Kbits/s, users should set LIN communication clock to multiple of 20 MHz, 24 MHz or 28 MHz. In this case LWBR.PRS[2:0] should be configured as "000b".
    - 38.4Kbps and 115.2Kbps are outside a LIN standard. This function should check an operating condition by the product side.
- Variable frame structure
  - Break Low reception length (fixed baud rate) 9.5 or 10.5Tbit
  - Break Low reception length (Automatic baud rate detection) 10 or 11Tbit
  - Response Space (RS) 0 ~ 7Tbit
  - Inter-byte Space (IBS) 0 ~ 3Tbit
- Header reception mode selection. Two modes are selectable:
  - Automatic baud rate detection mode (baud rate detection in SYNC field).
  - Fixed baud rate mode (baud rate is fixed based on BRP value).

Wake-up transmission/reception

- Transmission (1 to 16Tbit selectable by software) / Reception of Wake-up possible in LIN Wake-up State.

- Status
  - Successful Transmission (Response)
  - Header Reception
  - Break Field Reception
  - Sync Field Reception
  - Successful Reception (Response)
  - One Byte Reception
  - Error SUM
  - LIN Mode Status
    - Reset
    - Normal
    - Wakeup
- Error status, detection can be enabled or disabled (except Checksum Error and Response preparation error)
  - Bit error
  - ID Parity error
  - Sync Field error
  - Framing error
  - Frame Timeout error / Response Timeout error
  - Checksum error
  - Response preparation error

3.4 UART COMMUNICATION FUNCTION

- Full-duplex and Half-duplex communication
- Configurable Data length.
  - 7 bits
  - 8 bits
  - 9 bits (expansion bit setting)
- Configurable number of Stop bits during Transmission
  - 1 bit
  - 2 bits
- Parity configuration
  - Even parity

  - Odd parity
  - 0 (parity bit is always "0")
  - None
- UART multi-byte transmission function -- possibility to handle up to 9 bytes with no Register load.
- Transmission/ Reception Inversion function. Two possibilities
  - No inversion of Tx/Rx
  - Inversion of Tx/Rx
- Bit order configuration. Two possibilities.
  - LSB first
  - MSB first
- Status
  - Successful Transmission
  - UART Transmission status
  - UART Reception status
  - ID match
  - Expansion bit detection
  - Error SUM
  - UART mode state
    - Reset
    - Normal
- Error status, detection can be enabled or disabled for Bit Errors & framing errors & Overrun error
  - Bit error
  - Framing error
  - Parity error
  - Overrun error
- Baud Rate Select Function
  - Supports bit rates up to 5.33 Mbits/s @32 MHz LIN communication clock frequency

3.5 INTERRUPTS

3.5.1 LIN mode Interrupts

In RLIN3 module, there are 2 options for generating Interrupt outputs if the IP is configured in LIN mode.

Option 1:
In LIN mode (Master / Slave), if LIN Interrupt output select bit is "1", then, the RLIN3 module will generate 3 active-high pulse interrupts. The 3 generated interrupts are:

- Successful Transmission interrupt request (Response of one data group, Header, Wake-up),
- Successful Reception interrupt request (Response of one data group, Header, Wake-up)
- Error Detection interrupt request

Option 2:
In LIN mode (Master / Slave), if LIN Interrupt output select bit is "0", then, the RLIN3 module will generate 1 active-high pulse interrupt that is created by using an OR gate for the 3 interrupt lines specified above.

Every interrupt source can also be disabled or enabled individually for both options.

3.5.2 UART mode Interrupts

In UART mode, the RLIN3 module outputs the following active-high pulse interrupts:

- Transmission interrupt request
- Reception completion interrupt request
- Status interrupt request
- Loop back delayed data consistency check interrupt request

These interrupts are pulse signals and hence are cleared automatically after 1 LIN communication clock cycle. The UART interrupts can not be disabled.

3.6 NOTES FOR THE PRODUCT DESIGN

None

3.7 NOTES FOR THE USER MANUAL (UM) CREATION

None

3.8 RLIN3 USAGE LIMITATION

Items, which are not open to the customer are formatted in pink colour style, and need to be deleted when the UM is created.

3.9 NOTES FOR THE PRODUCT DESIGN

3.9.1 Requirement notes

3.9.1.1 Virtual cells

RLIN3 is using the following virtual cells:

Table 3-1 virtual cells (uciaprln0044)

Signal name	Function
ux099smc01gck0	clock gating cell
ux099smcclinv0	Invertor
ux099smccland20	2 input AND
ux099smcclor20	2 input OR
ux099smcclmux20	2 to 1 selector
ux099smc01ffnrqp0	FF with reset

3.9.2 Protocol

This module can be used as a LIN master node or LIN communications (LIN frames and LIN Wakeup signals) complying with LIN protocol spec versions 1.3, 2.0, 2.1, 2.2 and SAE J2602 with a limited SW support.

3.9.3 Known bugs

None

3.9.4 Legal information (patent export control license)

None

3.10 MACRO SIZE

Target macro size is 8238[um2]. (Synthesis condition is 110[MHz]. for uciaprln0044)

3.11 INTERFACE SPECIFICATION

3.11.1 Structure

Figure 3-1 shows Signal connection structure.

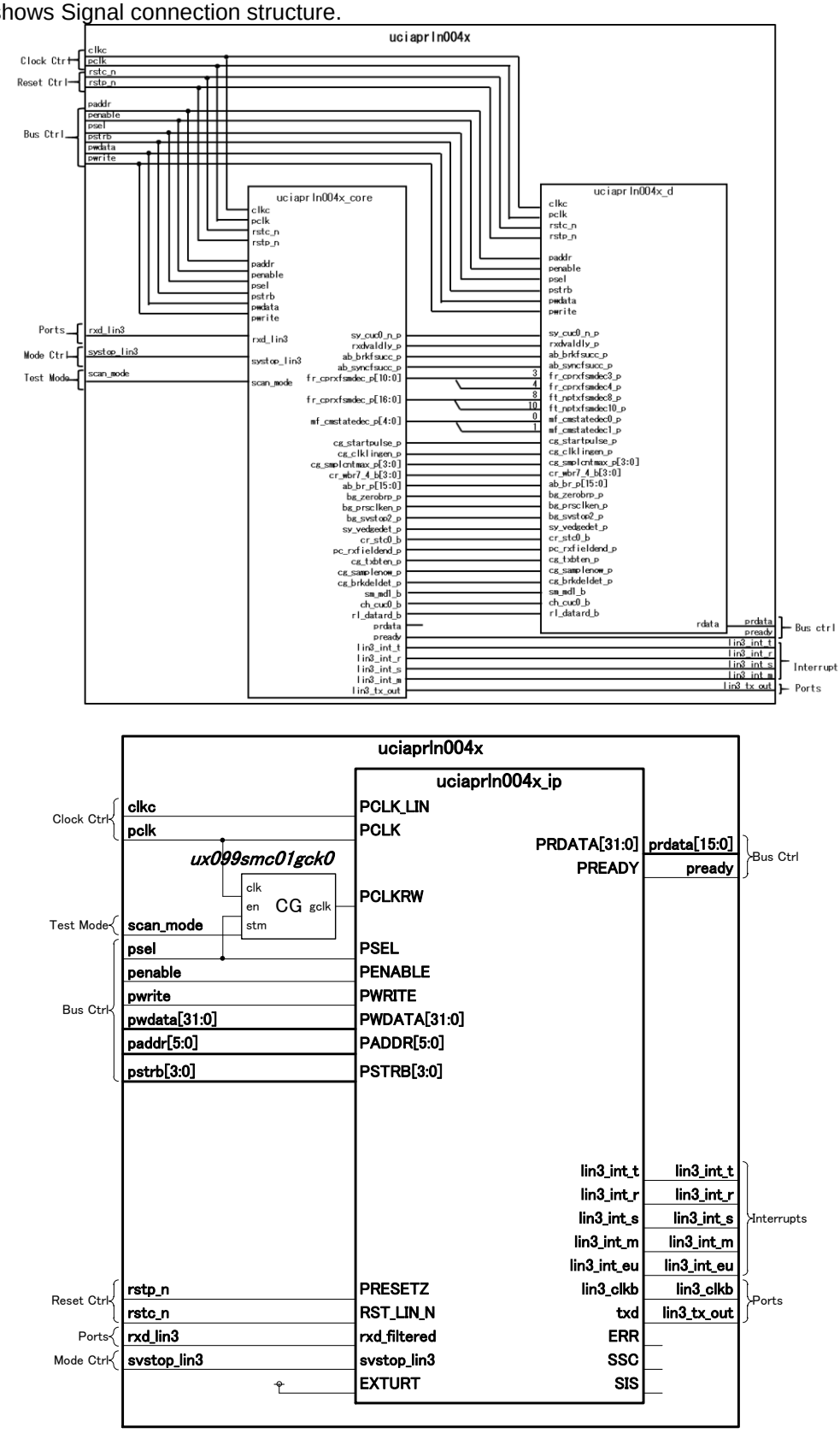


Figure 3-1: Signal connection structure (uciaprln0044)

3.11.2 Interface signals

3.11.2.1 Reset and Clock control

Table 3-2 Interface signals for Reset and Clock control

Signal name	IO	Function	Clock	Initial value	Unused handling
rstp_n	I	Asynchronous reset (Active Low) (pclk domain)	-	1'b0	1'b0
rstc_n	I	Asynchronous reset (Active Low) (clkc domain)	-	1'b0	1'b0
pclk	I	Peripheral (APB) clock)	-	-	1'b0
clkc	I	Clean clock with small clock jitter tolerance sufficient for LIN protocol communication clock	-	-	1'b0
scan_enable	I	Scan mode enable 0: Disabled 1: Enabled	-	-	1'b0
svstop_lin3	I	Supervisor enable 0: Disabled 1: Enabled	-	-	1'b0

3.11.2.1.1 Signal explanation

Table 3-3 Interface signals for Reset and Clock control description

Signal name	Description
rstp_n	If rstp_n is 1'b0, all FFs of the whole IP are reset asynchronously. It is expected that this input reset signal is released synchronously with pclk from the chip side.
rstc_n	If rstc_n is 1'b0, all FFs of the LIN engine are reset asynchronously. It is expected that this input reset signal is released synchronously with clkc from the chip side.
pclk	This signal is peripheral (APB clock).
clkc	This signal is LIN communication clock. In the case of the LIN communication clock (clkc) and the peripheral are asynchronous design: $freq_{(pclk)} \geqq freq_{(clkc)} * 2$ In the case of the LIN communication clock (clkc) and the peripheral are synchronous design: $freq_{(pclk)} = freq_{(clkc)} * n$ $n \geqq 1$, Integer number
scan_enable	Scan enable signal is used during SCAN TEST.
svstop_lin3	Supervisor enable signal is used during Supervisor mode. svstop_lin3 is connected SVSTOP.

3.11.2.1.2 Clock and Reset structure

Figure 2.2 shows the structure for clock and reset.

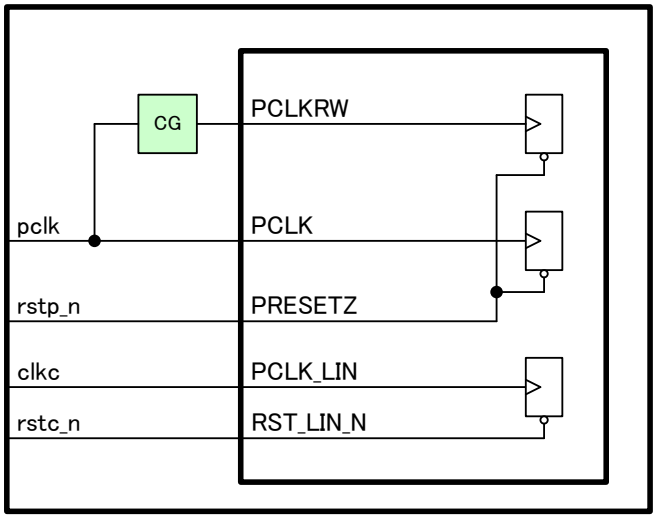


Figure 3-2: Clock and Reset structure (uciaprln0044)

3.11.2.1.1 Waveform

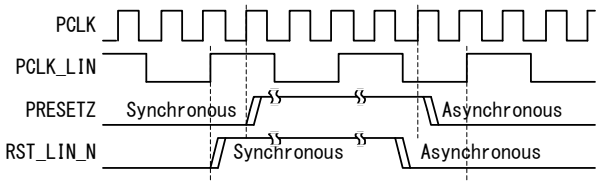


Figure 3-3: Waveform of Clock and Reset

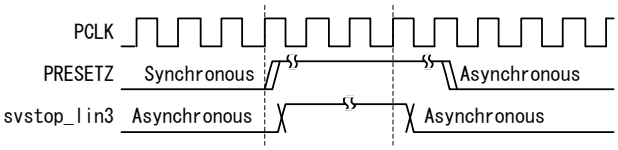


Figure 3-4: Waveform of Supervisor enable signal

3.11.2.1.2 Clock synchronization

Table 3-4 shows Clock synchronization.

Table 3-4 Clock synchronization

From \ To	pclk	pclkrw	clkc
pclk	Sync	Sync	Async
pclkrw	Sync	Sync	Async
clkc	Async	Async	Sync

3.11.2.1.3 Clock frequency

Table 3-5 shows the guaranteed clock frequency at the synthesis.

In the case of the LIN communication clock (clkc) and the peripheral are asynchronous design:

$freq_{(pclk)} \geqq freq_{(clkc)} * 2$

In the case of the LIN communication clock (clkc) and the peripheral are synchronous design:

$freq_{(pclk)} = freq_{(clkc)} * n$

$n \geqq 1$, Integer number

Designers information:

When the frequency of clkp(clk_p) is less than frequency of clkc(clk_lin) * 2, please refer to chapter 8 of the implementation instruction.

Table 3-5 Clock frequency

Clock name	Operation frequency	
	Min	Max
pclk	–	96 MHz
pclkrw	–	96 MHz
clkc	4 MHz	96 MHz

Note1: An input clock frequency is dependent on the baud rate to support. Please set up a clock frequency in less than 96MHz by the product side.

3.11.2.1.4 Baud Rate

Table 3-6 - Table 3-12 is shown the realized Baud Rate in each mode and the Baud Rate error. The tolerance of LIN Master mode is ±0.5%, the tolerance of LIN Slave mode is ±1.5%, and the tolerance of UART mode is ±1.9%. Red character is shown that the tolerance is out of the range.

Note: The tolerance of the nearest setting assumes an ideal clock (clock jitter is not considered).

Table 3-6 Baud Rate and Tolerance (LIN Master mode)

Clock frequency [MHz]	Target Baud Rate [kbps]	The nearest setting	
		Baud Rate [kbps]	Tolerance [%]
48	115.2	115.3846	0.16%
	38.4	38.4615	0.16%
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.4038	0.16%
	10.417	10.4167	0.00%
44	115.2	114.5833	**-0.54%**
	38.4	38.1944	**-0.54%**
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.7743	**-0.54%**
	2.4	2.4038	0.16%
	10.417	10.4167	0.00%
40	115.2	113.6364	**-1.36%**
	38.4	38.4615	0.16%
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.4038	0.16%
	10.417	10.4167	0.00%
36	115.2	112.5000	**-2.34%**
	38.4	38.1356	**-0.69%**
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.4038	0.16%
	10.417	10.4167	0.00%
32	115.2	117.6471	**2.12%**
	38.4	38.4615	0.16%
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.4038	0.16%
	10.417	10.4167	0.00%
30	115.2	117.1875	**1.73%**
	38.4	38.2653	-0.35%
	19.2	19.1327	-0.35%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.3916	-0.35%
	10.417	10.4167	0.00%
28	115.2	116.6667	**1.27%**
	38.4	38.0435	**-0.93%**
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.4038	0.16%
	10.417	10.4167	0.00%
24	115.2	115.3846	0.16%
	38.4	38.4615	0.16%
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.4038	0.16%
	10.417	10.4167	0.00%
20	115.2	113.6364	**-1.36%**
	38.4	37.8788	**-1.36%**
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.4038	0.16%
	10.417	10.4167	0.00%
16	115.2	111.1111	**-3.55%**
	38.4	38.4615	0.16%
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.4038	0.16%
	10.417	10.4167	0.00%
12	115.2	107.1429	**-6.99%**
	38.4	37.5000	**-2.34%**
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.4038	0.16%
	10.417	10.4167	0.00%
10	115.2	125.0000	**8.51%**
	38.4	39.0625	**1.73%**
	19.2	18.9394	**-1.36%**
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.4038	0.16%
	10.417	10.4167	0.00%
8	115.2	125.0000	**8.51%**
	38.4	38.4615	0.16%
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.4038	0.16%
	10.417	10.4167	0.00%
4	115.2	125.0000	**8.51%**
	38.4	35.7143	**-6.99%**
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.4038	0.16%
	10.417	10.4167	0.00%

Table 3-7 Baud Rate and Tolerance (LIN Slave Fixed Baud Rate mode)

Clock frequency [MHz]	Target Baud Rate [kbps]	The nearest setting	
		Baud Rate [kbps]	Tolerance [%]
48	115.2	115.3846	0.16%
	38.4	38.4615	0.16%
	19.2	19.2308	0.16%
	9.6	9.5847	-0.16%
	4.8	4.8000	0.00%
	2.4	2.4000	0.00%
	10.417	10.4167	0.00%
44	115.2	114.5833	-0.54%
	38.4	38.1944	-0.54%
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.7993	-0.01%
	2.4	2.3997	-0.01%
	10.417	10.4167	0.00%
40	115.2	113.6364	-1.36%
	38.4	38.4615	0.16%
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.7985	-0.03%
	2.4	2.3992	-0.03%
	10.417	10.4167	0.00%
36	115.2	112.5000	**-2.34%**
	38.4	38.1356	-0.69%
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.7974	-0.05%
	2.4	2.3987	-0.05%
	10.417	10.4167	0.00%
32	115.2	117.6471	**2.12%**
	38.4	38.4615	0.16%
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.7962	-0.08%
	2.4	2.4010	0.04%
	10.417	10.4167	0.00%
30	115.2	117.1875	**1.73%**
	38.4	38.2653	-0.35%
	19.2	19.1327	-0.35%
	9.6	9.6154	0.16%
	4.8	4.7954	-0.10%
	2.4	2.4008	0.03%
	10.417	10.4167	0.00%
28	115.2	116.6667	1.27%
	38.4	38.0435	-0.93%
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.7945	-0.11%
	2.4	2.4005	0.02%
	10.417	10.4167	0.00%
24	115.2	115.3846	0.16%
	38.4	38.4615	0.16%
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.7923	-0.16%
	2.4	2.4000	0.00%
	10.417	10.4167	0.00%
20	115.2	113.6364	-1.36%
	38.4	37.8788	-1.36%
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.3992	-0.03%
	10.417	10.4167	0.00%
16	115.2	111.1111	**-3.55%**
	38.4	38.4615	0.16%
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.3981	-0.08%
	10.417	10.4167	0.00%
12	115.2	107.1429	**-6.99%**
	38.4	37.5000	**-2.34%**
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.3962	-0.16%
	10.417	10.4167	0.00%
10	115.2	125.0000	**8.51%**
	38.4	39.0625	**1.73%**
	19.2	18.9394	-1.36%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.4038	0.16%
	10.417	10.4167	0.00%
8	115.2	125.0000	**8.51%**
	38.4	38.4615	0.16%
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.4038	0.16%
	10.417	10.4167	0.00%
4	115.2	125.0000	**8.51%**
	38.4	35.7143	**-6.99%**
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.8077	0.16%
	2.4	2.4038	0.16%
	10.417	10.4167	0.00%

Table 3-8 Baud rate range for LIN Slave with Auto baud rate

Prescaler clock [MHz]	4	8	10	12	16	20	24	32	40	48
Sampling per bit	4	4	4	4	4	4	4	4	4	4
Maximum baud rate [bps]	26000	53000	69000	80000	107000	115200	115200	115200	115200	115200
Minimum baud rate [bps]	1000	1200	1500	1800	2350	2950	3550	4700	5900	7050

Prescaler clock [MHz]	4	8	10	12	16	20	24	32	40	48
Sampling per bit	8	8	8	8	8	8	8	8	8	8
Maximum baud rate [bps]	13000	26000	34000	41000	53000	69000	80000	107000	115200	115200
Minimum baud rate [bps]	1000	1200	1500	1800	2350	2950	3550	4700	5900	7050

Communication clock (Slave) frequency deviation: Typ±15%
The clock deviation from the target baud rate after correction: Typ±1.5%

Table 3-9 Baud Rate and Tolerance (UART mode) (1)

Clock frequency [MHz]	Target Baud Rate [kbps]	The nearest setting	
		Baud Rate [kbps]	Tolerance [%]
48	5330	5333.3333	0.06%
	1500	1500.0000	0.00%
	1000	1000.0000	0.00%
	312.5	311.6883	-0.26%
	153.6	153.8462	0.16%
	128	128.0000	0.00%
	115.2	115.3846	0.16%
	76.8	76.9231	0.16%
	38.4	38.4000	0.00%
	31.25	31.2500	0.00%
	19.2	19.2000	0.00%
	9.6	9.6000	0.00%
	4.8	4.8000	0.00%
	2.4	2.4000	0.00%
	1.2	1.2000	0.00%
	0.6	0.6000	0.00%
	0.3	0.3000	0.00%
44	5330	5500.0000	**3.19%**
	1500	1466.6667	**-2.22%**
	1000	1000.0000	0.00%
	312.5	314.2857	0.57%
	153.6	153.8462	0.16%
	128	127.9070	-0.07%
	115.2	115.7895	0.51%
	76.8	76.9231	0.16%
	38.4	38.3944	-0.01%
	31.25	31.2500	0.00%
	19.2	19.1972	-0.01%
	9.6	9.5986	-0.01%
	4.8	4.7993	-0.01%
	2.4	2.4000	0.00%
	1.2	1.2000	0.00%
	0.6	0.6000	0.00%
	0.3	0.3000	0.00%

Clock frequency [MHz]	Target Baud Rate [kbps]	The nearest setting	
		Baud Rate [kbps]	Tolerance [%]
40	5330	5000.0000	**-6.19%**
	1500	1481.4815	-1.23%
	1000	1000.0000	0.00%
	312.5	312.5000	0.00%
	153.6	153.8462	0.16%
	128	128.2051	0.16%
	115.2	114.9425	-0.22%
	76.8	76.9231	0.16%
	38.4	38.3509	-0.13%
	31.25	31.2500	0.00%
	19.2	19.2123	0.06%
	9.6	9.5992	-0.01%
	4.8	4.8002	0.00%
	2.4	2.4000	0.00%
	1.2	1.2000	0.00%
	0.6	0.6000	0.00%
	0.3	0.3000	0.00%
36	5330	5142.8571	**-3.51%**
	1500	1500.0000	0.00%
	1000	1000.0000	0.00%
	312.5	315.7895	1.05%
	153.6	153.8462	0.16%
	128	127.6596	-0.27%
	115.2	115.3846	0.16%
	76.8	76.7591	-0.05%
	38.4	38.3795	-0.05%
	31.25	31.2500	0.00%
	19.2	19.2000	0.00%
	9.6	9.6000	0.00%
	4.8	4.8000	0.00%
	2.4	2.4000	0.00%
	1.2	1.2000	0.00%
	0.6	0.6000	0.00%
	0.3	0.3000	0.00%

Table 3-10 Baud Rate and Tolerance (UART mode) (2)

Clock frequency [MHz]	Target Baud Rate [kbps]	The nearest setting	
		Baud Rate [kbps]	Tolerance [%]
32	5330	5333.3333	0.06%
	1500	1523.8095	1.59%
	1000	1000.0000	0.00%
	312.5	313.7255	0.39%
	153.6	153.8462	0.16%
	128	128.0000	0.00%
	115.2	114.6953	-0.44%
	76.8	76.9231	0.16%
	38.4	38.4154	0.04%
	31.25	31.2500	0.00%
	19.2	19.2077	0.04%
	9.6	9.6010	0.01%
	4.8	4.8005	0.01%
	2.4	2.4002	0.01%
	1.2	1.2000	0.00%
	0.6	0.6000	0.00%
	0.3	0.3000	0.00%
30	5330	5000.0000	**-6.19%**
	1500	1500.0000	0.00%
	1000	1000.0000	0.00%
	312.5	312.5000	0.00%
	153.6	153.8462	0.16%
	128	128.2051	0.16%
	115.2	115.3846	0.16%
	76.8	76.9231	0.16%
	38.4	38.4123	0.03%
	31.25	31.2500	0.00%
	19.2	19.2061	0.03%
	9.6	9.5969	-0.03%
	4.8	4.8000	0.00%
	2.4	2.4000	0.00%
	1.2	1.2000	0.00%
	0.6	0.6000	0.00%
	0.3	0.3000	0.00%

Clock frequency [MHz]	Target Baud Rate [kbps]	The nearest setting	
		Baud Rate [kbps]	Tolerance [%]
28	5330	4666.6667	**-12.45%**
	1500	1555.5556	**3.70%**
	1000	1000.0000	0.00%
	312.5	311.1111	-0.44%
	153.6	153.8462	0.16%
	128	127.2727	-0.57%
	115.2	115.2263	0.02%
	76.8	76.9231	0.16%
	38.4	38.4088	0.02%
	31.25	31.2500	0.00%
	19.2	19.2044	0.02%
	9.6	9.6022	0.02%
	4.8	4.8011	0.02%
	2.4	2.3995	-0.02%
	1.2	1.2000	0.00%
	0.6	0.6000	0.00%
	0.3	0.3000	0.00%
24	5330	4000.0000	**-24.95%**
	1500	1500.0000	0.00%
	1000	1000.0000	0.00%
	312.5	311.6883	-0.26%
	153.6	153.8462	0.16%
	128	128.3422	0.27%
	115.2	115.3846	0.16%
	76.8	76.9231	0.16%
	38.4	38.4615	0.16%
	31.25	31.2500	0.00%
	19.2	19.2000	0.00%
	9.6	9.6000	0.00%
	4.8	4.8000	0.00%
	2.4	2.4000	0.00%
	1.2	1.2000	0.00%
	0.6	0.6000	0.00%
	0.3	0.3000	0.00%

Table 3-11 Baud Rate and Tolerance (UART mode) (3)

Clock frequency [MHz]	Target Baud Rate [kbps]	The nearest setting	
		Baud Rate [kbps]	Tolerance [%]
20	5330	3333.3333	**-37.46%**
	1500	1538.4615	**2.56%**
	1000	1000.0000	0.00%
	312.5	312.5000	0.00%
	153.6	153.8462	0.16%
	128	128.2051	0.16%
	115.2	114.9425	-0.22%
	76.8	76.9231	0.16%
	38.4	38.4615	0.16%
	31.25	31.2500	0.00%
	19.2	19.1755	-0.13%
	9.6	9.6061	0.06%
	4.8	4.7996	-0.01%
	2.4	2.4001	0.00%
	1.2	1.2000	0.00%
	0.6	0.6000	0.00%
	0.3	0.3000	0.00%
16	5330	2666.6667	**-49.97%**
	1500	1454.5455	**-3.03%**
	1000	1000.0000	0.00%
	312.5	307.6923	-1.54%
	153.6	153.8462	0.16%
	128	126.9841	-0.79%
	115.2	115.9420	0.64%
	76.8	76.9231	0.16%
	38.4	38.4615	0.16%
	31.25	31.2500	0.00%
	19.2	19.2077	0.04%
	9.6	9.6038	0.04%
	4.8	4.8005	0.01%
	2.4	2.4002	0.01%
	1.2	1.2001	0.01%
	0.6	0.6000	0.00%
	0.3	0.3000	0.00%

Clock frequency [MHz]	Target Baud Rate [kbps]	The nearest setting	
		Baud Rate [kbps]	Tolerance [%]
12	5330	2000.0000	**-62.48%**
	1500	1500.0000	0.00%
	1000	1000.0000	0.00%
	312.5	307.6923	-1.54%
	153.6	153.8462	0.16%
	128	125.0000	**-2.34%**
	115.2	115.3846	0.16%
	76.8	76.9231	0.16%
	38.4	38.4615	0.16%
	31.25	31.2500	0.00%
	19.2	19.2308	0.16%
	9.6	9.6000	0.00%
	4.8	4.8000	0.00%
	2.4	2.4000	0.00%
	1.2	1.2000	0.00%
	0.6	0.6000	0.00%
	0.3	0.3000	0.00%
10	5330	1666.6667	**-68.73%**
	1500	1428.5714	**-4.76%**
	1000	1000.0000	0.00%
	312.5	312.5000	0.00%
	153.6	153.8462	0.16%
	128	128.2051	0.16%
	115.2	113.6364	-1.36%
	76.8	76.9231	0.16%
	38.4	38.4615	0.16%
	31.25	31.2500	0.00%
	19.2	19.2308	0.16%
	9.6	9.5877	-0.13%
	4.8	4.8031	0.06%
	2.4	2.3998	-0.01%
	1.2	1.2000	0.00%
	0.6	0.6000	0.00%
	0.3	0.3000	0.00%

Table 3-12 Baud Rate and Tolerance (UART mode) (4)

Clock frequency [MHz]	Target Baud Rate [kbps]	The nearest setting	
		Baud Rate [kbps]	Tolerance [%]
8	5330	1333.3333	**-74.98%**
	1500	1333.3333	**-11.11%**
	1000	1000.0000	0.00%
	312.5	307.6923	-1.54%
	153.6	153.8462	0.16%
	128	126.9841	-0.79%
	115.2	114.2857	-0.79%
	76.8	76.9231	0.16%
	38.4	38.4615	0.16%
	31.25	31.2500	0.00%
	19.2	19.2308	0.16%
	9.6	9.6038	0.04%
	4.8	4.8019	0.04%
	2.4	2.4002	0.01%
	1.2	1.2001	0.01%
	0.6	0.6001	0.01%
	0.3	0.3000	0.00%

Clock frequency [MHz]	Target Baud Rate [kbps]	The nearest setting	
		Baud Rate [kbps]	Tolerance [%]
4	5330	666.6667	**-87.49%**
	1500	666.6667	**-55.56%**
	1000	666.6667	**-33.33%**
	312.5	307.6923	-1.54%
	153.6	153.8462	0.16%
	128	125.0000	**-2.34%**
	115.2	114.2857	-0.79%
	76.8	76.9231	0.16%
	38.4	38.4615	0.16%
	31.25	31.2500	0.00%
	19.2	19.2308	0.16%
	9.6	9.6154	0.16%
	4.8	4.8019	0.04%
	2.4	2.4010	0.04%
	1.2	1.2001	0.01%
	0.6	0.6001	0.01%
	0.3	0.3000	0.01%

3.11.2.1.5 Supervisor mode

The Baud Rate generator which had it built-in is stopped to read the internal state when LIN is entered into the Supervisor mode (svstop_lin3=1'b1). Frame transmission complete flag is cleared automatically by the transmission start bit for the next frame is set.

3.11.2.2 Bus interface

Table 3-13 shows the Bus interface signals.
APB ready signal (pready) is always fixed High.

Table 3-13 Bus interface signals

Signal name	IO	Function	Clock	Initial value	Unused handling
psel	I	APB select signal 0: Not selected 1: Selected	pclk	-	1'b0
paddr[5:0]	I	APB address Bus	pclk	-	6'b000000
penable	I	APB enable signal 0: cycle0 1: second and subsequent cycle	pclk	-	1'b0
pwrite	I	APB write signal 0: read 1: write	pclk	-	1'b0
pstrb[3:0]	I	APB Byte enable signal	pclk	-	4'b0000
pwdata[31:0]	I	APB Input Data bus	pclk	-	32'h00000000
prdata[31:0]	O	APB Output Data bus	pclk	32'h00000000	OPEN
pready	O	APB ready signal	-	1'b1	OPEN

3.11.2.2.1 Signal explanation

Table 3-14 Bus interface signals description

Signal name	Description
psel	SFR of the IP is accessed when APB select bit (psel) is set to 1'b1.
paddr[5:0]	Address decode is executed in IP, and SFR read/write access is executed.
penable	APB enable signal (penable) is asserted in access available period when peripheral IP is accessed.
pwrite	APB write signal (pwrite) is asserted in write access. The operation is read access or none operation, if APB write signal (pwrite) is 1'b0. The operation is write access, if APB write signal (pwrite) is 1'b1.
pstrb[3:0]	pstrb[0] controls byte writes for the address 4n, pstrb[1] controls byte write for the address (4n+1), pstrb[2] controls byte write for the address (4n+2), and pstrb[3] controls byte write for the address (4n+3). The byte write access is able to be executed, if APB Byte enable signal (pstrb) is 1'b1.
pwdata[31:0]	APB Input Data bus (pwdata) is SFR write data to the peripheral IP.
prdata[31:0]	APB Output Data bus (prdata) is SFR read data. APB Output Data bus (prdata) outputs the read data when IP is executed read access. APB Output Data bus (prdata) is holds the read data until the next read access or reset operation.
pready	APB ready signal (pready) always outputs 1'b1.

3.11.2.2.2 Waveform

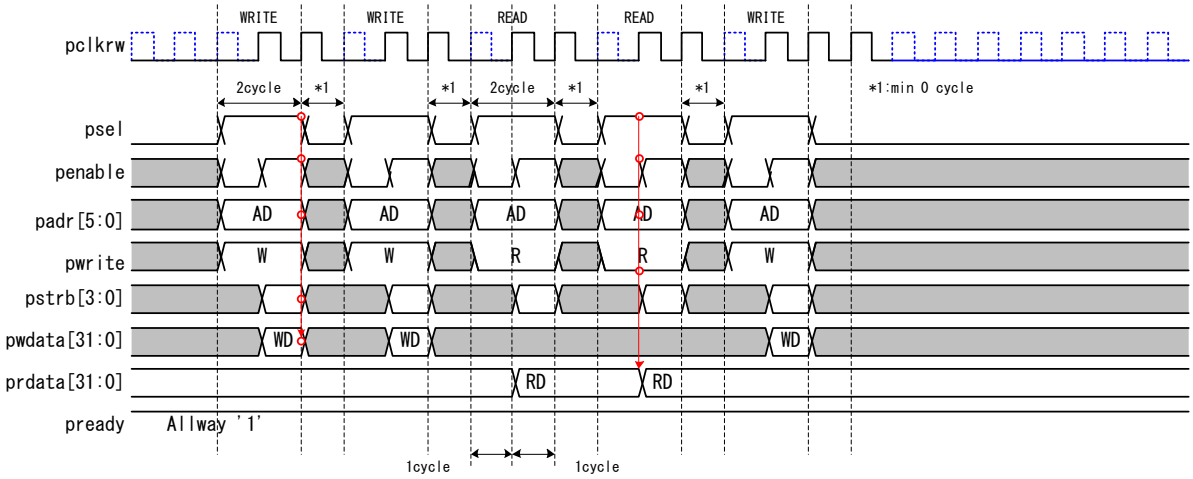


Figure 3-5: Waveform of Bus Interface for uciaprln004x / uciaprln004x

3.11.2.3 Interrupt interface

Table 3-15 shows the interrupt interface signals. All interrupt signals are outputted by High pulse signal. Therefore, the interrupt control block should detect the rising edge.

Table 3-15 Interrupt interface signals

Signal name	IO	Function	Clock	Initial value	Unused handling
lin3_int_t	O	Transmission interrupt (High pulse)	pclk	1'b0	OPEN
lin3_int_r	O	Reception interrupt (High pulse)	pclk	1'b0	OPEN
lin3_int_s	O	Status interrupt (High pulse)	pclk	1'b0	OPEN
lin3_int_m	O	RLIN2 compatible interrupt (High pulse)	pclk	1'b0	OPEN
lin3_int_eu	O	Extended UART interrupt (High pulse)	pclk	1'b0	OPEN

3.11.2.3.1 Signal explanation

Table 3-16 Interrupt interface signals description

Signal name	Description
lin3_int_t	The lin3_int_t signal outputs the transmission interrupt request by the High pulse.
lin3_int_r	The lin3_int_r signal outputs the reception interrupt request by the High pulse.
lin3_int_s	The lin3_int_r signal outputs the status interrupt request by the High pulse.
lin3_int_m	The lin3_int_m signal outputs the RLIN2 compatible interrupt request by the High pulse.
lin3_int_eu	The lin3_int_eu signal outputs the Extended UART interrupt request by the High pulse.

3.11.2.3.2 Interrupt signal and operation mode

Table 3-17 shows the relation of the interrupt signal and the operation mode. The unused interrupts are fixed to Low by the operation mode of RLIN3.

Table 3-17 Relation of the interrupt and the operation mode

Interrupt signal name	Operation mode					
	LIN Master mode		LIN Slave mode		UART mode	Extended UART mode
	RLIN2 compatible	RLIN2 not compatible	RLIN2 compatible	RLIN2 not compatible		
lin3_int_t	1'b0	Output	1'b0	Output	Output	Output
lin3_int_r	1'b0	Output	1'b0	Output	Output	Output
lin3_int_s	1'b0	Output	1'b0	Output	Output	Output
lin3_int_m	Output	1'b0	Output	1'b0	1'b0	1'b0
lin3_int_eu	1'b0	1'b0	1'b0	1'b0	1'b0	Output

3.11.2.3.1 Interrupt signal waveform

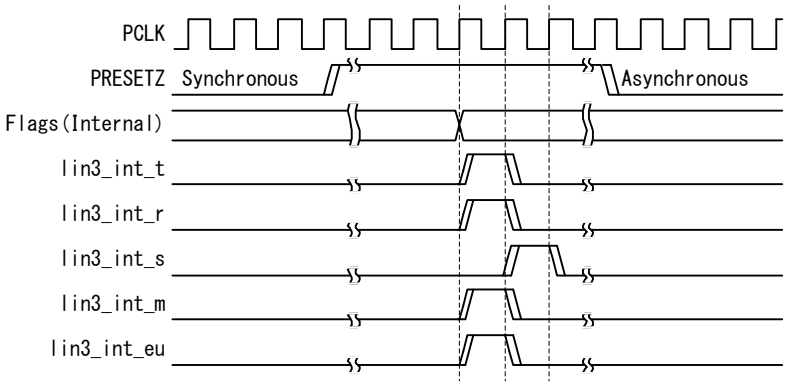


Figure 3-6: Waveform of Interrupt signal

3.11.2.4 Port interface

Table 3-19 shows the port interface signals. Reception data signal (rxd_lin3) and Transmission data signal (lin3_tx_out) are Low active signals. Reception data signal (rxd_lin3) should be inputted High level when LIN is not communicating. Transmission data signal (lin3_tx_out) outputs High level when LIN is not communicating.

Table 3-18 Port interface signals

Signal name	IO	Function	Clock	Initial value	Unused handling
rxd_lin3	I	Reception data signal	clkc	-	1'b1
lin3_tx_out	O	Transmission data signal	clkc	1'b1	OPEN
lin3_clkb	O	Baud rate clock signal	clkc	1'b0	OPEN

3.11.2.4.1 Signal explanation

Table 3-19 Port interface signals description

Signal name	Description
rxd_lin3	The rxd_lin3 is reception data signal. This signal should be inputted High level when LIN is not communicating.
lin3_tx_out	The lin3_tx_out is transmission data signal. This signal outputs High level when LIN is not communicating.
lin3_clkb	The lin3_clkb is baud rate clock signal. This signal is supported in Extended UART mode.

3.11.2.4.1 Waveform

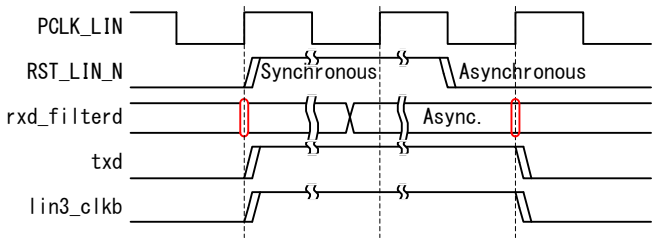


Figure 3-7: Waveform of Port interface signal

4 SFR OVERVIEW

The addresses given in this specification are relative to the Start address of the RLIN Module referred to as "Offset Address" in the SFR Overview table. The "Values after reset" refers to the status of the registers due to microcontroller's HW reset.

Most of the registers in the RLIN3 Module have a width of 8 bits. Hence, the "Access Size" column shows the value 8 for these registers. It is possible to access 2 registers with a 16-bit access and 4 registers together with a 32-bit access.

However, there are 4 registers that have a width of 16-bits. The "Access Size" column shows the value 16 for these registers. Please see the register description for these registers for details regarding Register access options.

Following naming convention is used on the following sections:

RST Mode -> LMST [0] is 0
IDLE Mode -> LMST[0] is 1 and LTRC[0] is 0
Operation Mode ->

- LTRC[0] is 1 for LIN Master and LIN Slave operation.
- Transmission or Reception in progress for UART mode.

Initial Value -> Initial value after CPU reset
R -> Read Access (Write not possible, h/w protection)
R/W -> Read & Write access
W0C -> Write Zero(0) to Clear
R0 -> Read Zero(0)
W0 -> Write only Zero (0). Not allowed to write One (1). (s/w Restriction)
W1 -> Write only One (1). Not available to write Zero (0). (s/w Restriction)

Don't Care for configuration registers -> Users shall set "initial value" to the register bit.
Don't Care for status registers -> Users shall ignore the register bit

Response Group Transmission -> Number of data bytes in a Response is more than or equal to 9 and hence the data is transmitted in multiple data groups. Size of each data group is between 1 and 8 bytes.
Response Group Reception -> Number of data bytes in a Response is more than or equal to 9 and hence the data is received in multiple data groups. Size of each data group is between 1 and 8 bytes.

Note 1: On software reset (writing 00 to LCUC[1:0]), all the registers will retain the existing value except the status registers & transmission control register i.e. LST, LEST, LUOE & LTRC.
Note 2: Words "should not" or "should" or "prohibited" indicates user restriction.
Note 3: Words "can not" or "can only" indicates H/W protection.

Table 4-1: SFR Overview table

Register Name	Symbol	Values after Reset	Offset Address	Access Size
Reserved	----	----	0000h	----
LIN Wake-up Baud Rate selector register	LWBR	00h	0001h	8
LIN / UART Baud rate Prescaler 0 register	LBRP0	00h	0002h	8, 16 *1
LIN / UART Baud rate Prescaler 1 register	LBRP1	00h	0003h	8, 16 *1
LIN Self Test Control register	LSTC	00h	0004h	8
Reserved	----	----	0005h, 0007h	----
LIN / UART Mode register	LMD	00h	0008h	8
LIN Break Field Configuration register / UART Configuration Register 1	LBFC	00h	0009h	8
LIN / UART Space Configuration register	LSC	00h	000Ah	8
LIN Wake-up configuration register	LWUP	00h	000Bh	8
LIN Interrupt Enable register	LIE	00h	000Ch	8
LIN / UART Error Detection Enable register	LEDE	00h	000Dh	8
LIN / UART Control Register	LCUC	00h	000Eh	8
Reserved	----	----	000Fh	----
LIN / UART Transmission Control register	LTRC	00h	0010h	8
LIN / UART Mode Status register	LMST	00h	0011h	8
LIN / UART Status register	LST	00h	0012h	8
LIN / UART Error Status register	LEST	00h	0013h	8
LIN / UART Data Field Configuration register	LDFC	00h	0014h	8
LIN / UART Identifier Buffer register	LIDB	00h	0015h	8
LIN Checksum Buffer register	LCBR	00h	0016h	8
UART Data Buffer 0 register	LUDB0	00h	0017h	8
LIN / UART Data Buffer 1 register	LDBR1	00h	0018h	8
LIN / UART Data Buffer 2 register	LDBR2	00h	0019h	8
LIN / UART Data Buffer 3 register	LDBR3	00h	001Ah	8
LIN / UART Data Buffer 4 register	LDBR4	00h	001Bh	8
LIN / UART Data Buffer 5 register	LDBR5	00h	001Ch	8
LIN / UART Data Buffer 6 register	LDBR6	00h	001Dh	8
LIN / UART Data Buffer 7 register	LDBR7	00h	001Eh	8
LIN / UART Data Buffer 8 register	LDBR8	00h	001Fh	8
UART Operation Enable Register	LUOER	00h	0020h	8
UART Option Register1	LUOR1	00h	0021h	8
UART Option Register2	LUOR2	01h	0022h	8
UART Transmit start Delay Control Register	LUTDCR	10h	0023h	8
UART 7bit / 8bit / 9bit Transmit Data Register	LUTDR	0000h	0024h, 0025h	8, 16
UART 7bit / 8bit / 9bit Receive Data Register	LURDR	0000h	0026h, 0027h	8, 16
UART 7bit / 8bit / 9bit Wait Transmit Data Register	LUWTDR	0000h	0028h, 0029h	8, 16
UART 7bit / 8bit / 9bit Receive Data Register for Emulation	LURDE	0000h	002Ah, 002Bh	8, 16
Reserved	----	----	002Ch to 002Fh	----
LIN slave Break/Sync field Status register	LBSS	00h	0030h	8
Reserved	----	----	0031h to 0033h	----
LIN slave Response Space Status register	LRSS	00h	0034h	8
Reserved	----	----	0035h to 003Fh	----

Writing to the address locations marked as "Reserved" in the SFR Overview Table has no influence on the module. The value read from these locations is always "00h".

*1: Users are able to write to LBRP0 and LBRP1 with 16bits access in LIN Slave mode and UART mode.

4.1 LIN WAKE-UP BAUD RATE SELECTOR REGISTER (LWBR)

Address: 0001h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**NSPB[3:0]**				**LPRS[2:0]**			**LWBR0**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R/W Note 2	R/W Note 2	R/W Note 2	R/W Note 2	R/W	R/W	R/W	R/W Note 1
LIN Master	**IDLE Mode**	R	R	R	R	R	R	R	R
	Operation Mode	R	R	R	R	R	R	R	R
LIN Slave	**IDLE Mode**	R	R	R	R	R	R	R	R
	Operation Mode	R	R	R	R	R	R	R	R
UART	**IDLE Mode**	R	R	R	R	R	R	R	R
	Operation Mode	R	R	R	R	R	R	R	R

Bit	Symbol	Bit Name	Register Function
b[0]	LWBR0	Wake-up baud rate select mode bit	0: Baud rate clock is based on System Clock configuration in Wake-up mode 1: Baud rate clock source is automatically set to "fa" in Wake-up mode.
b[3:1]	LPRS	Prescaler clock select bit	These bits configure the prescaler "000": 1/1 "001": 1/2 "010": 1/4 "011": 1/8 "100": 1/16 "101": 1/32 "110": 1/64 "111": 1/128
b[7:4]	NSPB	Number of Samples per bit	These bits configure the value for number of samples in 1 Bit time period. "0000": 16 samples per bit "0001": Prohibited "0010": Prohibited "0011": 4 samples per bit "0100": Prohibited "0101": 6 samples per bit "0110": 7 samples per bit "0111": 8 samples per bit "1000": 9 samples per bit "1001": 10 samples per bit "1010": 11 samples per bit "1011": 12 samples per bit "1100": 13 samples per bit "1101": 14 samples per bit "1110": 15 samples per bit "1111": 16 samples per bit

LWBR.LWBR0 Wake-up Baud Rate select mode bit

Users can not write to this bit if LMST[0] bit is "1".

This bit is used to control the automatic baud rate clock selection function in Wake-up mode.

Note 1: Users should write "0" to this bit if the RLIN3 module is expected to transmit or receive Wake-up signal as defined in LIN Specification version 1.3 in LIN Master mode.
Users should write "0" to this bit if the RLIN3 module is configured in LIN Slave mode.
This register bit is "Don't Care" in UART mode.

Refer to Section 7.2 for details related to Baud rate generation logic for "fa" settings.

LWBR.LPRS[2:0] Prescaler clock select bit

Users can not write to this bit if LMST[0] bit is "1".

These bits are used to configure the prescaler clock.

Note 2: Set to 4 to 48MHz the clock (prescaler clock) that has been divided by using a prescaler in LIN Slave mode with Auto baud rate.

LWBR.NSPB[3:0] Number of Samples per bit

Users can not write to this bit if LMST[0] bit is "1".

These bits are used to configure the number of samples in 1 Bit time period

Note 3: In LIN Master mode and LIN Slave mode with Fixed baud rate, the number of samples per bit shall be fixed to 16 samples per bit (NSPB[3:0] = "0000b").
In LIN Slave mode with Auto Baud rate detection, the number of samples per bit shall be fixed to 4 (NSPB[3:0] = "0011b) or 8 samples per bit (NSPB[3:0] = "0111b").
In UART mode, the configured value shall be more than or equal to 6 samples per bit (NSPB[3:0] = "0101b").

4.2 LIN BAUD RATE PRESCALER0/UART BAUD RATE PRESCALER0 (LBRP0)

4.2.1 LIN Master mode

Address: 0002h									
Bit		b7	b6	b5	b4	b3	b2	b1	b0
Bit Symbol		LBRP0[7:0]							
Initial Value		0	0	0	0	0	0	0	0
RST Mode		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LIN Master	IDLE Mode	R	R	R	R	R	R	R	R
	Operation Mode	R	R	R	R	R	R	R	R

Bit	Symbol	Bit Name	Register Function
b[7:0]	LBRP0	BRP0 Division Ratio	Selectable value: 00h ~ FFh

LBRP0.LBRP0 [7:0] BRP0 Division Ratio

Users can not write to these register bits if LMST[0] bit is "1.
The value in this register is used to control the "fa", "fb" and "fc" baud rate source clock frequencies.

Refer to Section 7.2 for details related to Baud rate generation logic.

4.2.2 LIN Slave mode or UART mode

Address: 0002h									
Bit		b7	b6	b5	b4	b3	b2	b1	b0
Bit Symbol		BRP[7:0]							
Initial Value		0	0	0	0	0	0	0	0
RST Mode		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LIN Slave	IDLE Mode	R	R	R	R	R	R	R	R
	Operation Mode	R	R	R	R	R	R	R	R
UART	IDLE Mode	R	R	R	R	R	R	R	R
	Operation Mode	R	R	R	R	R	R	R	R

Bit	Symbol	Bit Name	Register Function
b[7:0]	BRP[7:0]	Frequency Division Value	The frequency division value for the BRP counter.

LBRP0.BRP [7:0] Frequency Division Value

Users can not write to these register bits if LMST[0] bit is "1".
These are the lower 8 bits [7:0] of the 16-bit prescaler value. The value in this register is used to control the "fa" baud rate source clock frequency.
The "fb", "fc" and "fd" clock sources shall not be used for LIN Slave mode or UART mode.

Refer to Section 7.2 for details related to Baud rate generation logic.
Note 1: Users are able to write to LBRP0 and LBRP1 with 16bits access in LIN Slave mode and UART mode.

4.3 LIN BAUD RATE PRESCALER1/UART BAUD RATE PRESCALER1 (LBRP1)

4.3.1 LIN Master mode

Address: 0003h									
Bit		b7	b6	b5	b4	b3	b2	b1	b0
Bit Symbol		LBRP1[7:0]							
Initial Value		0	0	0	0	0	0	0	0
RST Mode		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LIN Master	IDLE Mode	R	R	R	R	R	R	R	R
	Operation Mode	R	R	R	R	R	R	R	R

Bit	Symbol	Bit Name	Register Function
b[7:0]	LBRP1	BRP1 Division Ratio	Selectable value: 00h ~ FFh

LBRP1.LBRP1 [7:0] BRP1 Division Ratio

Users can not write to these register bits if LMST[0] bit is "1".

The value in this register is used to control the "fd" baud rate source clock frequency.

Refer to Section 7.2 for details related to Baud rate generation logic.

4.3.2 LIN Slave mode or UART mode

Address: 0003h									
Bit		b7	b6	b5	b4	b3	b2	b1	b0
Bit Symbol		BRP[15:8]							
Initial Value		0	0	0	0	0	0	0	0
RST Mode		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LIN Slave	IDLE Mode	R	R	R	R	R	R	R	R
	Operation Mode	R	R	R	R	R	R	R	R
UART	IDLE Mode	R	R	R	R	R	R	R	R
	Operation Mode	R	R	R	R	R	R	R	R

Bit	Symbol	Bit Name	Register Function
b[7:0]	BRP[15:8]	Frequency Division Value	The frequency division value for the BRP counter.

LBRP1.BRP [15:8] Frequency Division Value

Users can not write to these register bits if LMST[0] bit is "1".

These are the upper 8 bits [15:8] of the 16-bit prescaler value. The value in this register is used to control the "fa" baud rate source clock frequency.
The "fb", "fc" and "fd" clock sources shall not be used for LIN Slave mode or UART mode.

Refer to Section 7.2 for details related to Baud rate generation logic.
Note 1: Users are able to write to LBRP0 and LBRP1 with 16bits access in LIN Slave mode and UART mode.

4.4 LIN SELF TEST CONTROL REGISTER (LSTC)

Address: 0004h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**LSFWC**	**LSTME[5:0]**						**LSTM**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R/W*	W/R0	W/R0	W/R0	W/R0	W/R0	W/R0	R/W*
LIN Master	**IDLE Mode**	R	R0	R0	R0	R0	R0	R0	R
	Operation Mode	R	R0	R0	R0	R0	R0	R0	R
LIN Slave	**IDLE Mode**	R	R0	R0	R0	R0	R0	R0	R
	Operation Mode	R	R0	R0	R0	R0	R0	R0	R
UART	**IDLE Mode**	R	R0	R0	R0	R0	R0	R0	R
	Operation Mode	R	R0	R0	R0	R0	R0	R0	R

* This bit can not be set unless the correct "unlock key sequence" is written to this register. This bit is cleared when RLIN3 module is transitioning to the reset mode.

Bit	Symbol	Bit Name	Register Function
b[0]	LSTM	Self test mode bit	0: Self Test mode disabled 1: Self Test mode enabled
b[6:1]	LSTME	Self test mode entry key bits	The test mode key values for configuring the RLIN3 module in Test mode.
b[7]	LSFWC	Status Flag write control bit	0: Status flag write control is disabled 1: Status flag write control is enabled

LSTC.LSTM Self test mode bit

Users can not write to this bit if LMST[0] bit is "1". This bit can not be set unless the correct "unlock key sequence" is written to this register.

This bit is used to configure the RLIN3 module into self test mode.
Refer to Section 7.14 for details of the self-test mode.

This bit is cleared when the RLIN3 module is transitioning to the reset mode.

Note 1: Users shall not set this bit to "1" in UART mode.

LSTC.LSTME[5:0] Self test mode entry key bits

Users can not write to these bits if LMST[0] bit is "1".
These bits are always read as 0.

Users are expected to write the Test mode Key sequence values to these bits. Refer to section 7.14.1 for details how to enter the Test mode Key.

LSTC.LSFWC Status flag write control bit

Users can not write to this bit if LMST[0] bit is "1". This bit can not be set unless the correct "unlock key sequence" is written to this register.

This bit is used to configure the Status flag write control test mode.
Refer to Section 7.15 for details of the Status flag write control mode operation.

This bit is cleared when the RLIN3 module is transitioning to the reset mode.

4.5 LIN MODE REGISTER/UART MODE REGISTER (LMD)

Address: 0008h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**EUMS**	**-**	**LRDNFS**	**LIOS**	**LCKS[1:0]**		**LMD[1:0]**	
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R/W	R0/W0	R/W	R/W	R/W	R/W	R/W	R/W
LIN Master	**IDLE Mode**	R	R0/W0	R	R	R	R	R	R
	Operation Mode	R	R0/W0	R	R	R	R	R	R
LIN Slave	**IDLE Mode**	R	R0/W0	R	R	R	R	R	R
	Operation Mode	R	R0/W0	R	R	R	R	R	R
UART	**IDLE Mode**	R	R0/W0	R	R	R	R	R	R
	Operation Mode	R	R0/W0	R	R	R	R	R	R

Bit	Symbol	Bit Name	Register Function
b[1:0]	LMD	LIN / UART Mode Select Bits	00: LIN Master mode 01: UART mode 10: LIN Slave mode with automatic baud rate detection 11: LIN Slave mode with fixed baud rate
b[3:2]	LCKS	LIN / UART System Clock Select Bits	00: fa 01: fb 10: fc 11: fd
b[4]	LIOS	LIN Interrupt Output Select Bit	0: Module generates 1 interrupt signal 1: Module generates 3 interrupt signals
b[5]	LRDNFS	LIN / UART Receive Data Noise Filter Select Bit	0: 3-bit majority voting logic for sampling RX data is enabled. 1: 3-bit majority voting logic for sampling RX data is disabled.
b[6]	-	Reserved	This bit is always read as 0. The write value should always be 0.
b[7]	EUMS	Extended UART mode select Bit	0: Extended UART mode disabled 1: Extended UART mode enabled

LMD.LMD[1:0] LIN / UART Mode Select Bits

Users can not write to these bits if LMST[0] bit is "1".

These bits configure the RLIN3 module in the RST mode.

LMD.LCKS[1:0] LIN / UART System Clock Select Bits

Users can not write to these bits if LMST[0] bit is "1".

These bits select the appropriate clock source for baud rate generation.
Refer to section 7.2 for details of baud rate generation logic.

Note: Users should not set either of these bits to "1" in LIN Slave mode and UART mode.

LMD. LIOS LIN Interrupt Output Select Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the Interrupt Output generation for LIN mode operation
Refer to Section 7.7.1 for details about Interrupt outputs.

Note 1: Users should not set this bit to "1" in UART mode.

LMD. LRDNFS LIN / UART Receive Data Noise Filter Select Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the use of Receive Data Noise filter.

The prescaler clock is used for the Receive Data Noise filter.
Refer to Section 7.4.3 for details about Receive Data Noise filter.

LMD.EUMS Extended UART mode select Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the use of Extended UART mode functions.

Note 1: Users should not set this bit to "1" in LIN mode.

4.6 LIN BREAK FIELD CONFIGURATION REGISTER/UART CONFIGURATION REGISTER1 (LBFC)

4.6.1 LIN Master mode

Address: 0009h								
Bit	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol	**-**	**-**	**BDT[1:0]**		**BLT[3:0]**			
Initial Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode	R0/W0	R/W	R/W	R/W	R/W	R/W	R/W	R/W
IDLE Mode	R0/W0	R	R	R	R	R	R	R
Operation Mode	R0/W0	R	R	R	R	R	R	R

Bit	Symbol	Bit Name	Register Function
b[3:0]	BLT	LIN Break Low Width Select Bits	0h = Break Low width is 13 Tbits 1h = Break Low width is 14 Tbits : : : : : Fh = Break Low width is 28 Tbits
b[5:4]	BDT	LIN Break Delimiter Width Select Bits	00: Break Delimiter width is 1 Tbit 01: Break Delimiter width is 2 Tbits 10: Break Delimiter width is 3 Tbits 11: Break Delimiter width is 4 Tbits
b[7:6]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LBFC.BLT[3:0] LIN Break Low Width Select Bits

Users can not write to these bits if LMST[0] bit is "1".

These bits control the width of the Break Low transmitted by the RLIN3 module in LIN Master mode.

Note 1: Timeout error (if enabled) in LIN Master mode might occur if large values are set for Break Low width, Break Del width, IBHS and IBS bits e.g.: In the case of the following setting, frame timeout error occurs. Break Low > 23 Tbits, Break Del = 4 Tbits, Response Space Width = 7 Tbits, IBS = 3 Tbits

LBFC.BDT[1:0] LIN Break Delimiter Width Select Bits

Users can not write to these bits if LMST[0] bit is "1".

These bits control the width of the Break Delimiter transmitted by the RLIN3 module in LIN Master mode.

Note 1: Timeout error (if enabled) in LIN Master mode might occur if large values are set for Break Low width, Break Del width, IBHS and IBS bits e.g.: In the case of the following setting, frame timeout error occurs. Break Low > 23 Tbits, Break Del = 4 Tbits, Response Space Width = 7 Tbits, IBS = 3 Tbits

LBFC[7:6] This bit is don't care in LIN Master mode

4.6.2 LIN Slave mode

Address: 0009h								
Bit	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**LBLT**
Initial Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode	R0/W0	R/W	R/W	R/W	R/W	R/W	R/W	R/W
IDLE Mode	R0/W0	R	R	R	R	R	R	R
Operation Mode	R0/W0	R	R	R	R	R	R	R

Bit	Symbol	Bit Name	Register Function
b[0]	LBLT	LIN Break Low Width Select Bit	For LMD.LMD = 10, auto baud rate LIN Slave mode 0 = Break Low width is 10 Tbits 1 = Break Low width is 11 Tbits For LMD.LMD = 11, fixed baud rate LIN Slave mode 0 = Break Low width is 9.5 Tbits 1 = Break Low width is 10.5 Tbits
b[7:1]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LBFC.LBLT LIN Break Low Width Select Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit selects the width for successful Break Low detection by the RLIN3 module in LIN Slave mode.
When LMD.LMD is "10" (automatic baud rate detection), the width for successful Break Low detection can only be configured between 10 Tbits (LBFC.LBLT = "0b") or 11 Tbits (LBFC.LBLT = "1b").
When LMD.LMD is "11" (fixed baud rate), the width for successful Break Low detection can only be configured between 9.5 Tbits (LBFC.LBLT = "0b") or 10.5 Tbits (LBFC.LBLT = "1b").

LBFC[7:1] These bits are don't care for LIN Slave mode

4.6.3 UART mode

Address: 0009h								
Bit	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol	**-**	**UTPS**	**URPS**	**UPS[1:0]**		**USBLS**	**UBOS**	**UBLS**
Initial Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode	R0/W0	R/W	R/W	R/W	R/W	R/W	R/W	R/W
IDLE Mode	R0/W0	R	R	R	R	R	R	R
Operation Mode	R0/W0	R	R	R	R	R	R	R

Bit	Symbol	Bit Name	Register Function
b[0]	UBLS	UART Bit Length Select bit	0: UART 8-bit communication 1: UART 7-bit communication
b[1]	UBOS	UART Bit Order Select bit	0: LSB first 1: MSB first
b[2]	USBLS	UART Stop Bit Length Select bit	0: Stop Bit 1 bit 1: Stop Bit 2 bits
b[4:3]	UPS	UART Parity Select bits	00: Parity Disabled 01: Even Parity 10: 0 Parity 11: Odd Parity
b[5]	URPS	UART Rx Polarity Switch bit	0: Without inversion 1: With inversion
b[6]	UTPS	UART Tx Polarity Switch bit	0: Without inversion 1: With inversion
b[7]	-	Reserved	This bit is always read as 0. The write value should always be 0.

LBFC.UBLS UART Bit Length Select bit

Users can not write to this bit if LMST[0] bit is "1".

This bit selects the bit length during UART communication.

Note 1: When UART Expansion bit is enabled, the UART bit length is fixed to 9. In this case, the configuration value for the UART bit Length select bit is "Don't Care".

LBFC.UBOS UART Bit Order Select bit

Users can not write to this bit if LMST[0] bit is "1".

This bit selects the order of data bits during UART communication.

LBFC.USBLS UART Stop bit length Select bit

Users can not write to this bit if LMST[0] bit is "1".

This bit selects the number of STOP bits during UART Tx communication.

LBFC.UPS[1:0] UART Parity Select bits

Users can not write to these bits if LMST[0] bit is "1".

These bits select the Parity type during UART communication.

1. **Even parity**
   - **a.** Transmission
     Parity bit is set to "1" when the number of "1s" is odd in transmission. And parity bit is set to "0" when the number of "1" is even in transmission. By this rule, the number of "1" included in transmission data and parity bit is controlled to become even.
   - **b.** Reception
     The number of "1s" included in reception data and parity bit is counted. And parity error occurs, if the number of "1" is odd.
2. **Odd parity**
   - **a.** Transmission
     The number of "1s" included in transmission data and parity bit is controlled to become odd.
   - **b.** Reception
     The number of "1s" included in reception data and parity bit is counted. And parity error occurs, if the number of "1s" is even.
3. **0 parity**
   - **a.** Transmission
     Parity bit is set to "0" without depending on the transmission data.
   - **b.** Reception
     The detecting of parity bit is not executed. Therefore, parity error doesn't occur.
4. **Disable parity**
   - **a.** Transmission
     Parity bit is not appended to transmission data.
   - **b.** Reception
     Reception operation is executed without process of parity bit. Parity error doesn't occur because there is no parity bit.

LBFC.URPS UART Rx Polarity Switch bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the inversion of reception data bits in UART mode.

All of the UART reception (data, start/stop/parity-bit and idle) will be inverted when inversion is enabled.

Users should set UTPS and URPS to the same value when half duplex operation is required.

Designers information:
If this bit is changed, the reception is possible after 2 prescaler clock cycles.

LBFC.UTPS UART Tx Polarity Switch bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the inversion of transmission data bits in UART mode.

All of the UART transmission (data, start/stop/parity-bit and idle) will be inverted when inversion is enabled.

Users should set UTPS and URPS to the same value when half duplex operation is required.

4.7 LIN / UART SPACE CONFIGURATION REGISTER (LSC)

Address: 000Ah									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**-**	**-**	**IBS[1:0]** Note 2		**-**	**IBHS[2:0]** Note 1		
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R0/W0	R0/W0	R/W	R/W	R0/W0	R/W	R/W	R/W
LIN Master	**IDLE Mode**	R0/W0	R0/W0	R	R	R0/W0	R	R	R
	Operation Mode	R0/W0	R0/W0	R	R	R0/W0	R	R	R
LIN Slave	**IDLE Mode**	R0/W0	R0/W0	R	R	R0/W0	R	R	R
	Operation Mode	R0/W0	R0/W0	R	R	R0/W0	R	R	R
UART	**IDLE Mode**	R0/W0	R0/W0	R	R	R0/W0	R	R	R
	Operation Mode	R0/W0	R0/W0	R	R	R0/W0	R	R	R

Bit	Symbol	Bit Name	Register Function
b[2:0]	IBHS	Inter-byte Header Space and Response Space Select Bits	0h: 0 Tbits 1h: 1 Tbit 2h: 2 Tbits 3h: 3 Tbits 4h: 4 Tbits 5h: 5 Tbits 6h: 6 Tbits 7h: 7 Tbits
b[3]	-	Reserved	This bit is always read as 0. The write value should always be 0.
b[5:4]	IBS	Inter-byte Space Select Bits	00b: 0 Tbits 01b: 1 Tbit 10b: 2 Tbits 11b: 3 Tbits
b[7:6]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LSC.IBHS[2:0] Inter-byte Header Space and Response Space Select Bits

Users can not write to these bits if LMST[0] bit is "1".

These bits select the Inter-Byte Header Space and the Response Space width during LIN Master mode transmission.
The width is the same for Inter Byte Header Space and Response Space in LIN Master mode.
These bits select the Response Space width during LIN slave mode response transmission.

Note 1: These bits are "Don't Care" for UART mode communication and during LIN mode reception.

Note 2: Timeout error (if enabled) in LIN Master/Slave mode might occur if large values are set for Break Low width, Break Del width, IBHS and IBS bits e.g.: In the case of the following setting, frame timeout error occurs. Break Low > 23 Tbits, Break Del = 4 Tbits, Response Space Width = 7 Tbits, IBS = 3 Tbits

LSC.IBS[1:0] Inter-byte Space Select Bits

Users can not write to these bits if LMST[0] bit is "1".

These bits define the width of Inter-byte space during Response transmission or UART multi-byte transmission.

Note 1: These bits are invalid during LIN mode Response reception or LIN Response data group reception.

Note 2: Timeout error (if enabled) in LIN Master/Slave mode might occur if large values are set for Break Low width, Break Del width, IBHS and IBS bits e.g.: In the case of the following setting, frame timeout error occurs. Break Low > 23 Tbits, Break Del = 4 Tbits, Response Space Width = 7 Tbits, IBS = 3 Tbits

Note 3: Users shall write "00" to these bits in extended UART mode.

Note 4: If data is transmitted from the transmit data register (LUTDR) or the wait transmit data register (LUWTDR), these bits must be set to "00b".

4.8 LIN WAKE-UP CONFIGURATION REGISTER (LWUP)

Address: 000Bh									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**WUTL[3:0]**				**-**	**-**	**-**	**-**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R/W	R/W	R/W	R/W	R0/W0	R0/W0	R0/W0	R0/W0
LIN Master	**IDLE Mode**	R	R	R	R	R0/W0	R0/W0	R0/W0	R0/W0
	Operation Mode	R	R	R	R	R0/W0	R0/W0	R0/W0	R0/W0
LIN Slave	**IDLE Mode**	R	R	R	R	R0/W0	R0/W0	R0/W0	R0/W0
	Operation Mode	R	R	R	R	R0/W0	R0/W0	R0/W0	R0/W0
UART	**IDLE Mode**	R	R	R	R	R0/W0	R0/W0	R0/W0	R0/W0
	Operation Mode	R	R	R	R	R0/W0	R0/W0	R0/W0	R0/W0

Bit	Symbol	Bit Name	Register Function
b[3:0]	-	Reserved	These bits are always read as 0. The write value should always be 0.
b[7:4]	WUTL	LIN Wake-up Transmission Low width Select Bits	0h = Low pulse transmission 1Tbit 1h = Low pulse transmission 2Tbits : : : : Fh = Low pulse transmission 16Tbits

LWUP.WUTL[3:0] LIN Wake-up Transmission Low width Select Bits

Users can not write to these bits if LMST[0] bit is "1".

This bit selects the width of transmitted wake-up signal in LIN Wake-up mode.

Note 1: These bits are "Don't Care" in UART mode.

4.9 LIN INTERRUPT ENABLE REGISTER (LIE)

Address: 000Ch									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**-**	**-**	**-**	**-**	**SHIE**	**ERRIE**	**FRCIE**	**FTCIE**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R0/W0	R0/W0	R0/W0	R0/W0	R/W	R/W	R/W	R/W
LIN Master	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R	R	R	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R	R	R	R
LIN Slave	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R	R	R	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R	R	R	R
UART	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R	R	R	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R	R	R	R

Bit	Symbol	Bit Name	Register Function
b[0]	FTCIE	LIN Successful Transmission Interrupt Enable Bit	0: LIN Response or LIN Wake-up successful Transmission Interrupt Disabled 1: LIN Response or LIN Wake-up successful transmission Interrupt Enabled
b[1]	FRCIE	LIN Successful Reception Interrupt Enable Bit	0: LIN Response or LIN Wake-up Successful Reception Interrupt Disabled 1: LIN Response or LIN Wake-up Successful Reception Interrupt Enabled
b[2]	ERRIE	LIN Error Detection Interrupt Enable Bit	0: Error Detection Interrupt Disabled 1: Error Detection Interrupt Enabled
b[3]	SHIE	LIN Successful Header Interrupt Enable Bit	0: LIN Successful Header interrupt disabled 1: LIN Successful Header interrupt enabled
b[7:4]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LIE.FTCIE LIN Successful Transmission Interrupt Enable Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the generation of Interrupt for successful Transmission.

Note 1: This bit is "Don't Care" in UART mode.

LIE.FRCIE LIN Successful Reception Interrupt Enable Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the generation of Interrupt for successful Reception.

Note 1: This bit is "Don't Care" in UART mode.

LIE.ERRIE LIN Error Detection Interrupt Enable Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the generation of Interrupt for Error detection.

Note 1: This bit is "Don't Care" in UART mode.

LIE.SHIE LIN Successful Header Interrupt Enable Bit

Users can not write to this bit LMST[0] bit is "1".

This bit controls the generation of Interrupt for Header Tx in LIN Master mode and Header Rx in LIN Slave mode.

Note 1: This bit is "Don't Care" in UART mode.

4.10 LIN / UART ERROR DETECTION ENABLE REGISTER (LEDE)

4.10.1 LIN Master mode

Address: 000Dh								
Bit	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol	**LTES**	**-**	**-**	**-**	**FERE**	**FTERE**	**PBERE**	**BERE**
Initial Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode	R/W	R/W	R0/W0	R/W	R/W	R/W	R/W	R/W
IDLE Mode	R	R	R0/W0	R	R	R	R	R
Operation Mode	R	R	R0/W0	R	R	R	R	R

Bit	Symbol	Bit Name	Register Function
b[0]	BERE	LIN Bit Error Detection Enable Bit	0: Bit Error Detection Disabled 1: Bit Error Detection Enabled
b[1]	PBERE	LIN Physical Bus Error Detection Enable Bit	0: Physical Bus Error Detection Disabled 1: Physical Bus Error Detection Enabled
b[2]	FTERE	LIN Frame / Response Timeout Error Detection Enable Bit	0: Frame / Response Timeout Error Detection Disabled 1: Frame / Response Timeout Error Detection Enabled
b[3]	FERE	LIN Framing Error Detection Enable Bit	0: Framing Error Detection Disabled 1: Framing Error Detection Enabled
b[6:4]	-	Reserved	These bits are always read as 0. The write value should always be 0.
b[7]	LTES	LIN Timeout Error Selection Bit	0: Frame Timeout error is selected 1: Response Timeout error is selected

LEDE.BERE LIN Bit Error Detection Enable Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the detection of Bit Error

Note 1: Users shall write "1" to this bit in LIN Master mode.

LEDE.PBERE LIN Physical Bus Error Detection Enable Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the detection of Physical Bus Error

LEDE.FTERE LIN Frame / Response Timeout Error Detection Enable Bit

Users can not write to this bit if LMST[0] bit is "1".

Note: Timeout error should be disabled for data group communication.

This bit controls the detection of Timeout Error

LEDE.FERE LIN Framing Error Detection Enable Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the detection of Framing Error

Note 1: Users shall write "1" to this bit in LIN Master mode.

LEDE.LTES LIN Timeout Error Selection Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit is used to configure the detection of Frame Timeout Error or Response Timeout error.

LEDE[6:4] These bits are don't care at LIN Master mode.

4.10.2 LIN Slave mode

Address: 000Dh								
Bit	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol	**LTES**	**IPERE**	**-**	**SFERE**	**FERE**	**TERE**	**-**	**BERE**
Initial Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode	R/W	R/W	R0/W0	R/W	R/W	R/W	R/W	R/W
IDLE Mode	R	R	R0/W0	R	R	R	R	R
Operation Mode	R	R	R0/W0	R	R	R	R	R

Bit	Symbol	Bit Name	Register Function
b[0]	BERE	LIN Bit Error Detection Enable Bit	0: Bit Error Detection Disabled 1: Bit Error Detection Enabled
b[1]	-	Reserved	This bit is always read as 0. The write value should always be 0.
b[2]	TERE	LIN Frame / Response Timeout Error Detection Enable Bit	0: Frame / Response Timeout Error Detection Disabled 1: Frame / Response Timeout Error Detection Enabled
b[3]	FERE	LIN Framing Error Detection Enable Bit	0: Framing Error Detection Disabled 1: Framing Error Detection Enabled
b[4]	SFERE	LIN SYNC field Error Detection Enable Bit	0: SYNC field Error Detection Disabled 1: SYNC field Error Detection Enabled
b[5]	-	Reserved	This bit is always read as 0. The write value should always be 0.
b[6]	IPERE	LIN Identifier Parity Error Detection Enable Bit	0: Identifier Parity Error Detection Disabled 1: Identifier Parity Error Detection Enabled
b[7]	LTES	LIN Timeout Error Selection Bit	0: Frame Timeout error is selected 1: Response Timeout error is selected

LEDE.BERE LIN Bit Error Detection Enable Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the detection of Bit Error

Note 1: Users shall write "1" to this bit in LIN Slave mode. Otherwise, a new header may be not received.

LEDE.TERE LIN Frame / Response Timeout Error Detection Enable Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the detection of Timeout Error.

Note: Timeout error should be disabled for data group communication. Timeout error should also be disabled for Auto baud rate LIN Slave mode operation.

LEDE.FERE LIN Framing Error Detection Enable Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the detection of Framing Error

Note 1: Users shall write "1" to this bit in LIN Slave mode. Otherwise, a new header may be not received.

LEDE.SFERE LIN SYNC field Error Detection Enable Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the detection of SYNC field Error.

Note 1: This bit only controls the setting SYNC field error flag. If a SYNC Field Error is detected, then the module will always abort ongoing Header detection and will wait for the next Header.

LEDE.IPERE LIN Identifier Parity Error Detection Enable Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the detection of Identifier Parity Error.

Note 1: Users shall write "1" to this bit in LIN Slave mode. Otherwise, a new header may be not received.

LEDE.LTES LIN Timeout Error Selection Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit is used to configure the detection of Frame Timeout Error or Response Timeout error.

LEDE[5], LEDE[1] These bits are don't care at Slave mode.

4.10.3 UART mode

Address: 000Dh								
Bit	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol	**-**	**-**	**-**	**-**	**FERE**	**OERE**	**-**	**BERE**
Initial Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode	R/W	R/W	R0/W0	R/W	R/W	R/W	R/W	R/W
IDLE Mode	R	R	R0/W0	R	R	R	R	R
Operation Mode	R	R	R0/W0	R	R	R	R	R

Bit	Symbol	Bit Name	Register Function
b[0]	BERE	UART Bit Error Detection Enable Bit	0: Bit Error Detection Disabled 1: Bit Error Detection Enabled
b[1]	-	Reserved	This bit is always read as 0. The write value should always be 0.
b[2]	OERE	UART Overrun Error Detection Enable Bit	0: Overrun Error Detection Disabled 1: Overrun Error Detection Enabled
b[3]	FERE	UART Framing Error Detection Enable Bit	0: Framing Error Detection Disabled 1: Framing Error Detection Enabled
b[7:4]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LEDE.BERE UART Bit Error Detection Enable Bit

Users can not write to this bit if LMST[0] bit is "1".

Users should not set this bit in Full Duplex communication.

This bit controls the detection of Bit Error

Note 1: Users should not set this bit when LWBR[7:4] bits are 4'b0101 (6 samples per bit) and LMD[5] bit is 1'b0 (3-bit majority voting logic for sampling RX data is enabled).
Note 2: Users shall write "0" to this bit in extended UART mode.

LEDE.OERE UART Overrun Error Detection Enable Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the detection of Overrun Error

LEDE.FERE UART Framing Error Detection Enable Bit

Users can not write to this bit if LMST[0] bit is "1".

This bit controls the detection of Framing Error

LEDE[7:4], LEDE[1] These bits are don't care at UART mode.

4.11 LIN / UART CONTROL REGISTER (LCUC)

Address: 000Eh									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**-**	**-**	**-**	**-**	**-**	**-**	**OM1**	**OM0**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W	R/W
LIN Master	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W	R/W
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R	R/W
LIN Slave	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W	R/W
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R	R/W
UART	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R	R/W
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R	R/W

Bit	Symbol	Bit Name	Register Function
b[0]	OM0	LIN/UART Reset bit	0: SW Reset request is active. 1: SW Reset request is inactive
b[1]	OM1	LIN / UART mode select bit	0: LIN Wake-up mode enabled 1: LIN Normal Communication mode enabled
b[7:2]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LCUC.OM0 LIN/UART Reset bit

After writing to bit LCUC[0], users should not write to this register until bit LMST[0] value matches the bit LCUC[0] value.

This bit controls the SW reset request generation for the RLIN3 module.

LCUC.OM1 LIN / UART mode select bit

Users can not write to this bit if LTRC[0] is set to "1".

In LIN Master mode or LIN Slave mode, this bit configures the RLIN3 module in LIN Normal communication mode or LIN Wake-up mode.

Note 1: Users can not write to this bit in UART mode.

Note 2: While writing to this register, write "01b" to configure module in LIN Wake-up mode after exiting Reset state or "11b" to configure the module in LIN Normal mode after exiting Reset state.

4.12 LIN / UART TRANSMISSION CONTROL REGISTER (LTRC)

4.12.1 LIN Master mode

Address: 0010h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**-**	**-**	**-**	**-**	**-**	**-**	**RTS**	**FTS**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0	R0	R0
LIN Master	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0	R/W1
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W1	R

Bit	Symbol	Bit Name	Register Function
b[0]	FTS	LIN Communication start bit	0: Frame Communication is stopped 1: Frame Communication start is enabled
b[1]	RTS	Response Transmission or Reception start bit	0: Response transmission or reception stopped in Frame Separate mode 1: Response transmission or reception start in Frame Separate mode
b[7:2]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LTRC.FTS LIN Communication start bit

This bit is used to start LIN Header TX, Response TX (only in Frame combined mode) and Wake-up TX in LIN Master mode.
This bit is used for enabling Response RX and Wakeup RX in LIN Master mode.

Users can not write to this bit if LMST[0] bit is "0".
Users can not write to this bit if the LTRC[0] bit is "1".

This bit is cleared after successful completion of Frame (TX or RX of the last data byte)
This bit is cleared after successful Wake-up TX or RX.
This bit is cleared after detection of an error during Frame TX or RX or Wake-up TX.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

LTRC.RTS Response Transmission or Reception start bit

This bit is used to start LIN Response transmission or LIN Response data group transmission or enable LIN Response data group reception in LIN Master mode if the module is configured in Frame Separate mode. For LIN Response data group transmission or reception, users should set this bit to start transmission of each data group or enable reception of each data group.

This bit can not be set to 1 when the LIN Communication Start bit (FTS) is "0b" in LIN Master mode.
Users can not write to this bit if LMST[0] bit is "0".
This bit should be set if the LST.FTC bit or LST.FRC bit is set by a previous data group transmission complete or data group reception complete and there are some next data groups in the data group response.
This bit can not be cleared by Register access.
This bit is cleared after each successful data group response (TX or RX).
This bit is cleared after detection of an error during Frame TX or RX.
This bit is cleared when RLIN3 module is transitioning to the reset mode.
There is the possibility that LTRC.FTS is set again in case the value 03H is written into LTRC register to set this bit in Frame Separate mode and LTRC.FTS is cleared by Error (Bit error or Timeout error) at the same time. For details, refer to Section 8.3.

4.12.2 LIN Slave mode

Address: 0010h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**-**	**-**	**-**	**-**	**-**	**LNRR**	**RTS**	**FTS**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0	R0	R0
LIN Slave	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0	R0	R/W1
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W1	R/W1	R

Bit	Symbol	Bit Name	Register Function
b[0]	FTS	LIN Communication start bit	0: Frame Communication is stopped 1: Frame Communication start is enabled
b[1]	RTS	Response Transmission or Reception start bit	0: Response transmission or reception stopped 1: Response transmission or reception start
b[2]	LNRR	LIN No Response Request bit	0: Response for received ID is present 1: Response for received ID is absent
b[7:3]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LTRC.FTS LIN Communication start bit

This bit is used to start Wake-up TX in LIN Slave mode.
This bit is used for enabling LIN Header RX and Wake-up RX in LIN Slave mode.

Users can not write to this bit if LMST[0] bit is "0".
Users can not write to this bit if the LTRC[0] bit is set.

This bit is cleared after successful Wake-up TX or RX or if error is detected during Wake-up TX.

This bit is cleared when RLIN3 module is transitioning to the reset mode.

LTRC.RTS Response Transmission or Reception start bit

This bit is used to start LIN Response transmission or LIN Response data group transmission or enable Response reception or LIN Response data group reception in LIN Slave mode.
For LIN Response data group transmission or reception, users should set this bit to start transmission of each data group or enable reception of each data group.

Users should not write to this bit if LTRC[2] is set to "1" (No response for received ID).

This bit should only be set if the LST.HTRC bit is set after header reception.
LIN Response Preparation Error is detected, if LTRC.RTS isn't set until 1st byte reception.

Users can not write to this bit if LMST[0] bit is "0".
This bit can not be set to 1 when the LIN Communication Start bit (FTS) is "0b" in LIN Slave mode.
This bit can not be cleared by Register access.

This bit is cleared after each successful data group response (TX or RX).
This bit is cleared after detection of an error during response TX or RX.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

This bit is automatically cleared when the RLIN3 module successfully detects a new Sync field.

Designers information:

- LTRC.RTS setting area:
  Start point : Header reception (LST.HTRC = 1)
  End point : Sync field detection, Error detection (LST.ERR = 1), Response complete ((LST.FTC = 1 or LST.FRC = 1) and LDFC.LSS = 0)
- LTRC.RTS active area:
  - Fixed baud rate mode:
    Communication is stopped when the RLIN3 module successfully detects a new Break low.
  - Auto baud rate mode:
    Communication is stopped when the RLIN3 module successfully detects a new Sync field.

LTRC.LNRR LIN No Response Request bit

In LIN Slave mode, this bit is used to control the Response communication.
This bit is used when a response is not applicable for the received ID in the LIN Slave mode.

Users can not write to this bit if LMST[0] bit is "0".
This bit can not be cleared by Register access in LIN slave mode.
This bit can not be set to 1 when the LIN Communication Start bit (FTS) is "0b" in LIN Slave mode.

Users shall not write to this bit if LTRC[1] is set to "1" (Response is enabled).

This bit is automatically cleared when the RLIN3 module successfully detects a new Sync field.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Users should use this bit only 1st data group in LIN Response data group communication.

4.12.3 UART mode

Address: 0010h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**-**	**-**	**-**	**-**	**-**	**-**	**RTS**	**-**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0	R0	R0
UART	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W1	R/W
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W1	R

Bit	Symbol	Bit Name	Register Function
b[0]	-	Reserved	This bit is always read as 0. The write value should always be 0.
b[1]	RTS	UART multi-byte transmission start bit	0: UART buffer transmission stopped 1: UART buffer transmission start
b[7:2]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LTRC.RTS UART multi-byte transmission start bit

This bit can not be cleared by Register access.
Users can not write to this bit if LMST[0] bit is "0".

Users should not write to this bit when a transmit operation is in progress (LST.UTS = "1").
Users should set this bit only when LUOER.UTOE bit is 1 and UART multi-byte transmission is used.

It is also cleared at the end of UART multi-byte communication (When a transmission has completed the number of data configured by LDFC.MDL in spite of a presence of an error).

This bit is cleared when RLIN3 module is transitioning to the reset mode.
Note 1: Users shall write "0" to this bit in extended UART mode.

4.13 LIN / UART MODE STATUS REGISTER (LMST)

Address: 0011h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**-**	**-**	**-**	**-**	**-**	**-**	**OMM1**	**OMM0**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R	R
LIN Master	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R	R
LIN Slave	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R	R
UART	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R	R

Bit	Symbol	Bit Name	Register Function
b[0]	OMM0	LIN/UART Reset status bit	0: Module is in Reset state. 1: Module is not in Reset state
b[1]	OMM1	LIN mode status bit	0: LIN Wake-up mode enabled 1: LIN Normal Communication mode enabled
b[7:2]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LMST.OMM0 LIN/UART Reset status bit

Users can not write data to this bit.

Clearing condition(s):
RLIN3 module enters Reset state due to HW Reset or SW reset request.

Setting condition(s):
RLIN3 module exits reset state when the SW Reset request is de-activated.

LMST.OMM1 LIN mode status bit

Users can not write data to this bit.

Clearing condition(s):
In LIN mode, this bit is cleared when module is configured in Wake-up mode.

Setting condition(s):
In LIN mode, this bit is set when module is configured in Normal communication mode.

Note 1: This bit is "Don't Care" when the RLIN3 Module is in UART mode.

4.14 LIN / UART STATUS REGISTER (LST)

4.14.1 LIN Master mode

Address: 0012h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**HTRC**	**D1RC**	**-**	**-**	**ERR**	**-**	**FRC**	**FTC**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R0	R0	R0	R0	R0	R0/W0	R0	R0
LIN Master	**IDLE Mode**	R/W0C*1	R/W0C*1	R0	R0	R	R0/W0	R/W0C*1	R/W0C*1
	Operation Mode	R/W0C	R/W0C	R0	R0	R	R0/W0	R/W0C	R/W0C

1 These bits can only be written '0' or '1' if the bit (LSTC.LSFWC**) is enabled & in IDLE mode, (not open spec).*

Note: For this register, when only a single bit is to be cleared by the program, do not use bit clear instruction - use the MOV instruction to ensure that only the specified bit is cleared. Then the other bits remain set to "1". Writing "1" gives no influence to the bit values.

Bit	Symbol	Bit Name	Register Function
b[0]	FTC	Frame Transmission complete flag	0: Response or Wake-up transmission not completed 1: Response or Wake-up transmitted successfully
b[1]	FRC	Frame Reception complete flag	0: Response or Wake-up reception not completed 1: Response or Wake-up received successfully
b[2]	-	Reserved	This bit is always read as 0. The write value should always be 0.
b[3]	ERR	LIN Error SUM status	0: No error detected in LIN mode 1: Errors detected in LIN mode
b[5:4]	-	Reserved	These bits are always read as 0. The write value should always be 0.
b[6]	D1RC	LIN One byte reception flag	0: One Byte reception not completed 1: One Byte reception completed
b[7]	HTRC	LIN Header Transmission / Reception flag	0: LIN Header Tx not completed 1: LIN Header Tx completed successfully

LST.FTC Frame Transmission complete flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared automatically when LTRC[0] bit is set in LIN Master mode.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when LIN Response transmission or LIN Response data group transmission completed successfully.
This bit is set when Wake-up transmission is completed successfully.

LST.FRC Frame Reception complete flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared automatically when LTRC[0] bit is set in LIN Master mode.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when LIN Response reception or LIN Response data group reception is completed successfully.
This bit is set when Wake-up signal detection is completed successfully.

LST.ERR LIN Error SUM status

Users can not write to this bit.

Clearing condition(s):
This bit is clear when all bits in the LEST register are cleared to "0" in LIN mode.

Setting condition(s):
This bit is set when at least 1 bit in the LEST register is set to "1" in LIN mode.

LST.D1RC LIN One byte reception flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
In LIN Master mode, this bit is cleared by writing "0" to it.
This bit is cleared automatically when LTRC[0] bit is set in LIN Master mode.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when 1st Data byte is successfully received during Response reception.
This bit is set whenever RLIN3 module receives the data of the beginning of each data group when receiving 9 bytes or more of response data.

LST.HTRC LIN Header Transmission / Reception flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
In LIN Master mode, this bit is cleared by writing "0" to it.
This bit is cleared automatically when LTRC[0] bit is set in LIN Master mode.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when Header is successfully transmitted in LIN Master mode

4.14.2 LIN Slave mode

Address: 0012h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**HTRC**	**D1RC**	**-**	**-**	**ERR**	**-**	**FRC**	**FTC**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R0	R0	R0	R0	R0	R0/W0	R0	R0
LIN Slave	**IDLE Mode**	R/W0C*1	R/W0C*1	R0	R0	R	R0/W0	R/W0C*1	R/W0C*1
	Operation Mode	R/W0C	R/W0C	R0	R0	R	R0/W0	R/W0C	R/W0C

1 These bits can only be written '0' or '1' if the bit (LSTC.LSFWC**) is enabled & in IDLE mode, (not open spec).*

Note: For this register, when only a single bit is to be cleared by the program, do not use bit clear instruction - use the MOV instruction to ensure that only the specified bit is cleared. Then the other bits remain set to "1". Writing "1" gives no influence to the bit values.

Bit	Symbol	Bit Name	Register Function
b[0]	FTC	Frame Transmission complete flag	0: Response or Wake-up transmission not completed 1: Response or Wake-up transmitted successfully
b[1]	FRC	Frame Reception complete flag	0: Response or Wake-up reception not completed 1: Response or Wake-up received successfully
b[2]	-	Reserved	This bit is always read as 0. The write value should always be 0.
b[3]	ERR	LIN Error SUM status	0: No error detected in LIN mode 1: Errors detected in LIN mode
b[5:4]	-	Reserved	These bits are always read as 0. The write value should always be 0.
b[6]	D1RC	LIN One byte reception flag	0: One Byte reception not completed 1: One Byte reception completed
b[7]	HTRC	LIN Header Transmission / Reception flag	0: LIN Header Rx not completed 1: LIN Header Rx completed successfully

LST.FTC Frame Transmission complete flag

Users can not write to this bit if LMST[0] bit is "0".
The interrupt is not generated even if Response or Wake-up transmission is completed when LST.FTC is 1.

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.
This bit is cleared automatically when LTRC[0] bit is set in LIN Slave mode.

Setting condition(s):
This bit is set when LIN Response transmission or LIN Response data group transmission completed successfully.
This bit is set when Wake-up transmission is completed successfully.

LST.FRC Frame Reception complete flag

Users can not write to this bit if LMST[0] bit is "0".
The interrupt is not generated even if Response or Wake-up reception is completed when LST.FRC is 1.

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.
This bit is cleared automatically when LTRC[0] bit is set in LIN Slave mode.

Setting condition(s):
This bit is set when LIN Response reception or LIN Response data group reception is completed successfully.
This bit is set when Wake-up signal detection is completed successfully.

LST.ERR LIN Error SUM status

Users can not write to this bit.

Clearing condition(s):
This bit is clear when all bits in the LEST register are cleared to "0" in LIN mode.

Setting condition(s):
This bit is set when at least 1 bit in the LEST register is set to "1" in LIN mode.

LST.D1RC LIN One byte reception flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.
This bit is cleared automatically when LTRC[0] bit is set in LIN Slave mode.

Setting condition(s):
This bit is set when 1st Data byte is successfully received during Response reception.
This bit is set whenever RLIN3 module receives the data of the beginning of each data group when receiving 9 bytes or more of response data.

LST.HTRC LIN Header Transmission / Reception flag

Users can not write to this bit if LMST[0] bit is "0".
The interrupt is not generated when Header reception is completed and LST.HTRC is 1.

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.
This bit is cleared automatically when LTRC[0] bit is set in LIN Slave mode.

Setting condition(s):
This bit is set when Header is successfully received in LIN Slave mode.

Note: RLIN3 does not generate Successful Header Reception interruption in the detection of new header, if this flag is not cleared to '0'.

4.14.3 UART mode

Address: 0012h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**-**	**-**	**URS**	**UTS**	**ERR**	**-**	**-**	**FTC**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R0	R0	R0	R0	R0	R0/W0	R0	R0
UART	**IDLE Mode**	R0	R0	R	R	R	R0/W0	R0	R/W0C*1
	Operation Mode	R0	R0	R	R	R	R0/W0	R0	R/W0C

1 These bits can only be written '0' or '1' if the bit (LSTC.LSFWC**) is enabled & in IDLE mode, (not open spec).*

*Users should not write "1" to LST[7:6], [1] in UART, even if the bit (**LSTC.LSFWC**) is enabled & in IDLE mode.*

Note: For this register, when only a single bit is to be cleared by the program, do not use bit clear instruction - use the MOV instruction to ensure that only the specified bit is cleared. Then the other bits remain set to "1". Writing "1" gives no influence to the bit values.

Bit	Symbol	Bit Name	Register Function
b[0]	FTC	Frame Transmission complete flag	0: Frame transmission not completed 1: Frame transmitted completed
b[2:1]	-	Reserved	These bits are always read as 0. The write value should always be 0.
b[3]	ERR	UART Error SUM status	0: No changes in Error status detected in UART mode. 1: Change in Error status detected in UART mode.
b[4]	UTS	UART Transmission Status	0: A transmit operation is not in progress. 1: A transmit operation is in progress.
b[5]	URS	UART Reception Status	0: A receive operation is not in progress. 1: A receive operation is in progress.
b[7:6]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LST.FTC Frame Transmission complete flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when UART multi-byte transmission is completed successfully and configured number of data bytes are transmitted in spite of a presence of an error.

LST.ERR UART Error SUM status

Users can not write to this bit.

Clearing condition(s):
This bit is clear when all bits in the LEST register are cleared to "0" in UART mode.
(LEST.LDCER bit is an exception.)

Setting condition(s):
This bit is set when at least 1 bit in the LEST register is set to "1" in UART mode
(LEST.LDCER bit is an exception.)

LST.UTS UART Transmission Status

Users can not write to this bit.

Clearing condition(s):
In UART mode, this bit is cleared when Frame Transmission stops due to the following cases:

- When next transmit data is not written in UART 7bit/8bit/9bit Transmit Data Register, UART 7bit/8bit/9bit Wait Transmit Data register upon transmission completion
- When LTRC[1] bit is cleared at the end of UART multi-byte transmission.

This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
In UART mode, this bit is set in the following cases:

- Data is written to UART 7bit/8bit/9bit Transmit Data Register or UART 7bit/8bit/9bit Wait Transmit Data register
- LTRC[1] bit is set.

LST.URS UART Reception Status

Users can not write to this bit.

Clearing condition(s):
In UART mode, this bit is cleared when Frame Reception stops due to the following cases:

- Sampling point of STOP bit is detected for the UART frame

This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):

- In UART mode, this bit is set when start bit is detected successfully.

4.15 LIN/UART ERROR STATUS REGISTER (LEST)

4.15.1 LIN Master mode

Address: 0013h								
Bit	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol	**RPER**	**-**	**CSER**	**-**	**FER**	**FTER**	**PBER**	**BER**
Initial Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode	R0	R0	R0	R0	R0	R0	R0	R0
IDLE Mode	R/W0C*1	R0*1	R/W0C*1	R0*1	R/W0C*1	R/W0C*1	R/W0C*1	R/W0C*1
Operation Mode	R	R0	R	R0	R	R	R	R

1 These bits can be written '0' or '1' if the bit (LSTC.LSFWC**) is enabled & in IDLE mode, (not open spec). Users should not write "1" to LEST[6], [4] in LIN Master, even if the bit (**LSTC.LSFWC**) is enabled & in IDLE mode.*

Note 1: For this register, when only a single bit is to be cleared by the program, do not use bit clear instruction - use the MOV instruction to ensure that only the specified bit is cleared. Then the other bits remain set to "1". Writing "1" gives no influence to the bit values.

Bit	Symbol	Bit Name	Register Function
b[0]	BER	LIN Bit Error flag	0: Bit error not detected 1: Bit error detected
b[1]	PBER	LIN Physical Bus Error flag	0: Physical Bus error not detected 1: Physical Bus error detected
b[2]	FTER	LIN Timeout Error flag	0: LIN Timeout error not detected 1: LIN Timeout error detected
b[3]	FER	LIN Framing Error flag	0: LIN Framing error not detected 1: LIN Framing error detected
b[4]	-	Reserved	This bit is always read as 0. The write value should always be 0.
b[5]	CSER	LIN CheckSum Error flag	0: LIN Checksum error not detected 1: LIN Checksum error detected
b[6]	-	Reserved	This bit is always read as 0. The write value should always be 0.
b[7]	RPER	LIN Response Preparation Error flag	0: Response Preparation error not detected 1: Response Preparation error detected

LEST.BER LIN Bit Error flag

Users can not write to this bit if LMST[0] bit is "0".
Users can not write to this bit if LTRC[0] bit is "1".

Clearing condition(s):
This bit is cleared in IDLE mode by writing "0" to it.
This bit is cleared automatically when LTRC[0] bit is set in LIN Master mode.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when the sampled bit value does not match transmitted bit value during transmission and the error detection is enabled.

LEST.PBER LIN Physical Bus Error flag

Users can not write to this bit if LMST[0] bit is "0".
Users can not write to this bit if LTRC[0] bit is "1".

Clearing condition(s):
This bit is cleared in IDLE mode by writing "0" to it.
This bit is cleared automatically when LTRC[0] bit is set in LIN Master mode.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when the sampled bit value does not match expectation value during Wake-up(Wake-Up Low) or Break field(Break Low, Break Delimiter) transmission and the error detection is enabled.

LEST.FTER LIN Timeout Error flag

Users can not write to this bit if LMST[0] bit is "0".
Users can not write to this bit if LTRC[0] bit is "1".

Clearing condition(s):
This bit is cleared in IDLE mode by writing "0" to it.
This bit is cleared automatically when LTRC[0] bit is set in LIN Master mode.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when the timeout counter (frame or response timeout) reaches the error threshold value (calculated automatically) and the error detection is enabled.

LEST.FER LIN Framing Error flag

Users can not write to this bit if LMST[0] bit is "0".
Users can not write to this bit if LTRC[0] bit is "1".

Clearing condition(s):
This bit is cleared in IDLE mode by writing "0" to it.
This bit is cleared automatically when LTRC[0] bit is set in LIN Master mode.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when a "0" value is sampled for STOP bit during reception and the error detection is enabled.

LEST.CSER LIN CheckSum Error flag

Users can not write to this bit if LMST[0] bit is "0".
Users can not write to this bit if LTRC[0] bit is "1".

Clearing condition(s):
This bit is cleared in IDLE mode by writing "0" to it.
This bit is cleared automatically when LTRC[0] bit is set in LIN Master mode.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when received Checksum value during response reception does not match internally calculated Checksum value.

LEST.RPER LIN Response Preparation Error flag

Users can not write to this bit if LMST[0] bit is "0".
Users can not write to this bit if LTRC[0] bit is "1".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared automatically when LTRC[0] bit is set in LIN Master mode.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
In LIN Master mode, this bit is set in the following cases:

- In Frame Separate mode, Response preparation is not completed before reception of the 1st byte of the data group response is completed when LDFC.RFT is set to 0b (Response Reception).

4.15.2 LIN Slave mode

Address: 0013h								
Bit	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol	**RPER**	**IPER**	**CSER**	**SFER**	**FER**	**TER**	**-**	**BER**
Initial Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode	R0	R0	R0	R0	R0	R0	R0	R0
IDLE Mode	R/W0C*1	R/W0C*1	R/W0C*1	R/W0C*1	R/W0C*1	R/W0C*1	R0*1	R/W0C*1
Operation Mode	R/W0C	R/W0C	R/W0C	R/W0C	R/W0C	R/W0C	R0	R/W0C

1 These bits can be written '0' or '1' if the bit (LSTC.LSFWC**) is enabled & in IDLE mode, (not open spec). Users should not write "1" to LEST[1] in LIN Slave, even if the bit (**LSTC.LSFWC**) is enabled & in IDLE mode.*

Note: For this register, when only a single bit is to be cleared by the program, do not use bit clear instruction - use the MOV instruction to ensure that only the specified bit is cleared. Then the other bits remain set to "1". Writing "1" gives no influence to the bit values.

Bit	Symbol	Bit Name	Register Function
b[0]	BER	LIN Bit Error flag	0: Bit error not detected 1: Bit error detected
b[1]	-	Reserved	This bit is always read as 0. The write value should always be 0.
b[2]	TER	LIN Timeout Error flag	0: LIN Timeout error not detected 1: LIN Timeout error detected
b[3]	FER	LIN Framing Error flag	0: LIN Framing error not detected 1: LIN Framing error detected
b[4]	SFER	LIN SYNC field Error flag	0: SYNC field Error not detected 1: SYNC field Error detected
b[5]	CSER	LIN CheckSum Error flag	0: LIN Checksum error not detected 1: LIN Checksum error detected
b[6]	IPER	LIN Identifier Parity Error flag	0: Identifier Parity Error not detected 1: Identifier Parity Error detected
b[7]	RPER	LIN Response Preparation Error flag	0: Response Preparation error not detected 1: Response Preparation error detected

LEST.BER LIN Bit Error flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.
This bit is cleared automatically when LTRC[0] bit is set in LIN Slave mode.

Setting condition(s):
This bit is set when sampled bit value does not match transmitted bit value during transmission and the error detection is enabled.

LEST.TER LIN Timeout Error flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.
This bit is cleared automatically when LTRC[0] bit is set in LIN Slave mode.

Setting condition(s):
This bit is set when the timeout counter (frame or response timeout) reaches the error threshold value (calculated automatically) and the error detection is enabled.

LEST.FER LIN Framing Error flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.
This bit is cleared automatically when LTRC[0] bit is set in LIN Slave mode.

Setting condition(s):
This bit is set when a "0" value is sampled for STOP bit during reception and the error detection is enabled.

LEST.SFER LIN SYNC field Error flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.
This bit is cleared automatically when LTRC[0] bit is set in LIN Slave mode.

Setting condition(s):
This bit is set if the Sync field is not detected as "55h" and Break LOW width is more than or equal to configured Break Low width.

LEST.CSER LIN CheckSum Error flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.
This bit is cleared automatically when LTRC[0] bit is set in LIN Slave mode.

Setting condition(s):
This bit is set when received Checksum value during response reception does not match internally calculated Checksum value.

LEST.IPER LIN Identifier Parity Error flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.
This bit is cleared automatically when LTRC[0] bit is set in LIN Slave mode.

Setting condition(s):
This bit is set when the received Identifier parity bit values do not match the calculated Identifier Parity bit values and the error detection is enabled.

LEST.RPER LIN Response Preparation Error flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.
This bit is cleared automatically when LTRC[0] bit is set in LIN Slave mode.

Setting condition(s):
In Slave mode, this bit is set in the following cases:

- Response preparation is not completed before reception of the 1st byte of the response when LDFC.RFT is set to 0b or 1b (Response Reception/Response Transmission).
- Response preparation is not completed before reception of the 1st byte of the data group response is completed when LDFC.RFT is set to 0b (Response Reception).
- Response preparation is not completed before reception of the 1st byte of the data group response is completed only at the 1st data group response when LDFC.RFT is set to 1b (Response Transmission).

This error can also be detected in LIN Slave mode with automatic baud rate detection and LIN Slave mode with fixed baud rate.

4.15.3 UART mode

Address: 0013h								
Bit	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol	**-**	**UPER**	**IDMT**	**EXBT**	**FER**	**OER**	**LDCER**	**BER**
Initial Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode	R0	R0	R0	R0	R0	R0	R0	R0
IDLE Mode	R0	R/W0C*1	R/W0C*1	R/W0C*1	R/W0C*1	R/W0C*1	R/W0C*1	R/W0C*1
Operation Mode	R0	R/W0C	R/W0C	R/W0C	R/W0C	R/W0C	R/W0C	R/W0C

1 These bits can be written '0' or '1' if the bit (LSTC.LSFWC**) is enabled & in IDLE mode, (not open spec). Users should not write "1" to LEST[7] in UART, even if the bit (**LSTC.LSFWC**) is enabled & in IDLE mode.*

Note: For this register, when only a single bit is to be cleared by the program, do not use bit clear instruction - use the MOV instruction to ensure that only the specified bit is cleared. Then the other bits remain set to "1". Writing "1" gives no influence to the bit values.

Bit	Symbol	Bit Name	Register Function
b[0]	BER	UART Bit Error flag	0: Bit error not detected 1: Bit error detected
b[1]	LDCER	UART Loop-back Delayed data Consistency Error flag	0: Loop-back delayed data consistency error not detected. 1: Loop-back delayed data consistency error detected.
b[2]	OER	UART Overrun Error Flag	0: UART Overrun error not detected 1: UART Overrun error detected
b[3]	FER	UART Framing Error flag	0: UART Framing error not detected 1: UART Framing error detected
b[4]	EXBT	UART Expansion Bit Detection Flag	0: Expansion bit is not detected 1: Expansion bit is detected
b[5]	IDMT	UART ID Match Flag	0: Received byte does not match ID value 1: Received byte matches ID value.
b[6]	UPER	UART Parity Error flag	0: UART Parity Error not detected 1: UART Parity Error detected
b[7]	-	Reserved	This bit is always read as 0. The write value should always be 0.

LEST.BER UART Bit Error flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when sampled bit value does not match transmitted bit value during transmission and the error detection is enabled.

LEST. LDCER UART Loop-back Delayed data Consistency Error flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when the transmission data and the loop-back delayed data are not equal.

LEST.OER UART Overrun Error Flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when receive data has been stored into the UART receive data register and the next receive operation is completed before that receive data has been read and the error detection is enabled.

Note 1: If reception error is generated, Users should read the Receive Data register (LURDR). Otherwise, Overrun Error is generated at the time of the next data stop bit detection.

LEST.FER UART Framing Error flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when a framing error has occurred and the LUSC.USEC is not set. Only the 1st stop bit of the receive data stop bits is checked, regardless of the setting value of the UART Stop Bit Length Select Bit (LBFC.USBLS).

LEST.EXBT UART Expansion Bit Detection Flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when the level on the RX input has been detected based on the LUOR1.UEBDL setting and LUOR1.UEBE is set and LUOR1.UECD is not set and the LUSC.USEC is not set.

LEST.IDMT UART ID Match Flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when all of the below conditions are met:
1. Expansion bit is enabled (LUOR1.UEBE == 1),
2. Expansion bit data comparison is enabled (LUOR1.UEBDCE == 1),
3. UART Expansion Bit Comparison is enabled (LUOR1.UECD == 0),
4. Received expansion bit matches the expansion bit detection level (LUOR1.UEBDL),
5. Received data excluding the expansion bit matches the value in the LIDB register.

LEST.UPER UART Parity Error flag

Users can not write to this bit if LMST[0] bit is "0".

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when received value of Parity bit does not match the internally calculated value of Parity for a data byte and the LUSC.USEC is not set.

4.16 LIN / UART DATA FIELD CONFIGURATION REGISTER (LDFC)

4.16.1 LIN Master mode

Address: 0014h								
Bit	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol	**LSS**	**FSM**	**CSM**	**RFT**	**RFDL[3:0]**			
Initial Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
IDLE Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Operation Mode	R/W	R	R	R	R/W	R/W	R/W	R/W

Bit	Symbol	Bit Name	Register Function
b[3:0]	RFDL	LIN Response Field Data length select bits	0h = 0byte (+ Checksum) 1h = 1byte (+ Checksum) 2h = 2bytes (+ Checksum) : : : 8h to Fh= 8bytes (+ Checksum)
b[4]	RFT	LIN Response Communication Direction Select Bit	0: Response Reception 1: Response Transmission
b[5]	CSM	LIN Checksum Select Bit	0: Classic Checksum 1: Enhanced Checksum
b[6]	FSM	LIN Frame Separate Mode Select Bit	0: Frame Combined Mode 1: Frame Separate Mode
b[7]	LSS	LIN Successive selection bit	0: Last data group to be transmitted or received 1: Not the last data group

LDFC.RFDL[3:0] LIN Response Field Data length select bits

Users should not write to these bits if LTRC[0] is "1" for Response reception.
Users should not write to these bits if LTRC[0] is "1" for Response transmission in Frame Combined mode.
Users should not write to these bits if LTRC[1] is "1" for Response transmission in Frame Separate mode.
Users should not write to these bits if LTRC[1] is "1" for Response data group transmission or Response data group reception in Frame Separate mode.

These bits control the Response Field Data length.

Note that during response group reception and transmission the checksum is only present in the last data group (LDFC.LSS = "0"). In all other data groups (LDFC.LSS = 1) no checksum is included.

LDFC.RFT LIN Response Communication Direction Select Bit

Users should not write to this bit during Response data group communication.

Users can not write to this bit if LTRC[0] bit is set to "1b".

This bit controls the direction for Response communication, Response data group communication and Wake-up.

LDFC.CSM LIN Checksum Select Bit

Users should not write to this bit during Response data group communication.

Users can not write to this bit if LTRC[0] bit is set to ”1b”.

This bit selects the type of Checksum calculation for Response communication.

LDFC.FSM LIN Frame Separate Mode Select Bit

Users should not write to this bit during Response data group communication.

Users can not write to this bit if LTRC[0] bit is set to “1b”.

This bit selects the type of Response communication.
In Frame combined mode, RLIN3 module starts Response transmission or enables Response reception after successful Header transmission without setting the LTRC[1] bit.
In Frame separate mode, RLIN3 module starts Response transmission or Response data group transmission or enables Response data group reception only after both of the following conditions are met:

- successful Header transmission
- the users set the LTRC[1] bit.

Note: In LIN Master mode Frame separate mode for Response should only be used for data group reception.

LDFC.LSS LIN Successive selection bit

Users should not set this bit in Frame Combined mode.
Users should only clear this bit to indicate the last data group in Frame Separate mode.

This bit allows the users to transmit or receive more than or equal to 9 data bytes of Response.

Note: The checksum value for Response data group communication is calculated in the Response data of all data group.

4.16.2 LIN Slave mode

Address: 0014h								
Bit	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol	**LSS**	**-**	**LCS**	**RCDS**	**RFDL[3:0]**			
Initial Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
IDLE Mode	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Operation Mode	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Bit Name	Register Function
b[3:0]	RFDL	LIN Response Field Data length select bits	0h = 0byte (+ Checksum) 1h = 1byte (+ Checksum) 2h = 2bytes (+ Checksum) : : : 8h to Fh= 8bytes (+ Checksum)
b[4]	RCDS	LIN Response Communication Direction Select Bit	0: Response Reception 1: Response Transmission
b[5]	LCS	LIN Checksum Select Bit	0: Classic Checksum 1: Enhanced Checksum
b[6]	-	Reserved	This bit is always read as 0. The write value should always be 0.
b[7]	LSS	LIN Successive selection bit	0: Last data group to be transmitted or received 1: Not the last data group

LDFC.RFDL[3:0] LIN Response Field Data length select bits

Users should not write to these bits if LTRC[1] is "1" for Response reception or transmission and response data group reception or transmission.

These bits control the Response Field Data length in LIN Slave mode.

Note that during response group reception and transmission the checksum is only present in the last data group (LDFC.LSS = "0"). In all other data groups (LDFC.LSS = 1) no checksum is included.

LDFC.RCDS LIN Response Communication Direction Select Bit

Users can not write to this bit if LTRC[1] bit is set.
Users can not write to this bit if LTRC[0] bit is set in LIN Wake-up mode.

Users should not change this bit after setting to LTRC[1] for 1st data group transmission/reception.

This bit controls the direction for Response communication and Wake-up.

LDFC.LCS LIN Checksum Select Bit

Users can not write to this bit if LTRC[1] bit is set.

Users should not change this bit after setting to LTRC[1] for 1st data group transmission/reception.

This bit selects the type of Checksum calculation for Response communication.

If number of Response Data bytes is "0", then, users should only use Classic checksum.
LDFC.LSS LIN Successive selection bit

Users can not write to this bit if LTRC[1] bit is set.

This bit allows the users to transmit or receive more than or equal to 9 data bytes of Response. Users should only clear this bit to indicate the last data group.

LDFC[6] This bit is don't care for LIN Slave mode

Note: The checksum value for Response data group communication is calculated in the Response data of all data group.

4.16.3 UART mode

Address: 0014h								
Bit	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol	**-**	**-**	**UTSW**	**-**	**MDL[3:0]**			
Initial Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
IDLE Mode	R	R	R/W	R	R/W	R/W	R/W	R/W
Operation Mode	R	R	R	R	R	R	R	R

Bit	Symbol	Bit Name	Register Function
b[3:0]	MDL	UART Multi-byte Data length select bits	0h = 9bytes 1h = 1byte 2h = 2bytes : : : 8h = 8bytes 9h to Fh = 9bytes
b[4]	-	Reserved	This bit is always read as 0. The write value should always be 0.
b[5]	UTSW	UART Transmission Start Wait Bit	0: Starts transmission immediately when UART multi-byte transmission is requested 1: Delays starting of transmission until completion of stop bit of reception when UART multi-byte transmission is requested
b[7:6]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LDFC.MDL[3:0] UART Multi-byte Data length select bits

Users can not write to these bits if LTRC[1] is "1" for UART multi-byte transmission.

These bits control the Data length in UART mode communication.
Note 1: Users shall write "0000b" to these bits in extended UART mode.

LDFC.UTSW UART Transmission Start Wait Bit

Users can not write to this bit if the LTRC[1] bit is "1" for UART multi-byte transmission.
This bit becomes valid at the same time as the LTRC[1] bit is set to "1".

This bit controls the start of UART multi-byte transmission.
The wait time for STOP bit reception is over 0.5 to 1.5bit from sampling point of the STOP bit, because reception is completed at sampling point of the STOP bit.
Only a wait of one bit is performed, even if the stop bit length has been set to two bits by using the stop bit length select bit (LBFC[2]).

Note 1: Users should only use this bit when reception is switched to transmission (such as during transmission). This is required for the use case of Half-duplex communication in UART mode.
Note 2: Users shall write "0" to this bit in extended UART mode.

LDFC[7:6], LDFC[4] These bits are don't care at UART mode

4.17 LIN / UART IDENTIFIER BUFFER REGISTER (LIDB)

4.17.1 LIN Master mode

Address: 0015h								
Bit	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol	**IDP1**	**IDP0**	**ID[5:0]**					
Initial Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
IDLE Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Operation Mode	R	R	R	R	R	R	R	R

Note: In Self test mode, users should write the transmission value before starting communication. Users can read the inverted value of the received data after frame communication by loopback.

Bit	Symbol	Bit Name	Register Function
b[5:0]	ID	LIN ID select bits	value of ID to be transmitted within the ID Field
b[6]	IDP0	Parity (P0) bit	Value of the parity (P0) bit to be transmitted with ID
b[7]	IDP1	Parity (P1) bit	Value of the parity (P1) bit to be transmitted with ID

LIDB.ID[5:0] LIN ID select bits

Users can not write to these bits if LTRC[0] bit is set.

Users should write the ID value to be transmitted during Header Transmission to these bits.

LIDB.IDP0 Parity (P0) bit

Users can not write to this bit if LTRC[0] bit is set.

Users should write the parity bit (P0) value to be transmitted during Header Transmission to this bit. The parity value is not checked by the RLIN3 module and users shall write the correct value for this bit.

LIDB.IDP1 Parity (P1) bit

Users can not write to this bit if LTRC[0] bit is set.

Users should write the parity bit (P1) value to be transmitted during Header Transmission to this bit. The parity value is not checked by the RLIN3 module and users shall write the correct value for this bit.

4.17.2 LIN Slave mode

Address: 0015h								
Bit	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**B0**
Bit Symbol	**IDP1**	**IDP0**	**ID[5:0]**					
Initial Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
IDLE Mode	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Operation Mode	R	R	R	R	R	R	R	R

* Users can not write to these bits if the module is not configured in Self-Test mode

Bit	Symbol	Bit Name	Register Function
b[5:0]	ID	LIN ID select bits	value of ID in the ID Field
b[6]	IDP0	Parity (P0) bit	Value of the parity (P0) bit
b[7]	IDP1	Parity (P1) bit	Value of the parity (P1) bit

LIDB.ID[5:0] LIN ID select bits

Users can not write to these bits if LMST[0] = "1".

In LIN Slave mode, the value of the ID received by the module during Header Reception will be written in to these bits.

Data in this register is valid only when header is received successfully by the RLIN3 module.

LIDB.IDP0 Parity (P0) bit

Users can not write to this bit if LMST[0] = "1".

In LIN Slave mode, the value of the parity bit (P0) received by the module during Header Reception will be written in to this bit.
The received value will be checked against the value calculated internally if the error detection is enabled, the Identifier Parity Error flag will be set if this bit is not the correct value.

LIDB.IDP1 Parity (P1) bit

Users can not write to this bit if LMST[0] = "1".

In LIN Slave mode, the value of the parity bit (P1) received by the module during Header Reception will be written in to this bit.
The received value will be checked against the value calculated internally if the error detection is enabled, the Identifier Parity Error flag will be set if this bit is not the correct value.

4.17.3 UART mode

Address: 0015h								
Bit	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol	**ID[7:0]**							
Initial Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
IDLE Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Operation Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Bit Name	Register Function
b[7:0]	ID	Reference ID value bits	Reference value of ID for comparison with received value

LIDB.ID[7:0] Reference ID value bits

Users should not write to these bits when a receive operation is in progress (LST.URS = "1").

When module is in normal UART mode and expansion bit data comparison is enabled, then, users should write the reference ID value for comparison into this register.

Note 1: Users shall not be accessed these bits in extended UART mode.

4.18 LIN CHECKSUM BUFFER REGISTER (LCBR)

Address: 0016h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**CKSM[7:0]**							
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R	R	R	R	R	R	R	R
LIN Master	**IDLE Mode**	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1
	Operation Mode	R	R	R	R	R	R	R	R
LIN Slave	**IDLE Mode**	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1
	Operation Mode	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1
UART	**IDLE Mode**	R*2	R*2	R*2	R*2	R*2	R*2	R*2	R*2
	Operation Mode	R	R	R	R	R	R	R	R

*1 Users can not write to this bit if the module is not configured in Self-Test mode (LIN master or LIN slave modes).
*2 Users should not write to LCBR in UART, even if the module is configured in Self-Test mode.

Bit	Symbol	Bit Name	Register Function
b[7:0]	CKSM	LIN Checksum value	value of Checksum in the Response field

LCBR.CKSM[7:0] LIN Checksum value

Users can not write to these bits if the module is not configured in Self-Test mode (LIN master or LIN slave modes).
Users should write to LCBR when LTRC.FTS is 0.

The Checksum value in the Response field is stored in these bits.

The Checksum Buffer Register is updated at the end of the last data group response transmission.
The Checksum Buffer Register is updated at the end of the last data group response reception.

Note 1: These register bits are "Don't care" in UART mode.
Note 2: Users shall not be accessed these bits in extended UART mode.

4.19 UART DATA BUFFER 0 REGISTER (LUDB0)

Address: 0017h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**UDB[7:0]**							
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LIN Master	**IDLE Mode**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Operation Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LIN Slave	**IDLE Mode**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Operation Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
UART	**IDLE Mode**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Operation Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Bit Name	Register Function
b[7:0]	UDB	UART Data byte	value of UART transmission data

LUDB0.UDB[7:0] UART Data byte

Users can not write to these bits if the LTRC[1] is "1".

If the data length selection corresponds to 9 data bytes for UART multi-byte transmission, then the 1st Data value for UART communication is present in this buffer.

Note 1: These bits shall not be accessed in LIN mode.
Note 2: In UART mode, this register is used only for the UART multi-byte transmission.
Note 3: Users shall not be accessed these bits in extended UART mode.

4.20 LIN / UART DATA BUFFER N REGISTER (LDBRN (N=1~8))

Address: 0018h to 001Fh									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**LDB[7:0]**							
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LIN Master	**IDLE Mode**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Operation Mode	R*/W*	R*/W*	R*/W*	R*/W*	R*/W*	R*/W*	R*/W*	R*/W*
LIN Slave	**IDLE Mode**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Operation Mode	R*/W*	R*/W*	R*/W*	R*/W*	R*/W*	R*/W*	R*/W*	R*/W*
UART	**IDLE Mode**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Operation Mode	R*/W*	R*/W*	R*/W*	R*/W*	R*/W*	R*/W*	R*/W*	R*/W*

Bit	Symbol	Bit Name	Register Function
b[7:0]	LDB	LIN Data bytes	value of LIN / UART data

LDBRN.LDB[7:0] LIN Data bytes

The Data value for LIN Response or UART multi-byte transmission is present in these buffers.

*The following shall be followed when accessing these registers:

LIN Master mode:

Transmission

- If the Frame Separate Mode Select Bit is 0, the data buffer registers can only be written when LTRC[0] is 0.
- If the Frame Separate Mode Select Bit is 1, the data buffer registers can only be written when LTRC[1] is 0.

Reception

- Users should not write these registers when LTRC[0] bit is 1 and RLIN3 module is not configured for data group reception
- During data group reception, RLIN3 module shall be configured in Frame Separate mode for LIN Master operation. In this case, the Data buffers are valid when the LTRC[1] bit is "0". This bit needs to be set to allow the RLIN3 module to store the received data into the Data buffers for each group.
- After every reception, the data buffer will be overwritten.
- The data byte in which error is detected is stored in the buffer before reception is stopped.

LIN Slave mode:

- These registers should not be written when LTRC[1] bit is 1 for response transmission or reception or response data group transmission or reception.
- After every reception, the data buffer will be overwritten.
- The data byte in which error is detected is stored in the buffer before reception is stopped.

UART mode:

- These registers are valid only if UART multi-byte transmission is used.
- The data buffers should not be written when LTRC[1] bit is 1.

Note 1: Users shall not be accessed these bits in extended UART mode.

4.21 UART OPERATION ENABLE REGISTER (LUOER)

Address: 0020h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**-**	**-**	**-**	**-**	**-**	**-**	**UROE**	**UTOE**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0	R0
LIN Master	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W	R/W
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W	R/W
LIN Slave	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W	R/W
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W	R/W
UART	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W	R/W
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W	R/W

Bit	Symbol	Bit Name	Register Function
b[0]	UTOE	UART Transmission Operation Enable Bit	0: Stops transmission operation 1: Enables transmission operation
b[1]	UROE	UART Reception Operation Enable Bit	0: Stops reception operation 1: Enables reception operation
b[7:2]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LUOER.UTOE UART Transmission Operation Enable Bit

Users can not write to this bit if LMST[0] is "0".

This bit is cleared when RLIN3 module is in reset mode i.e. LMST[0] bit ='0'.
This bit controls the frame transmission in UART mode

Note 1: This bit is "Don't Care" in LIN mode.
Note 2: Users shall use SW reset if users abort the communication in UART mode.

LUOER.UROE UART Reception Operation Enable Bit

Users can not write to this bit if LMST[0] is "0".

This bit is cleared when RLIN3 module is in reset mode i.e. LMST[0] bit ='0'.
This bit controls the frame reception in UART mode

Note 1: This bit is "Don't Care" in LIN mode.
Note 2: Users shall use SW reset if users abort the communication in UART mode.
Note 3: Users shall not set this bit during multi-byte transmission in UART mode.

4.22 UART OPTION REGISTER1 (LUOR1)

Address: 0021h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**-**	**-**	**-**	**UECD**	**UTIGTS**	**UEBDCE**	**UEBDL**	**UEBE**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R0/W0	R0/W0	R0/W0	R/W	R/W	R/W	R/W	R/W
LIN Master	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R	R/W	R	R	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R	R/W	R	R	R
LIN Slave	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R	R/W	R	R	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R	R/W	R	R	R
UART	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R	R/W	R	R	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R	R/W	R	R	R

Bit	Symbol	Bit Name	Register Function
b[0]	UEBE	UART Expansion Bit Enable Bit	0: Disables expansion bit operation 1: Enables expansion bit operation
b[1]	UEBDL	UART Expansion Bit Detection Level Select Bit	0: Selects expansion bit value "0" as expansion bit detection level 1: Selects expansion bit value "1" as expansion bit detection level
b[2]	UEBDCE	UART Expansion Bit Data Comparison Enable Bit	0: No comparison 1: Compares UART 7bit/8bit/9bit Receive Data Register and LIN / UART Identifier Buffer Register when the level selected for UART Expansion Bit Detection Level Select Bit has been detected as the expansion bit
b[3]	UTIGTS	UART Transmission Interrupt Generation Timing Select Bit	0: Outputs transmission interrupt request upon transmission start 1: Outputs transmission interrupt request upon transmission completion
b[4]	UECD	UART Expansion Bit Comparison Disable Bit	0: Expansion bit comparison enable 1: Expansion bit comparison disable
b[7:5]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LUOR1.UEBE UART Expansion Bit Enable Bit

Users can not write to this bit if LMST[0] is "1". This bit should not be set for UART multi-byte transmission.

Note 1: This bit is "Don't Care" in LIN mode.

This bit controls the Expansion bit function in UART mode

LUOR1.UEBDL UART Expansion Bit Detection Level Select Bit

Users can not write to this bit if LMST[0] is "1". This bit should not be set in UART multi-byte transmission.
Note 1: This bit is "Don't Care" in LIN mode.
Note 2: Users shall write "0" to this bit in extended UART mode.

This bit selects the Expansion bit detection level in UART mode

LUOR1.UEBDCE UART Expansion Bit Data Comparison Enable Bit

Users can not write to this bit if LMST[0] is "1". This bit should not be set in UART multi-byte transmission.

Note 1: This bit is "Don't Care" in LIN mode.
Note 2: Users should not set this bit if LUOR1.UEBE bit is not set.
Note 3: Users should not set this bit if LUOR1.UECD bit is set.
Note 4: Users should not set this bit if LUSC.UWC bit is set.
Note 5: Users shall write "0" to this bit in extended UART mode.

This bit controls the Expansion bit data comparison function in UART mode

LUOR1.UTIGTS UART Transmission Interrupt Generation Timing Select Bit

Note 1: This bit is "Don't Care" in LIN mode.

This bit controls the Transmission Interrupt generation timing in UART mode

LUOR1.UECD UART Expansion Bit Comparison Disable Bit

Users can not write to this bit if LMST[0] is "1". This bit should not be set in UART multi-byte transmission.

This bit controls Expansion bit comparison function in UART mode.

Note 1: This bit is "Don't Care" in LIN mode.
Note 2: Users should not set this bit if LUOR1.UEBDCE bit is set.
Note 3: Users shall write "1" to this bit in extended UART mode.

4.23 UART OPTION REGISTER2 (LUOR2)

Address: 0022h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**-**	**-**	**-**	**-**	**UBCOE**	**UDPS**	**UFST[1:0]**	
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
RST Mode		R0/W0	R0/W0	R0/W0	R0/W0	R/W*1	R/W*1	R/W*1	R/W*1
LIN Master	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R	R	R	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R	R	R	R
LIN Slave	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R	R	R	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R	R	R	R
UART	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R	R	R	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R	R	R	R

*1 Users can write to these bits if LMD[7] is set.
Users should not write to these bits in LIN Master and LIN Slave even if LMD[7] is set.

Bit	Symbol	Bit Name	Register Function
b[1:0]	UFST	UART Frame Start Timing of Loop Back Delayed Data Consistency Select Bits	00: Data consistency check is OFF 01: Transmit start ～ (1/Bit clock) ×4 10: Transmit start ～ (1/Bit clock) ×5 11: Transmit start ～ (1/Bit clock) ×6
b[2]	UDPS	UART Data Phase Select Bit	0: Baud rate clock*2 non-inverted 1: Baud rate clock*2 inverted.
b[3]	UBCOE	UART Baud Rate Clock*2 Output Enable Bit	0: Baud rate clock*2 output disable (Output is "0") 1: Baud rate clock*2 output enable
b[7:4]	-	Reserved	These bits are always read as 0. The write value should always be 0.

*2 Baud rate clock is the bit timing clock.

LUOR2.UFST[1:0] UART Frame Start Timing of Loop Back Delayed Data Consistency Select Bits

Users can not write to these bits if LMST[0] is "1".

These bits control the timing delay for the loop-back frame start.

The initial value of these bits is 01b if LMD.EUMS is "1",
These bits become the reservation bit, read value is always 00b if LMD.EUMS is "0".

Note 1: These bits are "Don't Care" in LIN mode.

LUOR2.UDPS UART Data Phase Select Bit

Users can not write to this bit if LMST[0] is "1".

This bit controls the synchronisation of the TxD output to the serial clock.

Note 1: This bit is "Don't Care" in LIN mode.

LUOR2.UBCOE UART Baud Rate Clock Output Enable Bit

Users can not write to this bit if LMST[0] is "1".

This bit controls the baud rate clock output.

Note 1: This bit is "Don't Care" in LIN mode.
Note 2: Users can output UART Baud Rate Clock only in Extended UART mode.

4.24 UART TRANSMIT START DELAY CONTROL REGISTER (LUTDCR)

Address: 0023h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**-**	**-**	**-**	**UTSDV[4:0]**				
Initial Value		**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
RST Mode		R0/W0	R0/W0	R0/W0	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1
LIN Master	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1
	Operation Mode	R0/W0	R0/W0	R0/W0	R	R	R	R	R
LIN Slave	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1
	Operation Mode	R0/W0	R0/W0	R0/W0	R	R	R	R	R
UART	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1
	Operation Mode	R0/W0	R0/W0	R0/W0	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1

*1 Users can write to these bits if LMD[7] is set.
Users should not write to these bits in LIN Master and LIN Slave even if LMD[7] is set.

Bit	Symbol	Bit Name	Register Function
b[4:0]	UTSDV	UART Transmit Start Delay Value Select Bit	00H: UART Transmission Start delay function is not operation. 01H: (1/Bit Clock)×1 : : : 18H: (1/Bit Clock)×24 19H: (1/Bit Clock)×25 : : : 1FH: (1/Bit Clock)×31
b[7:5]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LUTDCR.UTSDV[4:0] UART Transmit Start Delay Value Select Bit

These bits control the timing delay for the frame start after the transmit request is generated.
If transmit request is generated during reception, then the delay is applicable only after the STOP bit is detected for the frame reception.

The initial value of these bits is 10000b if LMD.EUMS is "1".
These bits become the reservation bit, read value is always 00000b if LMD.EUMS is "0".

Note 1: These bits are "Don't Care" in LIN mode.
Note 2: Users should not write to LUTDCR until the UART Transmission Interrupt is set after the UART transmission data is written into LUTDR.

4.25 UART 7BIT / 8BIT / 9BIT TRANSMIT DATA REGISTER (LUTDR)

Address: 0024h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**UTD[7:0]**							
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LIN Master	**IDLE Mode**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Operation Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LIN Slave	**IDLE Mode**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Operation Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
UART	**IDLE Mode**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Operation Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0025h									
Bit		**b15**	**b14**	**b13**	**b12**	**b11**	**b10**	**b9**	**b8**
Bit Symbol		**-**	**-**	**-**	**-**	**-**	**-**	**-**	**UTD[8]**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W
LIN Master	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W
LIN Slave	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W
UART	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W

Bit	Symbol	Bit Name	Register Function
b[8:0]	UTD	UART 7bit / 8bit / 9bit Transmit Data	Value of transmit data in UART mode
b[15:9]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LUTDR.UTD[8:0] UART 7bit / 8bit / 9bit Transmit Data

The Data value for UART transmission is present in this register.

Note 1: These bits are "Don't Care" in LIN mode.
Note 2: Users should not use 8-bit access while writing data into this register in 9bit communication.
Note 3: A write access to this register triggers a start of transmission if UART Transmission Operation Enable Bit is set.
Note 4: In Extended UART mode, Transmission start depends upon the LUTDCR register configuration. The LUTDCR.UTSDV bits control the frame start timing after transmit request is generated.
Note 5: Users can use 8-bit access when reading data from this register.
Note 6: Users should not write to this register during UART multi-byte transmission.
Note 7: Users should not write to this register if transmission has already been triggered by writing to the LUWTDR register.

Note 8: When RLIN3 is in UART mode and the transmit interrupt generation timing is transmission

completion (UTIGTS = 1), if users write to the transmission buffer(LUTDR) before the transmission interrupt occurs, the transmission interrupt does not occur.

Transmission Condition	UTD[8]	UTD[7]	UTD[6]	UTD[5]	UTD[4]	UTD[3]	UTD[2]	UTD[1]	UTD[0]
7bit LSB-first	*	*	Data6	Data5	Data4	Data3	Data2	Data1	Data0
7bit MSB-first	*	*	Data0	Data1	Data2	Data3	Data4	Data5	Data6
8bit LSB-first	*	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
8bit MSB-first	*	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7
9bit LSB-first	Data8	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
9bit MSB-first	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7	Data8

4.26 UART 7BIT / 8BIT / 9BIT RECEIVE DATA REGISTER (LURDR)

Address: 0026h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**URD[7:0]**							
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R	R	R	R	R	R	R	R
LIN Master	**IDLE Mode**	R	R	R	R	R	R	R	R
	Operation Mode	R	R	R	R	R	R	R	R
LIN Slave	**IDLE Mode**	R	R	R	R	R	R	R	R
	Operation Mode	R	R	R	R	R	R	R	R
UART	**IDLE Mode**	R	R	R	R	R	R	R	R
	Operation Mode	R	R	R	R	R	R	R	R

Address: 0027h									
Bit		**b15**	**b14**	**b13**	**b12**	**b11**	**b10**	**b9**	**b8**
Bit Symbol		**-**	**-**	**-**	**-**	**-**	**-**	**-**	**URD[8]**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R
LIN Master	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R
LIN Slave	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R
UART	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R

Bit	Symbol	Bit Name	Register Function
b[8:0]	URD	UART 7bit / 8bit / 9bit Receive Data	Value of received data in UART mode
b[15:9]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LURDR.URD[8:0] UART 7bit / 8bit / 9bit Receive Data

Users can not write to these bits

The Data value for UART reception is present in this buffer.

LURDR.URD register is updated at the stop bit detection of a UART frame reception. This will be done even if errors occur for Parity and STOP bit. The register will not be updated if overrun error occurs However, the register is updated if overrun error is disabled.
LURDR.URD register is not updated when LUOR1.UEBDCE is set and Expansion Bit or ID data is mismatch in UART Expansion Bit mode. Please refer to 6.11 UART MODE -EXPANSION BIT.

Note 1: These bits are "Don't Care" in LIN mode.
Note 2: If the RLIN3 module is configured UART 7bit / 8bit mode, Users can use 8-bit access when reading data from this register.
Note 3: If the RLIN3 module is configured UART 9bit mode, Users should use 16-bit access when reading

data from this register.

Reception Condition	URD[8]	URD[7]	URD[6]	URD[5]	URD[4]	URD[3]	URD[2]	URD[1]	URD[0]
7bit LSB-first	0	0	Data6	Data5	Data4	Data3	Data2	Data1	Data0
7bit MSB-first	0	0	Data0	Data1	Data2	Data3	Data4	Data5	Data6
8bit LSB-first	0	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
8bit MSB-first	0	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7
9bit LSB-first	Data8	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
9bit MSB-first	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7	Data8

4.27 UART 7BIT / 8BIT / 9BIT WAIT TRANSMIT DATA REGISTER (LUWTDR)

Address: 0028h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**UWTD[7:0]**							
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LIN Master	**IDLE Mode**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Operation Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LIN Slave	**IDLE Mode**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Operation Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
UART	**IDLE Mode**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Operation Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0029h									
Bit		**b15**	**b14**	**b13**	**b12**	**b11**	**b10**	**b9**	**b8**
Bit Symbol		**-**	**-**	**-**	**-**	**-**	**-**	**-**	**UWTD[8]**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W
LIN Master	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W
LIN Slave	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W
UART	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W

Bit	Symbol	Bit Name	Register Function
b[8:0]	UWTD	UART 7bit / 8bit / 9bit Wait Transmit Data	Value of transmit data in UART mode with STOP bit reception
b[15:9]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LUWTDR.UWTD[8:0] UART 7bit / 8bit / 9bit Wait Transmit Data

The Data value for UART transmission is present in this buffer.
Please refer to Section 6.8 for details of the use of this buffer.
The wait time for STOP bit reception is over 0.5 to 1.5bit from sampling point of the STOP bit, because reception is completed at sampling point of the STOP bit. Only a wait of one bit is performed, even if the stop bit length has been set to two bits by using the stop bit length select bit (LBFC[2]).
This buffer is used when requiring Half Duplex functionality

The read value of the LUWTDR register is the read value of the LUTDR register.

Note 1: These bits are "Don't Care" in LIN mode.
Note 2: Users should not use 8-bit access while writing data into this register in 9bit communication.
Note 3: A write access to this register triggers a start of transmission if UART Transmission Operation Enable bit is set.
Note 4: Users can use 8-bit access when reading data from this register.

Note 5: Users shall not write to this register during UART multi-byte transmission.
Note 6: Users shall only use this register when reception is switched to transmission. Additionally, users shall only write to this register during STOP bit of current reception. This is required for the Half-duplex UART mode operation.
Note 7: Users shall not be accessed this bit in extended UART mode.

Transmission Condition	UWTD[8]	UWTD[7]	UWTD[6]	UWTD[5]	UWTD[4]	UWTD[3]	UWTD[2]	UWTD[1]	UWTD[0]
7bit LSB-first	*	*	Data6	Data5	Data4	Data3	Data2	Data1	Data0
7bit MSB-first	*	*	Data0	Data1	Data2	Data3	Data4	Data5	Data6
8bit LSB-first	*	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
8bit MSB-first	*	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7
9bit LSB-first	Data8	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
9bit MSB-first	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7	Data8

4.28 UART 7BIT / 8BIT / 9BIT RECEIVE DATA REGISTER FOR EMULATION (LURDE)

Address: 002Ah									
Bit		b7	b6	b5	b4	b3	b2	b1	b0
Bit Symbol		RDE[7:0]							
Initial Value		0	0	0	0	0	0	0	0
RST Mode		R	R	R	R	R	R	R	R
LIN Master	IDLE Mode	R	R	R	R	R	R	R	R
	Operation Mode	R	R	R	R	R	R	R	R
LIN Slave	IDLE Mode	R	R	R	R	R	R	R	R
	Operation Mode	R	R	R	R	R	R	R	R
UART	IDLE Mode	R	R	R	R	R	R	R	R
	Operation Mode	R	R	R	R	R	R	R	R

Address: 002Bh									
Bit		b15	b14	b13	b12	b11	b10	b9	b8
Bit Symbol		-	-	-	-	-	-	-	RDE[8]
Initial Value		0	0	0	0	0	0	0	0
RST Mode		R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R
LIN Master	IDLE Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R
LIN Slave	IDLE Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R
UART	IDLE Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R

Bit	Symbol	Bit Name	Register Function
b[8:0]	RDE	UART 7bit / 8bit / 9bit Receive data bits for Emulation	The value of UART 7bit / 8bit / 9bit receive data register
b[15:9]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LURDE.RDE[8:0] UART 7bit / 8bit / 9bit Receive data bits for Emulation

The Data value for LURDR register can be read in this register.

Users can not write to these bits

Note 1: These bits are "Don't Care" in LIN mode.
Note 2: Users can use 8-bit access when reading data from this register.
Note 3: This register is used to access the Received data in Emulation mode. It should be accessed in Emulation mode.

Reception Condition	RDE[8]	RDE[7]	RDSE[6]	RDE[5]	RDE[4]	RDE[3]	RDE[2]	RDE[1]	RDE[0]
7bit LSB-first	0	0	Data6	Data5	Data4	Data3	Data2	Data1	Data0
7bit MSB-first	0	0	Data0	Data1	Data2	Data3	Data4	Data5	Data6
8bit LSB-first	0	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
8bit MSB-first	0	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7
9bit LSB-first	Data8	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
9bit MSB-first	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7	Data8

4.29 LIN SLAVE BREAK/SYNC FIELD STATUS REGISTER (LBSS)

Address: 0030h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**-**	**-**	**-**	**-**	**-**	**-**	**SYCC**	**BRKC**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0	R0
LIN Master	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0	R0
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0	R0
LIN Slave	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W0C	R/W0C
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R/W0C	R/W0C
UART	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0	R0
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0	R0

Note: For this register, when only a single bit is to be cleared by the program, do not use bit clear instruction - use the MOV instruction to ensure that only the specified bit is cleared. Then the other bits remain set to "1". Writing "1" gives no influence to the bit values.

Bit	Symbol	Bit Name	Register Function
b[0]	BRKC	LIN Break Field Reception flag	0: LIN Break Field Rx not completed 1: LIN Break Field Rx completed successfully
b[1]	SYCC	LIN Sync Field Reception flag	0: LIN Sync Field Rx not completed 1: LIN Sync Field Rx completed successfully
b[7:2]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LBSS.BRKC LIN Break Field Reception flag.

Users can not write to this bit if LMST[0] bit is "0".
Users should use this bit only for the re-transmission of a wake-up signal.(Refer to)

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when Break field is successfully reception in LIN Slave mode

Refer to Section 6.2 and 8.4 for details about this flag.

Designers information:
When a Frame Timeout Error is detected during a break field reception, the frame is aborted and the RLIN3 transitions to the Break low wait state, so the following Sync field is not detected. However, this bit is set at the end of break field after the Frame Timeout Error, because the break field detection circuit continues to operate until the break delimiter is detected.

LBSS.SYCC LIN Sync Field Reception flag.

Users can not write to this bit if LMST[0] bit is "0".
Users should use this bit only for the re-transmission of a wake-up signal.(Refer to)

Clearing condition(s):
This bit is cleared by writing "0" to it.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when Sync field is successfully reception in LIN Slave mode

Refer to Section 6.2 and 8.4 for details about this flag.

4.30 LIN SLAVE RESPONSE SPACE STATUS REGISTER (LRSS)

Address: 0034h									
Bit		**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Bit Symbol		**-**	**-**	**-**	**-**	**-**	**-**	**-**	**RSDD**
Initial Value		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
RST Mode		R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0
LIN Master	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0
LIN Slave	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R
UART	**IDLE Mode**	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0
	Operation Mode	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0/W0	R0

Bit	Symbol	Bit Name	Register Function
b[0]	RSDD	Response Space Dominant Detection Flag	0: No dominant detected. 1: Dominant detected.
b[7:1]	-	Reserved	These bits are always read as 0. The write value should always be 0.

LRSS.RSDD Response Space Dominant Detection Flag.

Users can not write to this bit.
This bit is valid only for LIN response transmission in LIN slave mode.
This bit is invalid when a bit error is occurred in the transmission of the response space.

Clearing condition(s):
This bit is cleared when Sync field is received.
This bit is cleared when RLIN3 module is transitioning to the reset mode.

Setting condition(s):
This bit is set when a dominant level of 0.5 Tbit or more is detected from the completion of the header reception (the stop bit of the ID field) to the start of transmission(*) in LIN slave mode.

Note(*) : When LSC.IBHS =0h, it is the transmission of the start bit of the 1st Data byte.
When LSC.IBHS =1 to 7h, it is the transmission of the response space.

Refer to Section 5.2.3, 6.4 and 8.5 for details about this flag.

5 STATE TRANSITION

5.1 OVERVIEW

The RLIN3 module transits to Reset State automatically where all the functions are initialized, if HW reset is cleared. From Reset state, the module can be put in either of the following states:

1. Reset mode
2. LIN mode
    - LIN Master mode
        - LIN Master Normal
        - LIN Master WUP
    - LIN Slave mode
        - LIN Slave Normal
        - LIN Slave WUP
3. UART mode
4. LIN Self Test mode.

5.1.1 Reset mode

- All output signals are initialized.
- All operations are initialized.
- When HW Reset or SW Reset (LMST.OMM0 is cleared to "0") is applied, the LST & LEST register bits are cleared on transition to Reset mode. However, configuration and control registers are not affected.

5.1.2 LIN Master mode

The following functions are executed in this mode:

- Header transmission
- Response transmission
- Response reception
- Detection of errors

5.1.3 LIN Slave mode

The following functions are executed in this mode:

- Header reception
- Response transmission
- Response reception
- Detection of errors

5.1.4 LIN Wake-up mode

The following functions are executed in this mode:

- Wake-up signal transmission
- Wake-up signal reception
- Detection of errors (Bit error and Physical error during Wake-up transmission)

5.1.5 UART mode

The following functions are executed in this mode:

- UART frame transmission from 7bit/8bit/9bit transmit data register or 7bit/8bit/9bit Wait transmit data register
- UART frame transmission from Data Buffer N registers.
- UART frame reception in 7bit/8bit/9bit receive data register
- Expansion bit transmission
- Expansion bit reception with data comparison
- Expansion bit reception without data comparison
- Detection of errors

5.1.6 LIN self test mode

The following functions are executed in this mode:

- Header transmission (only in LIN Master mode)
- Header reception (only in LIN slave mode)
- Response transmission
- Response reception
- Detection of errors

Note 1: In self test mode, the transmission data is looped back internally into the reception data path logic and the module is disconnected from the LIN bus.

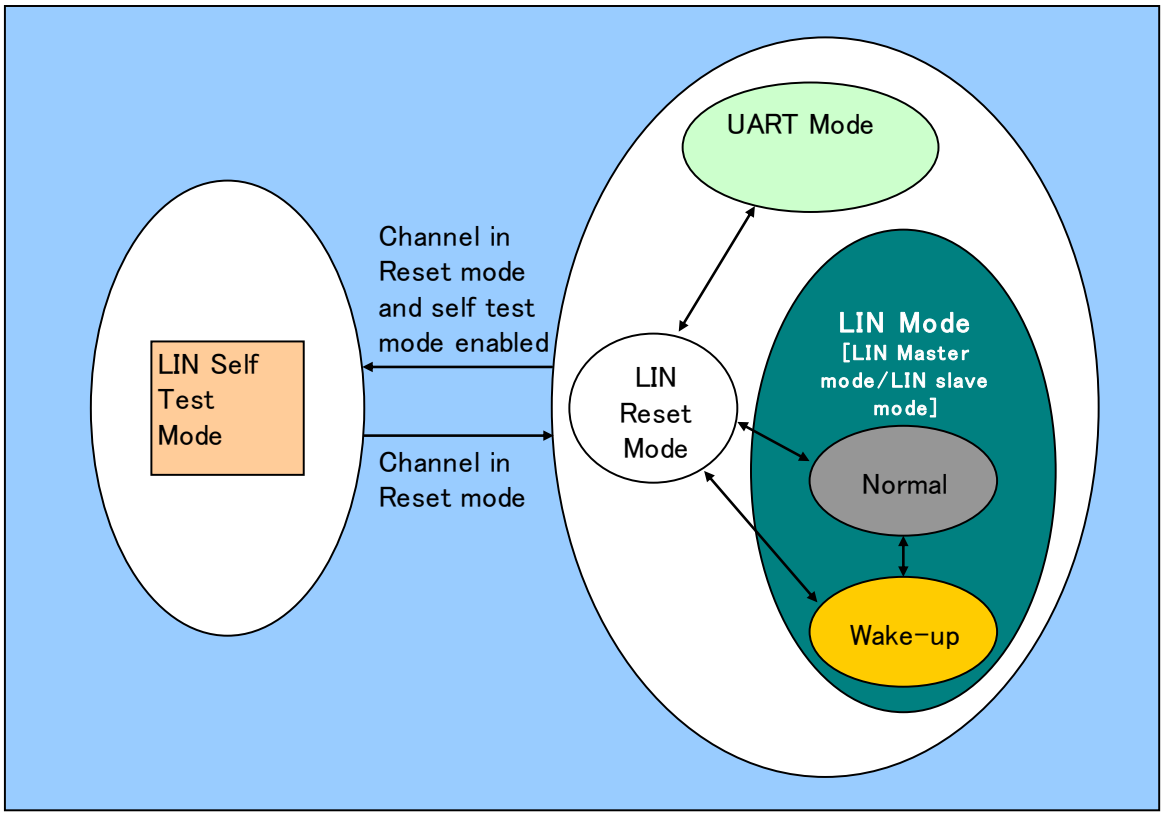


Figure 5-1: State transition diagram

Note 1: Transition from Wake-up to Normal & vice versa is allowed only when there is no communication requested i.e. LTRC[0] == 0.
Note 2: Transitions between LIN Master mode, LIN Slave mode and UART mode is only allowed when the RLIN3 module is in reset state (LMST[0] is equal to "0").

5.2 LIN CONTROLLER OPERATION DESCRIPTION

5.2.1 LIN Master mode Frame header handling

The figure below illustrates flow of the LIN Controller operation. When the LIN Controller detects a Bit Error during handling a header it is flagged at bit or byte boundary according to field & aborts communication.

1. Byte boundary: When in Sync field, ID.
2. Bit boundary: When in break low, Break delimiter, Inter-byte Header space.

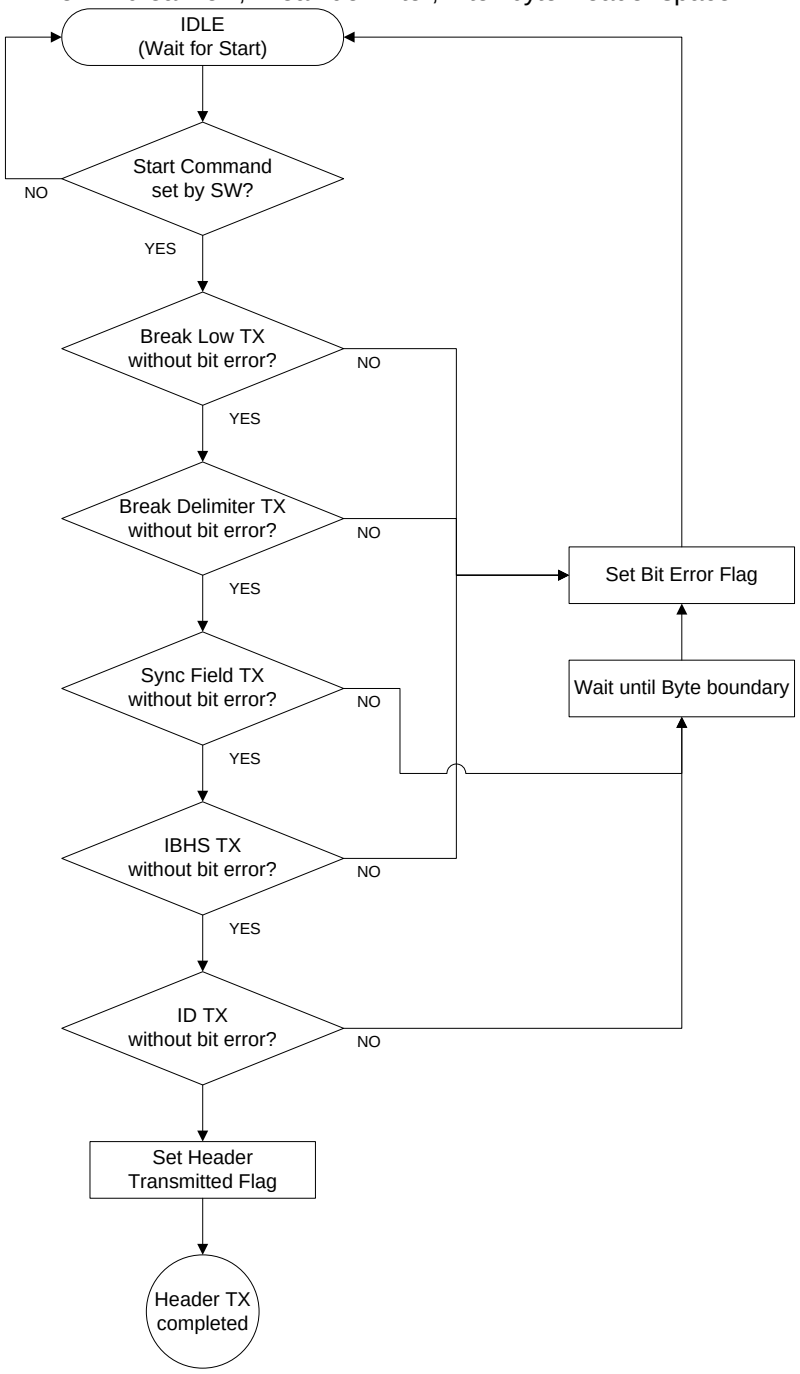


Figure 5-2: LIN Master mode Header Transmission Flow

5.2.2 LIN Slave mode Frame header handling

Break field detection and break delimiter detection operates different dependent of the baud rate detection mode.
Figure 5-3 below illustrates flow of the LIN Controller operation with fixed baud rate mode.
When LTRC[0] bit is set, then the RLIN3 module waits for the detection of a "falling-edge" and "low-level" on the RxD pin.
When "falling-edge" is detected, then, the module checks if the number of continuous "LOW" bits are detected (9.5 or 10.5 Tbits). If yes, then it waits for at least 0.5Tbit corresponding to Break delimiter and then waits for the SYNC field reception followed by ID field reception.

Figure 5-4 below illustrates flow of the LIN Controller operation in automatic baud rate detection mode.
When LTRC[0] bit is set, then the RLIN3 module waits for the detection of a "low-level" on the RxD pin.
When "low-level" is detected, then, the module starts counting the number of "LOW" bits. Following the detection of a "falling-edge" SYNC field reception starts followed by ID field reception. Details about the automatic baud rate detection function can be found in section 7.3.

Following this point the header handling is identical for fixed baud rate mode.

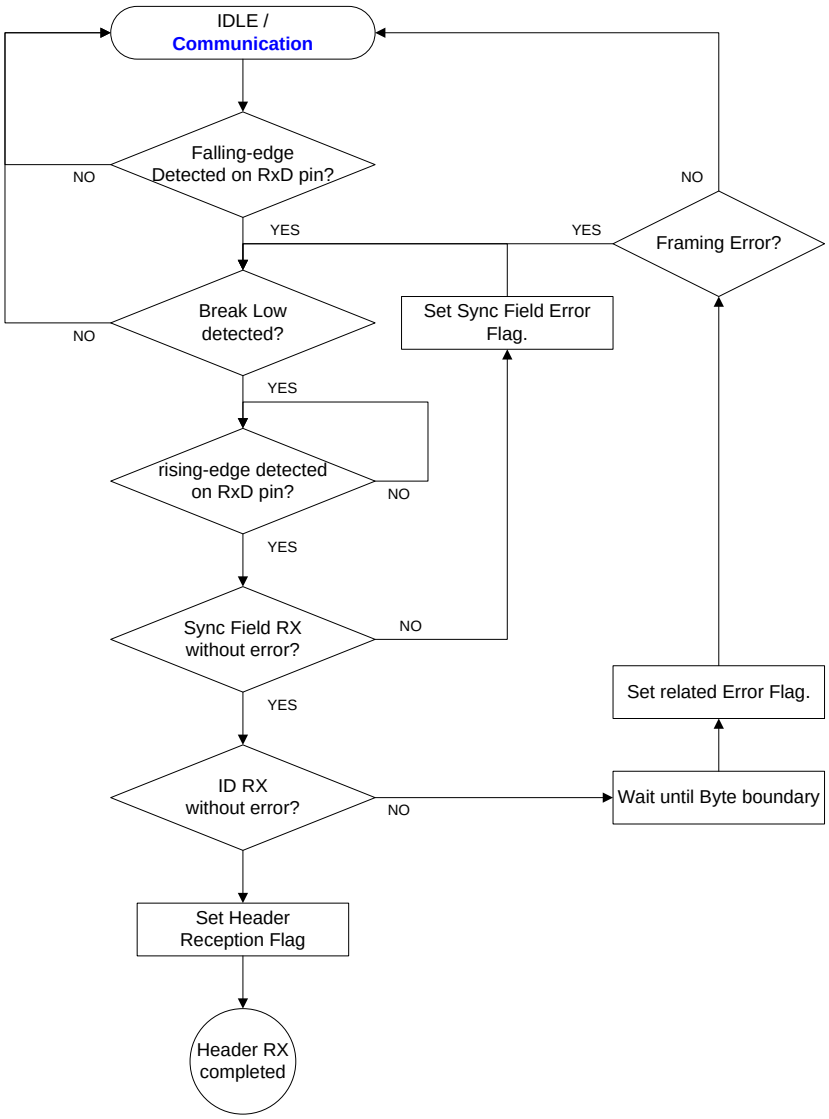


Figure 5-3: LIN Slave mode Header Reception Flow with fixed baud rate

Following this point the header handling is identical for automatic baud rate mode.

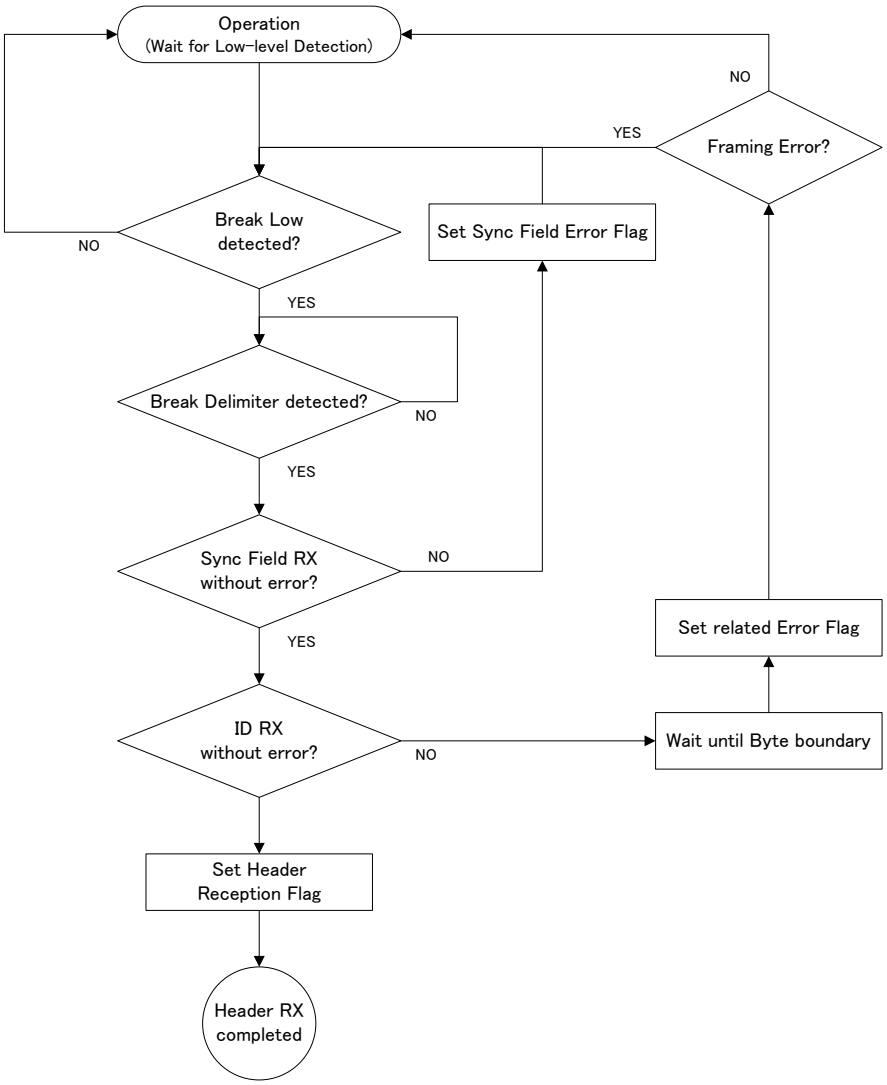


Figure 5-4: LIN Slave mode Header Reception Flow with automatic baud rate detection mode

If a SYNC field Error is detected during Header reception, operation is aborted and the flow stay to Header reception.
If error is detected in the last bit of the SYNC field (STOP bit), Sync field error detection is disabled and Framing error is enabled, Framing error is not set since SYNC field is not treated as a Data field.
If an Identifier parity error is detected during Header reception, operation is aborted and flow stay to Header reception.
If a Framing Error is detected during ID field reception, the operation is aborted and the flow stay to Header reception.
If ID Parity error detection and Framing error detection are enabled and both errors occur in ID field, then both, ID Parity as well as Framing error flag bits will be set in this case at the end of ID field.

Note 1: RLIN3 will be able to detect a new Break field during ID reception when configured in LIN slave mode.

Designers information:
At that time, if Break Low width select is set to 9.5Tbits in fixed baud rate mode, errors detected by byte boundary with new Break may be faster 0.5Tbit.

5.2.2.1 ID parity check function

When the ID parity check is selected, the ID parity bits (P0, P1) are checked when the received ID is stored into the ID register. At that time, if either parity bit includes an error, then, an ID parity error flag is set, a status interrupt request signal is generated instead of a reception complete interrupt request signal and the ID is stored into the ID register.

If ID Parity error detection is disabled, then any errors in the ID Parity are ignored.

5.2.3 LIN response handling (Master / slave mode)

The operation of the Frame State Machine is shown below in Figure 5-5.

If a Bit Error is detected during Response transmission, the operation is aborted and a Bit Error is flagged at bit or byte boundary according to field, and the flow stay to Operation.

1. Byte boundary: When in Data field, Checksum field.
2. Bit boundary: When in Response space, Inter-byte space.

If a Framing Error is detected during Response reception, the operation is aborted and the flow stay to Operation.

If a Response Timeout Error is detected during response transmission or reception, the operation is aborted at the moment of detection.

If a Frame Timeout Error is detected on transmission or reception, the operation is aborted at the moment of detection.

1. Successful transmission flag is set only when the transmission is successful up to CHECKSUM without frame timeout error detection.
2. Successful reception flag is set only when reception of CHECKSUM and judgement are successful without frame timeout error detection.

If a dominant level of 0.5 Tbit or more is detected during Response space (from the completion of the header reception to the start of transmission) in LIN slave mode, the operation is continued and the Response Space Dominant Detection flag(LRSS[0]) is set to "1".

Note 1: RLIN3 will be able to detect a new Break field during Response TX or RX when configured in LIN slave mode.

Designers information:
At that time, if Break Low width select is set to 9.5Tbits in fixed baud rate mode, errors detected by byte boundary with new Break may be faster 0.5Tbit.

The following process should be followed for LIN slave mode after reception of Header:

If a ID stored into the ID register is not a target when header reception is completed, then
LIN No Response bit should be set and subsequent transmission and reception processing are stopped (responses are ignored).

If a ID stored into the ID register is a target when header reception is completed, then following options are possible:

For a response reception ID, the Response Communication start bit is set after the configuration of response data length, Checksum type and Communication direction.

For a response transmission ID, the Response Communication start bit is set after the configuration of response data length, Checksum type, Communication direction and transmit data.

The ID should be processed before receiving the 1st byte of the response is completed. Otherwise, a response preparation error occurs.
During response reception or response transmission, transmission and reception operations are stopped if a

status interrupt request signal has been generated due to an error. In this case, the module waits for the next Break Field reception to be performed.

5.2.3.1 Automatic checksum function

Checksum is automatically calculated for the LIN Frames in LIN Master / slave mode.
The Checksum type can be selected for the LIN Frames in IDLE state for LIN Master mode (bit LTRC[0] is "0") and when response is not enabled for LIN slave mode (bit LTRC[1] is "0").
During response transmission, calculation is performed for each data byte and the calculation result is automatically added to the end of response transmission and transmitted. The transmitted Checksum value can be read in the Checksum register at the end of successful transmission.
During response reception, calculation is performed for each received data byte and the stored data and calculation result are automatically compared when the received checksum is stored into the Checksum buffer.
A reception complete interrupt request signal is generated when the comparison result is correct.
If the received Checksum value does not match the calculated Checksum value, then, a status interrupt request signal is generated instead of a reception complete interrupt request signal, a checksum error flag is set, and the received checksum is stored into the Checksum buffer.

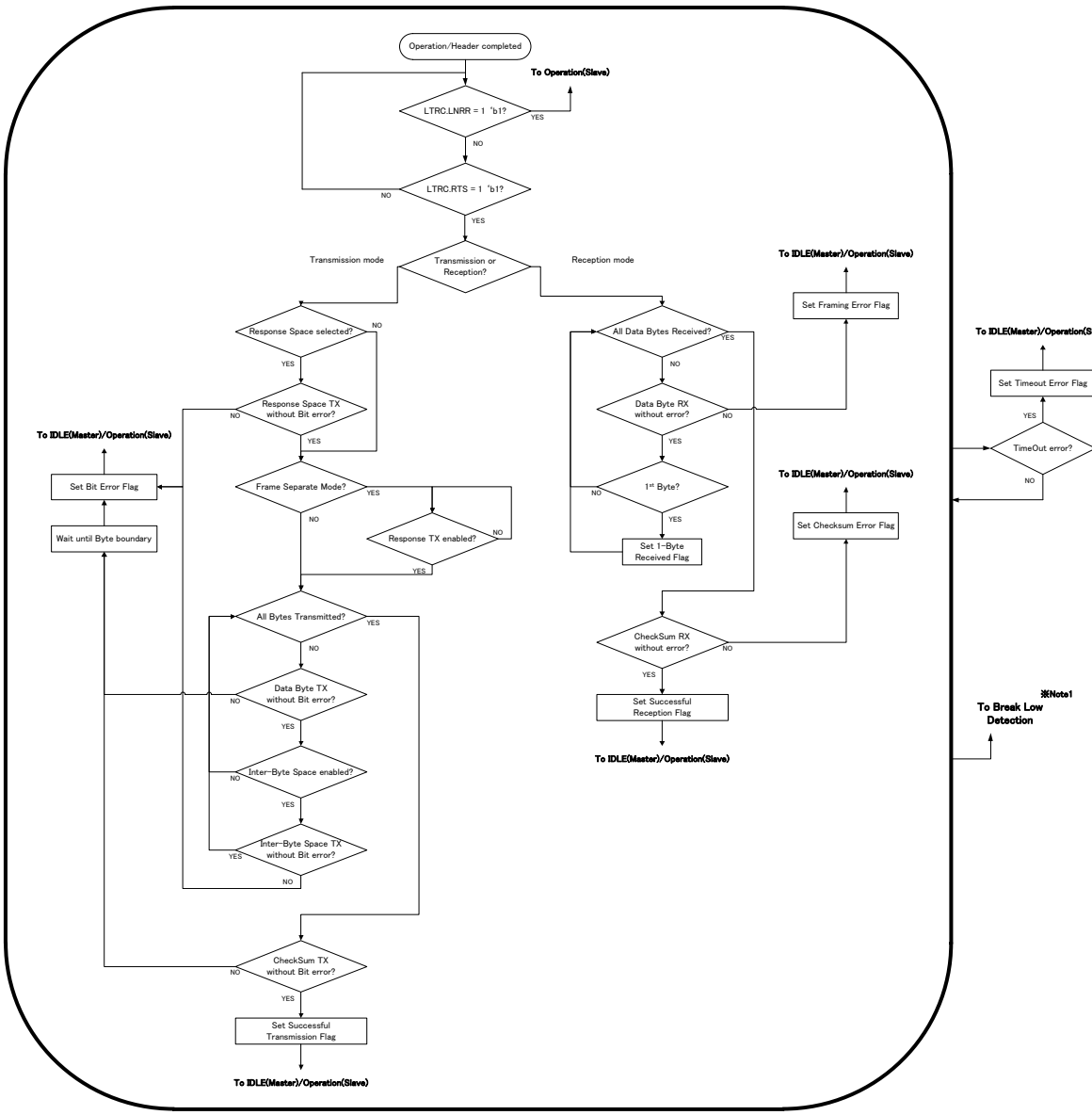


Figure 5-5: LIN mode Response Handling Flow (Master / Slave)

Note1: Break Detection is executed by Falling-edge Detection in LIN Slave mode, even if LIN response is handled.

5.2.3.2 Data group response transmission/reception function

In normal LIN communication, a response is no more than or equal to 9 bytes (including the checksum field). In case responses are more than or equal to 9 bytes (plus checksum field) users can use response communication.

In this case, response preparation error detection, Bit error detection, Framing error detection and automatic checksum function are valid.

If number of data bytes is more than or equal to 9, then the LIN Successive selection bit should be set to "1", for the 1st group of data bytes. After the 1st group of data bytes have been transmitted (or received), users should check if the next group of data bytes is the last group and the LIN Successive selection bit should be cleared to "0", for the last group of data bytes. The checksum is appended to the last data group.

Users should not use Frame Combined mode configuration for data group response communication in LIN Master mode.

Users can modify the Data length for each data group in data group response transmission by writing to the LDFC register bits when the LTRC[1] bit is "0".

Note 1: RLIN3 will be able to detect a new Break field during Response TX or RX when configured in LIN slave mode.

Designers information:
At that time, if Break Low width select is set to 9.5Tbits in fixed baud rate mode, errors detected by byte boundary with new Break may be faster 0.5Tbit.

5.2.4 UART mode

The communication flow in UART mode is described below.

5.2.4.1 UART Transmission

Transmission is enabled by setting the UART Transmission Enable bit (LUOER.UTOE). There are 2 modes of Transmission.

UART multi-byte Transmission:
The RLIN3 module can transmit up to 9 data bytes based on the UART Transmission byte count value. Transmission operation is started when the UART multi-byte transmission start bit is set. Transmission Interrupt is generated when transmission of all programmed Bytes is complete. Timing of the UART Transmission Interrupt is based on the UART Transmission Interrupt generation Timing Select bit configuration.

If the LTRC[1] bit is set when UART transmission is enabled, then the transmission will always occur from the Data Buffer N registers (see section 0). The 7bit/8bit/9bit transmit data register or 7bit/8bit/9bit wait transmit data register can not be used for transmission in this case.

For full-duplex communication, users can start transmission while reception is in progress.

For half-duplex communication, users shall not set the LTRC[1] bit if reception is in progress (UART reception status bit is set to "1").

The RLIN3 module can detect Bit Error even in the Inter-byte space between Data Bytes.

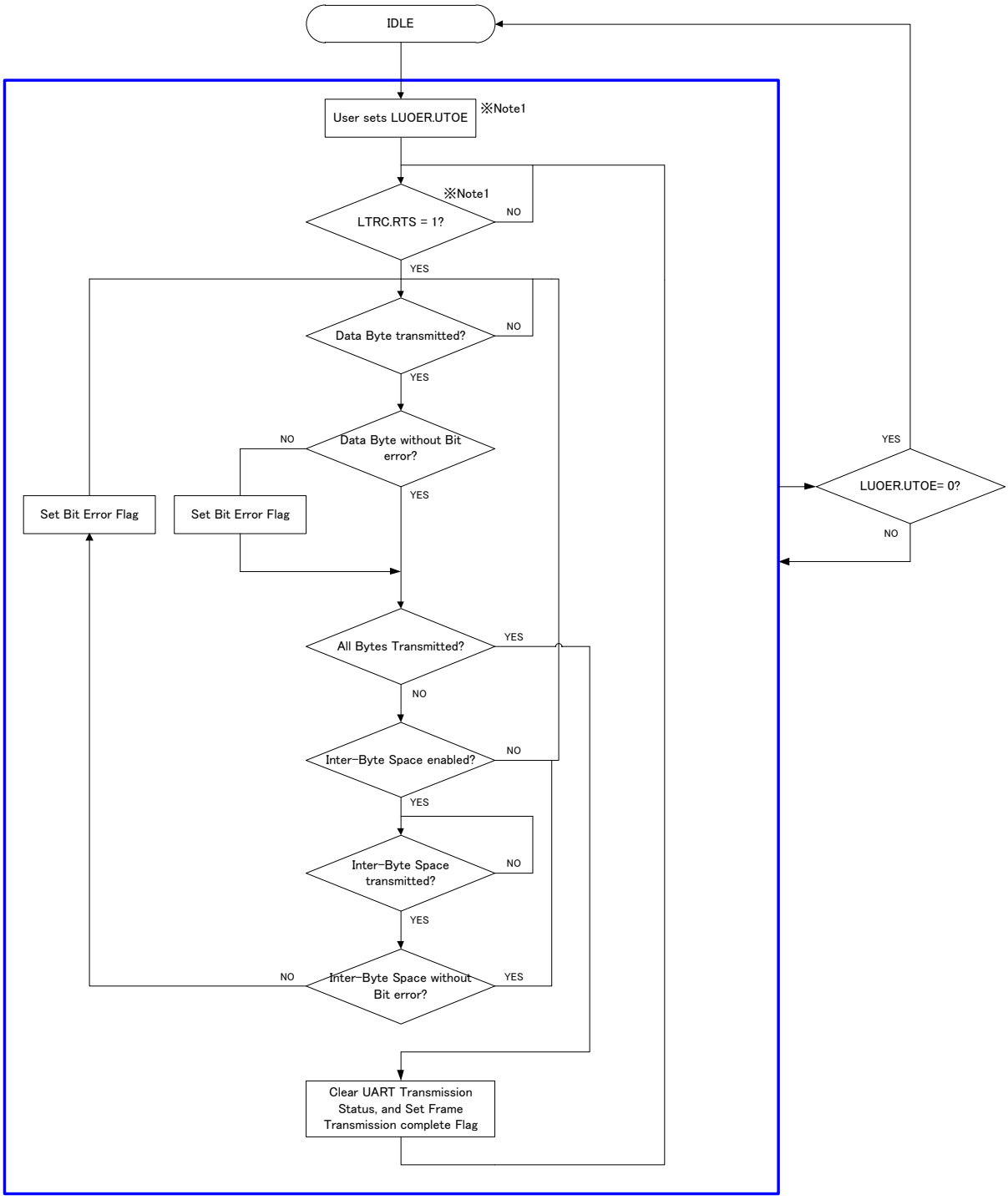


Figure 5-6: UART multi-byte Transmission Flow

Note1: UART Transmission Status is set in UART multi-byte Transmission when the both LUOER.UTOE and LTRC.RTS are set by Users.

In case of UART multi-byte transmission, users should set the UART Transmission Start Wait Bit before setting the LTRC[1] bit. The LIN Communication controller waits for completion of reception of 1 STOP bit and then starts transmission.

If STOP bit length is configured as 2 bits, then the transmission will start after receiving 1st STOP bit completely. The module will not wait for the 2nd STOP bit in this case.

Single-byte Transmission:

For single-byte UART transmission, transmission operation is started by writing data to the UART 7bit/8bit/9bit Transmit Data register or the UART 7bit/8bit/9bit Wait Transmit Data Register. Transmission Interrupt is generated based on the UART Transmission Interrupt generation Timing Select bit configuration.

For half-duplex communication, the data should not be written to these registers if reception is in progress (UART reception status bit is set to "1").

If a Bit Error (if detection is enabled) is detected during transmission, then bit error flag is set. It is set at the end of the data byte transmission.

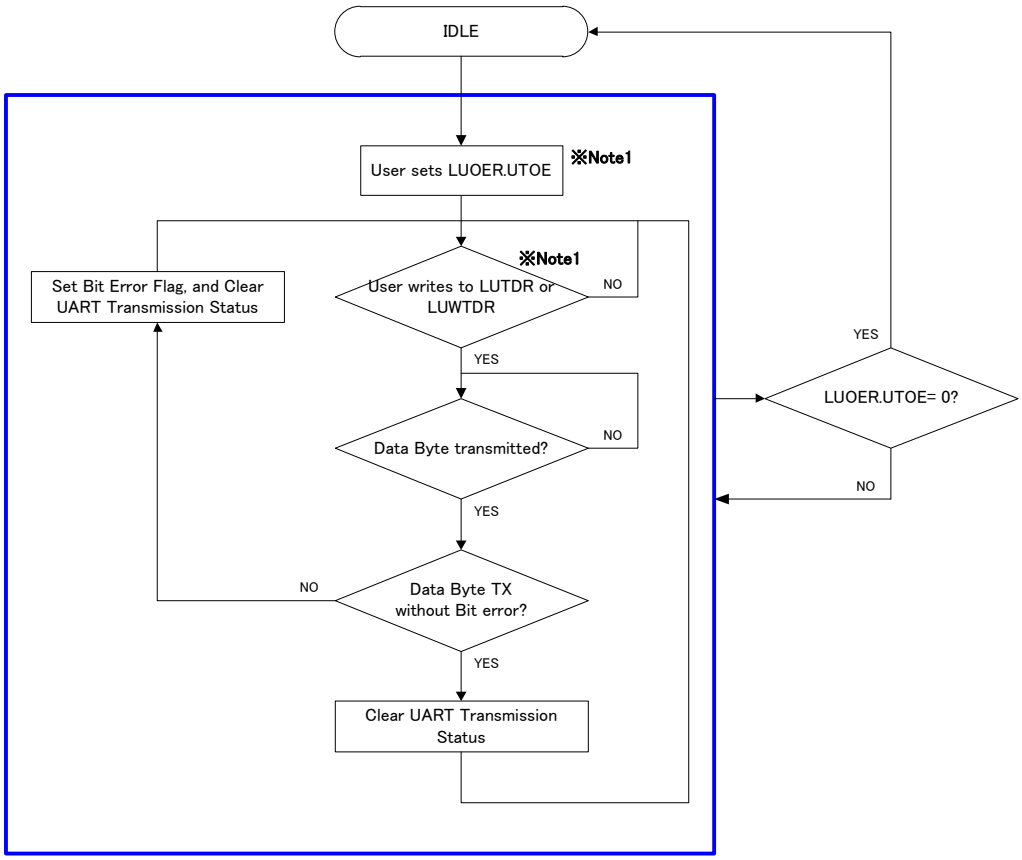


Figure 5-7: UART mode single-byte Transmission Flow

Note1: UART Transmission Status is set in UART single-byte Transmission when LUOER.UTOE is set and LUTDR or LUWTDR is written by Users.

5.2.4.2 UART transmission start delay

UART multi-byte Transmission:
When Frame Communication start is enabled (LTRC.RTS set to 1) during the reception of STOP bit and UART Transmission Start Wait Bit (LDFC.UTSW) is 0, then the transmission of data starts without waiting for the completion of STOP bit. In this case the STOP bit width is shortened due to transmission of START bit.

When Frame Communication start is enabled (LTRC.RTS set to 1) during the reception of STOP bit and UART Transmission Start Wait Bit (LDFC.UTSW) is 1, then the RLIN3 module waits until the complete STOP bit is received completely before starting the transmission.

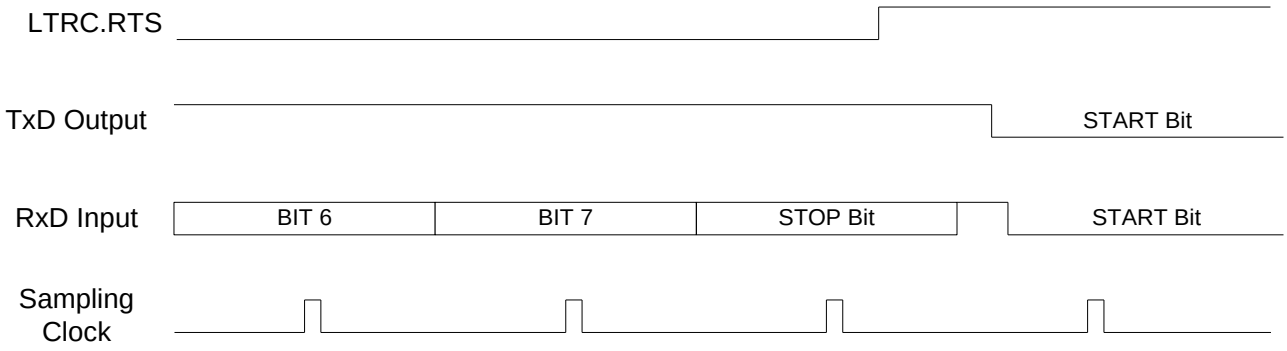


Figure 5-8: UART multi-byte Transmission Start delayed up to end of STOP bit

Single-byte Transmission:
When data is written in to the UART 7bit / 8bit / 9bit transmit Data register during reception of STOP bit, the transmission of data starts without waiting for the completion of STOP bit. In this case the STOP bit width is shortened due to transmission of START bit

When data is written in to the UART 7bit / 8bit / 9bit Wait transmit Data register during reception STOP bit, the transmission of data starts only after completion of the STOP bit.
In RLIN3 module, the transmission waits for completion of 1 STOP bit only. If STOP bit length is configured as 2 bits, then the transmission will start after receiving 1 STOP bit completely. The module will not wait for the 2nd STOP bit in this case.

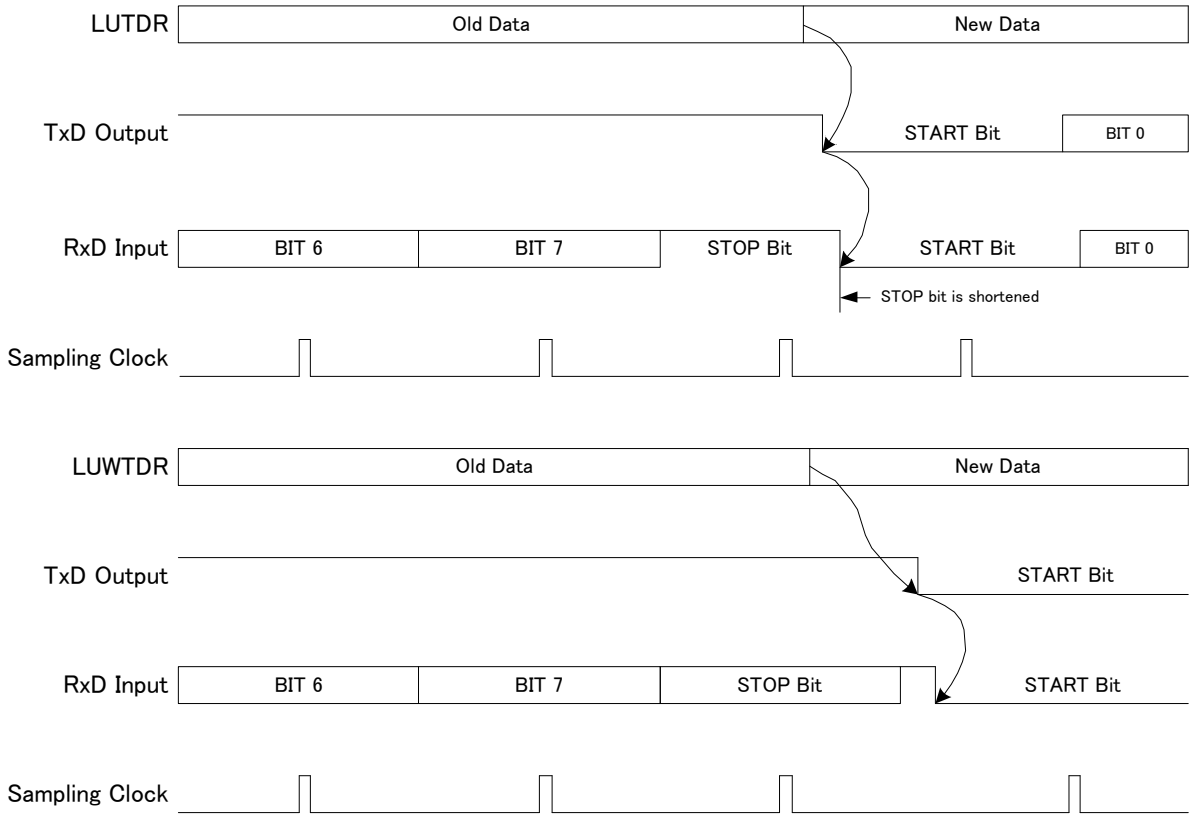


Figure 5-9: Single-byte Transmission Start delayed up to end of STOP bit

5.2.4.3 UART mode Reception

Reception is enabled by setting the UART Reception Enable bit.

In UART mode, received data is always stored in the UART 7bit/8bit/9bit Receive Data register.

In case a Parity Error or a Framing Error is detected, the relevant Error Status bit is set at the end of data reception.

Overrun error flag is set if data is received before the previous data is read by the Register.

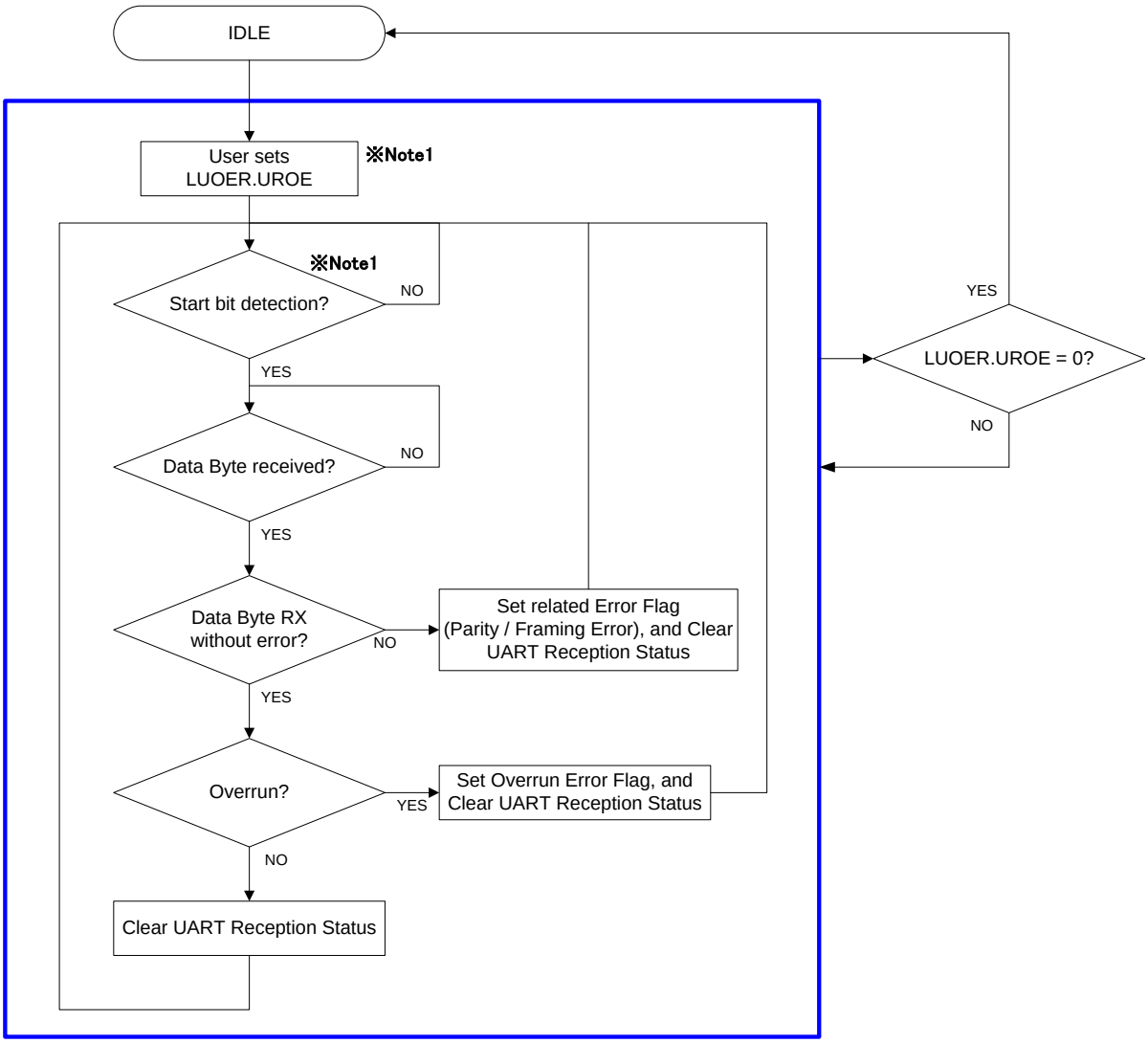


Figure 5-10: UART mode Reception Flow

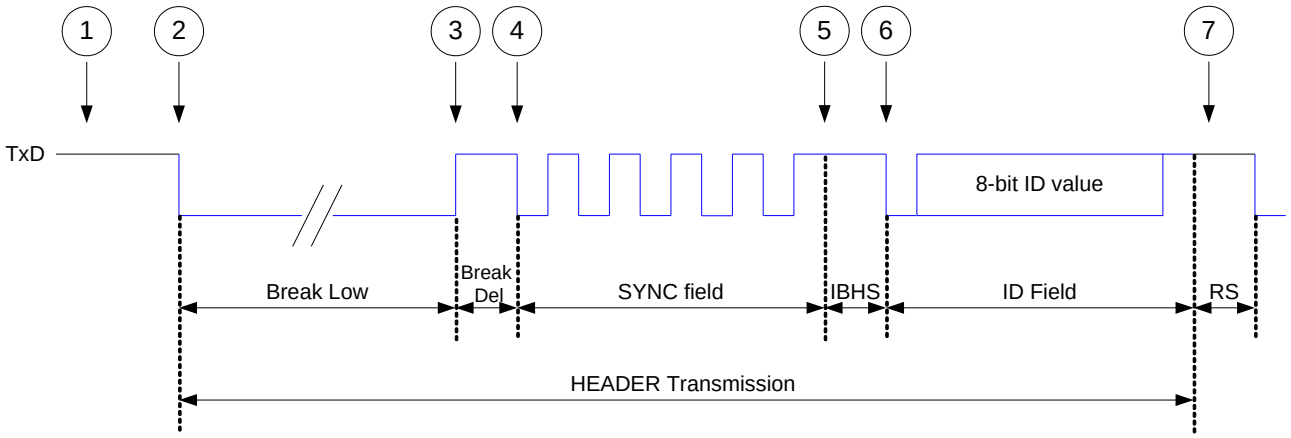
Note1: UART Reception Status is set in UART Reception when LUOER.UROE is set by Users and Start bit is detected.

6 OVERVIEW OF OPERATIONS

Note: In the sections below, the diagrams show the case for successful transmission or reception.

6.1 LIN MASTER MODE-HEADER TRANSMISSION

Flow of operation of the LIN controller on header transmission is illustrated below.



Break del = Break Delimiter IBHS = Inter-Byte Header Space RS = Response Space

Figure 6-1: Header transmission

6.1.1 LIN Controller operation

1. LIN Controller is waiting for completion of configuration and for setting of LIN Communication start bit to "1" by the SW drivers.
2. Break Low Transmission after the LIN Communication start bit is set.
3. Break Delimiter Transmission
4. SYNC field (55h) Transmission
5. Inter-Byte Header Space transmission
6. ID field transmission
7. Output LIN Header Transmission flag. LIN Header Transmission is completed and Response communication process can start.

6.2 LIN SLAVE MODE-HEADER DETECTION

Flow of operation of the LIN controller on header reception is illustrated below.

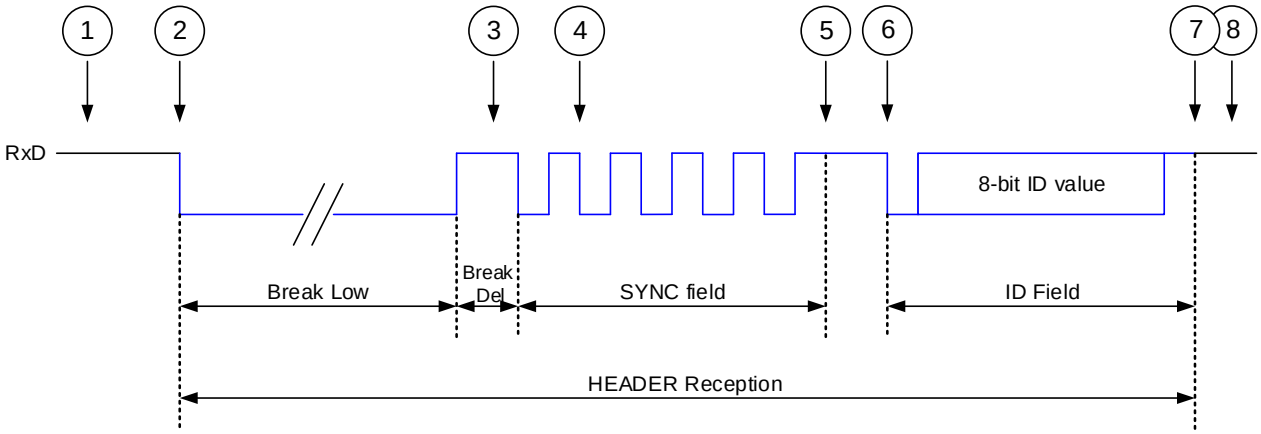


Figure 6-2: Header reception in LIN Slave mode

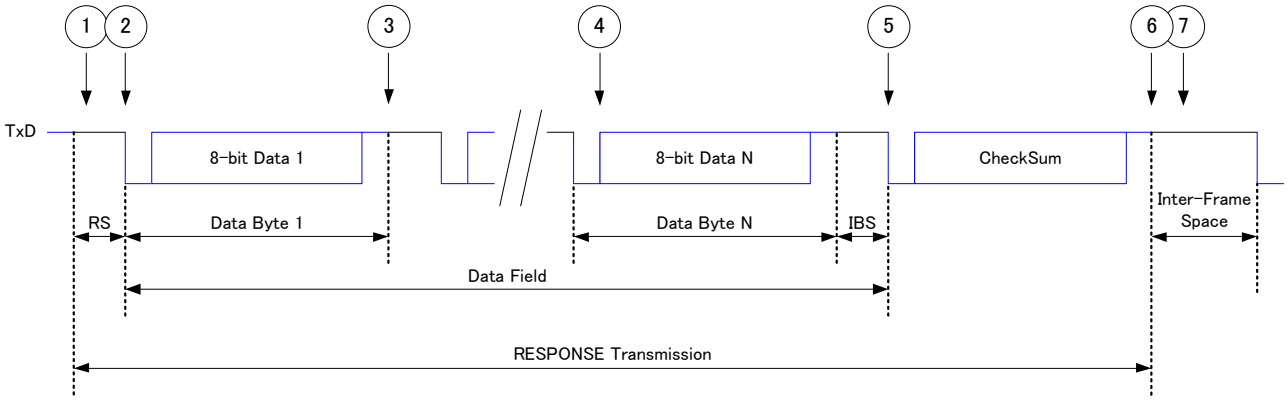
6.2.1 LIN Controller Operation

1. LIN Controller is waiting for completion of configuration and for setting of LIN Communication start bit to "1" by the SW drivers.
2. LIN Controller is waiting for detection of the Falling-edge on the RxD input pin (start of Break Low field).
3. Successfully detect Break Low & Break Delimiter and LIN Break Field Reception flag is set.(Fixed baud rate mode)
4. Successfully detect Break Low & Break Delimiter and LIN Break Field Reception flag is set. (Automatic Baud rate detection mode)
5. In the Sync field 2 options are available:
   - If Automatic Baud rate detection is enabled, then baud rate is detected in this field along with comparison of received byte value to "55h" for successful Sync filed detection.
   - If Fixed baud rate detection is selected, then the received byte value is compared to "55h" for detection of successful SYNC field

   The "Response Transmission or Reception start" bit and the "LIN No response request" bit are cleared by the LIN Controller at the end of successful detection of SYNC field.
   LIN Sync Field Reception flag is set when Sync field is successfully reception
6. After successful reception of SYNC field, the ID value is received. The ID Parity bits are checked for the received ID.
7. Output LIN Header Reception flag.
8. Header Reception process completed and SW drivers should read the received ID to check if Response preparation is required.

6.3 LIN MASTER MODE – RESPONSE TRANSMISSION

Operation of the LIN Controller on Response transmission is illustrated below.



RS = Response Space IBS = Inter-Byte Space

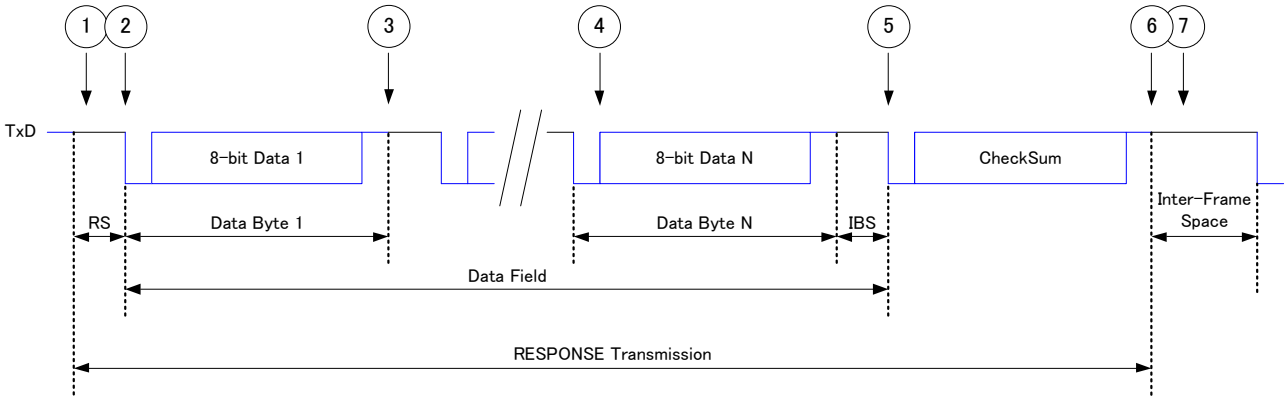
Figure 6-3: Response transmission

6.3.1 LIN Controller operation

1. 2 options are available
   - In Frame Separate mode, LIN Controller is waiting for transfer of data to data buffers and setting of Response Transmission or Reception start bit to "1" by the SW drivers. A "1" level is transmitted on the LIN bus.
   - In Frame Combined mode, Response Space is transmitted.
2. Transmit 1st Data byte.
3. Transmit Inter-byte Space (IBS)
4. Transmit the Data byte along with the IBS until configured number of data bytes is transmitted. Abort transmission if Bit error is detected.
   a. For more than or equal to 9 data bytes communication, the number of data bytes is controlled by the SW drivers using the LIN successive selection bit.
   b. If number of data bytes is more than or equal to 9, then the LIN Successive selection bit should be set to "1", for the 1st group of data bytes. After the 1st group of data bytes have been transmitted, users should check if the next group of data bytes is the last group and the LIN Successive selection bit should be cleared to "0", for the last group of data bytes
5. Checksum transmission
6. Output Frame Transmission complete flag. The LIN Communication start and Response Transmission or Reception start bits are cleared by HW.
7. LIN Response Transmission is completed and SW drivers should read the status and error status registers to check status of response transmission.

6.4 LIN SLAVE MODE – RESPONSE TRANSMISSION

Operation of the LIN Controller on Response transmission is illustrated below.



IBS = Inter-Byte Space

Figure 6-4: Response transmission

6.4.1 LIN Controller operation

1. LIN Controller is waiting for the SW to configure the response data and set Response Transmission or Reception start bit or the LIN No Response request bit to "1". When Response Transmission or Reception start bit is set and response Transmission is selected, LIN Controller transmits Response Space. (Refer to Section 6.6 for the case when No Response request bit is set to "1".)
2. Transmit 1st Data byte.
3. Transmit Inter-byte Space (IBS)
4. Transmit the Data byte along with the IBS until configured number of data bytes is transmitted. Abort transmission if Bit error is detected.
    a. For more than or equal to 9 data bytes communication, the number of data bytes is controlled by the SW drivers using the LIN successive selection bit.
    b. If number of data bytes is more than or equal to 9, then the LIN Successive selection bit should be set to "1", for the 1st group of data bytes. After the 1st group of data bytes have been transmitted, users should check if the next group of data bytes is the last group and the LIN Successive selection bit should be cleared to "0", for the last group of data bytes
5. Checksum transmission
6. Output Frame Transmission complete flag. The Response Transmission or Reception start bit is cleared by HW.
7. LIN Response Transmission is completed and SW drivers should read the status, error status and response space status registers to check status of response transmission.

6.5 LIN MODE (MASTER / SLAVE) – RESPONSE RECEPTION

Operation of the LIN controller on response reception is illustrated below.

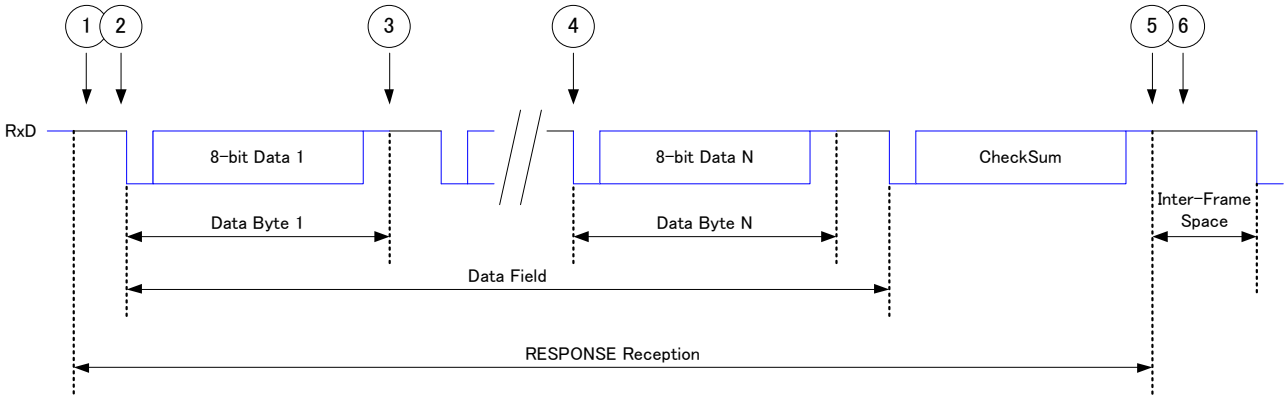


Figure 6-5: Response reception

6.5.1 LIN Controller operation

1. In case of LIN Master mode, LIN Controller is waiting for detection of START bit. In case of LIN Slave mode, LIN Controller is waiting for the SW to set Response Transmission or Reception start bit or the LIN No Response request bit to "1". When Response Transmission or Reception start bit is set and response Reception is selected, LIN Controller is waiting for detection of START bit. (Refer to Section 6.6 for the case when No Response request bit is set to "1".)
2. Falling-edge is detected on the RxD input pin.
3. Receive Data0 after detection of START bit. Set the LIN One Byte Reception flag to "1".
4. Continue reception of Data until the configured number of data bytes is received. Abort reception if an error is detected during Data reception.
    a. For more than or equal to 9 data bytes communication, the number of data bytes is controlled by the SW drivers using the LIN successive selection bit.
    b. If number of data bytes is more than or equal to 9, then the LIN Successive selection bit should be set to "1", for the 1st group of data bytes. After the 1st group of data bytes have been received, users should check if the next group of data bytes is the last group and the LIN Successive selection bit should be cleared to "0", for the last group of data bytes
5. Receive Checksum.
6. Check if received Checksum value matches the calculated value of Checksum and output the Frame Reception complete flag. LIN Response Reception is completed and SW drivers should read the status and error status registers to check status of response reception. The LIN Communication start bit is cleared by HW in LIN Master mode. However, the LIN Communication start bit is not cleared in LIN Slave mode. And Response Transmission or Reception start bit is cleared by HW.

6.6 LIN SLAVE MODE – NO RESPONSE

If a response does not exist for the received ID, then the SW drivers set the "LIN No Response Request" bit and hence no action is taken by the LIN controller until the next Header reception starts.

6.7 UART MODE –TRANSMISSION (SINGLE BUFFER)

Flow of operation of the UART controller for Frame transmission is illustrated below:

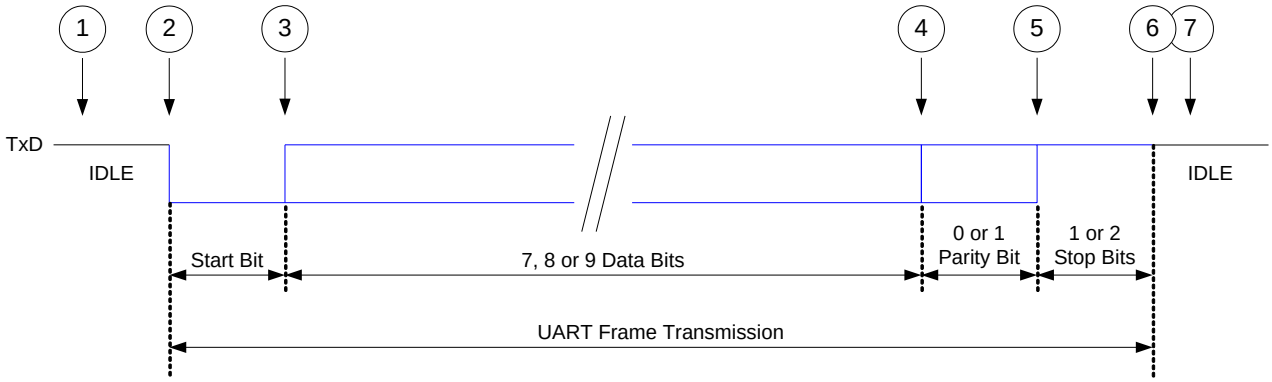


Figure 6-6: UART Frame transmission

1. LIN Controller is waiting for the configuration of registers and write access to UART 7bit/8bit/9bit transmit data register. UART Transmission Status is set when the data is written into the UART 7bit/8bit/9bit transmit data register.
2. Start bit is transmitted based on LUTDCR.UTSDV settings and Transmission Interrupt could be generated based on the TX Interrupt generation timing configuration.
3. Data is transmitted based on configuration.
4. If configured, a Parity bit is transmitted.
5. 1 or 2 STOP bits are transmitted.
6. Transmission Interrupt could be generated based on the TX Interrupt generation timing configuration. If SW drivers do not write the transmit data into the UART 7bit/8bit/9bit transmit data register, then the UART Transmission Status is cleared.
7. SW drivers should check status of frame transmission.

6.8 UART MODE –TRANSMISSION (SINGLE BUFFER BUT WAITING FOR STOP BIT)

Flow of operation of the UART controller for Frame transmission is illustrated below:

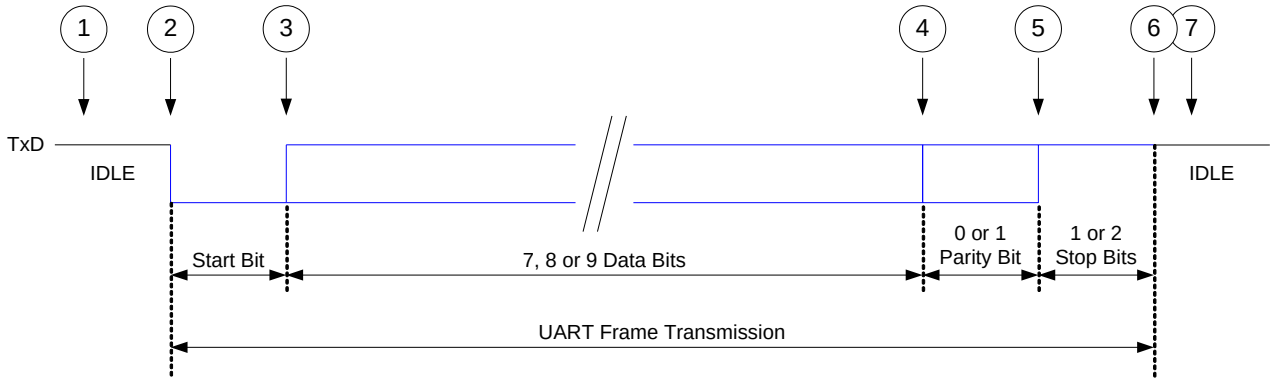


Figure 6-7: UART Frame transmission

1. LIN Controller is waiting for the configuration of registers and write access to UART 7bit/8bit/9bit Wait transmit data register. UART Transmission Status is set when the data is written into the UART 7bit/8bit/9bit Wait transmit data register.
2. LIN Controller waits for the end of the 1st STOP bit if Start bit is transmitted after detection of 1st Stop bit. Transmission Interrupt could be generated based on the TX Interrupt generation timing configuration.
3. 7, 8 or 9-bit Data is transmitted based on configuration.
4. If configured, a Parity bit is transmitted.
5. 1 or 2 STOP bits are transmitted.
6. Transmission Interrupt could be generated based on the TX Interrupt generation timing configuration. If SW drivers do not write the transmit data into the UART 7bit/8bit/9bit transmit data register, then the UART Transmission Status is cleared.
7. SW drivers should check status of frame transmission.

6.9 UART MODE –TRANSMISSION (UART MULTI-BYTE TRANSMISSION)

Flow of operation of the UART controller for Frame transmission is illustrated below:

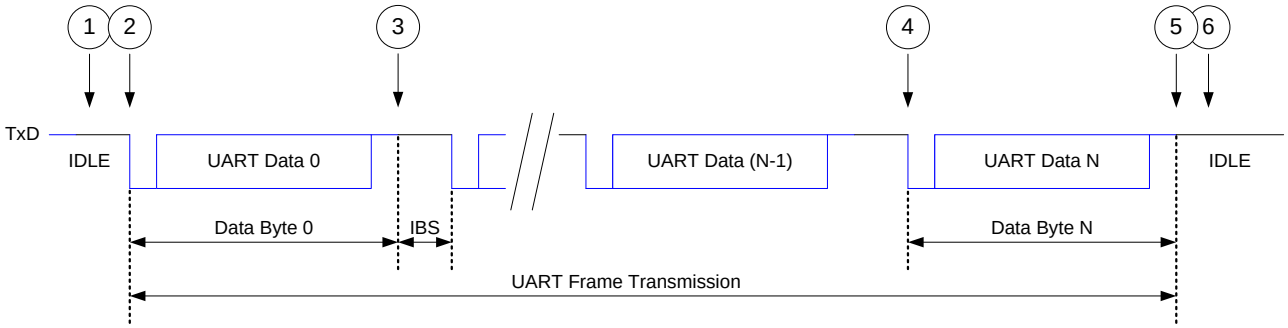


Figure 6-8: UART Multi-Byte transmission

1. LIN Controller is waiting for the SW drivers to
   a. configure registers
   b. write data to UART Data Buffer N registers
   c. set the UART multi-byte transmission start bit

   UART Transmission Status is set when the UART multi-byte transmission start bit is set.
2. Start bit is transmitted based on LDFC.UTSW setting. Transmit 1st Data with the configured values for Bit length, Parity bit and number of stop bits. Transmission Interrupt could be generated based on the TX Interrupt generation timing configuration, when user sets 4'b0001 to LDFC.MDL[3:0].
3. Transmit Inter-byte Space, when user sets 4'b0000 or between 4'b0010 to 4'b1001 to LDFC.MDL[3:0]. Transmission Interrupt could be generated based on the TX Interrupt generation timing configuration, when user sets 4'b0001 to LDFC.MDL[3:0].
4. Transmit the Data along with the IBS until configured number of data fields is transmitted. Transmission Interrupt could be generated based on the TX Interrupt generation timing configuration, when user sets 4'b0000 or between 4'b0010 to 4'b1001 to LDFC.MDL[3:0].
5. The UART multi-byte transmission start bit is cleared by HW. UART Transmission Status is cleared. Transmission Interrupt could be generated based on the TX Interrupt generation timing configuration, when user sets 4'b0000 or between 4'b0010 to 4'b1001 to LDFC.MDL[3:0].
6. SW drivers should check status of frame transmission.

6.10 UART MODE –RECEPTION (SINGLE BUFFER)

Flow of operation of the UART controller for Frame reception is illustrated below:

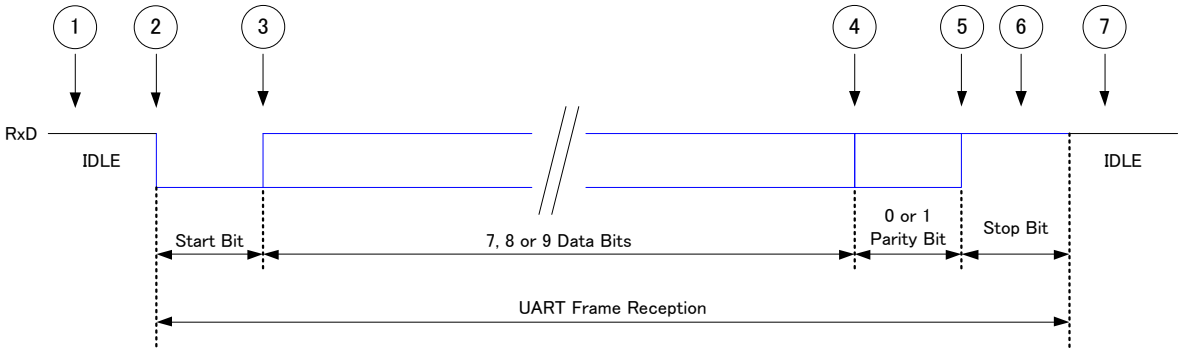


Figure 6-9: UART Frame reception

1. LIN controller is waiting for the SW drivers to enable UART reception
2. Wait for falling-edge on the RxD input pin and then check for valid START bit. UART Reception Status is set when START bit is sampled.
3. Data Byte Reception starts.
4. Parity Bit reception starts (if selected)
5. STOP Bit reception starts (1 Bit only). UART Reception Status is cleared when STOP bit is sampled.
6. Generate successful reception interrupt.
7. SW drivers should check status of frame reception

Designers Information:

The figure below shows a capture operation of the received data when there is the conflict occurrence of SW reset and reception complete timing.

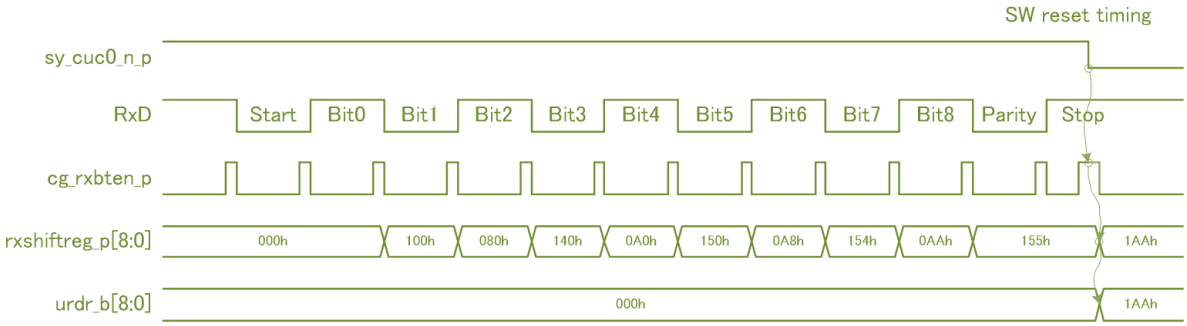


Figure 6-10: Conflict of SW reset and reception complete timing

If SW reset occurrence conflict with reception complete, the receive shift register is shifted once more because of bit enable issued by SW reset, therefore, receive data has been stored into the UART receive data register.

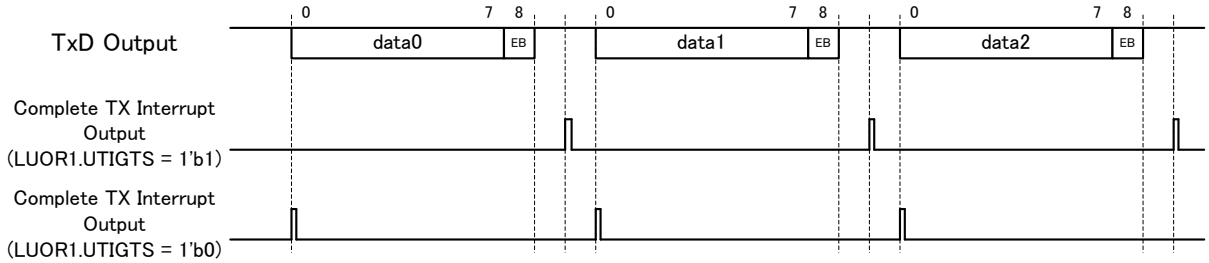
At this time, reception complete interrupt is issued.
In addition, the internal state is cleaned up by SW reset, overrun error condition does not occur in the next frame.

6.11 UART MODE –EXPANSION BIT

In UART mode, data of 9-bit lengths can be transmitted or received by setting the expansion bit enable bit. In Expansion bit mode, users should not set Overrun Error Detection bit when Expansion Bit Data comparison is enabled.

6.11.1 Expansion bit mode transmission

In Expansion bit mode, transmission is started by writing to the UART 7bit/8bit/9bit Transmit Data Register or UART 7bit/8bit/9bit Wait Transmit Data Register.



EB: *Expansion* Bit

Figure 6-11: Expansion bit mode transmission (LSB First)

6.11.2 Expansion bit mode reception without Expansion bit comparison

In Expansion bit mode, 9 bits reception is always possible without the comparison of Expansion bit when Expansion bit comparison is disable. Reception completion interrupt occurs regardless of the configuration of the LUOR1. UEBDL bit when 9 bits data is received without Expansion bit match, ID data match and error detection.

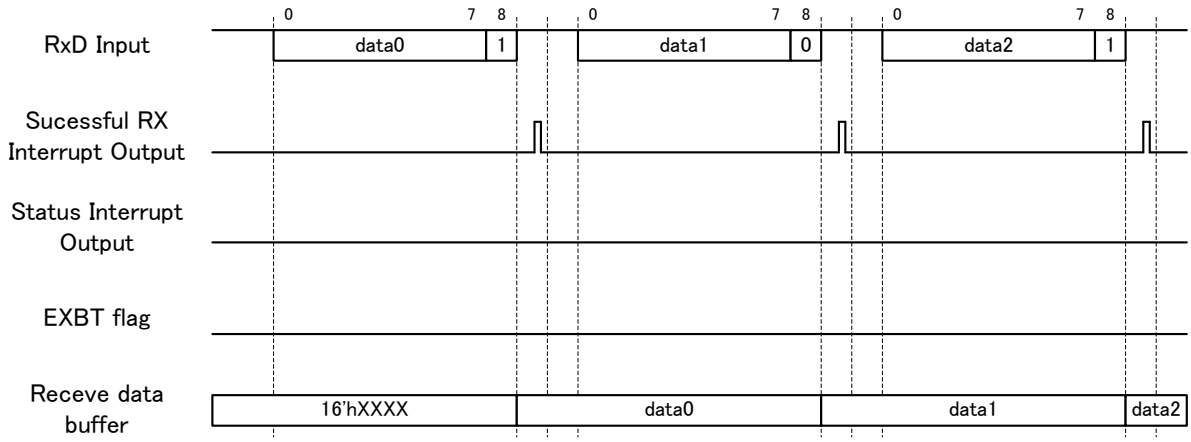


Figure 6-12: Expansion bit mode reception without Expansion bit comparison (LSB First, UECD= "0")

6.11.3 Expansion bit mode reception without data comparison

When expansion bit comparison is enabled and expansion bit data comparison is disabled in expansion bit mode, reception in 9-bit lengths can always be performed without data comparison.
When a level set by using the expansion bit detection level select bit is detected, a status interrupt request signal is generated upon completion of data reception, and an expansion bit detection flag is set.
When an inverted value of the expansion bit detection level is detected, a reception complete interrupt request signal is generated.
In either case, the receive data is stored into the UART 7bit / 8bit / 9bit Receive Data register if no overrun error has occurred.

RLIN3 Module does not judge the expansion bit comparison, if the reception error (parity error, framing error) occurs.
RLIN3 Module judge the expansion bit comparison, if the reception error (overrun error) occurs.

An example with expansion bit detection level select bit (UEBDL) configured to "0" is shown below.

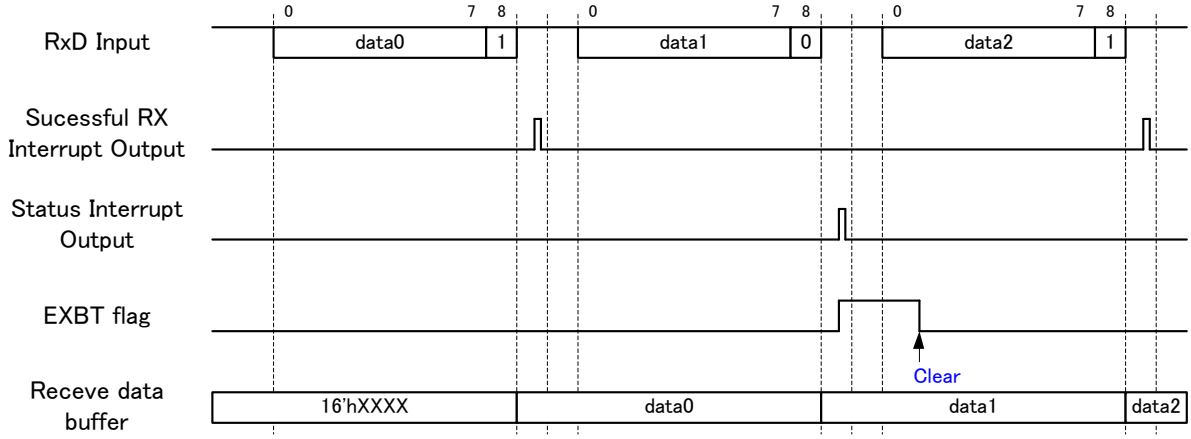


Figure 6-13: Expansion bit mode reception without data comparison (LSB First, UEBDL= "0")

When the comparison result of expansion bit is match and the reception error (parity error, framing error) occurs, RLIN3 updates only the reception error flag.
When the comparison result of expansion bit is match and the reception error (overrun error) occurs, RLIN3 updates EXBT flag and the reception error flag.

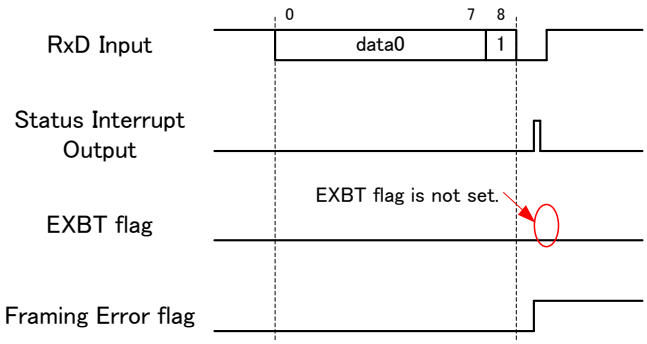


Figure 6-14: EXBT flag and reception error flag

6.11.4 Expansion bit mode reception with data comparison enabled

When expansion bit comparison is enabled and expansion bit data comparison is enabled in expansion bit mode, if a level set by using the expansion bit detection level select bit is detected, 8 bits excluding the receive data expansion bit are compared with the value of the ID register set in advance.
If the comparison results have matched the following actions are taken by the module:

- status interrupt request signal is generated,
- ID match flag is set
- expansion bit detection flag is set
- the receive data is stored into the UART 7bit / 8bit / 9bit Receive Data Register.

In the case of expansion bit mismatch without data comparison or expansion bit match and data mismatch, no interrupt is generated, no flag is updated, and the receive data is not stored.
End the processing before completion of the next data reception, because data will be omitted if the UEBDCE bit is changed after the next data reception has been completed.

RLIN3 Module does not judge the expansion bit comparison and expansion bit data comparison, if the reception error (parity error, framing error) occurs.
RLIN3 Module judge the expansion bit comparison and expansion bit data comparison, if the reception error (overrun error) occurs.

An example with expansion bit detection level select bit (UEBDL) configured to "0" is shown below.

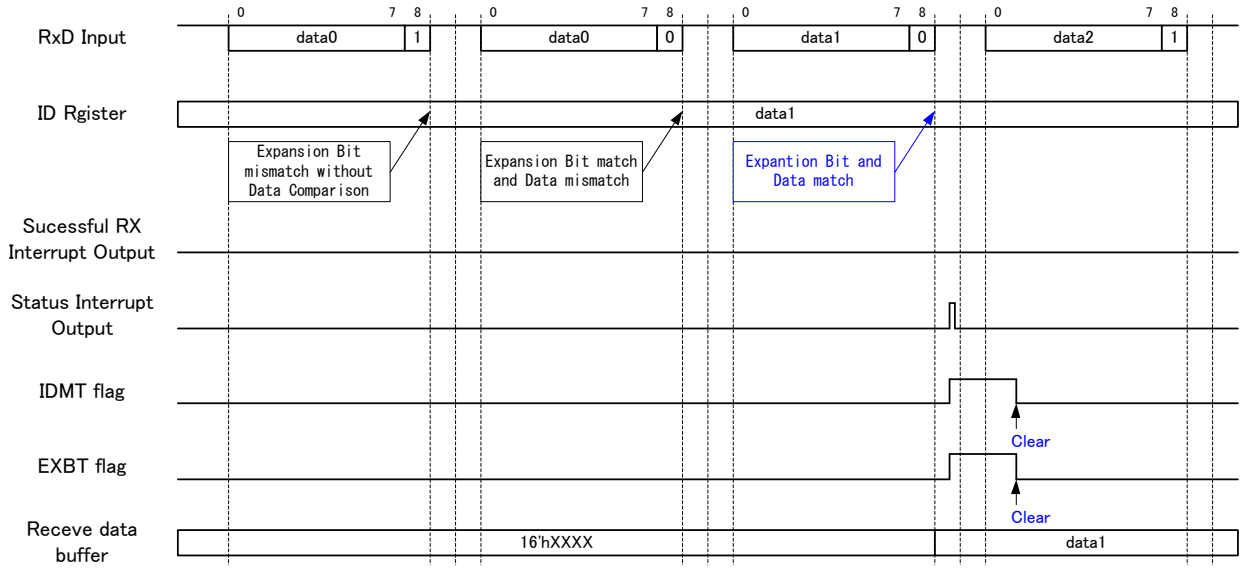


Figure 6-15: Expansion bit mode reception with data comparison (LSB First, UEBDL = "0")

6.12 UART MODE – EXTENDED UART MODE (NOT OPEN TO CUSTOMERS)

In RLIN3 the UART mode has been extended to meet some specific requirements. The UART mode has been extended to support following functions:

- Loop-back delay function for data consistency check
- Transmit Start Delay function
- Baud rate clock output function

The extended UART functions can be enabled by setting the Extended UART mode select bit in the LMD register.

Note 1: The UART multi-byte communication is not supported in Extended UART mode.
Note 2: Users should not set the bit error detection enable bit (LEDE.BERE='0').
Note 3: Users should use SW reset if users abort the communication in Extended UART mode.
Note 4: Users should not use LUWTDR register in Extended UART mode.
Note 5: Users should not set the UART multi-byte transmission start bit (LTRC.RTS='0').
Note 6: Users should not clear the UART Expansion Bit Comparison Disable Bit (LUOR1.UECD='1').
Note 7: Users should not set the UART Expansion Bit Data Comparison Enable Bit (LUOR1.UEBDCE ='0').

6.12.1 Loop-back delay function for data consistency check

The UART Frame Start Timing of Loop-back delayed Data Consistency Select Bits can be used to configure the timing of the window for comparison of the transmitted value with the received value. The timing of the window is a function of the UART baud rate clock.
If the received data bit value matches the transmitted data bit value during from a transmit start to a transmit end + LUOR2.UFST + 1 Tbits period, then the Loop-back delayed data consistency check interrupt is generated along with the reception completion interrupt.
If the received data bit value does not match the transmitted data bit value during the window, then, the UART Loop-back Delayed Data consistency Error flag is set and the Loop-back delayed data consistency check interrupt is generated along with the reception completion interrupt.

6.12.2 Transmit Start Delay function

The UART Transmit Start Delay Value select bits can be used to configure the delay value for the start of transmission after transmission is enabled and the data is written into the related Transmit Data register. UART transmitting start delay is controlled synchronizing with the bit timing of transmission.
If transmission is enabled and data is written into the related Transmit data register while reception is in progress (LST.URS is "1"), then the transmission delay count always starts after the completion of reception. Similarly, if reception starts in the middle of the delay count, then the delay count reloads count value, and then it stops count down until the reception is completed.
The UART Transmit Start Delay Value is loaded to UART Transmit Start Delay counter with the following timing.

(1). The SW Reset is active (LCUC.OM0 is "0")
(2). The transmission is in progress (during the TxD output)
(3). The reception is in progress (LST.URS is "1")
(4). The timing of Write to transmission data (LUTDR.UTD)

6.12.3 Baud rate clock output function

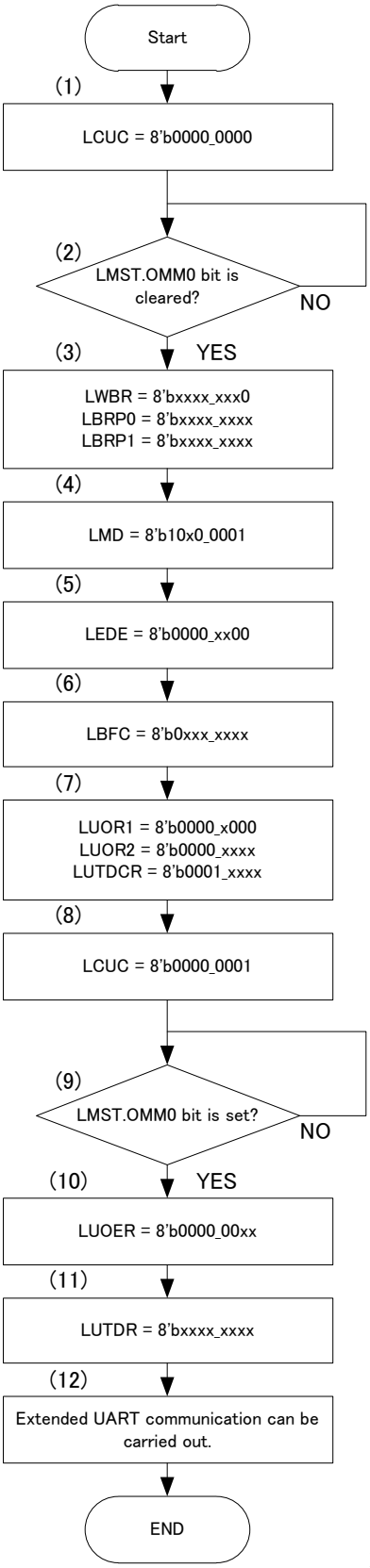
The UART Baud Rate clock output enable bit is used to control the Baud rate clock output. The UART Data Phase select bit is used to select the clock-edge for synchronising the TxD output with the Baud rate clock. This function operates only in Extended UART mode.

6.12.4 Configuration for Entry in Extended UART mode

Following steps are to be performed to execute this mode.

1. Enter reset state.
2. Is module in reset state?
3. Set prescaler, baud rate and number of samples per bit.
4. Set Extended UART mode and noise filter select bit.
5. Set error detection enable bits.
6. Set UART configuration register1.
7. Set UART option register1, UART option register2 and UART transmit start delay control register.
8. Enter idle state.
9. Is module in idle state?
10. Set UART operation enable register. Both LUOER.UTOE and LUOER.UROE should be set "1" when users apply the loop back delayed data consistency check.
11. Set UART 7bit/8bit/9bit transmit data register and UART 7bit/8bit/9bit wait transmit data register. Note1
12. Start Extended UART communication. Note1

Note1: The reception operation of Extended UART mode is the same as the reception operation of Normal UART mode.
Note2: The movement is also no problem by reverse order for "3", "4", "5", "6" and "7".
Note3: Users shall write to the UART transmitting start delay value (LUTDCR.UTSDV) from the start of transmission to the write of the next transmission data(LUTDR.UTD).
Note4: Refer to 7.9.2 for conflicts of the loop back delayed data consistency check and RX error status.



x: any value

Figure 6-16: Configuration of Flow diagram for Extended UART mode Entry

6.12.5 Operation in Extended UART mode

Following steps are the operation in this mode.

1. The configured LUTDCR.UTSDV value is loaded to Tx start delay counter.
2. The counting down of Tx start delay counter is started.
3. Is the value of Tx start delay counter "0"?
4. The configured LUTDCR.UTSDV value is loaded to Tx start delay counter again. And data byte is transmitted.
5. Is LST.UTS cleared by HW?
6. Is Tx interrupt set? (In case of LUOR1.UTIGTS is set to "1". Tx interrupt is set at the start timing of data byte transmission, if LUOR1.UTIGTS is set to "0".)
7. Is the start bit of Rx detected?
8. Data byte is received.
9. Is LST.URS cleared by HW?
10. Are Rx interrupt and Loop-back delayed data consistency check interrupt set by HW?

Note 1: 1-6: UART Transmission steps, 7-10: UART Reception steps
Note 2: Users are able to execute Loop-back delayed Data Consistency check, if LUOER.UROE is set to "1".
Note 3 : If a parity error and a flaming error occur, the completion interrupt request of reception and data consistency check interruption is not generated. A status interrupt is generated.

The definition for loop-back delay window is the following.

1. If detected sample point of start bit in loop-back delay window, execute Loop-back delayed Data Consistency check.
2. If detected sample point of start bit during 0.5Tbits from the start of loop-back delay window, execute Loop-back delayed Data Consistency check, but it does not guarantee the result of the operation.
   (Only for RxD which is delayed TxD will loop back, the result of the operation is guaranteed.)
3. If the loop-back data and data from other devices conflict occurs, received data after Loop-back delayed Data Consistency check is not reliable.

The following figure is shown the operation of Loop-back delay window.

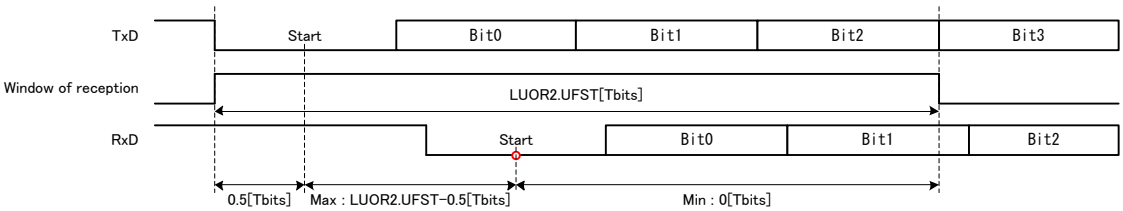


Figure 6-17: Definition for loop-back delay window

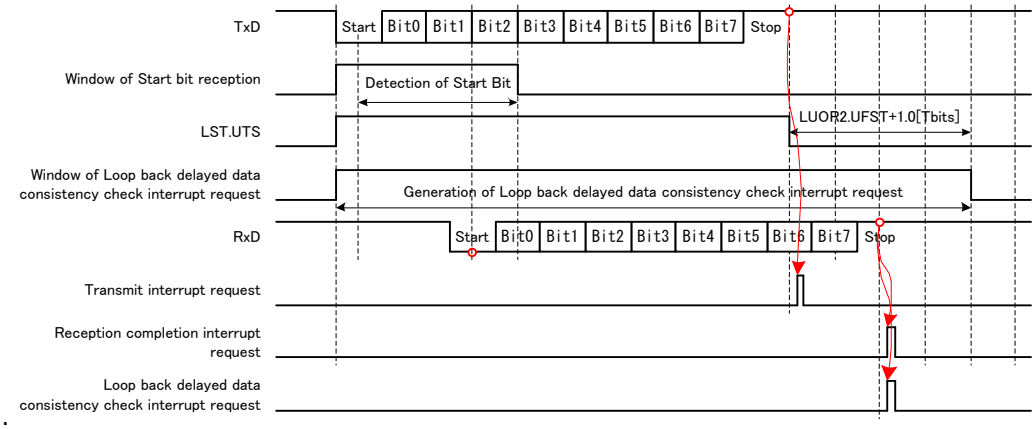


Figure 6-18: In the case of detected sample point of start bit in loop-back delay window

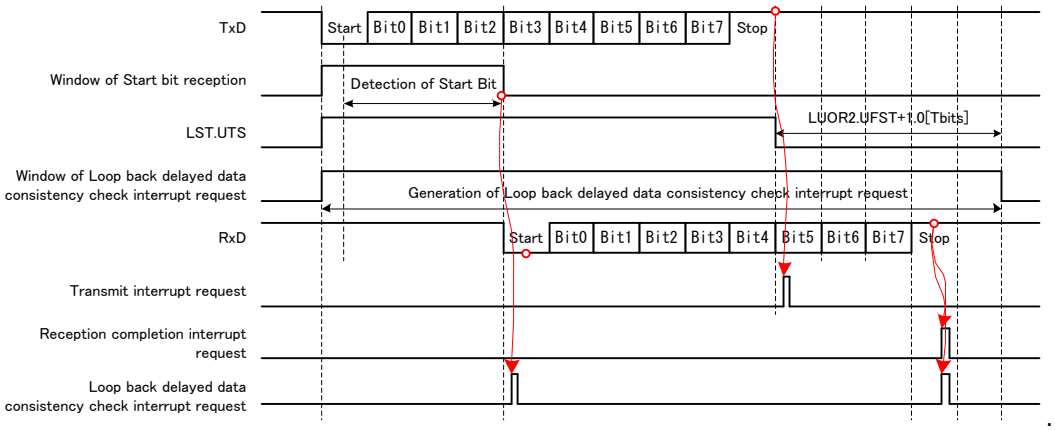


Figure 6-19: In the case of not detected sample point of start bit in loop-back delay window and detected sample point of stop bit in loop-back delayed data consistency check window

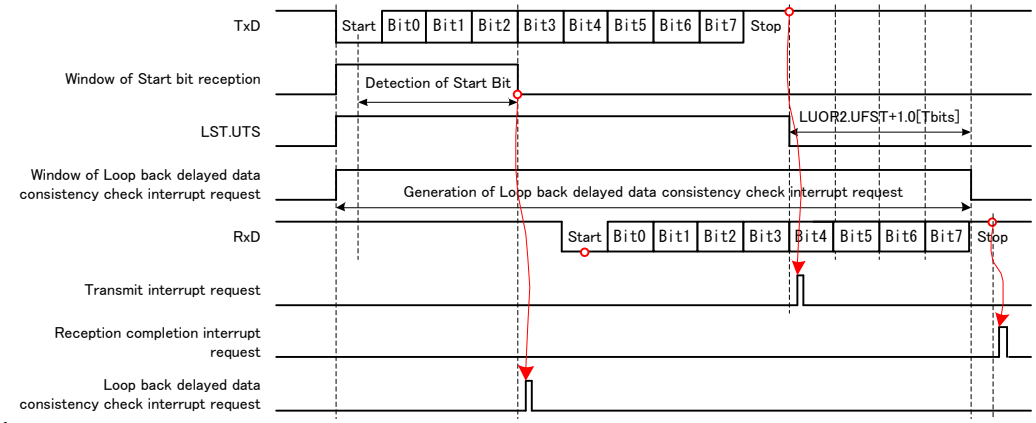


Figure 6-20: In the case of not detected sample point of start bit in loop-back delay window and not detected sample point of stop bit in loop-back delayed data consistency check window

The following is the flow chart at the time of normal operation.

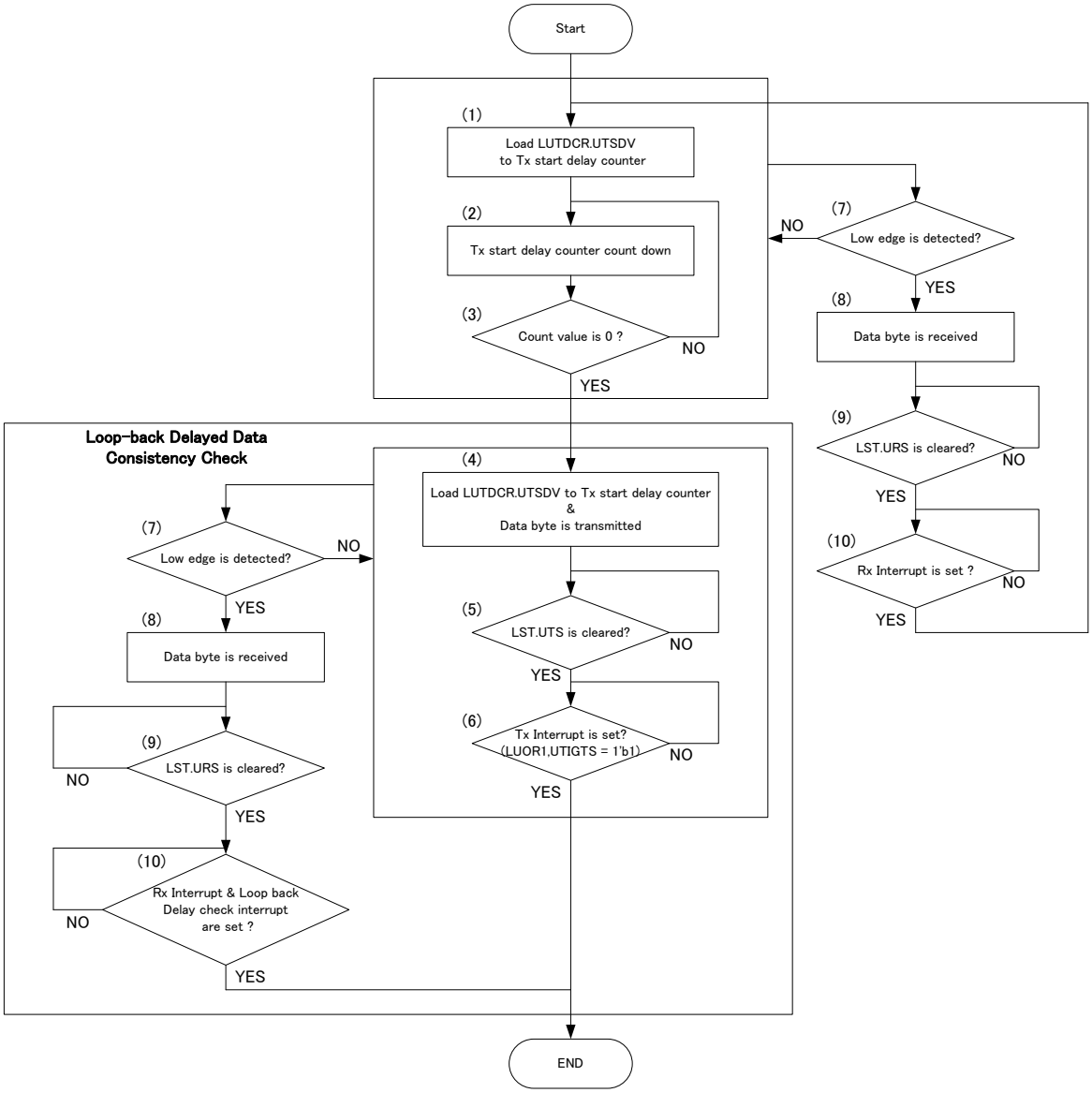


Figure 6-21: Operation of Flow diagram for Extended UART mode

The basic Operation of the Extended UART is illustrated below.
The frame window set by LUOR2.UFST is the width of 4 Tbit in this case. The loop back data is received in it. The transmit interrupt request is generated. Both the reception completion interrupt request and the loop back delayed data consistency check interrupt request are generated after receiving RxD.

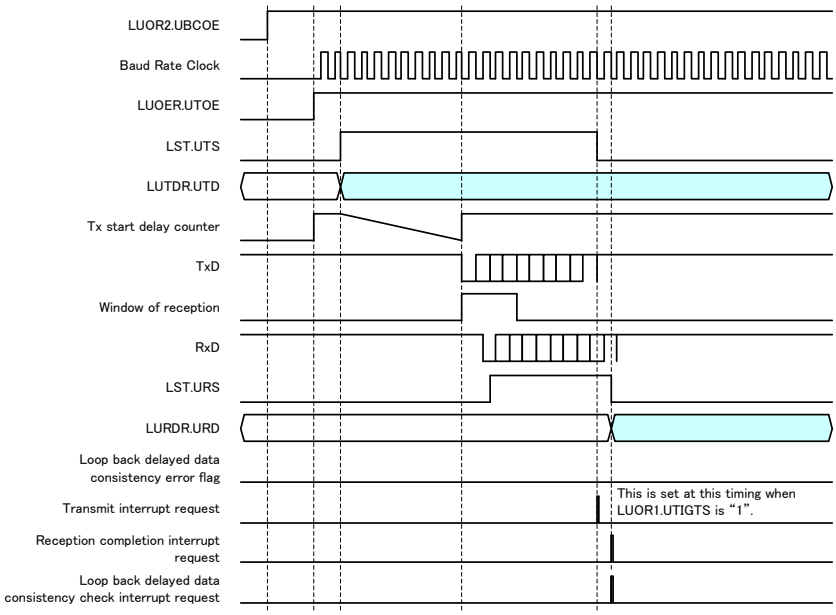


Figure 6-22: No Reception after transmission delay count –No loop back delayed data consistency check error detected

The following timing chart shows that there is not the loop back data in the window of reception.
Both the loop back delayed data consistency error flag and the loop back delayed data consistency check interrupt request are generated after the window of reception.

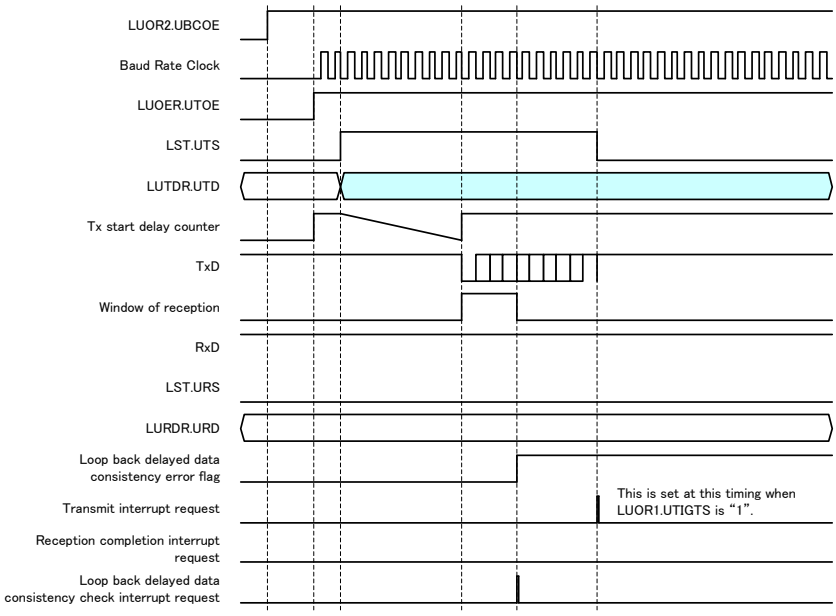


Figure 6-23: No Reception after transmission delay count -loop back delayed data consistency check error detected

The following timing chart shows that RxD is received during counting the Tx delay counter.
The transmit delay counter is reloaded simultaneously with the reception of RxD and keeps the value during the reception.
If StartBit detection of RxD and count value = "0" conflicts, then Transmission is high priority.

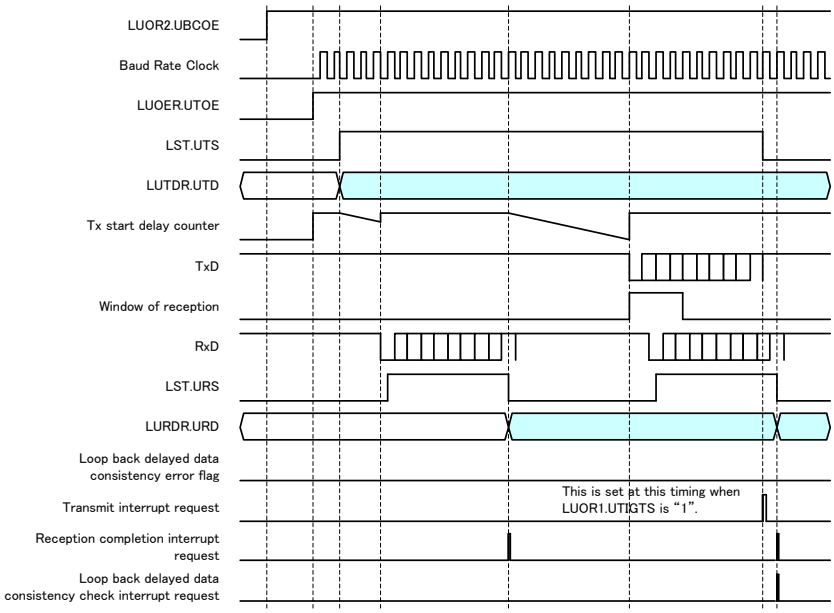


Figure 6-24: Reception during transmission delay count -No loop back delayed data consistency check error detected

The following timing chart shows that there is the transmission request during reception.
The transmit delay counter keeps the value during the reception.

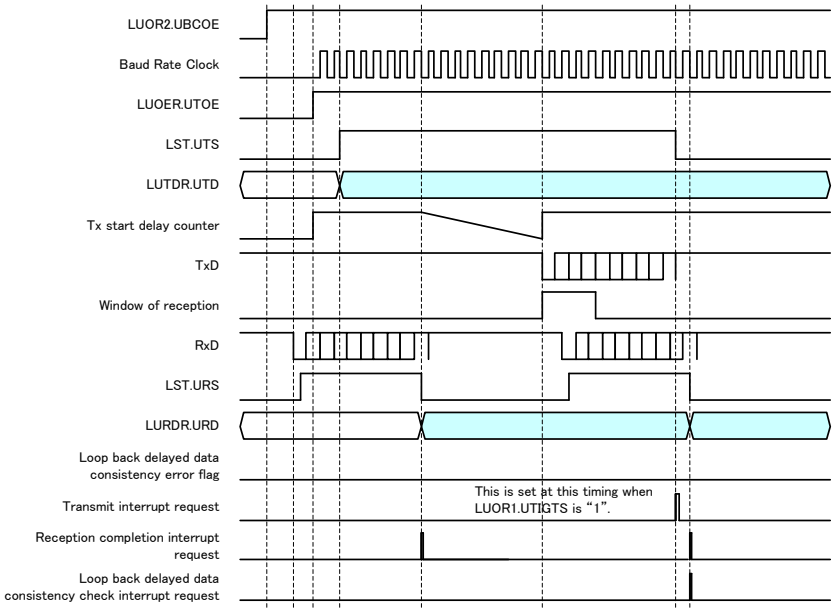


Figure 6-25: Reception before transmission delay count -No loop back delayed data consistency check error detected

The following timing chart shows that TxD and RxD are mismatch.
Both the loop back delayed data consistency error flag and the loop back delayed data consistency check interrupt request are generated after the reception

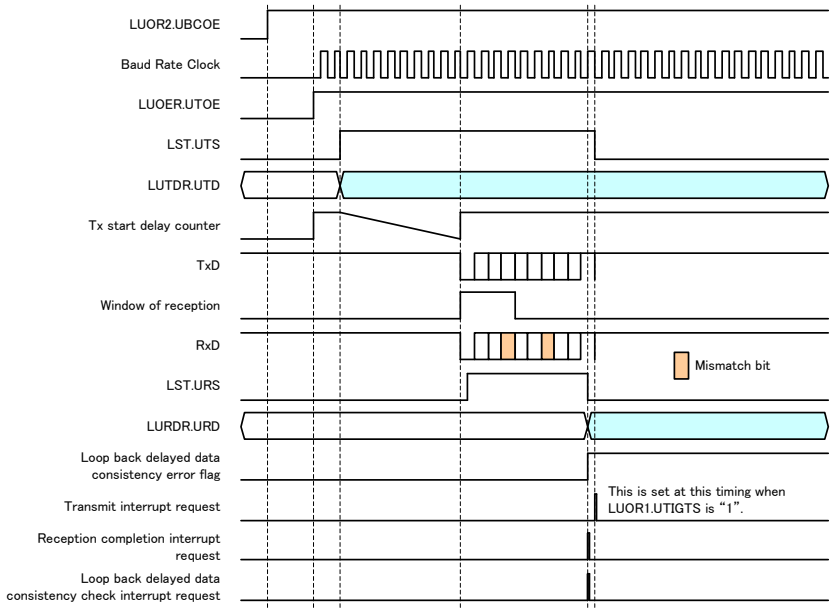


Figure 6-26: Reception after transmission delay count -loop back delayed data consistency check error detected

The following timing chart shows that TxD and the delayed RxD are mismatch.
Both the loop back delayed data consistency error flag and the loop back delayed data consistency check interrupt request are generated after the reception

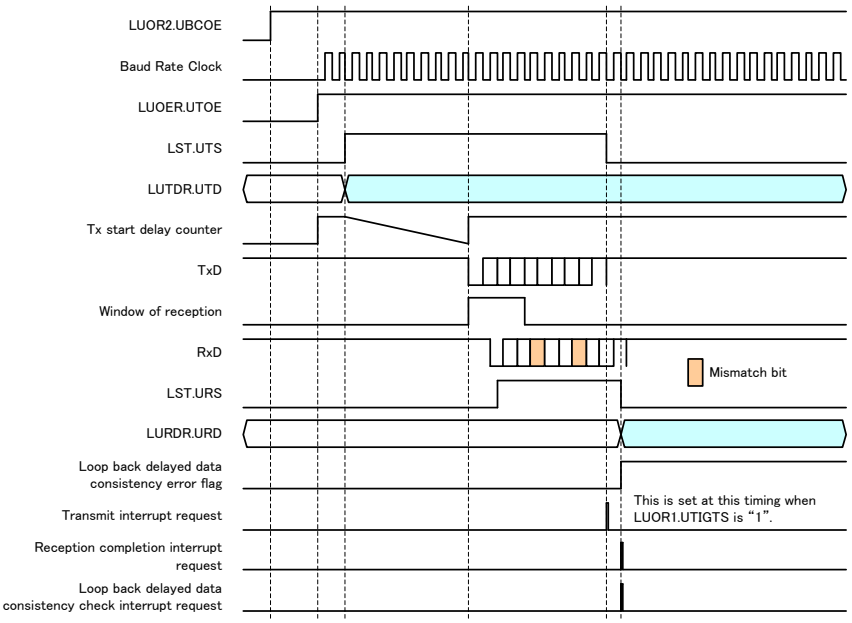


Figure 6-27: No Reception during transmission delay count -loop back delayed data consistency check error detected

The following timing chart shows that SW reset becomes active during keeping the Tx delay counter by the transmission abort function. The Tx delay counter is reloaded simultaneously with the SW reset.

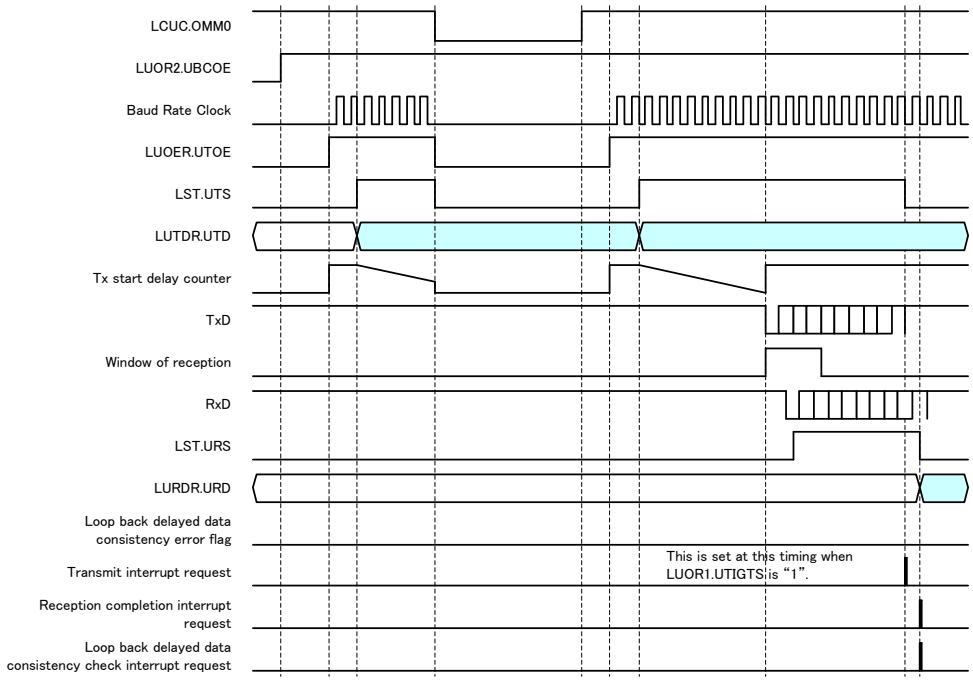


Figure 6-28: SW reset after transmission abort function during transmission delay count

The following timing chart shows that the consecutive transmission in Extended UART mode. The re-configuration of LUTDCR.UTSDV is possible until the UART transmission data of the 2nd frame is written into LUTDR after the UART Transmission Interrupt of the 1st frame is set.

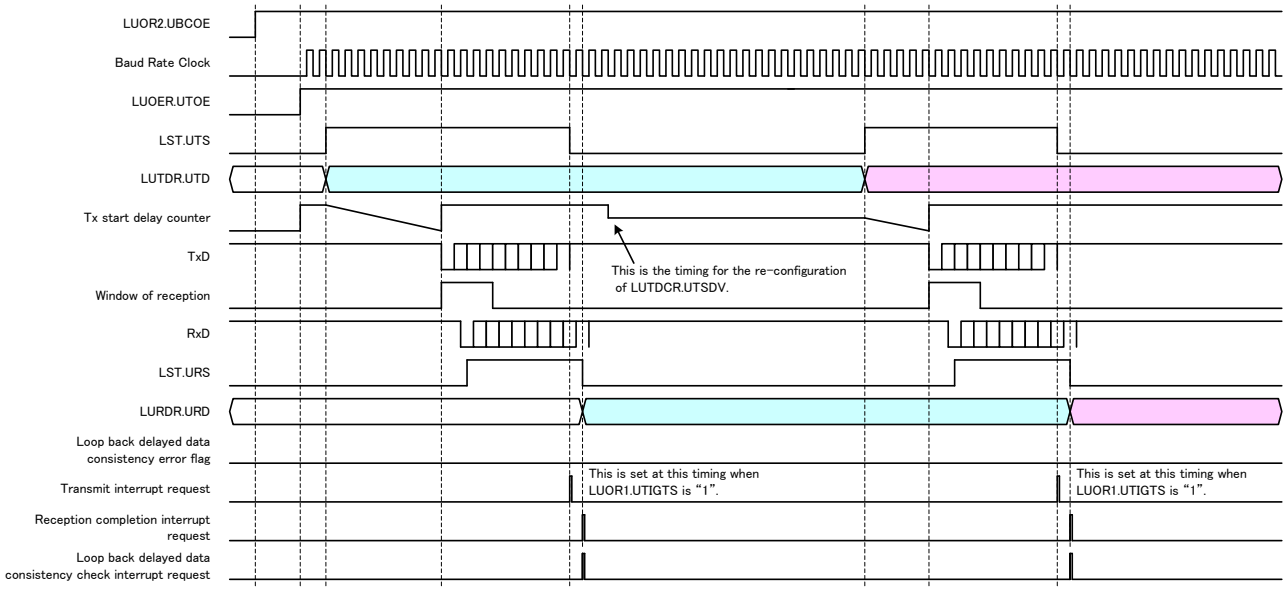


Figure 6-29: Consecutive transmission in the Extended UART mode

7 DETAILS OF THE OPERATION

7.1 CLOCK SOURCE DESCRIPTION

The RLIN3 module, requires 3 clock sources:

- PCLK (peripheral clock that is always active)
- PCLKRW (Bus clock that is active only during Register access to RLIN3 registers)
- PCLK_LIN (LIN communication clock for the LIN Protocol engine functions)

The clock signals "clk_p" (PCLK) and "clk_p_rw" (PCLKRW) are in phase with the Register access clock.

A separate LIN communication clock "clk_lin" (PCLK_LIN) is necessary because LIN operation requires a stable clock with low variations in clock frequency to meet the tolerance defined in the LIN protocol specification. Use of a separate clock source for "clk_lin" also allows the LIN module to continue communication on the LIN Bus even if the clock "clk_p_rw" is stopped.

Note1: If 115.2K baud rate frequency needs to be met, then 24 MHz clock source should be used for LIN communication clock. 115.2Kbps is outside a LIN standard. This function should check an operating condition by the product side.

Note2: An input clock frequency is dependent on the baud rate to support. Please set up a clock frequency in less than 96MHz by the product side.

Note3: In the case of the LIN communication clock (clkc) and the peripheral are asynchronous design:

$$freq_{(pclk)} \geqq freq_{(clkc)} * 2$$

In the case of the LIN communication clock (clkc) and the peripheral are synchronous design:

$$freq_{(pclk)} = freq_{(clkc)} * n$$

$$n \geqq 1, \text{ Integer number}$$

Note4: Some values of clock frequency for PCLK_LIN are not suitable due to the tolerance range of 0.5% allowed for the LIN Master mode Baud Rate in the LIN Specifications. Appropriate clock must be chosen after
calculating the values of baud rate tolerance based on the clock source frequency and the required baud rate.

7.2 BAUD RATE GENERATOR

As per LIN specification, the RLIN module should support all bit rates in the range of 1 to 20 Kbps. However in today's applications in the market only four bit rates are important, viz. 19.2, 9.6, 2.4 and 10.417 Kbps. Therefore, the BRG is designed based on these requirements.
RLIN3 is additionally required to support some higher baud rate values like 115.2 Kbps and 38.4 Kbps in LIN mode.

The proper baud rate generation clock frequencies used to feed the LIN / UART Controller logic are derived by scaling down the input frequency through prescalers.

The Baud Rate generation logic is separated for LIN Master mode operation and the LIN slave mode or UART mode operation.

The following Figure 7-1 explains the Baud rate source clock generation logic for LIN Master mode.

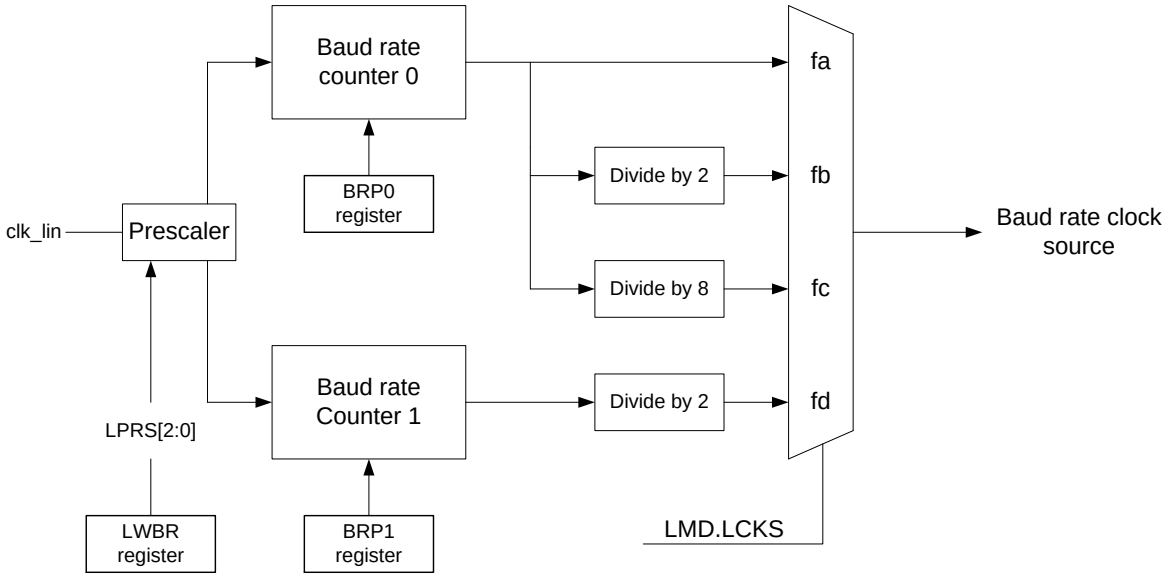


Figure 7-1: Baud rate generation logic in Master mode

The baud rate source clock "fa" is generated by dividing the input clock "clk_lin" based on the value programmed in the LBRP0 register.

Frequency of "fa" = (frequency of clk_lin divided by Prescaler) / ((LBRP0 value) + 1)
Frequency of "fb" = (frequency of "fa") / 2
Frequency of "fc" = (frequency of "fa") / 8
Frequency of "fd" = [(frequency of clk_lin divided by Prescaler) / ((LBRP1 value) + 1)] / 2

Users should calculate the values of "fa", "fb", "fc" and "fd" baud rate clock frequencies based on the input clock "clk_lin" frequency and the LBRP0 and LBRP1 register values and then select the appropriate clock source for baud rate generation.

Note 1: The baud rate clock source will be further divided based on the number of samples per bit to generate the actual baud rate.

Baud rate clock source frequency = (required baud rate) * (number of samples per bit)

The following Figure 7-2 explains the Baud rate source clock generation logic for LIN Slave mode or UART mode.

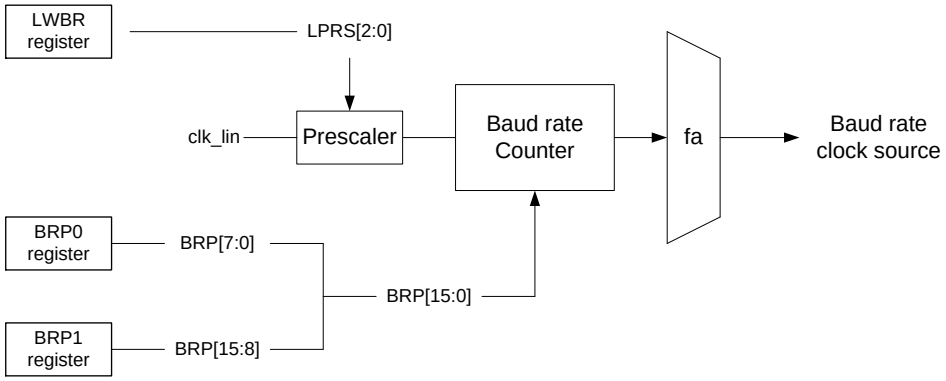


Figure 7-2: Baud rate generation logic in LIN Slave mode or UART mode

The input LIN communication clock "clk_lin" is divided based on the value programmed in the BRP[15:0] bits in the LBRP1 and LBRP0 registers and LPRS[2:0] bits in LWBR register.

In LIN Slave mode and UART mode, users should not select "fb", "fc" and "fd" as Baud rate clock source and should only select "fa" as the Baud rate clock source.

Frequency of "fa" = (frequency of counter clock source) / ((BRP value) + 1).

Users should configure the BRP[15:0] value and LPRS[2:0] value to generate the required clock source for baud rate generation (refer to section 4.1, 4.2.2 and 4.3.2).

Note 2: The baud rate clock source will be further divided based on the number of samples per bit to generate the actual baud rate.

Baud rate clock source frequency = (required baud rate) * (number of samples per bit)

The number of samples per bit should be configured in the NSPB[3:0] bits of the LWBR register (refer to section 4.1).

Note3: In LIN communication automatic baud rate mode, The Frequency Division Value (BRP[15:0] bits in the LBRP1 and LBRP0 registers) should be set to 15 or more. If less than 15, it is not possible to guarantee a normal operation.

7.3 AUTOMATIC BAUD RATE DETECTION

In LIN communication automatic baud rate mode, a Break Field and SYNC field are automatically detected and the baud rate setting (BRP[15:0] bits) is corrected according to the measurement result of the SYNC field. Prescaler clock should be configured to 4 to 48MHz in Automatic Baud Rate detection. Operation can be performed with the baud rate of the following table.

Table 7-1: Baud rate range for LIN Slave with Auto baud rate

Prescaler clock [MHz]	4	8	10	12	16	20	24	32	40	48
Sampling per bit	4	4	4	4	4	4	4	4	4	4
Maximum baud rate [bps]	26000	53000	69000	80000	107000	115200	115200	115200	115200	115200
Minimum baud rate [bps]	1000	1200	1500	1800	2350	2950	3550	4700	5900	7050

Prescaler clock [MHz]	4	8	10	12	16	20	24	32	40	48
Sampling per bit	8	8	8	8	8	8	8	8	8	8
Maximum baud rate [bps]	13000	26000	34000	41000	53000	69000	80000	107000	115200	115200
Minimum baud rate [bps]	1000	1200	1500	1800	2350	2950	3550	4700	5900	7050

Communication clock (Slave) frequency deviation: Typ±15%
The clock deviation from the target baud rate after correction: Typ±1.5%

7.3.1 Automatic baud rate correction function

Received low-level widths are always measured when in automatic baud rate mode.
Break Field detection is judged as being performed successfully when the first low-level width is at least 10 (LBFC[0] = 0) or 11 (LBFC[0] = 1) times the 1 Bit period width calculated as an average over the first 2 bits of SYNC field (period between first 2 consecutive falling-edges of SYNC field).
When it has been confirmed that the SYNC field data is 55h, successful SYNC field detection is judged and baud rate correction results are automatically set to the BRP register bits.
A reception complete interrupt request signal is generated when there are no errors upon ID reception completion (stop bit position).
On the other hand, when the data is not 55H, SYNC field detection is judged to have failed.
An error flag is set and a status interrupt request signal is generated when there is an error.

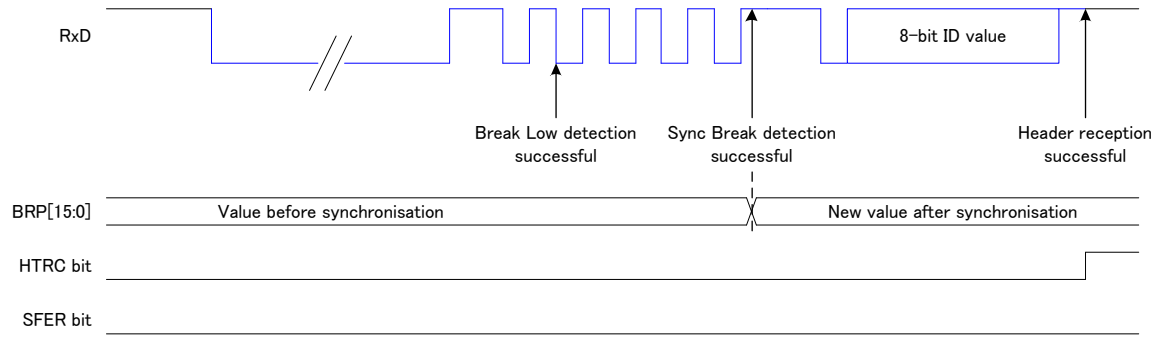


Figure 7-3: Automatic baud rate generation diagram (no errors)

In this case the module will wait for the detection of the next Break Field (low level).
The transmission or reception processing is stopped, and baud rate correction is not performed.
RLIN3 may be generated framing errors and bit errors, if the detection of new header during header reception, response transmission or reception
This is also applicable when a Break Field has been received during communication.

Designers Information:
Operation cannot be guaranteed when a baud rate changes more than two times.

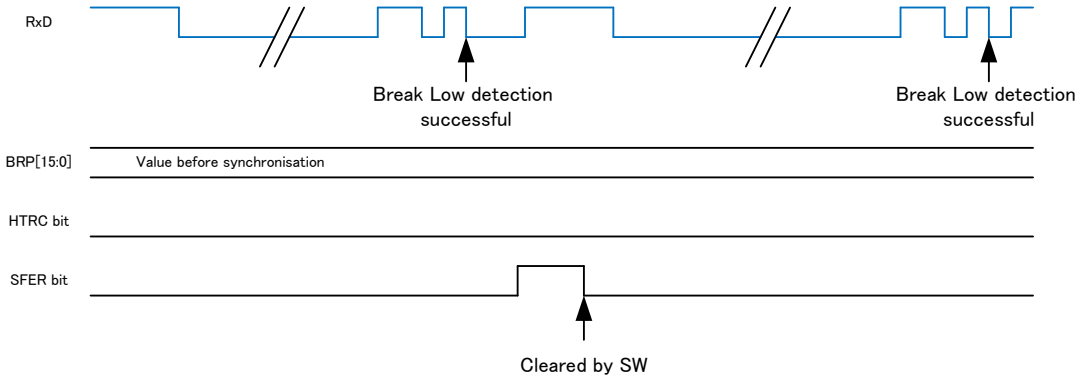


Figure 7-4: Automatic baud rate generation diagram (Sync field error)

7.3.2 Response preparation error detection function

If response preparation is not performed before reception of the 1st byte by a response is completed (sampling point of the stop bit (1st bit)), a response preparation error flag is set, a status interrupt request signal is generated, and subsequent transmission and reception processing are stopped (responses are ignored) with the 1st byte data being stored.
When only the RLIN3 module has performed response transmission, no response preparation error occurs, because reception is not performed at the RxD pin.
When response transmission is started after reception has started at the RxD pin (another node has started transmission of response already), then, this condition will cause Bit errors when the response bit transmitted by RLIN3 module does not match the response bit transmitted by the other node.

7.4 LIN DATA TRANSMISSION/RECEPTION

7.4.1 LIN Data Transmission

In LIN Master mode and LIN Slave (Fixed baud rate) mode 1 Tbit is generated from 16 basic clock cycles. The sampling point used to check the data read back from the LIN bus and detect Bit Error, is located at the 13th clock cycle (position of 81.25%).
However, 1 Tbit is generated from 4 or 8 basic clock cycles in LIN Slave (Auto baud rate) mode. The sampling point used to check the data read back from the LIN bus and detect Bit Error, is located at the 3rd or 7th clock cycle (position of 75% or 87.5%).

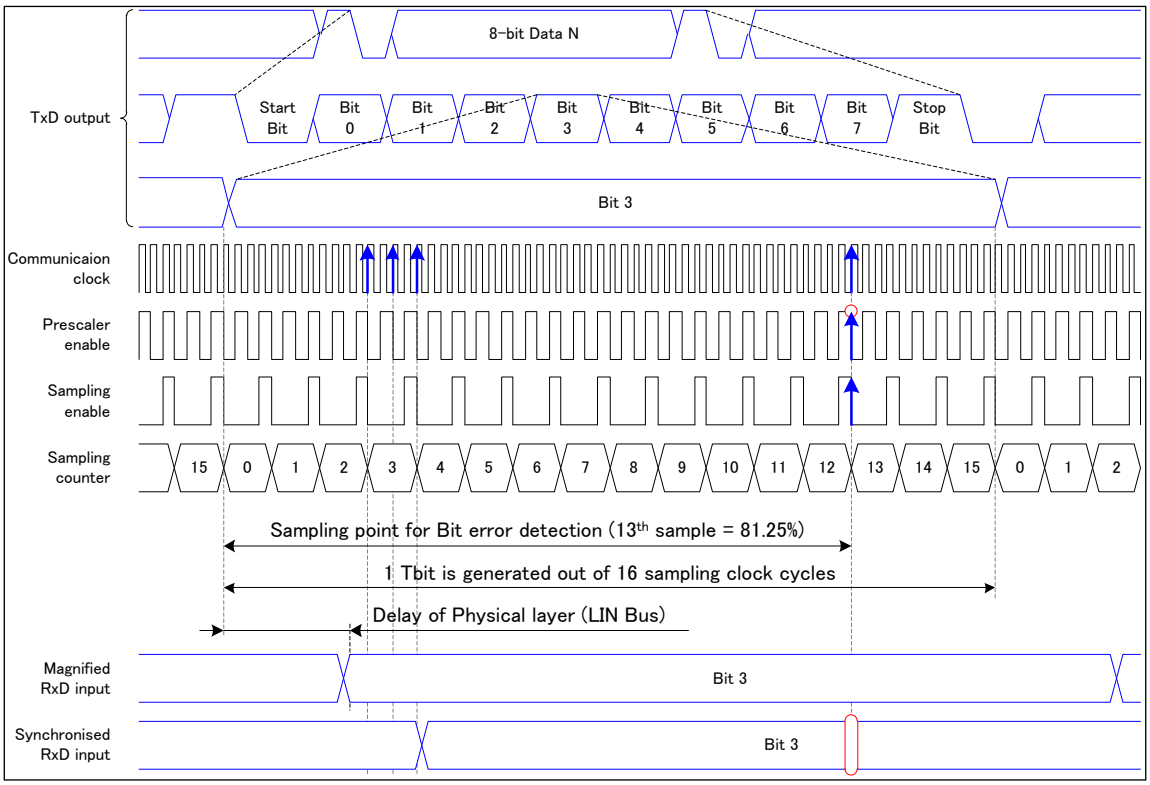


Figure 7-5: Data transmission in LIN Master and Slave (Fixed baud rate) mode

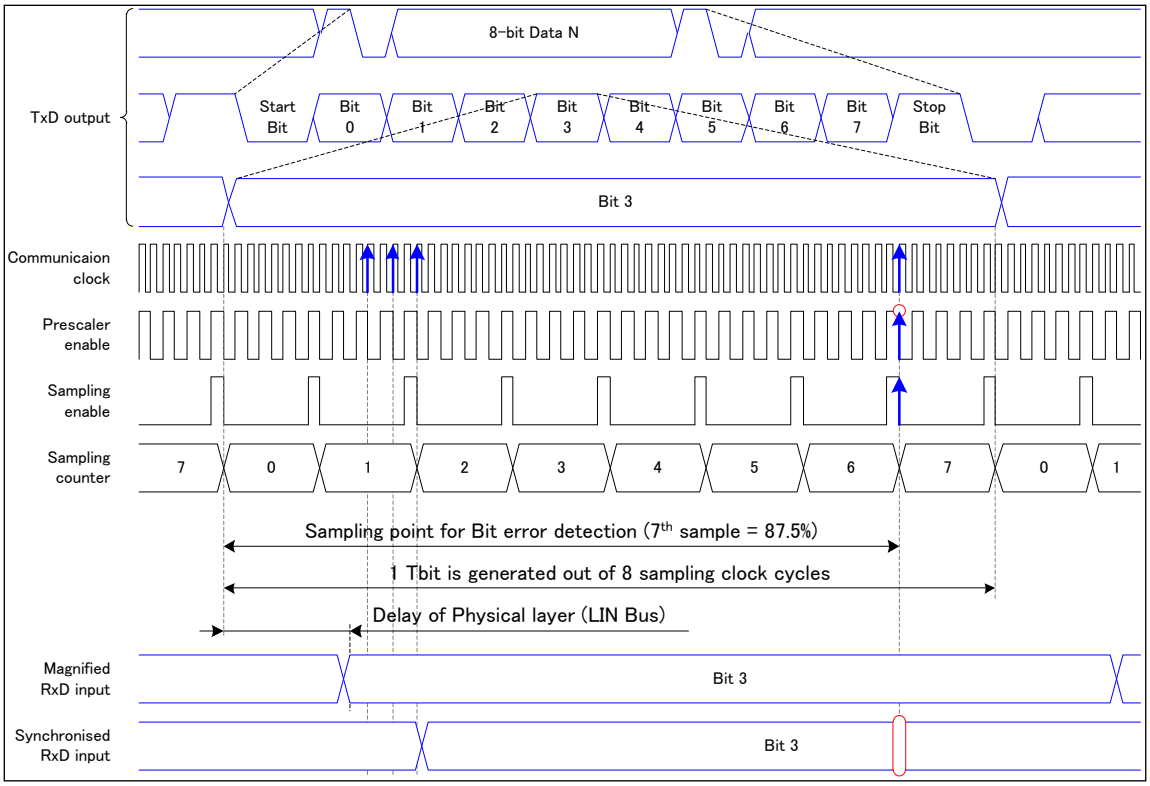


Figure 7-6: Data transmission in LIN Slave (Auto baud rate) mode

7.4.2 Speed-Performance of the LIN Transceiver

From speed performance analysis of the data sheet of existing LIN transceivers in the market, it is possible to confirm that Bit Error judgment in transmission can be performed without problems within the full range of the speed allowed on the LIN bus (If the delay from TxD to RxD is 40.6µs or shorter) if the Bit error judgement is performed at 81.25% of the bit.

7.4.3 LIN Data Reception

Reception is synchronised at the start bit (Low) of each data-byte.
Three points sampling is used to detect a bit if enabled by SW drivers. As far as the detection of the Start Bit is concerned, a bit is acknowledged as a Start Bit if "Low" is detected at a position 0.5Tbit after detection of an edge of H → L.
In case a falling edge is detected (example: due to noise) on the RxD input and a "High" level is detected at 0.5Tbit position, the bit is not recognised as a Start Bit.
If Framing error is disabled and stop bit is sampled as "LOW", then RLIN3 detects beginning of next START bit only when a "falling-edge" occurs on the RxD input pin.
Once the start bit is detected, data bits are sampled every 1 Tbit.

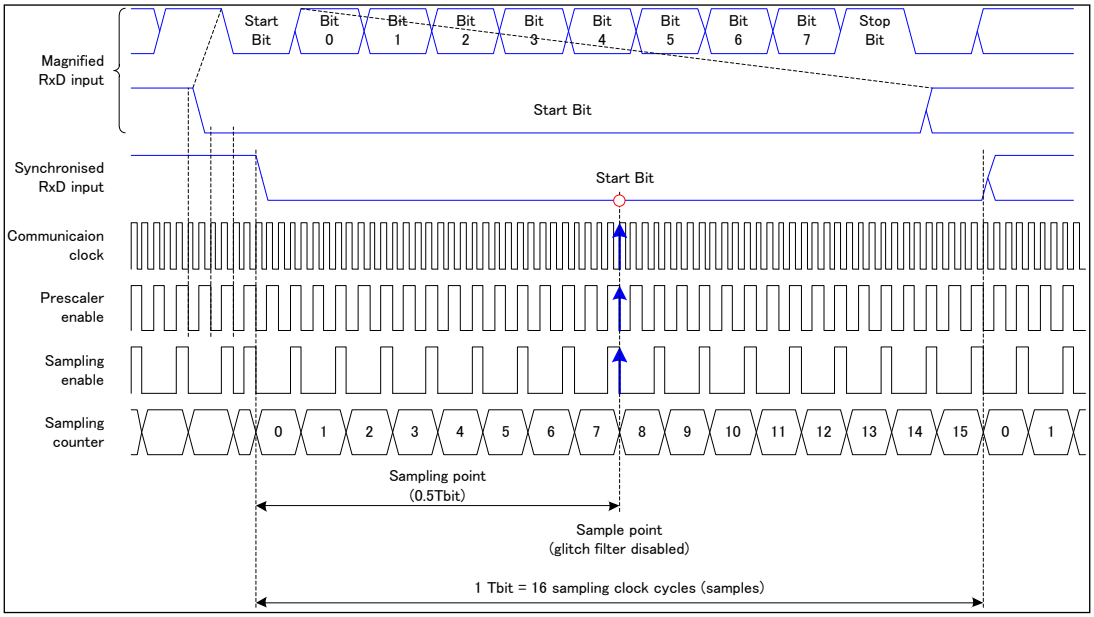


Figure 7-7: Data reception in LIN Master and Slave (Fixed baud rate) mode (glitch filter disabled)

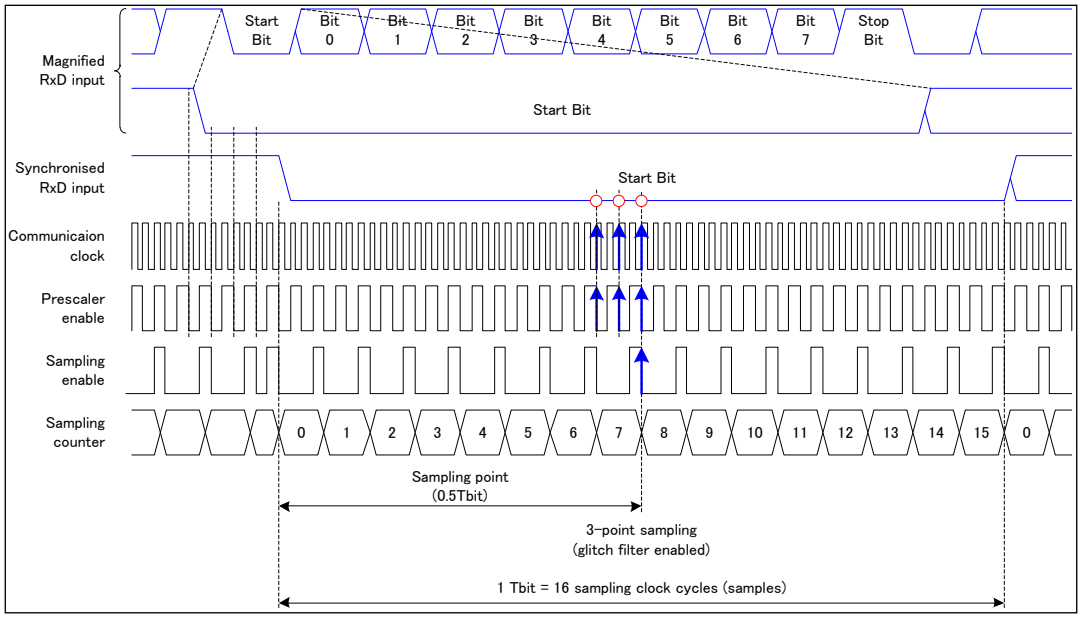


Figure 7-8: Data reception in LIN Master and Slave (Fixed baud rate) mode (glitch filter enabled)

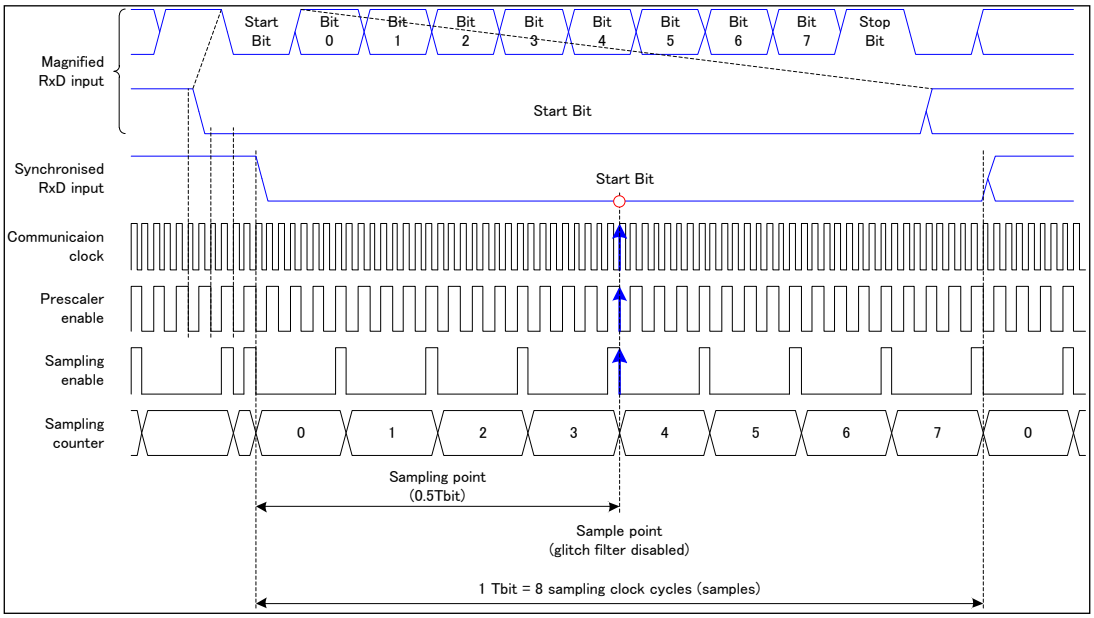


Figure 7-9: Data reception in LIN Slave (Auto baud rate) mode (glitch filter disabled)

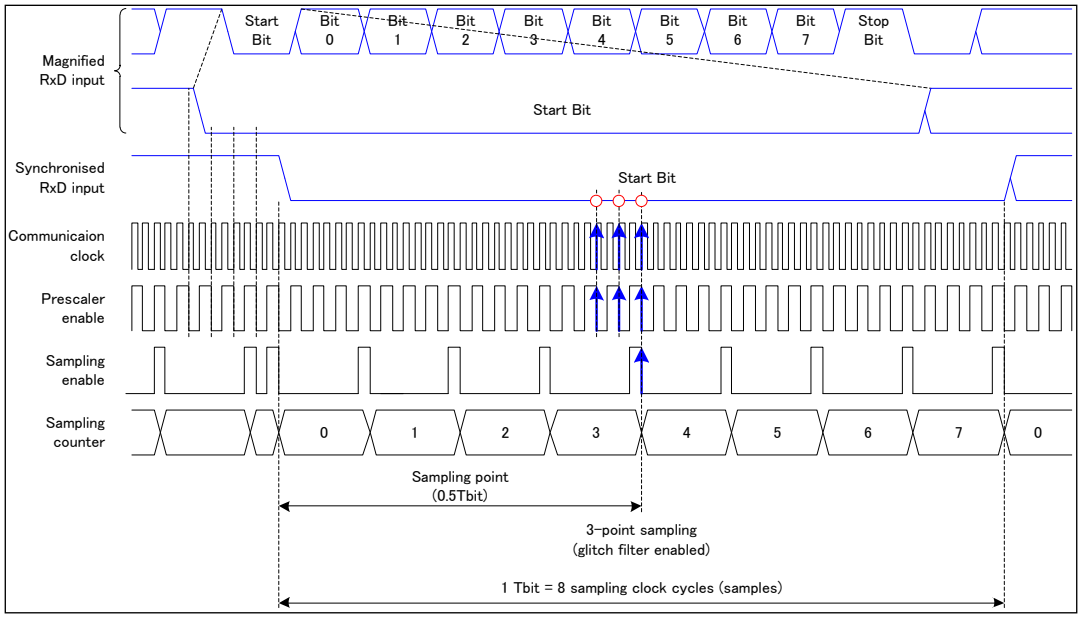


Figure 7-10: Data reception in LIN Slave (Auto baud rate) mode (glitch filter enabled)

7.5 UART DATA TRANSMISSION/RECEPTION

7.5.1 UART Data Transmission

In UART mode 1 Tbit is generated from 6-16 basic clock cycles. In Half duplex, the sampling point used to check the data read back from reception path and detect Bit Error, is located at the 0.5Tbit + 1 Prescaler clock cycle.

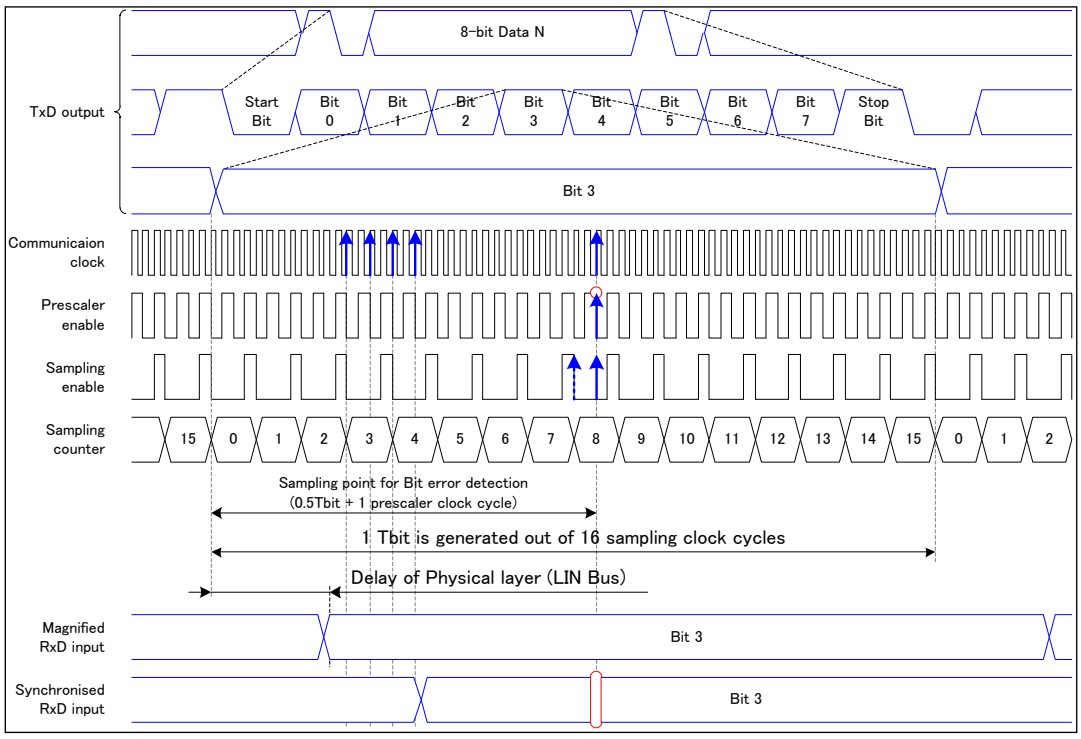


Figure 7-11: Data transmission in UART mode (16 sampling)

7.5.2 UART Data Reception

Reception is synchronised at the start bit (Low) of each data-byte.
Three points sampling is used to detect a bit if enabled by SW drivers. As far as the detection of the Start Bit is concerned, a bit is acknowledged as a Start Bit if "Low" is detected at a position 0.5Tbit after detection of an edge of H → L.
In case a falling edge is detected (example: due to noise) on the RxD input and a "High" level is detected at 0.5Tbit position, the bit is not recognised as a Start Bit.
However, if Bit error detection is enabled, the sampling position is 0.5Tbit + 1 Prescaler cycle from the position of Start Bit for the transmission.
If Framing error is disabled and stop bit is sampled as "LOW", then RLIN3 detects beginning of next START bit only when a "falling-edge" occurs on the RxD input pin.
Once the start bit is detected, data bits are sampled every 1 Tbit.

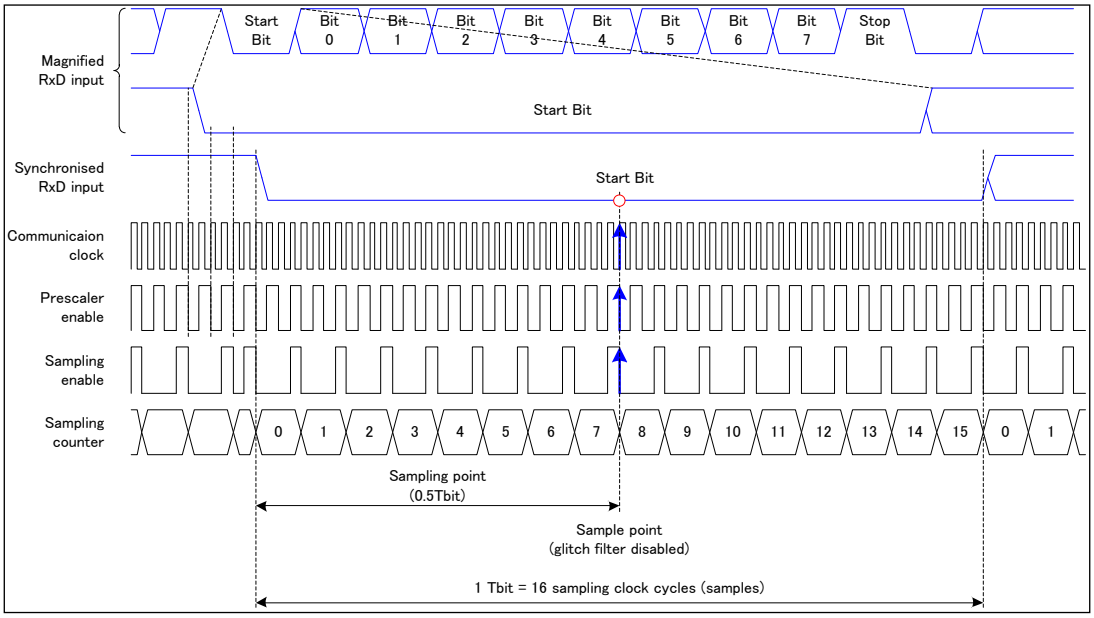


Figure 7-12: Data reception in UART mode (glitch filter disabled)

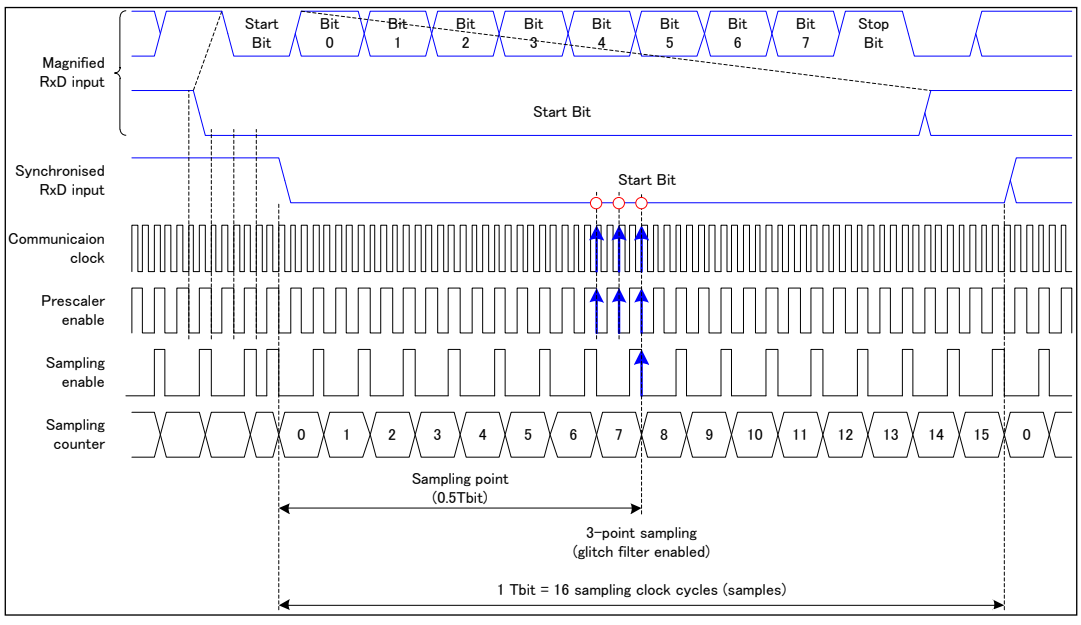


Figure 7-13: Data reception in UART mode (glitch filter enabled)

7.5.3 UART Data Transmission/Reception (Odd number Sampling)

[UART Data Transmission]
The sampling point used to check the data read back from reception path and detect Bit Error, is located at the (number sampling + 1) / 2 sampling position + 1 Prescaler clock cycle.

[UART Data Reception]
The sampling point is located at the (number sampling + 1) / 2 sampling position.
On the other hand, if Bit error detection is enabled, the sampling point is (number sampling + 1) / 2 sampling position + 1 Prescaler cycle from the position of Start Bit for the transmission.

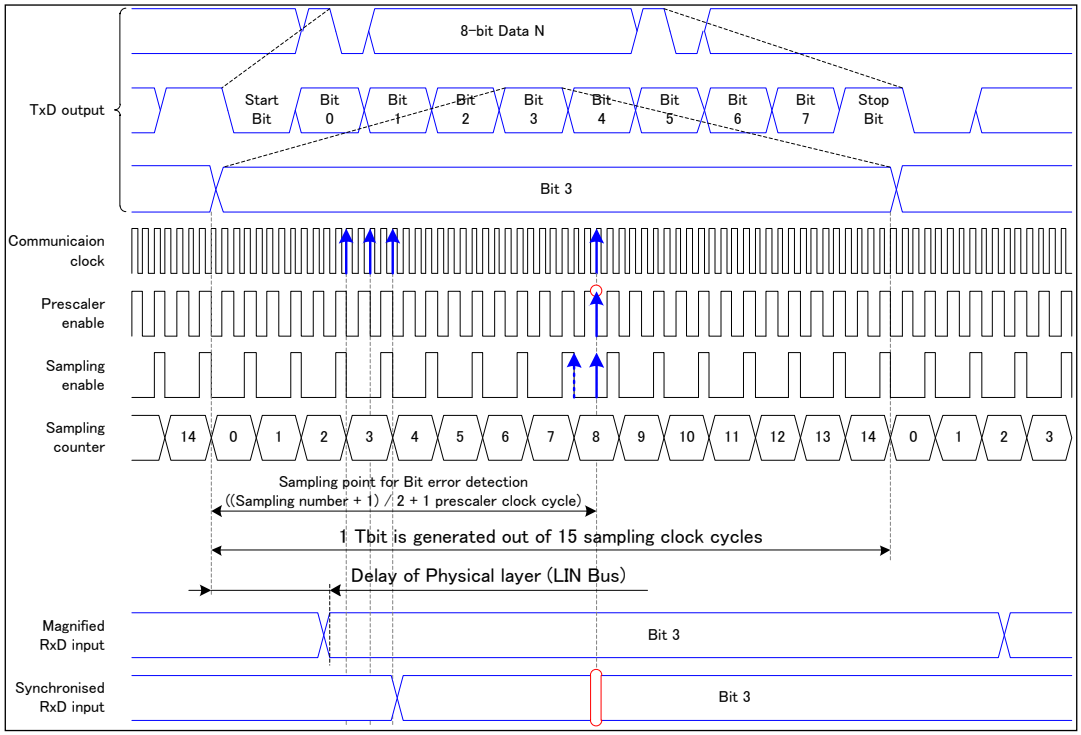


Figure 7-14: Data transmission in UART mode (15 sampling)

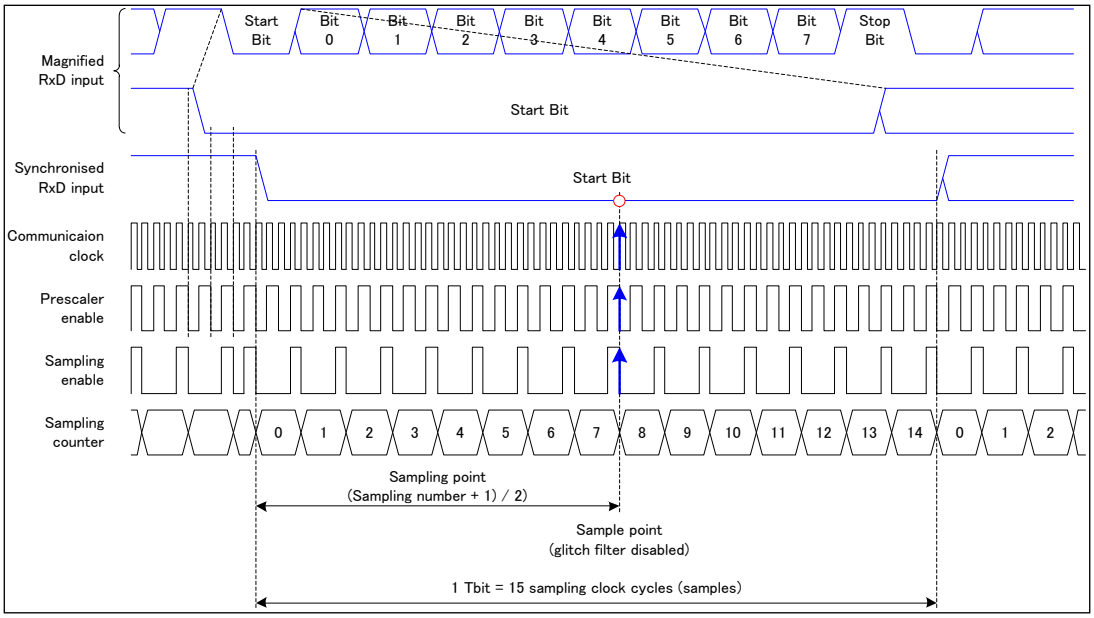


Figure 7-15: Data reception in UART mode (glitch filter disabled and 15 sampling)

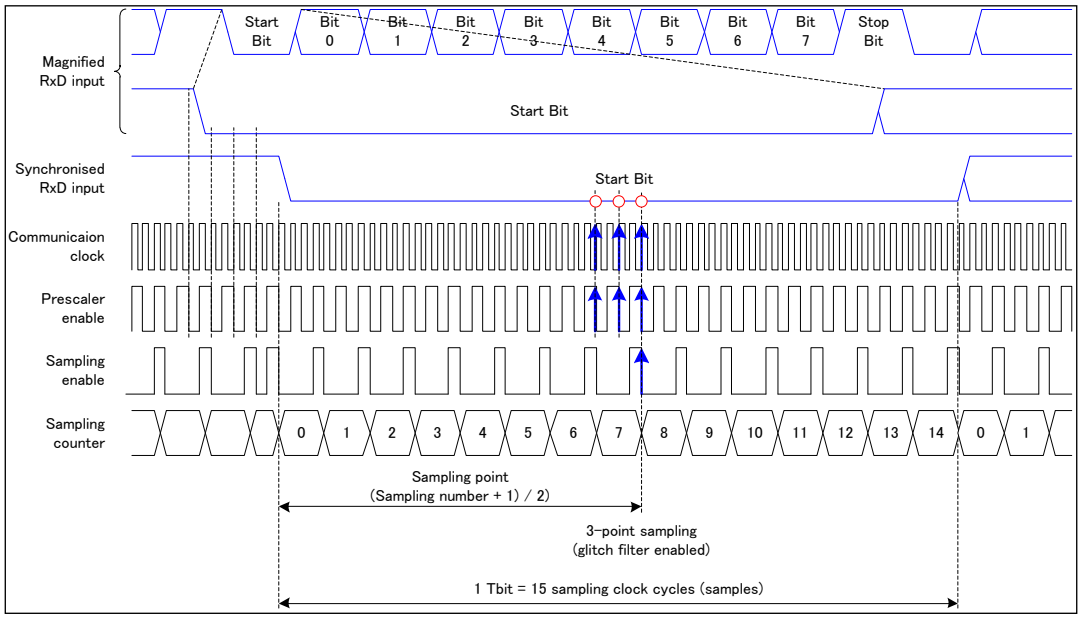


Figure 7-16: Data reception in UART mode (glitch filter enabled and 15 sampling)

7.6 HANDLING OF THE TRANSMIT/RECEIVE DATA WITH BUFFERS

This section gives an explanation on the buffer operation on successive data transmission/reception of the LIN and UART frames.

7.6.1 Transmission/Reception of the LIN frame

7.6.1.1 Transmission

In case of 8-byte transmission, the contents stored in the DATA Buffer 1 ~ 8 are transmitted to the spaces of DATA1 ~ DATA8 of the LIN Frame in a relevant order. In case of 4-byte transmission, the contents of the DATA Buffers 1 ~ 4- are output to the spaces of DATA1 ~ DATA4 of the LIN Frame; contents of the DATA Buffer 5~8 are not transmitted.

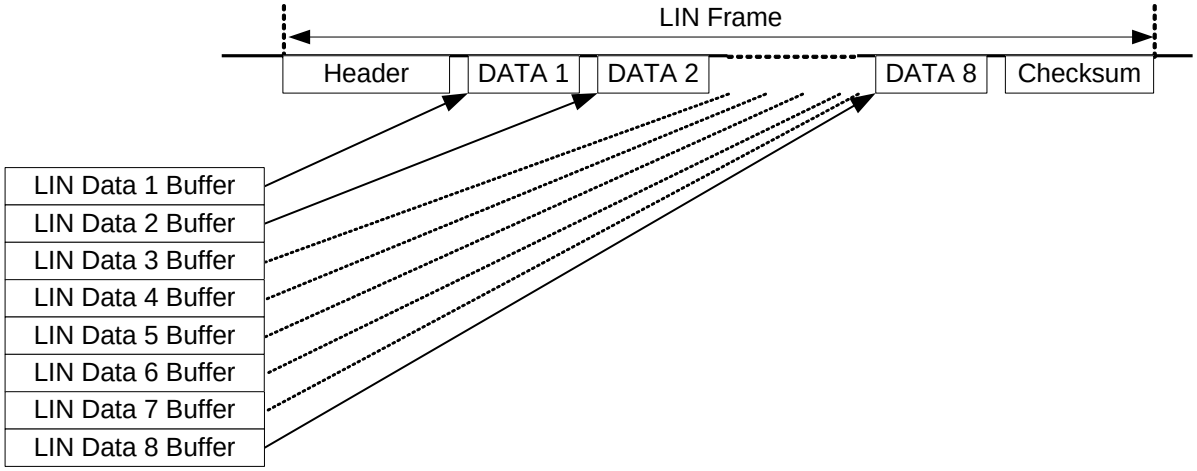


Figure 7-17: LIN transmission operation and buffers

7.6.1.2 Reception

In case of 8-byte reception, the contents of the areas of DATA1 ~ DATA8 of the LIN Frame are stored to the DATA Buffer 1 ~ 8 on every successful reception of a Stop Bit. In case of 4-byte reception, the contents of the areas of DATA1 ~ DATA4 of the LIN Frame are stored to the DATA Buffer 1 ~ 4. Data in the DATA Buffers 5 ~ 8 is unchanged.

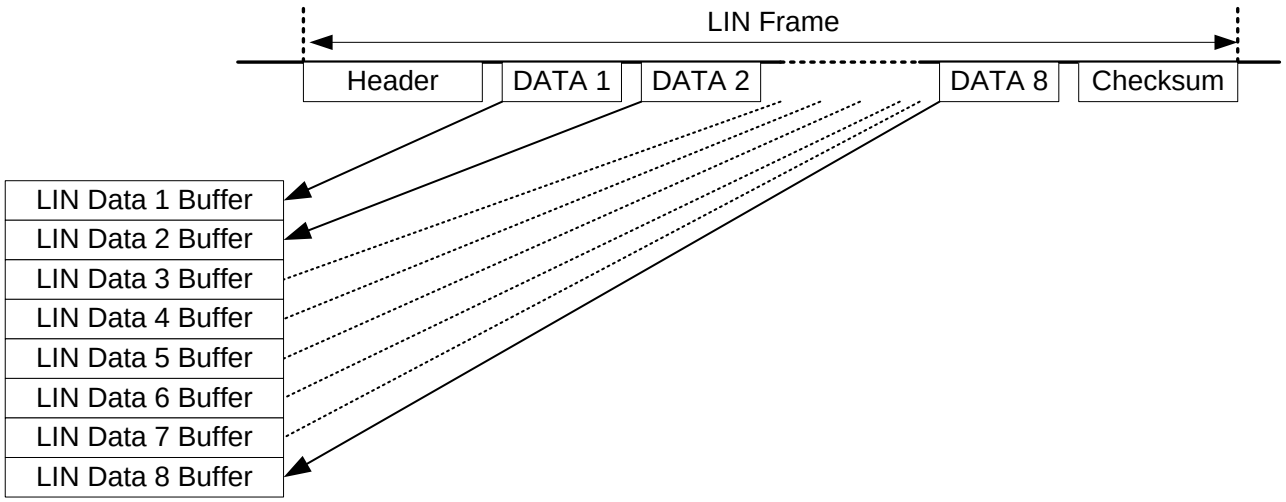


Figure 7-18: LIN reception operation and buffers

7.6.2 UART multi-byte Transmission

In case of 9-byte transmission, the contents stored in the DATA Buffer 0 ~ 8 are transmitted in DATA0 to DATA8 spaces successively. DATA Buffer 0 is used only when 9-byte transmission is selected. In all other cases DATA Buffers 1~ 8 are selected depending on the data length. In case of 4-byte transmission, the contents of the DATA Buffers 1 ~ 4 are transmitted in the DATA1 to DATA4 spaces successively. Contents of the DATA Buffers 5 ~ 8 are not transmitted. A successful Transmission Interrupt is generated after the successful transmission of the number of bytes specified in data length register. The space in between each byte transmitted complies with the inter-byte space length configuration.

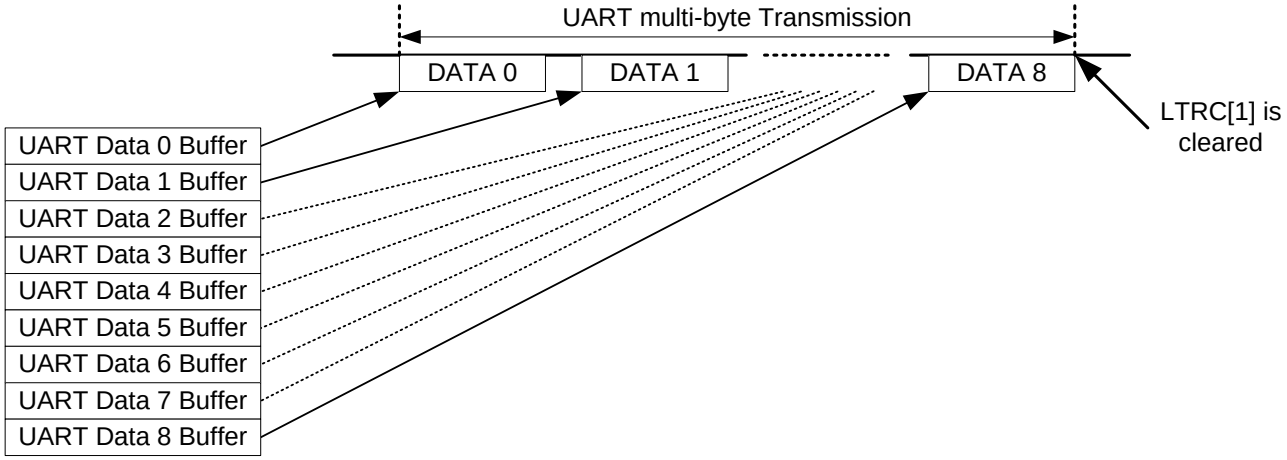


Figure 7-19: UART successive transmission operation and buffers (9-byte)

7.7 INTERRUPT OUTPUT GENERATION IN LIN / UART MODES.

7.7.1 LIN mode Interrupts

In LIN mode, an Interrupt request is generated for the following conditions

- Successful Transmission of Response or Header (only in LIN Master mode) or Wake-up signal
- Successful Reception of Response or Header (only in LIN Slave mode) or Wake-up signal
- Error Detection during Header or Response or Response Space.

The related flags will also be set in the LIN Status register and the LIN Error Status register.

Note: For interrupt generation in LIN Master or LIN Slave mode, users should set the related interrupt enable bits in the LIE register.

7.7.1.1 Successful transmission interrupt request condition

The interrupt is generated for the following conditions in LIN Master or LIN Slave mode:

- Successful header transmission in LIN Master mode
- Successful response transmission in LIN Master or LIN Slave mode
- Successful wake-up transmission in LIN Master or Lin Slave mode

7.7.1.2 Successful reception interrupt request condition

The interrupt is generated for the following conditions in LIN Master or LIN Slave mode:

- Successful header reception in LIN Slave mode
- Successful response reception in LIN Master or LIN Slave mode
- Successful wake-up reception in LIN Master or Lin Slave mode

7.7.1.3 Error interrupt request condition

The interrupt is generated when a Bit error or a Physical bus error or a Timeout error or a Framing error or a Checksum error or a Response preparation error is detected in LIN Master mode.

The interrupt is generated when a Bit error or a Timeout error or a Framing error or a Sync field error Checksum error or LIN Identifier parity error or a Response preparation error is detected in LIN Slave mode.

7.7.1.4 Interrupt generation timings

A successful header transmission interrupt is generated when the last bit of the ID field was transmitted without any error.

A successful response transmission interrupt is generated when the last bit of either the last data byte or the last data byte in every data group was transmitted without any error.

A successful wake-up transmission interrupt is generated when the last bit of the configured low phase was transmitted without any error.

A successful header reception interrupt is generated when the last bit of the ID field was received without any error.

A successful response reception interrupt is generated when the last bit of either the last data byte or the last data byte in every data group was received without any error.

A successful wake-up reception interrupt is generated after 0.5 Tbit when 2.5 consecutive dominant bits where detected on the RXD input pin.

The conditions presented above are shown for each mode in the tables below.

Table 7-2: Interrupt generation timings (LIN Master mode)

Operation Mode	Enable/Status/Error Status			registers		Interrupt (#1)					Note
	Category	Register Name	Set Condition	LUOR.UTIGTS	LMD.LIOS	Mix	Tx	Rx	Status	EU	
LIN Master	Status	LIN Header Transmission / Reception flag (LST.HTRC)	End of StopBit	-	0	**1**	0	0	0	0	
				-	1	0	1	0	0	0	
		LIN Error SUM status (LTRC.ERR)	One or more errors have been set	-	0	**1**	0	0	0	0	
				-	1	0	0	0	**1**	0	
		Response Frame Reception complete (LST.FRC)	End of StopBit	-	0	**1**	0	0	0	0	
				-	1	0	0	**1**	0	0	
		Wake-up Reception complete (LST.FRC)	End of 3.0TBit (Reception determination:2.5Tbit)	-	0	**1**	0	0	0	0	
				-	1	0	0	**1**	0	0	
		Response Frame Transmission complete (LST.FTC)	End of StopBit	-	0	**1**	0	0	0	0	
				-	1	0	**1**	0	0	0	
		Wake-up Transmission complete (LST.FTC)	End of TBit width set	-	0	**1**	0	0	0	0	
				-	1	0	**1**	0	0	0	
	Error Status	LIN Response Preparation Error (LEST.RPER)	StopBit detection (Sample point)	-	0	**1**	0	0	0	0	(1)
				-	1	0	0	0	**1**	0	
		LIN CheckSum Error (LEST.CSER)	End of StopBit	-	0	**1**	0	0	0	0	
				-	1	0	0	0	**1**	0	
		LIN Framing Error (LEST.FER)	End of StopBit	-	0	**1**	0	0	0	0	(2)
				-	1	0	0	0	**1**	0	
		LIN Frame Timeout Error (LEST.FTER)	End of TBit width set	-	0	**1**	0	0	0	0	
				-	1	0	0	0	**1**	0	
		LIN Response Timeout Error (LEST.FTER)	End of TBit width set	-	0	**1**	0	0	0	0	
				-	1	0	0	0	**1**	0	
		LIN Physical Bus Error (LEST.PBER)	End of TBit	-	0	**1**	0	0	0	0	
				-	1	0	0	0	**1**	0	
		LIN Bit Error (LEST.BER)	End of Tbit (WAKEUP,IBS,RS)	-	0	**1**	0	0	0	0	(3)
				-	1	0	0	0	**1**	0	
			End of StopBit (DATA,CHECKSUM)	-	0	**1**	0	0	0	0	
				-	1	0	0	0	**1**	0	

#1:"-" : Don't care "1" : One Shot Pulse

(1): An error occurs if there is no writing of LTRC.RTS before StopBit reception of 1st byte in the response received

(2): Sample points of StopBit results in an error in the case of 'L'

(3): Two conditions do not occur simultaneously

Table 7-3: Interrupt generation timings (LIN Slave mode)

Operation Mode	Enable/Status/Error Status			registers		Interrupt (#1)					Note
	Category	Register Name	Set Condition	LUOR.UTIGTS	LMD.LIOS	Mix	Tx	Rx	Status	EU	
LIN Slave	Status	LIN Header Transmission / Reception (LST.HTRC)	StopBit detection (Sample point)	-	0	**1**	0	0	0	0	
				-	1	0	0	**1**	0	0	
		LIN Error SUM status (LTRC.ERR)	One or more errors have been set	-	0	**1**	0	0	0	0	
				-	1	0	0	0	**1**	0	
		Response Frame Reception complete (LST.FRC)	End of StopBit	-	0	**1**	0	0	0	0	
				-	1	0	0	1	0	0	
		Wake-up Reception complete (LST.FRC)	End of 3.0TBit (Reception determination:2.5Tbit)	-	0	**1**	0	0	0	0	
				-	1	0	0	**1**	0	0	
		Response Frame Transmission complete (LST.FTC)	End of StopBit	-	0	**1**	0	0	0	0	
				-	1	0	**1**	0	0	0	
		Wake-up Transmission complete (LST.FTC)	End of TBit width set	-	0	**1**	0	0	0	0	
				-	1	0	**1**	0	0	0	
	Error Status	LIN Response Preparation Error (LEST.RPER)	End of StopBit(#2)	-	0	**1**	0	0	0	0	(1)
				-	1	0	0	0	**1**	0	
		LIN Identifier Parity Error (LEST.IPER)	End of StopBit(#2)	-	0	**1**	0	0	0	0	
				-	1	0	0	0	**1**	0	
		LIN CheckSum Error (LEST.CSER)	End of StopBit(#2)	-	0	**1**	0	0	0	0	
				-	1	0	0	0	**1**	0	
		LIN SYNC field Error (LEST.SFER)	End of TBit(FB)	-	0	**1**	0	0	0	0	
				-	1	0	0	0	**1**	0	
			Bit Detection(AB) (Sample point)	-	0	**1**	0	0	0	0	
				-	1	0	0	0	**1**	0	
		LIN Framing Error (LEST.FER)	End of StopBit(#2)	-	0	**1**	0	0	0	0	(2)
				-	1	0	0	0	**1**	0	
		LIN Frame Timeout Error (LEST.FTER)	End of TBit width set	-	0	**1**	0	0	0	0	
				-	1	0	0	0	**1**	0	
		LIN Response Timeout Error (LEST.FTER)	End of TBit width set	-	0	**1**	0	0	0	0	
				-	1	0	0	0	**1**	0	
		LIN Bit Error (LEST.BER)	End of TBit (WAKEUP,IBS,RS)	-	0	**1**	0	0	0	0	(3)
				-	1	0	0	0	**1**	0	
			End of StopBit (DATA,CHECKSUM)	-	0	**1**	0	0	0	0	
				-	1	0	0	0	**1**	0	

#1: "-" : Don't care "1" : One Shot Pulse

#2: StopBit detection if a conflict with a new BreakLow detected in 9.5Tbits (Sample point)

(1): An error occurs if there is no writing of LTRC.RTS before StopBit reception of 1st byte in the response received

(2): Sample points of StopBit results in an error in the case of 'L'

(3): Two conditions do not occur simultaneously

7.7.2 UART mode Interrupts

In UART mode, the RLIN3 module outputs the following active-high pulse interrupts:

- Transmission interrupt request
- Reception completion interrupt request
- Status interrupt request
- Loop back delayed data consistency check interrupt request

7.7.2.1 Status interrupt request

A status interrupt request is generated if a Parity error, or a Framing error or an Overrun error or Bit error or ID match condition or Expansion bit detection condition occurs in UART mode.

7.7.2.2 Reception completion interrupt request

A reception complete interrupt request is generated when data is stored in the UART receive data register when the reception is enabled.
If a reception error occurs, then, a reception complete interrupt request is not generated. A status interrupt request signal is generated in this case.

The reception complete interrupt request signal is not generated if the reception is disabled.

If expansion bit operation is enabled and expansion bit data comparison is disabled, a reception complete interrupt request signal is generated when an inverted value of the configured expansion bit detection level select bit is detected as an expansion bit.

If the URDCC bit is set, then, a reception complete interrupt request signal is generated if the received Data matches the reference data in ID register in SNOOZE mode.

7.7.2.3 Transmission interrupt request

A transmission interrupt request is generated at the start of transmission if the UART Transmission Interrupt Generation Timing Select Bit is "0". The transmission interrupt request is generated when the transmission data is copied from the single byte transmit buffers or UART multi-byte transmit buffers into the transmit shift register.
A transmission interrupt request is generated at the end of transmission if the UART Transmission Interrupt Generation Timing Select Bit is "1".

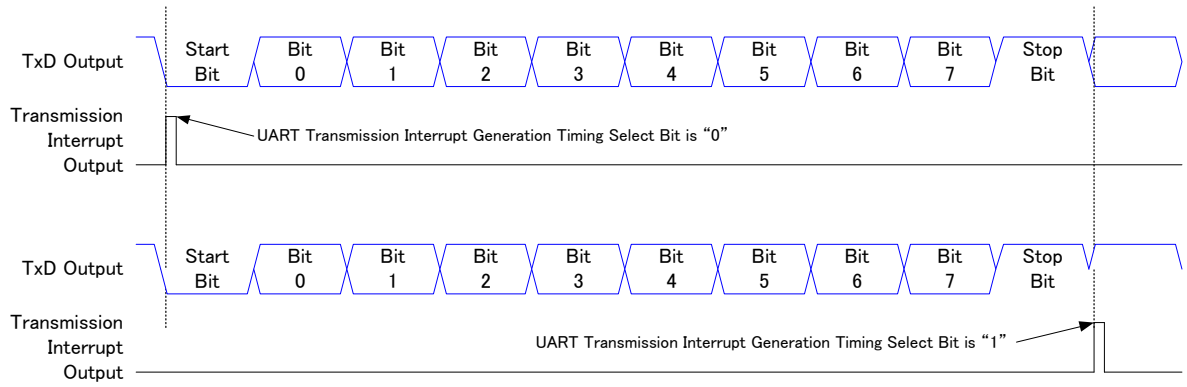


Figure 7-20: Transmission interrupt request

For UART multi-byte transmission, the Transmission interrupt is only generated for the last byte. The interrupt generation timing is the same as shown in Figure 7-20 above.

7.7.2.4 Interrupt generation timings

The table below shows the conditions for interrupt generation in UART mode.

Table 7-4: Interrupt generation timings (UART mode)

Operation Mode		Enable/Status/Error Status			registers		Interrupt (#1)					Note
		Category	Register Name	Set Condition	LUOR.UTIGTS	LMD.LIOS	Mix	Tx	Rx	Status	EU	
UART	Transmission	Status	UART Transmission Status (LST.UTS)	Writing UTDR/ Writing UWTDR/ Writing RTS(TRC[1])	0	-	0	**#2**	0	0	0	(1),(4)
					1	-	0	**#3**	0	0	0	
			Frame Transmission complete (LST.FTC)	End of StopBit	-	-	0	**1**	0	0	0	
		Error Status	UART Bit Error (LEST.BER)	End of StopBit	-	-	0	0	0	**1**	0	
	Reception	Status	UART Reception Status (LST.URS)	StartBit detection (Sample point)	-	-	0	0	**#4**	0	0	
			UART ID Match (LEST.IDMT)	StopBit detection (Sample point)	-	-	0	0	0	**1**	0	
			UART Expansion Bit Detection Flag (LEST.EXBT)	StopBit detection (Sample point)	-	-	0	0	0	**1**	0	
		Error Status	UART Parity Error (LEST.UPER)	StopBit detection (Sample point)	-	-	0	0	0	**1**	0	
			UART Framing Error (LEST.FER)	StopBit detection (Sample point)	-	-	0	0	0	**1**	0	(2)
			UART Overrun Error (LEST.OER)	StopBit detection (Sample point)	-	-	0	0	0	**1**	0	(3)
Extended UART	Transmission and Reception	Status	UART Loop-back Delayed data Consistency Error (LEST.LDCER)	StopBit detection (Sample point)	-	-	0	0	**1**	0	**1**	
				StartBit undetected(The end of the reception window)	-	-	0	0	0	0	**1**	

#1: "-" : Don't care "1" : One Shot Pulse
#2: At the start of transmission
#3: At the end of transmission
#4: At the end of Reception
(1): Each condition does not occur at the same time.
(2): Sample points of StopBit results in an error in the case of 'L'
(3): An error occurs if the reading of the received data of the previous one did not take place until the Sample point of StopBit
(4): The case of a multi-byte, interrupt output in the last byte

7.8 STATUS BITS

The table below shows the status bits, controlled by the RLIN3 module controls and the description of conditions for setting and clearing of these bits in various modes.
The status bits are present in the LIN / UART Mode Status register and the LIN / UART status register.

Table 7-5: Status bits description

Status	For setting to "1"	For clearing to "0"	Detection Mode
Reset	Internal mode control State Machine exits RESET state.	Internal mode control Sate Machine enters RESET state.	In all modes
LIN Mode	"LIN Normal" mode is requested by SW drivers.	"LIN WUP" mode is requested by SW drivers	LIN Normal, LIN WUP
Successful Transmission #1	On successful transmission of Response or WUP, and complete transmission of UART multi-byte transmission	Clearing by SW reset Clearing by write to "1" this flag Clearing by LTRC.FTS is set to "1"(LIN Mode only)	LIN Normal, LIN WUP, UART
Successful Reception #1	On successful reception of Response or WUP	Clearing by SW reset Clearing by write to "1" this flag Clearing by LTRC.FTS is set to "1"	LIN Normal, LIN WUP
Error SUM	Error Status ≠ All 0 #2	Error Status = All 0 #2	LIN Normal, LIN WUP
	Error Status ≠ All 0 #2	Error Status = All 0 #2	UART
UART Transmission Status	Frame Transmission is triggered by • Write access to UART 7bit/8bit/9bit Transmit Data Register or UART 7bit/8bit/9bit Wait Transmit Data register. • Setting of LTRC[1] bit	Clearing by SW reset • Frame transmission is complete and next transmission data is not set. • LTRC.RTS bit is cleared at the end of UART multi-byte transmission.	UART
UART Reception Status	Frame Reception Starts (START bit is detected)	Clearing by SW reset • Sampling point of stop bit is detected for the UART frame.	UART
LIN RX one byte	On successful reception of 1st Data byte	Clearing by SW reset Clearing by write to "1" this flag Clearing by LTRC.FTS is set to "1"	LIN Normal
LIN header successful	On successful transmission / reception of Header	Clearing by SW reset Clearing by write to "1" this flag Clearing by LTRC.FTS is set to "1"	LIN Normal
LIN Break Field Reception	On successful reception of Break Field	Clearing by SW reset Clearing by write to "0" this flag	LIN WUP
LIN Sync Field Reception	On successful reception of Sync Field	Clearing by SW reset Clearing by write to "0" this flag	LIN WUP

Status	For setting to "1"	For clearing to "0"	Detection Mode
Response Space Dominant Detection	A dominant level of 0.5 Tbit or more is detected from the completion of the header reception to the start of transmission.	Clearing by SW reset Detected a new sync field.	LIN slave mode

#1: In LIN Mode, Successful Transmission and Successful Reception Status get set when Transmission Frame and Reception Frame are completed without an error respectively. In UART Mode, Successful Transmission Status gets set when all programmed number of data at LDFC[3:0] bytes are successfully transmitted.

#2: Error Status denotes the content in the Error Status Register.
(without Loop-back Delayed data Consistency Error)

Note: In LIN master mode, all status flags related to LIN Master operation will be cleared when LTRC[0] bit is set.

7.8.1 Conflicts of Status Bits

The table below shows the condition of status bits that occurs at the end of single frame in LIN Master Mode. The combination not listed in the table, condition does not occur.

1: set status
0: no condition

Table 7-6: Conflicts of Status (LIN Master Mode)

Number of Conflict	Kinds of Status				
	FTC	FRC	ERR	D1RC	HTRC
1	1	0	0	0	0
	0	1	0	0	0
	0	0	1	0	0
	0	0	0	1	0
	0	0	0	0	1
2	1	0	0	0	1
	0	1	0	1	0
	0	1	0	0	1
	0	0	1	1	0
	0	0	1	0	1
	0	0	0	1	1
3	0	1	0	1	1
	0	0	1	1	1
4	-	-	-	-	-
5	-	-	-	-	-

The table below shows the condition of status bits that occurs at the end of single frame in LIN Slave Mode. The combination not listed in the table, condition does not occur.

1: set status
0: no condition

Table 7-7: Conflicts of Status (LIN Slave Mode)

Number of Conflict	Kinds of Status				
	FTC	FRC	ERR	D1RC	HTRC
1	1	0	0	0	0
	0	1	0	0	0
	0	0	1	0	0
	0	0	0	1	0
	0	0	0	0	1
2	1	0	0	0	1
	0	1	0	1	0
	0	1	0	0	1
	0	0	1	1	0
	0	0	1	0	1
	0	0	0	1	1
3	0	1	0	1	1
	0	0	1	1	1
4	-	-	-	-	-
5	-	-	-	-	-

The table below shows the condition of status bits that occurs at the end of single frame in UART Mode. The combination not listed in the table, condition does not occur.

1: set status
0: no condition

Table 7-8: Conflicts of Status (UART Mode)

Number of Conflict	Kinds of Status			
	FTC	ERR	UTS	URS
1	1	0	0	0
	0	1	0	0
	0	0	1	0
	0	0	0	1
2	1	1	0	0
	0	1	1	0
	0	1	0	1
	0	0	1	1
	1	0	0	1
3	-	-	-	-
4	-	-	-	-

7.8.2 Conflicts of Set and Clear timing in Flag and Status Bits

The table below shows the conflict of set and clear timing in flag and status bits that occurs at single frame in All Mode.

Table 7-9: Conflicts of Set and Clear timing in Flag and Status Bits (Common)

Operation Mode		Enable / Status / Error Status			
		Category	Register Name	Set Condition (Number is priority)	Clear Condition (Number is priority)
Common	—	Status	LIN/UART Reset bit (LCUC.OMM0)	②LCUC.OM0 is set to '1'(SW reset is inactive)	①LCUC.OM0 is cleard to '0'(SW reset is active)
			LIN/UART mode select bit (LCUC.OMM1)	②LCUC.OM1 is set to '1'(Normal)	①LCUC.OM1 is cleard to '0'(Wake-Up)

Note 1: Number is priority.

The table below shows the conflict of set and clear timing in flag and status bits that occurs at single frame in LIN Master Mode.

Table 7-10: Conflicts of Set and Clear timing in Flag and Status Bits (LIN Master)

Operation Mode		Enable / Status / Error Status			
		Category	Register Name	Set Condition (Number is priority)	Clear Condition (Number is priority)
LIN	Master	Operation Control	Response Transmission or Reception start bit (LTRC.RTS)	③LTRC.RTS is set to '1'	①LCUC.OMO is cleard to '0'(SW reset is active) ②Ssuccessful completion of Frame (TX or RX of the last data byte) ②Detection of the error
			LIN Communication start bit (LTRC.FTS)	③LTRC.FTS is set to '1'	①LCUC.OMO is cleard to '0'(SW reset is active) ②Ssuccessful completion of Frame (TX or RX of the last data byte) ②Detection of the error
		Status	LIN Header Transmission / Reception flag (LST.HTRC)	②End of StopBit(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LST.HTRC is cleard to '0'
			LIN One byte reception flag (LST.DIR)	②Detection of StopBit(Sample point)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LST.DIR is cleard to '0'
			LIN Error SUM status (LTRC.ERR)	Error Status ≠ All 0	Error Status = All 0
			Frame Reception complete flag(Response) (LST.FRC)	②End of StopBit(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LST.FRC is cleard to '0'
			Frame Reception complete flag(WakeUp) (LST.FRC)	②End of 3.0TBit(End of Bit) (Judgment of reception : 2.5Tbit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LST.FRC is cleard to '0'
			Frame Transmission complete flag(Response) (LST.FTC)	②End of StopBit(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LST.FTC is cleard to '0'
			Frame Transmission complete flag(WakeUp) (LST.FTC)	②End of window at Setting Value(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LST.FTC is cleard to '0'
		Error Status	LIN Response Preparation Error flag (LEST.RPER)	②Detection of StopBit(Sample point)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.RPER is cleard to '0'
			LIN CheckSum Error flag (LEST.CSER)	②End of StopBit(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.CSER is cleard to '0'
			LIN Framing Error flag (LEST.FER)	②End of StopBit(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.FER is cleard to '0'
			LIN Timeout Error flag (Frame Timeout) (LEST.FTER)	②End of window at Setting Value(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.FTER is cleard to '0'
			LIN Timeout Error flag (Response Timeout) (LEST.FTER)	②End of window at Setting Value(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.FTER is cleard to '0'
			LIN Physical Bus Error flag (LEST.PBER)	②End of Bit(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.PBER is cleard to '0'
			LIN Bit Error flag (LEST.BER)	②End of Bit(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.BER is cleard to '0'
				②End of StopBit(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.BER is cleard to '0'

Note 1: Number is priority.

The table below shows the conflict of set and clear timing in flag and status bits that occurs at single frame in LIN Slave Mode.

Table 7-11: Conflicts of Set and Clear timing in Flag and Status Bits (LIN Slave)

Operation Mode		Enable / Status / Error Status			
		Category	Register Name	Set Condition (Number is priority)	Clear Condition (Number is priority)
LIN	Slave	Operation Control	LIN No Response Request bit (LTRC.LNRR)	③LTRC.LNRR is set to '1'	①LCUC.OMO is cleard to '0'(SW reset is active) ②detection of a Sync field
			Response Transmission or Reception start bit (LTRC.RTS)	③LTRC.RTS is set to '1'	①LCUC.OMO is cleard to '0'(SW reset is active) ②Ssuccessful completion of Frame (TX or RX of the last data byte) ②Detection of the error ②Detection of a Sync field
			LIN Communication start bit (LTRC.FTS)	②LTRC.FTS is set to '1'	①LCUC.OMO is cleard to '0'(SW reset is active)
		Status	LIN Header Transmission / Reception flag (LST.HTRC)	②Detection of StopBit(Sample point)	①LCUC.OMO is cleard to '0'(SW reset is active) ③LST.HTRC is cleard to '0'
			LIN One byte reception flag (LST.DIR)	②Detection of StopBit(Sample point)	①LCUC.OMO is cleard to '0'(SW reset is active) ③LST.DIRC is cleard to '0'
			LIN Error SUM status (LTRC.ERR)	Error Status ≠ All 0	Error Status = All 0
			Frame Reception complete flag(Response) (LST.FRC)	②End of StopBit(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LST.FRC is cleard to '0'
			Frame Reception complete flag(WakeUp) (LST.FRC)	②End of 3.0TBit(End of Bit) (Judgment of reception : 2.5Tbit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LST.FRC is cleard to '0'
			Frame Transmission complete flag(Response) (LST.FTC)	②End of StopBit(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LST.FTC is cleard to '0'
			Frame Transmission complete flag(WakeUp) (LST.FTC)	②End of window at Setting Value(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LST.FTC is cleard to '0'
			LIN Break Field Reception flag (LBSS.BRKC)	②Detection of Break Delimiter(FB mode) (Sampling point)	①LCUC.OMO is cleard to '0'(SW reset is active) ③LBSS.BRKC is cleard to '0'
				②Detection of Break Delimiter(AB mode) (End of bit0 of Sync field)	①LCUC.OMO is cleard to '0'(SW reset is active) ③LBSS.BRKC is cleard to '0'
			LIN Sync Field Reception flag (LBSS.SYCC)	②Detection of StopBit(Sample point)	①LCUC.OMO is cleard to '0'(SW reset is active) ③LBSS.SYCC is cleard to '0'
			Response Space Dominant Reception flag (LRSS.RSDD)	③Detection of Dominant noise(0.5Tbit)	①LCUC.OMO is cleard to '0'(SW reset is active) ②Detection of a Sync field(Sample point)
		Error Status	LIN Response Preparation Error flag (LEST.RPER)	②End of StopBit(End of Bit) (Detection of StopBit(Sample point), If detection conflicts with new BreakLow detection in LINSlave FB mode (LBFC.LBLT="0"))	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.RPER is cleard to '0'
			LIN Identifier Parity Error flag (LEST.IPER)	②End of StopBit(End of Bit) (Detection of StopBit(Sample point), If detection conflicts with new BreakLow detection in LINSlave FB mode (LBFC.LBLT="0"))	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.IPER is cleard to '0'
			LIN CheckSum Error flag (LEST.CSER)	②End of StopBit(End of Bit) (Detection of StopBit(Sample point), If detection conflicts with new BreakLow detection in LINSlave FB mode (LBFC.LBLT="0"))	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.CSER is cleard to '0'
			LIN SYNC field Error flag (LEST.SFER)	②End of Bit(FB mode)(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.SFER is cleard to '0'
				②Detection of Bit(AB mode)(Sample point)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.SFER is cleard to '0'
			LIN Framing Error flag (LEST.FER)	②End of StopBit(End of Bit) (Detection of StopBit(Sample point), If detection conflicts with new BreakLow detection in LINSlave FB mode (LBFC.LBLT="0"))	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.FER is cleard to '0'
			LIN Timeout Error flag (Frame Timeout) (LEST.FTER)	②End of window at Setting Value(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.TER is cleard to '0'
			LIN Timeout Error flag (Response Timeout) (LEST.FTER)	②End of window at Setting Value(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.TER is cleard to '0'
			LIN Bit Error flag (LEST.BER)	②End of Bit(End of Bit) (WAKEUP,IBS,RS)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.BER is cleard to '0'
				②End of StopBit(End of Bit) (DATA,CHECKSUM)	①LCUC.OMO is cleard to '0'(SW reset is active) ①LTRC.FTS is set to '1' ③LEST.BER is cleard to '0'

Note 1: Number is priority.

The table below shows the conflict of set and clear timing in flag and status bits that occurs at single frame in UART / Extended UART Mode.

Table 7-12: Conflicts of Set and Clear timing in Flag and Status Bits (UART / Extended UART Mode)

Operation Mode		Enable / Status / Error Status			
		Category	Register Name	Set Condition (Number is priority)	Clear Condition (Number is priority)
UART	Common	Status	LIN Error SUM status (LTRC.ERR)	Error Status ≠ All 0	Error Status = All 0
	Tx	Operation Control	UART Transmission Operation Enable Bit (LUOER.UTOE)	②LUOER.UTOE is set to '1'	①LCUC.OMO is cleard to '0'(SW reset is active) ②LUOER.UTOE is cleard to '0'
			UART multi-byte transmission start bit (LTRC.RTS)	③LTRC.RTS is set to '1'	①LCUC.OMO is cleard to '0'(SW reset is active) ②Ssuccessful completion of Frame (TX)
		Status	UART Transmission Status (LST.UTS)	②Writing UTDR ②Writing UWTDR ②LTRC.RTS is set to '1'	①LCUC.OMO is cleard to '0'(SW reset is active) ①Negate of UTOE ③Detection of StopBit(End of Bit) (Without next transmission data)
			Frame Transmission complete flag (LST.FTC)	②End of StopBit(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ③LST.FTC is cleard to '0'
		Error Status	LIN Bit Error flag (LEST.BER)	②End of StopBit(End of Bit)	①LCUC.OMO is cleard to '0'(SW reset is active) ③LEST.BER is cleard to '0'
	Rx	Operation Control	UART Reception Operation Enable Bit (LUOER.UROE)	②LUOER.UROE is set to '1'	①LCUC.OMO is cleard to '0'(SW reset is active) ②LUOER.UROE is cleard to '0'
		Status	UART Reception Status (LST.URS)	②Detection of StartBit(Sample point)	①LCUC.OMO is cleard to '0'(SW reset is active) ①Negate of UROE ①Detection of StopBit(Sample point)
			UART ID Match Flag (LEST.IDMT)	②Detection of StopBit(Sample point)	①LCUC.OMO is cleard to '0'(SW reset is active) ③LEST.IDMT is cleard to '0'
			UART Expansion Bit Detection Flag (LEST.EXBT)	②Detection of StopBit(Sample point)	①LCUC.OMO is cleard to '0'(SW reset is active) ③LEST.EXBT is cleard to '0'
		Error Status	UART Parity Error flag (LEST.UPER)	②Detection of StopBit(Sample point)	①LCUC.OMO is cleard to '0'(SW reset is active) ③LEST.UPER is cleard to '0'
			LIN Framing Error flag (LEST.FER)	②Detection of StopBit(Sample point)	①LCUC.OMO is cleard to '0'(SW reset is active) ③LEST.FER is cleard to '0'
			UART Overrun Error Flag (LEST.OER)	③Detection of StopBit(Sample point)	①LCUC.OMO is cleard to '0'(SW reset is active) ②Read of LURDR.URD ④LEST.OER is cleard to '0'
Extended UART	Tx / Rx	Status	UART Loop-back Delayed data Consistency Error flag (LEST.LDCER)	②Detection of StopBit(Sample point)	①LCUC.OMO is cleard to '0'(SW reset is active) ③LEST.LDCER is cleard to '0'
				②None detection of StartBit(End of a reception window)	①LCUC.OMO is cleard to '0'(SW reset is active) ③LEST.LDCER is cleard to '0'

Note 1: Number is priority.

7.9 ERROR STATUS

7.9.1 Kinds of Error Status

The table below shows the error status controlled by the RLIN3 module and the description of conditions for setting and clearing of these bits in various modes.
These errors are indicated in the Error Status Register.

O: detection enable/disable possible
X: detection always enabled

Table 7-13: Error status bits description

Kind	For setting to "1" (Clearing to "0" is done by the software)	Detection Possible	Communication operation	Selection of detection on/off
Bit Error	Sets when Bit Error is detected. (Tx pin signal level does not match the sampled Rx pin signal level)	LIN, UART	Abort (for LIN mode only)	O
Physical Bus Error	Sets in following cases 1. When bus is detected high during transmission of break low field. 2. When bus is detected low during transmission of break delimiter field. 3. When bus is detected high during transmission of a WUP.	LIN Master	Abort	O
Response Preparation Error	LIN Master mode and Frame Separate Mode: Sets after Header transmission is completed or previous data group is completed in data group communication, and then 1st byte of response is received before Response Reception of the data group start bit is set. LIN Slave mode: Sets after Header reception is completed or previous data group is completed in data group communication, and then 1st byte of response is received before Response Transmission and Reception, Response Reception of the data group or Response Transmission of the only 1st data group start bit is set.	LIN Normal	Abort	X
Timeout Error	Sets when the Time-out count reaches the timeout value. Timeout error can be selected for Frame Timeout or Response Timeout detection.	LIN Normal	Abort	O
Framing Error	Sets when in reception the Stop Bit is received Low.	LIN Normal	Abort	O
Framing Error	Sets when in reception the 1st Stop Bit is received Low regardless of the setting value LBFC.USBLS.	UART	- (already completed at the time of setting)	O

Kind	For setting to "1" (Clearing to "0" is done by the software)	Detection Possible	Communication operation	Selection of detection on/off
SYNC field Error	Sets in the following cases • Break Low width is more than or equal configured Break Low width • SYNC field is not "55h"	LIN Slave Normal	Abort (wait for next Break Low detection)	O (only setting of the flag can be enabled or disabled.)
Checksum Error	Sets when received Checksum does not match with the calculated Checksum in the RLIN module.	LIN Normal	− (already completed at the time of setting)	X
LIN ID parity error	Sets when received LIN ID parity bits (IDP0 or IDP1) do not match the automatically calculated value in the RLIN3 module	LIN Slave Normal	Abort	O
UART Loop-back delayed data consistency error	Sets when the transmitted data and loop-back delayed data are not equal	Extended UART mode	Communication completed	O
Overrun Error Flag[#1]	Sets when next receive operation is completed before data is read from the UART 7bit/8bit/9bit receive register	UART	− (already completed at the time of setting, but data is not stored)	O
Expansion Bit detection	Sets when expansion bit is enabled and level of detected Expansion bit matches the level of the expansion bit detection level select bit	UART	Not Applicable	O
ID match	Sets in the following cases ・Expansion bit is enabled ・Expansion bit comparison is enabled ・Expansion bit data comparison is enabled ・Level of detected Expansion bit matches the level of the expansion bit detection level select bit ・Received 8bit data (excluding expansion bit) matches the ID register value	UART	Not Applicable	O
Parity Error	Sets when Parity error is detected on Reception.	UART	− (Abort operation is not executed)	O

#1: In LIN mode an overrun error does not exist because users can control the start timing of every response reception by setting the reception request after reading the data from the data buffers.

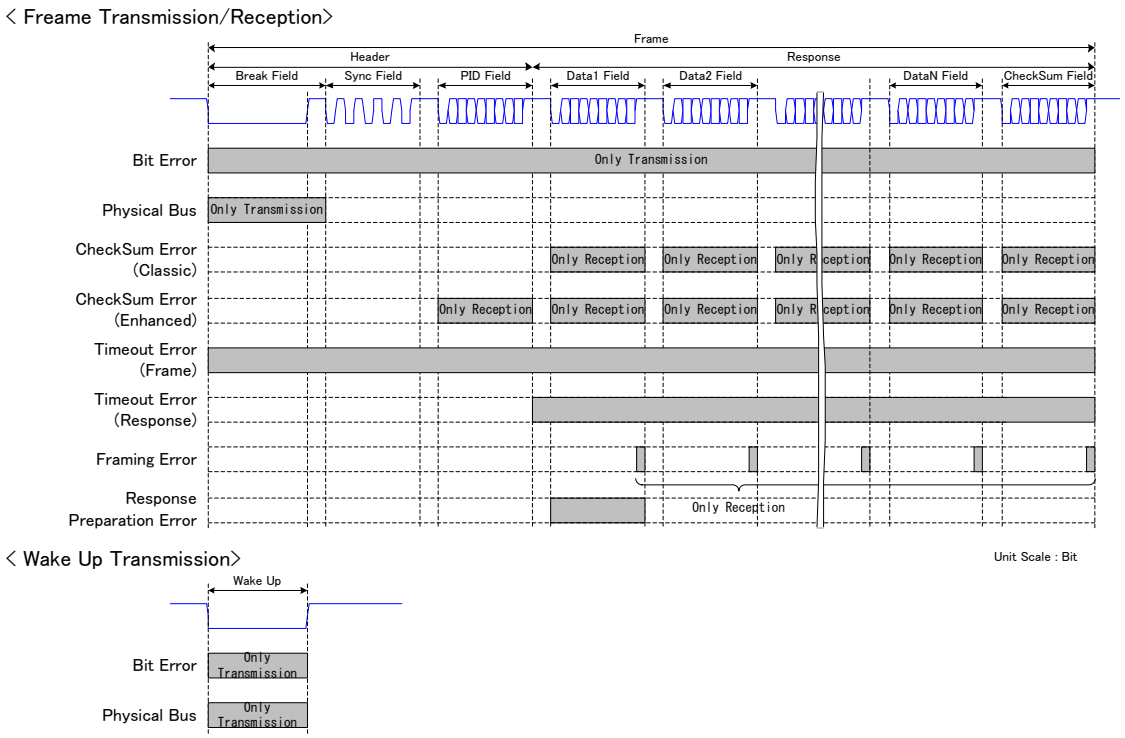


Figure 7-21: Error detection area in LIN Master mode

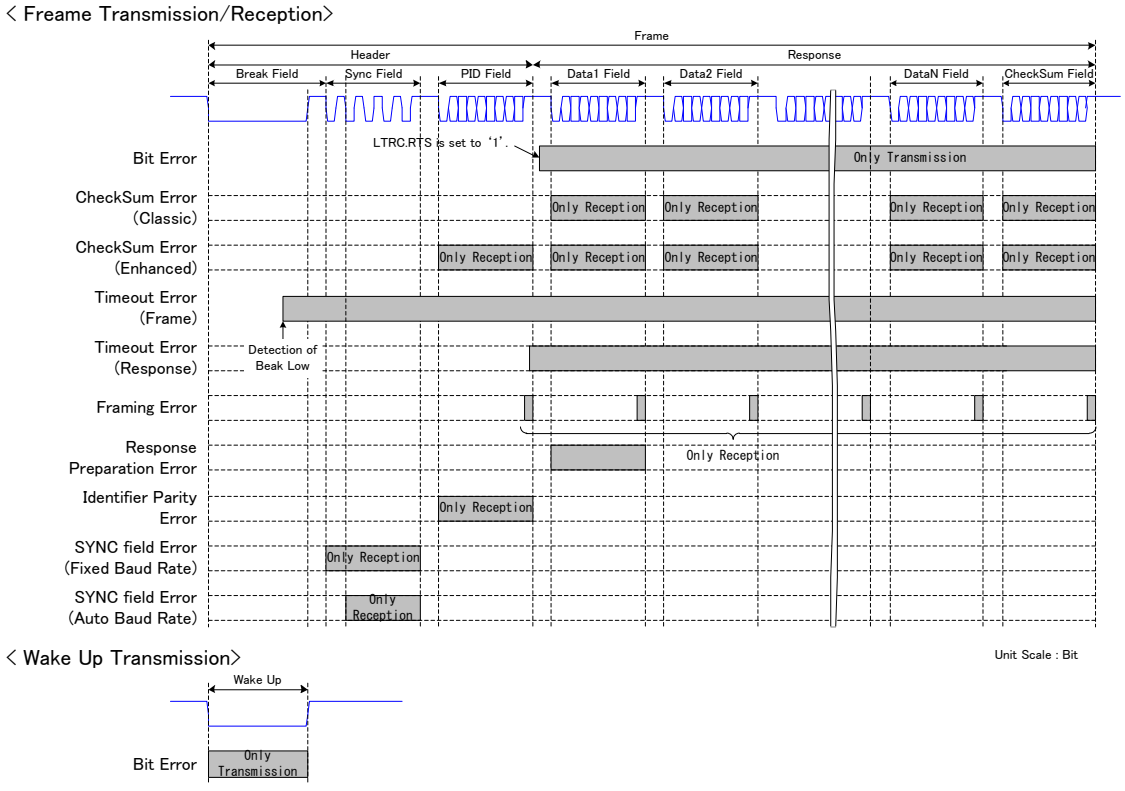


Figure 7-22: Error detection area in LIN Slave mode

7.9.2 Conflicts of Error Status

The table below shows the condition of error status bits that occurs at the end of single frame in LIN Master Mode.
The combination not listed in the table, condition does not occur.

1: set error
0: no error

Table 7-14: Conflicts of Error Status (LIN Master Mode)

Number of Conflict	Kinds of Errors					
	BER	PBER	TER	FER	CSER	RPER
1	1	0	0	0	0	0
	0	1	0	0	0	0
	0	0	1	0	0	0
	0	0	0	1	0	0
	0	0	0	0	1	0
	0	0	0	0	0	1
2	1	1	0	0	0	0
	1	1	1	0	0	0
	0	0	1	1	0	0
	0	0	1	0	1	0
	0	0	1	0	0	1
	0	0	0	1	1	0
	0	0	0	1	0	1
	0	0	0	0	1	1
3	0	0	1	1	1	0
	0	0	1	1	0	1
	0	0	1	0	1	1
	0	0	0	1	1	1
4	0	0	1	1	1	1
5	-	-	-	-	-	-
6						

The table below shows the condition of error status bits that occurs at the end of single frame in LIN Slave Mode.
The combination not listed in the table, condition does not occur.

1: set error
0: no error

Table 7-15: Conflicts of Error Status (LIN Slave Mode)

Number of Conflict	Kinds of Errors						
	BER	TER	FER	SFER	CSER	IPER	RPER
1	1	0	0	0	0	0	0
	0	1	0	0	0	0	0
	0	0	1	0	0	0	0
	0	0	0	1	0	0	0
	0	0	0	0	1	0	0
	0	0	0	0	0	1	0
	0	0	0	0	0	0	1
2	1	1	0	0	0	0	0
	0	1	1	0	0	0	0
	0	1	0	1	0	0	0
	0	1	0	0	1	0	0
	0	1	0	0	0	1	0
	0	1	0	0	0	0	1
	0	0	1	0	1	0	0
	0	0	1	0	0	1	0
	0	0	1	0	0	0	1
	0	0	0	0	1	0	1
3	0	1	1	0	1	0	0
	0	1	1	0	0	1	0
	0	1	1	0	0	0	1
	0	1	0	0	1	0	1
	0	0	1	0	1	0	1
4	0	1	1	0	1	0	1
5	-	-	-	-	-	-	-
6	-	-	-	-	-	-	-
7	-	-	-	-	-	-	-

Designers information:
In the case of TER and other error flags become "1" conflict:
In the case of a sample clock and communication clock are same frequency, Other error flags become "1".
In the case of others, Other error flags become "0".

The table below shows the condition of error status bits that occurs at the end of single frame in UART Mode.
The combination not listed in the table, condition does not occur.

1: set error
0: no error

Table 7-16: Conflicts of Error Status (UART Mode)

Number of Conflict	Kinds of Errors					
	BER/LDCER	OER	FER	EXBT	IDMT	UPER
1	1	0	0	0	0	0
	0	1	0	0	0	0
	0	0	1	0	0	0
	0	0	0	1	0	0
	0	0	0	0	0	1
2	1	1	0	0	0	0
	1	0	1	0	0	0
	1	0	0	1	0	0
	1	0	0	0	0	1
	0	1	1	0	0	0
	0	1	0	1	0	0
	0	1	0	0	0	1
	0	0	1	0	0	1
	0	0	0	1	1	0
3	1	1	1	0	0	0
	1	1	0	1	0	0
	1	1	0	0	0	1
	1	0	1	0	0	1
	1	0	0	1	1	0
	0	1	1	0	0	1
	0	1	0	1	1	0
4	1	1	0	1	1	0
	1	1	1	0	0	1
5	-	-	-	-	-	-
6	-	-	-		-	-

7.10 SPECIFICATION FOR TIMEOUT ERROR

RLIN3 supports detection of Frame Timeout error or Response Timeout error for LIN Master mode or LIN slave mode operation based on the configuration chosen by the SW drivers.
SW drivers can enable or disable the timeout error detection function.

7.10.1 Frame Timeout Error

This function checks the length of the frame on the LIN bus. If the length exceeds the specified value then it is judged as an error, and the frame is aborted.

If a LIN frame does not finish within ((49 or 48) + 14 * (communication byte count + 1)) Tbits, this is judged as an error. Here, "communication byte count" denotes the specified value for the communication data length in the SFR. The value 49 is selected for Classic Checksum and the value 48 is chosen for Enhanced Checksum.

7.10.1.1 LIN Master mode

A LIN Master node always transmits the Header and hence the Frame timeout count starts at the same time as Header Transmission Start (Break Low Start).

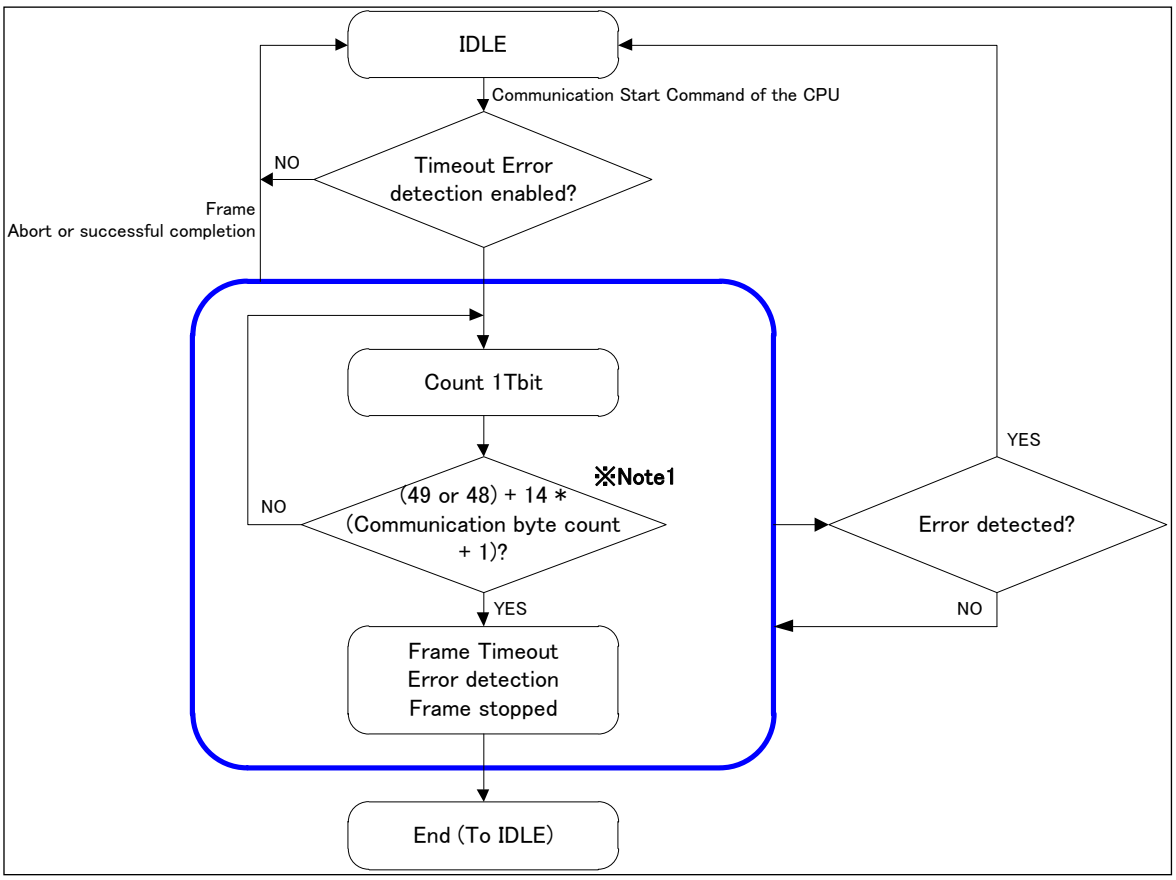


Figure 7-23: Frame TimeOut Error detection in LIN Master mode

Note 1: If LIN Classic Checksum is selected then value 49 is selected. If LIN Enhanced Checksum is selected then value 48 is selected.

7.10.1.2 LIN Slave mode

A LIN slave mode, always needs to detect the header and hence the Timeout error measurement needs to start when the falling-edge detection of Break-Low signal.
Additionally, the "communication byte count" value is update by Register bus access after the end of ID reception (when Response communication is enabled) and hence the Frame Timeout error period is calculated again when the Byte count value is updated and Response TX / RX is enabled.

Note: Timeout error detection is not supported for Auto Baud rate LIN Slave mode.

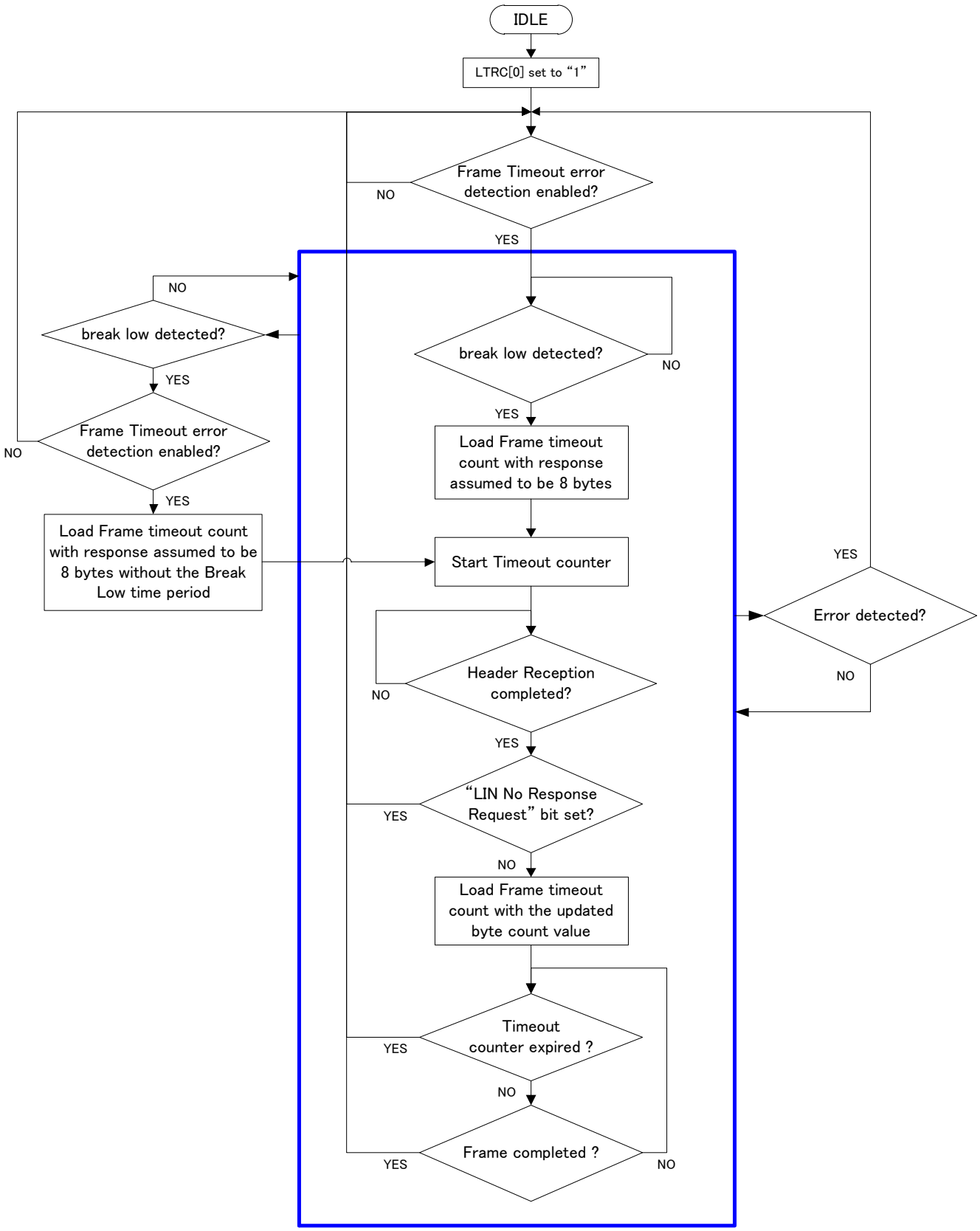


Figure 7-24: Frame TimeOut Error detection in LIN Slave mode

If the response is not enabled (LIN No Response Request bit is set by users), timeout counter will be stopped and hence Frame timeout error will not be flagged. Also, in case of response preparation error or Framing error or Bit error or Sync field error or ID Parity error detection, Frame timeout counter will be stopped since Frame is aborted for these errors.

The Frame timeout counter starts with the detection of Break low in IDLE mode or detection of Break Low during Frame communication. The value of Timeout period is based on the value defined in the LIN protocol specification documents. It covers all the fields of the LIN Frame including Break Low, Break Delimiter, response Space up to the end of the Checksum field.

Once the timeout counter starts, it will stop only when one of the following options occurs:

- Timeout counter expires and timeout error condition is met.
- Frame is aborted due to detection of error
- Frame is completed due to end of communication.
- Frame is ignored after Header reception due to setting of LTRC.LNRR bit (no response) in LIN Slave mode.

7.10.2 Response Timeout Error

This function checks if the response duration exceeds the "timeout" value based on the configuration. The error flag is set if the duration exceeds the timeout value.
If a LIN response does not finish within (14 * (communication byte count + 1)) Tbits, this is judged as an error. Here, "communication byte count" denotes the specified value for the communication data length in the SFR.

The Response timeout counter starts at the Header transmission/reception end.
If RLIN3 module is configured to LIN Slave mode, the Response timeout counter starts as "communication byte count" is 8bytes.

Additionally, the "communication byte count" value is update when Response communication is enabled by users and hence the Response timeout error period is calculated again.

If the response is not enabled (LIN No Response Request bit is set by users), Response timeout counter will be stopped.

Also, in case of response preparation error or Framing error or Bit error detection, Response timeout counter will be stopped since Response is aborted for these errors.

Note: Timeout error detection is not supported for Auto Baud rate LIN Slave mode.

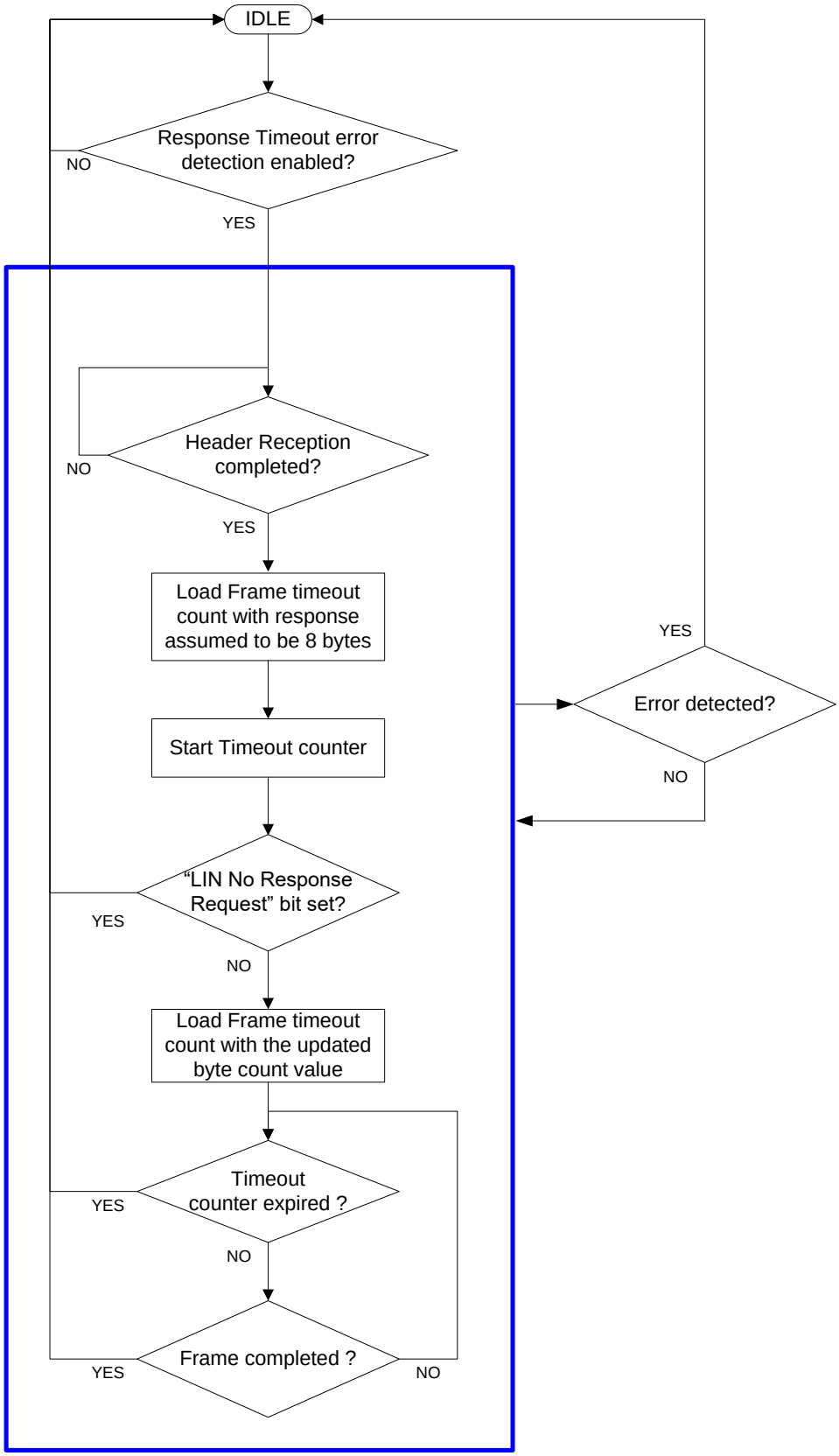


Figure 7-25: Response TimeOut Error detection in LIN Master or Slave mode

7.11 WAKE-UP

7.11.1 Selection of Baud Rate

The RLIN3 module can transmit wakeup at different baud rate than normal mode communication. This can be done with "Wake-up baud rate select mode bit". The clock change in Wake-up mode is independent of the baud rate source clock select bits configuration in the LMD register.

If the Wake-up baud rate select mode bit is "1", then the baud rate clock selection in Wake-up mode is switched to "fa" automatically even if the System clock configuration in wake-up mode is not "fa".

This setting can be used if LIN Wake-up signal is based on LIN protocol specification version 2.X.
For Wake-up reception, the LIN node is expected to detect a LOW signal on the bus for 150 µs.
This period is approximately 2.5 "LOW" bits when baud rate is 19.2 Kbits/s.

For Wake-up transmission, the LIN node is expected to transmit a "LOW" signal on the bus for 250 µs. This period is approximately 5 LOW bits when the baud rate is 19.2 Kbits/s.

The system clock source "fa" has the fastest clock frequency for baud rate generation using the register LBRP0. Usually, "fa" is expected to generate baud rate of 19.2 Kbits/s, "fb" is expected to generate baud rate of 9.6 Kbits/s and "fc" is expected to generate baud rate of 2.4 Kbits/s

Hence, by automatically selecting "fa" and configuring LBRP0 such that "fa" generates baud rate of 19.2 Kbits/s, the RLIN3 module saves significant SW interactions needed to re-configure the baud rate settings required in Wake-up mode.

This setting should not be used for LIN wake-up signal based on LIN protocol specification ver 1.3 and it should also not be used for slave mode or UART mode operation.

7.11.2 Transmission

In Wake-up state, IP will transmit wakeup signal if "LIN Communication start bit" is set and "LIN Response Communication Direction Select bit" is configured for Transmission. The format of the Wake-up signal complies with the configuration in the SFR's Wake-up Low Transmission Length. A Successful Transmission Interrupt is output when Low level of the Wake-up is output for the programmed length of time without an Error. The Wakeup transmission is aborted when error is detected & appropriate error status flags are set. Users are able to execute Wakeup Transmission in LIN mode. Then, users should configure the LBRP0 and LBRP1.

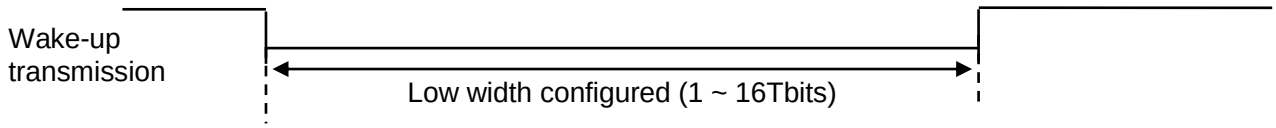


Figure 7-26: Wakeup Transmission

For wakeup retransmission in LIN slave mode, refer to Section 8.4.

7.11.3 Reception

In Wake-up state IP will detect (receive) wakeup signal when "Communication bit" is set & direction bit is configured for Reception. The IP will set successful wakeup reception flag if 2.5 consecutive dominant bits are detected on the RXD input pin.
Users are able to execute Wakeup Transmission in LIN mode. Then, users should configure the LBRP0 and LBRP1.

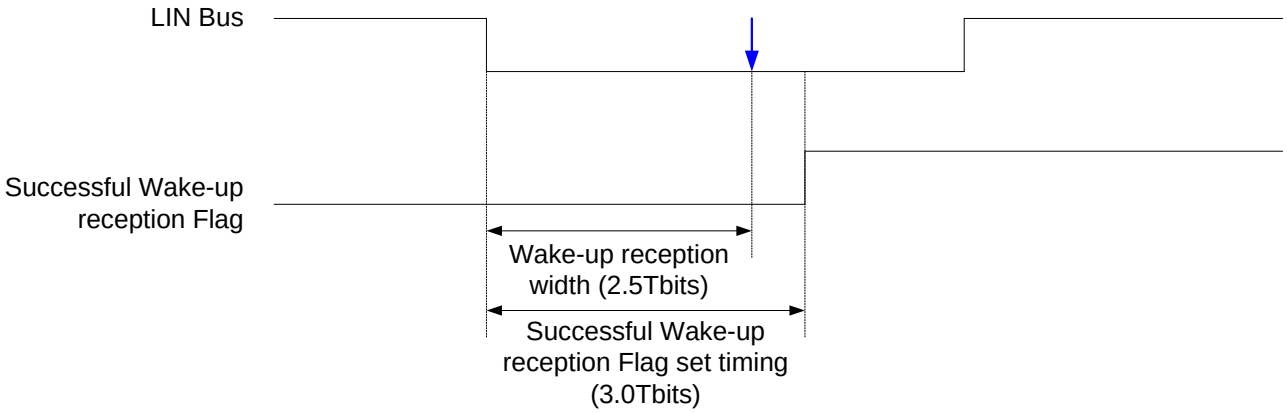


Figure 7-27: Wakeup Reception

7.12 SUPERVISOR MODE OPERATION

This is a special mode to check the status of the RLIN3 module. If this mode is enabled (a high level detected on the SVSTOP input pin) then the communication will be stopped by the RLIN3 module.
In this mode, for registers that HW protection, can not write.

The following actions occur in this mode:

1. The internal baud rate clock is stopped and hence the operation of the LIN Controller logic is stopped.
2. All communication stops in the 2 clock cycles of peripheral clock.
3. The Registers can be accessed as normal and values can be read and written into various registers as defined in the SFR section. Configuration and control register values can be updated and flags can be cleared.
4. In order to leave the supervisor mode SVSTOP pin shall be driven with "low" level and then the users should apply the SW reset before starting any communication process.

7.13 RECEIVED DATA READ EMULATION (NOT OPEN TO CUSTOMERS)

The data in the UART 7bit/8bit/9bit receive data register can be read in the UART 7bit/8bit/9bit receive data register for emulation.
A read access of the UART 7bit/8bit/9bit receive data register for emulation is not treated as a read access of the UART 7bit/8bit/9bit receive data register and hence overrun error can occur if new data is received and the data from UART 7bit/8bit/9bit receive data register is not read by the Register bus access.

This register reads the value of a LURDR register. The data in the UART 7bit/8bit/9bit receive data register flip-flops can be also be read at the address location specified for the UART 7bit/8bit/9bit receive data register for emulation.

7.14 SELF TEST MODE

RLIN module offers self-test mode, which could be only used when IP is in LIN mode. Following are the key points related to Self Test mode.

1. IP in LIN Normal mode.
2. No Wakeup function supported.
3. Frame separate mode is not supported.
4. LIN Response data group communication is not supported.
5. LIN Slave Auto Baud Rate mode is not supported.
6. BRG will be bypassed thus BRP0 & BRP1 register value, LWBR.LPRS bits and LMD.LCKS bits have no influence.
7. CPU is not allowed to access any register (except LCUC.OM0) when communication bit is set.

Once the IP is in self-test mode, the Internal Tx is looped back to Internal Rx. Following figure explains this concept.

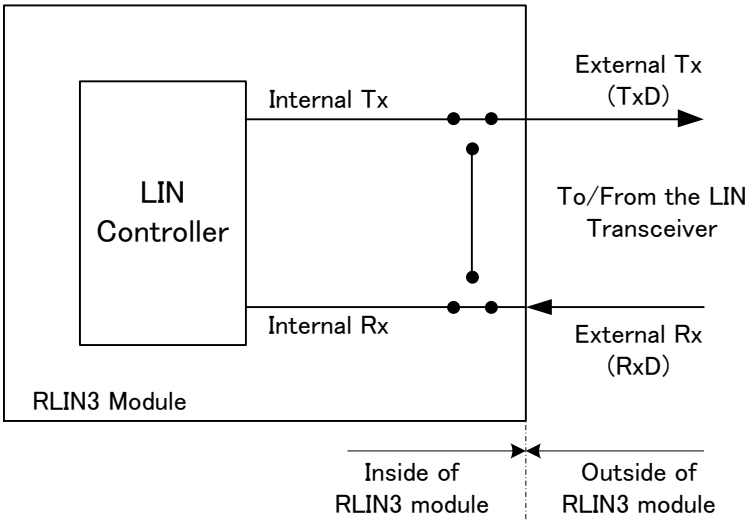


Figure 7-28: Normal Mode connection

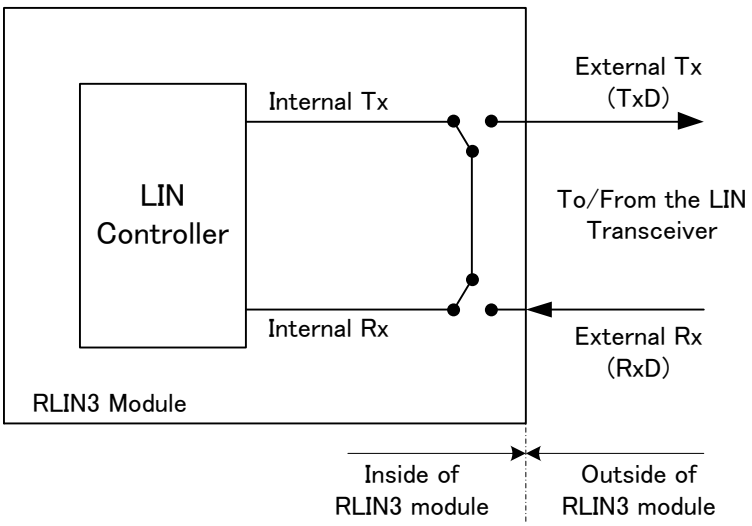


Figure 7-29: Self-Test Mode connection

Since self-test mode is a special mode during which RLIN module will not be able to drive the LIN bus, there is a special key sequence to be followed in Reset state to enter this mode.

Note: Timeout Error detection is not supported in Self Test mode.

7.14.1 Entry into Self test mode

To enter the self-test mode a particular Self-test mode key sequence shall be used. In this key sequence users have to do three consecutive writes to Self-test Mode register as follows.

1. Enter Reset Mode
2. Select LIN mode operation
3. 1st write: LIN Self test Control Register [7:0] = "1010 0111" (0xA7)
4. 2nd write: LIN Self test Control Register [7:0] = "0101 1000" (0x58)
5. 3rd write: LIN Self test Control Register [7:0] = "0000 0001" (0x01)

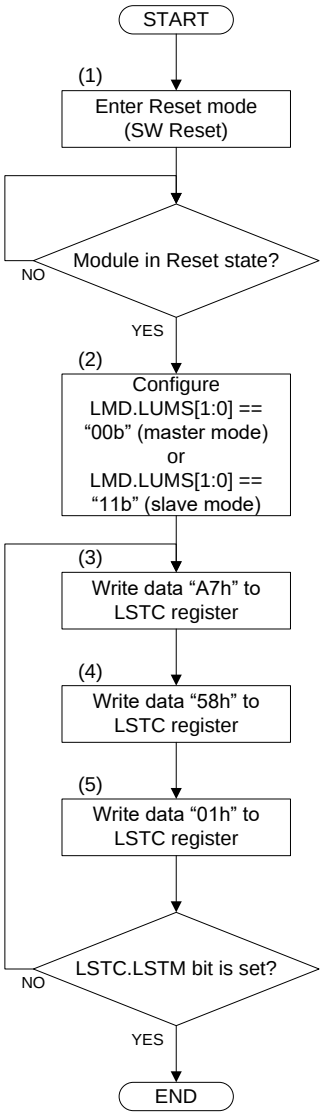


Figure 7-30: Flow diagram for Self-test Mode Entry using Self-test Mode key sequence logic

The advantage of the Self-test Mode key sequence is that software has to use a specific sequence of write accesses to the self-test Mode key register to allow the RLIN3 module to enter Self-test Mode. This will reduce any chances of an accidental entry into self-test mode. If the 1st key is written twice, then the sequence is broken and shall be restarted. Hence, users have to write 1st key again followed by the 2nd key and then the 3rd value to enter test mode.

If this sequence is broken by a write access to any other SFR locations of the RLIN module, then the sequence shall be restarted.

Self-test mode does not support Frame Separate Mode in LIN Master mode or automatic baud rate detection in LIN slave mode.
4 tests can be carried out.

1. LIN Master Self Test mode – Transmission : Header Transmission & Response Transmission
2. LIN Master Self Test mode – Reception : Header Transmission & Response Reception
3. LIN Slave Self Test mode – Transmission : Header Reception & Response Transmission
4. LIN Slave Self Test mode – Reception : Header Reception & Response Reception

7.14.2 LIN Master Self Test mode – Transmission

Following steps are the configuration example for the LIN Master transmission after the entry into Self test mode.

1. Set prescaler, baud rate, number of samples per bit and LMD.LCKS. The setting value of prescaler, baud rate and LMD.LCKS do not influence operation. Therefore, the writing to these bits is not necessary.
2. Set interrupt enable bits and error detection enable bits.
3. Set LIN break field and LIN space bits. LSC.IBS and LSC.IBHS of LIN space configuration bits influence operation.
4. Enter idle state. Wake-up mode is not supported in Self test mode.
5. Set LIN Identifier buffer, data buffers and LIN data field configuration bits. Frame separate mode and data group communication are not supported in Self test mode.
6. Is module in idle state?
7. Start frame transmission.

Self test mode is executed. Interrupt generation and update of status bits is appropriately executed. If transmission is successful, the loopback data can be read from data buffer, ID buffer and checksum buffer in inverted format. LTRC.FTS is cleared by transmission completion. If transmission is unsuccessful due to error(s) then appropriate error status flag will be set.

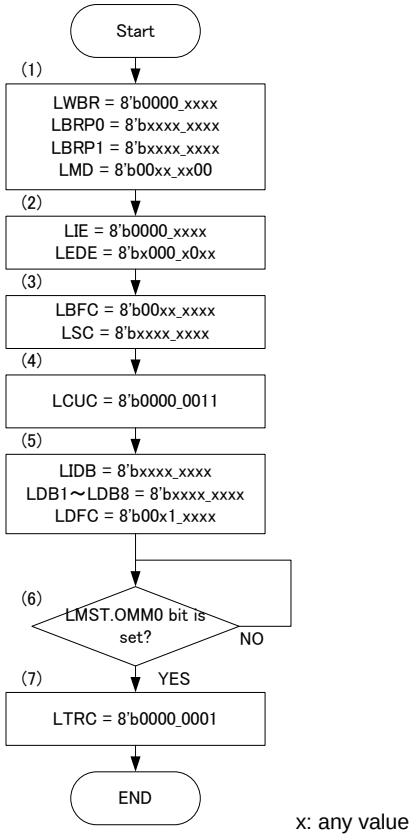


Figure 7-31: Flow diagram for Example of the Configuration after Self-test Mode Entry (Transmission)

Note1: Users are not able to detect LIN Successful Response Interrupt, when LIN Header Transmission flag (LST.HTRC) is not cleared until LIN Successful Response Interrupt is detected.
LIN Successful Header Interrupt Enable (LIE.SHIE) should not be set to "1", when LIN Successful Header Interrupt software routine takes more time than setting of the LIN Successful Response Interrupt after the setting LIN Successful Header Interrupt.

The Following is LIN Successful Response from the setting LIN Successful Header Interrupt.
10 * (LDFC.RFDL + 1) [Bit]
1Bit width is the period of the LIN communication clock (clk_lin) * 16.

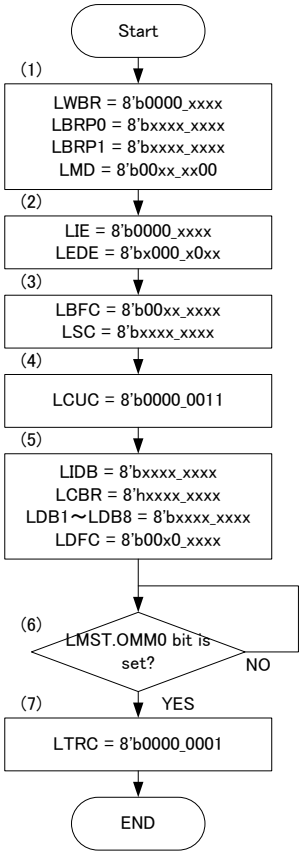
7.14.3 LIN Master Self Test mode – Reception

Following steps are the configuration example for the LIN Master reception after the entry into Self test mode.

1. Set prescaler, baud rate, number of samples per bit and LMD.LCKS. The setting value of prescaler, baud rate and LMD.LCKS do not influence operation. Therefore, the writing to these bits is not necessary.
2. Set interrupt enable bits and error detection enable bits.
3. Set LIN break field and LIN space bits. LSC.IBHS of LIN space configuration bits influence operation. LSC.IBS of LIN space configuration bits do not influence operation.
4. Enter idle state. Wake-up mode is not supported in Self test mode.
5. Set LIN Identifier buffer, data buffers, LIN Checksum buffer and LIN data field configuration bits. LIN Checksum Buffer bits can be set only in Self test mode. Frame separate mode and data group communication are not supported in Self test mode.
6. Is module in idle state?
7. Start frame communication.

Self test mode is executed. Interrupt generation and update to status bits is appropriately executed. If reception is successful, the loopback data can be read from the data buffer, ID buffer and the checksum from the checksum buffer in inverted format. LTRC.FTS is cleared by reception completion. If reception is unsuccessful due to error(s) then appropriate error status flag will be set.

Note1: The checksum value in transmission frame is not calculated automatically.
Therefore, users should set calculated value to LCBR.CKSM register.
RLIN3 module can test the checksum error by which users set the wrong checksum value to LCBR.CKSM.



x: any value

Figure 7-32: Flow diagram for Example of the Configuration after Self-test Mode Entry (Reception)

Note1: Users are not able to detect LIN Successful Response Interrupt, when LIN Header Transmission flag (LST.HTRC) is not cleared until LIN Successful Response Interrupt is detected.
LIN Successful Header Interrupt Enable (LIE.SHIE) should not be set to "1", when LIN Successful Header Interrupt software routine takes more time than setting of the LIN Successful Response Interrupt after the setting LIN Successful Header Interrupt.

The Following is LIN Successful Response from the setting LIN Successful Header Interrupt.
10 * (LDFC.RFDL + 1) [Bit]
1Bit width is the period of the LIN communication clock (clk_lin) * 16.

7.14.4 LIN Slave Self Test mode – Transmission

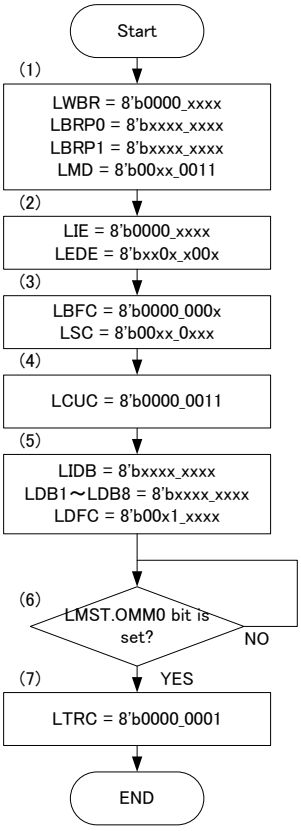
Following steps are the configuration example for the LIN Slave transmission after the entry into Self test mode.

1. Set prescaler, baud rate, number of samples per bit and LMD.LCKS. The setting value of prescaler, baud rate and LMD.LCKS do not influence operation. Therefore, the writing to these bits is not necessary.
2. Set interrupt enable bits and error detection enable bits.
3. Set LIN break field and LIN space bits. LSC.IBS of LIN space configuration bits influence operation. Users should set 3'b001 to LSC.IBHS in LIN Slave Self test mode.
4. Enter idle state. Wake-up mode is not supported in Self test mode.
5. Set LIN Identifier buffer, data buffers and LIN data field configuration. LIN Identifier buffer bits can be set only in Self test mode.
6. Is module in idle state?
7. Start frame transmission. Response Transmission or Reception start bit (LTRC.RTS), LIN No Response Request bit (LTRC.LNRR) and data group communication are not supported in Self test mode.

Self test mode is executed. Interrupt generation and update of status bits is appropriately executed. If transmission is successful, the loopback data can be read from data buffer, ID buffer and checksum buffer in inverted format. LTRC.FTS is cleared by transmission completion. If transmission is unsuccessful due to error(s) then appropriate error status flag will be set.

Note1: In Self test mode, header reception and response transmission are executed by only setting LTRC.FTS without controlling LTRC.RTS. Furthermore, LTRC.FTS is cleared by end of a frame communication.

Note2: Break Low width is able to be configured only to 9.5Tbit or 10.5Tbit by LBFC.LBLT.



x: any value

Figure 7-33: Flow diagram for Example of the Configuration after Self-test Mode Entry (Transmission)

Note1: Users are not able to detect LIN Successful Response Interrupt, when LIN Header Reception flag (LST.HTRC) is not cleared until LIN Successful Response Interrupt is detected.
LIN Successful Header Interrupt Enable (LIE.SHIE) should not be set to "1", when LIN Successful Header Interrupt software routine takes more time than setting of the LIN Successful Response Interrupt after the setting LIN Successful Header Interrupt.

The Following is LIN Successful Response from the setting LIN Successful Header Interrupt.
10 * (LDFC.RFDL + 1) [Bit]
1Bit width is the period of the LIN communication clock (clk_lin) * 16.

7.14.5 LIN Slave Self Test mode – Reception

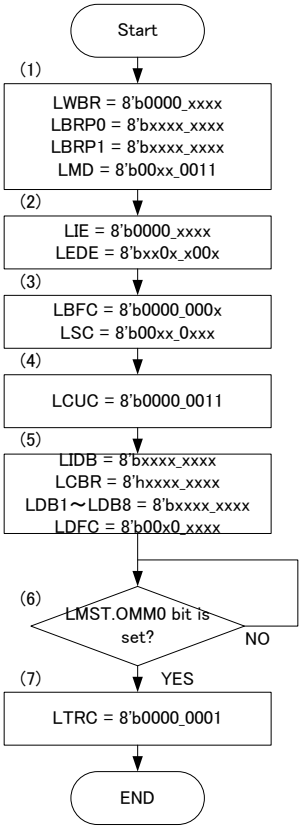
Following steps are the configuration example for the LIN Slave reception after the entry into Self test mode.

1. Set prescaler, baud rate, number of samples per bit and LMD.LCKS. The setting value of prescaler, baud rate and LMD.LCKS do not influence operation. Therefore, the writing to these bits is not necessary.
2. Set interrupt enable bits and error detection enable bits.
3. Set LIN break field and LIN space bits. LIN space configuration bits do not influence operation. Users should set 3'b001 to LSC.IBHS in LIN Slave Self test mode.
4. Enter idle state. Wake-up mode is not supported in Self test mode.
5. Set LIN Identifier buffer, LIN Checksum buffer, data buffers and LIN data field configuration bits. LIN Identifier buffer and LIN Checksum buffer can be set only in Self test mode.
6. Is module in idle state?
7. Start frame communication. Response Transmission or Reception start bit (LTRC.RTS), LIN No Response Request bit (LTRC.LNRR) and data group communication are not supported in Self test mode.

Self test mode is executed. Interrupt generation and update of status bits is appropriately executed. If reception is successful, the loopback data can be read from data buffer, ID buffer and checksum buffer in inverted format. LTRC.FTS is cleared by reception completion. If reception is unsuccessful due to error(s) then appropriate error status flag will be set.

Note1: In Self test mode, header reception and response reception are executed by only setting LTRC.FTS without controlling LTRC.RTS. Furthermore, LTRC.FTS is cleared by end of a frame communication.
Note2: Break Low width is able to be configured only to 9.5Tbit or 10.5Tbit by LBFC.LBLT.

Note3: The checksum value in transmission frame is not calculated automatically.
Therefore, users should set calculated value to LCBR.CKSM register.
RLIN3 module can test the checksum error by which users set the wrong checksum value to LCBR.CKSM.



x: any value

Figure 7-34: Flow diagram for Example of the Configuration after Self-test Mode Entry (Reception)

Note1: Users are not able to detect LIN Successful Response Interrupt, when LIN Header Reception flag (LST.HTRC) is not cleared until LIN Successful Response Interrupt is detected. LIN Successful Header Interrupt Enable (LIE.SHIE) should not be set to "1", when LIN Successful Header Interrupt software routine takes more time than setting of the LIN Successful Response Interrupt after the setting LIN Successful Header Interrupt.

The Following is LIN Successful Response from the setting LIN Successful Header Interrupt.
10 * (LDFC.RFDL + 1) [Bit]
1Bit width is the period of the LIN communication clock (clk_lin) * 16.

7.14.6 Exit from self test mode

To exit from self-test mode, users need to follow following steps:

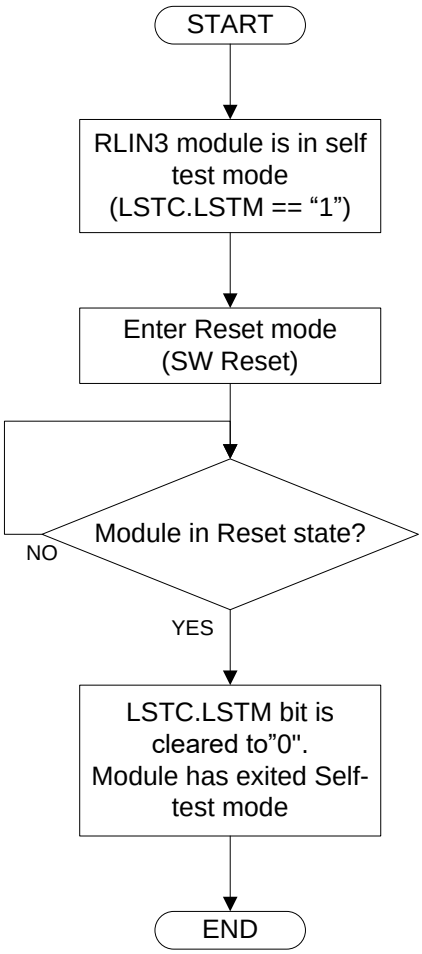


Figure 7-35: Flow diagram for Self-test Mode Exit

7.15 STATUS FLAG WRITE CONTROL MODE (NOT OPEN TO CUSTOMER)

The status flag registers LST & LEST can be written in Idle mode to check generation of interrupts. This mode is only for checking the generation of interrupts & usage in normal operation is not permitted. Bit STC[7] is used to control write operation. STC[7] can be set only through a special key sequence.
In this key sequence users have to do three consecutive writes to the Self Test Mode register as follows.

1. Enter Reset Mode
2. Select Interrupt output: Configure LIN Interrupt Enable Bits
3. Select Interrupt output: Configure LIN Interrupt Output Select Bits
4. 1st write: LIN Self test Control Register [7:0] = "1010 0111" (0xA7)
5. 2nd write: LIN Self test Control Register [7:0] = "0101 1000" (0x58)
6. 3rd write: LIN Self test Control Register [7:0] = "1000 0000" (0x80)

If the 1st key is written twice, then the sequence is broken and shall be restarted. Hence users have to write 1st key again followed by the 2nd key and then the 3rd value. If this sequence is broken by a write access at any other SFR locations of the RLIN module, then it shall be restarted.

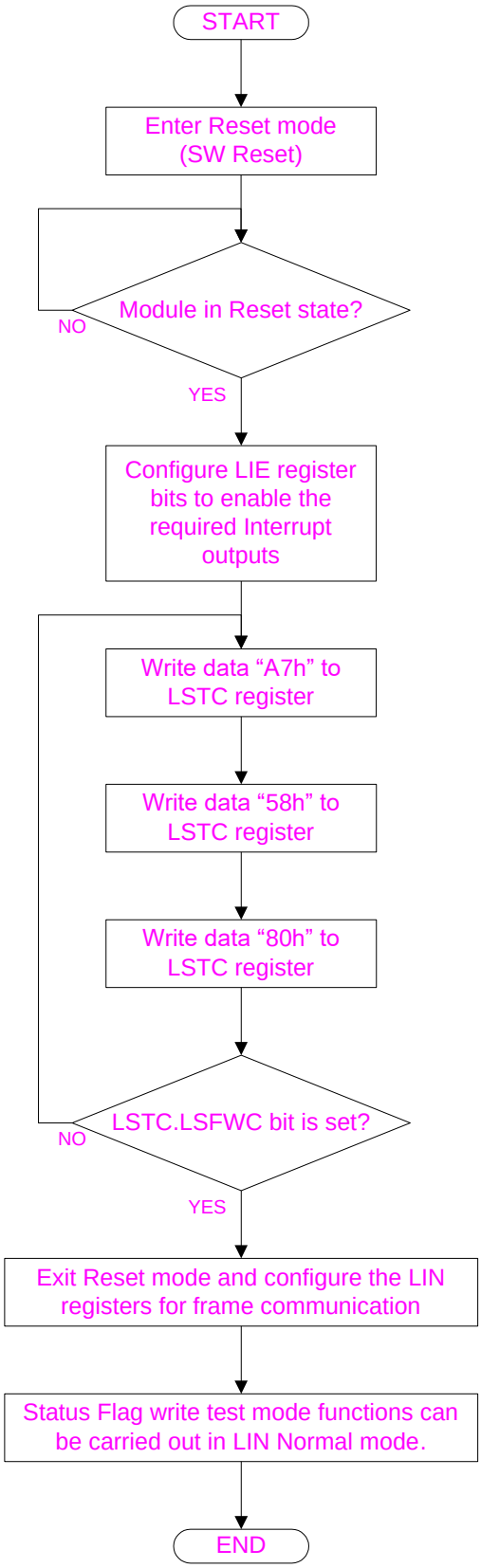


Figure 7-36: Flow diagram for status flag write control mode Entry using Self-test Mode key sequence logic

To exit from Status flag write control mode users need to follow following steps:

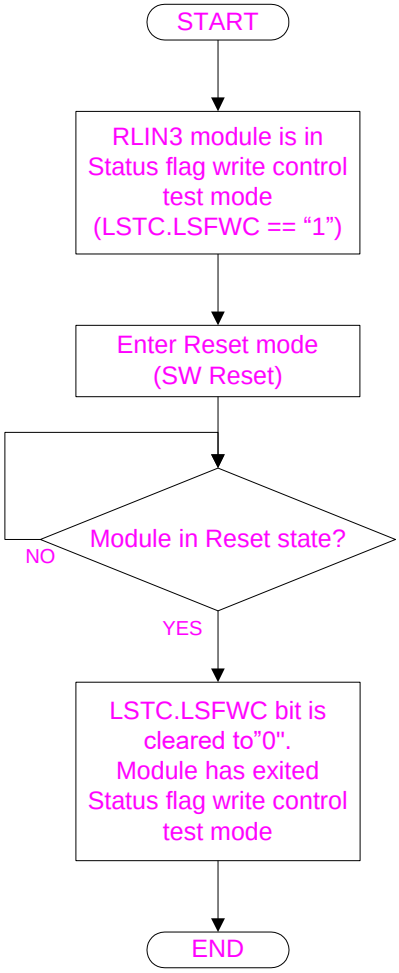


Figure 7-37: Flow diagram for Status flag write control Mode Exit

8 APPENDIX

8.1 RXD LOW LEVEL DETECTION WHEN RLIN3 MODULE IS NOT CLOCKED

Depending on the product, the RLIN3 module may not receive its clock in CPU wait mode. In such products, the RxD low-level detection can be implemented externally to the IP. Following figure shows the scheme.

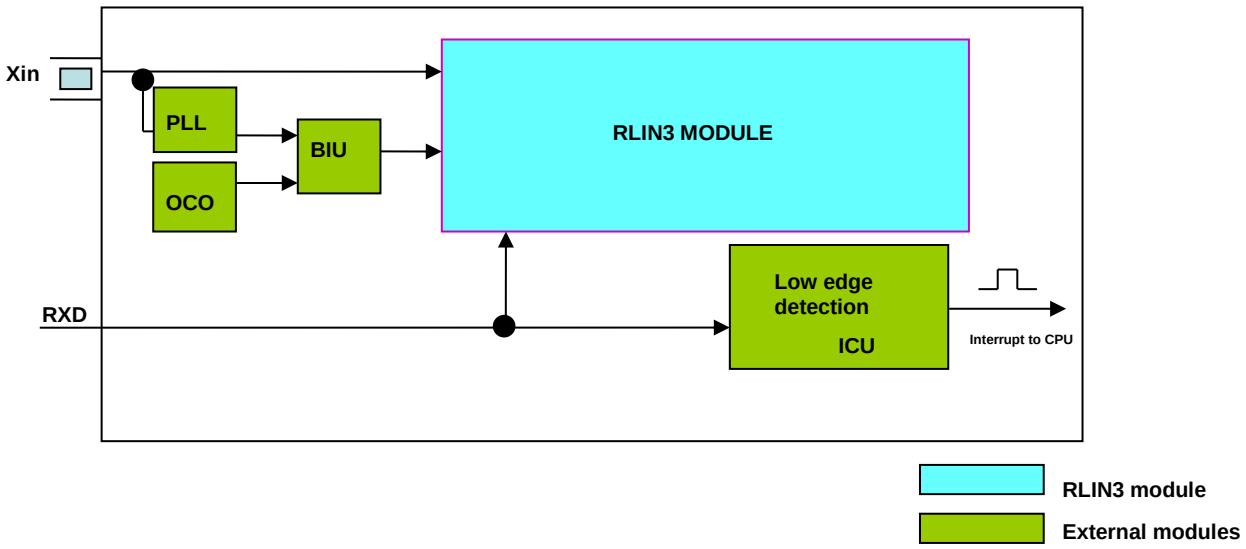


Figure 8-1 : RxD low-level detection

In such an implementation, two Wake Up pulses are required for the detection of a valid slave request:

- 1st Wake Up pulse → IrQ is generated to the CPU that needs to recover clock to the RLIN3 module
- 2nd Wake Up pulse → RLIN3 module is able to check the length and flag if this is a valid request.

This is possible as per LIN spec a slave can send up to 3 Wake Up pulses.
In products where the LIN communication clock (clk_lin) is provided to the RLIN3 module also in CPU Wait mode and it is active, Wake Up detection is performed entirely by the RLIN3 module.

8.2 RLIN3 MODULE OPERATION CONFIGURATION

8.2.1 LIN Master mode

Table 8-1: RLIN3 module configuration (LIN master mode)

Sr. No.	Operation	LDFC[7] bit	LDFC[6] bit	LTRC[0] bit	LTRC[1] bit	LDFC[4] bit	Abortion possibility
1	LIN Response Transmission	Reset	Reset	Set	Reset	Set	SW Reset
		Reset	Set	Set	Set	Set	SW Reset
2	LIN Response Reception	Reset	Reset	Set	Reset	Reset	SW Reset
3	Wake-up Transmission	Reset	Don't Care	Set	Don't Care	Set	SW Reset
4	Wake-up Reception	Reset	Don't Care	Set	Don't Care	Reset	SW Reset
5	LIN data group response transmission	Set	Set	Set	Set	Set	SW Reset
6	LIN data group response reception	Set	Set	Set	Set	Reset	SW Reset

Note 1: Changing direction from transmission to reception & vice versa is not possible in the middle of communication.

Note 2: After transmission or reception of each data group, the LTRC[1] bit is cleared. The LDFC register can then be configured to select number of bytes and also the LDFC[7] bit can be cleared for the last data group. After this LTRC[1] bit should be set again to start transmission of the next data group or enable the reception of the next data group.

8.2.2 LIN Slave mode

Table 8-2: RLIN3 module configuration (LIN slave mode)

Sr. No.	Operation	LDFC[7] bit	LTRC[0] bit	LTRC[1] bit	LTRC[2] bit	LDFC[4] bit	Abortion possibility
1	LIN Header Reception	Don't Care	Set	Don't Care	Don't Care	Don't care	SW Reset
2	LIN Response Transmission	Reset	Set	Set	Reset	Set	SW Reset
3	LIN Response Reception	Reset	Set	Set	Reset	Reset	SW Reset
4	No response	Reset	Set	Reset	Set	Don't care	SW Reset
5	Wake-up Transmission	Reset	Set	Don't Care	Don't Care	Set	SW Reset
6	Wake-up Reception	Reset	Set	Don't Care	Don't Care	Reset	SW Reset
7	LIN data group response transmission	Set	Set	Set	Don't Care	Set	SW Reset
8	LIN data group response reception	Set	Set	Set	Don't Care	Reset	SW Reset

Note 1: Changing direction from transmission to reception & vice versa is not possible in the middle of communication.

Note 2: Going from Wakeup to normal & vice versa is not possible without going to Reset mode.

Note 3: After transmission or reception of each data group, the LTRC[1] bit is cleared. The LDFC register can then be configured to select number of bytes and also the LDFC[7] bit can be cleared for the last data group. After this LTRC[1] bit should be set again to start transmission of the next data group or enable the reception of the next data group.

8.2.3 UART mode

Table 8-3: RLIN3 module configuration (UART mode)

Sr. No.	Operation	LUOER[0] bit	LUOER[1] bit	LDFC[5] bit	Trigger condition	Abortion possibility
1	UART Frame Reception	Don't care	Set	Don't care	Falling-edge on RxD pin	SW Reset or Clear LUOER[1]
2	UART Frame Transmission (single frame)	Set	Don't Care	Don't care	Write data in to LUTDR register	SW Reset or Clear LUOER[0]
3	UART Frame Transmission with guarantee of reception (single frame)	Set	Don't Care	Don't care	Write data in to LUWTDR register	SW Reset or Clear LUOER[0]
4	UART Frame Transmission (UART multi-byte transmission)	Set	Don't Care	Reset	Set LTRC[1]	SW Reset or Clear LUOER[0]
5	UART Frame Transmission with guarantee of reception (UART multi-byte transmission)	Set	Don't Care	Set	Set LTRC[1]	SW Reset or Clear LUOER[0]

8.3 RTS SETTING DURING HEADER TX OR IN RESPONSE WAIT

This section describes the behaviour of the RLIN3 module if an error (bit error or timeout) occurs in the "Wait Response" state in the frame separate response and the SW is trying to set the RTS bit at the same time.

For Example:

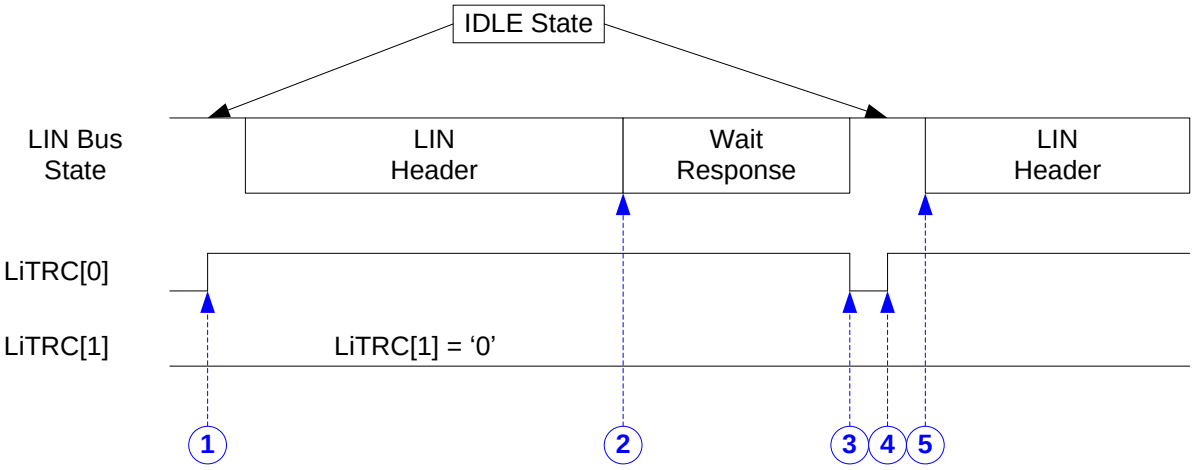


Figure 8-2 : Example of RTS setting during header TX or in response wait

1. SW Drivers configure the RLIN3 module in Frame separate mode and initiate Header Transmission by setting the LTRC[0] bits to "1".
2. Header Transmission is successful and RLIN3 module is in "Wait Response" state (waiting for SW drivers to set LTRC[1] bit for Response Transmission).
3. SW drivers try to set LTRC[1] bit. However, at the same time, error (Bit error or Timeout error) occurs in the "Wait Response" field and hence LTRC[0] bit is cleared automatically.
4. The LTRC[0] bit is set again with the "read-modify-write" access.
5. Header transmission starts due to setting of the LTRC[0] bit.

8.4 WAKE-UP PROCESSING FOR RETRANSMISSION IN LIN SLAVE MODE

The figure below illustrates flow of the wake-up processing in LIN slave mode.

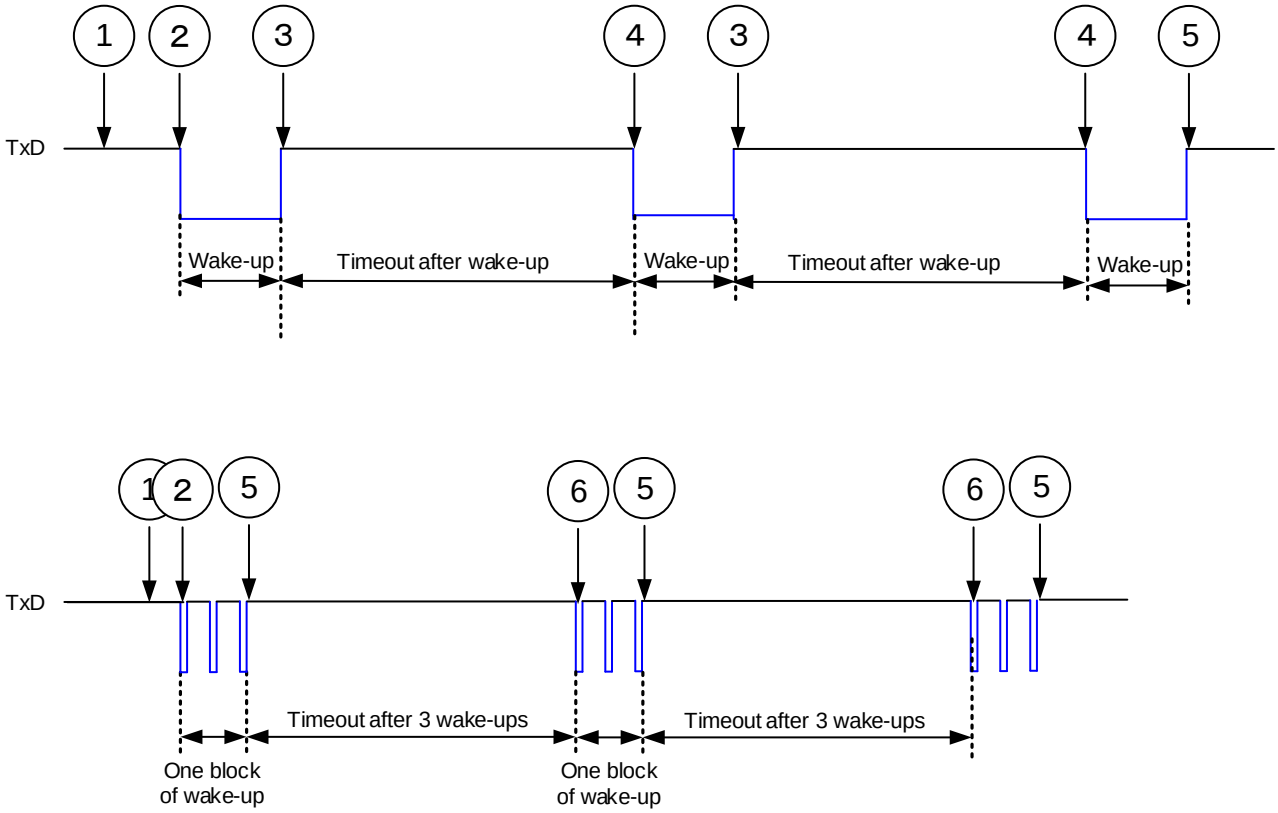


Figure 8-3 : the wake-up processing with retransmission in LIN slave mode.

1. LIN Break Field Reception flag and LIN Sync Field Reception flag are cleared by writing "0" to them.
2. Transmitting a wake-up signal.
3. Wait for wake-up signal transmission complete. When the wake-up transmission is aborted, LIN controller handles the error. When the wake-up transmission is successful, a timer for "timeout after wake-up" is started.
4. When a master node does not transmit a header (the LIN Break Field Reception flag or the LIN Sync Field Reception flag is not set) within the time specified by LIN standard, a SW driver should retransmit a wake-up signal.
5. When three wake-up transmissions are completed, a timer for "timeout after 3 wake-ups" is started.
6. When a master node does not transmit a header (the LIN Break Field Reception flag or the LIN Sync Field Reception flag is not set) within the time specified (after three wake-up signals) by LIN standard, a SW driver should retransmit a wake-up signal.

8.5 DETAIL OF RESPONSE SPACE DOMINANT DETECTION.

Flow of operation on response space dominant detection is illustrated below.
The detection period of the Response Space Dominant Detection Flag is ② to ④ in the figure below.

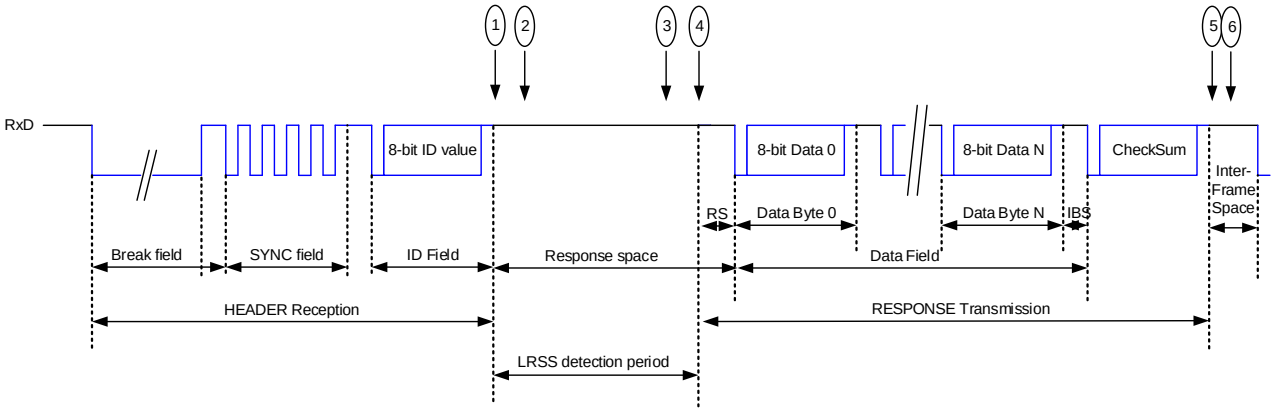


Figure 8-4 : Flow of operation of the LIN controller on response space dominant detection

1. Output LIN Header Reception flag.
2. Header Reception process completed and SW drivers should read the received ID to check if Response preparation is required.
3. Check the LIN Response Space Dominant Detection flag and set Response Transmission or Reception start bit or the LIN No Response request bit to "1".
4. When Response Transmission or Reception start bit is set and response Transmission is selected, LIN Controller transmits Response Space.
5. Output Frame Transmission complete flag. The Response Transmission or Reception start bit is cleared by HW.
6. LIN Response Transmission is completed and SW drivers should read the Response Space Dominant Detection Flag to check status of response transmission.

The figure below illustrates a flow of response transmission in LIN slave mode.

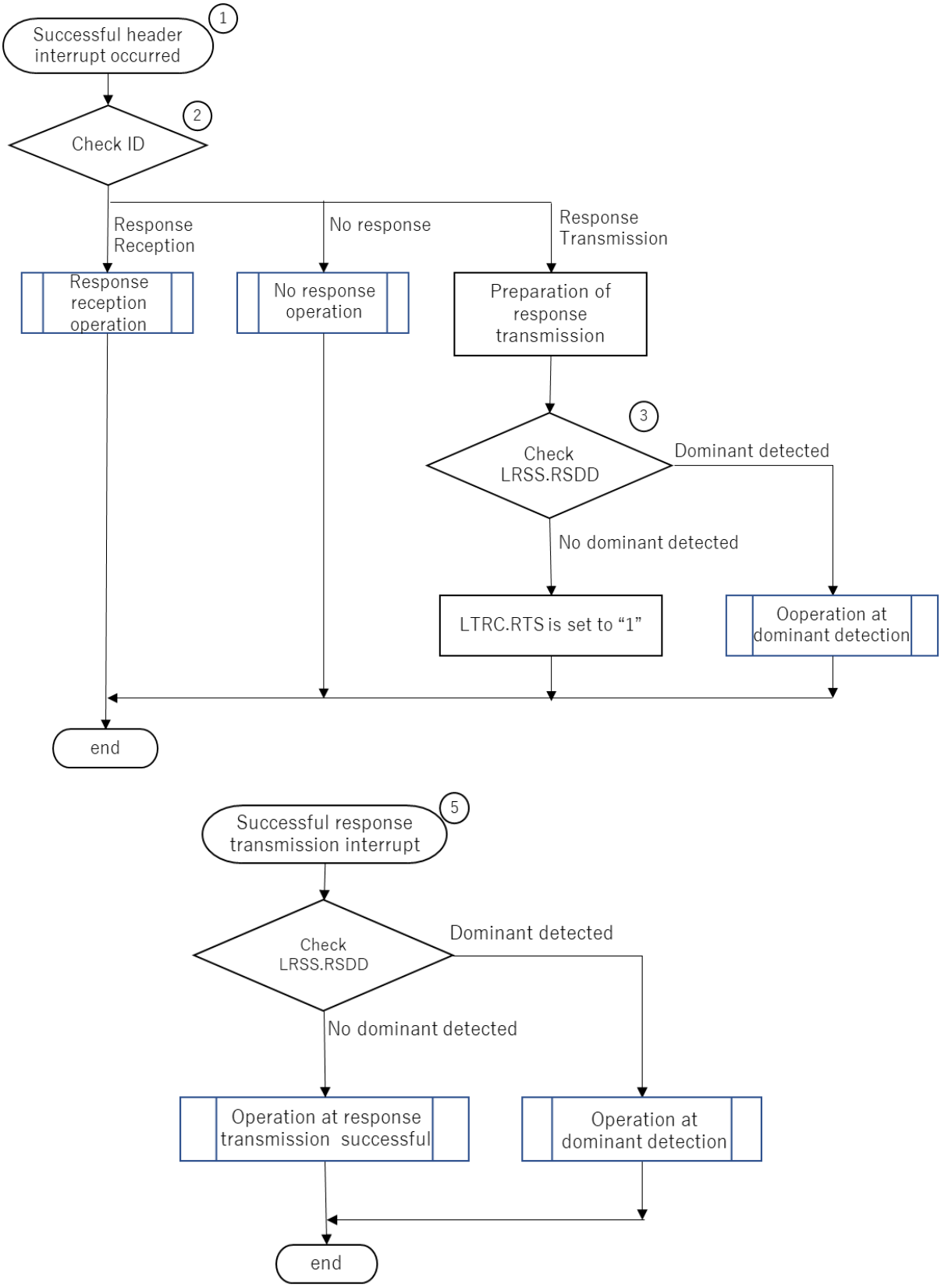


Figure 8-5 : flow of response transmission in LIN slave mode

TABLE OF FIGURES AND TABLES

9 DOCUMENT CHANGE HISTORY

NEW TO ISSUE	SECTIONS	CHANGE	CHANGED BY	DATE
00.01	All	First Draft. Copy from "M40PF uciaprln0043 Specification Ver. 01.00" and modified the following: - Page7. Glossary Color of Tests: Add comment of the color Green. - Page8. 2. Abbreviations HOCO: High speed On Chip Ocsillator -> High speed On Chip Oscillator (typo) - Page17. 3.11.2.1.4 Baud Rate: Add note. - Page 19. 3.11.2.1.4 Baud Rate: Table 3-7: Clock frequency is corrected. - Page32. 4 SFR Overview Table 4-1: Add LIN slave Response Space Status register (LRSS) and LIN slave Break/Sync field Detection register (LBSR) - Page 43. 4.6.3 UART mode LBFC.URPS: description was corrected. All bits of the UART frame will be inverted when inversion is enabled. -> All of the UART reception (data, start/stop-bit and idle) will be inverted when inversion is enabled. LBFC.UTPS: description was corrected. All bits of the UART frame will be inverted when inversion is enabled. -> All of the UART transmission (data, start/stop-bit and idle) will be inverted when inversion is enabled. - Page 46. 4.7 LIN/UART Space Configuration Register (LSC) LSC.IBS[1:0]: Add Note4. - Page 95. 4.26 UART 7BIT / 8BIT / 9BIT RECEIVE DATA REGISTER (LURDR): LURDR.URD[8:0] the register are updated… -> the register is updated … - Page 101. 4.29 LIN Slave Response Space Status Register (LRSS):	ETD1-PC-DP1 K.Ishimi	25 May 2017

		Add section. - Page 102. 4.30 LIN slave Break/Sync Field Reception Register (LBSR) Add section. - Page 122. 6.10 UART Mode-Reception (Single Buffer) Figure 6-10 and the description was changed to designer info. - Page 136. 7.1 CLOCK SOURCE DESCRIPTION Please set up a clock frequency in less then 96MHz… -> Please set up a clock frequency in less than 96MHz… (typo) - Page 149. 7.6.2 UART multi-byte Transmission The space in between each bytes … -> The space in between each byte... (typo) - Page 151. 7.7.1.4 Interrupt generation timings Two conditions are not occur simultaneously. -> Two conditions do not occur simultaneously. - Page 152. 7.7.1.4 Interrupt generation timings Two conditions are not occur simultaneously. -> Two conditions do not occur simultaneously.		
0.02	4 4.6.3 4.29	LIN slave Response Space Status register(LRSS) : Move the offset address : 0030h -> 0034h LIN slave Break/Sync field Reception register(LBSR): Move the offset address : 0034h -> 0030h and change the register name to "LIN slave Break/Sync field Status register(LBSS)" - Page 32. 4 SFR Overview Table 4-1 : - Page 101. 4.29 LIN slave Break/Sync Field Status Register (LBSS) - Page 102. 4.30 LIN Slave Response Space Status Register (LRSS) Page 43 and 44 - LBFC.UTPS and LBFC.URPS: Description was corrected. (data, start/stop-bit and idle) -> (data, start/stop/parity-bit and idle) Page 101. - LIN slave Break/Sync Field Status Register (LBSS) Add note. - LBSS.BRKC LIN Break Field Reception flag. Add description. (Refer to …) - LBSS.SYCC LIN Sync Field Reception flag.	ETD1-PC-DP1 K.Ishimi	6 June 2017

	4.30 0 All	Add description. (Refer to …) Page 102. - LRSS.RSDD Response Space Dominant Detection Flag. Add description. (This bit is valid only …) Setting condition(s): Description was corrected. Note was removed. Page 116 - LIN Slave Mode-Header Detection Figure 6-2 and description was corrected. Typo was corrected. - Page 102 4.30 LIN Slave Response Space Status Register (LRSS) LIE.BRKC -> LRSS.BRKC LIE.SYCC -> LRSS.SYCC		
00.03	3.11.2.1.4 4.29 4.30	Page 19: - Baud Rate Table 3-7: "Target baud rate" and "The nearest setting" was corrected. (Clock frequency = 24,20,16,12 [MHz]) Page 101. - LIN slave Break/Sync Field Status Register (LBSS) Address : 34h -> 30h (typo) Page 102. - LIN slave Response Space Status register(LRSS) Address : 30h -> 34h (typo)	ETD1-PC-DP1 K.Ishimi	23 June 2017
0.04	Cover 4.30	Cover - Add document(ID&Name) of Corresponding Requirement Specification - Copyright is corrected.(RSD -> REL) Page 102. - LRSS.RSDD Add description of invalid condition. Setting condition(s) is corrected.	BBU-SRDD2-PCDD-DPDS1 K.Ishimi	18 July 2017
1.00	2 3.3 3.9.1.1 3.10 3.11.1 3.11.2.1.2 3.11.2.2.1 3.11.2.2.2	Page 8 - Add RS and IBS. Page 10 - Status: Add "Break Field Reception" and "Sync Field Reception" Page 12 - Table 3-1: Title was corrected. (uciaprln0043→uciaprln0044) Page 12 - Macro size and description were corrected. Page 13 - Figure 3-1 was corrected. Page 15 Figure 3-2 : Title was corrected. (uciaprln0043→uciaprln0044) Page 26 - Table 3-14 : Description of pstrb[3:0]: Typo was corrected (...write... -> ...writes...) Page 27 - Figure 3-5 : Title was corrected.	BBU-SRDD2-PCDD-DPDS1 K.Ishimi	25 Aug 2017

		(uciaprln003x→uciaprln004x)		
	4.6.3	Page 42 - Bit Name of USBLS : ...bit length...->... Bit Length... (Typo)		
	4.29	Page 101 - LRSS.BRKC: ・ Add description. (Users should use this bit only for ...) ・ Add reference to Section 8.4 - LBSS.SYCC: ・ Add description. (Users should use this bit only for ...) ・ Add reference to Section 8.4		
	4.30	Page 102 - LRSS.RSDD: Add reference to 5.2.3, 6.4 and 8.5		
	5.2.3	Page 108 - Add description. (If a dominant level of ...)		
	6.2	Page 116 - Figure 6-2 was corrected.		
	6.4.1	Page 118 - 7: Add target registers. (error status and response space status)		
	7.8	Page 156 - Table 7-5 : Add status: "LIN Break Field Reception", "LIN Sync Field Reception" and "Response Space Dominant Detection"		
	7.11.2	Page 175 - Add reference to Section 8.4 for wakeup retransmission.		
	8.1	Page 192 - Add Figure number. (Figure 8-1)		
	8.2.1	Page 193 - Add Table number. (Table 8-1)		
	8.2.2	Page 193 - Add Table number. (Table 8-2)		
	8.2.3	Page 194 - Add Table number. (Table 8-3)		
	8.3	Page 195 - Add Figure number. (Figure 8-2)		
	8.4	Page 196 - Add Section 8.4.		
	8.5	Page 197 - Add Section 8.5.		
1.01	4.29 7.8.2	Page 101 - Add designers infomation. Page 164 - Table 7-11: Add status registers (LBSS.BRKC,LBSS.SYCC,LRSS.RSDD).	BBU-SRDD2-PCDD-DPDS1 K.Ishimi	26 Sep 2017