Section 43 Analog to Digital Converter (ADCJ)

This section contains a description of the A/D Converter (ADCJ).

The first part of this section describes all of this products specific properties, such as the number of units, register base addresses, etc. The remainder of the section describes the functions and registers of the ADCJ.

43.1 Features

43.1.1 Number of Units and Channels

This microcontroller has the following number of ADCJ units.

Table 43.1 Number of Units (For RH850/U2A-EVA)

Product name	U2A-EVA	U2A16		U2A8
		292 pin	516 pin	
Name	ADCJn			
Number of ADCJ Units	3 (n = 0 to 2)	3 (n = 0 to 2)	3 (n = 0 to 2)	3 (n = 0 to 2)
Name	AVSEG			
Number of AVSEG Units	1	1		1

The number of physical channels & virtual channels on individual product are listed below:

Table 43.2 Unit Configurations and Physical Channels (For RH850/U2A-EVA)

Unit Name (Number of Channels) ADCJn		U2A-EVA	U2A16		U2A8
			292 pin	516 pin	
ADCJ0	High accuracy inputs	20	20	20	20
	Low accuracy inputs	10	10	10	10
ADCJ1	High accuracy inputs	20	20	20	20
	Low accuracy inputs	14	14	14	14
ADCJ2	High accuracy inputs	20	5	20	5
	Low accuracy inputs	10	10	10	10

Table 43.3 Unit Configurations and Virtual Channels (For RH850/U2A-EVA)

Unit Name (Number of Channels) ADCJn	U2A-EVA	U2A16		U2A8
		292 pin	516 pin	
ADCJ0	64	64		64
ADCJ1	64	64		64
ADCJ2	64	64		64

Table 43.4 Indices of Products (For RH850/U2A-EVA)

Index	Description
n	Throughout this section, the individual ADCJ units are identified by the index “n” (n = 0 to 2); for example, ADCJnADHALTR indicates the A/D force halt register.
p	Throughout this section, the individual physical channel groups (channel group in the unit) of ADCJn are identified by the index “p”; for example, ANnpq.
q	Throughout this section, the individual physical sub channels (sub channel in the unit) of ADCJn are identified by the index “q”; for example, ANnpq.
j	Throughout this section, the individual virtual channels of ADCJn are identified by the index “j”; for example, ADCJnVCRj indicates the virtual channel register
i	Throughout this section, the individual A/D conversion data of ADCJnVCRj are identified by the index “i”; for example, ADCJnDRj.DRi indicates the A/D conversion data of virtual channel “j”
x	Throughout this section, the individual scan groups (SG) of ADCJn are identified by the index “x” (x = 0 to 4); for example, ADCJnSGSTCRx indicates the scan group x start control register.
y	Throughout this section, the individual A/D timers of ADCJn are identified by the index “y” (y = 3 to 4); for example, ADCJnADTSTCRy indicates the A/D timer y start control register.

43.1.2 Register Base Address

The ADCJn base addresses are listed in the following table.

The ADCJn register addresses are given as offsets from the base address.

Table 43.5 Register Base Address (For RH850/U2A-EVA)

Base Address Name	Base Address	Bus Group
<ADCJ0_base>	FFCA 0000$_H$	Peripheral Group 6L
<AVSEG_base>	FFCA 2000$_H$	Peripheral Group 6L
<ADCJ1_base>	FFF2 0000$_H$	Peripheral Group 7
<ADCJ2_base>	FF9A 2000$_H$	Peripheral Group 2L-A
<ADCJ2_SELB_base>	FF9A 3800$_H$	Peripheral Group 2L-A

43.1.3 Clock Supply

The ADCJn clock supplies are shown in the following table.

Table 43.6 Clock Supply (For RH850/U2A-EVA)

Unit Name	Clock for the Unit	Supply Clock Name
ADCJn (n=0,1)	ADCLK	CLK_ADC
	Register access clock	CLK_LSB
ADCJ2	ADCLK	CLKA_ADC
	Register access clock	CLKA_ADC
AVSEG	Register access clock	CLK_LSB

43.1.4 Interrupt Requests

The ADCJn interrupt requests are listed in the following table.

Table 43.7 Interrupt Requests (1)

Interrupt symbol name	Unit Interrupt Signal	Outline	Interrupt Number	sDMA Trigger Number	DTS Trigger Number	Other Trigger Signals
ADCJ0						
	INTADCJ0ERR (merged INT_ADE0 & INT_UL0)	A/D error interrupt Upper/lower limit error interrupt	228	—	—	—
	INTADCJ0SEC	Secondary voltage monitor error interrupt	T.B.D	—	—	—
	INTADCJ0I0	Scan group 0 (SG0) end interrupt	229	0*2	0*2	GTM*1
	INTADCJ0I1	Scan group 1 (SG1) end interrupt	230	1*2	1*2	GTM*1
	INTADCJ0I2	Scan group 2 (SG2) end interrupt	231	2*2	2*2	GTM*1
	INTADCJ0I3	Scan group 3 (SG3) end interrupt	232	3*2	3*2	GTM*1
	INTADCJ0I4	Scan group 4 (SG4) end interrupt	233	4*2	4*2	GTM*1
	ADMPXI0	MPX DMA trigger request	—	5*2	—	—
	PVCR_END0	PWM A/D conversion end signal	—	6*2	—	—
ADCJ1						
	INTADCJ1ERR (merged INT_ADE1 & INT_UL1)	A/D error interrupt Upper/lower limit error interrupt	234	—	—	—
	INTADCJ1I0	Scan group 0 (SG0) end interrupt	235	7*2	6*2	GTM*1
	INTADCJ1I1	Scan group 1 (SG1) end interrupt	236	8*2	7*2	GTM*1
	INTADCJ1I2	Scan group 2 (SG2) end interrupt	237	9*2	8*2	GTM*1
	INTADCJ1I3	Scan group 3 (SG3) end interrupt	238	10*2	9*2	GTM*1
	INTADCJ1I4	Scan group 4 (SG4) end interrupt	239	11*2	10*2	GTM*1
	ADMPXI1	MPX DMA trigger request	—	12*2	—	—
	PVCR_END1	PWM A/D conversion end signal	—	13*2	—	—

Table 43.8 Interrupt Requests (1)

Interrupt symbol name	Unit Interrupt Signal	Outline	Interrupt Number	sDMA Trigger Number	DTS Trigger Number	Other Trigger Signals
ADCJ2						
	INTADCJ2ERR (merged INT_ADE2 & INT_UL2)	A/D error interrupt Upper/lower limit error interrupt	240	—	—	—
	INTADCJ2I0	Scan group 0 (SG0) end interrupt	241	14*2	12*2	LPS, WUP2
	INTADCJ2I1	Scan group 1 (SG1) end interrupt	242	15*2	13*2	LPS, WUP2
	INTADCJ2I2	Scan group 2 (SG2) end interrupt	243	16*2	14*2	LPS, WUP2
	INTADCJ2I3	Scan group 3 (SG3) end interrupt	244	17*2	15*2	LPS, WUP2
	INTADCJ2I4	Scan group 4 (SG4) end interrupt	245	18*2	16*2	LPS, WUP2
	ADMPXI2	MPX DMA trigger request	—	19*2	—	—
	PVCR_END2	PWM A/D conversion end signal	—	20*2	—	—

Note 1. INTADCJ0I0-4, INTADCJ1I0-4 and INTADCJ2I0-4 are chosen by the PIC (Peripheral Interconnection), and these are forwarded to the GTM. For details, refer to **Section 41, Peripheral Interconnection (PIC)**.

Note 2. All DTS trigger number of ADCJ0, ADCJ1 & ADCJ2 belong to DTS transfer request Group 0.
All DMA trigger number of ADCJ0, ADCJ1 & ADCJ2 belong to DMAC Group 0.

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43.1.5 Reset Source

The ADCJn reset sources are listed in the following table. The ADCJn is initialized by the following reset sources.

Table 43.9 Reset Sources (For RH850/U2A-EVA)

Unit Name	Register Name	Reset Condition						
		Power On Reset	System Reset 1	System Reset 2	Application Reset	DeepSTOP Reset	Module Reset	JTAG Reset
ADCJn (n=0,1)	All registers	√	√	√	√	√	√	—
ADCJ2	All registers	√	√	√	√	—	√	—
AVSEG	All registers	√	√	√	√	√	√	—

43.1.6 External Input/Output Signals

The External Input/Output signals of the ADCJn are listed below.

Table 43.10 ADCJ0 External Input / Output Signals (For RH850/U2A-EVA)

Unit Signal Name	Outline	Alternative Port Pin Signal
A0VCC	Power supply pin for the analog part	A0VCC
A0VSS	Ground pin for the analog part	A0VSS
A0VREFH	Reference voltage pin for the analog part	A0VREFH
AN000	Analog input pin	ADCJ0I0
AN001	Analog input pin	ADCJ0I1
AN002	Analog input pin	ADCJ0I2
AN003	Analog input pin	ADCJ0I3
AN010	Analog input pin	ADCJ0I4
AN011	Analog input pin	ADCJ0I5
AN012	Analog input pin	ADCJ0I6
AN013	Analog input pin	ADCJ0I7
AN020	Analog input pin	ADCJ0I8
AN021	Analog input pin	ADCJ0I9
AN022	Analog input pin	ADCJ0I10
AN023	Analog input pin	ADCJ0I11
AN030	Analog input pin	ADCJ0I12
AN031	Analog input pin	ADCJ0I13
AN032	Analog input pin	ADCJ0I14
AN033	Analog input pin	ADCJ0I15
AN040	Analog input pin	ADCJ0I16
AN041	Analog input pin	ADCJ0I17
AN042	Analog input pin	ADCJ0I18
AN043	Analog input pin	ADCJ0I19
VMON_VCC	Secondary supply voltage monitor for VCC	-
VMON_E0VCC	Secondary supply voltage monitor for E0VCC	-
VMON_ISOVDD	Secondary supply voltage monitor for ISOVDD	-
VMON_AWOVDD	Secondary supply voltage monitor for AWOVDD	-
AN050(*1)	Analog input pin	ADCJ0I0S
AN051(*1)	Analog input pin	ADCJ0I1S
AN052(*1)	Analog input pin	ADCJ0I2S
AN053(*1)	Analog input pin	ADCJ0I3S
AN060(*1)	Analog input pin	ADCJ0I4S
AN061(*1)	Analog input pin	ADCJ0I5S
AN062(*1)	Analog input pin	ADCJ0I6S
AN063(*1)	Analog input pin	ADCJ0I7S
AN070(*1)	Analog input pin	ADCJ0I8S
AN071(*1)	Analog input pin	ADCJ0I9S
ADCJ0TRG0	External trigger pin (Scan group 0) (*2)	ADCJ0TRG0
ADCJ0TRG1	External trigger pin (Scan group 1) (*2)	ADCJ0TRG1
ADCJ0TRG2	External trigger pin (Scan group 2) (*2)	ADCJ0TRG2
ADCJ0TRG3	External trigger pin (Scan group 3) (*2)	ADCJ0TRG3
ADCJ0TRG4	External trigger pin (Scan group 4) (*2)	ADCJ0TRG4

ADCJ0SEL0	External analog multiplexer (MPX) output pin 0	ADCJ0SEL0
ADCJ0SEL1	External analog multiplexer (MPX) output pin 1	ADCJ0SEL1
ADCJ0SEL2	External analog multiplexer (MPX) output pin 2	ADCJ0SEL2
ADEND0	A/D conversion timing monitor pin (Scan group 0)	ADCJ0CNV0
ADEND1	A/D conversion timing monitor pin (Scan group 1)	ADCJ0CNV1
ADEND2	A/D conversion timing monitor pin (Scan group 2)	ADCJ0CNV2
ADEND3	A/D conversion timing monitor pin (Scan group 3)	ADCJ0CNV3
ADEND4	A/D conversion timing monitor pin (Scan group 4)	ADCJ0CNV4

Note 1. Max resolution is 10-bit.
Note 2. When the external trigger pin is used, the noise filter for the port needs to be set. For details, refer to **Section 2 Pin Function**.

Table 43.11 ADCJ0 Physical Channel, Physical Channel Group, Physical Sub Channel, RRAMP & T&H (For RH850/U2A-EVA)

Analog Input or VMON	Physical Channel	Physical Channel Group	Physical Sub Channel	RRAMP Correspondence		T&H
				RRAMP00	RRAMP01	
AN000	0	0	0	√	—	√
AN001	1		1	—	√	√
AN002	2		2	√	—	√
AN003	3		3	—	√	√
AN010	4	1	0	√	—	—
AN011	5		1	—	√	—
AN012	6		2	√	—	—
AN013	7		3	—	√	—
AN020	8	2	0	√	—	—
AN021	9		1	—	√	—
AN022	10		2	√	—	—
AN023	11		3	—	√	—
AN030	12	3	0	√	—	—
AN031	13		1	—	√	—
AN032	14		2	√	—	—
AN033	15		3	—	√	—
AN040	16	4	0	√	—	—
AN041	17		1	—	√	—
AN042	18		2	√	—	—
AN043	19		3	—	√	—
VMON_VCC(*1)	20	5	0	—	—	—
VMON_EVCC(*2)	21		1	—	—	—
VMON_ISOVDD(*3)	22		2	—	—	—
VMON_AWOVDD(*4)	23		3	—	—	—
AN050(*5)	24	6	0	√	—	—
AN051(*5)	25		1	√	—	—
AN052(*5)	26		2	√	—	—
AN053(*5)	27		3	√	—	—
AN060(*5)	28	7	0	√	—	—

AN061(*5)	29		1	√	—	—
AN062(*5)	30		2	√	—	—
AN063(*5)	31		3	√	—	—
AN070(*5)	32	8	0	√	—	—
AN071(*5)	33		1	√	—	—

Note 1. This is the secondary supply voltage monitor for VCC.
Note 2. This is the secondary supply voltage monitor for EVCC.
Note 3. This is the secondary supply voltage monitor for ISOVDD.
Note 4. This is the secondary supply voltage monitor for AWOVDD.
Note 5. Max resolution is 10-bit.

Table 43.12 ADCJ1 External Input / Output Signals (For RH850/U2A-EVA)

Unit Signal Name	Outline	Alternative Port Pin Signal
A1VCC	Power supply pin for the analog part	A1VCC
A1VSS	Ground pin for the analog part	A1VSS
A1VREFH	Reference voltage pin for the analog part	A1VREFH
AN100	Analog input pin	ADCJ1I0
AN101	Analog input pin	ADCJ1I1
AN102	Analog input pin	ADCJ1I2
AN103	Analog input pin	ADCJ1I3
AN110	Analog input pin	ADCJ1I4
AN111	Analog input pin	ADCJ1I5
AN112	Analog input pin	ADCJ1I6
AN113	Analog input pin	ADCJ1I7
AN120	Analog input pin	ADCJ1I8
AN121	Analog input pin	ADCJ1I9
AN122	Analog input pin	ADCJ1I10
AN123	Analog input pin	ADCJ1I11
AN130	Analog input pin	ADCJ1I12
AN131	Analog input pin	ADCJ1I13
AN132	Analog input pin	ADCJ1I14
AN133	Analog input pin	ADCJ1I15
AN140	Analog input pin	ADCJ1I16
AN141	Analog input pin	ADCJ1I17
AN142	Analog input pin	ADCJ1I18
AN143	Analog input pin	ADCJ1I19
AN150(*1)	Analog input pin	ADCJ1I0S
AN151(*1)	Analog input pin	ADCJ1I1S
AN152(*1)	Analog input pin	ADCJ1I2S
AN153(*1)	Analog input pin	ADCJ1I3S
AN160(*1)	Analog input pin	ADCJ1I4S
AN161(*1)	Analog input pin	ADCJ1I5S
AN162(*1)	Analog input pin	ADCJ1I6S
AN163(*1)	Analog input pin	ADCJ1I7S
AN170(*1)	Analog input pin	ADCJ1I8S
AN171(*1)	Analog input pin	ADCJ1I9S
AN172(*1)	Analog input pin	ADCJ1I10S
AN173(*1)	Analog input pin	ADCJ1I11S
AN180(*1)	Analog input pin	ADCJ1I12S
AN181(*1)	Analog input pin	ADCJ1I13S
ADCJ1TRG0	External trigger pin (Scan group 0) (*2)	ADCJ1TRG0
ADCJ1TRG1	External trigger pin (Scan group 1) (*2)	ADCJ1TRG1
ADCJ1TRG2	External trigger pin (Scan group 2) (*2)	ADCJ1TRG2
ADCJ1TRG3	External trigger pin (Scan group 3) (*2)	ADCJ1TRG3
ADCJ1TRG4	External trigger pin (Scan group 4) (*2)	ADCJ1TRG4
ADCJ1SEL0	External analog multiplexer (MPX) output pin 0	ADCJ1SEL0
ADCJ1SEL1	External analog multiplexer (MPX) output pin 1	ADCJ1SEL1
ADCJ1SEL2	External analog multiplexer (MPX) output pin 2	ADCJ1SEL2

ADEND0	A/D conversion timing monitor pin (Scan group 0)	ADCJ1CNV0
ADEND1	A/D conversion timing monitor pin (Scan group 1)	ADCJ1CNV1
ADEND2	A/D conversion timing monitor pin (Scan group 2)	ADCJ1CNV2
ADEND3	A/D conversion timing monitor pin (Scan group 3)	ADCJ1CNV3
ADEND4	A/D conversion timing monitor pin (Scan group 4)	ADCJ1CNV4

Note 1. Max resolution is 10-bit.

Note 2. When the external trigger pin is used, the noise filter for the port needs to be set. For details, refer to **Section 2 Pin Function**.

Table 43.13 ADCJ1 Physical Channel, Physical Channel Group, Physical Sub Channel, RRAMP & T&H (For RH850/U2A-EVA)

Analog Input or VMON	Physical Channel	Physical Channel Group	Physical Sub Channel	RRAMP Correspondence		T&H
				RRAMP10	RRAMP11	
AN100	0	0	0	√	—	√
AN101	1		1	—	√	√
AN102	2		2	√	—	√
AN103	3		3	—	√	√
AN110	4	1	0	√	—	—
AN111	5		1	—	√	—
AN112	6		2	√	—	—
AN113	7		3	—	√	—
AN120	8	2	0	√	—	—
AN121	9		1	—	√	—
AN122	10		2	√	—	—
AN123	11		3	—	√	—
AN130	12	3	0	√	—	—
AN131	13		1	—	√	—
AN132	14		2	√	—	—
AN133	15		3	—	√	—
AN140	16	4	0	√	—	—
AN141	17		1	—	√	—
AN142	18		2	√	—	—
AN143	19		3	—	√	—
AN150(*1)	20	5	0	√	—	—
AN151(*1)	21		1	√	—	—
AN152(*1)	22		2	√	—	—
AN153(*1)	23		3	√	—	—
AN160(*1)	24	6	0	√	—	—
AN161(*1)	25		1	√	—	—
AN162(*1)	26		2	√	—	—
AN163(*1)	27		3	√	—	—
AN170(*1)	28	7	0	√	—	—
AN171(*1)	29		1	√	—	—
AN172(*1)	30		2	√	—	—
AN173(*1)	31		3	√	—	—
AN180(*1)	32	8	0	√	—	—
AN181(*1)	33		1	√	—	—

Note 1. Max resolution is 10-bit.

Table 43.14 ADCJ2 External Input / Output Signals (For RH850/U2A-EVA)

Unit Signal Name	Outline	Alternative Port Pin Signal
A2VCC	Power supply pin for the analog part	A2VCC
A2VSS	Ground pin for the analog part	A2VSS
A2VREFH	Reference voltage pin for the analog part	A2VREFH
AN200	Analog input pin	ADCJ2I0
AN201	Analog input pin	ADCJ2I1
AN202	Analog input pin	ADCJ2I2
AN203	Analog input pin	ADCJ2I3
AN210	Analog input pin	ADCJ2I4
AN211	Analog input pin	ADCJ2I5
AN212	Analog input pin	ADCJ2I6
AN213	Analog input pin	ADCJ2I7
AN220	Analog input pin	ADCJ2I8
AN221	Analog input pin	ADCJ2I9
AN222	Analog input pin	ADCJ2I10
AN223	Analog input pin	ADCJ2I11
AN230	Analog input pin	ADCJ2I12
AN231	Analog input pin	ADCJ2I13
AN232	Analog input pin	ADCJ2I14
AN233	Analog input pin	ADCJ2I15
AN240	Analog input pin	ADCJ2I16
AN241	Analog input pin	ADCJ2I17
AN242	Analog input pin	ADCJ2I18
AN243	Analog input pin	ADCJ2I19
AN250(*1)	Analog input pin	ADCJ2I0S
AN251(*1)	Analog input pin	ADCJ2I1S
AN252(*1)	Analog input pin	ADCJ2I2S
AN253(*1)	Analog input pin	ADCJ2I3S
AN260(*1)	Analog input pin	ADCJ2I4S
AN261(*1)	Analog input pin	ADCJ2I5S
AN262(*1)	Analog input pin	ADCJ2I6S
AN263(*1)	Analog input pin	ADCJ2I7S
AN270(*1)	Analog input pin	ADCJ2I8S
AN271(*1)	Analog input pin	ADCJ2I9S
ADCJ2TRG0	External trigger pin (Scan group 0) (*2)	ADCJ2TRG0
ADCJ2TRG1	External trigger pin (Scan group 1) (*2)	ADCJ2TRG1
ADCJ2TRG2	External trigger pin (Scan group 2) (*2)	ADCJ2TRG2
ADCJ2TRG3	External trigger pin (Scan group 3) (*2)	ADCJ2TRG3
ADCJ2TRG4	External trigger pin (Scan group 4) (*2)	ADCJ2TRG4
ADCJ2SEL0	External analog multiplexer (MPX) output pin 0	ADCJ2SEL0
ADCJ2SEL1	External analog multiplexer (MPX) output pin 1	ADCJ2SEL1
ADCJ2SEL2	External analog multiplexer (MPX) output pin 2	ADCJ2SEL2

ADEND0	A/D conversion timing monitor pin (Scan group 0)	ADCJ2CNV0
ADEND1	A/D conversion timing monitor pin (Scan group 1)	ADCJ2CNV1
ADEND2	A/D conversion timing monitor pin (Scan group 2)	ADCJ2CNV2
ADEND3	A/D conversion timing monitor pin (Scan group 3)	ADCJ2CNV3
ADEND4	A/D conversion timing monitor pin (Scan group 4)	ADCJ2CNV4

Note 1. Max resolution is 10-bit.
Note 2. When the external trigger pin is used, the noise filter for the port needs to be set. For details, refer to **Section 2 Pin Function**.

Table 43.15 ADCJ2 Physical Channel, Physical Channel Group, Physical Sub Channel, RRAMP & T&H (For RH850/U2A-EVA)

Analog Input or VMON	Physical Channel	Physical Channel Group	Physical Sub Channel	RRAMP Correspondence		T&H
				RRAMP20	RRAMP21	
AN200	0	0	0	√	—	—
AN201	1		1	—	√	—
AN202	2		2	√	—	—
AN203	3		3	—	√	—
AN210	4	1	0	√	—	—
AN211	5		1	—	√	—
AN212	6		2	√	—	—
AN213	7		3	—	√	—
AN220	8	2	0	√	—	—
AN221	9		1	—	√	—
AN222	10		2	√	—	—
AN223	11		3	—	√	—
AN230	12	3	0	√	—	—
AN231	13		1	—	√	—
AN232	14		2	√	—	—
AN233	15		3	—	√	—
AN240	16	4	0	√	—	—
AN241	17		1	—	√	—
AN242	18		2	√	—	—
AN243	19		3	—	√	—
AN250(*1)	20	5	0	√	—	—
AN251(*1)	21		1	√	—	—
AN252(*1)	22		2	√	—	—
AN253(*1)	23		3	√	—	—
AN260(*1)	24	6	0	√	—	—
AN261(*1)	25		1	√	—	—
AN262(*1)	26		2	√	—	—
AN263(*1)	27		3	√	—	—
AN270(*1)	28	7	0	√	—	—
AN271(*1)	29		1	√	—	—

Note 1. Max resolution is 10-bit.

[Product design point]

RRAMP is the estimate by which sharing is possible to at most 10 analog input per 1 (Estimate result by ACTD).

Allocation of RRAMP has been discussed and decided with an IP developer with ACTD.

For way to allocate of RRAMP of each number of use of RRAMP, refer to IP target specifications.

43.2 Overview

43.2.1 Functional Overview

The ADCJADCJ has the following features.

- Configuration of analog input pins
  See **Section 43.1.1, Number of Units and Channels** about the number of modules, the number of total analog input pins, the number of high accuracy inputs and low accuracy inputs.
- Sample-and-hold function
  Each module has an internal sample-and-hold circuit that enables each module to perform an A/D conversion independently.
- Advanced A/D converter
  Resolution: 12 / 10 bits
  A/D conversion method: Successive approximation
  Conversion speed: 1.0 µs (min)
- Supporting five scan groups
  Each ADCJADCJ has five scan groups (SG0, SG1, SG2, SG3 and SG4).

  SG4 can select PWM-Diag function.

  Scan settings can be made independently for each scan group.
- Track & Hold (T&H) input channels
  - 4 channel inputs per unit (ADCJ0,1) can select T&H circuit for synchronize conversion.
- Two scan modes
  Each ADCJADCJ has two scan modes.
  Multicycle scan mode executes the specified number of scans.
  Continuous scan mode executes scans repeatedly without limit.
- Virtual channels
  Each ADCJADCJ has several virtual channels. See **Section 43.1.1, Number of Units and Channels** about the number of virtual channels. Analog channels for which A/D conversion is to be made and other accompanying information are set for each virtual channel. By sequentially performing the processing for the virtual channels indicated by the start virtual channel pointer and the end virtual channel pointer in each scan group, scans (which can perform A/D conversion for any analog channels in any order) can be executed. Each virtual channel can be mapped to any physical channel.
- Extended physical channels
  Each ADCJADCJ can extend physical channels by using an external analog multiplexer. Furthermore, an external analog multiplexer can be used with either discrete port pins or the ~~CSIH~~MSPI peripheral. The discrete port pins and/or ~~CSIH~~MSPI is under the control of the ADCJADCJ for multiplexer channel selection. The ~~CSIH~~MSPI interface requires DMA when used. ~~(One channel can be set for each~~ ADCJADCJ~~.)~~
- Interval function
  The ADCJADCJ can start scan groups in any cycle by using the A/D timer equipped in the scan groups 3 and 4. This enables scans with intervals inserted.
- A/D-converted value adding function
  The ADCJADCJ performs A/D conversion sequentially twice or four times for a channel, and stores the addition result in the data register. The addition count can be set for each virtual channel.

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The effect of the moving average filter can be gained by using this function.
In addition, using the optional ADC Summation Function (ASF) makes an extended summation function available. For details, see **Section 34.8, ADC Summation Function (ASF)**.

- Data registers
  Data registers corresponding to virtual channels are provided.
- Start trigger for each scan group
  Hardware triggers and software triggers can start the processing of each scan group. Only scan groups 3 and 4 can start processing by an A/D timer trigger.
- Asynchronous/synchronous suspend and resume function
  Processing for a scan group can interrupt an ongoing processing for another scan group.
  The priority is as follows:

  Low High

  SG0 < SG1 < SG2 < SG3 < SG4 (SG: Scan group)

  The following suspend methods can be chosen:
  Synchronous suspend: Processing is suspended after the ongoing virtual channel processing has stopped.
  Asynchronous suspend: Processing is suspended immediately.
  Synchronous/asynchronous mixture type suspend:
  SGx except for SG0 is “synchronous suspend” mode.
  SG0 is in “asynchronous suspend” mode.
- Entry to the digital filter engine, and the ADC summation function, and the Generic Timer Module
  A/D-converted values can be directly entered into the Digital Filter Engine (DFE), or the ADC Summation Function (ASF), or the Generic Timer Module (GTM). Whether to enable or disable entry and a tag used to define the target channel to be entered can be set for each virtual channel. Entry to the DFE (GTM)GTM or entry to the ASF can be set for each scan group.
  For details of the DFE, refer to **Section 37, Digital Filter Engine (DFE)**.
  For details of the ASF, refer to **Section 34.8, ADC Summation Function (ASF)**.
  For details of the GTM, refer to **Section 3138, Generic Timer Module (GTM)**.
- Scan end interrupt and DMA transfer
  Each scan group can generate an interrupt request to the INTC and activate the DMAC each time a processing for the virtual channel indicated by the end virtual channel pointer ends or a virtual channel ends.
- Interrupt and DMA transfer for an external analog multiplexer
  The ADCJADCJ can generate an interrupt request to the INTC and activate the DMAC when the specified virtual channel is started. This enables transfer of the MPX value to an external analog multiplexer in cooperation with an I/O port or CSIHMSPI. There is a register to provide for a programmable ADC conversion delay (N us (N = 0, 1, 2, ..., 10)) for DMA transfer time and external multiplexer settling time.
- Selectable analog conversion voltage
  The AnVREFH pin can be used to set the voltage range for analog conversion.
- A/D conversion monitor output
  The processing timing of a desired virtual channel can be output to the A/D conversion monitor output pin (ADENDn).
- A wide range of safety functions
  The ADCJADCJ has various safety functions, including self-diagnosis, pin-level self-diagnosis, wiring-break detection, self-diagnosis of the wiring-break detection function, self-diagnosis of the secondary power supply voltage monitor function (For RH850/E2x-FCC1, E2M, E2L U2A-EVA), self-diagnosis of the secondary power supply

~~voltage monitor function~~, self-diagnosis of the T&H path, normality check for the analog selection, upper-limit/lower-limit check for the data registers (8 tables), trigger overlap check, parity check for the data registers, overwrite check for the data registers, and read and clear functions for the data registers.

- Upper/lower-limit-excursion-notice-function to ADC VMON secondary error generator (AVSEG) (For RH850/~~E2x-FCC1, E2M, E2L~~ U2A-EVA) ~~or ADC boundary flag generator (ABFG)~~ in each virtual channel
  The ADCJADCJn can output to the ADC-VMON-secondary-error-generator (AVSEG) (The output to AVSEG is ADCJADCJ0 only) (For RH850/~~E2x-FCC1, E2M, E2L~~ U2A-EVA) ~~or the ADC boundary flag generator (ABFG)~~ a signal to notify that an A/D conversion result has increased above the upper limit value of the designated table in each virtual channel or that an A/D conversion result has decreased below the lower limit value of the designated table in each virtual channel.
  Once the Table register for the upper/lower limit value is set, it can be rewritten at any time.
  For details of the AVSEG, **Section 43.7, ADC VMON Secondary Error Generator (AVSEG)**. (For RH850/~~E2x-FCC1, E2M, E2L~~ U2A-EVA)
  ~~For details of the ABFG, **Section 34.11, ADC Boundary Flag Generator (ABFG)**.~~
- Secondary power supply voltage monitor (VMON) (For RH850/~~E2x-FCC1, E2M, E2L~~ U2A-EVA) (this item is added by product development member)
  The ADCJADCJ0 can convert the voltage of VCC, EVCC, ISOVDD and the AWOVDD power supply in AD.
  Secondary HDET, Secondary LDET of each power supply (VCC, EVCC, ISOVDD and AWOVDD) can be notified to ECM by using the upper/lower-limit-excess-notice-function of ADCJADCJ0 and AVSEG.
  For details of AVSEG, **Section 43.7, ADC VMON Secondary Error Generator (AVSEG).**
  For the whole description of power supply voltage monitor, refer to **Section ~~12~~ 11, Power Supply Voltage Monitor**.

43.2.2 Block Diagram

The block diagram of ADCJ0 is shown in **Figure 43.1**. The block diagram of ADCJ1 is shown in **Figure 43.2**. The block diagram of ADCJ2 is shown in **Figure 43.3**.

(1) Configuration of ADCJ0ADCJ0

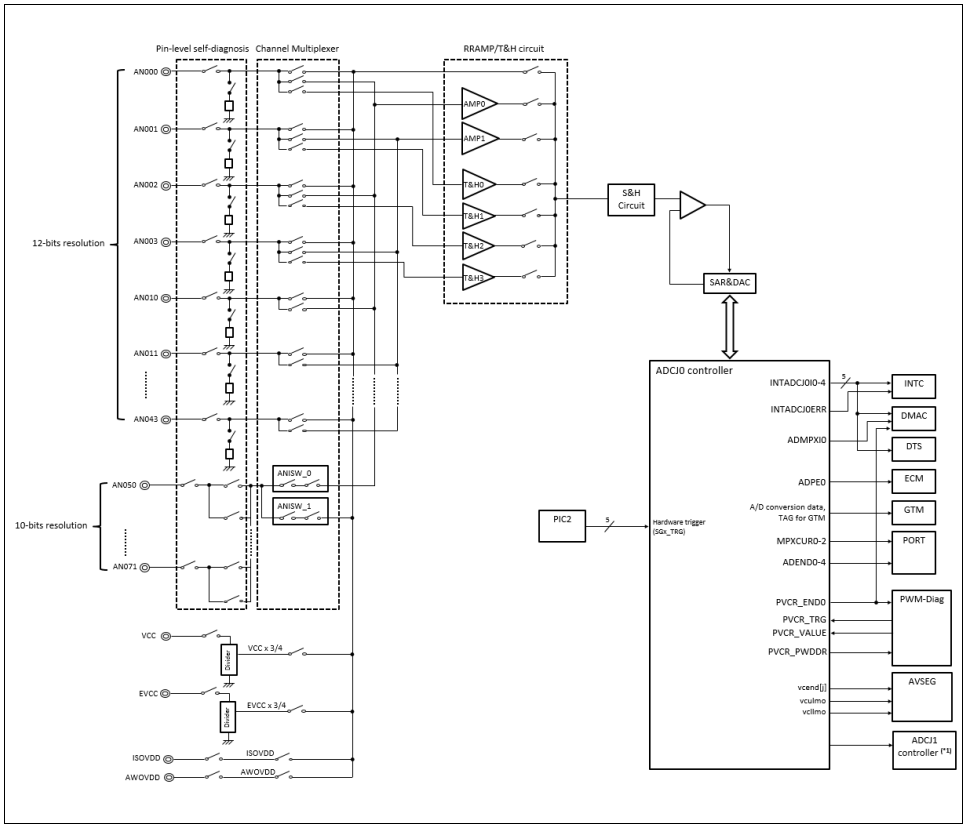

Figure 43.1 ADCJ0ADCJ0 Block Diagram (For RH850/E2x-FCC1U2A-EVA)

Note 1. Support simultaneous start between ADCJ0 and ADCJ1.

(2) Configuration of ADCJ~~2~~ ADCJ1

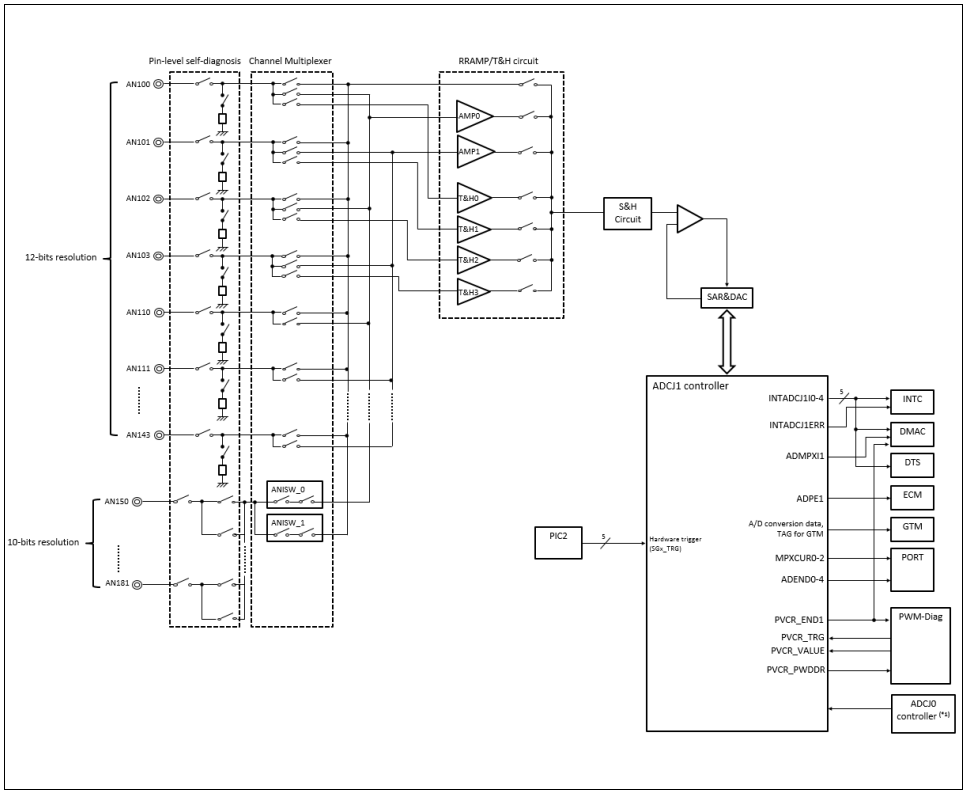

Figure 43.2 ADCJ~~2~~ ADCJ1 Block Diagram (For RH850/~~E2x-FCC1~~ U2A-EVA)

Note 1. Support simultaneous start between ADCJ0 and ADCJ1.

(3) Configuration of ADCJ~~3~~ ADCJ2 (For RH850/~~E2x-FCC1~~ U2A-EVA)

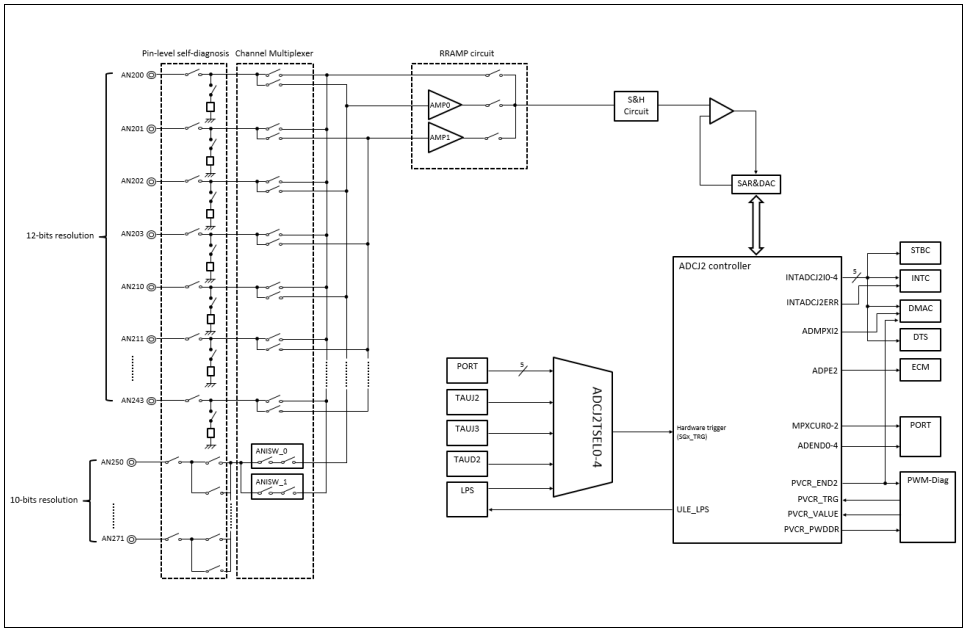

Figure 43.3 ADCJ~~3~~ADCJ2 Block Diagram (For RH850/~~E2x-FCC1~~ U2A-EVA)

43.3 Registers

43.3.1 List of Registers

The ADCJ ADCJ registers are listed in the following table.

For details about <ADCJn ADCJn_base>, see **Section 43.1.2, Register Base Address**.

Table 43.16 List of Registers (1/3)

Module Name	Register Name	Symbol	Address	Access	Access Protection
ADCJ Common Registers					
ADCJ0	A/D synchronization start control register	ADCJ0ADSYNSTCR	<ADCJ0_base> + 610_H	8, 16, 32	—
ADCJ0	A/D timer synchronization start control register	ADCJ0ADTSYNSTCR	<ADCJ0_base> + 614_H	8, 16, 32	—
ADCJ0	Voltage monitor voltage divider control register 1	ADCJ0VMONVDCR1	<ADCJ0_base> + 740_H	8, 16, 32	—
ADCJ0	Voltage monitor voltage divider control register 2	ADCJ0VMONVDCR2	<ADCJ0_base> + 744_H	8, 16, 32	—

Table 43.16 List of Registers (2/3)

Module Name	Register Name	Symbol	Address	Access	Access Protection
ADCJ Specific Registers (Virtual Channel)					
ADCJn	Virtual channel register j	ADCJnVCRj	<ADCJn_base> + j × 4_H	8, 16, 32	—
ADCJn	PWM-Diag Virtual Channel Register	ADCJnPWDVCR	<ADCJn_base> + 180_H	—	—
ADCJn	Data register j	ADCJnDRj	<ADCJn_base> + ~~1001~~A0$_H$ + j × 2_H	16, 32 (j is even) 16 (j is odd)	—
ADCJn	PWM-Diag Data Register	ADCJnPWDDR	<ADCJn_base> + 260_H	—	—
ADCJn	Data supplementary information register j	ADCJnDIRj	<ADCJn_base> + ~~200~~280$_H$ + j × 4_H	16, 32	—
ADCJn	PWM-Diag data supplementary information register	ADCJnPWDDIR	<ADCJn_base> + 400_H	—	—
ADCJ Specific Registers (Control)					
ADCJn	A/D halt register	ADCJnADHALTR	<ADCJn_base> + 640_H	8, 16, 32	—
ADCJn	A/D control register 1	ADCJnADCR1	<ADCJn_base> + 644_H	8, 16, 32	—
ADCJn	A/D control register 2	ADCJnADCR2	<ADCJn_base> + 648_H	8, 16, 32	—
ADCJn	Sampling Control Register	ADCJnSMPCR	<ADCJn_base> + $64C_H$	8, 16, 32	—
ADCJn	MPX current control register	ADCJnMPXCURCR	<ADCJn_base> + 650_H	8, 16	—
ADCJn	MPX interrupt enable register	ADCJnMPXINTER	<ADCJn_base> + 654_H	8, 16	—

ADCJn	MPX current register 1	ADCJnMPXCURR1	<ADCJn_base> + 658_H	—	—
ADCJn	MPX current register 2	ADCJnMPXCURR2	<ADCJn_base> + $65C_H$	—	—
ADCJn	MPX command information register	ADCJnMPXCMDR	<ADCJn_base> + 660_H	8, 16, 32	—
ADCJn	GTM entry scan group enable register	ADCJnGTMENTSGER	<ADCJn_base> + 670_H	8, 16, 32	—
ADCJn	A/D conversion monitor virtual channel pointer x	ADCJnADENDPx	<ADCJn_base> + x × 04_H + 674_H	8, 16, 32	—
ADCJn	T&H Sampling Start Control Register	ADCJnTHSMPSTCR	<ADCJn_base> + 690_H	8, 16, 32	—
ADCJn	T&H Stop Control Register	ADCJnTHSTPCR	<ADCJn_base> + 694_H	8, 16, 32	—
ADCJn	T&H Control Register	ADCJnTHCR	<ADCJn_base> + 698_H	8, 16, 32	—
ADCJn	T&H Group A hold start control register	ADCJnTHAHLDSTCR	<ADCJn_base> + $6A0_H$	8, 16, 32	—
ADCJn	T&H Group B hold start control register	ADCJnTHBHLDSTCR	<ADCJn_base> + $6A4_H$	8, 16, 32	—
ADCJn	T&H Group Selection Register	ADCJnTHGSR	<ADCJn_base> + $6B0_H$	8, 16, 32	—
ADCJn	T&H Enable Register	ADCJnTHER	<ADCJn_base> + $6B4_H$	8, 16, 32	—
ADCJn	T&H Group A Control Register	ADCJnTHACR	<ADCJn_base> + $6C0_H$	8, 16, 32	—
ADCJn	T&H Group B Control Register	ADCJnTHBCR	<ADCJn_base> + $6C4_H$	8, 16, 32	—
ADCJn	Wait setting register 0	ADCJnWAITTR0	<ADCJn_base> + 700_H	8, 16	—
ADCJn	Wait setting register 1	ADCJnWAITTR1	<ADCJn_base> + 704_H	8, 16	—
ADCJn	Wait setting register 2	ADCJnWAITTR2	<ADCJn_base> + 708_H	8, 16	—
ADCJn	Wait setting register 3	ADCJnWAITTR3	<ADCJn_base> + $70C_H$	8, 16	—
ADCJn	Wait setting register 4	ADCJnWAITTR4	<ADCJn_base> + 710_H	8, 16	—
ADCJn	Wait setting register 5	ADCJnWAITTR5	<ADCJn_base> + 714_H	8, 16	—
ADCJn	Wait setting register 6	ADCJnWAITTR6	<ADCJn_base> + 718_H	8, 16	—
ADCJn	Wait setting register 7	ADCJnWAITTR7	<ADCJn_base> + $71C_H$	8, 16	—
ADCJn	Emulation Control Register	ADCJnEMUCR	<ADCJn_base> + 750_H	8, 16, 32	—

Table 43.16 List of Registers (3/3)

Module Name	Register Name	Symbol	Address	Access	Access Protection
ADCJ Specific Registers (Safety-related)					
ADCJn	Pin-level self-diagnosis control register	ADCJnTDCR	<ADCJn_base> + 760_H	8, 16, 32	—
ADCJn	Wiring-break detection control register	ADCJnODCR	<ADCJn_base> + 764_H	8, 16, 32	—
ADCJn	Safety control register	ADCJnSFTCR	<ADCJn_base> + 770_H	8, 16, 32	—
ADCJn	Trigger overlap check control register	ADCJnTOCCR	<ADCJn_base> + 774_H	8, 16, 32	—
ADCJn	Upper/Lower Limit Error table register 0	ADCJnULLMTBR0	<ADCJn_base> + 780_H	8, 16, 32	—
ADCJn	Upper/Lower Limit Error table register 1	ADCJnULLMTBR1	<ADCJn_base> + 784_H	8, 16, 32	—
ADCJn	Upper/Lower Limit Error table register 2	ADCJnULLMTBR2	<ADCJn_base> + 788_H	8, 16, 32	—
ADCJn	Trigger overlap check error status register	ADCJnTOCER	<ADCJn_base> + 790_H	—	—
ADCJn	Synchronization Error Register	ADCJnSYNCER	<ADCJn_base> + 794_H	—	—
ADCJn	Upper/Lower Limit Error status register	ADCJnULER	<ADCJn_base> + 798_H	—	—
ADCJn	Overwrite error register	ADCJnOWER	<ADCJn_base> + $79C_H$	—	—
ADCJn	Parity error register	ADCJnPER	<ADCJn_base> + $7A0_H$	—	—
ADCJn	ID Error Register	IDER	<ADCJn_base> + $7A4_H$	—	—
ADCJn	Error clear register	ADCJnECR	<ADCJn_base> + $7A8_H$	8, 16, 32	—
ADCJn	Upper/Lower Limit Check Table Register 0	ADCJnVCULLMTBR0	<ADCJn_base> + 800_H	32	—
ADCJn	Upper/Lower Limit Check Table Register 1	ADCJnVCULLMTBR1	<ADCJn_base> + 804_H	32	—
ADCJn	Upper/Lower Limit Check Table Register 2	ADCJnVCULLMTBR2	<ADCJn_base> + 808_H	32	—
ADCJn	Upper/Lower Limit Check Table Register 3	ADCJnVCULLMTBR3	<ADCJn_base> + $80C_H$	32	—
ADCJn	Upper/Lower Limit Check Table Register 4	ADCJnVCULLMTBR4	<ADCJn_base> + 810_H	32	—
ADCJn	Upper/Lower Limit Check Table Register 5	ADCJnVCULLMTBR5	<ADCJn_base> + 814_H	32	—
ADCJn	Upper/Lower Limit Check Table Register 6	ADCJnVCULLMTBR6	<ADCJn_base> + 818_H	32	—
ADCJn	Upper/Lower Limit Check Table Register 7	ADCJnVCULLMTBR7	<ADCJn_base> + $81C_H$	32	—
ADCJn	Upper/Lower Limit Check Interrupt Enable Register 1	ADCJnVCLMINTER1	<ADCJn_base> + 840_H	8, 16, 32	—
ADCJn	Upper/Lower Limit Check Interrupt Enable Register 2	ADCJnVCLMINTER2	<ADCJn_base> + 844_H	8, 16, 32	—
ADCJn	Upper/Lower Limit Check Interrupt Enable Register 3	ADCJnVCLMINTER3	<ADCJn_base> + 848_H	8, 16, 32	—

ADCJn	PWM-Diag Upper/Lower Limit Check Interrupt Enable Register	ADCJnPWVCLMINTER	<ADCJn_base> + $84C_H$	8, 16, 32	—
ADCJn	Upper/Lower Limit Check Status Register 1	ADCJnVCLMSR1	<ADCJn_base> + 860_H	—	—
ADCJn	Upper/Lower Limit Check Status Register 2	ADCJnVCLMSR2	<ADCJn_base> + 864_H	—	—
ADCJn	Upper/Lower Limit Check Status Register 3	ADCJnVCLMSR3	<ADCJn_base> + 868_H	—	—
ADCJn	PWM-Diag Upper/Lower Limit Check Status Register	ADCJnPWVCLMSR	<ADCJn_base> + $86C_H$	—	—
ADCJn	Scan group x Upper/Lower Limit Check Status Register	ADCJnSGULCRx	<ADCJn_base> + x × 04_H + 880_H	—	—
ADCJn	Upper/Lower Limit Check Status Clear Register 1	ADCJnVCLMSCR1	<ADCJn_base> + $8A0_H$	8, 16, 32	—
ADCJn	Upper/Lower Limit Check Status Clear Register 2	ADCJnVCLMSCR2	<ADCJn_base> + $8A4_H$	8, 16, 32	—
ADCJn	Upper/Lower Limit Check Status Clear Register 3	ADCJnVCLMSCR3	<ADCJn_base> + $8A8_H$	8, 16, 32	—
ADCJn	PWM-Diag Upper/Lower Limit Check Status Clear Register	ADCJnPWVCLMSCR	<ADCJn_base> + $8AC_H$	8, 16, 32	—
ADCJn	Scan Group Upper/Lower Limit Check Status Clear Register	ADCJnSGULCCR	<ADCJn_base> + $8B4_H$	8, 16, 32	—
ADCJn	Virtual Channel Upper/Lower Limit Check Status Clear Register	ADCJnVCLMASCR	<ADCJn_base> + $8B8_H$	8, 16, 32	—
ADCJ Scan Group Specific Registers					
ADCJn	Scan group x start control register	ADCJnSGSTCRx	<ADCJn_base> + x × 40_H + 440_H	8, 16, 32	—
ADCJn	Scan group x stop control register	ADCJnSGSTPCRx	<ADCJn_base> + x × 40_H + 444_H	8, 16, 32	—
ADCJn	Scan group x control register	ADCJnSGCRx	<ADCJn_base> + x × 40_H + 450_H	8, 16, 32	—
ADCJn	Scan group x virtual channel pointer	ADCJnSGVCSPx	<ADCJn_base> + x × 40_H + 454_H	16, 32	—
ADCJn	Scan group x multicycle register	ADCJnSGMCYCRx	<ADCJn_base> + x × 40_H + 458_H	8, 16, 32	—
ADCJn	Scan group x status register	ADCJnSGSRx	<ADCJn_base> + x × 40_H + 460_H	—	—
ADCJn	Scan group x Upper/Lower Limit Error Table Select Register	ADCJnULLMSRx	<ADCJn_base> + x × 40_H + 470_H	8, 16, 32	—
ADCJn	A/D timer y start control register	ADCJnADTSTCRy	<ADCJn_base> + y × ~~80~~40_H + ~~488~~448_H	8, 16, 32	—
ADCJn	A/D timer y end control register	ADCJnADTENDCRy	<ADCJn_base> + y × ~~80~~40_H + ~~48C~~$44C_H$	8, 16, 32	—
ADCJn	A/D timer y initial phase register	ADCJnADTIPRy	<ADCJn_base> + y × 40_H + 464_H	8, 16, 32	—
ADCJn	A/D timer y cycle register	ADCJnADTPRRy	<ADCJn_base> + y × 40_H + 468_H	8, 16, 32	—
ADCJn	PWM-Diag control register	ADCJnPWDCR	<ADCJn_base> + 580_H	8, 16, 32	—
ADCJn	PWM-Diag scan group control register	ADCJnPWDSGCR	<ADCJn_base> + 584_H	8, 16, 32	—
ADCJn	PWM-Diag start control register	ADCJnPWDSGSTCR	<ADCJn_base> + 588_H	8, 16, 32	—
ADCJn	PWM-Diag Scan Group select register	ADCJnPWDSGSR	<ADCJn_base> + $58C_H$	8, 16, 32	—

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ADCJn	Scan Group Common Status Register	ADCJnSGSTR	<ADCJn_base> + 600_H	—	—
ADCJn	A/D synchronization start control register	ADCJnADSYNSTCR	<ADCJn_base> + 610_H	8, 16, 32	—
ADCJn	A/D timer synchronization start control register	ADCJnADTSYNSTCR	<ADCJn_base> + 614_H	8, 16, 32	—
ADCJ Test Specific Registers					
ADCJn	Trimming Control Register	ADCJnTRMCR	<ADCJn_base> + $8C0_H$	8, 16, 32	—
ADCJn	AD Test Register A	ADCJnADTSTRA	<ADCJn_base> + $8C4_H$	8, 16, 32	—
ADCJn	AD Test Register B	ADCJnADTSTRB	<ADCJn_base> + $8C8_H$	8, 16, 32	—
ADCJn	AD Test Register C	ADCJnADTSTRC	<ADCJn_base> + $8CC_H$	8, 16, 32	—
ADCJn	AD Test Register D	ADCJnADTSTRD	<ADCJn_base> + $8D0_H$	8, 16, 32	—

43.3.2 ADCJ Common Registers

This section describes the common registers for each ADCJ.

43.3.2.1 ADCJ0ADSYNSTCR — A/D Synchronization Start Control Register

ADCJnADSYNSTCR is an 8-bit write-only register to control simultaneous start of A/D conversion of scan groups ADCJ0 and ADCJ1.

This register setting is available only for ADCJ0.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	ADSTART
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	W

Table 43.17 ADCJ0ADSYNSTCR Register Contents

Bit Position	Bit Name	Function
7 to 1	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
0	ADSTART	A/D Conversion Simultaneous Start This software trigger is used to simultaneously start A/D conversion of scan groups ADCJ0 and ADCJ1. 0: No function (Writing 0 to this bit is ignored.) 1: A/D conversion start Set the scan group synchronization start enable bit (ADCJnSGCRx.ADSTARTE bit of ADCJ0 and ADCJ1) of desired scan group x in advance.

[For internal use only]

It's necessary to implement as follows so that this function can be achieved.

adcsm_0.adstart_o → adcsm_0.adstart_i
→ adcsm_1.adstart_i
adcsm_1.adstart_o → Open
adcsm_2.adstart_o → Open

NOTE

The ADSTART setting in ADCJnADSYNSTCR is transferred to the output signal adstart_o. The output signal adstart_o of ADCJ0 is connected to the input signal adstart_i of ADCJ1, but the output signal adstart_o of ADCJ1 is not connected to any signal. Therefore, the ADSTART setting in ADCJnADSYNSTCR of ADCJ1 is invalid.

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43.3.2.2 ADCJ0ADTSYNSTCR — A/D Timer Synchronization Start Control Register

ADCJnADTSYNSTCR is an 8-bit write-only register to control simultaneous count operation start of each AD timer of ADCJ0 and ADCJ1.

This register setting is available only for ADCJ0.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	ADTSTART
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	W

Table 43.18 ADCJ0ADTSYNSTCR Register Contents

Bit Position	Bit Name	Function
7 to 1	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
0	ADTSTART	AD Timer Simultaneous Start This software trigger is used to simultaneously start AD timer count operation of ADCJ0 and ADCJ1. 0: No function (Writing 0 to this bit is ignored.) 1: AD timer count start The AD timer is implemented in scan groups 3 and 4. Set the AD timer synchronization start enable bit (ADCJnSGCRx.ADTSTARTE bit of ADCJ0 and ADCJ1) of desired scan group x in advance. A/D conversion of the scan group starts at the end of AD timer count.

[For internal use only]

It's necessary to implement as follows so that this function can be achieved.

adcsm_0.adtstart_o → adcsm_0.adtstart_i
→ adcsm_1.adtstart_i
adcsm_1.adtstart_o → Open
adcsm_2.adtstart_o → Open

NOTE

The ADTSTART setting in ADTSYNSTCR is transferred to the output signal adtstart_o. The output signal adtstart_o of ADCJ0 is connected to the input signal adtstart_i of ADCJ1, but the output signal adtstart_o of ADCJ1is not connected to any signal. Therefore, the ADTSTART setting in ADTSYNSTCR of ADCJ1 is invalid.

43.3.2.3 ADCJ0VMONVDCR1 — Voltage monitor voltage divider control register 1

ADCJnVMONVDCR1 is an 8-bit readable and writable register to control the voltage monitoring voltage divider of VCC and E0VCC.

This is only present in ADCJ0.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	VDE1
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W

Table 43.19 ADCJ0VMONVDCR1 Register Contents

Bit Position	Bit Name	Function
7 to 1	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
0	VDE1	Voltage Divider Enable (Voltage Dividing Resistor Control) This bit is used to control the voltage dividing resistor together with the VDE2 bit in ADCJnVMONVDCR2. For details, see "Table 43.20 Resistance Voltage Divider and Pull-down Control Setting Table"

CAUTIONS

1. To prevent a malfunction, this register has restrictions for updating settings. For restrictions on updating settings, see "**Error! Reference source not found. Error! Reference source not found.**".
2. Do not perform A/D conversion with the setting of ADCJnVMONVDCR1.VDE1 or ADCJnVMONVDCR2.VDE2 = 01B or 10B.

43.3.2.4 ADCJ0VMONVDCR2 — Voltage monitor voltage divider control register 2

VMONVDCR2 is an 8-bit readable and writable register to control the voltage monitoring voltage divider of VCC and E0VCC.

This is only present in ADCJ0.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	VDE2
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W

Table 43.21 ADCJ0VMONVDCR2 Register Contents

Bit Position	Bit Name	Function
7 to 1	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
0	VDE2	Voltage Divider Enable (Voltage Dividing Resistor Control) This bit is used to control the voltage dividing resistor together with the VDE1 bit in ADCJnVMONVDCR1. For details, see "Table 43.22 Resistance Voltage Divider and Pull-down Control Setting Table"

CAUTIONS

1. To prevent a malfunction, this register has restrictions for updating settings. For restrictions on updating settings, see "**Error! Reference source not found. Error! Reference source not found.**".
2. Do not perform A/D conversion with the setting of ADCJnVMONVDCR1.VDE1 or ADCJnVMONVDCR2.VDE2 = 01B or 10B.

Table 43.23 Resistance Voltage Divider and Pull-down Control Setting Table

VDE1	VDE2	Resistance voltage divide	Pull-Down
0	0	OFF	ON
0	1	OFF	OFF
1	0	OFF	OFF
1	1	ON	OFF

43.3.3 ADCJ Specific Registers (Virtual Channel, Control, Safety-related)

43.3.3.1 ADCJnVCRj — Virtual Channel Register j

ADCJnVCRj is a 32-bit readable and writable register to make settings for each virtual channel.

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VCULLMTBS[3:0]				WTTS[3:0]				—	—	—	GTMENT	GTMTAG[3:0]			
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	CNVCLS[3:0]			MPXV[2:0]				ADIE	—	GCTRL[5:0]					
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 43.24 ADCJnVCRj Register Contents

Bit Position	Bit Name	Function
31 to 28	VCULLMTBS[3:0]	Upper/Lower Limit Check Table Register Select Select an upper/lower limit check table register to be compared. 0$_H$: Disable 1$_H$: VCULLMTBR0 is chosen 2$_H$: VCULLMTBR1 is chosen 3$_H$: VCULLMTBR2 is chosen 4$_H$: VCULLMTBR3 is chosen 5$_H$: VCULLMTBR4 is chosen 6$_H$: VCULLMTBR5 is chosen 7$_H$: VCULLMTBR6 is chosen 8$_H$: VCULLMTBR7 is chosen Other than above: Setting prohibited (same as 0$_H$).
27 to 24	WTTS[3:0]	Wait Time Table Select 0$_H$: Disabled 1$_H$: WAITTR0 is chosen. 2$_H$: WAITTR1 is chosen. 3$_H$: WAITTR2 is chosen. 4$_H$: WAITTR3 is chosen. 5$_H$: WAITTR4 is chosen. 6$_H$: WAITTR5 is chosen. 7$_H$: WAITTR6 is chosen. 8$_H$: WAITTR7 is chosen. Other than above: Setting prohibited (same as 0$_H$).
23 to 21	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
20	GTMENT	GTM Entry 0: Entry disabled 1: Entry enabled Select whether to perform entry to the GTM (Generic timer module). Entry is available only in scan groups enabled by GTMENTSGxE in GTMENTSGER.
19 to 16	GTMTAG[3:0]	GTM-TAG When entry is requested to ~~DFE~~GTM, entry is performed to the channel of ~~DFE~~GTM for which the ~~DF~~GTMTAG[3:0] TAG is set. If multiple channels match, entry is performed to them. ~~When entry is requested to ASF, entry is performed to the channel of ASF corresponding to DFTAG[3:0]. When making an entry request to ASF, set a DFTAG[3:0] value unique to each~~

		~~VCRn. If a duplicated value is set in DFTAG[3:0], the cumulative value of ASF is not guaranteed.~~
15	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
14 to 11	CNVCLS[3:0]	Conversion Type 0 H: Normal A/D conversion 1 H: Hold value A/D conversion 2 H: Normal A/D conversion at extended sampling cycle 3 H: ADcore self-diagnosis A/D conversion 4 H: Addition mode A/D conversion 5 H: MPX normal A/D conversion 6 H: MPX addition mode A/D conversion 7 H: Pin level self-diagnosis A/D conversion 8 H: A/D conversion in wiring-break detection mode 1 9 H: A/D conversion in wiring-break detection mode 2 (physical channel IO pull-down) A H: A/D conversion in wiring-break detection mode 2 (physical channel IO pull-up) B H: Self-diagnosis A/D conversion in wiring-break detection mode 1 C H: Self-diagnosis A/D conversion in wiring-break detection mode 2 (physical channel IO pull-down) D H: Self-diagnosis A/D conversion in wiring-break detection mode 2 (physical channel IO pull-up) E H: A/D conversion of A/D conversion data path diagnosis (ADVAL mode) F H: Reserved ~~(Normal A/D conversion)~~
10 to 8	MPXV[2:0]	These bits are used to set the channel of external MPX to be transferred to the external analog multiplexer.
7	ADIE	Virtual Channel End Interrupt Enable 0: INT_ADx is not output at the end of virtual channel n in SGx. 1: INT_ADx is output at the end of virtual channel n in SGx. For details of the relationship between ADIE in ADCJnSGCRx and ADIE in ADCJnVCR~~#~~j, see "**Error! Reference source not found. Error! Reference source not found.**" .
6	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
5 to 0	GCTRL[5:0]	General Control Set A/D conversion for each conversion mode. Normal A/D conversion (CNVCLS[3:0] = 0H) GCTRL[5:2]: Set the physical channel group number. 0 H: Group number of physical channels ANn00 to ANn03 1 H: Group number of physical channels ANn10 to ANn13 2 H: Group number of physical channels ANn20 to ANn23 3 H: Group number of physical channels ANn30 to ANn33 4 H: Group number of physical channels ANn40 to ANn43 5 H: Group number of secondary supply voltage monitor for VCC, E0VCC, ISOVDD & AWOVDD 6 H: Group number of physical channels ANn50 to ANn53(*1) 7 H: Group number of physical channels ANn60 to ANn63(*1) 8 H: Group number of physical channels ANn70 to ANn71(*1) : 9 H - F H: Reserved. GCTRL[1:0]: Set the physical sub channel number. 0 H: Sub channel 0 of the physical channel group specified by GCTRL[5:2] 1 H: Sub channel 1 of the physical channel group specified by GCTRL[5:2] 2 H: Sub channel 2 of the physical channel group specified by GCTRL[5:2] 3 H: Sub channel 3 of the physical channel group specified by GCTRL[5:2] Example of setting: To specify ANn10, set GCTRL[5:2]: = 1H and GCTRL[1:0] = 0H. To specify ANn62, set GCTRL[5:2]: = 7H and GCTRL[1:0] = 2H. Hold value A/D conversion (CNVCLS[3:0] = 1H)

GCTRL[5:3]: Set 000B.
GCTRL[2:0]: Set the T&H channel number.
0 H: The T&H0 hold value is A/D converted.
1 H: The T&H1 hold value is A/D converted.
2 H: The T&H2 hold value is A/D converted.
3 H: The T&H3 hold value is A/D converted.
4 H: Setting prohibited
5 H: Setting prohibited
6 H: Setting prohibited
7 H: Setting prohibited

Formatted: Pattern: Clear

Formatted: Pattern: Clear

Normal A/D conversion (CNVCLS[3:0] = 2H) with extended sampling period
Make the same settings as normal A/D conversion (CNVCLS[3:0] = 0H).

ADcore self-diagnosis A/D conversion (CNVCLS[3:0] = 3H)
GCTRL[5]: Set 0.
GCTRL[4:0]: Set the ADcore self-diagnosis voltage level.
10 H: AVREFH × 1
0C H: AVREFH × 3/4
08 H: AVREFH × 1/2
04 H: AVREFH × 1/4
00 H: AVREFH × 0
Other than above: Setting prohibited ~~(AVREFH × 0)~~

When the CNVCLS[3:0] value is set to the following value (CNVCLS[3:0] = 4H to DH), make the same settings as normal A/D conversion (CNVCLS[3:0] = 0H).
For addition mode A/D conversion (CNVCLS[3:0] = 4H)
For MPX normal A/D conversion (CNVCLS[3:0] = 5H)
For MPX addition mode A/D conversion (CNVCLS[3:0] = 6H)
For pin level self-diagnosis A/D conversion (CNVCLS[2:0] = 7H)
For A/D conversion in wiring-break detection mode 1 (CNVCLS[3:0] = 8H)
For A/D conversion in wiring-break detection mode 2 (physical channel IO pull-down) (CNVCLS[3:0] = 9H)
For A/D conversion in wiring-break detection mode 2 (physical channel IO pull-up) (CNVCLS[3:0] = AH)
For self-diagnosis A/D conversion in wiring-break detection mode 1 (CNVCLS[3:0] = BH)
For self-diagnosis A/D conversion in wiring-break detection mode 2 (physical channel IO pull-down) (CNVCLS[3:0] = CH)
For self-diagnosis A/D conversion in wiring-break detection mode 2 (physical channel IO pull-up) (CNVCLS[3:0] = DH)

A/D conversion data path diagnosis A/D conversion (ADVAL mode) (CNVCLS[3:0] = EH)
GCTRL[5:1]: Set 0.
GCTRL[0]
0: Fix the A/D conversion data from ADCore to AAAH.
1: Fix the A/D conversion data from ADCore to 555H.

Note 1. Max resolution is 10-bit.

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CAUTION

To prevent a malfunction, there is the limitations of setting update in this register.
For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**. But when scan group is terminated, clearing ADIE to 0 isn't included in the limitations.

43.3.3.2 ADCJnPWDVCR — PWM-Diag Virtual Channel Register

ADCJnPWDVCR is a 32-bit readable register to control PWM-Diag virtual channels.

Because a value set by the register of another macro PWSC is input as a PVCR_VALUE[17:0] value in the control by the PWM-Diag function, ADCJnPWDVCR is an insubstantial register.

Value after reset 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	WTTS[3:0]			
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MPXE	MPXV[2:0]			VCULLMTBS[3:0]				—	—	GCTRL[5:0]					
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 43.25 ADCJnPWDVCR Register Contents

Bit Position	Bit Name	Function
31 to 20	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
19 to 16	WTTS[3:0]	Wait Time Table Select 0 H: Disabled 1 H: WAITTR0 is chosen. 2 H: WAITTR1 is chosen. 3 H: WAITTR2 is chosen. 4 H: WAITTR3 is chosen. 5 H: WAITTR4 is chosen. 6 H: WAITTR5 is chosen. 7 H: WAITTR6 is chosen. 8 H: WAITTR7 is chosen. Other than above: Setting prohibited.
15	MPXE	MPX Enable When operating this this bit, set MPXE in the register of the PWSD module. 0: Normal A/D conversion is performed. The MPXV[2:0] value is not transferred to the output pin PVCR_MUXCUR[2:0]. No wait is inserted before A/D conversion starts. 1: MPX normal A/D conversion is performed. The MPXV[2:0] value is transferred to the output pin PVCR_MUXCUR[2:0]. A wait is inserted before A/D conversion starts.
14 to 12	MPXV[2:0]	MPX Value When operating these bits, set MPXV[2:0] in the register of the PWSD module. Use this bit to select an MPX channel of the external analog multiplexer.
11 to 8	VCULLMTBS[3:0]	Upper/Lower Limit Check Table Register Select When operating these bits, set VCULLMTBS[3:0] in the register of the PWSD module. Select the upper/lower limit check table register to be compared. 0 H: Disabled 1 H: VCULLMTBR0 is chosen. 2 H: VCULLMTBR1 is chosen. 3 H: VCULLMTBR2 is chosen. 4 H: VCULLMTBR3 is chosen. 5 H: VCULLMTBR4 is chosen. 6 H: VCULLMTBR5 is chosen. 7 H: VCULLMTBR6 is chosen.

		8 H: VCULLMTBR7 is chosen. Other than above: Setting prohibited.
7 to 6	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
5 to 0	GCTRL[5:0]	When operating these bits, set GCTRL[5:0] in the register of the PWSC module. GCTRL[5:2]: Set the physical channel group number. GCTRL[1:0]: Set the physical sub channel number. Example of setting: To specify ANn10, set GCTRL[5:2]: = 1H and GCTRL[1:0] = 0H. To specify ANn62, set GCTRL[5:2]: = 7H and GCTRL[1:0] = 2H.

CAUTION

When using MPX normal A/D conversion, be sure to insert a wait.

NOTE

1. VCULLMTBS[3:0] in PWDVCR and VCULLMTBS[3:0] in VCRn are the same function.
2. PVCR_VALUE[17:0] is allocated to the following bits.
   PVCR_VALUE[17:14]=WTTS[3:0]
   PVCR_VALUE[13]=MPXE
   PVCR_VALUE[12:10]=MPXV[2:0]
   PVCR_VALUE[9:6]= VCULLMTBS[3:0]
   PVCR_VALUE[5:0]= GCTRL[5:0]

43.3.3.3 ADCJnDRj — Data Register j

ADCJnDRj is a 16-bit read-only register to store A/D conversion value.

Value after reset 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRi[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 43.26 ADCJnDRj Register Contents

Bit Position	Bit Name	Function
15 to 0	DRi[15:0]	Data Register These bits store A/D conversion result data ADCJnVCRj

The ADCJnDRj format varies as shown below with the settings of data format (ADCJnADCR2.DFMT[2:0]), addition mode (ADCJnVCRj.CNVCLS[3:0]), and addition count (ADCJnADCR2.ADDNT).

How to round the resolution from 12 bits to 10 bits is shown below.

	12-bit A/D conversion value			10-bit A/D conversion value
	[11:2]	[1]	[0]	[9:0]
Without addition (convert once)	$3FF_H$	Round down	Round down	12-bit A/D conversion value [11:2]
	$3FE_H$ to 000_H	Added to [11:2]		12-bit A/D conversion value [11:2] + 12-bit A/D conversion value [1]

	12-bit A/D conversion value			10-bit A/D conversion value
	[12:2]	[1]	[0]	[10:0]
Addition twice (convert twice)	$7FF_H$	Round down	Round down	12-bit A/D conversion value [12:2]
	$7FE_H$ to 000_H	Added to [12:2]		12-bit A/D conversion value [12:2] + 12-bit A/D conversion value [1]

	12-bit A/D conversion value			10-bit A/D conversion value
	[13:2]	[1]	[0]	[11:0]
Addition four times (convert 4 times)	FFF_H	Round down	Round down	12-bit A/D conversion value [13:2]
	FFE_H to 000_H	Added to [13:2]		12-bit A/D conversion value [13:2] + 12-bit A/D conversion value [1]

The storage format to ADCJnDRj by the combination of the data format (ADCJnADCR2.DFMT [2:0]), the addition mode (ADCJnVCRj.CNVCLS [3:0]) and the addition number of steps (ADCJnADCR2.ADDNT) is described below.

(1) The format when reading from the P-Bus

For Resolution 12 bit signed fixed-point format (DFMT[2:0] = 000)

Addition	CNVCLS	ADDNT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Once	≠4H, 6H	—	S													0	0	0
Twice	= 4H, 6H	0	S														0	0
4 times		1	S															0

Position of decimal point

For Resolution 12 bit signed integer format (DFMT[1:0] = 001)

Addition	CNVCLS	ADDNT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Once	≠ 4H, 6H	—	S	S	S	S												
Twice	= 4H, 6H	0	S	S	S													
4 times		1	S	S														

Position of decimal point

For Resolution 12 bit unsigned fixed-point format (DFMT[1:0] = 010)

Addition	CNVCLS	ADDNT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Once	≠ 4H, 6H	—													0	0	0	0
Twice	= 4H, 6H	0														0	0	0
4 times		1															0	0

Position of decimal point

For Resolution 10 bit unsigned fixed-point format (DFMT[1:0] = 011)

Addition	CNVCLS	ADDNT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Once	≠ 4H, 6H	—											0	0	0	0	0	0
Twice	= 4H, 6H	0												0	0	0	0	0
4 times		1													0	0	0	0

Position of decimal point

S	: Sign bit (always 0)
0	: Zero extension

(2) The format of the data transferred to the GTM

For unsigned 12 bit fixed-point format (DFMT[2:0] = 000/010/011)

Addition	CNVCLS	ADDNT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Once	≠ 4H, 6H	—	S													0	0	0
Twice	= 4H, 6H	0	S														0	0
4 times		1	S															0

Position of decimal point

S	: Sign bit (always 0)
0	: Zero extension
	: When DFMT is 11, it's fixed to zero.

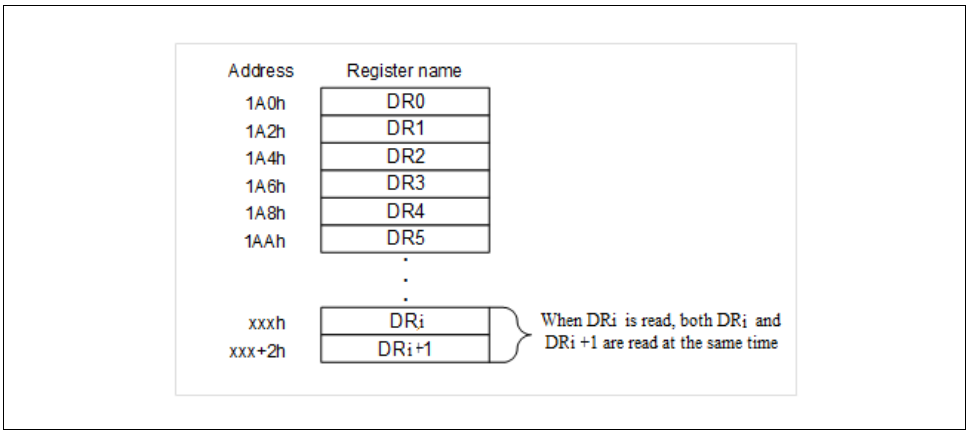

Figure 43-4 ADCJnDRj Read Specifications

So, when both DR_i and DR_{i+1} are read at the same time by CPU order, set the read and clear enable bit valid(ADCJnSFTCR.RDCLRE=1).

When whether DR_i or DR_{i+1} is read by CPU order, the other DRi is cleared. So, set the read and clear enable bit invalid(ADCJnSFTCR.RDCLRE=0).

And when whether DR_i or DR_{i+1} is read by CPU order, it is prohibited to use the overwrite function. So, disable the overwrite function (*1).

*1: When all of the following three conditions are met, the overwrite function is disabled.

(1) Do not compare the expected value of the WFLAG bit in ADCJnDIRj.

(2) Do not judge an error using the OWE bit in ADCJnOWER.

(3) Set the OWEIE bit in ADCJnSFTCR to 0 (disabled).

Error! Use the Home tab to apply 見出し 1 to the text that you want to appear here.

NOTE

1. j = 0, 1, 2, …, 63; i = 0, 2, 4, …(even number)

2. All registers are read with 32-bit width. Therefore, if either DRi or DRi+1 is read as 16-bit data by a CPU instruction, the other DRi+1 or DRi is also cleared.

3. When the read and clear enable bit is valid(ADCJnSFTCR.RDCLRE = 1), ADCJnDIRj is cleared by reading ADCJnDRj.

4. The overwrite function operates independently of the read and clear function. When whether DRi or DRi+1 is read by CPU order, the other ADCJnDRj.WFLAG is cleared. So it is prohibited to use the overwrite function when whether DRi or DRi+1 is read by CPU order.

43.3.3.4 ADCJnPWDDR — PWM-Diag Data Register

ADCJnPWDDR is a 16-bit read-only register to store A/D conversion value of PWM-Diag.

When reading ADCJnPWDDR, set the read and clear enable bit (ADCJnSFTCR.RDCLRE = 1).

No overwrite error of ADCJnPWDDR is generated.

No upper/lower limit error of ADCJnPWDDR is generated.

Value after reset 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PWDDR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 43.27 ADCJnPWDDR Register Contents

Bit Position	Bit Name	Function
15 to 0	PWDDR[15:0]	PWM-Diag Data Ragister These bits are used to store the A/D conversion result data for the PWM-Diag.

NOTE

1. The ADCJnPWDDR format varies with the setting of data format (ADCJnADCR2.DFMT[2:0]). For details, check **Error! Reference source not found.Error! Reference source not found.**.

[For internal use only]

The PWM-Diag performs only normal A/D conversion or MPX normal A/D conversion.
Addition mode is not provided.

43.3.3.5 ADCJnDIRj — Data Supplementary Information Register j

ADCJnDIRj is a 32-bit read-only register to store supplementary information of ADCJnDRj and A/D conversion value. When reading ADCJnDIRj as 16-bit data by CPU order, read ADCJnDIRj according to the 16-bit read restriction of 43.3.3.3 ADCJnDRj — Data Register j.

Value after reset 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MPXE	MPXV[2:0]			—	IDEF	WFLAG	PRTY	—	—	ID[5:0]					
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADCJnDRj[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 43.28 ADCJnDIRj Register Contents

Bit Position	Bit Name	Function
31	MPXE	MPX Enable Flag 0: The MPX function is not used. 1: The MPX function is used.
30 to 28	MPXV[2:0]	These bits are used to store the MPX value transferred to the external analog multiplexer.
27	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
26	IDEF	ID Error 0: There is an error. 1: There is no error.
25	WFLAG	Write Flag Setting and clearing conditions 0: Clearing conditions Reading ADCJnDRj or ADCJnDIRj 1: Setting condition Storing A/D conversion value in ADCJnDRj
24	PRTY	Even parity bit of ADCJnDRj[15:0], ID[5:0], IDEF, MPXV[2:0], and MPXE
23 to 22	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
21 to 16	ID[5:0]	ID Information The executed GCTRL[5:0] value in ADCJnVCRj is stored. When normal A/D conversion (ADCJnVCRj.CNVCLS[3:0] = 0H) is performed, the ID[5:2] value means physical channel group and the ID[1:0] value means physical sub channel. When hold value A/D conversion (ADCJnVCRj.CNVCLS[3:0] = 1H) is performed, the T&H whose hold value was A/D converted is stored in ID[2:0]. 0H: The hold value of T&H0 is A/D converted. 1H: The hold value of T&H1 is A/D converted. 2H: The hold value of T&H2 is A/D converted. 3H: The hold value of T&H3 is A/D converted. The ID bits value other than above is always 0.

		When normal A/D conversion (ADCJnVCRj.CNVCLS[3:0] = 2H) at the extended sampling cycle is performed, the same information as normal A/D conversion (ADCJnVCRj.CNVCLS[3:0] = 0H) is stored. When ADcore self-diagnosis A/D conversion (ADCJnVCRj.CNVCLS[3:0] = 3H) is performed, the ADcore self-diagnosis level is stored in ID[4:0]. 10H: AVREFH × 1 0CH: AVREFH × 3/4 08H: AVREFH × 1/2 04H: AVREFH × 1/4 00H: AVREFH × 0 The ID bits value other than above is always 0. When the ADCJnVCRj.CNVCLS[3:0] value is set to the following value (ADCJnVCRj.CNVCLS[3:0] = 4H to EH), the same information as normal A/D conversion (ADCJnVCRj.CNVCLS[3:0] = 0H) is stored. For addition mode A/D conversion (ADCJnVCRj.CNVCLS[3:0] = 4H) For MPX normal A/D conversion (ADCJnVCRj.CNVCLS[3:0] = 5H) For MPX addition mode A/D conversion (ADCJnVCRj.CNVCLS[3:0] = 6H) For pin level self-diagnosis A/D conversion (ADCJnVCRj.CNVCLS[2:0] = 7H) For A/D conversion in wiring-break detection mode 1 (ADCJnVCRj.CNVCLS[3:0] = 8H) For A/D conversion in wiring-break detection mode 2 (physical channel IO pull-down) (ADCJnVCRj.CNVCLS[3:0] = 9H) For A/D conversion in wiring-break detection mode 2 (physical channel IO pull-up) (ADCJnVCRj.CNVCLS[3:0] = AH) For self-diagnosis A/D conversion in wiring-break detection mode 1 (ADCJnVCRj.CNVCLS[3:0] = BH) For self-diagnosis A/D conversion in wiring-break detection mode 2 (physical channel IO pull-down) (ADCJnVCRj.CNVCLS[3:0] = CH) For self-diagnosis A/D conversion in wiring-break detection mode 2 (physical channel IO pull-up) (ADCJnVCRj.CNVCLS[3:0] = DH) When A/D conversion data path diagnosis (ADVAL mode) (ADCJnVCRj.CNVCLS[3:0] = EH) is performed, the executed GCTRL[5:0] value in ADCJnVCRj is stored.
15 to 0	ADCJnDRj[15:0]	It is ADCJnDRj itself. Refer to 43.3.3.3 ADCJnDRj — Data Register j for detail.

CAUTION

1. When ADCJnDIRj is not used, set the read and clear valid or invalid according to the read constraint of 43.3.3.3 ADCJnDRj — Data Register j.

NOTES

1. The IDEF bit is cleared to 0 in the initial status or when ADCJnDRj or ADCJnDIRj is read and cleared or when an ID error occurs. The IDEF bit is set to 1 when an ID error is not detected during A/D conversion.

   The IDEF bit is set to 1 at the same time as when the A/D conversion result is stored in the data register (ADCJnDRj).
2. The WFLAG bit is cleared to 0 by reading ADCJnDRj or ADCJnDIRj regardless of the read and clear enable (ADCJnSFTCR.RDCLRE) bit value.
3. The PRTY bit and the ADCJnDRj[15:0] bits are cleared by reading ADCJnDRj or ADCJnDIRj when the read and clear enable bit is set (ADCJnSFTCR.RDCLRE = 1).

4. ADCJnDRj[15:0] bit is ADCJnDRj register itself. So, when the read and clear is valid (ADCJnSFTCR.RDCLRE=1), all bits of ADCJnDIRj is cleared by read ADCJnDRj register.

5. The MPXE bit is set to 1 when the MPX is in use (ADCJnVCRj.CNVCLS[3:0] = 5H or 6H) in the executed virtual channel.

6. The MPXV bit of the executed virtual channel is stored in the MPXV[2:0] bits.

7. All registers are read with 32-bit width. Therefore, when DR_i is read, the other

DR_{i+1} is cleared at the same time. So when the read and clear is valid (ADCJnSFTCR.RDCLRE=1), all bits of $ADCJnDIR_j$ and $ADCJnDIR_{j+1}$ is cleared at the same time.

43.3.3.6 ADCJnPWDDIR — PWM-Diag Data Supplementary Information Register

ADCJnPWDDIR is a 32-bit read-only register to store supplementary information of ADCJnPWDDR and A/D conversion values. Read this register with a 16-bit or 32-bit width.

When reading ADCJnPWDDIR as 16-bit data by CPU order, read ADCJnPWDDIR according to the 16-bit read restriction of 43.3.3.4 ADCJnPWDDR - PWM-Diag Data Register.

No overwrite error of ADCJnPWDDIR is generated.

No upper/lower limit error of ADCJnPWDDIR is generated.

Value after reset 0000 0000H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MPXE	MPXV[2:0]			—	IDEF	WFLAG	PRTY	—	—	ID[5:0]					
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADCJnPWDDR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 43.29 ADCJnPWDDIR Register Contents

Bit Position	Bit Name	Function
31	MPXE	MPX Enable Flag 0: The MPX function is not used. 1: The MPX function is used.
30 to 28	MPXV[2:0]	These bits are used to store the MPX value transferred to the external analog multiplexer.
27	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
26	IDEF	ID error 0: There is an error. 1: There is no error.
25	WFLAG	Write Flag Setting and clearing conditions 0: Clearing condition Reading PWDDR or PWDDIR 1: Setting condition Storing A/D conversion value in PWDDR
24	PRTY	Even parity bit of ADCJnPWDDR[15:0], ID[5:0], IDEF, MPXV[2:0], and MPXE
23 to 22	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
21 to 16	ID[5:0]	ID Information The executed GCTRL[5:0] value in ADCJnPWDVCR is stored. The ID[5:2] value means physical channel group. The ID[1:0] value means physical sub channel.
15 to 0	ADCJnPWDDR[15:0]	It is ADCJnPWDDR itself. Refer to 43.3.3.4 ADCJnPWDDR - PWM-Diag Data Register for detail.

NOTES

1. The IDEF bit is cleared to 0 in the initial status or when ADCJnPWDDR or ADCJnPWDDIR is read and cleared or when an ID error occurs. The IDEF bit is set to 1 when an ID error is not detected during A/D conversion.
   The IDEF bit is set to 1 at the same time as when the A/D conversion result is stored in the data register (ADCJnPWDDR).
2. The WFLAG bit is cleared to 0 by reading ADCJnPWDDR or ADCJnPWDDIR regardless of the read and clear enable (ADCJnSFTCR.RDCLRE) bit value.
3. The PRTY bit and the ADCJnPWDDR[15:0] bits are cleared by reading ADCJnPWDDR or ADCJnPWDDIR when the read and clear enable bit is set (ADCJnSFTCR.RDCLRE = 1).
4. ADCJnPWDDR[15:0] bit is ADCJnPWDDR register itself. So, when the read and clear is valid (ADCJnSFTCR.RDCLRE=1), all bits of ADCJnPWDDIR is cleared by read ADCJnPWDDR register.
5. The MPXE bit is set to 1 when the MPX is in use (MPXE = 1) in the executed ADCJnPWDVCR.
6. The MPXV bit value in ADCJnPWDVCR is stored in the MPXV[2:0] bits.

43.3.3.7 ADCJnADHALTR — A/D Halt Register

ADCJnADHALTR is an 8-bit write-only register that forcibly terminates the A/D conversion. The register bits are always read as 0.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	HALT
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	W

Table 43.30 ADCJnADHALTR Register Contents

Bit Position	Bit Name	Function
7 to 1	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
0	HALT	Halt All scan groups and all AD timers are halted and initialized, and the ADC changes to the idle state. Writing 0: Scan groups and timers are not halted. Writing 1: Scan groups and timers are halted.

43.3.3.8 ADCJnADCR1 — AD Control Register 1

ADCJnADCR1 is an 8-bit readable/writable register for ADC common control. ADCJnADCR1 is initialized to 00_H at reset.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	SUSMTD[1:0]	
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R/W	R/W

Table 43.31 ADCJnADCR1 Register Contents

Bit Position	Bit Name	Function
7 to 2	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
1, 0	SUSMTD[1:0]	Suspend Method These bits select the suspend method when a higher-priority scan group interrupts a lower-priority scan group. Synchronous suspend: If a request from a higher-priority SG is present while a lower-priority SG is being processed, processing for the lower-priority SG is suspended after the ongoing virtual channel processing is completed, and then processing for the higher-priority SG is executed. After processing for the higher-priority SG is completed, the suspended virtual channel processing for the lower-priority SG is resumed. Asynchronous suspend: If a request from a higher-priority SG is present while a lower-priority SG is being processed, the ongoing virtual channel processing is immediately suspended, and then processing for the higher-priority SG is executed. After processing for the higher-priority SG is completed, the suspended virtual channel processing for the lower-priority SG is resumed. 0_H: Synchronous suspend 1_H: Asynchronous suspend when a higher-priority SG interrupts SG0, Synchronous suspend when a higher-priority SG interrupts a lower-priority SG (except for SG0) 2_H: Asynchronous suspend 3_H: Setting prohibited For details, see **Figure 43.11** and **Figure 43.12**.

CAUTION

To prevent a malfunction, there is the limitations of setting update in this register.
For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.3.3.9 ADCJnMPXCURCR — MPX Current Control Register

ADCJnMPXCURCR is an 8-bit readable/writable register that controls the ADCJnMPXCURR format.
ADCJnMPXCURCR is initialized to 00_H at reset.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	MSKCFMT[3:0]			
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W

Table 43.32 ADCJnMPXCURCR Register Contents

Bit Position	Bit Name	Function
7 to 4	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
3 to 0	MSKCFMT[3:0]	MSKC Format Specification These bits specify the MSKC[15:0] format of ADCJnMPXCURR. MSKCFMT[3] 0: MSKC[15:12] = 0000 1: MSKC[15:12] = 1111 MSKCFMT[2] 0: MSKC[11:8] = 0000 1: MSKC[11:8] = 1111 MSKCFMT[1] 0: MSKC[7:4] = 0000 1: MSKC[7:4] = 0001 MSKCFMT[0] 0: MSKC[3:0] = 0000 1: MSKC[3:0] = 1111

CAUTION

To prevent a malfunction, there is the limitations of setting update in this register.
For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.3.3.10 ADCJnMPXINTER — MPX Interrupt Enable Register

ADCJnMPXINTER is an 8-bit readable/writable register that controls the interrupt (ADMPXIn) output.
ADCJnMPXINTER is initialized to 00_H at reset.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	ADMPXIE
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W

Table 43.33 ADCJnMPXINTER Register Contents

Bit Position	Bit Name	Function
7 to 1	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
0	ADMPXIE	MPX interrupt enable This bits controls the ADMPXIn interrupt (ADMPXIn) output. 0: ADMPXIn is not output 1: ADMPXIn is output

CAUTION

To prevent a malfunction, there is the limitations of setting update in this register.
For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.3.3.11 ADCJnMPXCURR — MPX Current Register

ADCJnMPXCURR is a 32-bit read-only register that stores the MPX value for an external analog multiplexer.
ADCJnMPXCURR is initialized to 0000 0000_H at reset.

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSKC[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MPXCMD[7:0]								—	—	—	MPXCUR[4:0]				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 43.34 ADCJnMPXCURR Register Contents

Bit Position	Bit Name	Function
31 to 16	MSKC[15:0]	Mask Control The format depends on the MSKCFMT[3:0] setting of ADCJnMPXCURCR. For details, see **Section 43.3.3.9, ADCJnMPXCURCR — MPX Current Control Register**.
15 to 8	MPXCMD[7:0]	SPI Communication Command Information A command information register to control an external analog multiplexer by using SPI communication. When a virtual channel in which CNVCLS[2:0] in ADCJnVCRj is set to 5_H or 6_H is started, the MPXCMD[7:0] value in ADCJnMPXCMDR is transferred to MPXCMD[7:0] in ADCJnMPXCURR.
7 to 5	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
4 to 0	MPXCUR[4:0]	Current MPX Value When a virtual channel for which CNVCLS[2:0] in ADCJnVCRj is set to 5_H or 6_H is started, GCTRL[4:0] in ADCJnVCRj is transferred to MPXCUR[4:0].At this time, an interrupt request to the INTC or a DMA transfer request is generated. The DMAC transfers ADCJnMPXCURR to Pn or PSRn of the I/O port or to CSIHnTX0H of CSIH, enabling the MPX value to be sent to an external analog multiplexer. When Pn is used, transfer the lower 5 bits. When PSRn is used, transfer the MPX value as a 32-bit value. This enables you to rewrite only the necessary ports by using the format control in MSKC[15:0]. When transferring the value to CSIHnTX0H, transfer the lower 16 bits. For details, see **Section 43.4.4.4, Normal A/D Conversion with the MPX and Normal A/D Conversion with the MPX in Addition Mode**.

43.3.3.12 ADCJnMPXOWR — MPX Optional Wait register

ADCJnMPXOWR is an 8-bit readable/writable register that specifies the wait time to be inserted for an external analog multiplexer. ADCJnMPXOWR is initialized to 00_H at reset.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	MPXOW[3:0]			
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W

Table 43.35 ADCJnMPXOWR Register Contents

Bit Position	Bit Name	Function
7 to 4	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
3 to 0	MPXOW[3:0]	MPX Optional Wait These bits specify the wait time to be inserted before an A/D conversion is started after a virtual channel for which CNVCLS[2:0] in ADCJnVCRj is 5_H or 6_H is started. 0_H: 0 µs 1_H: 1 µs 2_H: 2 µs 3_H: 3 µs 4_H: 4 µs 5_H: 5 µs 6_H: 6 µs 7_H: 7 µs 8_H: 8 µs 9_H: 9 µs A_H: 10 µs B_H to F_H: Setting prohibited For details, see **Section 43.4.4.4, Normal A/D Conversion with the MPX and Normal A/D Conversion with the MPX in Addition Mode**.

CAUTION

To prevent a malfunction, there is the limitations of setting update in this register.
For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.3.3.13 ADCJnMPXCMDR — MPX Command Information Register

ADCJnMPXCMDR is an 8-bit readable/writable register that stores SPI communication command information to be transferred to an external analog multiplexer. ADCJnMPXCMDR is initialized to 00_H at reset.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	MPXCMD[7:0]							
Value after reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 43.36 ADCJnMPXCMDR Register Contents

Bit Position	Bit Name	Function
7 to 0	MPXCMD[7:0]	SPI Communication Command Information These bits store command information for controlling an external analog multiplexer by using the SPI communication. When a virtual channel for which CNVCLS[2:0] in ADCJnVCRj is set to 5_H or 6_H is started, MPXCMD[7:0] in ADCJnMPXCMDR is transferred to MPXCMD[7:0] in ADCJnMPXCURR and it can be read by ADCJnMPXCURR together with MPXCUR[4:0].

CAUTION

To prevent a malfunction, there is the limitations of setting update in this register.
For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.3.3.14 ADCJnADCR2 — AD Control Register 2

ADCJnADCR2 is an 8-bit readable/writable register for ADC common control.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	DFMT[1:0]		—	—	—	ADDNT
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R	R	R	R/W

Table 43.37 ADCJnADCR2 Register Contents

Bit Position	Bit Name	Function
7 to 6	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
5 to 4	DFMT[1:0]	Data Format 00: Signed 12bit fixed-point format 01: Signed 12bit integer format 10: Unsigned 12bit fixed-point format 11: Unsigned 10bit fixed-point format For data transferred to the DFE.GTM and ASF, it is always signed fixed-point format regardless of the DFMT setting. For details of data format, see **Section 43.3.3.2, ADCJnPWDVCR — PWM-Diag Virtual Channel** Register

ADCJnPWDVCR is a 32-bit readable register to control PWM-Diag virtual channels.
Because a value set by the register of another macro PWSC is input as a PVCR_VALUE[17:0] value in the control by the PWM-Diag function, ADCJnPWDVCR is an insubstantial register.

0_H

28	27	26	25	24	23	22	21	20	19	18	17	16
—	—	—	—	—	—	—	—	—	WTTS[3:0]			
0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R

12	11	10	9	8	7	6	5	4	3	2	1	0
	VCULLMTBS[3:0]				—	—	GCTRL[5:0]					
0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R

Table 43.25 ADCJnPWDVCR Register Contents

Bit Position	Bit Name	Function
31 to 20	—	Reserved When read, the value after reset is returned. When writ
19 to 16	WTTS[3:0]	Wait Time Table Select 0 H: Disabled 1 H: WAITTR0 is chosen. 2 H: WAITTR1 is chosen. 3 H: WAITTR2 is chosen.

		4 H: WAITTR3 is chosen. 5 H: WAITTR4 is chosen. 6 H: WAITTR5 is chosen. 7 H: WAITTR6 is chosen. 8 H: WAITTR7 is chosen. Other than above: Setting prohibited.
15	MPXE	MPX Enable When operating this this bit, set MPXE in the register of the PWSD module. 0: Normal A/D conversion is performed. The MPXV[2:0] value is not transferred to the output pin PVCR_MUXCUR[2:0]. No wait is inserted before A/D conversion starts. 1: MPX normal A/D conversion is performed. The MPXV[2:0] value is transferred to the output pin PVCR_MUXCUR[2:0]. A wait is inserted before A/D conversion starts.
14 to 12	MPXV[2:0]	MPX Value When operating these bits, set MPXV[2:0] in the register of the PWSD module. Use this bit to select an MPX channel of the external analog multiplexer.
11 to 8	VCULLMTBS[3:0]	Upper/Lower Limit Check Table Register Select When operating these bits, set VCULLMTBS[3:0] in the register of the PWSD module. Select the upper/lower limit check table register to be compared. 0 H: Disabled 1 H: VCULLMTBR0 is chosen. 2 H: VCULLMTBR1 is chosen. 3 H: VCULLMTBR2 is chosen. 4 H: VCULLMTBR3 is chosen. 5 H: VCULLMTBR4 is chosen. 6 H: VCULLMTBR5 is chosen. 7 H: VCULLMTBR6 is chosen. 8 H: VCULLMTBR7 is chosen. Other than above: Setting prohibited.
7 to 6	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
5 to 0	GCTRL[5:0]	When operating these bits, set GCTRL[5:0] in the register of the PWSC module. GCTRL[5:2]: Set the physical channel group number. GCTRL[1:0]: Set the physical sub channel number. Example of setting: To specify ANn10, set GCTRL[5:2]: = 1H and GCTRL[1:0] = 0H. To specify ANn62, set GCTRL[5:2]: = 7H and GCTRL[1:0] = 2H.

CAUTION

When using MPX normal A/D conversion, be sure to insert a wait.

NOTE

1. VCULLMTBS[3:0] in PWDVCR and VCULLMTBS[3:0] in VCRn
2. PVCR_VALUE[17:0] is allocated to the following bits.
   PVCR_VALUE[17:14]=WTTS[3:0]
   PVCR_VALUE[13]=MPXE
   PVCR_VALUE[12:10]=MPXV[2:0]
   PVCR_VALUE[9:6]= VCULLMTBS[3:0]
   PVCR_VALUE[5:0]= GCTRL[5:0]

		ADCJnDRj — Data Register j.
3 to 1	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
0	ADDNT	Addition Count Select 0: Add twice 1: Add 4 times This register is valid only when CNVCLS[2:0] is 4_H or 6_H.

CAUTION

To prevent a malfunction, there is the limitations of setting update in this register.
For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.3.3.15 ADCJnDFASENTSGER — DFE/ASF Entry Scan Group Enable Register

ADCJnDFASENTSGER is a 16-bit readable/writable register that enables or disables scan groups to be transferred to the DFE, and the ASF. ADCJnDFASENTSGER is initialized to 0000_H at reset.

Value after reset: 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	DFENTSG4E	DFENTSG3E	DFENTSG2E	DFENTSG1E	DFENTSG0E	—	—	—	ASENTSG4E	ASENTSG3E	ASENTSG2E	ASENTSG1E	ASENTSG0E
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Table 43.38 ADCJnDFASENTSGER Register Contents

Bit Position	Bit Name	Function
15 to 13	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
12 to 8	DFENTSGxE	DFE Entry Scan Group Enable 0: Entry to DFE is disabled when starting SGx. 1: Entry to DFE is enabled when starting SGx. Entry is performed for virtual channels for which DFENT in ADCJnVCRj is set to 1. Use the DFENTSGxE bits by setting one of these bits to 1.
7 to 5	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
4 to 0	ASENTSGxE	ASF Entry Scan Group Enable 0: Entry to ASF is disabled when starting SGx. 1: Entry to ASF is enabled when starting SGx. Entry is performed for virtual channels for which DFENT in ADCJnVCRj is set to 1. Use the ASENTSGxE bits by setting one of these bits to 1.

CAUTIONS

1. To prevent a malfunction, there is the limitations of setting update in this register.
   For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.
2. Do not set DFENTSGxE or ASENTSGxE for the same scan group to 1. If it is enabled for the same scan group, entry is performed for both DFE and ASF of virtual channels for which DFENT in ADCJnVCRj is set to 1 specified for the scan group.

43.3.3.16 ADCJnADENDP — A/D Conversion Monitor Virtual Channel Pointer

ADCJnADENDP is an 8-bit readable/writable register that selects a virtual channel that outputs the A/D conversion timing to ADENDn. ADCJnADENDP is initialized to 00_H at reset.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	ENDP[5:0]					
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 43.39 ADCJnADENDP Register Contents

Bit Position	Bit Name	Function
7, 6	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
5 to 0	ENDP[5:0]	A/D Conversion Monitor Virtual Channel Pointer When the virtual channel selected by ADCJnADENDP is started, a high level is output to ADENDn. When the virtual channel selected by ADCJnADENDP ends, a low level is output.

CAUTION

To prevent a malfunction, there is the limitations of setting update in this register.
For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.3.3.17 ADCJnSFTCR — Safety Control Register

ADCJnSFTCR is an 8-bit readable/writable register for safety control. ADCJnSFTCR is initialized to 00_H at reset.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	RDCLRE	—	OWEIE	PEIE	IDEIE
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R	R/W	R/W	R/W

Table 43.40 ADCJnSFTCR Register Contents

Bit Position	Bit Name	Function
7 to 5	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
4	RDCLRE	Read and Clear Enable 0: ADCJnDRj and ADCJnDIRj are not cleared by reading ADCJnDRj or ADCJnDIRj or by reading ADCJnDRj via the IFC. 1: ADCJnDRj and ADCJnDIRj are cleared by reading ADCJnDRj or ADCJnDIRj or by reading ADCJnDRj via the IFC. **CAUTION:** WFLG in ADCJnDIRj is cleared by reading ADCJnDRj or ADCJnDIRj or by reading ADCJnDRj via the IFC regardless of the RDCLRE setting.
3	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
2	OWEIE	Overwrite Error Interrupt Enable 0: Disabled 1: Enabled
1	PEIE	Parity Error Interrupt Enable 0: Disabled 1: Enabled
0	IDEIE	ID Error Interrupt Enable 0: Disabled 1: Enabled

CAUTION

To prevent a malfunction, there is the limitations of setting update in this register.
For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.3.3.18 ADCJnTDCR — Pin-Level Self-Diagnosis Control Register

ADCJnTDCR is an 8-bit readable/writable register that controls the pin-level self-diagnosis. ADCJnTDCR is initialized to 00_H at reset.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	TDE	—	—	—	—	—	TDLV[1:0]	
Value after reset	0	0	0	0	0	0	0	0
R/W	R/W	R	R	R	R	R	R/W	R/W

Table 43.41 ADCJnTDCR Register Contents

Bit Position	Bit Name	Function
7	TDE	Pin-Level Self-Diagnosis 0: Pin-level self-diagnosis is disabled. 1: Pin-level self-diagnosis is enabled. When TDE is set to 1, all analog pins are disconnected from the input buffer. When TDE is set to 0, all analog pins are connected to the input buffer. When TDE is set to 1, the voltage is fixed to the level specified by TDLV[1:0]. Performing an A/D conversion in this state and checking the A/D converted value allows diagnosis of the path from an analog pin to the ADC.
6 to 2	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
1, 0	TDLV[1:0]	Pin-Level Self-Diagnosis 0_H: Even numbers of physical channel groups are discharged to AnVSS, and odd numbers of physical channel groups are charged to AnVCC. 1_H: Even numbers of physical channel groups are charged to AnVCC, and odd numbers of physical channel groups are discharged to AnVSS. 2_H: Even numbers of physical channel groups are discharged to AnVSS, and odd numbers of physical channel groups are charged to 1/2*AnVCC. 3_H: Even numbers of physical channel groups are charged to 1/2*AnVCC, and odd numbers of physical channel groups are discharged to AnVSS.

CAUTION

To prevent a malfunction, there is the limitations of setting update in this register.
For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.3.3.19 ADCJnODCR — Wiring-break Detection Control Register

ADCJnODCR is a 32-bit readable/writable register that controls wiring-break detection.

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ODDE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	ODE	—	ODPW[5:0]					
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 43.42 ADCJnODCR Register Contents

Bit Position	Bit Name	Function
31	ODDE	Wiring-break Detection Self-diagnosis Enable 0: Wiring-break detection self-diagnosis is not enabled. 1: Wiring-break detection self-diagnosis is enabled. When ODDE is set to 1, wiring-break detection self-diagnosis is enabled for all analog pins.
30 to 8	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
7	ODE	Wiring-break Detection Enable 0: Wiring-break is not detected. 1: Wiring-break is detected. When ODE is set to 1, wiring-break detection is enabled for all analog pins. After sampling for an A/D conversion ends, analog pins for which an A/D conversion is to be performed are discharged with the pulse width specified in ODPW[5:0].
6	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
5 to 0	ODPW[5:0]*1	Wiring-break Detection Pulse Width 04_H: 1 state (of internal clock) 05_H: 2 states (of internal clock) : 13_H: 16 states (of internal clock) 14_H: 17 states (of internal clock)

Note 1. The setting of ODPW[5:0] must be greater than 03_H and less than 15_H.

CAUTION

To prevent a malfunction, there is the limitations of setting update in this register.
For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.3.3.20 ADCJnECR — Error Clear Register

ADCJnECR is an 8-bit write-only register that controls error clearing. The register bits are always read as 0.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	OWEC	PEC	—
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	W	W	R

Table 43.43 ADCJnECR Register Contents

Bit Position	Bit Name	Function
7 to 3	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
2	OWEC	Overwrite Error Clear Writing 0: Not cleared Writing 1: Cleared
1	PEC	Parity Error Clear Writing 0: Not cleared Writing 1: Cleared
0	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.

43.3.3.21 ADCJnOWER — Overwrite Error Register

ADCJnOWER is an 8-bit read-only register that indicates an overwrite error.

ADCJnOWER is initialized to 00_H at reset.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	OWE	—	OWECAP[5:0]					
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Table 43.44 ADCJnOWER Register Contents

Bit Position	Bit Name	Function
7	OWE	Overwrite Error 0: No error is present 1: An error is present. Setting condition The A/D converted value is written to ADCJnDRj when WFLG = 1. Clearing condition A value of 1 is written to OWEC in ADCJnECR.
6	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
5 to 0	OWECAP[5:0]	Overwrite Error Capture The virtual channel at the time when an overwrite error occurred is captured. Capturing condition The A/D converted value is written to ADCJnDRj when OWE = 0 and WFLG = 1. Clearing condition A value of 1 is written to OWEC in ADCJnECR.

CAUTION

ADCJnOWER is updated when the A/D converted value is written to ADCJnDRj.

43.3.3.22 ADCJnPER — Parity Error Register

ADCJnPER is an 8-bit read-only register that indicates a parity error. ADCJnPER is initialized to 00_H at reset.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	PE	—	PECAP[5:0]					
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Table 43.45 ADCJnPER Register Contents

Bit Position	Bit Name	Function
7	PE	Parity Error 0: No errors present 1: An error is present. Setting condition A parity error is detected. Clearing condition A value of 1 is written to PEC in ADCJnECR.
6	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
5 to 0	PECAP[5:0]	Parity Error Capture The virtual channel at the time when a parity error occurred is captured. Capturing condition A parity error is detected when PE = 0. Clearing condition A value of 1 is written to PEC in ADCJnECR.

CAUTION

ADCJnPER is updated when ADCJnDRj or ADCJnDIRj is read, but is not updated when ADCJnDRj is read via the IFC.

43.3.3.23 ADCJnVCULLMTBR0 to 6 — Virtual Channel Upper/Lower Limit Table Register 0 to 6

ADCJnVCULLMTBR0 to ADCJnVCULLMTBR6 are 32-bit readable/writable registers. ADCJnVCULLMTBR0 to ADCJnVCULLMTBR6 are selected from ADCJnVCRj.VCULLMTBS[2:0]. These registers are initialized to 7FFE 0000_H by reset.

Value after reset: 7FFE 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VCULMTB[15:0]															
Value after reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VCLLMTB[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Table 43.46 ADCJnVCULLMTBR Register Contents 0 to 6

Bit Position	Bit Name	Function
31 to 16	VCULMTB[15:0]	Upper Limit Table These bits specify the upper-limit value of an A/D converted value. Setting range: 0000_H to $7FFE_H$ Be sure to set it to the signed fixed-point format. VCULMTB[15] and VCULMTB[0] are always fixed to 0. When in normal-A/D-conversion-in-addition-mode (ADCJnVCRj.CNVCLS[2:0] = 4_H), or normal-A/D-conversion-with-the-MPX-in-addition-mode (ADCJnVCRj.CNVCLS[2:0] = 6_H), set the comparative value to the addition sum.
15 to 0	VCLLMTB[15:0]	Lower Limit Table These bits specify the lower-limit value of an A/D converted value. Setting range: 0000_H to $7FFE_H$ Be sure to set it to the signed fixed-point format. VCLLMTB[15] and VCLLMTB[0] are always fixed to 0. When in normal-A/D-conversion-in-addition-mode (ADCJnVCRj.CNVCLS[2:0] = 4_H), or normal-A/D-conversion-with-the-MPX-in-addition-mode (ADCJnVCRj.CNVCLS[2:0] = 6_H), set the comparative value to the addition sum.

43.3.3.24 ADCJnVCLMINTER1 — Virtual Channel Upper/Lower Limit Error Interrupt Enable Register 1

ADCJnVCLMINTER1 is a 32-bit readable/writable register for output control of the upper/lower limit error interrupt for virtual channels 0 to 31. ADCJnVCLMINTER1 is initialized to 0000 0000_H at reset.

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ADUL31IE	ADUL30IE	ADUL29IE	ADUL28IE	ADUL27IE	ADUL26IE	ADUL25IE	ADUL24IE	ADUL23IE	ADUL22IE	ADUL21IE	ADUL20IE	ADUL19IE	ADUL18IE	ADUL17IE	ADUL16IE
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADUL15IE	ADUL14IE	ADUL13IE	ADUL12IE	ADUL11IE	ADUL10IE	ADUL09IE	ADUL08IE	ADUL07IE	ADUL06IE	ADUL05IE	ADUL04IE	ADUL03IE	ADUL02IE	ADUL01IE	ADUL00IE
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 43.47 ADCJnVCLMINTER1 Register Contents

Bit Position	Bit Name	Function
31 to 0	ADULjIE	Virtual channel upper / lower limit error enable 0: The upper / lower limit error interrupt (INT_ULn) is not output by result of the virtual channel j. 1: The upper / lower limit error interrupt (INT_ULn) is output by the result of the virtual channel j.

CAUTION

To prevent a malfunction, there is the limitations of setting update in this register.
For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.3.3.25 ADCJnVCLMINTER2 — Virtual Channel Upper/Lower Limit Error Interrupt Enable Register 2

ADCJnVCLMINTER2 is a 32-bit readable/writable register for output control of the upper/lower limit error interrupt for virtual channels 32 to 39. ADCJnVCLMINTER2 is initialized to 0000 0000_H at reset.

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	ADUL39IE	ADUL38IE	ADUL37IE	ADUL36IE	ADUL35IE	ADUL34IE	ADUL33IE	ADUL32IE
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 43.48 ADCJnVCLMINTER2 Register Contents

Bit Position	Bit Name	Function
31 to 8	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
7 to 0	ADULjIE	Virtual channel upper / lower limit error enable 0: The upper / lower limit error interrupt (INT_ULn) is not output by the result of the virtual channel j. 1: The upper / lower limit error interrupt (INT_ULn) is output by the result of the virtual channel j.

CAUTION

To prevent a malfunction, there is the limitations of setting update in this register.
For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.3.3.26 ADCJnVCLMSR1 — Virtual Channel Upper/Lower Limit Excess Status Register 1

ADCJnVCLMSR1 is a 32-bit read-only register that indicates an upper/lower limit excursion of virtual channel 0 to 31. ADCJnVCLMSR1 is initialized to 0000 0000_H at reset.

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VC31LMS	VC30LMS	VC29LMS	VC28LMS	VC27LMS	VC26LMS	VC25LMS	VC24LMS	VC23LMS	VC22LMS	VC21LMS	VC20LMS	VC19LMS	VC18LMS	VC17LMS	VC16LMS
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VC15LMS	VC14LMS	VC13LMS	VC12LMS	VC11LMS	VC10LMS	VC09LMS	VC08LMS	VC07LMS	VC06LMS	VC05LMS	VC04LMS	VC03LMS	VC02LMS	VC01LMS	VC00LMS
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 43.49 ADCJnVCLMSR1 Register Contents

Bit Position	Bit Name	Function
31 to 0	VCjLMS	Virtual channel j upper / lower limit status 0: Limit has not been passed. 1: Limit has been passed. Setting condition The upper limit or the lower limit excursion has been detected. Clearing condition A value of 1 is written to VCjLMSC of VCLMSCR1.

43.3.3.27 ADCJnVCLMSR2 — Virtual Channel Upper/Lower Limit Excess Status Register 2

ADCJnVCLMSR2 is a 32-bit read-only register that indicates an upper/lower limit excursion of virtual channel 32 to 39. ADCJnVCLMSR2 is initialized to 0000 0000_H at reset.

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	VC39LMS	VC38LMS	VC37LMS	VC36LMS	VC35LMS	VC34LMS	VC33LMS	VC32LMS
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 43.50 ADCJnVCLMSR2 Register Contents

Bit Position	Bit Name	Function
31 to 8	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
7 to 0	VCjLMS	Virtual channel j upper / lower limit excursion status 0: The limit has not been passed. 1: The limit has been passed. Setting condition The upper limit or the lower limit excursion has been is detected. Clearing condition A value of 1 is written to VCjLMSC of VCLMSCR2.

43.3.3.28 ADCJnVCLMSCR1 — Virtual Channel Upper/Lower Limit Excess Status Clear Register 1

ADCJnVCLMSCR1 is a 32-bit write-only register that clears virtual channel upper/lower limit excursion status register1 (ADCJnVCLMSR1). The register bits are always read as 0.

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VC31LMSC	VC30LMSC	VC29LMSC	VC28LMSC	VC27LMSC	VC26LMSC	VC25LMSC	VC24LMSC	VC23LMSC	VC22LMSC	VC21LMSC	VC20LMSC	VC19LMSC	VC18LMSC	VC17LMSC	VC16LMSC
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VC15LMSC	VC14LMSC	VC13LMSC	VC12LMSC	VC11LMSC	VC10LMSC	VC09LMSC	VC08LMSC	VC07LMSC	VC06LMSC	VC05LMSC	VC04LMSC	VC03LMSC	VC02LMSC	VC01LMSC	VC00LMSC
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Table 43.51 ADCJnVCLMSCR1 Register Contents

Bit Position	Bit Name	Function
31 to 0	VCjLMSC	Virtual channel j upper / lower limit excursion status clear 0: Not cleared. 1: VCjLMS of VCLMSR1 is cleared.

43.3.3.29 ADCJnVCLMSCR2 — Virtual Channel Upper/Lower Limit Excess Status Clear Register 2

ADCJnVCLMSCR2 is a 32-bit write-only register that clears the virtual channel upper/lower limit excursion status register2 (ADCJnVCLMSR2). The register bits are always read as 0.

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	VC39LMSC	VC38LMSC	VC37LMSC	VC36LMSC	VC35LMSC	VC34LMSC	VC33LMSC	VC32LMSC
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W

Table 43.52 ADCJnVCLMSCR2 Register Contents

Bit Position	Bit Name	Function
31 to 8	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
7 to 0	VCjLMSC	Virtual channel j upper / lower limit excess status clear 0: Not cleared. 1: VCjLMS of VCLMSR2 is cleared.

43.3.4 Scan Group Specific Registers

This section describes registers provided for each scan group.

43.3.4.1 ADCJnSGSTCRx — Scan Group x Start Control Register

ADCJnSGSTCRx is an 8-bit write-only register that controls the start of scan group x. The register bits are always read as 0.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SGST
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	W

Table 43.53 ADCJnSGSTCRx Register Contents

Bit Position	Bit Name	Function
7 to 1	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
0	SGST	Scan Group Start Condition for starting scan group x: A value of 1 is written to SGST when SGACT = 0

43.3.4.2 ADCJnSGSTPCRx — Scan Group x Stop Control Register

ADCJnSGSTPCRx is an 8-bit write-only register that controls the stop of scan group x. The register bits are always read as 0.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SGSTP
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	W

Table 43.54 ADCJnSGSTPCRx Register Contents

Bit Position	Bit Name	Function
7 to 1	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
0	SGSTP	Scan Group Stop Condition for stopping scan group x: A value of 1 is written to SGSTP when SGACT = 1

43.3.4.3 ADCJnADTSTCRy — A/D Timer y Start Control Register

ADCJnADTSTCRy is an 8-bit write-only register that controls the start of A/D timer y. The register bits are always read as 0.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	ADTST
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	W

Table 43.55 ADCJnADTSTCRy Register Contents

Bit Position	Bit Name	Function
7 to 1	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
0	ADTST	A/D Timer Start Condition for starting A/D timer y: A value of 1 is written to ADTST when ADTACT = 0

43.3.4.4 ADCJnADTENDCRy — A/D Timer y End Control Register

ADCJnADTENDCRy is an 8-bit write-only register that controls stop of A/D timer y. The register bits are always read as 0.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	ADTEND
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	W

Table 43.56 ADCJnADTENDCRy Register Contents

Bit Position	Bit Name	Function
7 to 1	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
0	ADTEND	A/D Timer End Condition for finishing A/D timer y: A value of 1 is written to ADTEND when ADTACT = 1

43.3.4.5 ADCJnSGCRx — Scan Group x Control Register

ADCJnSGCRx is an 8-bit readable/writable register that controls scan group x. ADCJnSGCRx is initialized to 00_H at reset.

Value after reset: 00_H

- **When x = 0 to 2**

Bit	7	6	5	4	3	2	1	0
	—	ADSTARTE	SCANMD	ADIE	—	—	—	TRGMD
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R	R	R	R/W

Table 43.57 ADCJnSGCRx Register Contents (x = 0 to 2)

Bit Position	Bit Name	Function
7	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
6	ADSTARTE	Scan Group Synchronization Start Enable 0: ADSTART is disabled. 1: ADSTART is enabled.
5	SCANMD	Scan Mode 0: Multicycle scan mode 1: Continuous scan mode In multicycle scan mode, scans are repeated as many times as specified in ADCJnSGMCYCRx. In continuous scan mode, scans are repeated with no limit of times.
4	ADIE	Scan End Interrupt Enable 0: ADInx is not output at the end of scan for SGx. 1: ADInx is output at the end of scan for SGx. ADIE of ADCJnSGCRx is independent of ADIE of ADCJnVCRj. For details, see **Section 43.4.6.1, Scan End Interrupt Request**.
3 to 1	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
0	TRGMD	Trigger Mode 0: Trigger input to SGx is disabled. 1: The SGx_TRG hardware trigger is selected for the trigger input to SGx.

- **When x = 3 or 4**

Bit	7	6	5	4	3	2	1	0
	ADTSTARTE	ADSTARTE	SCANMD	ADIE	—	—	TRGMD[1:0]	
Value after reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W

Table 43.58 ADCJnSGCRx Register Contents (x = 3 or 4)

Bit Position	Bit Name	Function
7	ADTSTARTE	A/D Timer Synchronization Start Enable 0: ADTSTART is disabled. 1: ADTSTART is enabled.
6	ADSTARTE	Scan Group Synchronization Start Enable 0: ADSTART is disabled. 1: ADSTART is enabled.
5	SCANMD	Scan Mode 0: Multicycle scan mode 1: Continuous scan mode In multicycle scan mode, scans are repeated as many times as specified in ADCJnSGMCYCRx. In continuous scan mode, scans are repeated with no limit of times.
4	ADIE	Scan End Interrupt Enable 0: ADInx is not output at the end of scan for SGx. 1: ADInx is output at the end of scan for SGx. ADIE of ADCJnSGCRx is independent of ADIE of ADCJnVCRj. For details, see **Section 43.4.6.1, Scan End Interrupt Request**.
3, 2	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
1, 0	TRGMD[1:0]	Trigger Mode 0_H: Trigger input to SGx is disabled. Trigger input to A/D timer x is disabled. 1_H: SGx_TRG hardware trigger is selected for the trigger input to SGx. Trigger input to A/D timer x is disabled. 2_H: A/D timer trigger x is selected for the trigger input to SGx. Trigger input to A/D timer x is disabled. 3_H: A/D timer trigger x is selected for the trigger input to SGx. The SGx_TRG hardware trigger is selected for the trigger input to A/D timer x.

CAUTIONS

1. To prevent a malfunction, there is the limitations of setting update in this register.
   For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**. But when scan group is terminated, clearing ADIE and TRGMD to 0 isn't included in the limitations.
2. If a trigger of a lower-priority scan group is input to a scan group for which continuous scan mode is set (SCANMD = 1_H), the trigger is not accepted. Therefore, it is assumed that the continuous scan mode is set for scan group 0.
3. Hardware trigger (scan group x start) input to a started scan group x is ignored.

43.3.4.6 ADCJnSGVCSPx — Scan Group x Start Virtual Channel Pointer

See **Section 43.3.4.12, ADCJnSGVCPRx — Scan Group x Virtual Channel Pointer Register** together.

ADCJnSGVCSPx is an 8-bit readable/writable register that specifies the start pointer of a virtual channel.
ADCJnSGVCSPx is initialized to 00_H at reset.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	VCSP[5:0]					
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 43.59 ADCJnSGVCSPx Register Contents

Bit Position	Bit Name	Function
7, 6	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
5 to 0	VCSP[5:0] ADCJnSGVCSPx must be equal to or less than ADCJnSGVCEPx.	Start Virtual Channel Pointer These bits select the virtual channel from which the scan is to be started. When an SGx is started, processing for the virtual channels from ADCJnSGVCSPx to ADCJnSGVCEPx is executed.

CAUTIONS

1. Do not set the value greater than 39.
2. ADCJnSGVCSPx must be equal to or less than ADCJnSGVCEPx.
3. This register has a mirror structure as follows. While scan group x is executing, if it is necessary to rewrite SGVCSP and SGVCEP, be sure to use a mirror register.

This Register	Mirror Register
ADCJnVCSPx.VCSP[5:0]	ADCJnVCPRx.VCSP[5:0]

4. It is possible to set same virtual channel n (ADCJnVCRj) in more than one scan group x by setting the start / end virtual channel pointer.
   But, when a virtual channel is overwritten while one scan group is operating, the setting for A/D conversion might be different from the desired setting for this scan group.

   Make sure to use caution of the information below to avoid this problem.

   – When designing a system, always specify the same value for the ADCJnVCRj setting when it is used by multiple scan groups for the target channel.

   – Rewrite ADCJnVCRj after stopping all scan groups of a target channel. When VCRs are not protected, A/D conversion results can't be guaranteed.
5. To prevent a malfunction, there is the limitations of setting update in this register.
   For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.3.4.7 ADCJnSGVCEPx — Scan Group x End Virtual Channel Pointer

See **Section 43.3.4.12, ADCJnSGVCPRx — Scan Group x Virtual Channel Pointer Register** together.

ADCJnSGVCEPx is an 8-bit readable/writable register that specifies the end pointer of a virtual channel.
ADCJnSGVCEPx is initialized to 00_H at reset.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	VCEP[5:0]					
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 43.60 ADCJnSGVCEPx Register Contents

Bit Position	Bit Name	Function
7, 6	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
5 to 0	VCEP[5:0]	End Virtual Channel Pointer These bits select the virtual channel at which the scan is to be ended. When SGx is started, processing for the virtual channels from ADCJnSGVCSPx to ADCJnSGVCEPx is executed.

CAUTIONS

1. This register has a mirror structure as follows. While scan group x is executing, if it is necessary to rewrite SGVCSP and SGVCEP, be sure to use a mirror register.

This Register	Mirror Register
ADCJnVCEPx.VCSP[5:0]	ADCJnVCPRx.VCEP[5:0]

   See **Section 43.3.4.6, ADCJnSGVCSPx — Scan Group x Start Virtual Channel Pointer** for other cautions.

2. To prevent a malfunction, there is the limitations of setting update in this register.
   For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.3.4.8 ADCJnSGMCYCRx — Scan Group x Multicycle Register

ADCJnSGMCYCRx is an 8-bit readable/writable register that specifies the number of scan cycles in multicycle scan mode. ADCJnSGMCYCRx is initialized to 00_H at reset.

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	MCYC[7:0]							
Value after reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 43.61 ADCJnSGMCYCRx Register Contents

Bit Position	Bit Name	Function
7 to 0	MCYC[7:0]	Multicycle Specification These bits specify the number of scan cycles in multicycle scan mode. Number of scan cycles = MCYC[7:0] + 1 When SGx is started, scans are repeated for virtual channels from ADCJnSGVCSPx to ADCJnSGVCEPx for many cycles as specified in ADCJnSGMCYCRx.

CAUTION

To prevent malfunction, there is the limitations of setting update in this register.
For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.3.4.9 ADCJnSGSRx — Scan Group x Status Register

ADCJnSGSRx is an 8-bit read-only register that indicates the status of scan group x.

Value after reset: 00_H

- **When x = 0 to 2**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	SGACT	—
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Table 43.62 ADCJnSGSRx Register Contents (x = 0 to 2)

Bit Position	Bit Name	Function
7 to 2	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
1	SGACT	Scan Group Status 0: There is no source in SGx. 1: There is a source in SGx. (The period from the reception of a starting trigger until A/D conversion completion, or until aborting by ADHALT or SGSTP.)
0	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.

- **When x = 3 or 4**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	ADTACT	SGACT	—
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Table 43.63 ADCJnSGSRx Register Contents (x = 3, 4)

Bit Position	Bit Name	Function
7 to 3	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
2	ADTACT	A/D Timer Status 0: A/D timer x is in idle state. 1: A/D timer x is running.
1	SGACT	Scan Group Status 0: There is no source in SGx. 1: There is a source in SGx. (The period from the reception of a starting trigger until A/D conversion completion, or until aborting by ADHALT or SGSTP.)
0	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.

43.3.4.10 ADCJnADTIPRy — A/D Timer y Initial Count Register

ADCJnADTIPRy is a 32-bit readable/writable register that sets the initial count of A/D timer y. ADCJnADTIPRy is initialized to 0000 0000_H at reset.

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	ADTIP[20:16]				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADTIP[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 43.64 ADCJnADTIPRy Register Contents

Bit Position	Bit Name	Function
31 to 21	-	Reserved When read, the value after reset is returned. When writing, write the value after reset.
20 to 0	ADTIP[20:0]	A/D Timer Initial Count These bits set the initial phase of A/D timer y. (1) After A/D timer y is started, ADCJnADTIPRy is loaded to A/D timer y and the timer counts down. (2) After A/D timer y becomes 0, A/D timer trigger y is output for one cycle, ADCJnADTPRRy is loaded to A/D timer y, and the timer counts down again. After that, (2) is repeated. For details, see **Section 43.4.5.3, A/D Timer Trigger**.

CAUTION

To prevent a malfunction, there is the limitations of setting update in this register.
For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.3.4.11 ADCJnADTPRRy — A/D Timer y Cycle Count Register

ADCJnADTPRRy is a 32-bit readable/writable register that sets the cycle count of A/D timer y. ADCJnADTPRRy is initialized to 001F FFFF$_H$ at reset.

Value after reset: 001F FFFF$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	ADTPR[20:16]				
Value after reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADTPR[15:0]															
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 43.65 ADCJnADTPRRy Register Contents

Bit Position	Bit Name	Function
31 to 21	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
20 to 0	ADTPR[20:0]	A/D Timer Cycle These bits set the cycle of A/D timer y. (1) After A/D timer y is started, ADCJnADTIPRy is loaded to A/D timer y and the timer counts down. (2) After A/D timer y becomes 0, A/D timer trigger y is output for one cycle, ADCJnADTPRRy is loaded to A/D timer y, and the timer counts down again. After that, (2) is repeated. For details, see **Section 43.4.5.3, A/D Timer Trigger**.

CAUTION

To prevent a malfunction, there is the limitations of setting update in this register.
For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.3.4.12 ADCJnSGVCPRx — Scan Group x Virtual Channel Pointer Register

ADCJnSGVCPRx is a 16-bit readable/writable register that specifies the start/end pointer of a virtual channel. For this register, write as 16-bit.

Value after reset: 00_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	VCEP[5:0]						—	—	VCSP[5:0]					
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 43.66 ADCJnSGVCPRx Register Contents

Bit Position	Bit Name	Function
15 to 14	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
13 to 8	VCEP[5:0]*1	End Virtual Channel Pointer (mirror of ADCJnSGVCEP)
7 to 6	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
5 to 0	VCSP[5:0]*1	Start Virtual Channel Pointer (mirror of ADCJnSGVCSP)

Note 1. For details of this function, see **Section 43.3.4.6, ADCJnSGVCSPx — Scan Group x Start Virtual Channel Pointer** and **Section 43.3.4.7, ADCJnSGVCEPx — Scan Group x End Virtual Channel Pointer**.

43.3.4.13 ADCJnSGVCOWRx — Scan Group x Virtual Channel Optional Waiting Times Register

ADCJnSGVCOWRx is a 16-bit readable/writable register that specifies an optional wait time in an execution interval of virtual channel j and virtual channel j+1.

Value after reset: 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	VCOW[11:0]											
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 43.67 ADCJnSGVCOWRx Register Contents

Bit Position	Bit Name	Function
15 to 12	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
11 to 0	VCOW[11:0]	Wait Time Specification Between Virtual Channels of same scan group 000_H: No wait. 001_H to FFF_H: set value x 4 ADCLK Note: For example, if you want to set wait times to 1us, set to VCOW[11:0] $00A_H$. Wait time, please set the VCOW value in the range of 1...400us at 1us intervals.

CAUTION

To prevent a malfunction, there is the limitations of setting update in this register.
For the limitations of setting update, refer to **Section 43.4.1.4, Limitations of Setting Update**.

43.4 Operation

A/D conversion is performed by scan group.

Virtual channels that are assigned by the scan group start/end pointer are scanned in ascending order.

When multiple scan groups start up, the processing is performed from the scan group with the highest priority.

After the initial settings, scan starts by input of the start trigger.

Scan ends when A/D conversion ends for the specified count or by forced termination.

Information about the settings, functions, and operations is described below.

43.4.1 Setting Procedure

43.4.1.1 Initial Settings

The initial settings must be specified while the trigger of all the scan groups is disabled and all the scan groups and all accumulation channels stop.

If such items shown above are running, perform the termination procedure.

Use the value after reset for the register setting value of the function that is not to be used.

(1) Registers that must be set

The control bit that is required to be set at minimum for executing A/D conversion is defined as a required setting bit.

The required setting bit contains the following bits:

- Bits that determine the operating mode of the SAR-ADC (SM).

- Bits that determine physical channels and virtual channels to be subject to A/D conversion.

Registers that contain the required setting bits are as below:

Table 43.68 Required Registers which must be set for proper operation

Classification	Register	Indispensable Setting Bit	Explanation	Addition
Required	ADCJnADCR1	SUSMTD	Suspend method	—
	ADCJnADCR2	DFMT	Data format	—
	ADCJnVCRj	CNVCLS, GCTRL	Conversion class, General control	Setting is unnecessary for ADCJnVCRj which are not used.
	ADCJnSGCRx	SCANMD	Scan mode	Setting is unnecessary for SGx which are not used.
	ADCJnSGMCYCRx	MCYC[7:0]	The number of multi-cycle-scan times	Setting is unnecessary for SGx that a continuous mode is chosen.
	ADCJnSGVCOWRx	VCOM[11:0]	Optional waiting times of between virtual channels	Setting is unnecessary for SGx that the waiting times aren't inserted between the virtual channels.
At least one of these must be set	ADCJnSGVCSPx, ADCJnSGVCEPx	VCSP, VCEP	Starting / end pointer	Setting is unnecessary for SGx which isn't used.
	ADCJnSGVCPRx			

Error! Use the Home tab to apply 見出し 1 to the text that you want to appear here.

Please set registers other than these properly according to the function to use.

(2) About Setting Order

Any register setting sequence is acceptable regardless of whether the register contains the required setting bit.

Set registers in the desired order.

The initial setting flow is shown below. The setting order in the flow is for convenience.

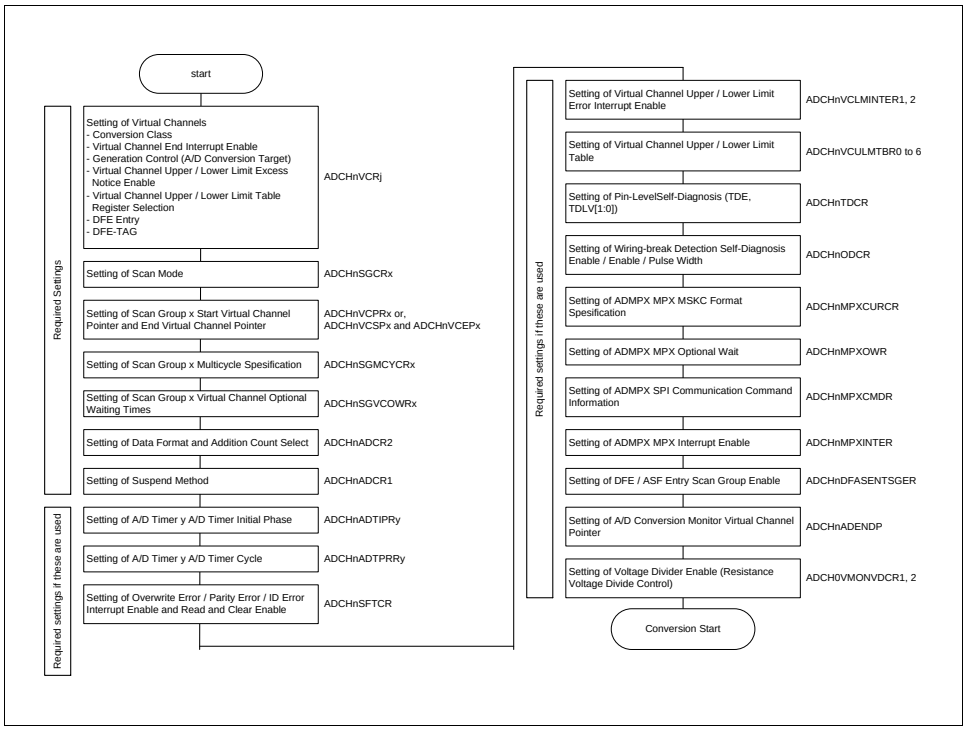

Figure 43.5 Initial Setting Flow

43.4.1.2 Startup Method

This section describes how to start up scan group x, AD timer x.

The procedure differs depending on the startup target.

Perform the startup procedure during the initial setting, or while scan group x to be started is stopped (ADCJnSGSRx.SGACT = 0) after the settings have been updated.

The startup procedure is ignored if the target is already operating.

Table 43.69 Startup Method of Scan Group x, AD Timer y and ASF

Starting target	Trigger type	Starting method
Scan group x	S/W trigger	Write 1 to ADCJnSGSTCRx.SGST.
	H/W trigger	1. Set 1_H to SGCRx.TRGMD [1:0]. 2. Input a High pulse signal of 1ADCLK width to the SGx_TRG terminal.
A/D conversion synchronous start	S/W trigger	1. Set SGCRx.ADSTARTE to 1 for scan group x of ADCJ0. 2. Set SGCRx.ADSTARTE to 1 for scan group x of ADCJ1. 3. Write 1 to ADSYNSTCR.ADSTART.
A/D timer y	S/W trigger	Write 1 to ADTSTCRx.ADTST.
	H/W trigger	1. Set SGCRx.TRGMD[1:0] to 3H. 2. Input the H pulse signal with 1 clkad width to the SGx_TRG pin.
A/D timer synchronous start	S/W trigger	1. Set SGCRx.ADTSTARTE to 1 for scan group x of ADCJ0. 2. Set SGCRx.ADTSTARTE to 1 for scan group x of ADCJ1. 3. Write 1 to ADTSYNSTCR.ADTSTART.
Setting of ASF	—	See **Section Error! Reference source not found., Error! Reference source not found.**.

43.4.1.3 Terminating Procedure

This section describes the procedure to terminate scan groups.

There are three termination methods: termination of all scan groups (forced termination), termination of scan group x 1 and termination of scan group x 2.

For the detailed description of ASFrCTL1 register in each flow, please see **Section** Error! Reference source not found., Error! Reference source not found..

(1) To Terminate All Scan Groups (Forced Termination)

This procedure is to terminate all scan groups.

Please clear the multiplication counter in ASF and all intermediate buffers as ASFrCTL1.ASFrST = 0 of ASF when either of scanning group is using ASF.

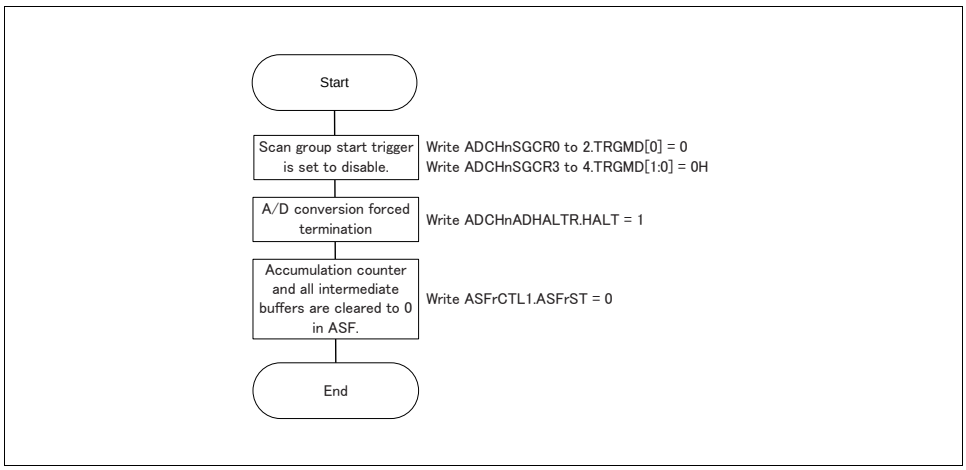

Figure 43.6 All Scan Group (A/D halt) Flow

For the detailed description of termination timing, please see **Section 43.4.14.1, Example of All Scan Group Stop (A/D Halt)**.

(2) Scan Group x Termination Procedure 1

This procedure is to terminate scan group x individually.

To terminate multiple scan groups, perform this termination procedure for each scan group.

This procedure can be applied to scan groups that are operating in multicycle scan mode.

When terminating a scan group that is operating in continuous scan mode, please see **Section 43.4.1.3(1), To Terminate All Scan Groups (Forced Termination)** or **Section 43.4.1.3(3), Scan Group x Termination Procedure 2**.

Please clear the multiplication counter in ASF and all intermediate buffers as ASFrCTL1.ASFrST=0 of ASF when the scanning group that stops is using ASF.

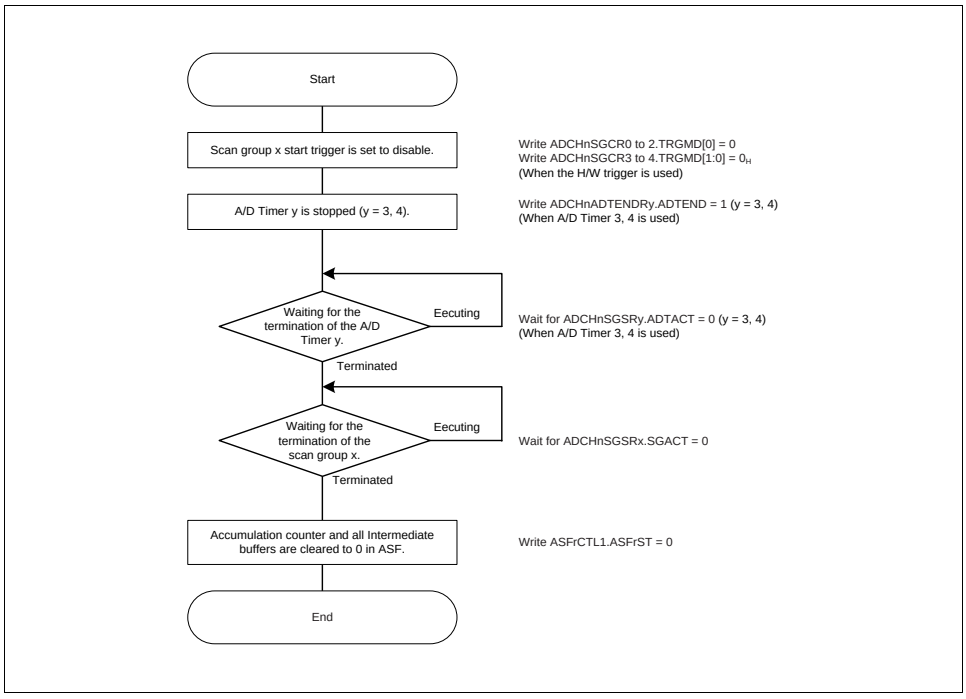

Figure 43.7 Scan Group x Termination Flow 1

(3) Scan Group x Termination Procedure 2

It is a procedure for stopping individual scanning group x.

Please execute the shutdown procedure to each scanning group when you stop two or more scanning groups.

The order of the proper move can be applied to the scanning group operating by either of the multi cycle scanning mode/mode of a continuous scanning.

When the processing of a virtual channel that works according to timing in which one is written in scanning group x stop control register ends when stopping in order of the proper move, scanning group x is ended.

Please clear the multiplication counter in ASF and all intermediate buffers as ASF1nCTL1.ASF1nST=0 of ASF when the scanning group that stops is using ASF.

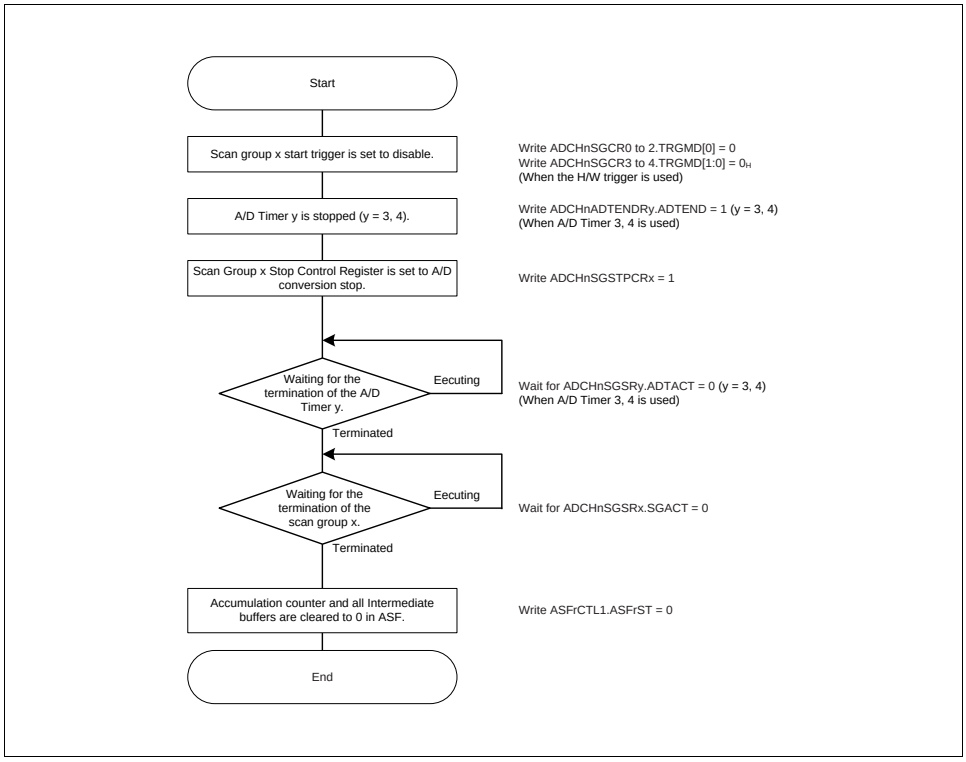

Figure 43.8 Scan Group x Termination Flow 2

The analog to digital translation end or the scanning end interrupt might be output by the setting though the scanning group that corresponds changes to IDLE when one is written in scanning group x stop control register in the analog to digital translation near the end. Please write one in scanning group x stop control register after disabling interrupt if it is inconvenient on the system.

For the detailed description of termination timing, please see **Section 43.4.14.2, Example of Scan Group x Stop**.

43.4.1.4 Limitations of Setting Update

A period to update the setting is limited for the registers shown in the initial setting flow.

To update:

Scan group stop → Register setting update → Scan group startup

Note 1. When a scan group of a stop target is using H/W trigger, invalidate H/W trigger before stopping.

The period for updating differs depending on registers as follows.

Update settings after the specified termination procedure according to the following table:

Table 43.70 Possible Period of Setting Update of Register for Initial Setup

Register	Update Possible Period
ADCJnADCR1	1) All scan groups stop
ADCJnADCR2	
ADCJnSFTCR	
ADCJnTDCR	
ADCJnODCR	
ADCJnMPXCURCR	
ADCJnMPXOWR	
ADCJnDFASENTSGER	
ADCJnADENDP	
ADCJnVMONVDCR1, 2 (For RH850/E2x-FCC1, E2M, E2L)	
ADCJnVMONVDCR1, 2	
ADCJnSGCRx	
ADCJnSGMCYCRx	
ADCJnSGVCSPx	
ADCJnSGVCEPx	
ADCJnSGVCOWRx	
ADCJnADTIPR3 to 4	
ADCJnADTPRR3 to 4	
ADCJnMPXCMDR	
ADCJnMPXINTER	
ADCJnVCLMINTER1, 2	
ADCJnVCR00 to 39	2) Setting target scan group x stop
ADCJnSGVCPRx	3) Always updatable
ADCJnVCULLMTBR0 to 6	

ADCJnSGVCPR, ADCJnVCULLMTBR0～6 are always updatable regardless of whether the scan group operates or stops.

The updated setting value is applied at the following timing.

ADCJnSGVCPR: Next time the corresponding scan group x starts up

ADCJnVCULLMTBR0～6: Immediately

[Supplement] Update the test register and T&H operation mode select register (THOMSR) while all scan groups stop.

43.4.2 Scan Mode

There are two scan modes.

43.4.2.1 Multicycle Scan Mode

A/D conversion for virtual channels assigned to the target SGx is repeated for a specified count (1 to 256 times.)

Set the SGCRx.SCANMD bit to 0 to start multicycle scan mode.

Specify the scan count in the SGMCYCR register. The setting range of the values is from 00H to FFH. The setting value should be a value obtained by subtracting 1 from the desired execution count.

The following figure shows an operation example when the scan count is 2.

- Conversion type: Normal A/D conversion mode (CNVCLS[2:0] = 0H)
- Scan group 0
- Virtual channel: ADCJnVCR0 to ADCJnVCR3

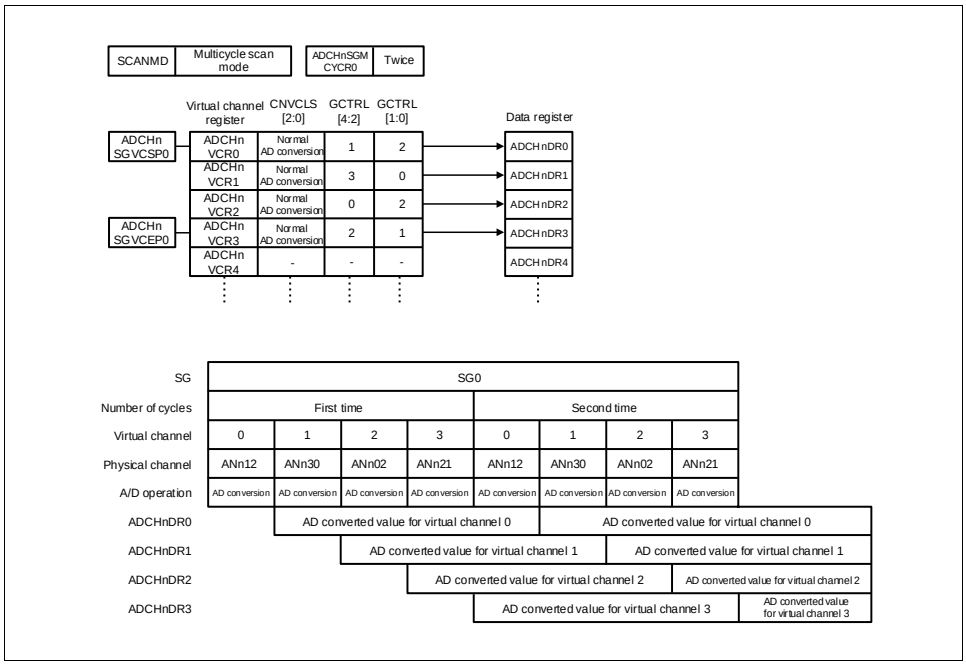

Figure 43.9 Example of Operation in Multicycle Scan Mode

43.4.2.2 Continuous Scan Mode

A/D conversion for virtual channels assigned to the target SGx is repeated with unlimited count.

Set the SGCRx.SCANMD bit to 1 to start continuous scan mode. The setting value of the SGMCYCR register is not effective.

When a trigger for a scan group having a lower priority is input to the scan group that is set in continuous scan mode, the trigger is not accepted.

To stop continuous scan, perform the procedure of terminating all scan groups.

The following figure shows an operation example.

- Conversion type: Normal A/D conversion mode (CNVCLS[2:0] = 0H)
- Scan group 0
- Virtual channel: ADCJnVCR0 to ADCJnVCR3

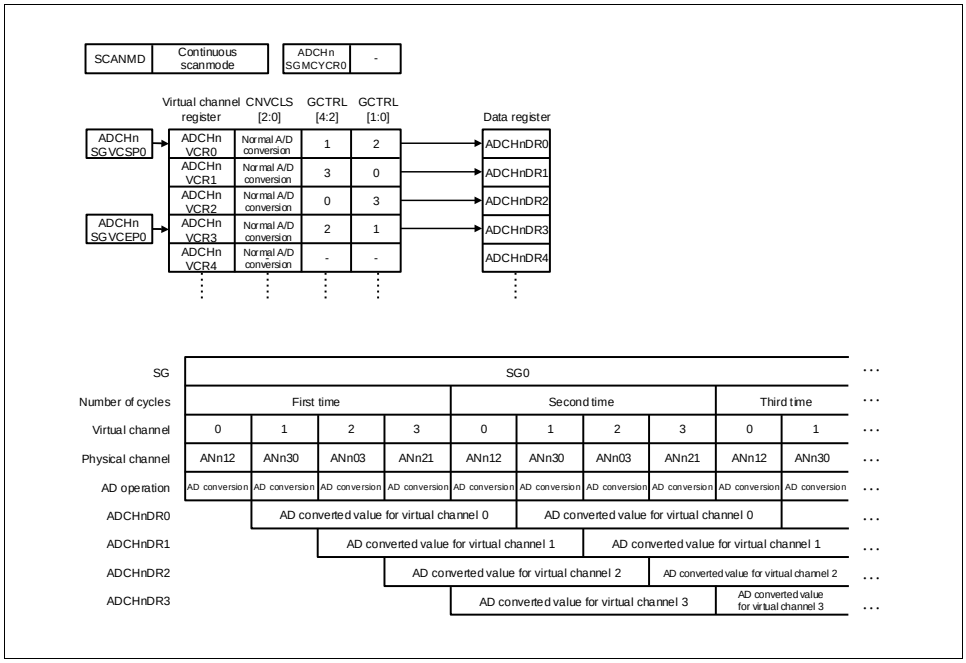

Figure 43.10 Example of Operation in Continuous Scan Mode

43.4.3 Suspend Method

When a start trigger for a scan group with higher priority is accepted during operation of a scan group with lower priority, the suspend function interrupts the scan group with lower priority and executes the scan group with higher priority.

After the processing of the scan group with higher priority is finished, the suspended scan group with lower priority resumes.

While a higher priority scanning group is operating, the start trigger for the lower priority scanning group is held pending. After the higher priority scanning group is processed, the process of the suspended lower priority scanning group is resumed.

The start trigger of the same scanning group is not accepted while the scanning group is operating or suspended.

There are three types of suspend methods.

The priority of scan groups 0 to 4 is as follows:

Low								High
SG0	<	SG1	<	SG2	<	SG3	<	SG4

43.4.3.1 Synchronous Suspend

The synchronous suspend function interrupts the processing after A/D conversion operation for the virtual channel in progress ends and then starts A/D conversion for the scan group with higher priority.

After A/D conversion for the scan group with higher priority is completed, A/D conversion for the interrupted virtual channel resumes.

The following figure shows an operation example of synchronous suspend.

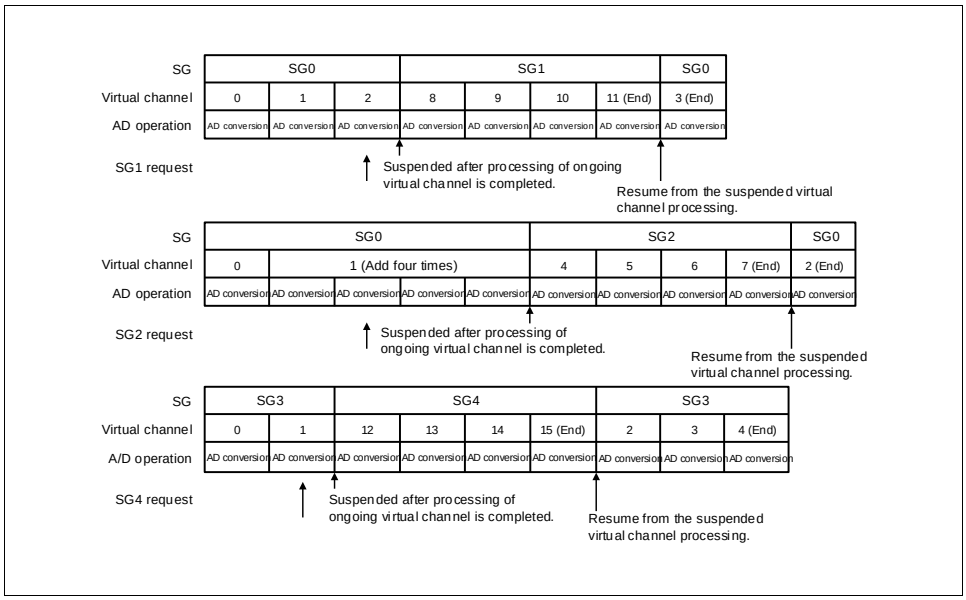

Figure 43.11 Example of Synchronous Suspend and Resume Operation

43.4.3.2 Asynchronous Suspend

The asynchronous suspend function immediately interrupts the processing without waiting until A/D conversion operation for the virtual channel in progress ends and then starts A/D conversion for the scan group with higher priority.

After A/D conversion for the scan group with higher priority is completed, A/D conversion for the interrupted virtual channel resumes from the beginning.

The following figure shows an operation example of asynchronous suspend.

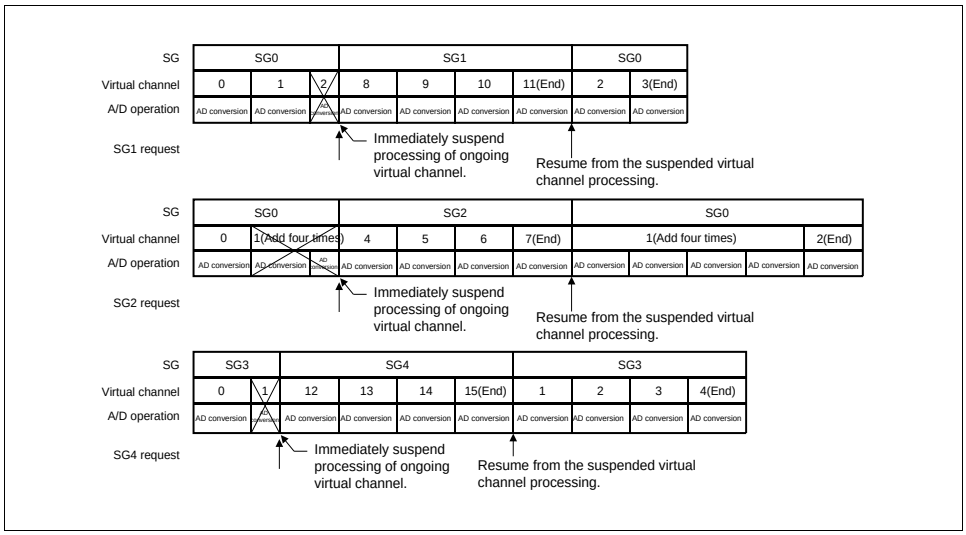

Figure 43.12 Example of Asynchronous Suspend and Resume Operation

43.4.3.3 Synchronous/Asynchronous Mixture Type Suspend

When a scan group with higher priority interrupts scan group 0, the asynchronous suspend method is applied. When a scan group with higher priority interrupts scan groups other than scan group 0, the synchronous suspend method is applied.

The following figure shows an operation example of synchronous/asynchronous-mixed suspend.

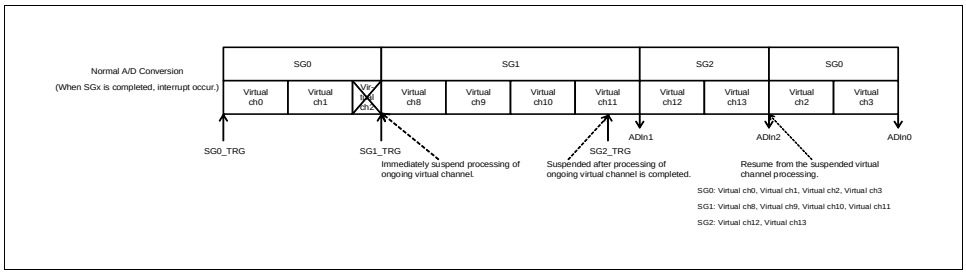

Figure 43.13 Synchronous/Asynchronous-Mixed Suspend

[Supplement] Timing when the virtual channel operation in progress becomes effective for asynchronous suspend

There is 3 clkad of latency from trigger acceptance until scan start. Therefore, even in asynchronous suspend, A/D conversion for the virtual channel in progress might end and the converted data might be stored in DR.

Trigger input timing	A/D conversion result of virtual channel in progress
cnv_cnt = 19 or shorter	Disabled → Not stored in DR
cnv_cnt = 20 to 22	Enabled → Stored in DR

43.4.4 Conversion Class

There are 5 conversion types. The conversion type must be set for each virtual channel, see **Section 43.4.13, Optional Waiting Times Insertion Function of Between Virtual Channels**.

43.4.4.1 Normal A/D Conversion

Normal A/D conversion converts an analog signal in the physical channel to a digital signal as-is.

For details about the operation, see **Section 43.4.2, Scan Mode**.

43.4.4.2 A/D Converter Self-Diagnosis

This conversion method is one of the safety functions.

A/D converter self-diagnosis A/D conversion separates the physical channel and applies the specified voltage to the analog input pin of the A/D converter to perform A/D conversion.

For details about the operation, see **Section 43.4.11.2, A/D Converter Self-Diagnosis**.

43.4.4.3 Example of Addition Mode A/D Conversion Operation

Addition mode A/D conversion converts an analog signal in the physical channel to a digital signal two or four times continuously, and then stores the addition value in the data register. The addition count (two or four times) is common among all the virtual channels.

The following figure shows an operation example:

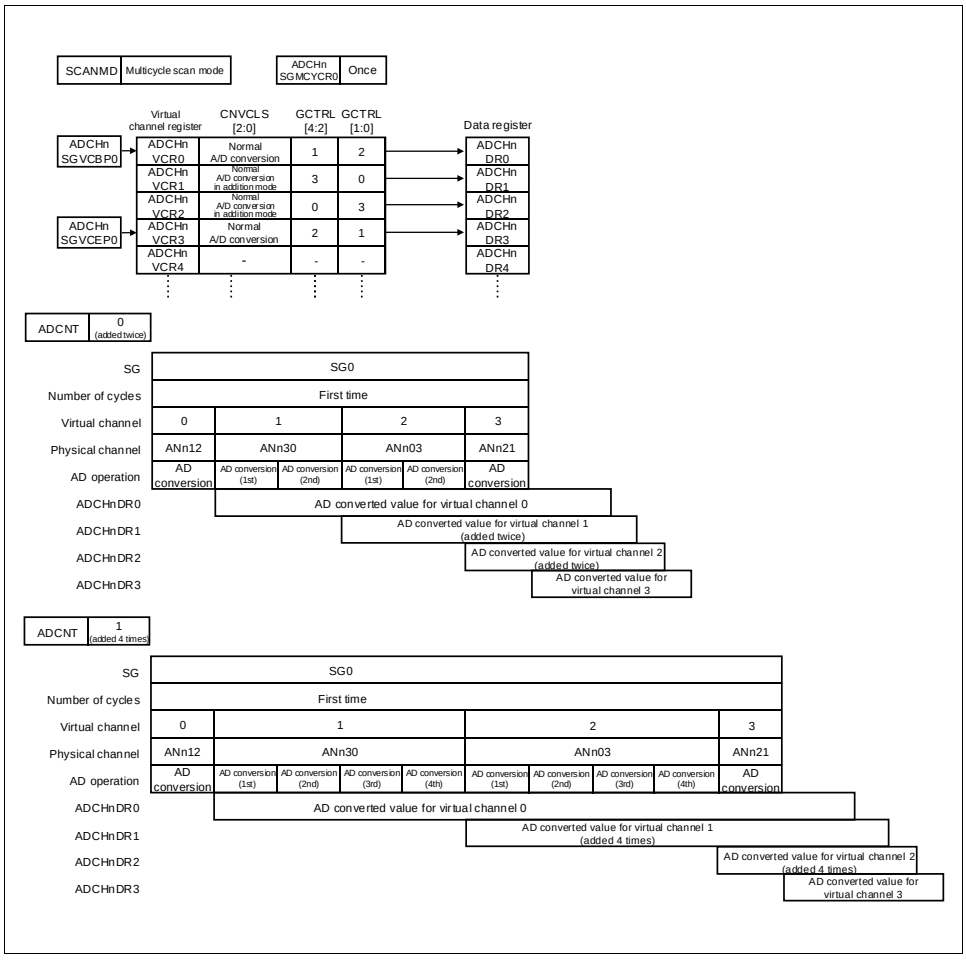

Figure 43.14 Example of Normal A/D Conversion Operation in Addition Mode

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Operation when suspend occurs during execution of addition mode A/D conversion is as follows:

Synchronous suspend:

Suspend occurs when A/D conversion ends.

Operation at resume depends on whether the state at suspend is the last A/D conversion.

Asynchronous suspend:

Suspend occurs in the middle of A/D conversion.

The processing re-executes from the first addition of the interrupted virtual channel.

43.4.4.4 Normal A/D Conversion with the MPX and Normal A/D Conversion with the MPX in Addition Mode

These functions perform A/D conversion by selecting the MPX input channel (MPX value) in the physical channel for which the MPX is connected to the external of the LSI.

There are two methods: normal A/D conversion (without addition) and addition mode A/D conversion.

To transfer the MPX value to the external of the LSI, use functions of the DMAC, IO port, and CSIH.

The following registers must be set in advance. See the specifications of each function to set the following registers:

- MPX current control register (ADCJnMPXCURCR)
- MPX command information register (ADCJnMPXCMDR)
- MPX physical channel number of the virtual channel register n (ADCJnVCRj.GCTRL[4:0])
- MPX optional wait register (ADCJnMPXOWR)
- MPX interrupt enable register (ADCJnMPXINTER)

The ADCJn operates as follows:

(1) Stores the values of ADCJnMPXCURCR, ADCJnMPXCMDR, ADCJnVCRj.GCTRL[4:0] in the MPX current register (ADCJnMPXCURR) when starting the virtual channel and outputs an interrupt signal (ADMPXIn).

(2) Output the ADCJnMPXCURR.MPXCUR[4:0] value to ADMPXn4 to ADMPXn0 when ADMPXIn outputs.

(3) Inserts wait states specified in MPXOWR.
(Waits until the MPX value is transferred by the DMAC, IO port, or CSIH and MPX output is settled.)

(4) Performs A/D conversion for the physical channel connected with the MPX.

Wait states must be set so that the MPX value transfer time and MPX output settling time can be secured.

Wait states can be set within the range from 0 to 10. 1 wait state is 40 ADCLK.

See the IO port specifications to set the mask setting value of the MPX current control register.

This setting value is used for IO port output and is not used for CSIH output.

Set the CSIH command information in the SPI command information register.

This setting value is used for CSIH output and is not used for IO port output.

Operation when suspend occurs during execution of Normal A/D Conversion with the MPX and Normal A/D Conversion with the MPX is as follows:

Synchronous suspend:

Suspend occurs when A/D conversion ends.

Operation at resume depends on whether the state at suspend is the last A/D conversion.

Asynchronous suspend:

Suspend occurs in the middle of A/D conversion.

The processing re-executes from the first wait state of the interrupted virtual channel.

(1) Using I/O Port Output

The following figure shows a structure and operation example when the DMA and IO port output are used.

- Normal A/D conversion w/MPX
- MPX wait state = 2 wait states
- ADCJnVCR2 to ADCJnVCR5 are used.

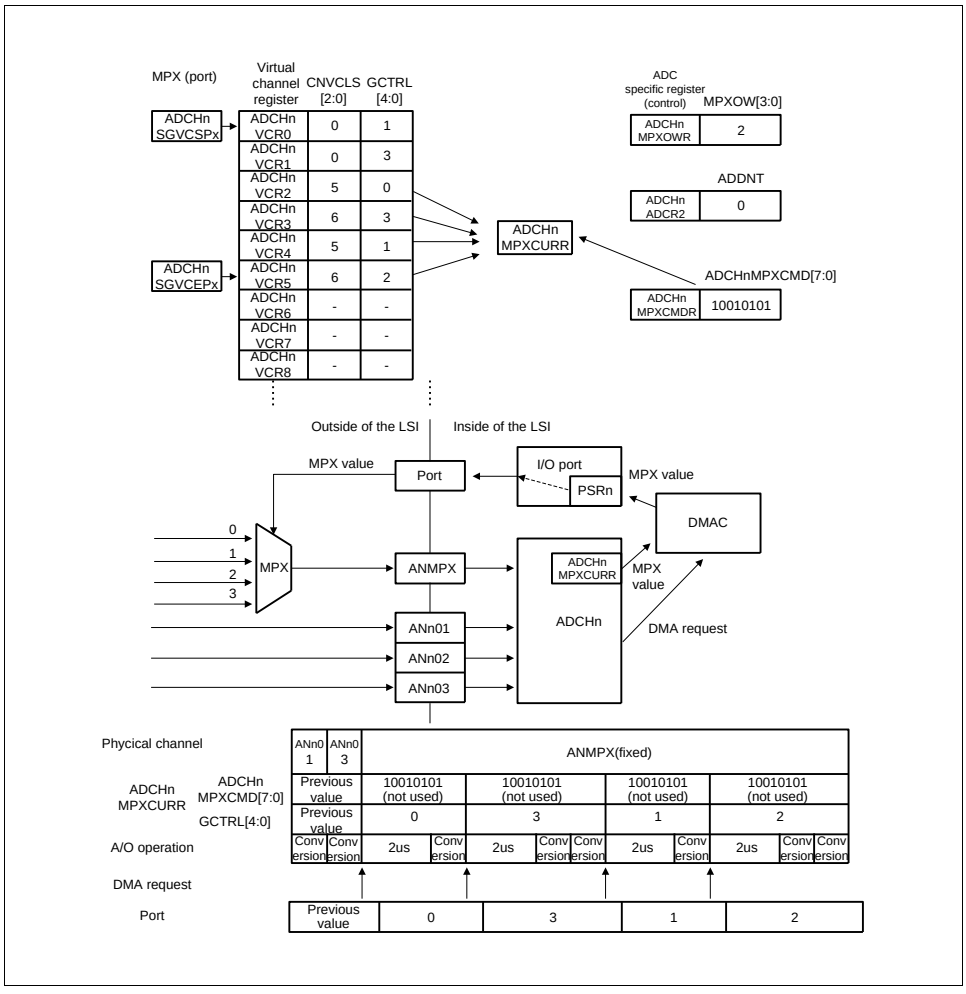

Figure 43.15 Example of Using an External Analog Multiplexer — I/O Port Output

NOTE

ADCJ0: ANMPX = AN131; ADCJ2: ANMPX = AN243; ADCJ1: ANMPX = AN100; ADCJ3: ANMPX = AN300

There are ADCJ1 and ADC3 in E2xFCC1 and E2M.

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(2) Using CSIH Output

The following figure shows a structure and operation example when the DMA and CSIH output are used.

- Addition mode A/D conversion w/MPX
- MPX wait state = 2 wait states
- ADCJnVCR2 to ADCJnVCR5 are used.

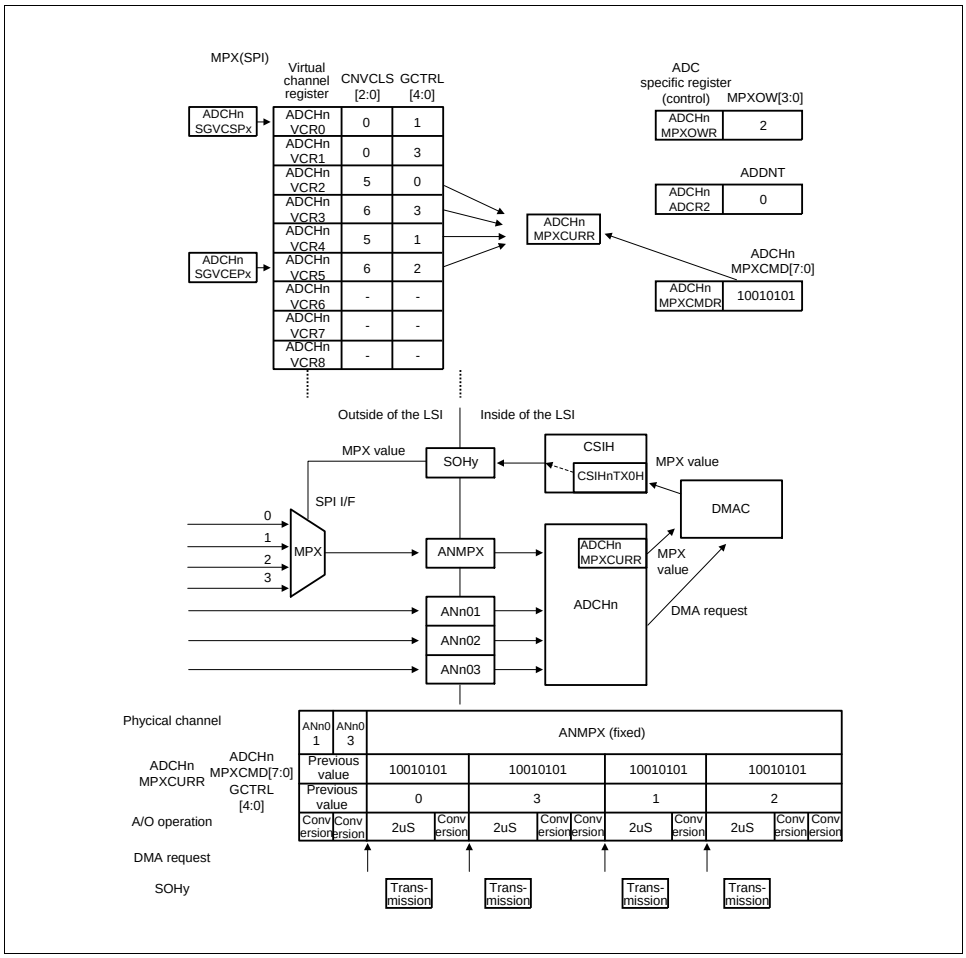


Figure 43.16 Example of Using an External Analog Multiplexer — CSIH Output

NOTE

ADCJ0: ANMPX = AN131; ADCJ2: ANMPX = AN243; ADCJ1: ANMPX = AN100; ADCJ3: ANMPX = AN300

There are ADCJ1 and ADC3 in E2xFCC1 and E2M.

43.4.5 Trigger Functions

The ADCJn has an S/W and H/W trigger.

The following table shows availability of the trigger function in each scan group:

Table 43.71 List of trigger functions for each a scan group

Classification	Function	Register bit name or terminal name	SG0	SG1	SG2	SG3	SG4
S/W Trigger	Scan Group x Starting	ADCJnSGSTCRx.SGST	√	√	√	√	√
	Scan Group x End	ADCJnSGSTPCRx.SGSTP	√	√	√	√	√
	A/D Conversion Synchronous Start	ADCJnADSYNSTCR.ADSTART	√	√	√	√	√
	A/D Abort	ADCJnADHALTR.HALT	√	√	√	√	√
	AD Timer Start	ADCJnADTSTCRy.ADTST	—	—	—	√	√
	AD Timer Synchronous Start	ADCJnADSYNSTCR.ADTSTART	—	—	—	√	√
	AD Timer end	ADCJnADTENDCRx.ADTEND	—	—	—	√	√
H/W Trigger	SGx Trigger	SGx_TRG	√	√	√	√	√

Note: √: Function present
—: Function not present

43.4.5.1 S/W Trigger

A S/W trigger occurs when a bit of a register is set to 1. Each S/W trigger possesses a single function.

(1) Scan Group x Starting Trigger

The A/D conversion of scan group x is started.

This trigger is always valid.

(2) Scan Group x Stop Trigger

The A/D conversion of scan group x is stopped.

This trigger is always valid.

(3) A/D Conversion Synchronous Start Trigger

The A/D conversion of scan group x in each ADCJ is started at the same time.

This trigger is valid for each scan group x where an A/D conversion synchronous starting enable bit of scan group x control register (ADCJnSGCRx.ADSTARTE) of each ADCJ is set 1.

(4) A/D Halt Trigger

Operation of all scan groups of the whole A/D conversion operation (including the scan group which is suspended) is halted and the internal state machine is initialized.

It is not possible to halt only a specific scan group x.

When scan group x has been started once again, scan group x cannot be resumed from the virtual channel set at the end of the prior conversion.

Processing is started from the virtual channel indicated by a start pointer.

This trigger is always valid.

(5) A/D Timer Starting Trigger

The Count operation of AD timer y is started.

It is possible to start scan group x at desired periods.

This trigger is always valid.

For details, see **Section 43.4.5.3, A/D Timer Trigger**.

(6) A/D Timer Synchronous Starting Trigger

The Count operation of A/D timer y in each ADCJ is started at the same time.

It is possible to start scan group y at the desired periods.

This trigger is valid to scan group x where the A/D timer synchronous starting enable bit of scan group y control register (SGCRy.ADTSTARTE) of each ADCJ is set 1.

For details, see **Section 43.4.5.3, A/D Timer Trigger**.

(7) A/D Timer Stop Trigger

The Count operation of AD timer y is stopped.

This trigger is always valid.

For details, see **Section 43.4.5.3, A/D Timer Trigger**.

43.4.5.2 H/W Trigger

A H/W trigger is a rising edge of SGx_TRG.

There are external triggers (ADTRGn), ATU and GTM as a trigger sources of SGx_TRG of each ADCJn, and they are chosen by the PIC. For details, refer to **Section 33, Peripheral Interconnection (PIC)**.

It functions as scan group start/AD timer start.

The function is chosen by a register setting.

(1) H/W Trigger List

The H/W trigger function chosen by each setting is indicated in the following table.

Table 43.72 H/W Trigger Functions List

SGx_TRG					ADCJnSGCRx			
4	3	2	1	0	TRGMD[1]	TRGMD[0]	SGx_TRG Functions	Notes
√	√	√	√	√	0	0	Invalid	Scan of SGx is not started.
						1	SGx scan start	
√	√	—	—	—	1	0	Invalid	Scan of SGx is not started.
						1	AD timer y start	

Note: √: Function present —: Function not present

(2) H/W Trigger Route

The route of H/W trigger input is illustrated using figure.

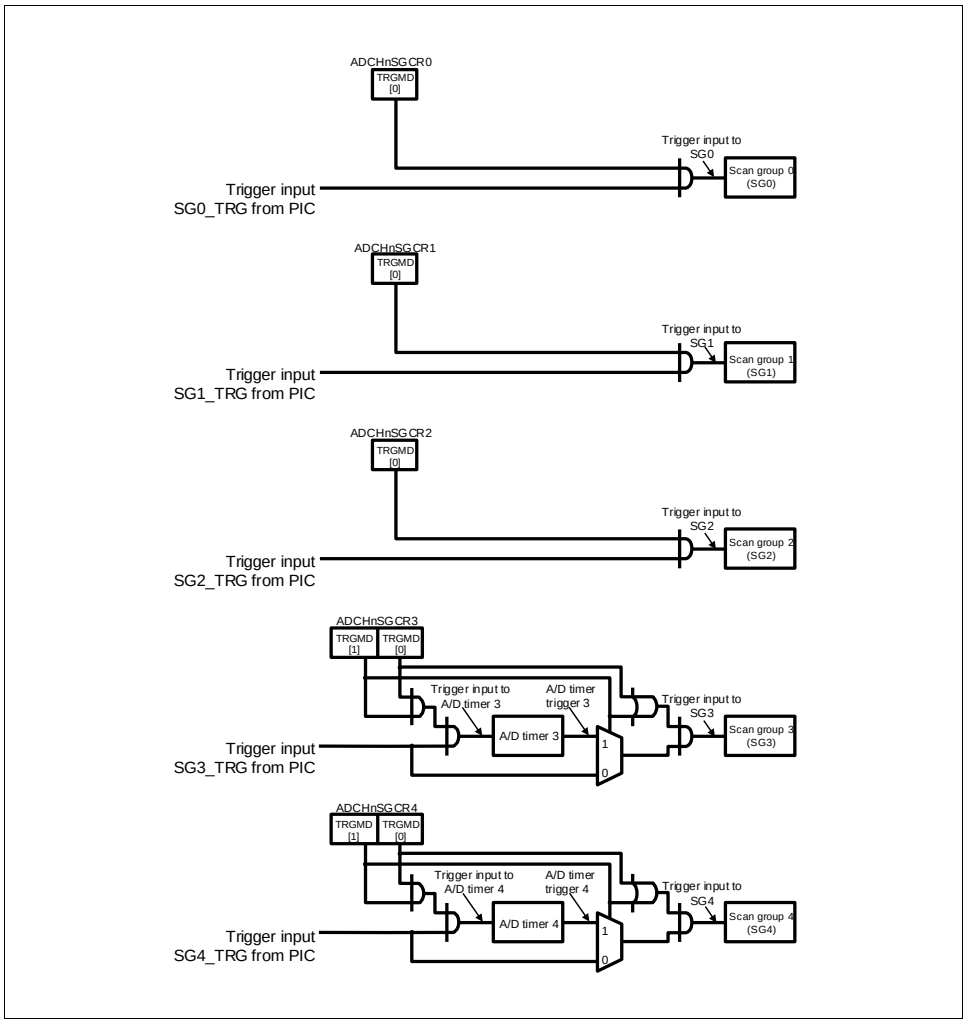


Figure 43.17 Route of Trigger Input

43.4.5.3 A/D Timer Trigger

It is possible to a start scan group y at a constant interval by using an A/D timer trigger.

The A/D timer counts in synchronization with the ADCLK.

[Recommendation flow]

The A/D timer y initial count register (ADCJnADTIPRy) and A/D timer y cycle count register (ADCJnADTPRR) must be initialized.

The range of these registers is 00_0000_H to $1F\_FFFF_H$.

Set these register so that the period of the A/D timer trigger doesn't become shorter than the execution time of scan group y.

The AD timer y is started by an AD timer starting trigger.

The AD timer y is stopped by an AD timer stop trigger or A/D conversion halt (ADCJnADHALTR.HALT = 1).

An operation example is shown in the following.

(1) When A/D timer y is started, ADCJnADTIPRx is loaded in A/D timer y and the timer counts down.

(2) When A/D timer y is reaches 0, A/D timer trigger y is output in 1 ADCLK period, and ADCJnADTPRRx is loaded in A/D timer y and the timer counts down again.

After this, Step (2) will be repeated until A/D timer y is stopped.

When A/D timer y accepts the A/D timer starting trigger after A/D timer y is stopped, it is started from step (1).

It is possible to begin an AD timer of each ADCJn at the same time by an AD timer synchronous start trigger.

The operation after a synchronous start is same as above.

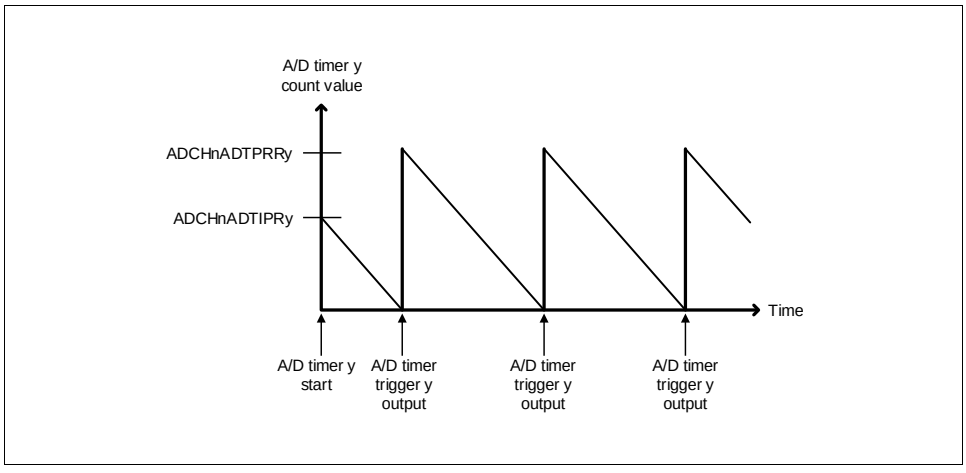


Figure 43.18 Example of A/D Timer Operation

43.4.6 Interrupt Request Functions

There is a scan end interrupt, A/D error interrupt, parity error interrupt, MPX interrupt, and upper/lower limit error interrupt.

The interrupt request is output in 1 register access clock period.

43.4.6.1 Scan End Interrupt Request

When scan group x (*1), or ADCJnVCRj has ended, a scan end interrupt request (ADInx) is generated.

A DMAC can be started by a scan end interrupt.

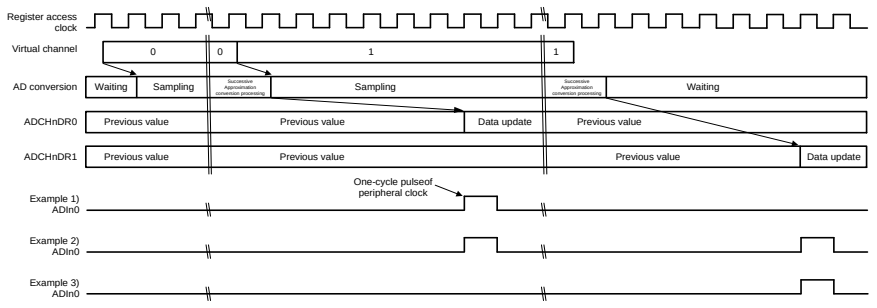
Output of ADInx is set by the permissions determined by the following bit.

- Scan end interrupt enable bit (ADCJnSGCRx.ADIE) in scan group x
- Virtual channel end interrupt enable bit (ADCJnVCRj.ADIE) in virtual channel register n

Table 43.73 ADInx Generation Permission / No Permission Settling List

ADCJnSGCRx	ADCJnVCRj		
ADIE	ADIE	ADInx Output	Generation Condition
0	0	Not permitted	—
	1	Permitted	Virtual channel j is ended
1	0	Permitted	Scan group x is ended (*1)
	1	Permitted	Scan group x is ended (*1), or virtual channel j is ended

Note 1. The meaning of 'the end the time of scan group x' is shown in the following.
- When an A/D conversion of the virtual channel indicated by 'the Scan Group x End Virtual Channel Pointer (ADCJnSGVCEPx)' is completed.
- When an A/D conversion of the virtual channel indicated by 'VCEP of the Scan Group x Virtual Channel Pointer Register (ADCJnSGVCPRx)' is completed.



Note: ADInx is generated when an A/D conversion result is stored in a data register (ADCJnDRj)

Figure 43.19 Scan Conversion End Interrupt Occurrence Timing

43.4.6.2 A/D Error Interrupt Request

When the following A/D error occurs, an A/D error interrupt (ADEn) is generated.

The generation timing of the A/D error interrupt is same as the generation timing of the scan end interrupt.

Clear the error status in the interrupt handler, after the interrupt is generated.

A/D error interrupt is generated when the OR-condition of the interrupt-enable-bit of the safety-control-register (ADCJnSFTCR) is valid.

Table 43.74 ADEn Generation Permitted List

ADCJnSFTCR			
OWEIE	IDEIE	ADEn	Generation Condition
0	0	Not permitted	—
0	1	Permitted	ID error is occurred
1	0	Permitted	Overwrite error is occurred
1	1	Permitted	Overwrite error is occurred, ID error is occurred

Each error detection is always valid.

Error status information is stored in the error register for each error.

When overwrite error were detected, the error flag bit is set 1, and the virtual channel number for the error generated is captured in the capture bit.

When ID error is detected, the error bit of the data supplementary information register j (ADCJnDIRj) which corresponds with the virtual channel (ADCJnVCRj) where an ID error is detected is set to 0. When an ID error is not detected, the error bit is set to 1.

Error status information except for that in the ADCJnDIRj.IDEF is maintained until it's cleared by the clear bit of each error flag of an error-clear-register. When the Read-and-Clear-Enable (RDCLRE) is set 1, ADCJnDIRj.IDEF maintains its status until the flag bit of the relevant error is read.

When the same error occurs once again without being cleared, the error is ignored.

If the interrupt-enable-bit is set to a valid state, when an error of following type occurs, the AD error interrupt is output.

Table 43.75 ADEn Error Factor Register List

	Error Register		Error Clear Register
Error Name	Flag Bit	Capture Bit	Clear Bit
Overwrite error	ADCJnQWER.OWE	ADCJnOWER.OWECAP[5:0]	ADCJnECR.OWEC
ID error	ADCJnDIRj.IDEF	no function.	no function.*1

Note 1. When the Read-and-Clear-Enable (RDCLRE) is set 1, and the data supplementary information register j (ADCJnDIRj) is read, the Error Clear Register clear bit set to 0.

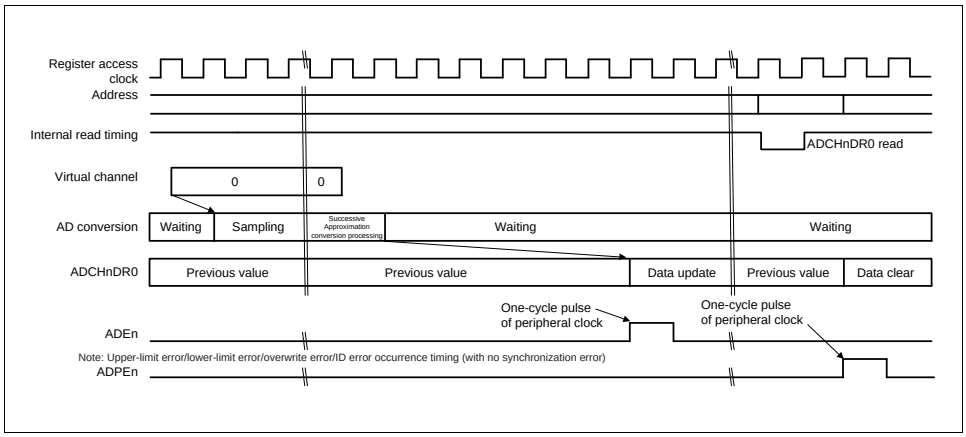


Figure 43.20 Timing of A/D Error Interrupt and Parity Error Interrupt Generation

43.4.6.3 Overwrite Error

This error indicates that the new A/D conversion result is overwritten to the data register before the data register (ADCJnDRj) is read.

When the write flag (ADCJnDIRj.WFLG) of the data accessory information register is 1 and the new A/D conversion result is stored in the corresponding data register j (ADCJnDRj), the error is detected.

43.4.6.4 ID Error

This error indicates that the physical channel specified in the virtual channel register (ADCJnVCRj) is inconsistent with the actually-converted physical channel, that is, an operational failure occurred in the internal analog switch of the IO buffer/RRAMP.

ID Error detection result is stored in the ID error bit of Data Supplementary Information Register j (ADCJnDIRj) that is corresponded to detect the Virtual Channel Register n (ADCJnVCRj) that detected ID error.

The signal level of feedback from IO buffer/RRAMP is checked.

The setting of ADCJnVCRj.GCTRL[5:0] is compared with IO buffer/RRAMP number that is activated, then when the result is not equal, the error is detected. Because IO buffer/RRAMP are controlled by one-hot, if feedback signal is not one-hot signal, the error is detected.

The ID error is detected when any of the following condition is met.

(1) Mismatched between selecting physical channel number and activated I/O buffer number.

(2) Mismatched between physical channel number that is assigned to the MPX and the I/O buffer number that is activated.*1

(3) Mismatched between activated I/O buffer number and activated RRAMP number.*2

(4) Several I/O buffer are activated when A/D conversion is executed.

(5) Several RRAMP are activated when A/D conversion is executed.

(6) Several RRAMP are activated in the period that all RRAMP output should off when A/D conversion is executed.

Note 1. Because there are no feedback from MPX, the check cannot be done comparing with MPXvalue.

Note 1. The RRAMP number of physical channel number change by ADCJn. For a detail description, please see **Section 43.1.6, External Input/Output Signals**.

The detection condition changes by detect factor.

Table 43.76 ID Error Detect List

Class of Conversion	(1)	(2)	(3)	(4)	(5)	(6)
Normal A/D conversion	√	—	√	√	√	√
Normal A/D conversion in addition mode	√	—	√	√	√	√
Normal A/D conversion with MPX	—	√	√	√	√	√
Normal A/D conversion with MPX in addition mode	—	√	√	√	√	√
A/D convertor self-diagnosis	—	—	—	—	—	—

43.4.6.5 Parity Error Interrupt Request

The ADCJn can issue a Parity Error notification (ADPEn) to the ECM.

The Parity Error is detected in second cycle when ADCJmDRj or ADCJmDIRj is read.

The Parity Error notification is generated by parity error when ADCJnSFTCR.PEIE is set to 1.

The Parity Error can checked by reading ADCJnDIRj.PRTY.

The parity bit is even parity for ADCJnDRj and ADCJnDIRj.IDEF.

The error status information is stored in PER register. When parity error is detected, PER.PE is set to 1 and PER.PRCAP[5:0] is set the virtual channel number that generate parity error.

The error status information is cleared by writing to 1 to ADCJnECR.PEC.

When PER.PE is set, next error is ignored, but when ADCBnSFTCR.PEIE is set to 1, the parity error is output to ECM if next error is generated.

43.4.6.6 MPX Interrupt Request

The ADCJn can issue an MPX interrupt request (ADMPXIn) to the INTC.

If the MPX-interrupt-enable-bit is set to a valid (ADCJnMPXINTER.ADMPXIE = 1) level, ADMPXIn is generated when a virtual channel for which normal-A/D-conversion-with-MPX (ADCJnVCRj.CNVCLS[2:0] = 5_H) or normal-A/D-conversion-with-MPX-in-addition-mode (ADCJnVCRj.CNVCLS[2:0] = 6_H) is started.

In both cases such as MPX wait and wait between virtual channels, ADMPXIn is output 4 register access clocks after the conversion is started.

The DMAC can be activated when an ADMPXIn occurs.

If the MPX-interrupt-enable-bit was set to an invalid state (ADCJnMPXINTER.ADMPXIE = 0), ADMPXIn is not output.

However, the ADMPXn0 to ADMPXn4 of the output ports is updated irrespective of the value of ADCJnMPXINTER.ADMPXIE.

ADMPXn0 to ADMPXn4 is output just as ADCJnMPXCURR.MPXCUR[4:0] is transferred, so the update timing is the same as ADCJnMPXCURR.MPXCUR[4:0].

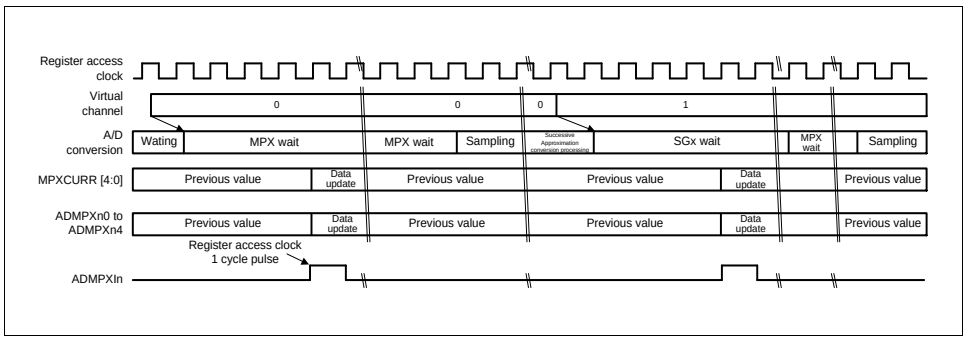


Figure 43.21 Timing of an MPX Interrupt Occurrence

43.4.6.7 Virtual Channel Upper/Lower Limit Error Interrupt

ADCJn detects that the A/D conversion result is above the upper limit or below the lower limit for each virtual channel, and generates an interrupt request (INT_ULn).

(1) Setting Registers

INT_ULn is to set the upper/lower-limit-error-interrupt-enable-bit (ADCJnVCLMINTER1.ADULjIE, ADCJnVCLMINTER2.ADULjIE) and the virtual-channel-upper-limit-excess-notice-enable-bit (ADCJnVCRj.VCULME) or virtual-channel-lower-limit-excess-notice-enable-bit (ADCJnVCRj.VCLLME) as 1, and this function is set to valid or invalid in each virtual channel.

When it is set as valid, the result which compares the A/D conversion result with the virtual-channel-upper/lower-limit-table-register (ADCJnVCULLMTBR0 to ADCJnVCULLMTBR6) is output to INT_ULn.

When ADULnIE is set as “0” or both of VCULME and VCLLME are set as “0”, INT_ULn is not output (the output is fixed low.)

Table 43.77 INT_ULn, vcend[j], vculmo and vcllmo Output Setting

ADULjIE	VCULME	VCLLME	INT_ULn	vculmo	vcllmo	vcend[j]
0	0	0	—	—	—	—
		1	—	—	√	√
	1	0	—	√	—	√
		1	—	√	√	√
1	0	0	—	—	—	—
		1	√	—	√	√
	1	0	√	√	—	√
		1	√	√	√	√

Note: For details of vcend[j], vculmo and vcllmo, first see **Figure 43.27** and see **Section 43.4.9, Virtual Channel Upper/Lower Limit Excess Notice**.
√: Valid —: Invalid

The output condition of the upper/lower limit error interrupt signal (INT_ULn) is as follows.

Precondition: When the A/D conversion value is greater than the upper limit value or less than the lower limit value.

(1) INT_ULn is not output irrespective of the setting of VCULME and VCLLME if ADULjIE=0.

(2) INT_ULn is not output irrespective of the setting of ADULjIE if VCULME=0 and VCLLME=0.

(3), (4), (5) When ADULjIE = 1 and both of VCULLME, VCLLME are set to “1” or VCULLME = 1 or VCLLME = 1, INT_ULn is output at same timing as scan end interrupt (ADIn).

When the class of conversion is "normal A/D conversion in addition mode", INT_ULn is output only after the end of the addition number of times of the designated A/D virtual channel.

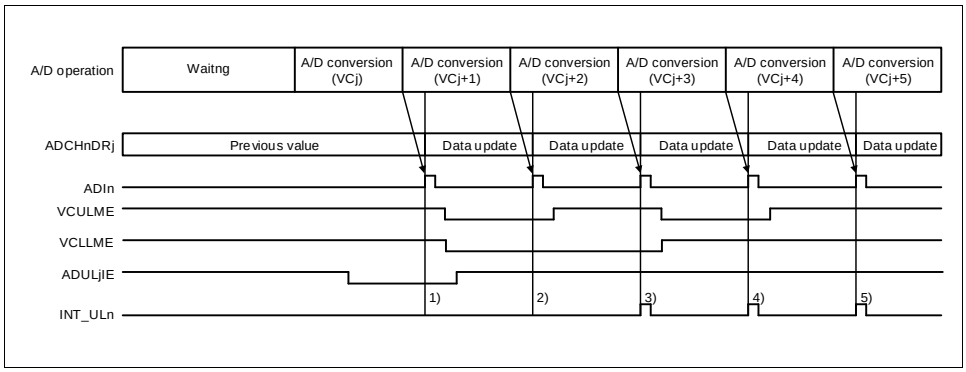


Figure 43.22 Output Condition of Upper / Lower Limit Error Interrupt

Table 43.78 INT_ULn Output Permitted List for Each Conversion Class

ADCJnVCRj. CONVCLS[2:0]	Conversion Class	Valid / Invalid	Notes
0_H	Normal A/D conversion	√	
1_H	Setting prohibited	—	
2_H	Setting prohibited	—	
3_H	A/D converter self-diagnosis	√	
4_H	Normal A/D conversion in addition mode	√	It is asserted only at the end of the designated addition counts.
5_H	Normal A/D conversion with the MPX	√	
6_H	Normal A/D conversion with the MPX in addition mode	√	It is asserted only at the end of the designated addition counts.
7_H	Setting prohibited	—	

Note: √: Valid —: Invalid

(2) Table Registers

See **Section 43.4.9.2, Table Registers**.

(3) Interface Signals

When this function is set as valid, every time A/D conversion in a virtual channel ends, a table register is compared with an A/D conversion result, and INT_ULn is output.

INT_ULn is a common signal for all virtual channels.

INT_ULn is one-shot-pulse signal output by a register access clock.

It's possible to determine the detected number of the virtual channel by reading the virtual-channel-upper/lower-limit-excess-status-register 1 (ADCJnVCLMSR1) and virtual-channel-upper/lower-limit-excess-status-register 2 (ADCJnVCLMSR2).

(4) Operating Timing

INT_ULn signals are synchronized with the register access clock.

Asserting-timing of this signal is the same as the assert-timing of a scan end interrupt signal (ADIn).

The operating timing chart is indicated below.

- 1st comparison period: A/D conversion result = 0x7FF8, INT_ULn is generated by upper limit value excess and flag is set.
- 2nd comparison period: A/D conversion result = 0x4FF8, INT_ULn is generated by lower limit value excess and flag is set.

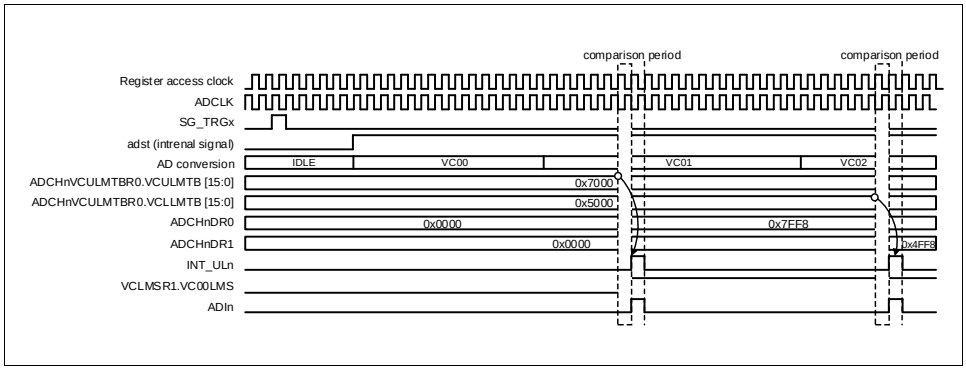


Figure 43.23 Timing Chart of Upper / Lower Limit Error Interrupt

43.4.7 DFE/ GTM/ASF Entry Function

The ADCJn can issue a request for entry to the DFE or GTM and a request for entry to the ASF for DFE, GTM, and ASF according to the settings of DFENT in ADCJnVCRj and DFENTSGxE and ASENTSGxE in ADCJnDFASENTSGER. At the same time, ADCJn outputs the TAG information and A/D conversion data that are set in DFTAG in ADCJnVCRj. For the format of the output A/D conversion data, see **Section 43.3.3.2, ADCJnPWDVCR — PWM-Diag Virtual Channel** Register

ADCJnPWDVCR is a 32-bit readable register to control PWM-Diag virtual channels.

Because a value set by the register of another macro PWSC is input as a PVCR_VALUE[17:0] value in the control by the PWM-Diag function, ADCJnPWDVCR is an insubstantial register.

Value after reset 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	WTTS[3:0]			
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MPXE	MPXV[2:0]			VCULLMTBS[3:0]				—	—	GCTRL[5:0]					
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 43.25 ADCJnPWDVCR Register Contents

Bit Position	Bit Name	Function
31 to 20	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
19 to 16	WTTS[3:0]	Wait Time Table Select 0 H: Disabled 1 H: WAITTR0 is chosen. 2 H: WAITTR1 is chosen. 3 H: WAITTR2 is chosen. 4 H: WAITTR3 is chosen. 5 H: WAITTR4 is chosen. 6 H: WAITTR5 is chosen. 7 H: WAITTR6 is chosen. 8 H: WAITTR7 is chosen. Other than above: Setting prohibited.
15	MPXE	MPX Enable When operating this this bit, set MPXE in the register of the PWSD module. 0: Normal A/D conversion is performed. The MPXV[2:0] value is not transferred to the output pin PVCR_MUXCUR[2:0]. No wait is inserted before A/D conversion starts. 1: MPX normal A/D conversion is performed. The MPXV[2:0] value is transferred to the output pin PVCR_MUXCUR[2:0]. A wait is inserted before A/D conversion starts.
14 to 12	MPXV[2:0]	MPX Value When operating these bits, set MPXV[2:0] in the register of the PWSD module. Use this bit to select an MPX channel of the external analog multiplexer.
11 to 8	VCULLMTBS[3:0]	Upper/Lower Limit Check Table Register Select When operating these bits, set VCULLMTBS[3:0] in the register of the PWSD module. Select the upper/lower limit check table register to be compared. 0 H: Disabled 1 H: VCULLMTBR0 is chosen.

		2 H: VCULLMTBR1 is chosen. 3 H: VCULLMTBR2 is chosen. 4 H: VCULLMTBR3 is chosen. 5 H: VCULLMTBR4 is chosen. 6 H: VCULLMTBR5 is chosen. 7 H: VCULLMTBR6 is chosen. 8 H: VCULLMTBR7 is chosen. Other than above: Setting prohibited.
7 to 6	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
5 to 0	GCTRL[5:0]	When operating these bits, set GCTRL[5:0] in the register of the PWSC module. GCTRL[5:2]: Set the physical channel group number. GCTRL[1:0]: Set the physical sub channel number. Example of setting: To specify ANn10, set GCTRL[5:2]: = 1H and GCTRL[1:0] = 0H. To specify ANn62, set GCTRL[5:2]: = 7H and GCTRL[1:0] = 2H.

CAUTION

When using MPX normal A/D conversion, be sure to insert a wait.

NOTE

1. VCULLMTBS[3:0] in PWDVCR and VCULLMTBS[3:0] in VCRn are the same function.
2. PVCR_VALUE[17:0] is allocated to the following bits.
   PVCR_VALUE[17:14]=WTTS[3:0]
   PVCR_VALUE[13]=MPXE
   PVCR_VALUE[12:10]=MPXV[2:0]
   PVCR_VALUE[9:6]= VCULLMTBS[3:0]
   PVCR_VALUE[5:0]= GCTRL[5:0]

ADCJnDRj — Data Register j.

For allocation of each ADCJn and each channel of DFE, refer to **Section 37, Digital Filter Engine (DFE)**.

For allocation of each ADCJn and each channel of GTM, refer to **Section 31 Generic Timer Module (GTM)**.

For allocation of ADCJ0 and each channel of ASF, refer to **Section** Error! Reference source not found.**,** Error! Reference source not found..

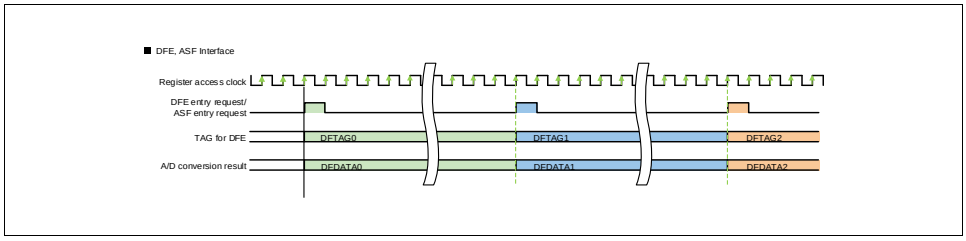


Figure 43.24 DFE / ASF Entry Timing

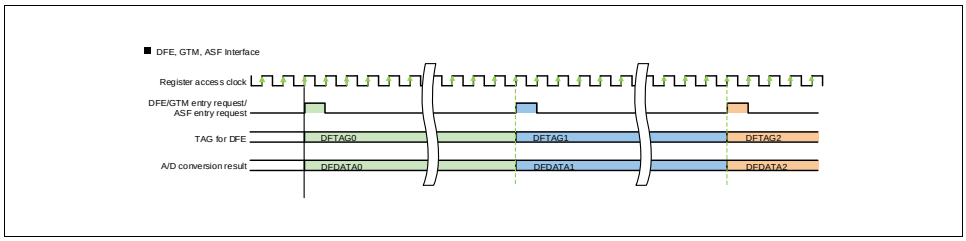


Figure 43.25 DFE/ GTM/ ASF Entry Timing

43.4.8 Monitoring Function Using the A/D Conversion Monitor Pin

ADENDn can be used to monitor the processing timing of the virtual channel specified by ADCJnADENDP. For details of pin settings, see **Section 2, Pin Function**.

Figure 43.26 shows the A/D conversion monitor timing.

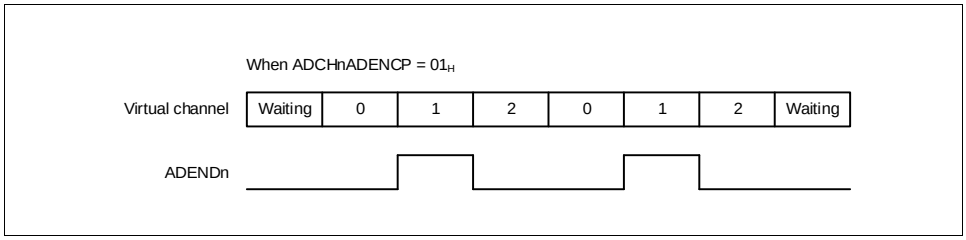


Figure 43.26 A/D Conversion Monitor Timing

CAUTION

If the high-level voltage is output from ADENDn in a lower-priority scan group and a higher-priority scan group suspends (asynchronous suspend) the processing of the lower-priority scan group, the low-level voltage is output from ADENDn. Since the suspended virtual channel processing for the lower-priority scan group resumes after that, the high-level voltage is output again from ADENDn.

43.4.9 Virtual Channel Upper/Lower Limit Excess Notice to ADC VMON Secondary Error Generator (AVSEG) (For RH850/E2x-FCC1, E2M, E2L), or to ADC VMON Secondary Error Generator (AVSEG), or to ADC Boundary Flag Generator (ABFG)

The ADCJn can detects that the A/D conversion result is greater than the upper limit value or less than the lower limit value for each virtual channel, and it is possible to notify the ADC VMON secondary error generator (AVSEG) (For RH850/E2x-FCC1, E2M, E2L), or the ADC VMON secondary error generator (AVSEG), or ADC boundary flag generator (ABFG).

43.4.9.1 Setting Registers

It is possible to set this function as valid or invalid in each virtual channel if the virtual-channel-upper-limit-excess-notice-enable-bit (ADCJnVCRj.VCULME) or virtual-channel-lower-limit-excess-notice-enable-bit (ADCJnVCRj.VCLLME) is set.

When it is set as valid, the A/D conversion result is compared with the virtual-channel-upper/lower-limit-table-register (ADCJnVCULLMTBR0 to ADCJnVCULLMTBR6) and is output to vcend[j] (A/D conversion end notice), vculmo (virtual channel upper limit excess notice) and vcllmo (virtual channel lower limit excess notice).

When both of VCULME and VCLLME are set to “0”, vculmo, vcllmo, and vcend[j] are not output (output is fixed low).

For details of vculmo, vcllmo, and vcend[j], see **Figure 43.27**.

Table 43.79 vcend[j], vculmo and vcllmo Output Setting

VCULME	VCLLME	Virtual Channel Upper Limit Excess Noticevculmo	Virtual Channel Lower Limit Excess Noticevcllmo	A/D Conversion End Noticevcend[j]
0	0	—	—	—
	1	—	√	√
1	0	√	—	√
	1	√	√	√

Note: √: Valid —: Invalid

Table 43.80 vcend[j], vculmo and vcllmo Notice Function Valid/ Invalid List for Each Conversion Class

ADCJnVCRj. CONVCLS[2:0]	Conversion Class	Valid / Invalid	Notes
0_H	Normal A/D conversion	√	
1_H	Setting prohibited	—	
2_H	Setting prohibited	—	
3_H	A/D converter self-diagnosis	√	
4_H	Normal A/D conversion in addition mode	√	It is asserted only at the end of the designated addition counts.
5_H	Normal A/D conversion with the MPX	√	
6_H	Normal A/D conversion with the MPX in addition mode	√	It is asserted only at the end of the designated addition counts.
7_H	Setting prohibited	—	

Note: √: Valid —: Invalid

43.4.9.2 Table Registers

The virtual-channel-upper/lower-limit-table-register (VCULLMTBR0 to VCULLMTBR6) are specified by the VCULLMTBS [2:0] bits of the virtual channel register (ADCJnVCRj).

The upper limit value table and the lower limit table are sets.

Therefore it isn't possible to choose the lower limit table for the register number different from the upper limit value table in one virtual channel.

Set the upper limit value to the upper-side 16 bits of the chosen VCULLMTBR and set the lower limit value to the lower-side 16 bits of the chosen VCULLMTBR.

Write using a 32 bit width. This register cannot be written using a 16 bit width or 8 bit width.

VCULLMTBR0 to VCULLMTBR6 can be rewritten at any time irrespective of the timing before scan group start and after scan group start.

Table 43.81 Correlation between ADCJnVCRj.VCULLMTBS[2:0] and VCULLMTBR0 to VCULLMTBR6

ADCJnVCRj. VCULLMTBS[2:0]	Register Name	Upper Limit Side Condition	Lower Limit Side Condition
0_H	VCULLMTBR0	A/D conversion value > VCULMTB[15:0]	A/D conversion value < VCLLMTB[15:0]
1_H	VCULLMTBR1		
2_H	VCULLMTBR2		
3_H	VCULLMTBR3		
4_H	VCULLMTBR4		
5_H	VCULLMTBR5		
6_H	VCULLMTBR6		
7_H	Setting prohibited		

43.4.9.3 Interface Signals

When this function is used, every time an A/D conversion in a virtual channel has ended, a table register is compared with an A/D conversion result, and vcend[j] (A/D conversion end notice), vculmo (virtual channel upper limit excess notice) and vcllmo (virtual channel lower limit excess notice) are output.

vcend[j], vculmo and vcllmo are one-shot-pulse signals output by the register access clock.

These signals are output when the A/D conversion ends.

vcend[j] is output irrespective of the result of the comparison.

Only when the upper limit value excess is detected, vculmo is output, and only when the lower limit value excess is detected, vcllmo is output.

vculmo and vcllmo are common signals for all virtual channels.

It's possible to determine the detected number of the virtual channel by using a pair of vcend[j] and vculmo, or using a pair of vcend[j] and vcllmo.

For details of vculmo, vcllmo, and vcend[j], see **Figure 43.27**.

Table 43.82 vcend[j], vculmo and vcllmo Output Timing

Signal Name	Means	Operation	Synchronizing Clock
vcend[j]	Virtual channel A/D conversion end notice	It is output at the A/D conversion end.	register access clock
vculmo	Virtual channel upper limit excess notice	When it occurs, it is output at the time of A/D conversion end.	
vcllmo	Virtual channel lower limit excess notice	When it occurs, it is output at the time of A/D conversion end.	

43.4.9.4 Operating Timing

The operation timing chart is indicated below.

vcend[j], vculmo and vcllmo are the signals which are with the register access clock.

Assert-timing of these signals is same as the assert-timing of the scan end interrupt signal (ADIn).

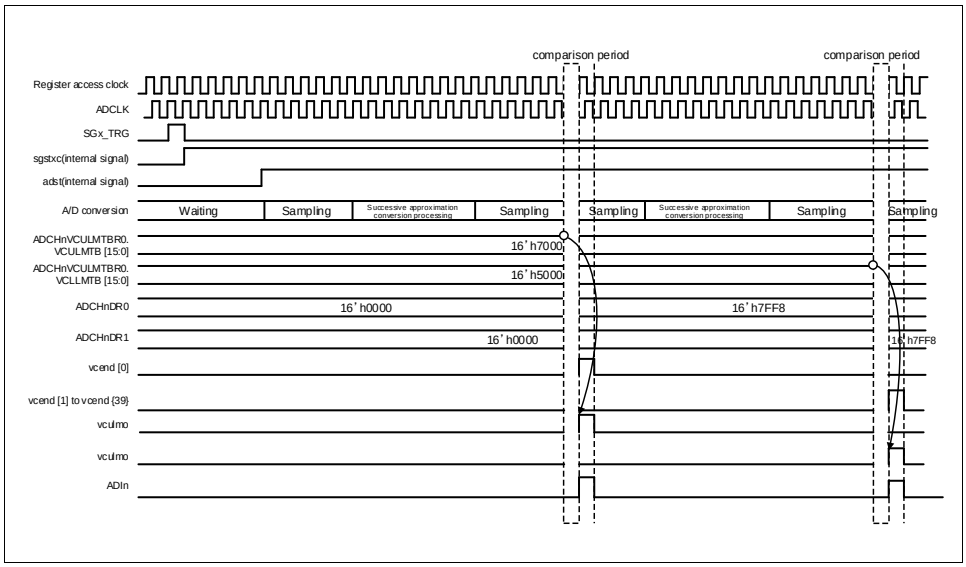


Figure 43.27 Output Timing Chart of Virtual Channel Upper / Lower Limit Excess Notice

The following diagram shows the timing chart when ADCJnDRj storage and ADCJnVCLLMTBR rewrite compete against each other.

Comparison is performed 1 register access clock period before ADCJnDRj storage. Therefore, if ADCJnDRj storage and ADCJnVCULLMTBR rewrite are performed simultaneously, the previous value of ADCJnVCULLMTBR is used for comparison.

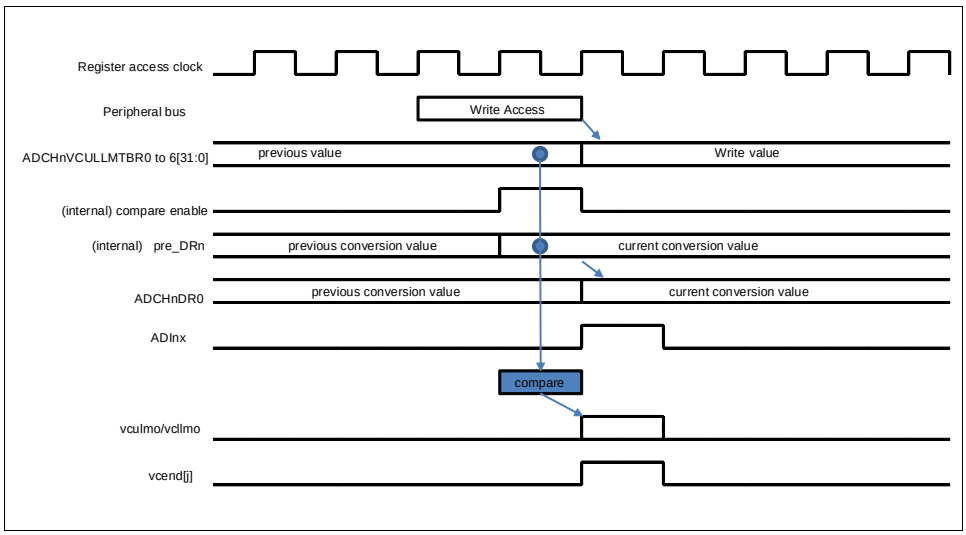


Figure 43.28 Timing Chart of Competition of Storing of ADCJnDRj and Rewriting of ADCJnVCULLMTBR

43.4.10 Wiring-Break Detection Function

The wiring-break detection function detects a wiring-break of the ANI. If a wiring-break is present, the conversion result attenuates to approximately 0 V, and an abnormal value is detected in the conversion result. This can be determined as a wiring-break. For details timing, refer to **Figure 43.29**.

[Feature]

(1) Users can select desired physical channels for which the wiring-break is to be detected.

[Settings]

(1) Set registers according to the initial settings (**Figure 43.5**).

(2) Set CNVCLS[2:0] in the virtual channel register ADCJnVCRj to 0_H and set GCTRL[5:0] to select desired channels.

(3) Set ODE in the wiring-break detection control register to 1_H and set ODPW[5:0] to specify the desired wiring-break detection pulse width.

(4) Assert SG0 to SG4 trigger signals to perform an A/D conversion.

(5) When the read A/D conversion result has attenuated to approximately 000h, judge that a wiring-break has occurred.

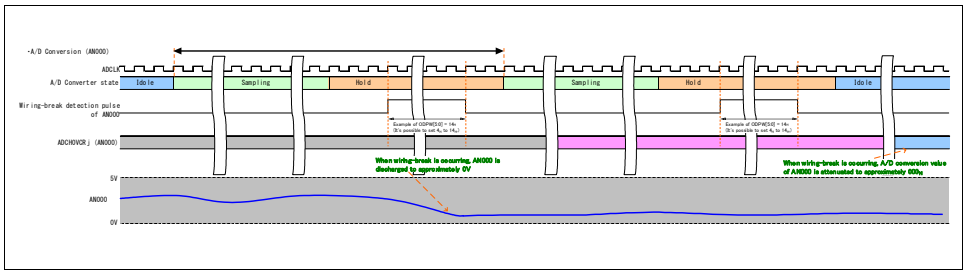


Figure 43.29 Timing Chart of Wiring-Break Detection Function

43.4.11 Self-Diagnostic Functions

The ADC is equipped with the following four self-diagnostic functions.

- Pin-level self-diagnosis
- A/D conversion circuit self-diagnosis
- Wiring-break detection self-diagnosis
- Secondary power supply voltage monitor self-diagnosis (For RH850/E2x-FCC1, E2M, E2L)
- Secondary power supply voltage monitor self-diagnosis

43.4.11.1 Pin-Level Self-Diagnosis

The pin-level self-diagnosis performs an A/D conversion that is set to a different voltage for even-numbered physical channel groups and odd-number physical channel groups to check for an abnormal path from the analog input.

When an A/D conversion result is not a static value, there is a possibility that the A/D converter is broken.

[Analog input route]

I/O Buffer → RRAMP → A/D Converter

[Recommendation flow]

Set the virtual channel register j (ADCJnVCRj) and pin level self-diagnosis register (ADCJnTDCR) according to the initial setting flow.

ADCJnVCRj

VCR number	CNVCLS[2:0]	GCTRL[5:0]
N	0H	ANIxx number

ADCJnTDCR

ADCJnTDCR		Injection Voltage to Physical Channel Group	
TDE	TDLV[1:0]	Even Group	Odd Group
0	*	—	—
1	0H	AnVSS	AnVCC
1	1H	AnVCC	AnVSS
1	2H	AnVSS	1/2 x AnVCC
1	3H	1/2 x AnVCC	AnVSS

Note: Don't use the pin level self-diagnosis function and the wiring-break-detection functions at same time.

Allocate the above-mentioned virtual channel n to scan group x.

Refer to the start flow chart, start the scan group x, and execute A/D conversions.

43.4.11.2 A/D Converter Self-Diagnosis

The A/D converter(A/D core) self-diagnosis is used to verify that A/D conversion operates correctly.

When the A/D conversion value is different from the expected value, there is a possibility that the A/D converter is broken.

The voltage value setting is made in GCTRL[4:0] when CNVCLS[2:0] = 3_H, and can be converted for AnVREFH × 1, AnVREFH × 3/4, AnVREFH × 1/2, AnVREFH × 1/4, and AnVREFH × 0.

Features of the A/D conversion circuit self-diagnosis are described below.

[Recommendation flow]

(1) Set registers according to the initial settings (**Figure 43.5**).

(2) Set CNVCLS[2:0] in the virtual channel register ADCJnVCRj (n = 0 to 47) to 3_H and set GCTRL[5:0] to specify the desired self-diagnosis voltage level.

(3) Set registers required for A/D conversion according to the initial settings (**Figure 43.5**).

(4) Assert SG0 to SG4 trigger signals to perform A/D conversions.

43.4.11.3 Wiring-Break Detection Self-Diagnosis

The self-diagnosis function of wiring-break detecting function is used to check that the wiring-break detecting function works normally.

A/D conversion execute in disabling ANI input and pull-down the ANI by ADCJnODCR setting. A/D conversion repeat several times, then the A/D conversion result of pull-down becomes lower to 0.1 V or below, the wiring-break detecting function is judged to be working normally. For the detail, refer to **Figure 43.30**.

A user can select the physical channel to do the self-diagnosis of detection the wiring-break by virtual channel setting.

The sample flow shows as below.

1) Set the initial value (refer to (**Figure 43.5**))
2) Set the physical channel by setting of ADCJnVCRj of CNVCLS[2:0] = 0_H and GCTRL[5:0].
3) Set ADCJnODCR (ODE and ODDE bit to 1 and ODPW[5:0].
4) Execute the A/D conversion by asserting SG0-4 trigger.
5) After repeat the A/D conversion several times, read the result of A/D conversion value. If the value attenuates to approximately 0V, the wiring-break detecting function is judged to be working normally.

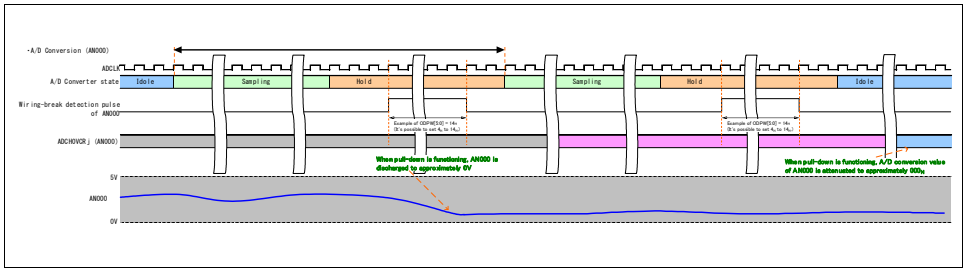


Figure 43.30 Timing Chart of Wiring-Break Detection Self-Diagnosis

43.4.11.4 Secondary Power Supply Voltage Monitor Self-Diagnosis (For RH850/E2x-FCC1, E2M, E2L)

The self-diagnosis function of secondary power supply voltage monitor function is used to check that the secondary power supply voltage monitor function works normally.

A/D conversion is performed when divided resistance is off by VMONVDCR1 and VMONVDCR2. Then the A/D conversion result becomes proximity 0V, the function is judged to be working normally.

When secondary power supply voltage monitor self-diagnosis function is used, A/D conversion of power supply and secondary power supply voltage monitor self-diagnosis should alternately be performed each power supply. For operation example, refer to **Figure 43.31**.

The sample flow shows as below.

1) Set the initial value (refer to (**Figure 43.5**))
2) Set the secondary power supply voltage monitor channel by setting of ADCJ0VCRj of CNVCLS[2:0] = 0_H and GCTRL[5:0] (VCC=28, EVCC=29, VDD=30).
3) Set VDE1 = 1 and dummy read x N times[*1], VDE2 set to 1.
4) Wait 500ns[*2], A/D conversion is performed, then check that the result is same as power supply voltage.
5) Set VDE1 = 0 and dummy read x N times[*1], VDE2 set to 0.
6) Wait 500ns[*2], A/D conversion (secondary power supply voltage monitor self-diagnosis) is performed, then check that the result is approximately 0V.

NOTE

When not using ADCJ0DIRj, set Read-and-Clear-Enable (ADCJ0SFTCR.RDCLRE) to 0.

Note 1. This is nonoverlap period for divided resistance switch and pull-down switch. 2 cycles according to Register access clock is guaranteed by the register access. Please delete it if the dummy read is unnecessary in the product evaluation.

Note 2. This is settling time of while divided resistance is disabling or enabling. When the settling time is unnecessary after the product evaluation, please delete it.

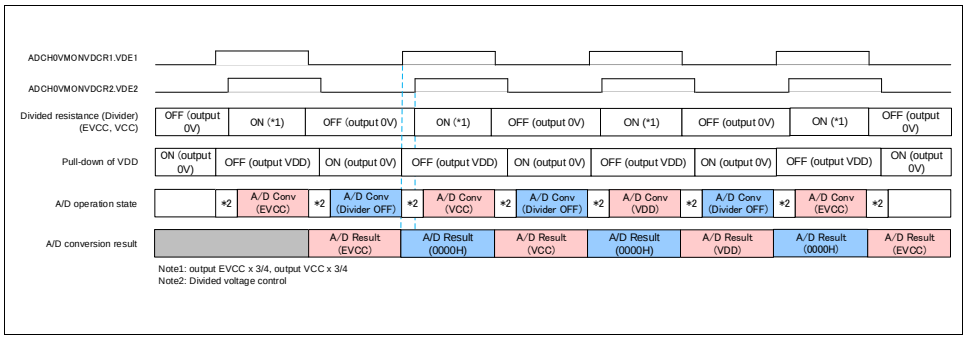


Figure 43.31 Example of Operation of Secondary Power Supply Voltage Monitor Self-Diagnosis

43.4.11.5 Secondary Power Supply Voltage Monitor Self-Diagnosis

The self-diagnosis function of secondary power supply voltage monitor function is used to check that the secondary power supply voltage monitor function works normally.

A/D conversion is performed when divided resistance is off by VMONVDCR1 and VMONVDCR2. Then the A/D conversion result becomes proximity 0V, the function is judged to be working normally.

When secondary power supply voltage monitor self-diagnosis function is used, A/D conversion of power supply and secondary power supply voltage monitor self-diagnosis should alternately be performed each power supply. For operation example, refer to **Figure 43.32**.

The sample flow shows as below.

7) Set the initial value (refer to (**Figure 43.5**))
8) Set the secondary power supply voltage monitor channel by setting of ADCJ0VCRj of CNVCLS[2:0] = 0_H and GCTRL[5:0] (VCC=28, EVCC=29, VDD=30).
9) Set VDE1 = 1 and dummy read x N times*1, VDE2 set to 1.
10) Wait 500ns*2, A/D conversion is performed, then check that the result is same as power supply voltage.
11) Set VDE1 = 0 and dummy read x N times*1, VDE2 set to 0.
12) Wait 500ns*2, A/D conversion (secondary power supply voltage monitor self-diagnosis) is performed, then check that the result is approximately 0V.

NOTE

When not using ADCJ0DIRj, set Read-and-Clear-Enable (ADCJ0SFTCR.RDCLRE) to 0.

Note 1. This is nonoverlap period for divided resistance switch and pull-down switch. 2 cycles according to Register access clock is guaranteed by the register access. Please delete it if the dummy read is unnecessary in the product evaluation.

Note 2. This is settling time of while divided resistance is disabling or enabling. When the settling time is unnecessary after the product evaluation, please delete it.

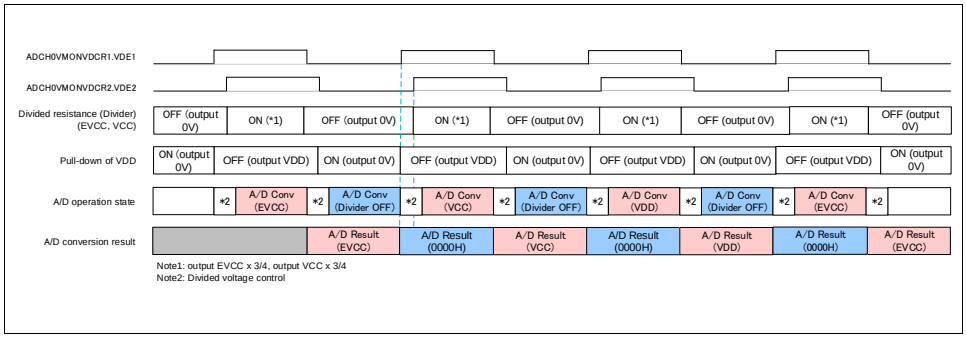


Figure 43.32 Example of Operation of Secondary Power Supply Voltage Monitor Self-Diagnosis

43.4.12 Timing Regulations

The operating timing of ADCJn is shown below.

Table 43.83 Timing in Normal A/D Conversion

Item	Symbol	Period	Unit
Scan group start delay time	tD	(2 to 4) × Pϕ + 5 × Iϕ	Pϕ (register access clock) Iϕ (ADCLK)
Sampling time	tSPL	18 × Iϕ	Iϕ (ADCLK)
Successive approximation conversion processing time	tSAR	22 × Iϕ	Iϕ (ADCLK)
Scan group end delay time	tED	(2 to 4) × Iϕ + 3 × Pϕ	Pϕ (register access clock) Iϕ (ADCLK)
Scan group processing time	tSG	47 × Iϕ + 5 × Pϕ to 49 × Iϕ + 7 × Pϕ	Pϕ (register access clock) Iϕ (ADCLK)

The processing time for a scan group (tSG) can be obtained from the following formula, where the number of virtual channels is i and the number of multicycles is j in multicycle scan mode:

$$tSG = tD + (tSPL + tSAR) \times i \times j + tED$$

The processing time for the first cycle of a scan in continuous scan mode is as follows:

$$tD + (tSPL + tSAR) \times i$$

The processing time for the second (or subsequent) cycle of a scan in continuous scan mode is as follows:

$$(tSPL + tSAR) \times i$$

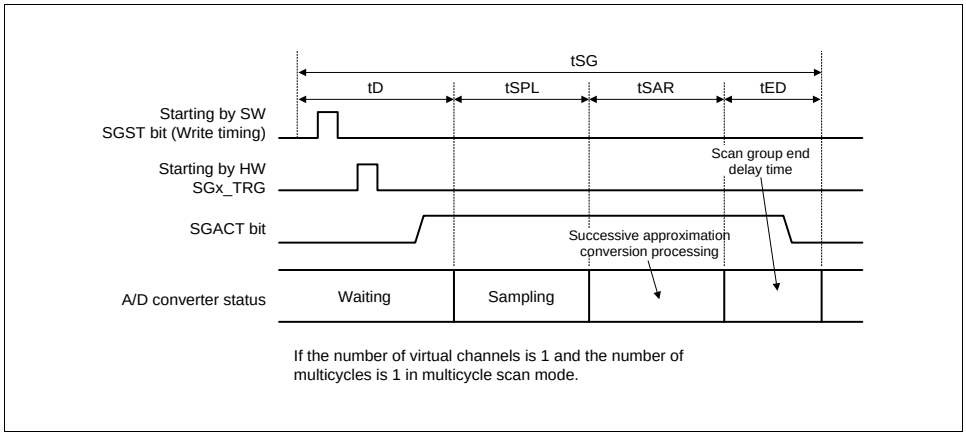


Figure 43.33 Timing Chart of Normal A/D Conversion Operation

43.4.13 Optional Waiting Times Insertion Function of Between Virtual Channels

The wait function is the function to insert any wait time in the processing between a virtual channel processing and a virtual channel processing. The wait time can set each scan group, but cannot set difference time in same scan group.

When using normal A/D conversion in addition mode, the wait cannot be insert in adding (2 times addition mode: within second A/D conversion, 4 times addition mode: within forth A/D conversion).

And after processing last virtual channel, the wait is not asserted independently of A/D conversion type in scan group.

43.4.13.1 Waiting Times Insertion in Normal A/D Conversion

When the normal A/D conversion is executed by using the wait function, a wait is inserted between virtual channel processes regardless of using MPX wait function.

A sample case shows in **Figure 43.34**.

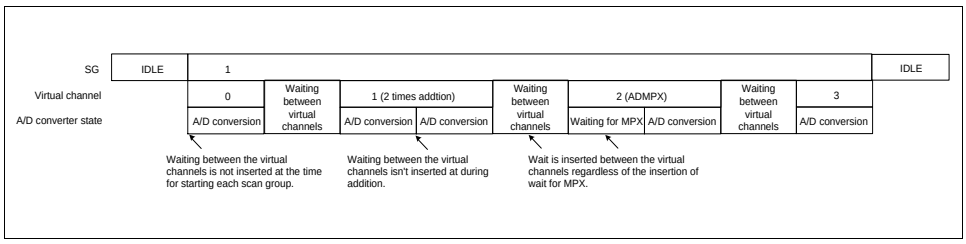


Figure 43.34 Example of Operation of Waiting Timing Insertion in Normal A/D Conversion

43.4.13.2 Waiting Time Insertion in Synchronous Suspend Movement

There are two cases that scan group with higher priority (SG2) interrupt to scan group with lower priority (SG1).

<Case 1> Processing a virtual channel of scan group with lower priority (SG1)

<Case 2> Waiting between virtual channels of scan group with lower priority (SG1)

A sample case shows in **Figure 43.35**.

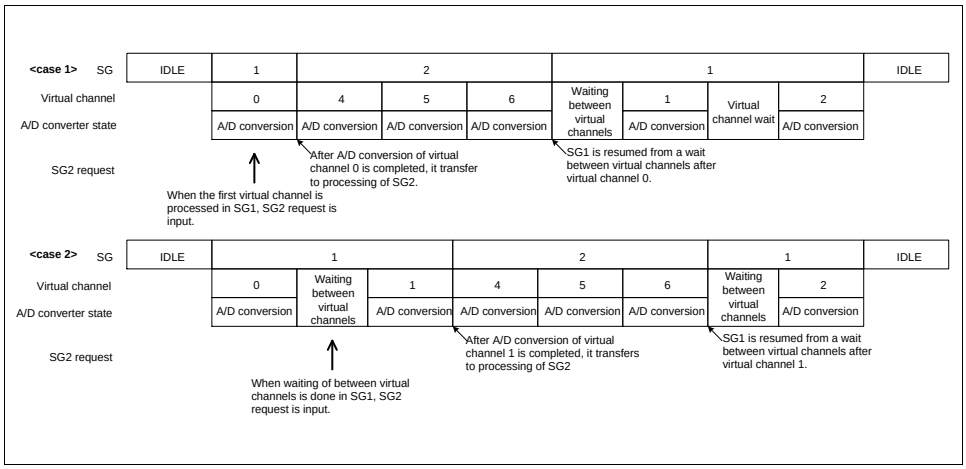


Figure 43.35 Example of Operation of Waiting Timing Insertion in Synchronous Suspend Movement

43.4.13.3 Waiting Times Insertion in Asynchronous Suspend Movement

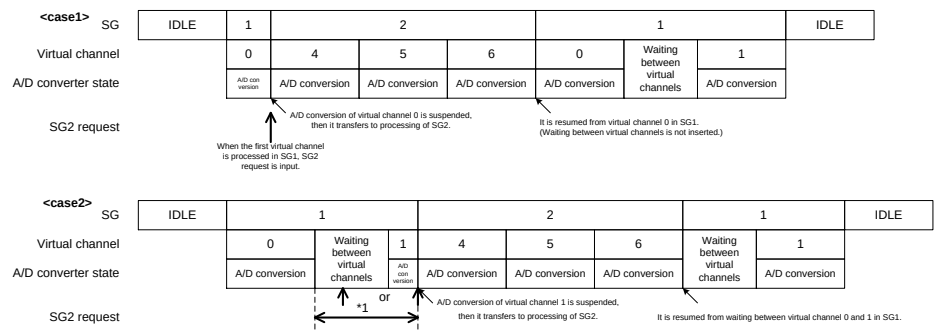
There are two cases that scan group with higher priority (SG2) interrupt to scan group with lower priority (SG1).

<Case 1> First virtual channel processing of scan group with lower priority (SG1)

<Case 2> Except first virtual channel processing of scan group with lower priority (SG1) or Interval a virtual channel processing.

When a scan group with lower priority (SG1) restart, a wait is not asserted in <Case 1>, but a wait is asserted in <Case 2>.

A sample case shows in **Figure 43.36**.



Note 1. When a virtual channel besides the first is processed in SG1 (scan group with lower priority), SG2 (scan group with higher priority) request is input. Or, when waiting between virtual channels is done in SG1, SG2 request is input.

Figure 43.36 Example of Operation of Waiting Timing Insertion in Asynchronous Suspend Movement

43.4.14 Example of Scan Group Stop

The example shows about the function of all scan groups stop (ADCJnADHALTR.HALT) and each scan group stop (ADCJnSGSTPCRx.SGSTP).

43.4.14.1 Example of All Scan Group Stop (A/D Halt)

When ADCJnADHALTR.HALT is set to 1, all scan groups and all AD timers are halted and initialized, and the ADC becomes the idle state (ADCBnSGSRx.SGACT = 0).

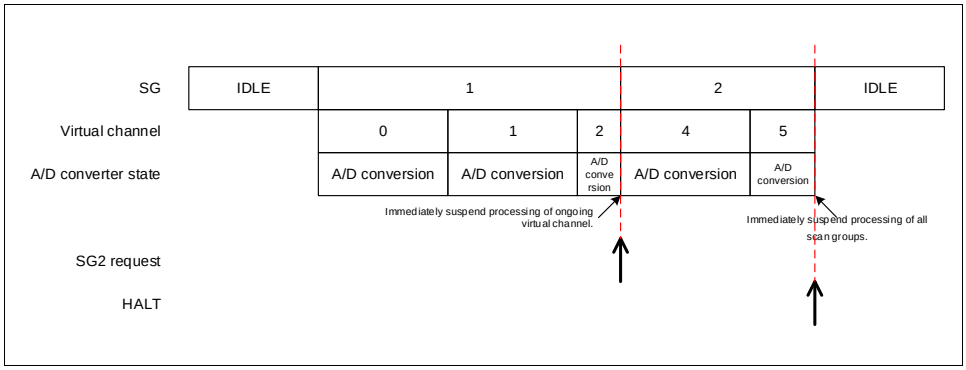


Figure 43.37 Example of All Scan Group Stop (A/D Halt)

43.4.14.2 Example of Scan Group x Stop

When ADCJnSGSTPCRx.SGSTP is set to 1, corresponding scan group become to be idle state after finishing current virtual channel process. A sample case shows in **Figure 43.38**.

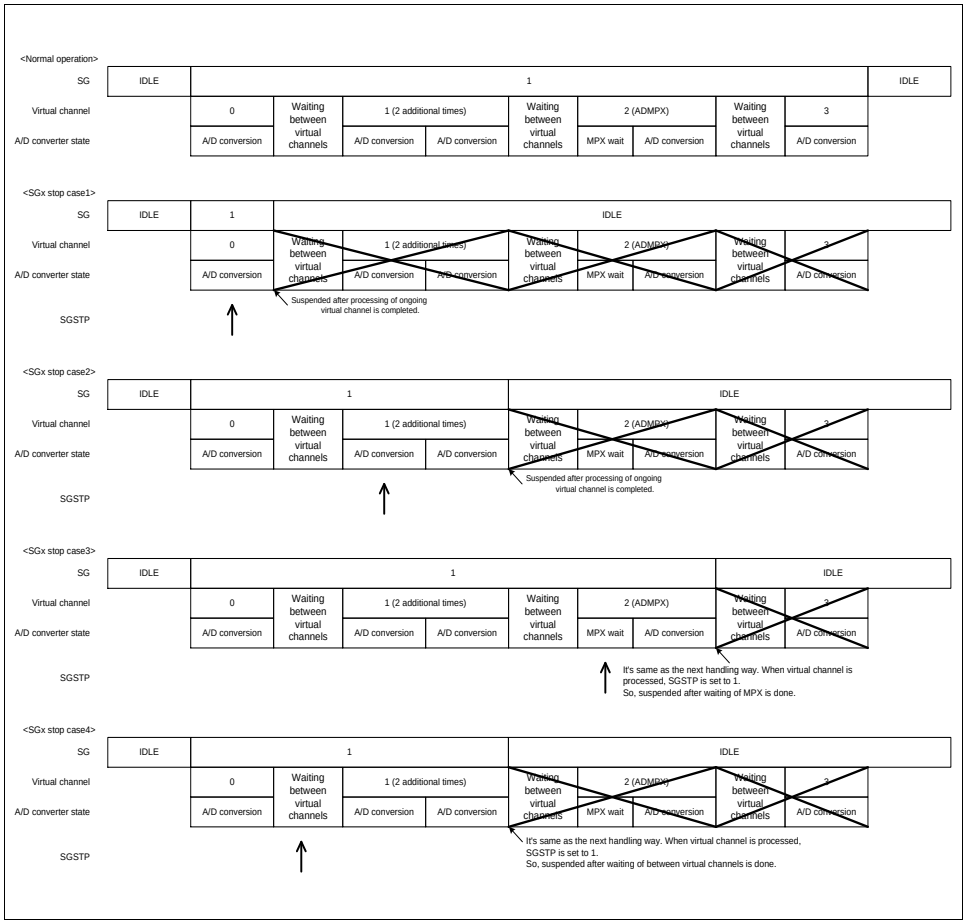


Figure 43.38 Example of Scan Group x Stop 1

When ADCJnSGSTPCRx.SGSTP is set to 1 in suspend state by synchronous suspend function or asynchronous suspend function,

ADCJ not resume and shift the idle state (SGACT = 0).

The **Figure 43.39** shows the case when asynchronous suspend is occurred by higher priority scan group in processing A/D conversion.

When synchronous suspend is occurred by higher priority scan group in processing A/D conversion,

ADCJ shift the idle state (SGACT = 0) after A/D conversion operation for the virtual channel is finished.

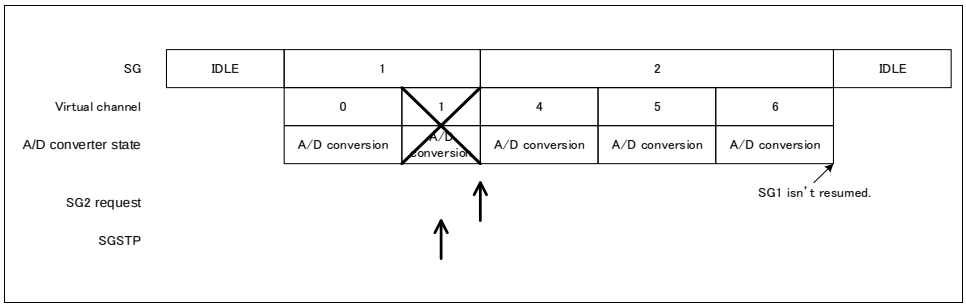


Figure 43.39 Example of Scan Group x Stop 2

43.4.15 Secondary Power Supply Voltage Monitor Function (For RH850/E2x-FCC1, E2M, E2L)

ADCJ0 can convert the voltage of VCC, EVCC, and the VDD power supply in AD. When voltage divider enable bit 1 and 2(VDE1 and VDE2) of voltage monitor voltage divider control register 1 and 2 (ADCJ0VMONVDCR1 and ADCJ0VMONVDCR2) are set as 1, it is possible to perform A/D conversion of each power supply voltage.

About VCC and EVCC, A/D conversion of divided voltage are performed.

For self-diagnosi flow of secondary power supply voltage monitor function, refer to **Section 43.4.11.4 Secondary Power Supply Voltage Monitor Self-Diagnosis (For RH850/E2x-FCC1, E2M, E2L)**.

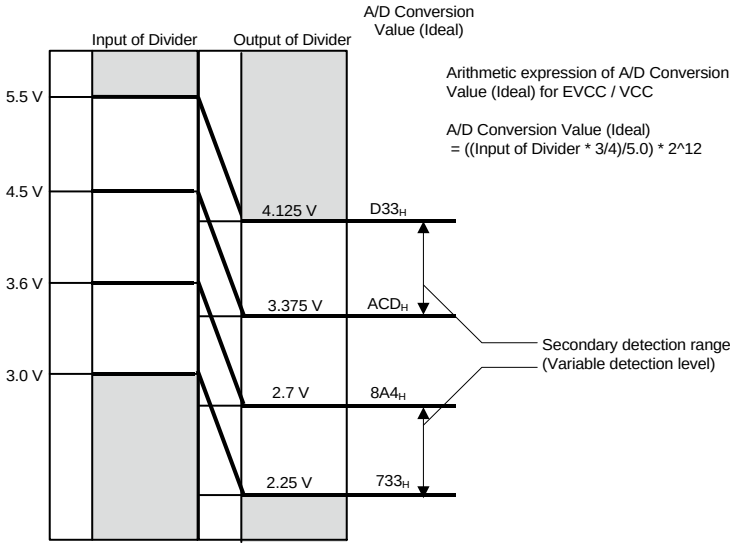
[Recommendation flow]

1) Set the initial value (refer to **Figure 43.5**)
2) Set CNVCLS[2:0] =0H, and set each power supply voltage (VCC=28, EVCC=29, VDD=30) to GCTRL[5:0] of ADCJ0VCR0, ADCJ0VCR1, and ADCJ0VCR2. (When they are three consecutive ADCJ0VCRj, arbitrary setting is permitted.).
   Additionally, set VCULME=1, VCLLME=1 and VCULLMTBS[2:0] =corresponding ADCJ0VCULLMTBR. (this procedure (from "Additionally,") was added by product development member)
3) Set VDE1 = 1 and dummy read x N times (*1), VDE2 set to 1.
4) Set upper limit value and lower limit value of each power supply voltage to ADCJ0VCULLMTBR0, ADCJ0VCULLMTBR1 and ADCJ0VCULLMTBR2 (any of ADCJ0VCULLMTBR (ADCJ0VCULLMTBR0 to ADCJ0VCULLMTBR6) are able to be used as voltage monitor). For reference value of upper / lower limit value, refer to **Figure 43.40**. (this procedure was added by product development member)
5) Set AVSEGVCCCHSCR (for VCC), AVSEGEVCCCHSCR (for EVCC) and AVSEGVDDCHSCR (for VDD) to allocate virtual channels which corresponds to each power source. For details of this setting, refer to **Section 43.7 ADC VMON Secondary Error Generator (AVSEG)**. (this procedure was added by product development member)
6) Allocate AVSEGVCCCHSCR (for VCC), AVSEGEVCCCHSCR (for EVCC) and AVSEGVDDCHSCR (for VDD) a virtual channel which corresponds to each power source. For details of this setting, refer to **Section 43.7 ADC VMON Secondary Error Generator (AVSEG)**. (this procedure was added by product development member)
7) Wait 500ns (*2), start SG, and perform A/D conversion.

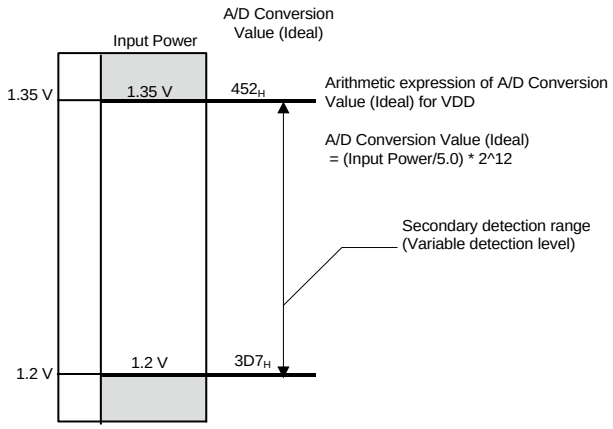
Note 1. This is nonoverlap period for divided resistance switch and pull-down switch. 2 cycles according to Register access clock is guaranteed by the register access. Please delete it if the dummy read is unnecessary in the product evaluation.

Note 2. This is settling time of while divided resistance is disabling or enabling. When the settling time is unnecessary after the product evaluation, please delete it.

EVCC / VCC Condition: A0VCC=A0VREFH=5.0 V



VDD Condition: A0VCC=A0VREFH=5.0 V



Note 1. EVCC can't be guaranteed operation in 3V (3.0 to 3.6V), can be guaranteed operation in 5V (4.5 to 5.5V).

Note 2. Set the upper / lower limit value as the value with which the absolute error of A/D conversion of power supply voltage is added to a reference value of this figure.

Figure 43.40 Reference Value of Upper / Lower Limit Value of Secondary Power Supply Voltage Monitor (this figure is added by product development member)

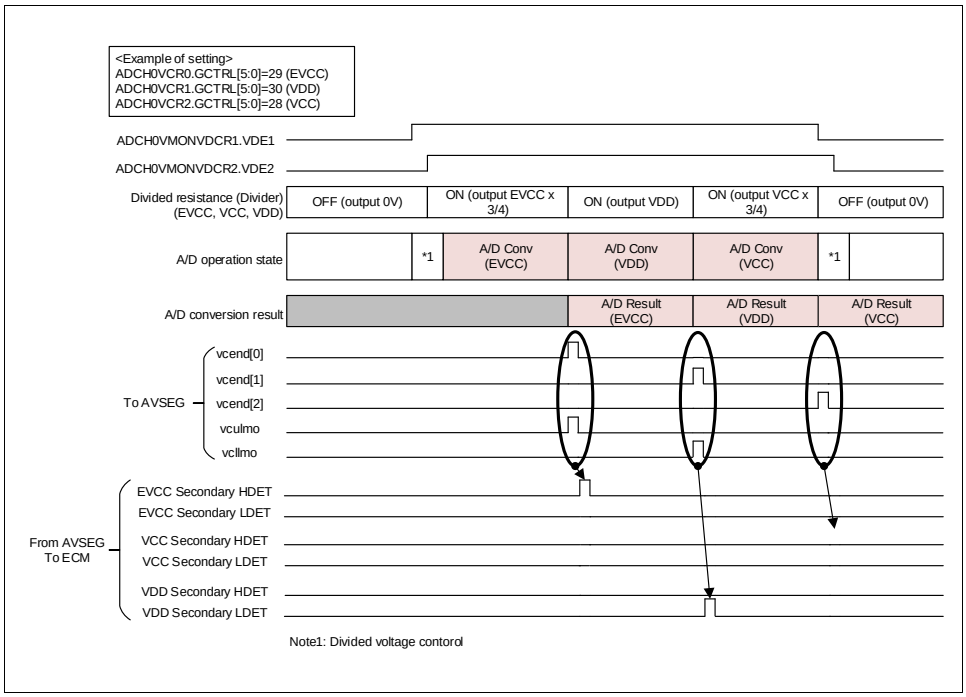


Figure 43.41 Example of Operation of Secondary Power Supply Voltage Monitor

NOTE

- When making it to the module standby, set VDE1 and VDE2 as 0 respectively, before it changes to the module standby.
- Please remove voltage fluctuation of A0VREFH as much as possible. (Please guide the value of the swinging width of A0VREFH, and the set value of the virtual channel upper/lower limit table register after evaluating a product.).

43.4.16 Secondary Power Supply Voltage Monitor Function

ADCJ0 can convert the voltage of VCC, EVCC, and the VDD power supply in AD. When voltage divider enable bit 1 and 2(VDE1 and VDE2) of voltage monitor voltage divider control register 1 and 2 (ADCJ0VMONVDCR1 and ADCJ0VMONVDCR2) are set as 1, it is possible to perform A/D conversion of each power supply voltage.

About VCC and EVCC, A/D conversion of divided voltage are performed.

For self-diagnosi flow of secondary power supply voltage monitor function, refer to **Section 43.4.11.5 Secondary Power Supply Voltage Monitor Self-Diagnosis**.

[Recommendation flow]

8) Set the initial value (refer to **Figure 43.5**)

9) Set CNVCLS[2:0] =0H, and set each power supply voltage (VCC=28, EVCC=29, VDD=30) to GCTRL[5:0] of ADCJ0VCR0, ADCJ0VCR1, and ADCJ0VCR2. (When they are three consecutive ADCJ0VCRj, arbitrary setting is permitted.).
Additionally, set VCULME=1, VCLLME=1 and VCULLMTBS[2:0] =corresponding ADCJ0VCULLMTBR. (this procedure (from "Additionally,") was added by product development member)

10) Set VDE1 = 1 and dummy read x N times (*1), VDE2 set to 1.

11) Set upper limit value and lower limit value of each power supply voltage to ADCJ0VCULLMTBR0, ADCJ0VCULLMTBR1 and ADCJ0VCULLMTBR2 (any of ADCJ0VCULLMTBR (ADCJ0VCULLMTBR0 to ADCJ0VCULLMTBR6) are able to be used as voltage monitor). For reference value of upper / lower limit value, refer to **Figure 43.42**. (this procedure was added by product development member)

12) Set AVSEGVCCCHSCR (for VCC), AVSEGEVCCCHSCR (for EVCC) and AVSEGVDDCHSCR (for VDD) to allocate virtual channels which corresponds to each power source. For details of this setting, refer to **Section** Error! Reference source not found. Error! Reference source not found.. (this procedure was added by product development member)

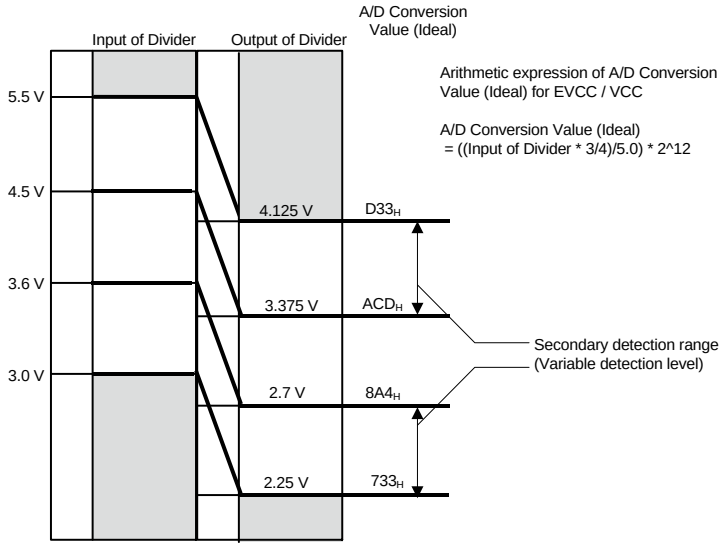
13) Allocate AVSEGVCCCHSCR (for VCC), AVSEGEVCCCHSCR (for EVCC) and AVSEGVDDCHSCR (for VDD) a virtual channel which corresponds to each power source. For details of this setting, refer to **Section** Error! Reference source not found. Error! Reference source not found.. (this procedure was added by product development member)

14) Wait 500ns (*2), start SG, and perform A/D conversion.

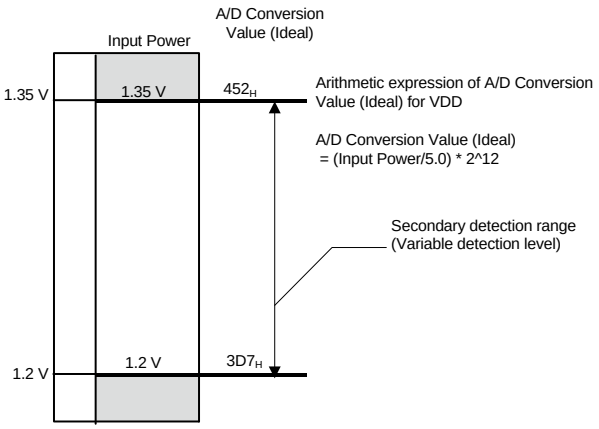
Note 3. This is nonoverlap period for divided resistance switch and pull-down switch. 2 cycles according to Register access clock is guaranteed by the register access. Please delete it if the dummy read is unnecessary in the product evaluation.

Note 4. This is settling time of while divided resistance is disabling or enabling. When the settling time is unnecessary after the product evaluation, please delete it.

EVCC / VCC Condition: A0VCC=A0VREFH=5.0 V



VDD Condition: A0VCC=A0VREFH=5.0 V



Note 3. EVCC can't be guaranteed operation in 3V (3.0 to 3.6V), can be guaranteed operation in 5V (4.5 to 5.5V).

Note 4. Set the upper / lower limit value as the value with which the absolute error of A/D conversion of power supply voltage is added to a reference value of this figure.

Figure 43.42 Reference Value of Upper / Lower Limit Value of Secondary Power Supply Voltage Monitor (this figure is added by product development member)

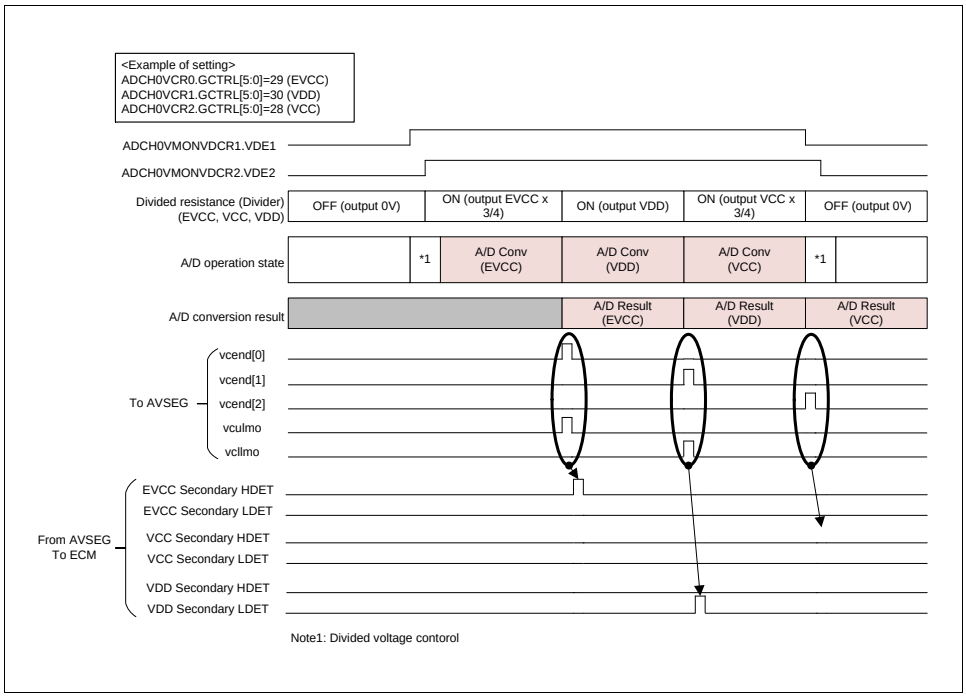


Figure 43.43 Example of Operation of Secondary Power Supply Voltage Monitor

NOTE

- When making it to the module standby, set VDE1 and VDE2 as 0 respectively, before it changes to the module standby.
- Please remove voltage fluctuation of A0VREFH as much as possible. (Please guide the value of the swinging width of A0VREFH, and the set value of the virtual channel upper/lower limit table register after evaluating a product.).

43.5 Definition of A/D Conversion Accuracy

A/D conversion accuracy is defined below.

- Resolution
  Number of digital output codes of the A/D converter
- Quantization error
  An error essentially contained in A/D converters, which is given as 1/2LSB (**Figure 43.44**).
- Offset error
  Deviation of the analog input voltage value from the ideal A/D conversion characteristics when the digital output changes from the minimum voltage value 000_H to 001_H. However, the quantization error is not included (**Figure 43.44**).
- Full-scale error
  Deviation of the analog input voltage value from the ideal A/D conversion characteristics when the digital output changes from FFE_H to FFF_H. However, the quantization error is not included (**Figure 43.44**).
- DNL (Differential nonlinear error)
  Deviation between the ideal digital output code width (Vq) and the actual digital output code width (Va), which is given as (Va - Vq)/Vq. However, the offset error, the full-scale error, and the quantization error are not included (**Figure 43.44**).
- INL (Integral nonlinear error)
  Deviation of the actual value from the ideal A/D conversion characteristics, from the zero voltage to the full-scale voltage, which is given as an integral of DNL from 000_H to a digital output code. However, the offset error, the full-scale error, and the quantization error are not included (**Figure 43.44**).
- TUE (Total unadjusted error)
  Deviation between the digital value and the analog input value. The offset error, the full-scale error, the quantization error, DNL, and INL are included (**Figure 43.44**).

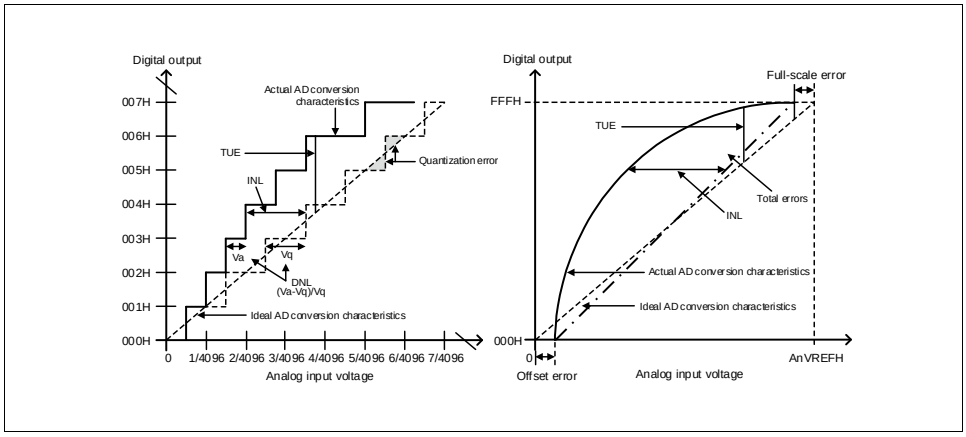


Figure 43.44 Definition of A/D Conversion Accuracy

43.6 Usage Notes

43.6.1 Notes on Using an External Analog Multiplexer

When you use an external multiplexer, observe the following notes so as not to cause system issues.

Other than for the exceptions below, set the MPX wait as follows:

- When an MPX value is transferred to a port: Insert a wait of at least 1 µs.
- When an MPX value is transferred with the SPI interface: Insert a wait of at least the SPI transmission time + 1 µs.

Exception 1) When an external multiplexer is used for one scan group

When an external multiplexer is used for SG0 with SUSMTD[1:0] set to 1_H, or when an external multiplexer is used for any of SG0 to SG3 with SUSMTD[1:0] set to 2_H, set the MPX wait as follows:

- When an MPX value is transferred to a port: Insert a wait of at least 1 µs.
- When an MPX value is transferred with the SPI interface: Insert a wait of at least SPI transmission time × 2.

Exception 2) When an external multiplexer is used for multiple scan groups

When an external multiplexer is used with SUSMTD[1:0] set to 1_H or 2_H, observe the following notes.

- For the starting virtual channel of each scan group, setup so as not to use an external multiplexer. (However, for the start virtual channel of the scan group whose priority is lowest among the scan groups for which the external multiplexer is used, settings to use an external multiplexer does not cause any problem.)
- Up to two scan groups can be transferred with the SPI interface.

Furthermore, set the MPX wait time as follows:

- When an MPX value is transferred to a port: Insert a wait of at least 1 µs.
- When an MPX value is transferred with the SPI interface: Insert a wait of at least SPI transmission time × 2.

43.6.2 Notes on Using Analog Input Pins

Do not perform an A/D conversion for the same analog pin with Delta-Sigma ADC, Cyclic ADC and SAR-ADC at the same time. Also, do not perform an A/D conversion with the SAR-ADC for an analog pin that is being used for a digital input. Doing so may degrade the A/D conversion accuracy.

When a digital input or output signal is multiplexed with an analog input signal, it can also be used as a digital general-purpose input or output pin. Changes in a digital input or output during an AD conversion may reduce the precision of conversion. Noise from the operation of digital pins near analog input pins may also reduce the precision of conversion. Notes on how to reduce the effects of digital input and output noise on the results of AD conversion are given below.

(1) Notes on Analog Input Pins

(a) Place the capacitors of RC circuits as close to the LSI pin as is possible. This reduces the effects of digital inputs and outputs on the precision of conversion. Since the improvement in precision also depends on other conditions of the board, evaluate the situation on the actual board.

(2) Notes on Digital Input and Output Pins near Analog Pins

(a) If digital input through the pin is not essential, disable the digital input.

(b) If a digital signal is input to such a pin, the signal should not include overshoot or undershoot.

(c) Design the board so that load capacitances connected to output pins to suppress discharge currents are small.

(d) Lower the output driving ability of pins that may be affected.

(3) Software Measures against Effects on the Results of Conversion

(a) Use an average of multiple results of AD conversion.

(b) When using multiple consecutive results of ADC conversion, exclude outlying results.

43.6.3 Module Standby Function

The ADCJn has a module standby function.

(For RH850/E2x-FCC1)

Module standby stops the clock supply to ADCJ0, ASF0 and AVSEG by setting MSR_SAD.MS_SAD0.

Module standby stops the clock supply to ADCJ2 by setting MSR_SAD.MS_SAD2.

Module standby stops the clock supply to ADCJ1 by setting MSR_SAD.MS_SAD1.

Module standby stops the clock supply to ADCJ3 by setting MSR_SAD.MS_SAD3.

Module standby stops the clock supply to IFC0. For the clock supply stop condition of IFC0, refer to **Table 43.84**.

Module standby stops the clock supply to IFC1. For the clock supply stop condition of IFC1, refer to **Table 43.85**.

Module standby stops the clock supply to ABFG and AIR. For the clock supply stop condition of ABFG and AIR, refer to **Table 43.89**.

(For RH850/E2M)

Module standby stops the clock supply to ADCJ0, ASF0 and AVSEG by setting MSR_SAD.MS_SAD0.

Module standby stops the clock supply to ADCJ2 by setting MSR_SAD.MS_SAD2.

Module standby stops the clock supply to ADCJ1 by setting MSR_SAD.MS_SAD1.

Module standby stops the clock supply to ADCJ3 by setting MSR_SAD.MS_SAD3.

Module standby stops the clock supply to IFC0. For the clock supply stop condition of IFC0, refer to **Table 43.84**.

Module standby stops the clock supply to IFC1. For the clock supply stop condition of IFC1, refer to **Table 43.86**.

Module standby stops the clock supply to ABFG and AIR. For the clock supply stop condition of ABFG and AIR, refer to **Table 43.90**.

(For RH850/E2GM)

Module standby stops the clock supply to ADCJ0 and ASF0 by setting MSR_SAD.MS_SAD0.

Module standby stops the clock supply to ADCJ2 by setting MSR_SAD.MS_SAD2.

Module standby stops the clock supply to ADCJ1 by setting MSR_SAD.MS_SAD1.

Module standby stops the clock supply to ADCJ3 by setting MSR_SAD.MS_SAD3.

Module standby stops the clock supply to IFC0. For the clock supply stop condition of IFC0, refer to **Table 43.84**.

Module standby stops the clock supply to IFC1. For the clock supply stop condition of IFC1, refer to **Table 43.87**.

Module standby stops the clock supply to ABFG and AIR. For the clock supply stop condition of ABFG and AIR, refer to **Table 43.91**.

(For RH850/E2L)

Module standby stops the clock supply to ADCJ0, ASF0 and AVSEG by setting MSR_SAD.MS_SAD0.

Module standby stops the clock supply to ADCJ2 by setting MSR_SAD.MS_SAD2.

Module standby stops the clock supply to IFC0. For the clock supply stop condition of IFC0, refer to **Table 43.84**.

Module standby stops the clock supply to ABFG and AIR. For the clock supply stop condition of ABFG and AIR, refer to **Table 43.92**.

Module standby stops the clock supply to ADCJ0, ASF0 and AVSEG by setting MSR_SAD.MS_SAD0.

Module standby stops the clock supply to ADCJ2 by setting MSR_SAD.MS_SAD2.

Module standby stops the clock supply to ADCJ1 by setting MSR_SAD.MS_SAD1.

Module standby stops the clock supply to ADCJ3 by setting MSR_SAD.MS_SAD3.

Module standby stops the clock supply to IFC0. For the clock supply stop condition of IFC0, refer to **Table 43.84**.

Module standby stops the clock supply to IFC1. For the clock supply stop condition of IFC1, refer to **Table 43.88**.

Module standby stops the clock supply to ABFG and AIR. For the clock supply stop condition of ABFG and AIR, refer to **Table 43.93**.

Table 43.84 Clock Supply Stop Condition of IFC0 by Module Standby

States	MSR_SAD.MS_SAD0	MSR_SAD.MS_SAD2
Clock Supply Active	0	0 or 1
Clock Supply Active	1	0
Clock Supply Stopped	1	1

Table 43.85 Clock Supply Stop Condition of IFC1 by Module Standby (For RH850/E2x-FCC1)

States	MSR_SAD.MS_SAD1	MSR_SAD.MS_SAD3
Clock Supply Active	0	0 or 1
Clock Supply Active	1	0
Clock Supply Stopped	1	1

Table 43.86 Clock Supply Stop Condition of IFC1 by Module Standby (For RH850/E2M)

States	MSR_SAD.MS_SAD1	MSR_SAD.MS_SAD3
Clock Supply Active	0	0 or 1
Clock Supply Active	1	0
Clock Supply Stopped	1	1

Table 43.87 Clock Supply Stop Condition of IFC1 by Module Standby (For RH850/E2GM)

States	MSR_SAD.MS_SAD1	MSR_SAD.MS_SAD3
Clock Supply Active	0	0 or 1
Clock Supply Active	1	0
Clock Supply Stopped	1	1

Table 43.88 Clock Supply Stop Condition of IFC1 by Module Standby

States	MSR_SAD.MS_SAD1	MSR_SAD.MS_SAD3
Clock Supply Active	0	0 or 1
Clock Supply Active	1	0
Clock Supply Stopped	1	1

Table 43.89 Clock Supply Stop Condition of ABFG and AIR by Module Standby (For RH850/E2x-FCC1)

States	MSR_DAD.MS_DAD00_10	MSR_DAD.MS_DAD20_12	MSR_DAD.MS_DAD13_11	MSR_CAD.MS_CAD	MSR_SAD.MS_SAD0	MSR_SAD.MS_SAD2	MSR_SAD.MS_SAD1	MSR_SAD.MS_SAD3
Clock Supply Active	0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	1	0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	1	1	0	0 or 1	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	1	1	1	0	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	1	1	1	1	0	0 or 1	0 or 1
Clock Supply Active	1	1	1	1	1	1	0	0 or 1
Clock Supply Active	1	1	1	1	1	1	1	0
Clock Supply Stopped	1	1	1	1	1	1	1	1

Table 43.90 Clock Supply Stop Condition of ABFG and AIR by Module Standby (For RH850/E2M)

States	MSR_DAD.MS_DAD00_10	MSR_DAD.MS_DAD20_12	MSR_DAD.MS_DAD13_11	MSR_CAD.MS_CAD	MSR_SAD.MS_SAD0	MSR_SAD.MS_SAD2	MSR_SAD.MS_SAD1	MSR_SAD.MS_SAD3
Clock Supply Active	0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	1	0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	1	1	0	0 or 1	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	1	1	1	0	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	1	1	1	1	0	0 or 1	0 or 1
Clock Supply Active	1	1	1	1	1	1	0	0 or 1
Clock Supply Active	1	1	1	1	1	1	1	0
Clock Supply Stopped	1	1	1	1	1	1	1	1

Table 43.91 Clock Supply Stop Condition of ABFG and AIR by Module Standby (For RH850/E2GM)

States	MSR_DAD.MS_DAD00	MSR_CAD.MS_CAD	MSR_SAD.MS_SAD0	MSR_SAD.MS_SAD2	MSR_SAD.MS_SAD1	MSR_SAD.MS_SAD3
Clock Supply Active	0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	0	0 or 1	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	1	0	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	1	1	0	0 or 1	0 or 1
Clock Supply Active	1	1	1	1	0	0 or 1
Clock Supply Active	1	1	1	1	1	0
Clock Supply Stopped	1	1	1	1	1	1

Table 43.92 Clock Supply Stop Condition of ABFG and AIR by Module Standby (For RH850/E2L)

States	MSR_DAD.MS_DAD00_10	MSR_DAD.MS_DAD20	MSR_CAD.MS_CAD	MSR_SAD.MS_SAD0	MSR_SAD.MS_SAD2
Clock Supply Active	0	0 or 1	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	0	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	1	0	0 or 1	0 or 1
Clock Supply Active	1	1	1	0	0 or 1

Clock Supply Active	1	1	1	1	0
Clock Supply Stopped	1	1	1	1	1

Table 43.93 Clock Supply Stop Condition of ABFG and AIR by Module Standby

States	MSR_DAD.MS_DAD00_10	MSR_DAD.MS_DAD20_12	MSR_DAD.MS_DAD13_11	MSR_DAD.MS_DAD15_14	MSR_DAD.MS_DAD22_21	MSR_CAD.MS_CAD	MSR_SAD.MS_SAD0	MSR_SAD.MS_SAD2	MSR_SAD.MS_SAD1	MSR_SAD.MS_SAD3
Clock Supply Active	0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	1	0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	1	1	0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	1	1	1	0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	1	1	1	1	0	0 or 1	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	1	1	1	1	1	0	0 or 1	0 or 1	0 or 1
Clock Supply Active	1	1	1	1	1	1	1	0	0 or 1	0 or 1
Clock Supply Active	1	1	1	1	1	1	1	1	0	0 or 1
Clock Supply Active	1	1	1	1	1	1	1	1	1	0
Clock Supply Stopped	1	1	1	1	1	1	1	1	1	1

43.7 ADC VMON Secondary Error Generator (AVSEG) (For RH850/U2A-EVA~~E2x-FCC1, E2M, E2L~~)

43.7.1 Overview

43.7.1.1 Function Overview

AVSEG is equivalent to the function which notify an upper error pulse (secondary HDET) and a lower error pulse (Secondary LDET) of each power supply (VCC, E0VCC, ~~and~~ ISOVDD and AWOVDD) to ~~ECM~~ INTC in the secondary power supply voltage monitor (Upper error pulse & Lower error pulse are merged together then routing to INTC).

- Upper Error Pulse Control and Lower Error Pulse Control

This function generates an error signal from ADCJ0 to ~~ECM~~ INTC if an upper or lower bound is exceeded.

- Noise Filter

The upper and lower error pulses are generated by signals passed through a filter to reduce noise.

COUTION

The input of both upper and lower pulses into the same module at the same time is prohibited.

43.7.1.2 Block Diagram

Figure 43.45 illustrates the AVSEG block diagram.

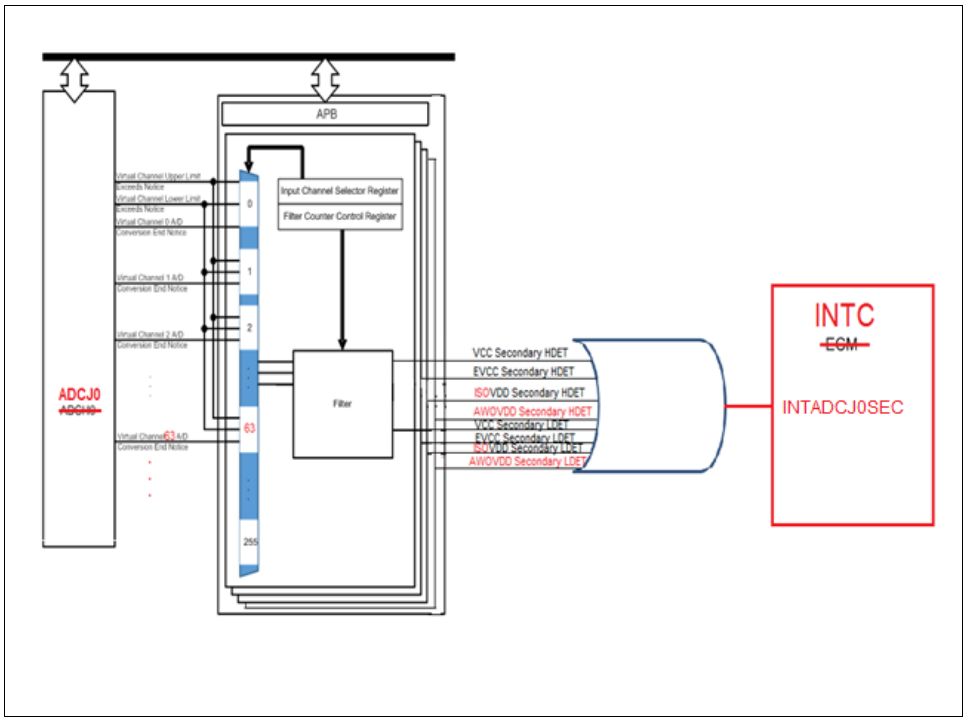


Figure 43.45 AVSEG Block Diagram

43.7.2 Registers

43.7.2.1 List of Registers

Table 43.94 List of Registers

Module Name	Register Name	Symbol	Address	Access	Access Protection
AVSEG	Input Channel Selector Register VCC	AVSEGVCCCHSCR	<AVSEG_base> + 00_H	32	—
AVSEG	Filter Counter Control Register VCC	AVSEGVCCCNTCR	<AVSEG_base> + 04_H	32	—
AVSEG	Input Channel Selector Register EVCC	AVSEGEVCCCHSCR	<AVSEG_base> + 10_H	32	—
AVSEG	Filter Counter Control Register EVCC	AVSEGEVCCCNTCR	<AVSEG_base> + 14_H	32	—
AVSEG	Input Channel Selector Register AWOVDD	AVSEGAWOVDDCHSCR	<AVSEG_base> + 20_H	32	—
AVSEG	Filter Counter Control Register AWOVDD	AVSEGAWOVDDCNTCR	<AVSEG_base> + 24_H	32	—
AVSEG	Input Channel Selector Register ISOVDD	AVSEGISOVDDCHSCR	<AVSEG_base> + 30_H	32	—
AVSEG	Filter Counter Control Register ISOVDD	AVSEGISOVDDCNTCR	<AVSEG_base> + 34_H	32	—
AVSEG	Secondary voltage monitor error register	AVSEGSECVMONERR	<AVSEG_base> + 40_H	32	—
AVSEG	Secondary voltage monitor error clear register	AVSEGSECVMONCLR	<AVSEG_base> + 44_H	32	—

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43.7.2.2 AVSEG Specific Registers

(1) AVSEGVCCCHSCR — Input Channel Selector Register VCC

This register selects the input channel.

Value after reset: 0000 0000H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	AVSEGVCCCHS							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 43.95 AVSEGVCCCHSCR Register Contents

Bit Position	Bit Name	Function
31 to 8	—	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	AVSEGVCCCHS	Input Channel Selector These bits select the channel used for generating error of VCC in the secondary power supply voltage monitor. 00H: Selects ADCJ0 virtual channel 0 : ~~27H~~ 3FH: Selects ADCJ0 virtual channel ~~39~~ 63 ~~28H~~ 40H to FFH: Reserved

(2) AVSEGVCCCNTCR — Filter Counter Control Register VCC

This register controls the filter counter. The noise filtering interval is controlled by using an error counter and a recovery counter. The internal down counter is reset with the written values when this register is modified.

Value after reset: 0000 0101H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	AVSEGVCCENB	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	AVSEGVCCNRMCNT				—	—	—	—	AVSEGVCCERRCNT			
Value after reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Table 43.96 AVSEGVCCCNTCR Register Contents (1/2)

Bit Position	Bit Name	Function
31 to 29	—	Reserved These bits are always read as 0. The write value should always be 0.
28	AVSEGVCCENB	Filter Enable This bit enable AVSEG for VCC 0: DISABLED 1: Enables the filter. When set to DISABLED all AVSEG for VCC functions are disabled.
27 to 12	—	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	AVSEGVCCNRMCNT	Recovery Counter Settings These bits control the number of counts until the signal is considered recovered. Once the signal is considered out of bounds, it will not be recovered until the set number of consecutive non-error pulses are detected. The counter value is reset when one of the following values is written to AVSEGVCCNRMCNT. 1H: Recovery after the signal is within the boundaries for 1 count. : FH: Recovery after the signal is within the boundaries for 15 consecutive counts.
7 to 4	—	Reserved These bits are always read as 0. The write value should always be 0.

Table 43.96 AVSEGVCCCNTCR Register Contents (2/2)

Bit Position	Bit Name	Function
3 to 0	AVSEGVCCERRCNT	Error Counter Control These bits control the number of counts until the signal is considered out of bounds. The signal is considered out of bounds once the set number of consecutive error pulses are detected. The counter value is reset when one of the following values is written to AVSEGVCCERRCNT. 1H: Out of bounds when the signal violates the boundaries for 1 count. : FH: Out of bounds when the signal violates the boundaries for 15 consecutive counts.

CAUTION

Setting AVSEGVCCNRMCNT and AVSEGVCCERRCNT to 0H is prohibited.

If AVSEGVCCNRMCNT is set to 0_H the counter will act as if it was set to 1_H.

The filter will not output any signals if AVSEGVCCERRCNT is set to 0_H.

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(3) AVSEGEVCCCHSCR — Input Channel Selector Register EVCC

This register selects the input channel.

Value after reset: 0000 0000H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	AVSEGEVCCCHS							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 43.97 AVSEGEVCCCHSCR Register Contents

Bit Position	Bit Name	Function
31 to 8	—	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	AVSEGEVCCCHS	Input Channel Selector These bits select the channel used for generating error of EVCC in the secondary power supply voltage monitor 00H: Selects ADCJ0 virtual channel 0 : ~~27H~~ 3FH: Selects ADCJ0 virtual channel ~~39~~ 63 ~~28H~~ 40H to FFH: Reserved

(4) AVSEGEVCCCNTCR — Filter Counter Control Register EVCC

This register controls the filter counter. The noise filtering interval is controlled by using an error counter and a recovery counter. The internal down counter is reset with the written values when this register is modified.

Value after reset: 0000 0101H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	AVSEGEVCCENB	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	AVSEGEVCCNRMCNT				—	—	—	—	AVSEGEVCCERRCNT			
Value after reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Table 43.98 AVSEGEVCCCNTCR Register Contents (1/2)

Bit Position	Bit Name	Function
31 to 29	—	Reserved These bits are always read as 0. The write value should always be 0.
28	AVSEGEVCCENB	Filter Enable This bit enable AVSEG for EVCC 0: DISABLED 1: Enables the filter. When set to DISABLED all AVSEG for EVCC functions are disabled.
27 to 12	—	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	AVSEGEVCCNRMCNT	Recovery Counter Settings These bits control the number of counts until the signal is considered recovered. Once the signal is considered out of bounds, it will not be recovered until the set number of consecutive non-error pulses are detected. The counter value is reset when one of the following values is written to AVSEGEVCCNRMCNT. 1H: Recovery after the signal is within the boundaries for 1 count. : FH: Recovery after the signal is within the boundaries for 15 consecutive counts.
7 to 4	—	Reserved These bits are always read as 0. The write value should always be 0.

Table 43.98 AVSEGEVCCCNTCR Register Contents (2/2)

Bit Position	Bit Name	Function
3 to 0	AVSEGEVCCERRCNT	Error Counter Control These bits control the number of counts until the signal is considered out of bounds. The signal is considered out of bounds once the set number of consecutive error pulses are detected. The counter value is reset when one of the following values is written to AVSEGEVCCERRCNT. 1H: Out of bounds when the signal violates the boundaries for 1 count. : FH: Out of bounds when the signal violates the boundaries for 15 consecutive counts.

CAUTION

Setting AVSEGEVCCNRMCNT and AVSEGEVCCERRCNT to 0H is prohibited.

If AVSEGEVCCNRMCNT is set to 0_H the counter will act as if it was set to 1_H.

The filter will not output any signals if AVSEGEVCCERRCNT is set to 0_H.

(5) AVSEGISOVDDCHSCR — Input Channel Selector Register ISOVDD

This register selects the input channel.

Value after reset: 0000 0000H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	AVSEGISOVDDCHS							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 43.99 AVSEGISOVDDCHSCR Register Contents

Bit Position	Bit Name	Function
31 to 8	—	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	AVSEGISOVDDCHS	Input Channel Selector These bits select the channel used for generating error of ISOVDD in the secondary power supply voltage monitor 00H: Selects ADCJ0 virtual channel 0 : ~~27H~~ 3FH: Selects ADCJ0 virtual channel ~~39~~ 63 ~~28H~~ 40H to FFH: Reserved

(6) AVSEGISOVDDCNTCR — Filter Counter Control Register ISOVDD

This register controls the filter counter. The noise filtering interval is controlled by using an error counter and a recovery counter. The internal down counter is reset with the written values when this register is modified.

Value after reset: 0000 0101H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	AVSEGISOVDDENB	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	AVSEGISOVDDNRMCNT				—	—	—	—	AVSEGISOVDDERRCNT			
Value after reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Table 43.100 AVSEGISOVDDCNTCR Register Contents

Bit Position	Bit Name	Function
31 to 29	—	Reserved These bits are always read as 0. The write value should always be 0.
28	AVSEGISOVDDENB	Filter Enable This bit enable AVSEG for ISOVDD 0: DISABLED 1: Enables the filter. When set to DISABLED all AVSEG for ISOVDD functions are disabled.
27 to 12	—	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	AVSEGISOVDDNRMCNT	Recovery Counter Settings These bits control the number of counts until the signal is considered recovered. Once the signal is considered out of bounds, it will not be recovered until the set number of consecutive non-error pulses are detected. The counter value is reset when one of the following values is written to AVSEGISOVDDNRMCNT. 1H: Recovery after the signal is within the boundaries for 1 count. : FH: Recovery after the signal is within the boundaries for 15 consecutive counts.
7 to 4	—	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	AVSEGISOVDDERRCNT	Error Counter Control These bits control the number of counts until the signal is considered out of bounds. The signal is considered out of bounds once the set number of consecutive error pulses are detected. The counter value is reset when one of the following values is written to AVSEGISOVDDERRCNT. 1H: Out of bounds when the signal violates the boundaries for 1 count. : FH: Out of bounds when the signal violates the boundaries for 15 consecutive counts.

CAUTION

Setting AVSEGISOVDDNRMCNT and AVSEGISOVDDERRCNT to 0H is prohibited.

If AVSEGISOVDDNRMCNT is set to 0_H the counter will act as if it was set to 1_H.

The filter will not output any signals if AVSEGISOVDDERRCNT is set to 0_H.

(7) AVSEGAWOVDDCHSCR — Input Channel Selector Register AWOVDD

This register selects the input channel.

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	AVSEGAWOVDDCHS							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 43.101 AVSEGAWOVDDCHSCR Register Contents

Bit Position	Bit Name	Function
31 to 8	—	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	AVSEGAWOVDDCHS	Input Channel Selector These bits select the channel used for generating error of AWOVDD in the secondary power supply voltage monitor 00H: Selects ADCJ0 virtual channel 0 : 3FH: Selects ADCJ0 virtual channel 63 40H to FFH: Reserved

(8) AVSEGAWOVDDCNTCR — Filter Counter Control Register AWOVDD

This register controls the filter counter. The noise filtering interval is controlled by using an error counter and a recovery counter. The internal down counter is reset with the written values when this register is modified.

Value after reset: $0000\ 0101_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	AVSEGAWOVDDENB	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	AVSEGAWOVDDNRMCNT				—	—	—	—	AVSEGAWOVDDERRCNT			
Value after reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Table 43.102 AVSEGAWOVDDCNTCR Register Contents

Bit Position	Bit Name	Function
31 to 29	—	Reserved These bits are always read as 0. The write value should always be 0.
28	AVSEGAWOVDDENB	Filter Enable This bit enable AVSEG for AWOVDD 0: DISABLED 1: Enables the filter. When set to DISABLED all AVSEG for AWOVDD functions are disabled.
27 to 12	—	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	AVSEGAWOVDDNRMCNT	Recovery Counter Settings These bits control the number of counts until the signal is considered recovered. Once the signal is considered out of bounds, it will not be recovered until the set number of consecutive non-error pulses are detected. The counter value is reset when one of the following values is written to AVSEGAWOVDDNRMCNT. 1H: Recovery after the signal is within the boundaries for 1 count. : FH: Recovery after the signal is within the boundaries for 15 consecutive counts.
7 to 4	—	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	AVSEGAWOVDDERRCNT	Error Counter Control These bits control the number of counts until the signal is considered out of bounds. The signal is considered out of bounds once the set number of consecutive error pulses are detected. The counter value is reset when one of the following values is written to AVSEGAWOVDDERRCNT. 1H: Out of bounds when the signal violates the boundaries for 1 count. : FH: Out of bounds when the signal violates the boundaries for 15 consecutive counts.

CAUTION

Setting AVSEGAWOVDDNRMCNT and AVSEGAWOVDDERRCNT to 0H is prohibited.

If AVSEGAWOVDDNRMCNT is set to 0_H the counter will act as if it was set to 1_H.

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The filter will not output any signals if AVSEGAWOVDDERRCNT is set to 0_H.

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(9) AVSEGSECVMONERR – Secondary voltage monitor error register

AVSEGSECVMONERR is an 32-bit read-only register that indicates Secondary voltage monitor error of VCC, E0VCC, ISOVDD and AWOVDD. AVSEGSECVMONERR is initialized to 0000_0000_H at reset.

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	AWOVDD_ULME	ISOVDD_ULME	EVCC_ULME	VCC_ULME
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	AWOVDD_LLME	ISOVDD_LLME	EVCC_LLME	VCC_LLME
Value after Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 43.103 AVSEGSECVMONERR Register Contents

Bit Position	Bit Name	Function
31 to 20	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
19	AWOVDD_ULME	Upper limit voltage error AWOVDD 0: No error present 1: An error is present Setting condition Upper limit voltage error of AWOVDD is detected Clearing condition A value of 1 is written to AWOVDD_ULMEC in AVSEGSECVMONCLR
18	ISOVDD_ULME	Upper limit voltage error ISOVDD 0: No error present 1: An error is present Setting condition Upper limit voltage error of ISOVDD is detected Clearing condition A value of 1 is written to ISOVDD_ULMEC in AVSEGSECVMONCLR
17	EVCC_ULME	Upper limit voltage error E0VCC 0: No error present 1: An error is present Setting condition Upper limit voltage error of E0VCC is detected Clearing condition A value of 1 is written to EVCC_ULMEC in AVSEGSECVMONCLR
16	VCC_ULME	Upper limit voltage error VCC 0: No error present 1: An error is present.

		Setting condition Upper limit voltage error of VCC is detected. Clearing condition A value of 1 is written to VCC_ULMEC in AVSEGSECVMONCLR
15 to 4	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
3	AWOVDD_LLME	Lower limit voltage error AWOVDD 0: No error present 1: An error is present. Setting condition Lower limit voltage error of AWOVDD is detected. Clearing condition A value of 1 is written to AWOVDD_LLMEC in AVSEGSECVMONCLR
2	ISOVDD_LLME	Lower limit voltage error ISOVDD 0: No error present 1: An error is present. Setting condition Lower limit voltage error of ISOVDD is detected. Clearing condition A value of 1 is written to ISOVDD_LLMEC in AVSEGSECVMONCLR
1	EVCC_LLME	Lower limit voltage error E0VCC 0: No error present 1: An error is present. Setting condition Lower limit voltage error of E0VCC is detected. Clearing condition A value of 1 is written to EVCC_LLMEC in AVSEGSECVMONCLR
0	VCC_LLME	Lower limit voltage error VCC 0: No error present 1: An error is present. Setting condition Lower limit voltage error of VCC is detected. Clearing condition A value of 1 is written to VCC_LLMEC in AVSEGSECVMONCLR

(10) AVSEGSECVMONCLR – Secondary voltage monitor error clear register

AVSEGSECVMONCLR is an 32-bit write-only register that control error clearing in AVSEGSECVMONERR register. AVSEGSECVMONCLR is always read as 0.

Value after reset: 0000 0000H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	AWOVDD_ULMEC	ISOVDD_ULMEC	EVCC_ULMEC	VCC_ULMEC
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	W	W	W	W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	AWOVDD_LLMEC	ISOVDD_LLMEC	EVCC_LLMEC	VCC_LLMEC
Value after Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	W	W	W	W

Table 43.104 AVSEGSECVMONCLR Register Contents

Bit Position	Bit Name	Function
31 to 20	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
19	AWOVDD_ULMEC	Upper limit voltage error AWOVDD clear Writing 0: Not clear Writing 1: Clear
18	ISOVDD_ULMEC	Upper limit voltage error ISOVDD clear Writing 0: Not clear Writing 1: Clear
17	EVCC_ULMEC	Upper limit voltage error E0VCC clear Writing 0: Not clear Writing 1: Clear
16	VCC_ULMEC	Upper limit voltage error VCC clear Writing 0: Not clear Writing 1: Clear
15 to 4	—	Reserved When read, the value after reset is returned. When writing, write the value after reset.
3	AWOVDD_LLMEC	Lower limit voltage error AWOVDD clear Writing 0: Not clear Writing 1: Clear
2	ISOVDD_LLMEC	Lower limit voltage error ISOVDD clear Writing 0: Not clear Writing 1: Clear
1	EVCC_LLMEC	Lower limit voltage error E0VCC clear Writing 0: Not clear Writing 1: Clear
0	VCC_LLMEC	Lower limit voltage error VCC clear Writing 0: Not clear Writing 1: Clear

43.7.3 Operation

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43.7.3.1 Noise Count Method

The AVSEG noise count methods are shown below. Noise is filtered and reduced by counting the number of times the ADC boundary values are exceeded using the input error pulses.

COUTION

The input of both upper and lower pulses into the same module at the same time is prohibited.

Example for the upper error pulse AVSEG for VCC:

Method 1:

AVSEGVCCCNTCR.AVSEGVCCERMCNT = 1_H to 3_H and AVSEGVCCCNTCR.AVSEGVCCNRMCNT = 1_H.

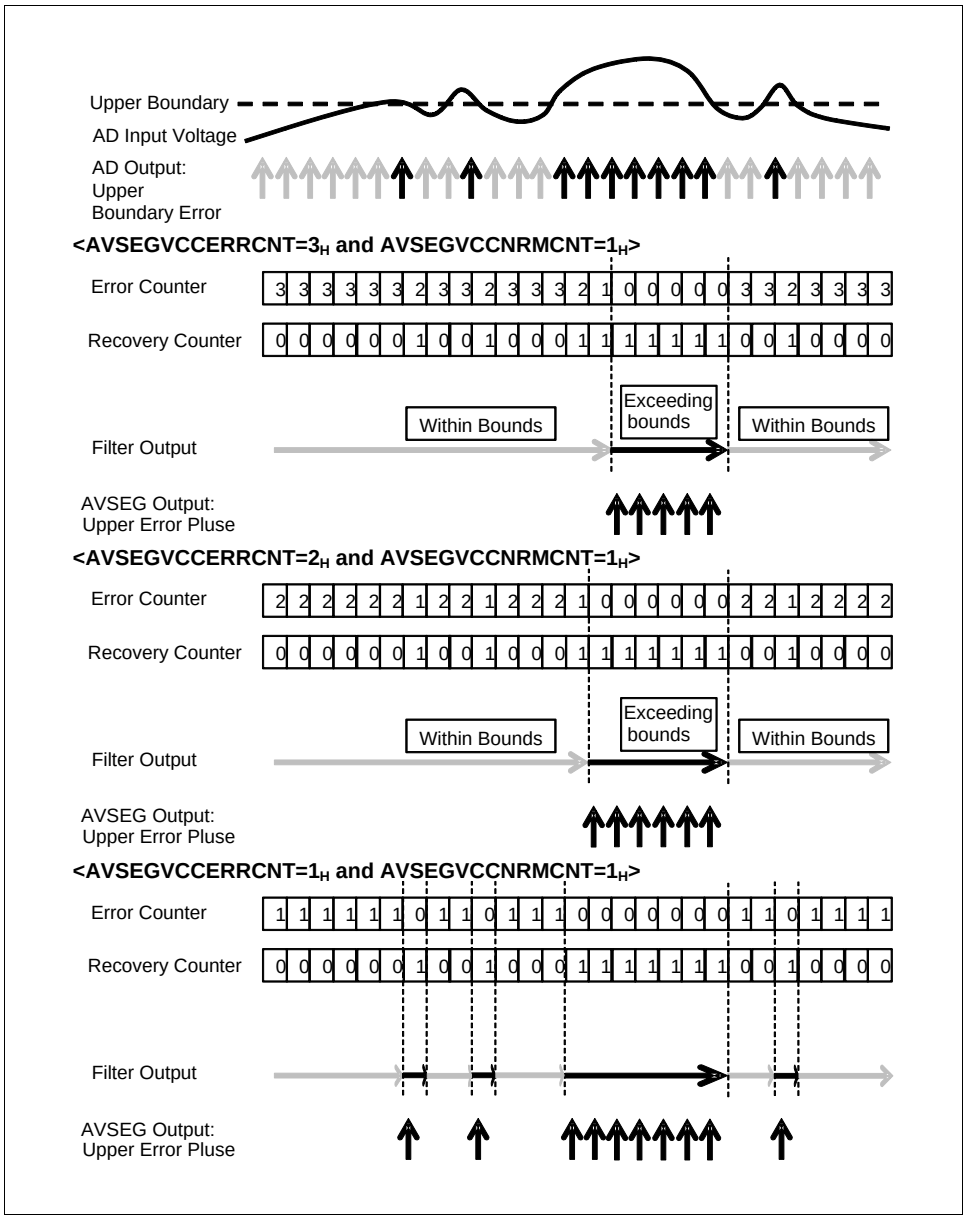

Figure 43.46 Noise Count (1)

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Method 2:

AVSEGVCCCNTCR.AVSEGVCCERMCNT = 1_H to 3_H and AVSEGVCCCNTCR.AVSEGVCCNRMCNT = 2_H.

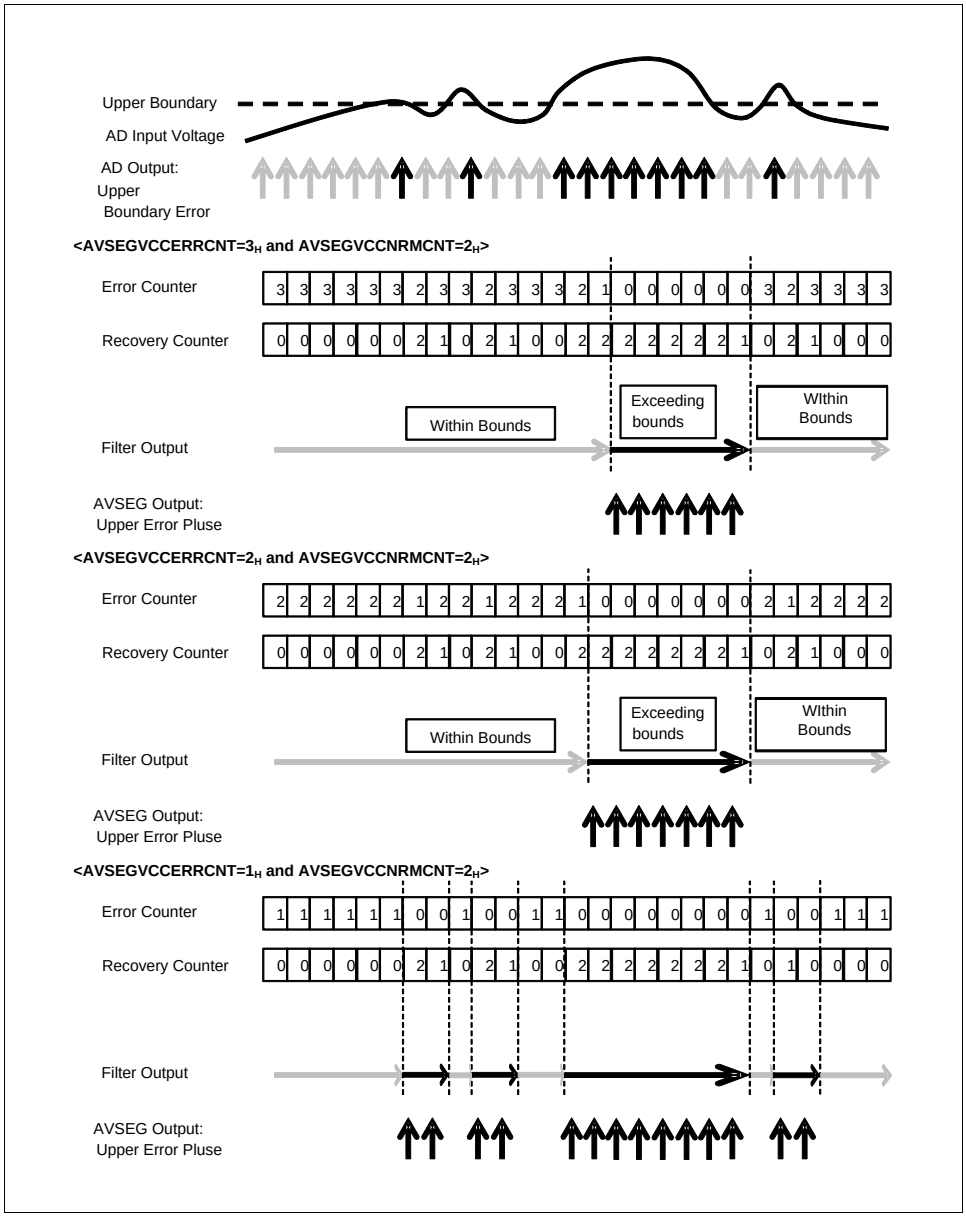

Figure 43.47 Noise Count (2)

Method 3:

AVSEGVCCCNTCR.AVSEGVCCERRCNT = 1_H to 3_H and AVSEGVCCCNTCR.AVSEGVCCNRMCNT = 3_H.

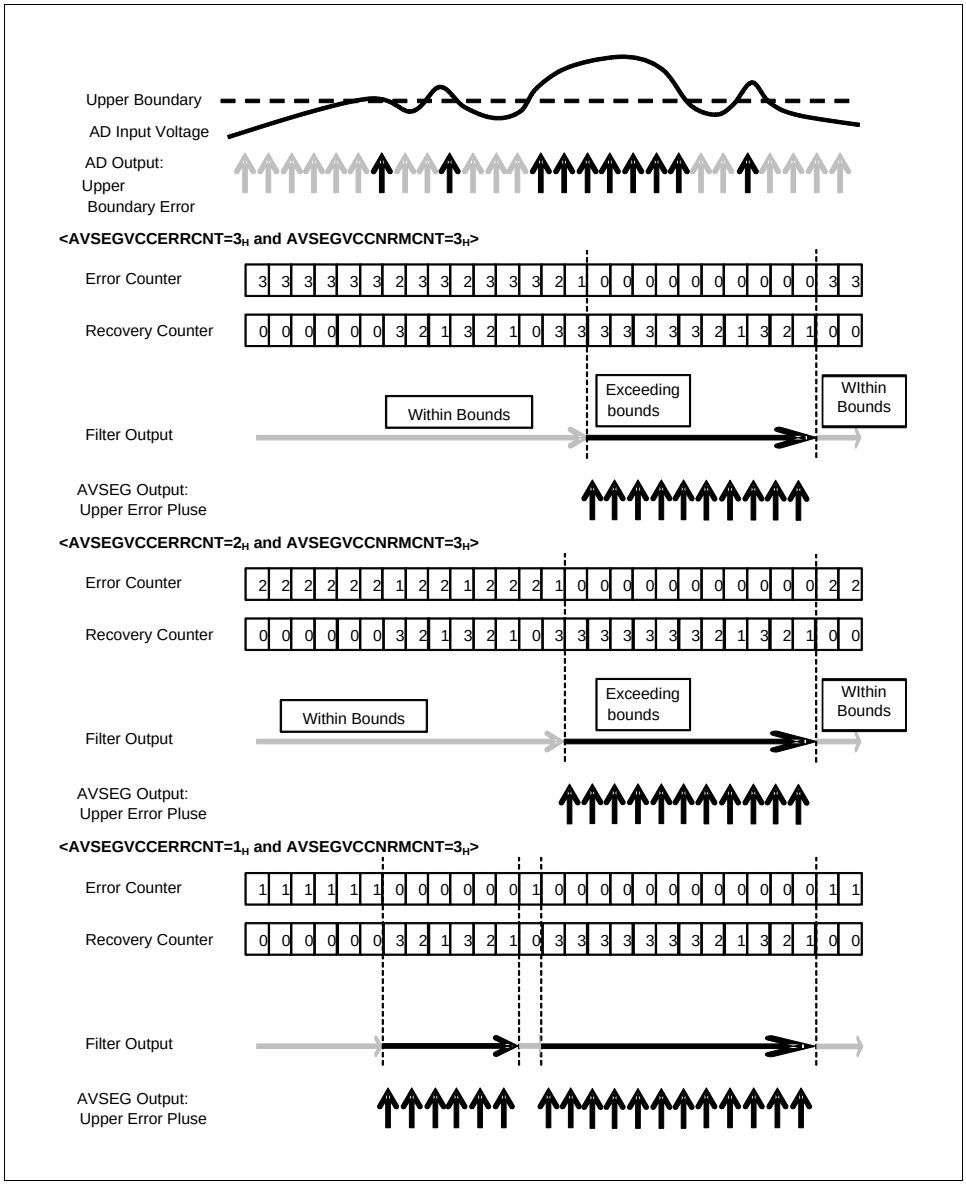

Figure 43.48 Noise Count (3)

43.7.3.2 Upper/Lower Error Pulse Output

The AVSEG upper/lower error pulse output signals are shown below. All output signals are generated by signals that have passed through the filter function to reduce noise.

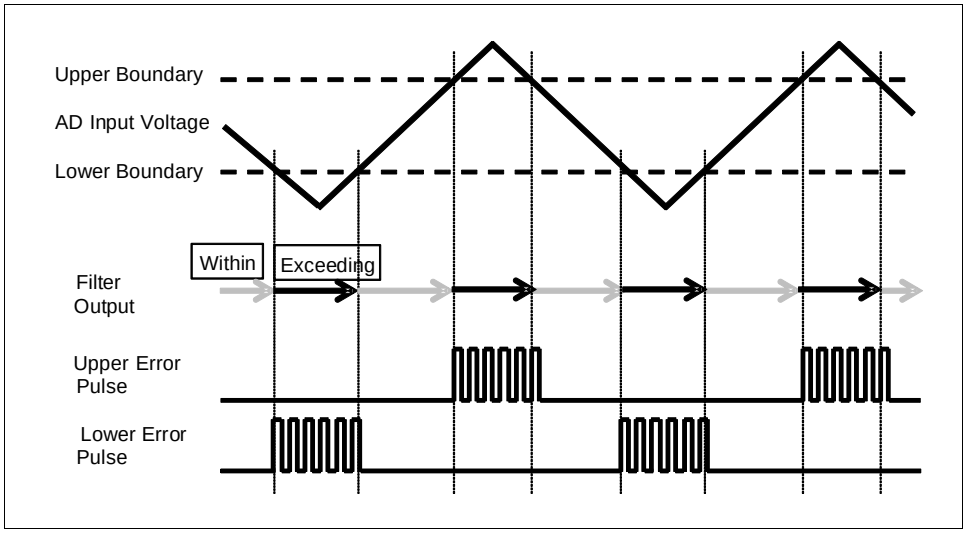

Figure 43.49 Upper/Lower Error Pulse Output

43.7.4 Use Method

(1) Startup Procedure Example

(a) ADC Settings (For details, refer to **Section ~~34~~ 43, Analog to Digital Converter (ADCJ)**

Set the virtual channel registers and virtual channel upper/lower limit table registers so that comparisons are made between the limit registers and the input voltage during conversion.

~~(b) ECM Settings~~

~~Refer to **Section 39, Error Control Module (ECM)**.~~

(b) Interrupt setting

Refer to section Interrupt controller (INTC).

(c) Clear error status in AVSEGSECVMONERR by writing to AVSEGSECVMONCLR register.

~~(c)~~(d) AVSEG Settings

Set the Input Channel Selector Register of respective voltage (AVSEGVCCCHSCR, AVSEGEVCCCHSCR, ~~and~~ AVSEGISOVDDCHSCR and AVSEGAWOVDDCHSCR).

Set the Filter Counter Control Register of respective voltage (AVSEGVCCCNTCR, AVSEGEVCCCNTCR, ~~and~~ AVSEGISOVDDCNTCR and AVSEGAWOVDDCNTCR).

~~(d)~~(e) Begin AD Conversion

Begin AD conversion after setting up AVSEG. If the AVSEG Filter Counter Control Register is modified, the error counter and recovery counter will be set with the written values, and all outputs change will be masked.

(2) Stop Procedure Example

(a) End A/D Conversion

Stop the ADCJ0.

(b) AVSEG Setting

Set the filter counter enable bit, AVSEGVCCCNTCR. AVSEGVCCENB, AVSEGEVCCCNTCR. AVSEGEVCCENB, ~~and~~ AVSEGISOVDDCNTCR. AVSEGISOVDDENB and AVSEGAWOVDDCNTCR. AVSEGAWOVDDENB to 0.

This will prevent any and all pulse signals from being output from AVSEG.

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NOTE

The internal filter counters will be reset to the written values during the AVSEGVCCCNTCR, AVSEGEVCCCNTCR, ~~and~~ AVSEGISOVDDCNTCR and AVSEGAWOVDDCNTCR write procedure.

(3) Usage Notes

(a) The input of both upper and lower error pulses into the same module at the same time is prohibited.

(b) Setting AVSEGVCCNRMCNT, AVSEGVCCERRCNT, AVSEGEVCCNRMCNT, AVSEGEVCCERRCNT, AVSEGISOVDDNRMCNT, ~~and~~ AVSEGISOVDDERRCNT, AVSEGAWOVDDNRMCNT and AVSEGAWOVDDERRCNT to 0H is prohibited.

43.8 Product Design Point

43.8.1 Correspondence of Synchronous Start

Refer to **Section 43.3.2.1, ADCJ0ADSYNSTCR — A/D Synchronization Start Control Register, Section 43.3.2.2, ADCJ0ADTSYNSTCR — A/D Timer Synchronization Start Control Register**.

43.8.2 Correspondence of ADMPX

For allocation of ADMPX, refer to **Section 43.1.6, External Input/Output Signals**.

For details of ADMPX, refer to **Section 43.4.4.4, Normal A/D Conversion with the MPX and Normal A/D Conversion with the MPX in Addition Mode.**

Way of setting of ADMPX is shown to the following.

Table 43.105 Way of Setting of ADMPX

	ADMPX	Signal for setting of ADMPX		
Instance	Allocation	Pin name	Setting value	Note
adcsm_0	AN131	ex_mpx_pch[2:0]	(3'b011)	Number of physical channel group
		ex_mpx_psubch[1:0]	(2'b01)	Number of physical sub channel
adcsm_2	AN243	ex_mpx_pch[2:0]	(3'b100)	Number of physical channel group
		ex_mpx_psubch[1:0]	(2'b11)	Number of physical sub channel
adcsm_1	AN100	ex_mpx_pch[2:0]	(3'b000)	Number of physical channel group
		ex_mpx_psubch[1:0]	(2'b00)	Number of physical sub channel
adcsm_3	AN300	ex_mpx_pch[2:0]	(3'b000)	Number of physical channel group
		ex_mpx_psubch[1:0]	(2'b00)	Number of physical sub channel

43.8.3 Correspondence of RRAMP

For allocation of RRAMP, refer to **Section 43.1.6, External Input/Output Signals**.

43.8.4 Correspondence of Option Byte

Allocation of option byte is shown to the following.

Table 43.106 Allocation of Option Byte

Instance	Option byte signal		Note
	Pin name	Connection net name	
adcsm_0	adctrm[1:0]	MEM_TOP.greg1084[25:24]	For adc_0.
	adctrm[3:2]	MEM_TOP.greg1084[17:16]	For adcam_00 to adcamp_02.
	adctrm[5:4]	(2'b00)	For T&H (HM), so it isn't used.
adcsm_2	adctrm[1:0]	MEM_TOP.greg1084[25:24]	For adc_2.
	adctrm[3:2]	MEM_TOP.greg1084[17:16]	For adcam_20 to adcamp_22.
	adctrm[5:4]	(2'b00)	For T&H (HM), so it isn't used.
adcsm_1	adctrm[1:0]	MEM_TOP.greg1084[25:24]	For adc_1.
	adctrm[3:2]	MEM_TOP.greg1084[17:16]	For adcam_10 to adcamp_11.
	adctrm[5:4]	(2'b00)	For T&H (HM), so it isn't used.
adcsm_3	adctrm[1:0]	MEM_TOP.greg1084[25:24]	For adc_3.
	adctrm[3:2]	MEM_TOP.greg1084[17:16]	For adcam_30 to adcamp_31.
	adctrm[5:4]	(2'b00)	For T&H (HM), so it isn't used.

43.8.5 Correspondence of Test Mode

Connect adcsm_n.test_mode to SYS_TOP.lvs_testmode_a[*1].

When test_mode is set to 1, it is possible to read, writing of test register (ADCJnTRMCR, ADCJnADTSTRA, ADCJnADTSTRB, ADCJnADTSTRC, ADCJnADTSTRD).

Connect adcsm_n.iddq_mode to SYS_TOP.IDDQMD.

When iddq_mode is set to 1, hard macros are shifted into the state of DC electric current off by soft macro (adcsm_n).

Note 1. This is instructions of SYS_TOP person in charge.

43.8.6 Correspondence of Scan Test

Instance of target of scan test is shown to the following.

Connect scan mode signal to DMS_TDR_SCAN_MODE of TEST_TOP.

Connect scan_enable signal to scan_enable of TEST_TOP.

Table 43.107 Target of Scan Test (1/2)

Instance	Target of scan test	Signal for scan test		Note
		Pin name	Connection net name	
adcsm_0	√	scan_mode	DMS_TDR_SCAN_MODE	
		scan_enable	scan_enable	
adcsm_2	√	scan_mode	DMS_TDR_SCAN_MODE	
		scan_enable	scan_enable	
adcsm_1	√	scan_mode	DMS_TDR_SCAN_MODE	
		scan_enable	scan_enable	
adcsm_3	√	scan_mode	DMS_TDR_SCAN_MODE	
		scan_enable	scan_enable	
ifc_0	√	scan_enable	scan_enable	
ifc_1	√	scan_enable	scan_enable	
asf	√	scan_enable	scan_enable	
adc50g	—	—	—	
adc52g	—	—	—	
adc51g	—	—	—	
adc53g	—	—	—	
avseg	√	scan_enable	scan_enable	
abfg	√	scan_enable	scan_enable	
air	√	scan_enable	scan_enable	
adc_gl2	—	—	—	
pd_avcc_0.adc50	—	—	—	
pd_avcc_2.adc52	—	—	—	
pd_avcc_1.adc51	—	—	—	
pd_avcc_3.adc53	—	—	—	
pd_avcc_0.adc_gl	—	—	—	
pd_avcc_2.adc_gl	—	—	—	
pd_avcc_1.adc_gl	—	—	—	
pd_avcc_3.adc_gl	—	—	—	

Table 43.107 Target of Scan Test (2/2)

Instance	Target of scan test	Signal for scan test		Note
		Pin name	Connection net name	
pd_avcc_0.adc_0	√	ADSCAN_MODE	DMS_TDR_SCAN_MODE	
		ADSCAN_ENABLE	(1'b0)	It's connected in a DFT process.
		ADSCAN_IN[2:0]	(3'b000)	It's connected in a DFT process.
		ADSCAN_OUT[2:0]	(FLT)	It's connected in a DFT process.
pd_avcc_2.adc_2	√	ADSCAN_MODE	DMS_TDR_SCAN_MODE	
		ADSCAN_ENABLE	(1'b0)	It's connected in a DFT process.
		ADSCAN_IN[2:0]	(3'b000)	It's connected in a DFT process.
		ADSCAN_OUT[2:0]	(FLT)	It's connected in a DFT process.
pd_avcc_1.adc_1	√	ADSCAN_MODE	DMS_TDR_SCAN_MODE	
		ADSCAN_ENABLE	(1'b0)	It's connected in a DFT process.
		ADSCAN_IN[2:0]	(3'b000)	It's connected in a DFT process.
		ADSCAN_OUT[2:0]	(FLT)	It's connected in a DFT process.
pd_avcc_3.adc_3	√	ADSCAN_MODE	DMS_TDR_SCAN_MODE	
		ADSCAN_ENABLE	(1'b0)	It's connected in a DFT process.
		ADSCAN_IN[2:0]	(3'b000)	It's connected in a DFT process.
		ADSCAN_OUT[2:0]	(FLT)	It's connected in a DFT process.
pd_avcc_0.adcamp_00	—	—	—	
pd_avcc_0.adcamp_01	—	—	—	
pd_avcc_0.adcamp_02	—	—	—	
pd_avcc_2.adcamp_20	—	—	—	
pd_avcc_2.adcamp_21	—	—	—	
pd_avcc_2.adcamp_22	—	—	—	
pd_avcc_2.adcamp_23	—	—	—	E2xFCC2/E2UH/E2H only
pd_avcc_1.adcamp_10	—	—	—	
pd_avcc_1.adcamp_11	—	—	—	
pd_avcc_3.adcamp_30	—	—	—	
pd_avcc_3.adcamp_31	—	—	—	
pd_avcc_3.adcamp_32	—	—	—	E2xFCC2/E2UH/E2H only
pd_avcc_3.adcamp_33	—	—	—	E2xFCC2/E2UH/E2H only
pd_avcc_0.adc50	—	—	—	
pd_avcc_2.adc52	—	—	—	
pd_avcc_1.adc51	—	—	—	
pd_avcc_3.adc53	—	—	—	
pd_avcc_0.adc_gl	—	—	—	
pd_avcc_2.adc_gl	—	—	—	
pd_avcc_1.adc_gl	—	—	—	
pd_avcc_3.adc_gl	—	—	—	
pd_avcc_0.vmon_vcc	—	—	—	
pd_avcc_0.vmon_e0vcc	—	—	—	
pd_avcc_0.vmon_vdd	—	—	—	