Lecture 3
Implementation Technology

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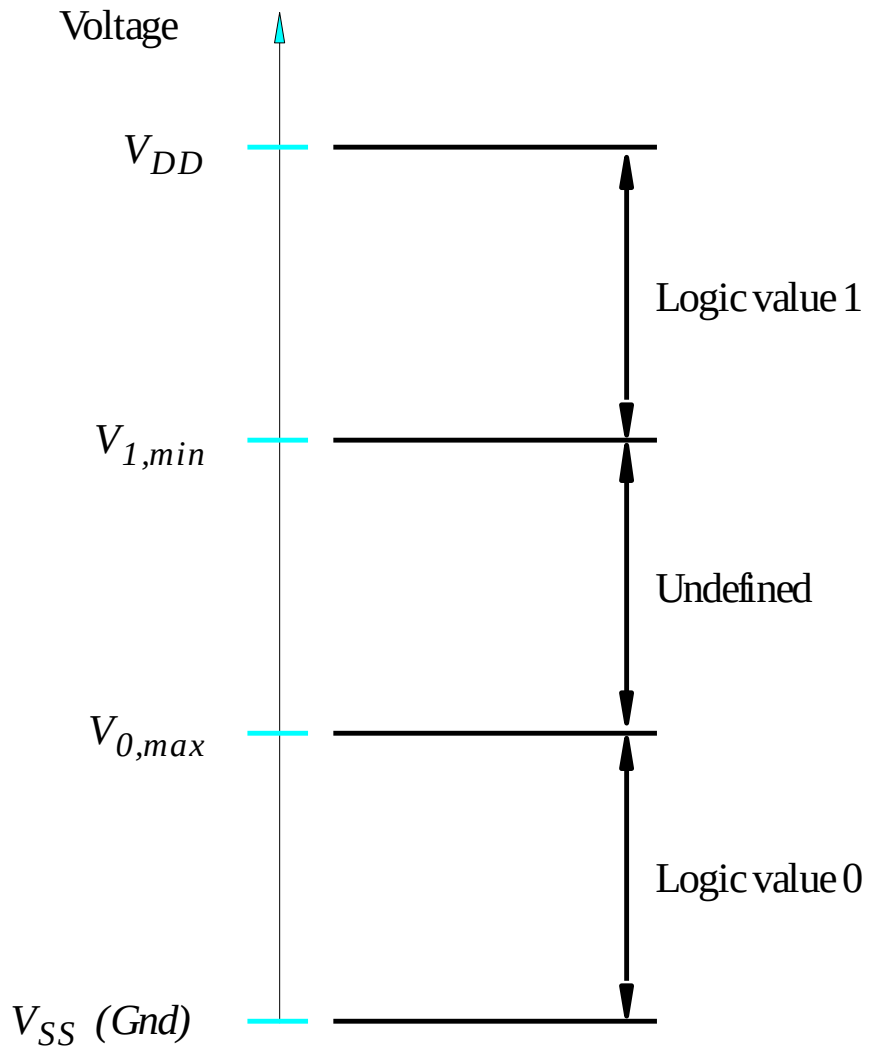
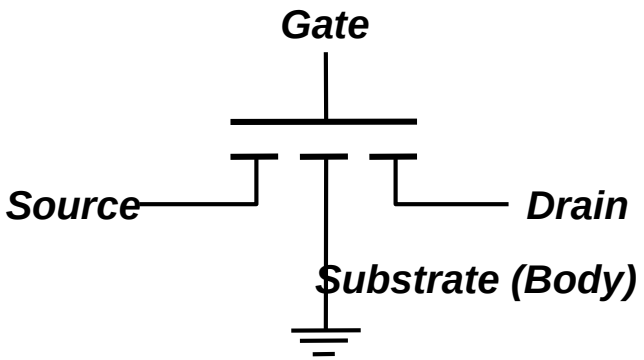
Representation of logic values by voltage levels

- Positive logic : 0 and 1 referred to low and high.
- Negative logic : 1 and 0 referred to low and high.
- V_{dd} = 5V conventionally, 3.3V->2.5V->1.8V->1.3V->~1V evolutionally.

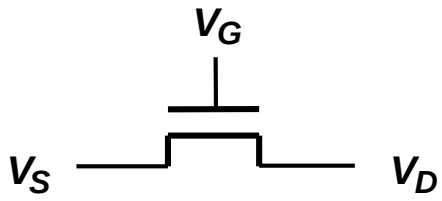


NMOS and PMOS Transistors as Switches

(a) A simple switch controlled by the input x

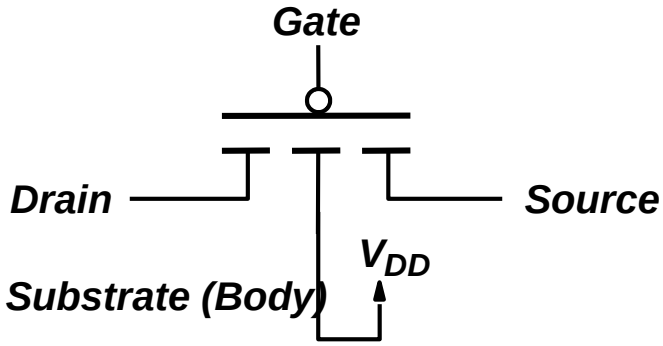


(b) NMOS transistor

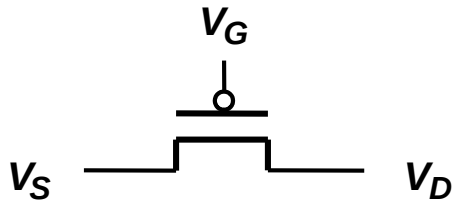


(c) Simplified symbol for an NMOS transistor

(a) A switch with the opposite behavior to left



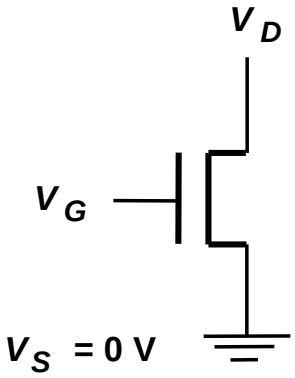
(b) PMOS transistor

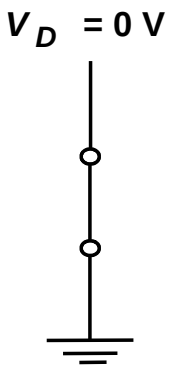


(c) Simplified symbol for a PMOS transistor

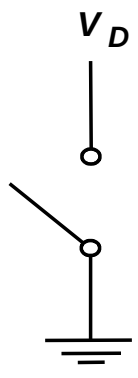
NMOS and PMOS Transistors in Logic Circuits

- NMOS



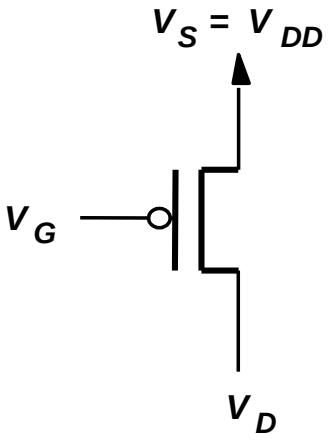


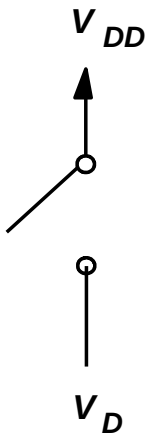
Closed switch
when $V_G = V_{DD}$



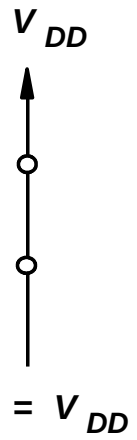
Open switch
when $V_G = 0$ V

- PMOS





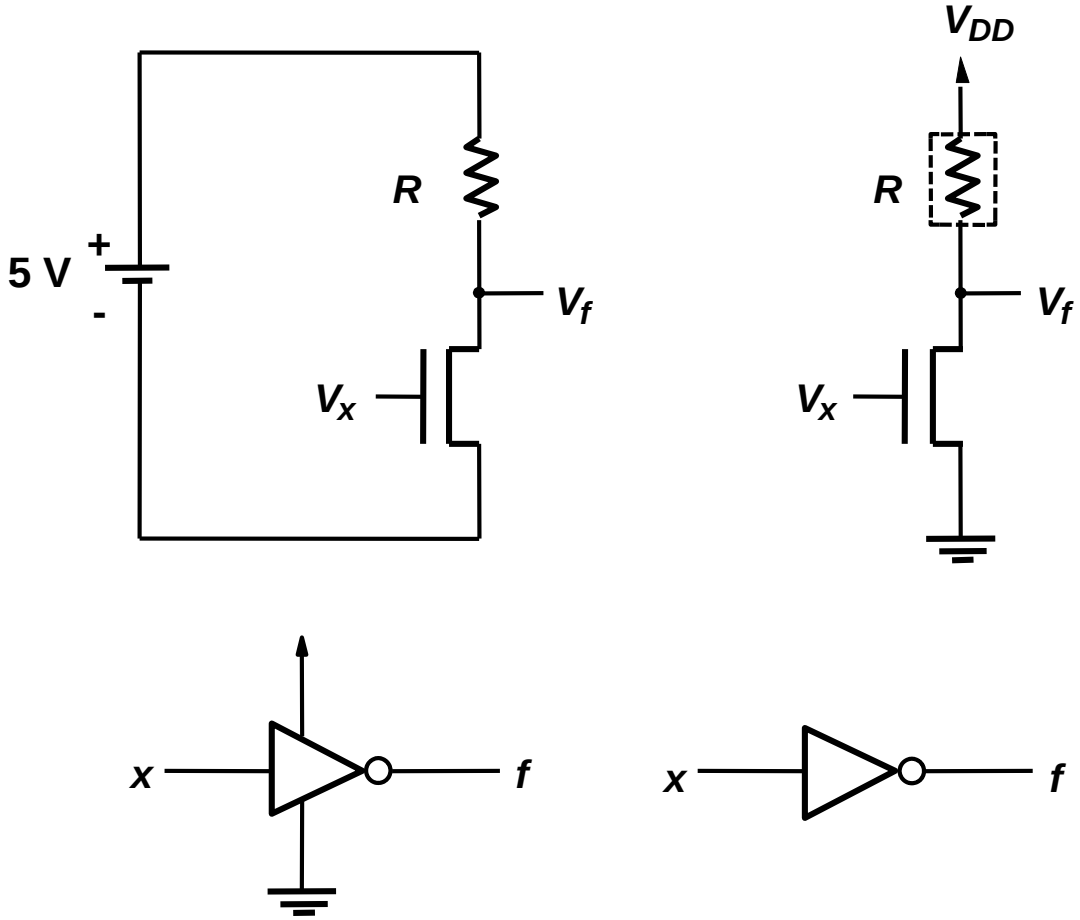
Open switch
when $V_G = V_{DD}$



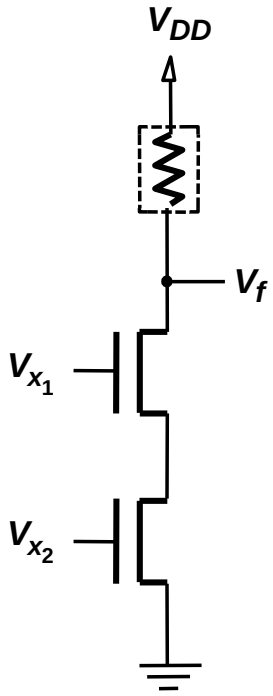
Closed switch
when $V_G = 0$ V

A NOT Gate Built with NMOS Tehcnology

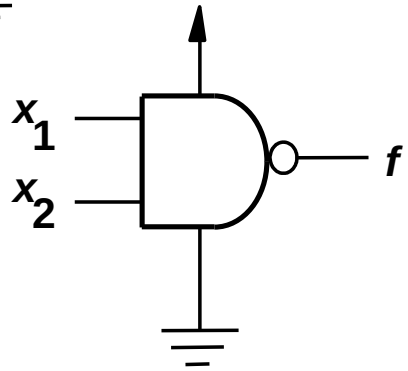
- Power consumption: V_{DD}^2/R when $V_x = V_{DD}$

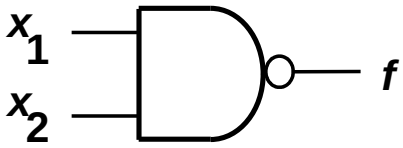


NMOS Realization of a NAND gate

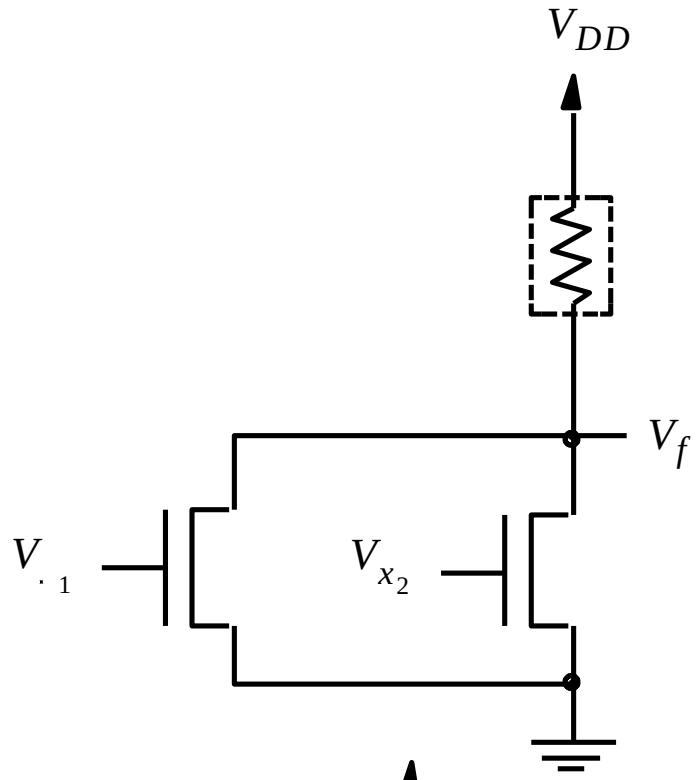


x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0

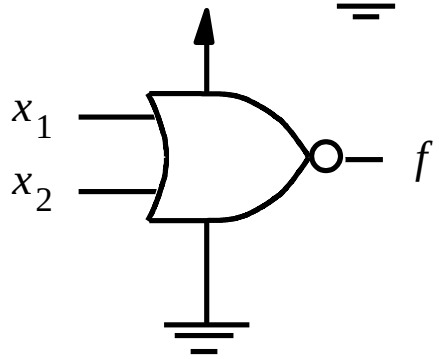


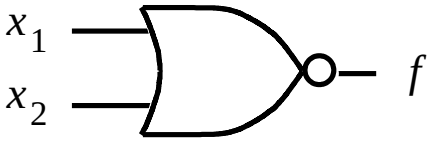


NMOS Realization of a NOR Gate

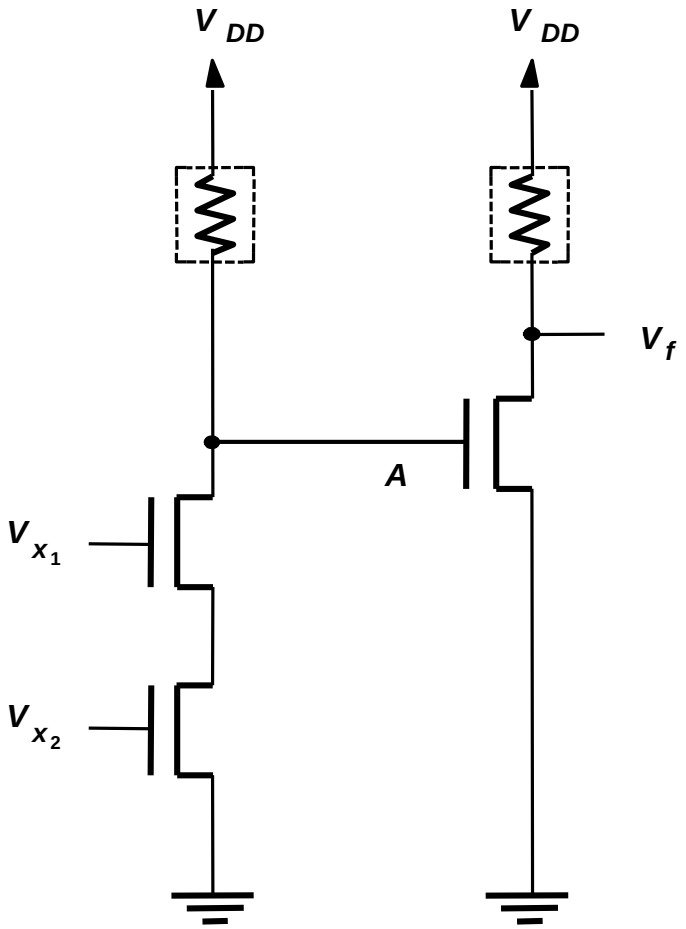


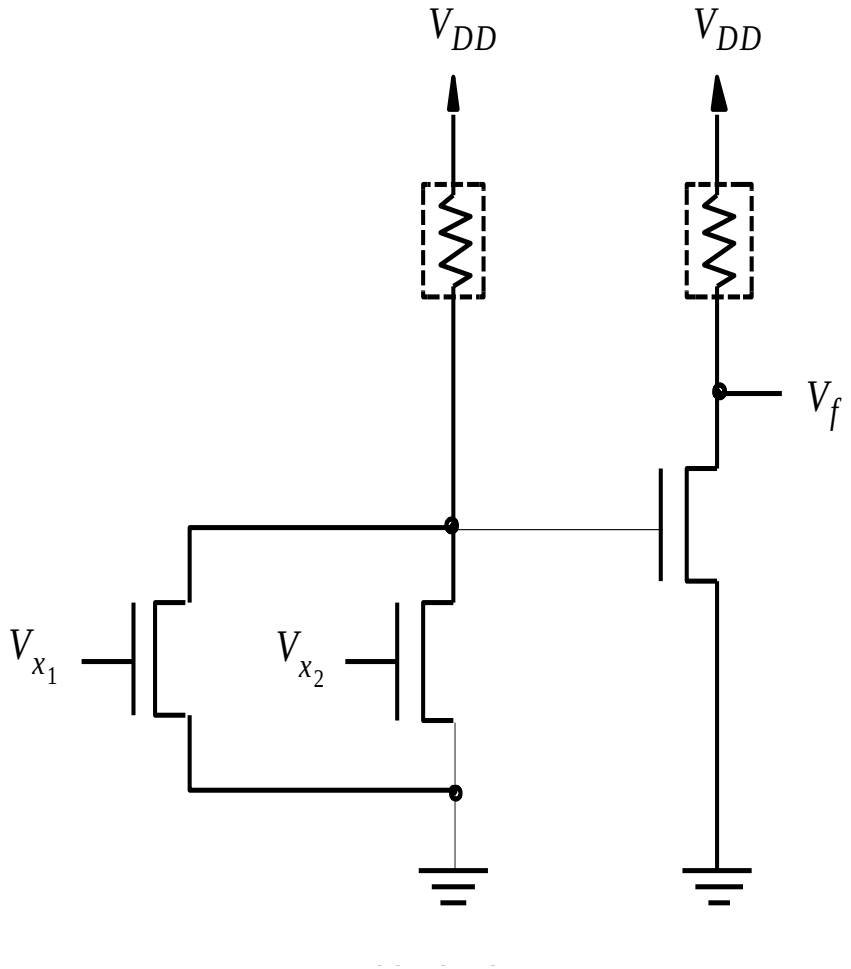
x_1	x_2	f
0	0	1
0	1	0
1	0	0
1	1	0





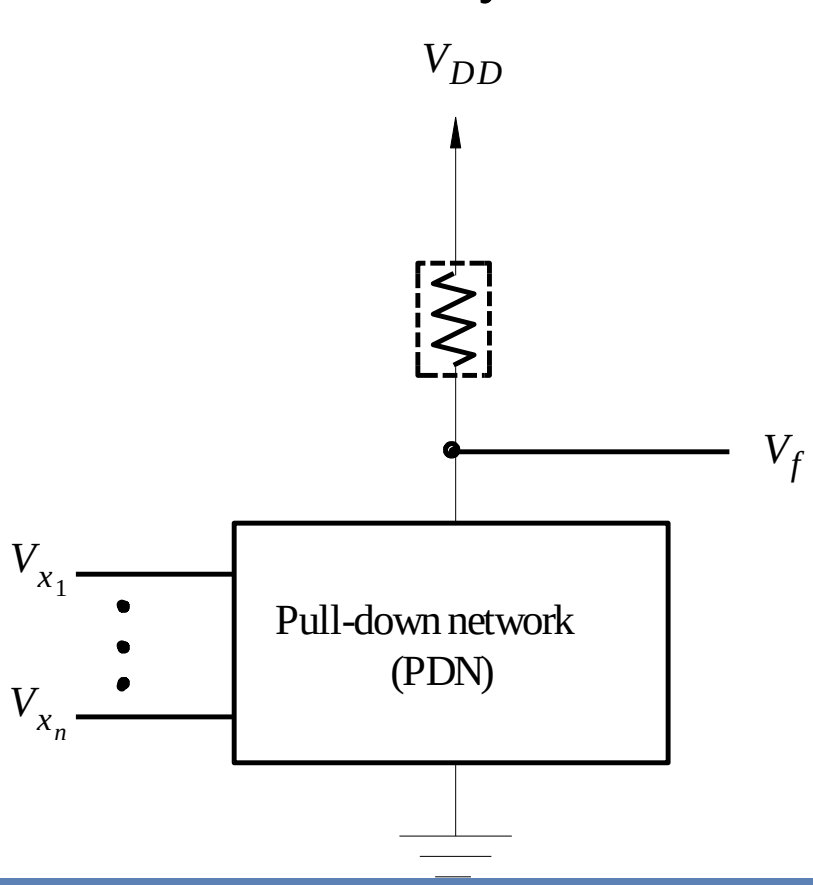
NMOS Realization of AND and OR Gates

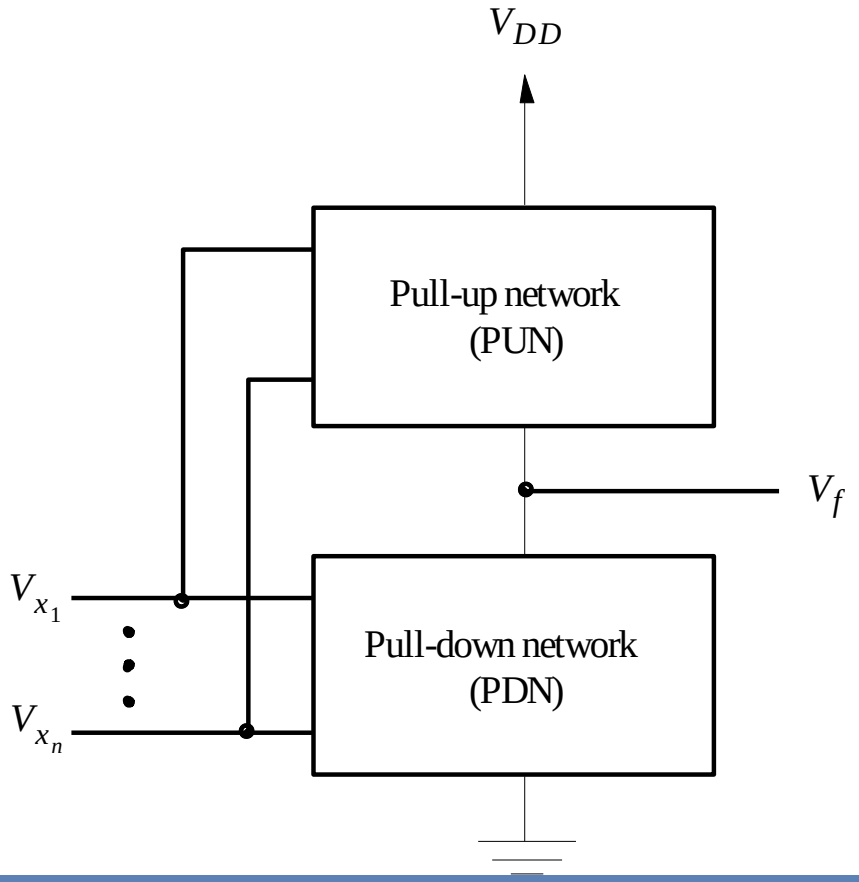




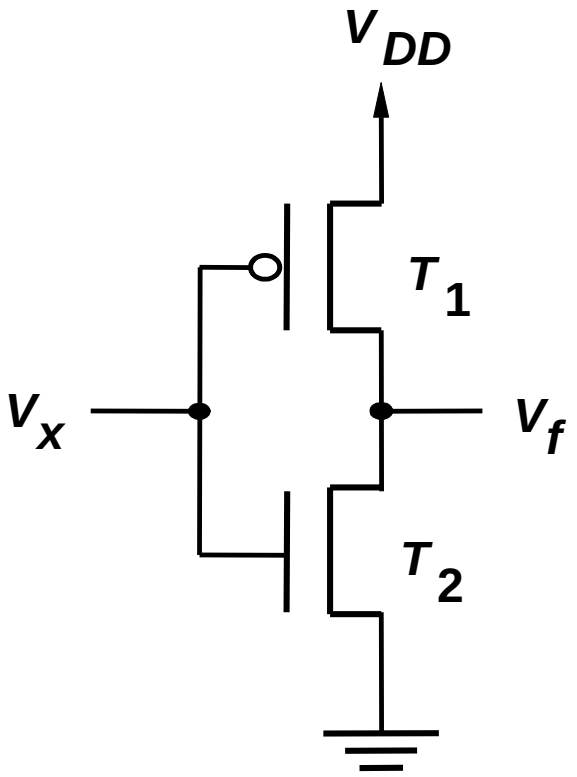
Structure of NMOS and CMOS Circuits

- Resistors are replaced as PMOS transistors, and thus P=0 theoretically.



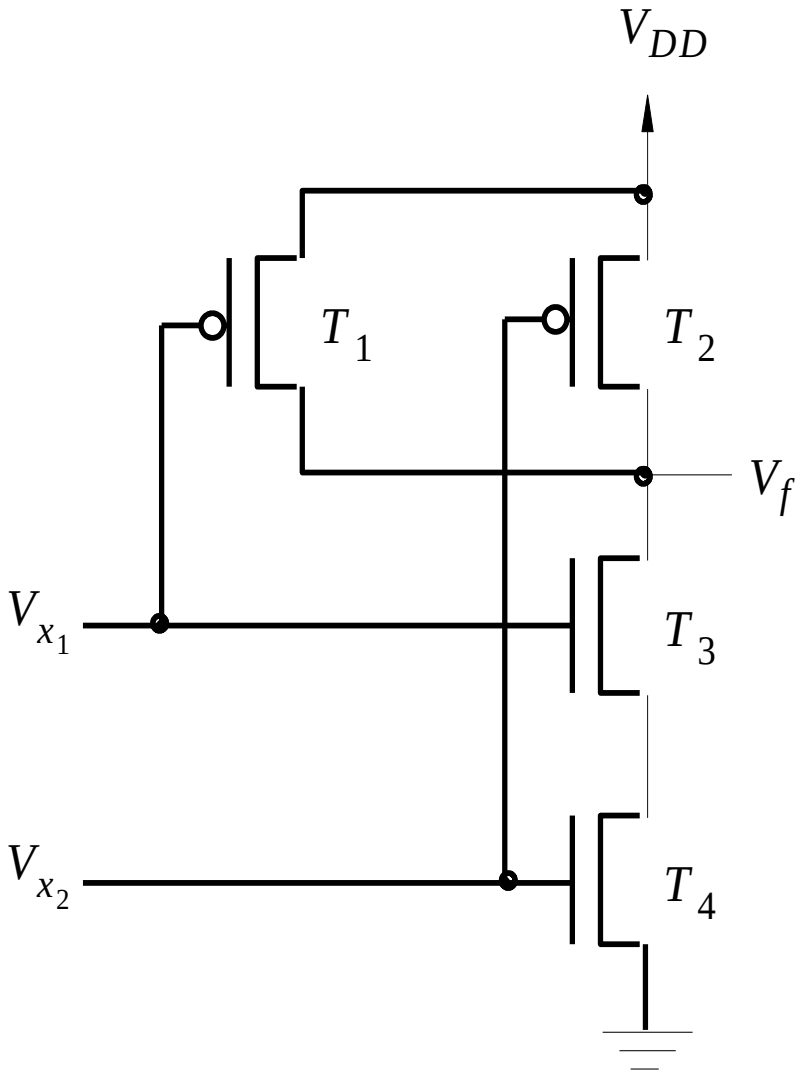


CMOS Realization of a NOT Gate



x	T_1 T_2	f
0	on off	1
1	off on	0

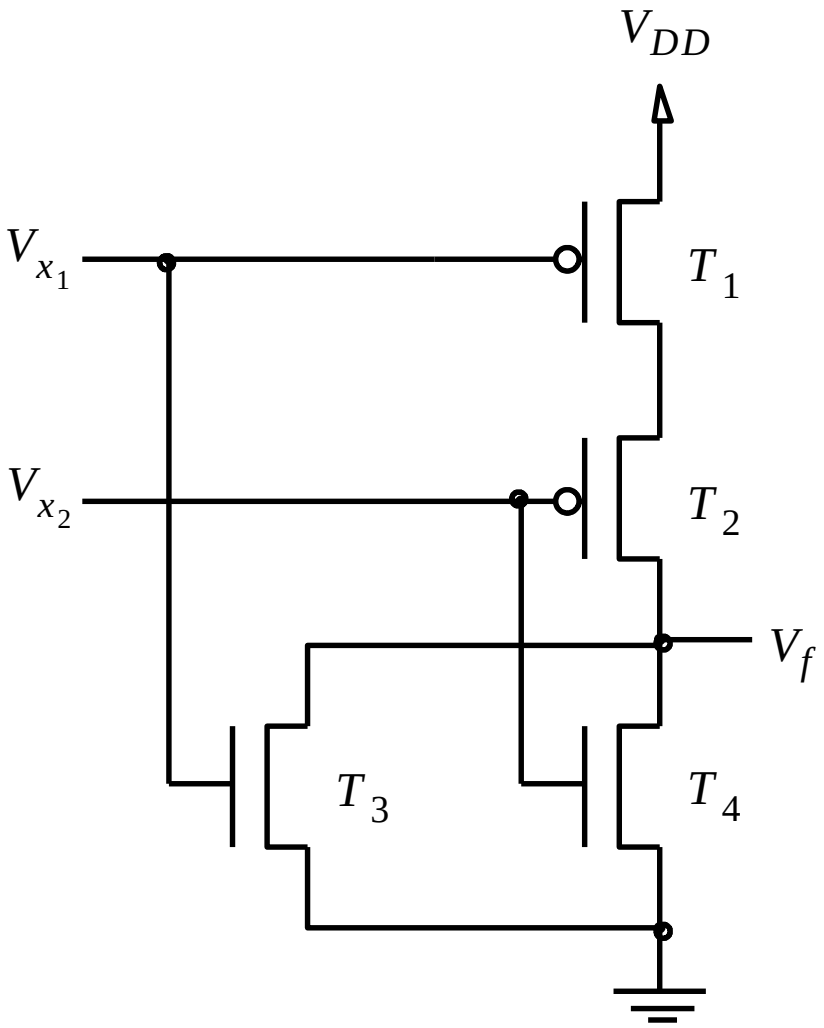
CMOS Realization of a NAND Gate



- PUN: $f = \overline{x_1 x_2} = \overline{x_1} + \overline{x_2}$
- PDN: $\bar{f} = x_1 x_2$

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

CMOS Realization of an NOR Gate

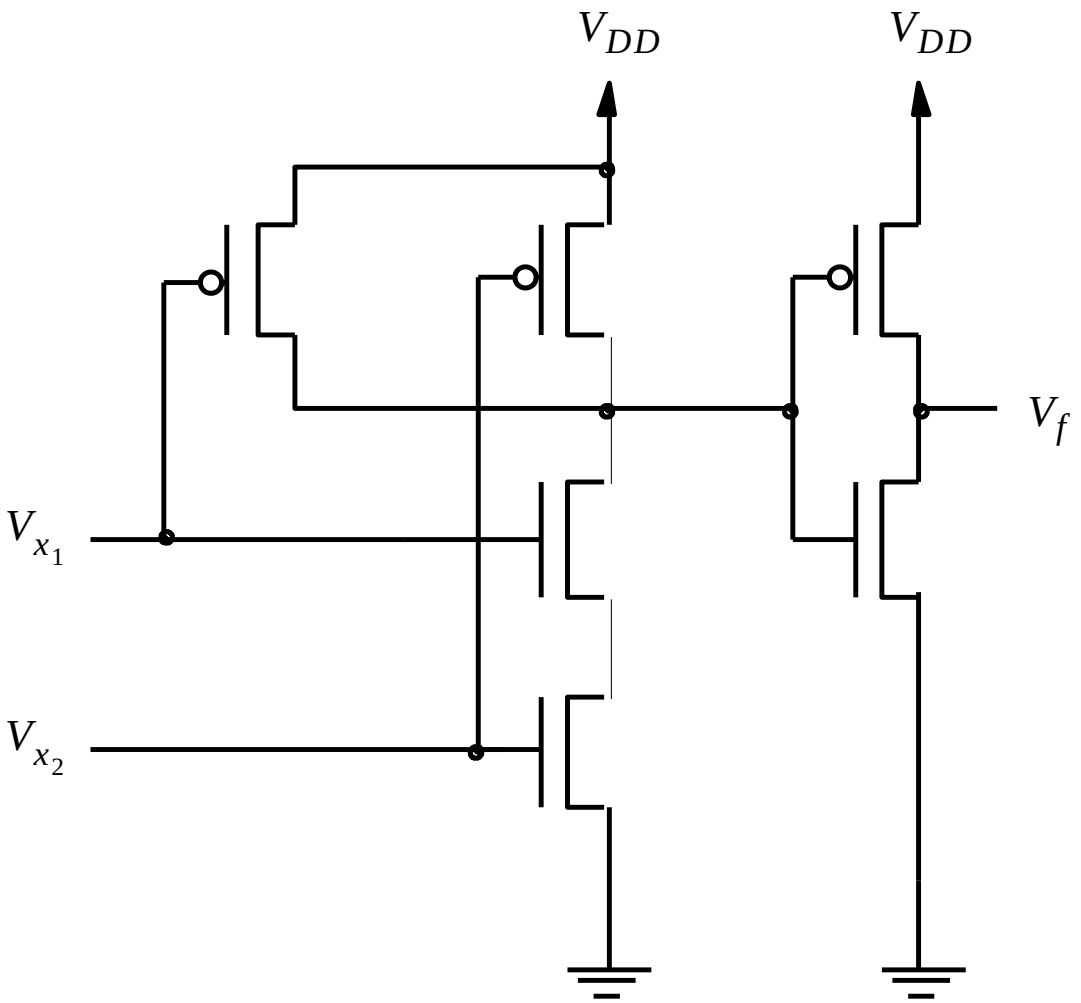


- PUN: $f = \overline{x_1 + x_2} = \overline{x_1 x_2}$
- PDN: $\bar{f} = x_1 + x_2$

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

CMOS Realization of an AND Gate

- NAND + NOT



Negative Logic System - NAND

- Voltage level

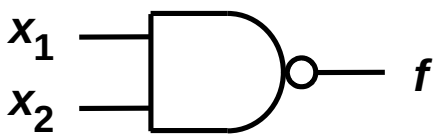
V_{x_1}	V_{x_2}	V_f
L	L	H
L	H	H
H	L	H
H	H	L

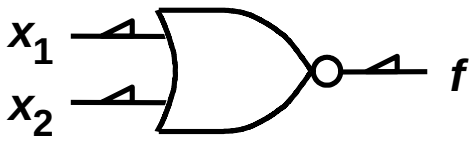
Positive logic

x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0

Negative logic

x_1	x_2	f
1	1	0
1	0	0
0	1	0
0	0	1





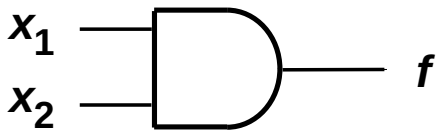
Negative Logic System - AND

- Voltage level

V_{x_1}	V_{x_2}	V_f
L	L	L
L	H	L
H	L	L
H	H	H

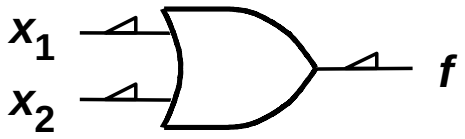
Positive logic

x_1	x_2	f
0	0	0
0	1	0
1	0	0
1	1	1

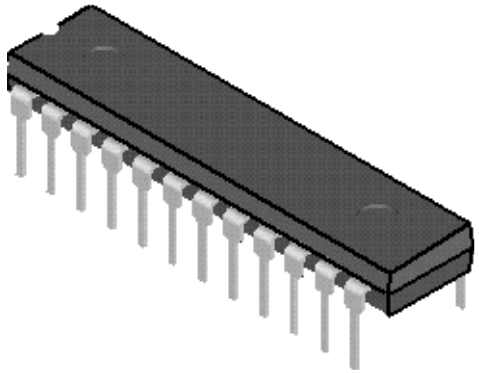


Negative logic

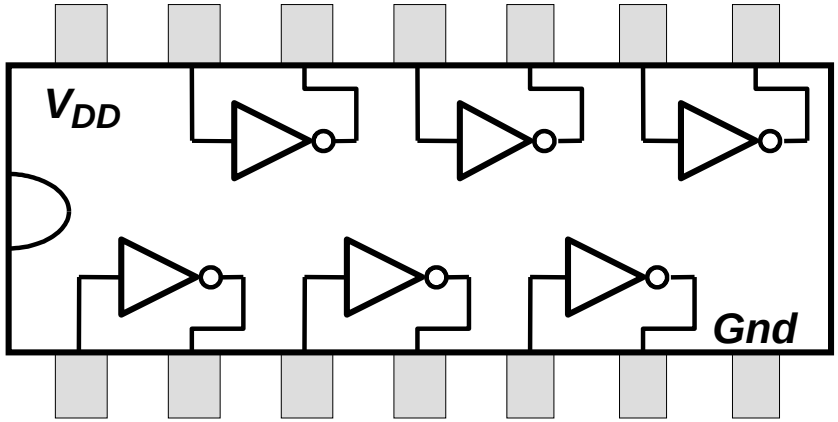
x_1	x_2	f
1	1	1
1	0	1
0	1	1
0	0	0



7400-Series Standard Chips

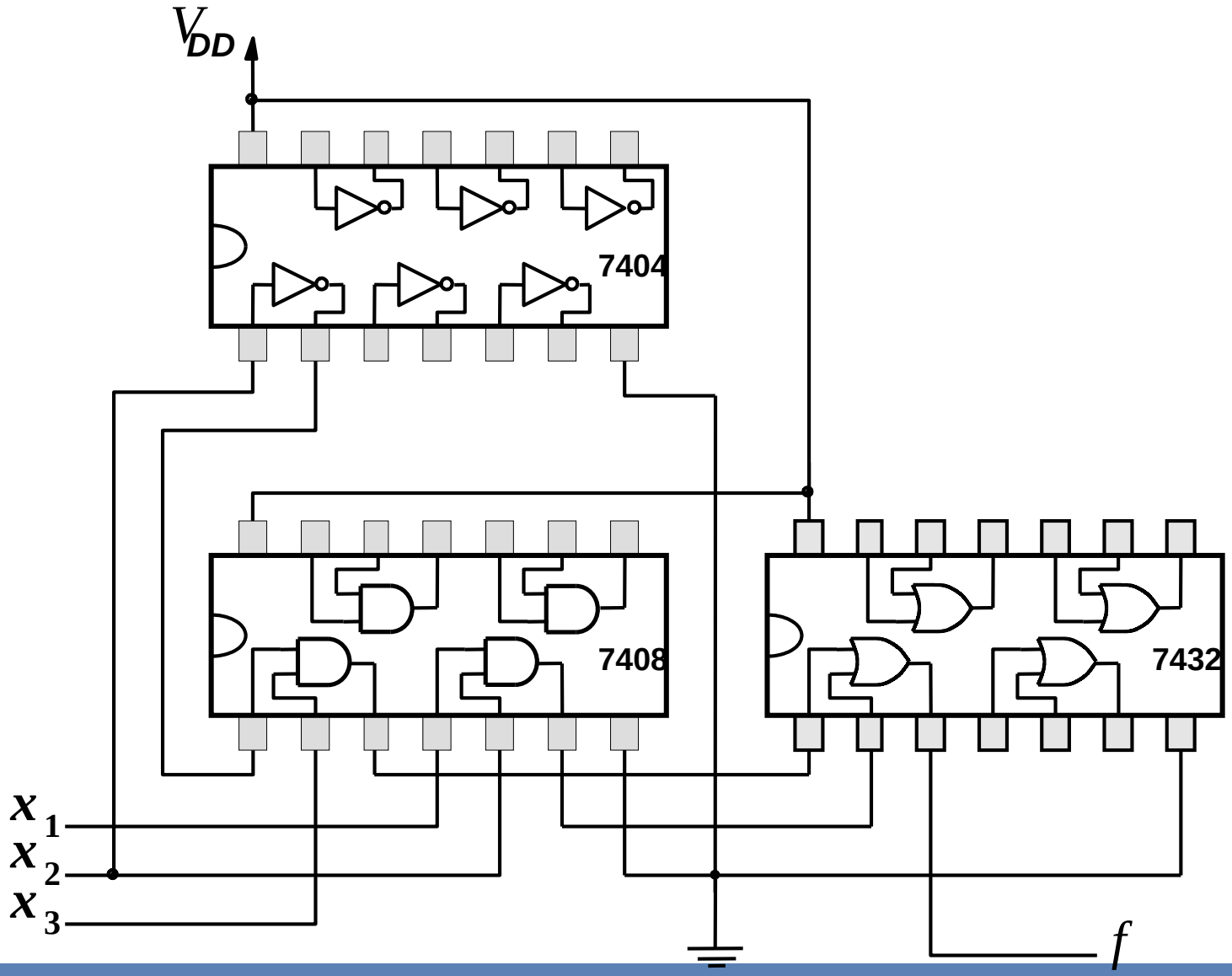


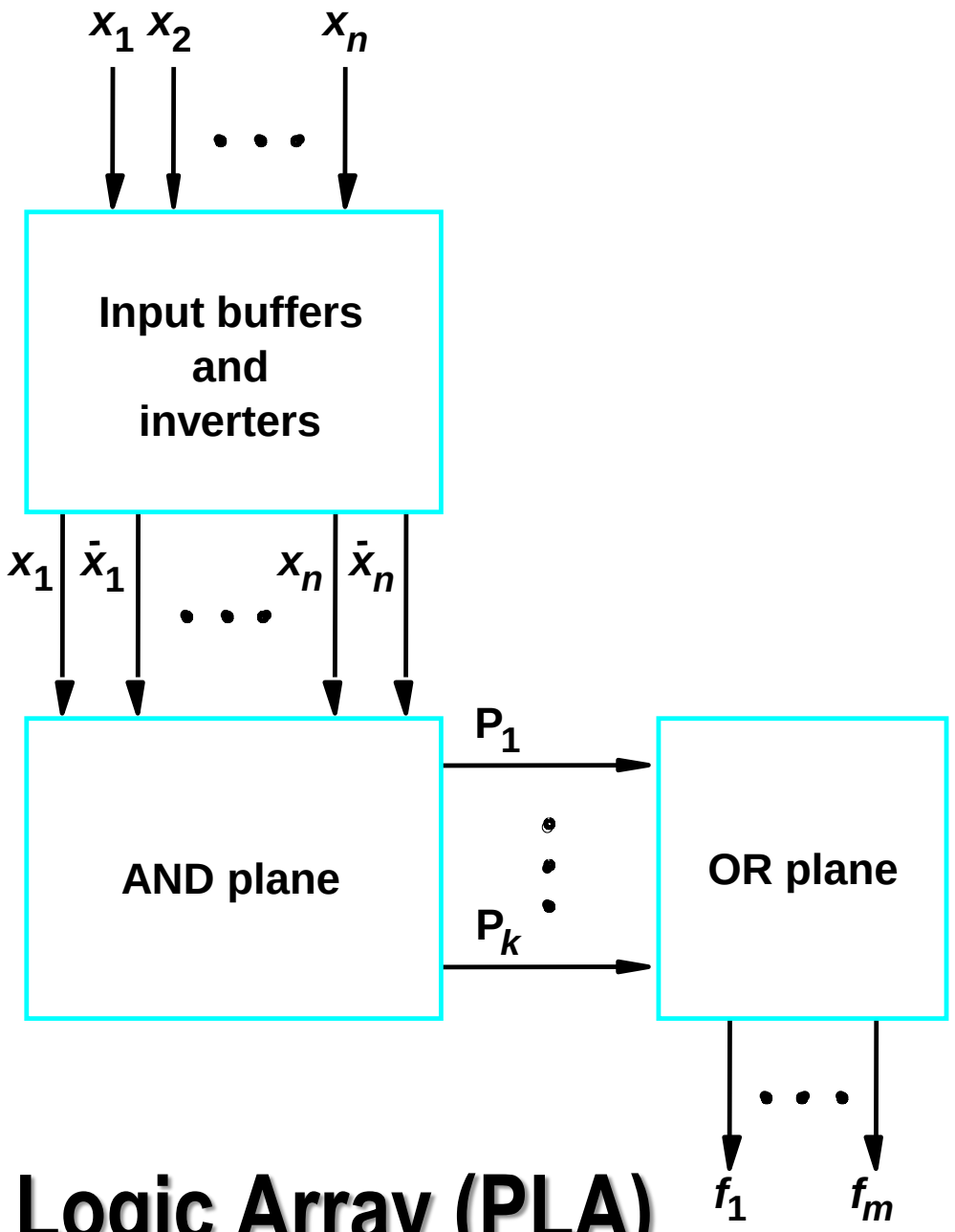
Dual-inline package



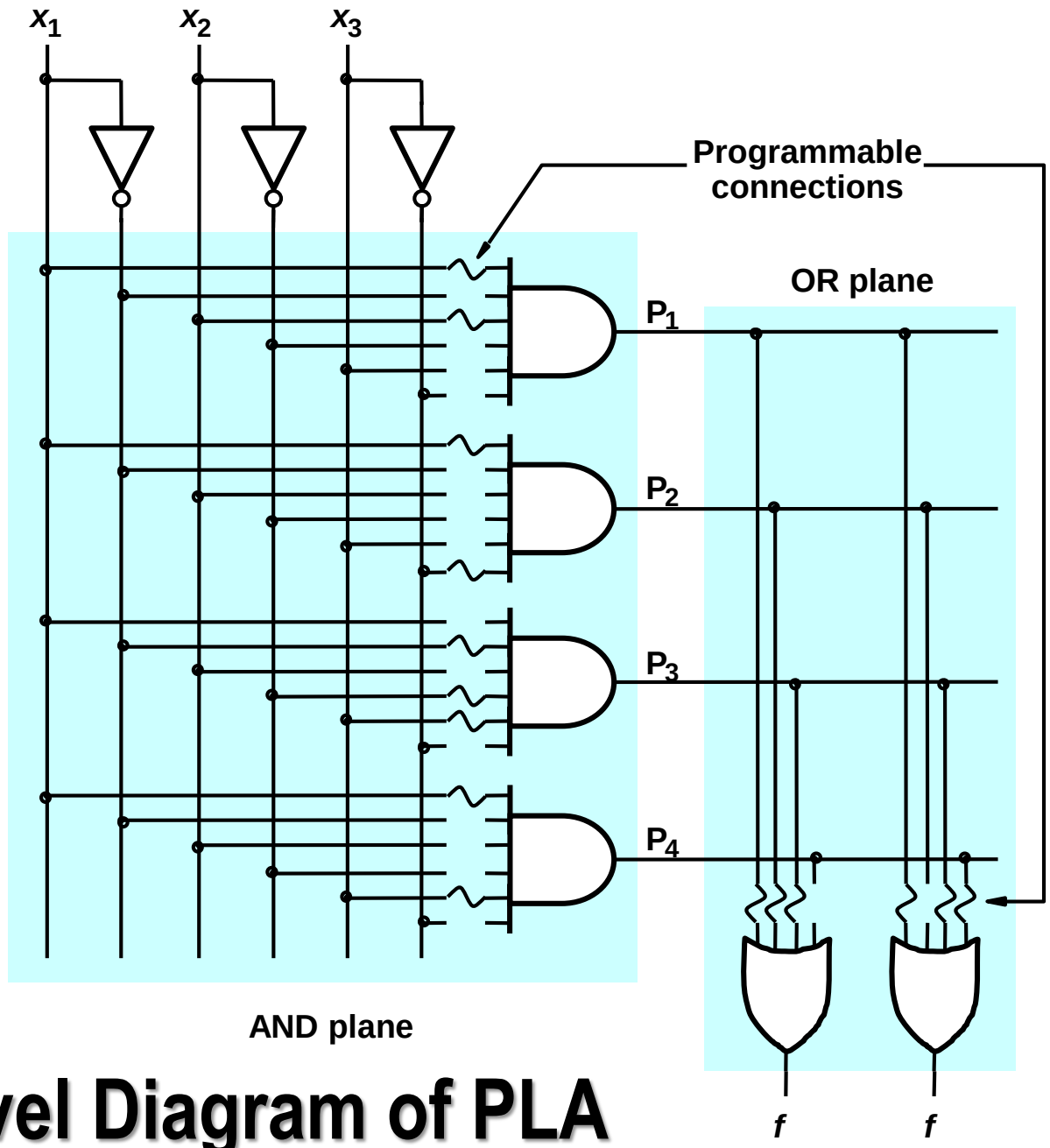
Structure of 7404 chip

Implementation with 74xx

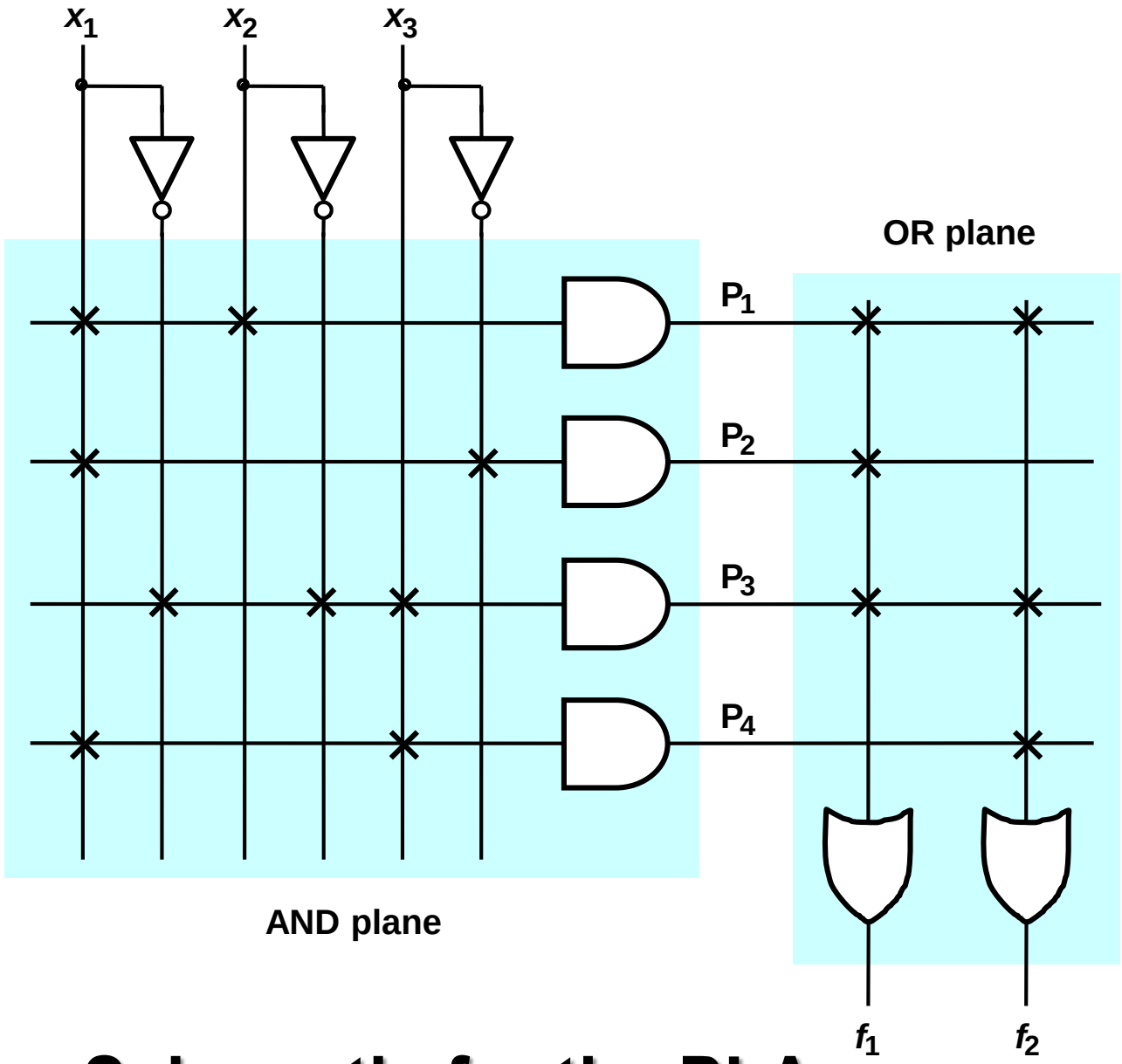




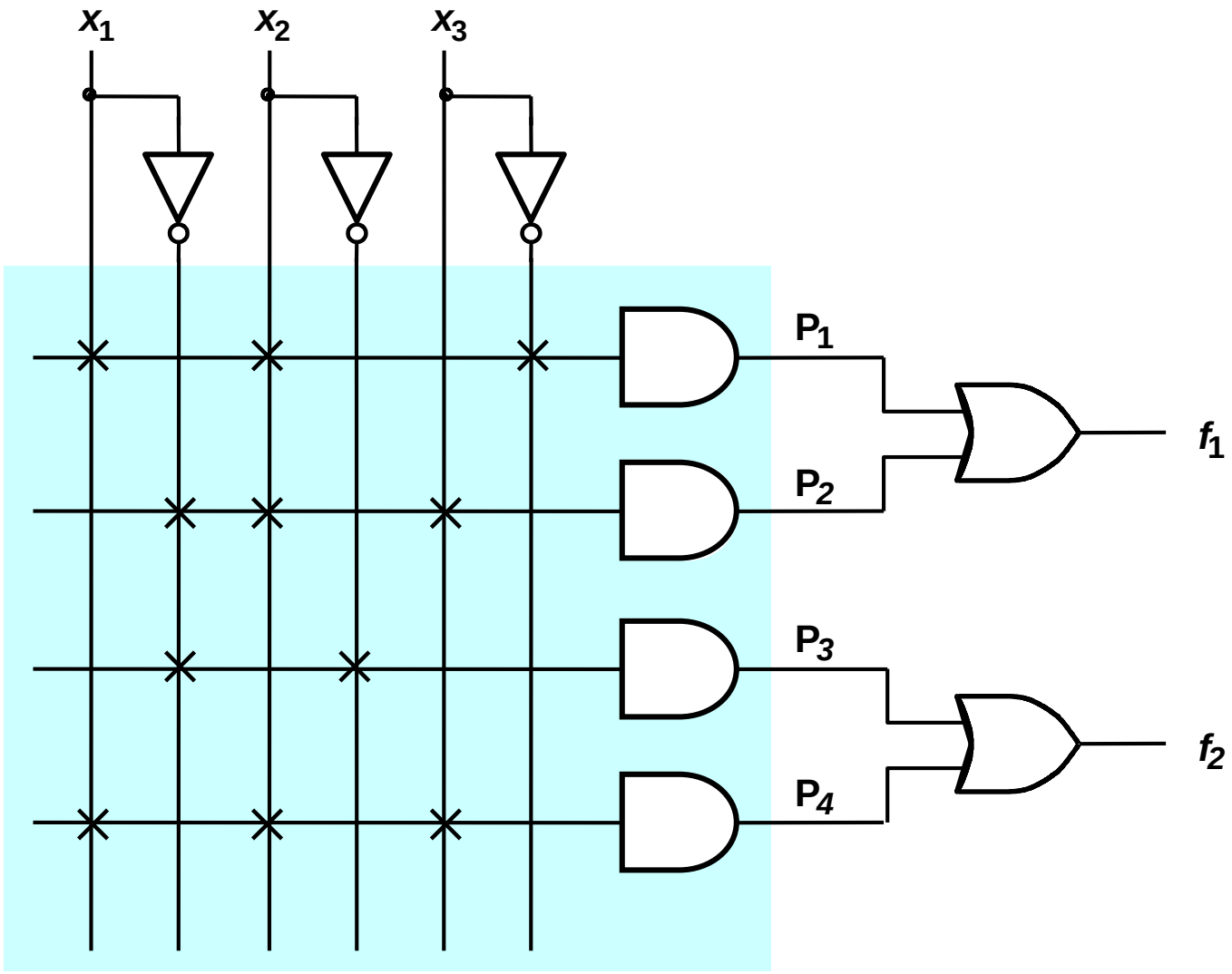
Programmable Logic Array (PLA)



Gate-level Diagram of PLA



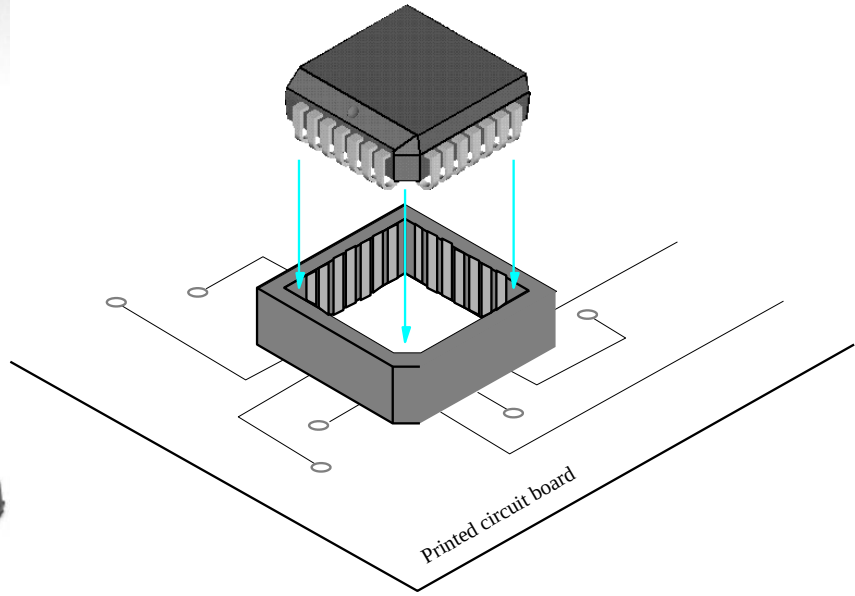
Customary Schematic for the PLA



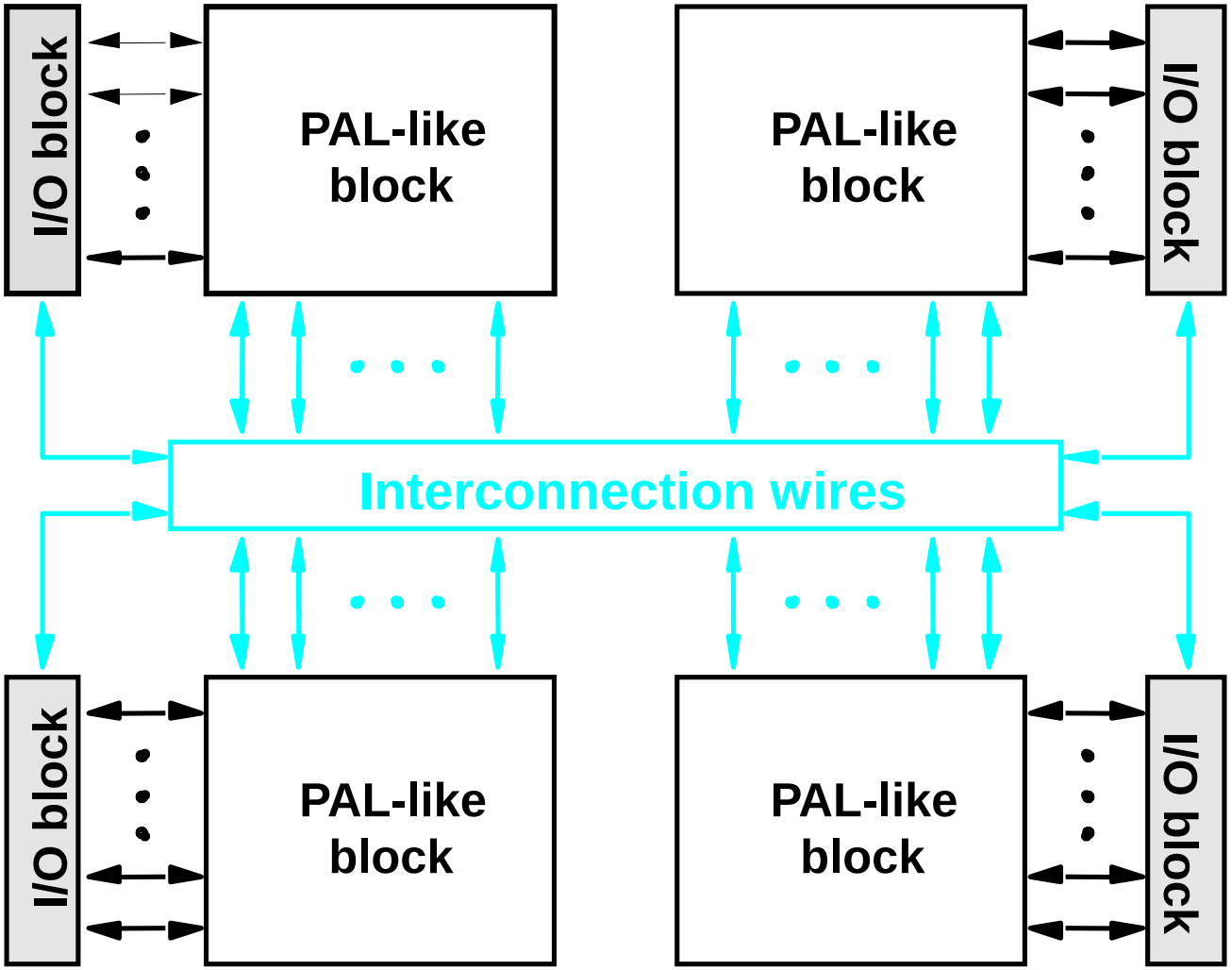
(Programmable Array Logic) PAL Example

Programming of PLD

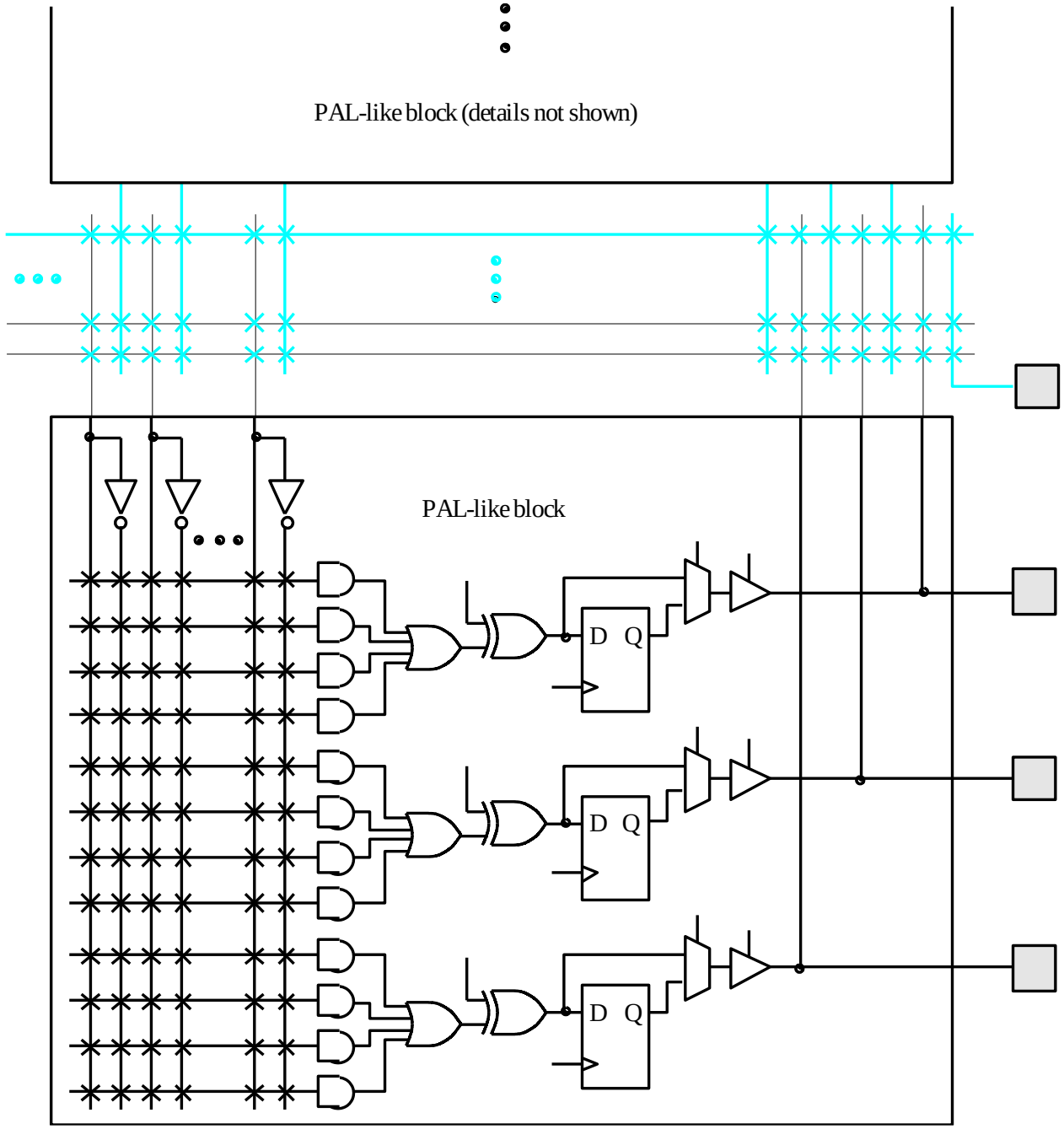
- Old Fashion: Programmer
- Current technology: Field programming



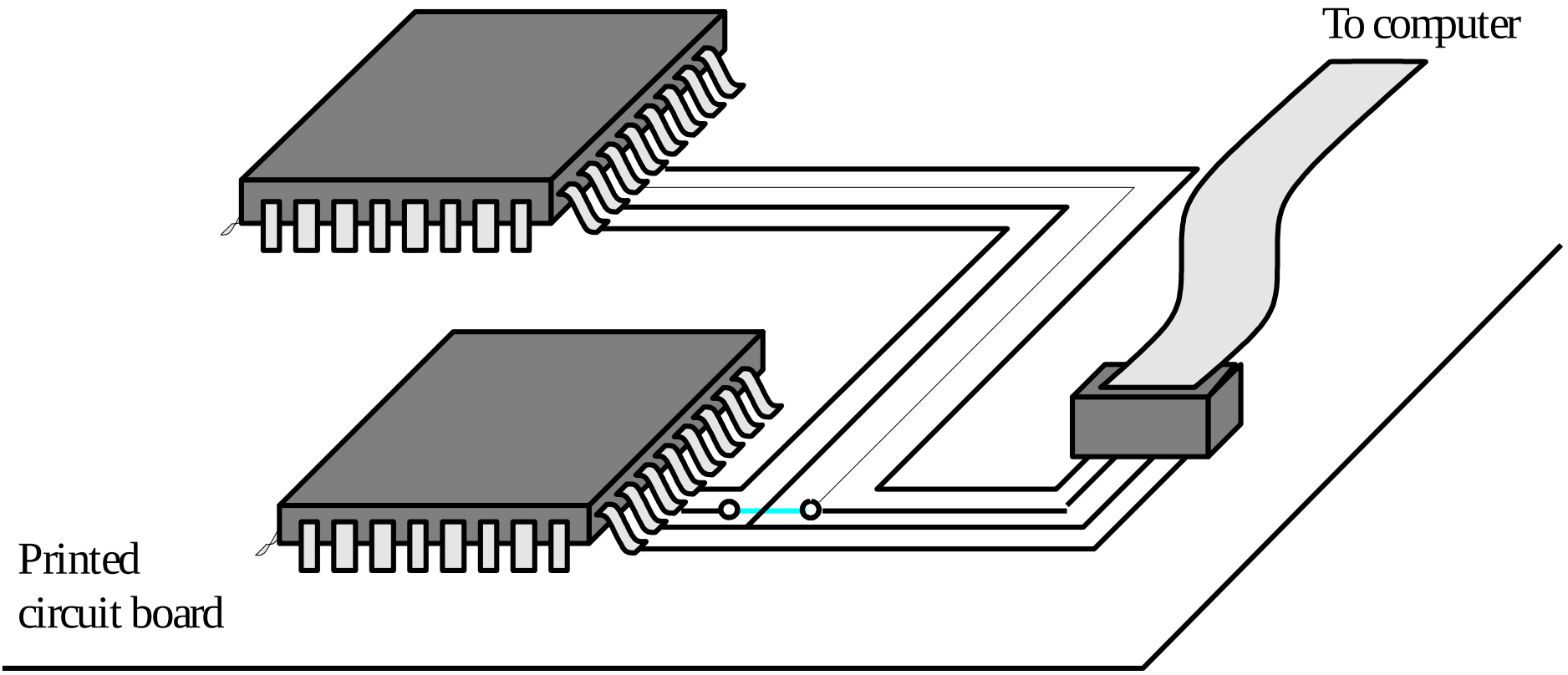
Complex Programmable Logic Device (CPLD)



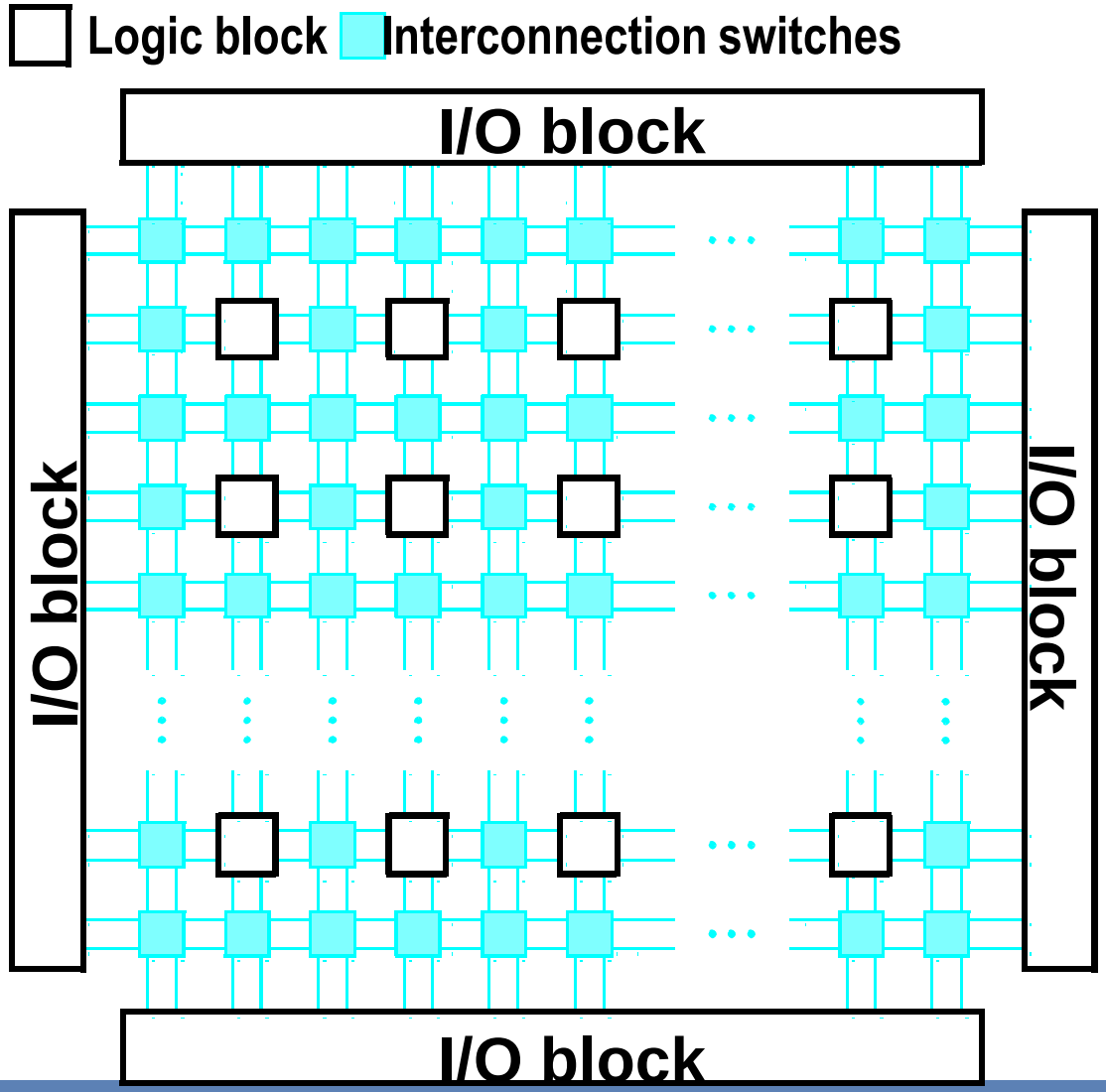
CPLD



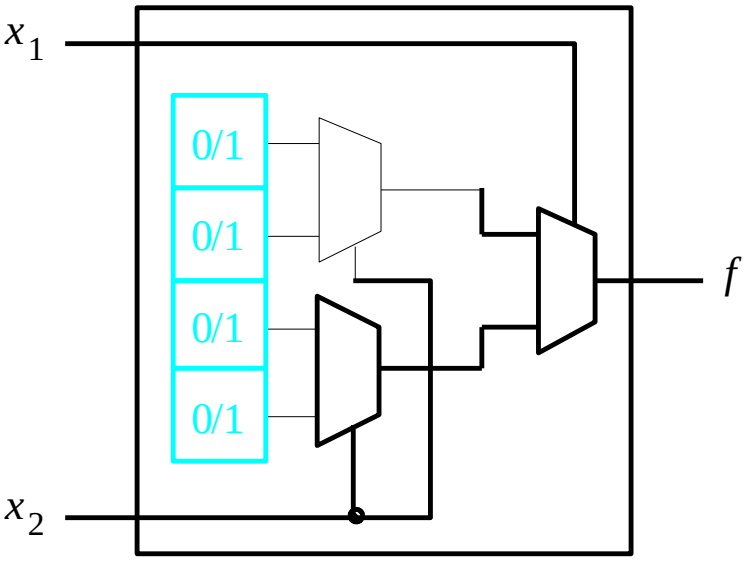
JTAG Programming



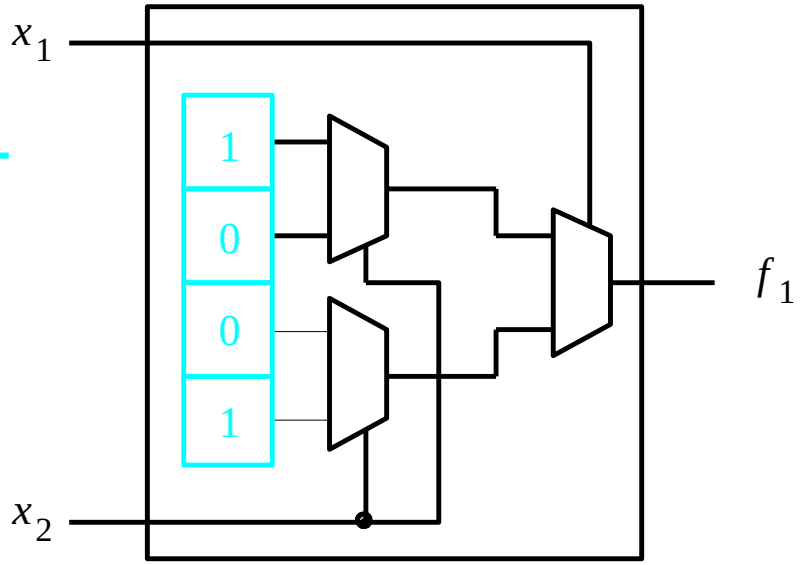
Field-Programmable Gate Arrays (FPGA)



Two-Input LUT (Look-up Table)



x_1	x_2	f_1
0	0	1
0	1	0
1	0	0
1	1	1



A Section of FPGA