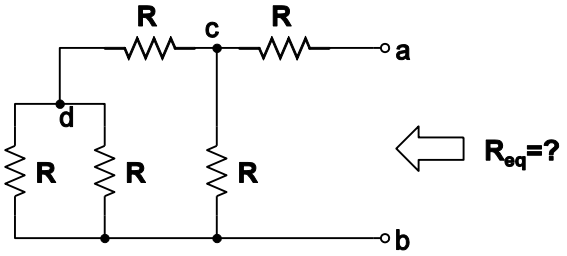
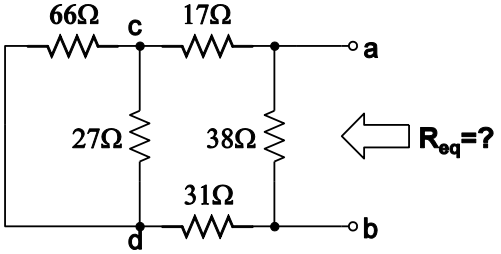
Exercises for Chapters 1 & 2

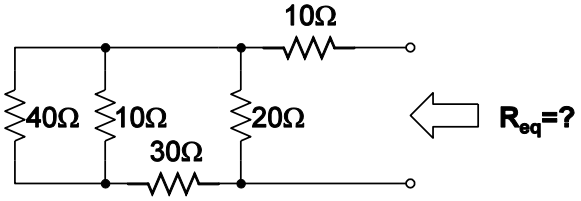
1. Please find the equivalent resistance of the following circuit.



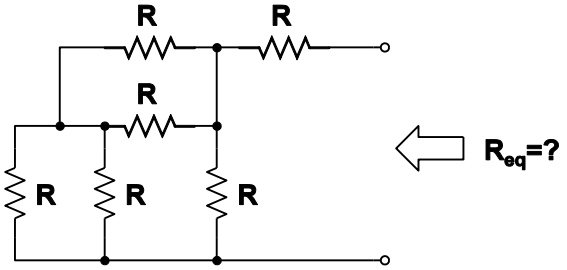
2. Please find the equivalent resistance of the following circuit.



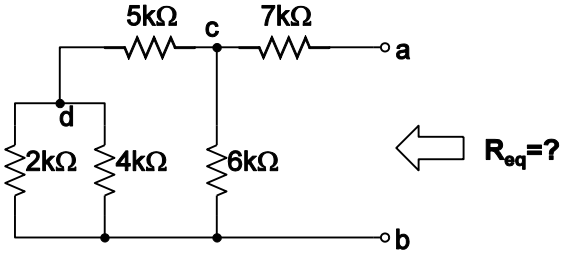
3. Please find the equivalent resistance of the following circuit.



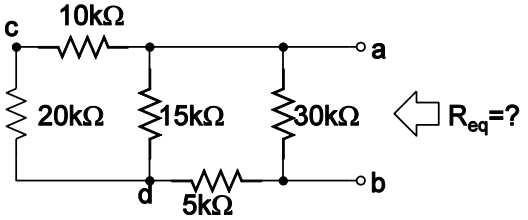
4. Please find the equivalent resistance of the following circuit [R=10Ω].



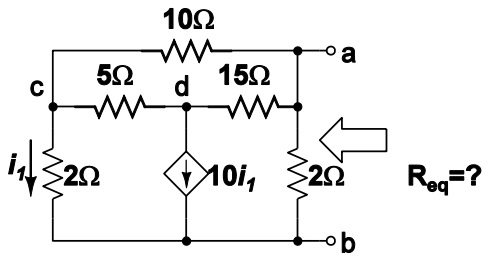
5. Please find the equivalent resistance of the following circuit.



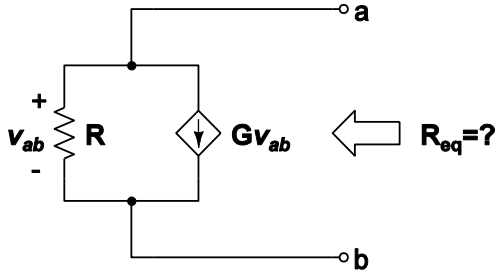
6. Please find the equivalent resistance of the following circuit.



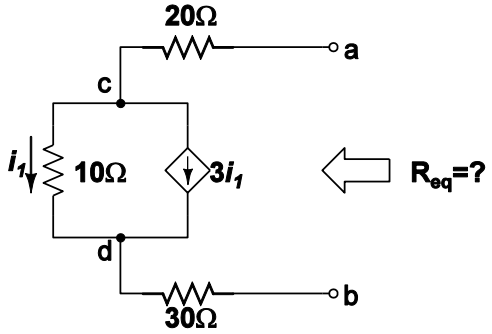
7. Please find the equivalent resistance of the following circuit.



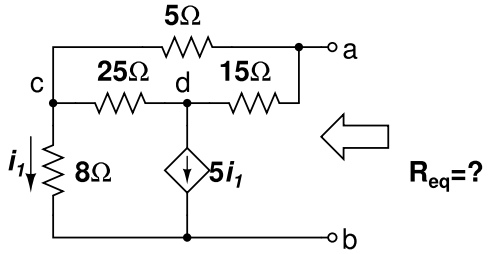
8. Please find the equivalent resistance of the following circuit.



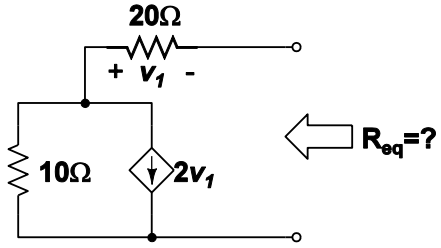
9. Please find the equivalent resistance of the following circuit.



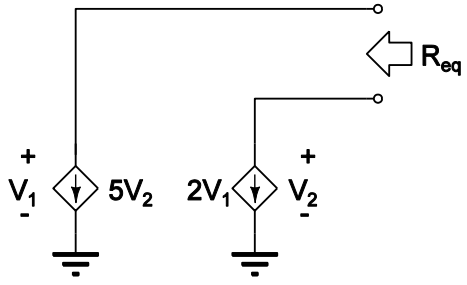
10. Please find the equivalent resistance of the following circuit.



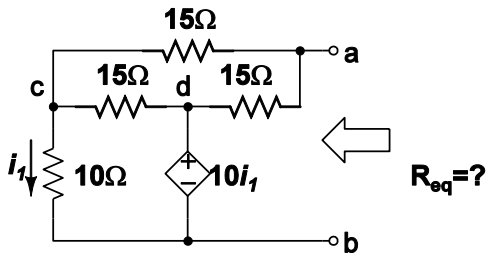
11. Please find the equivalent resistance of the following circuit.



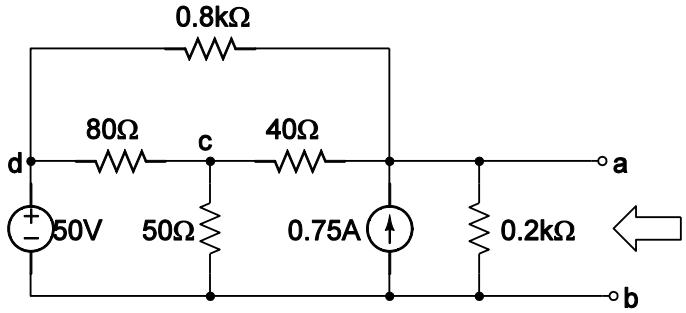
12. Please find the equivalent resistance of the following circuit.



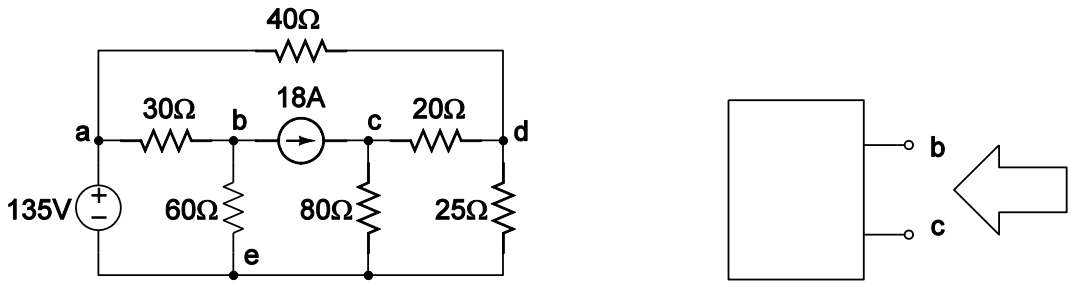
13. Please find the equivalent resistance of the following circuit.



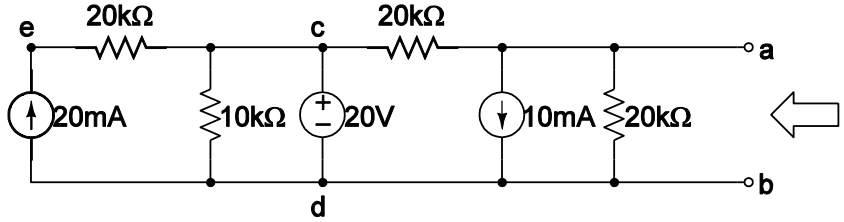
14. Please find the Thevenin equivalent circuit of the following circuit.



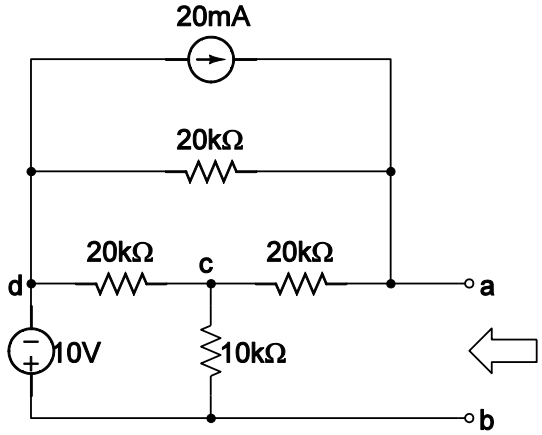
15. Please find the Norton equivalent circuit looking into nodes b and c.



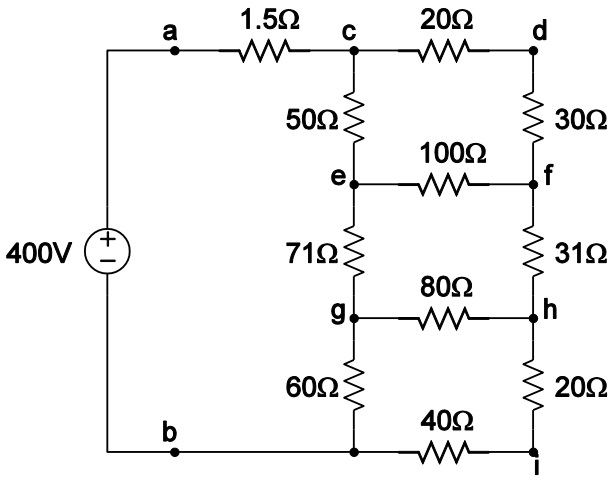
16. Please find the Thevenin equivalent circuit of the following circuit.



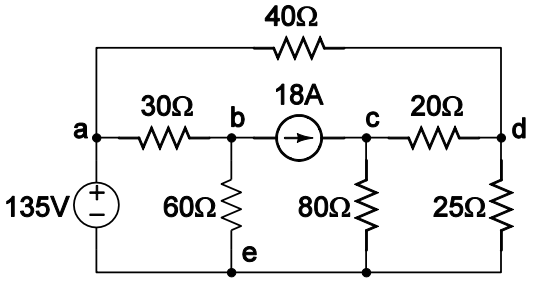
17. Please find the Norton equivalent circuit of the following circuit.



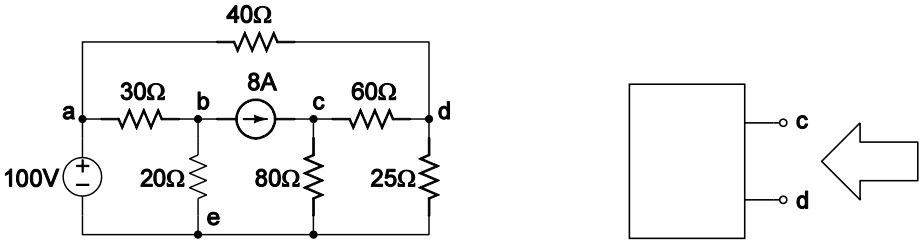
18. Please find the power dissipated in the 71Ω resistor.



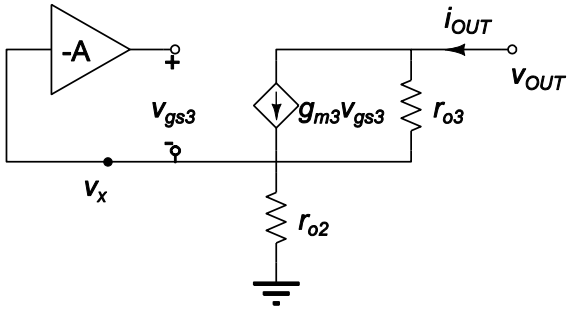
19. Please find the current provided by the 135V voltage source.



20. Please find the Thevenin equivalent circuit looking into nodes c and d.

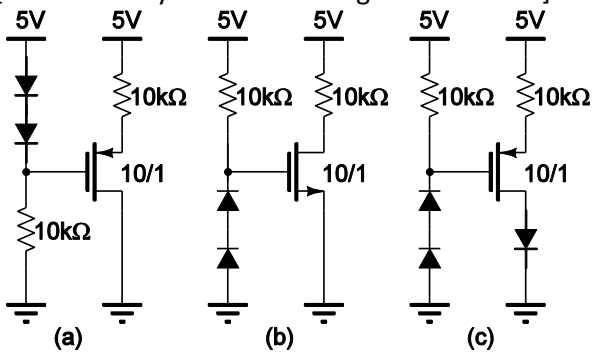


21. For the previous circuit, please find the power generated by each of the two ideal sources.
22. Please find the equivalent output resistance (looking into v_{out}) of the following circuit (note: -A is an voltage amplifier with gain of -A).



Exercises for Chapter 3

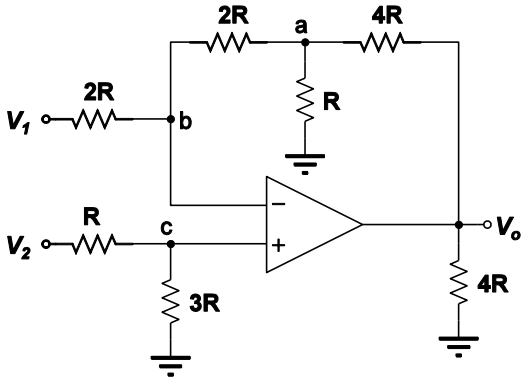
1. Assume all diodes have ON voltage of 0.7 V and all MOSFETs have the following parameters: $\mu_o C_{ox}$ = 1 mA/V^2, λ = 0.05, and $V_{tn} = -V_{tp}$ = 1V.Please find the operating region (cut-off, saturation, or triode) of the following circuits. [Please show your work leading to the answer]



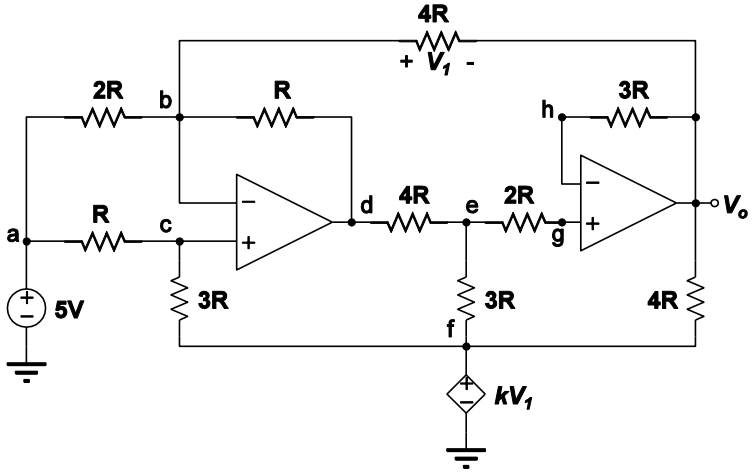
2. Please draw a CMOS logic implementation of Y=(A+B(C+D))' [Do not cascade stages and use only A, B, C, and D as inputs.]
3. A MOSFET operating in the triode region can be used as a resistor when V_{DS} is small. Please find the resistance between the source and drain terminals for an NMOS transistor if $\mu_n C_{ox}$ = 100 µA/V^2, W/L = 10 µm/1 µm, V_t = 0.7 V, and V_{GS} = 1.2 V.
4. Please find the resistivity of intrinsic silicon given that $n_i = 1.5\times10^{10}$ cm^{-3}, μ_n = 1350 cm^2/V·s, and μ_p = 480 cm^2/V·s.
5. Please draw the CMOS realization of (A(B+CD))'.
6. Please find the resistivity of intrinsic germanium given that $n_i = 2.4\times10^{13}$ cm^{-3}, μ_n = 3900 cm^2/V·s, and μ_p = 1900 cm^2/V·s.
7. Please draw a CMOS logic implementation of Y=AB+CD.

Exercises for Chapter 4

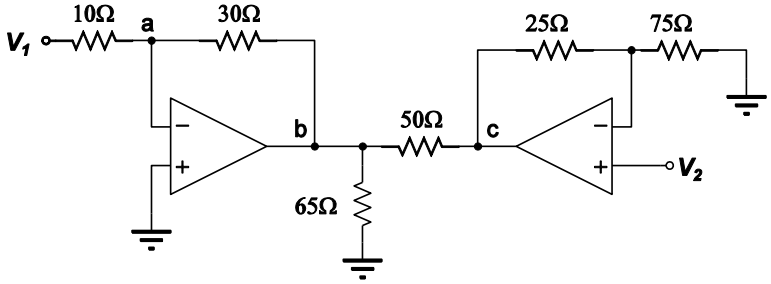
1. Please express V_o in terms of V_1 and V_2.



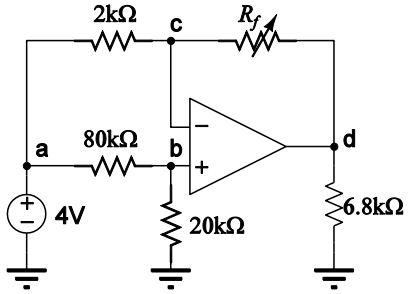
2. Please find k such that V_o=10V



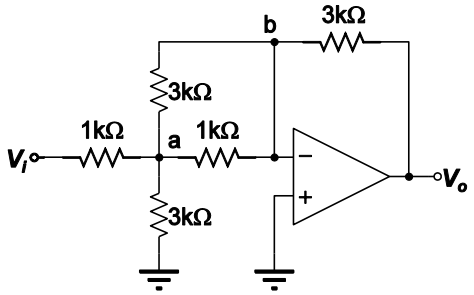
3. Please find the relationship of V_1 and V_2 such that no power is dissipated in the 50Ω resistor.



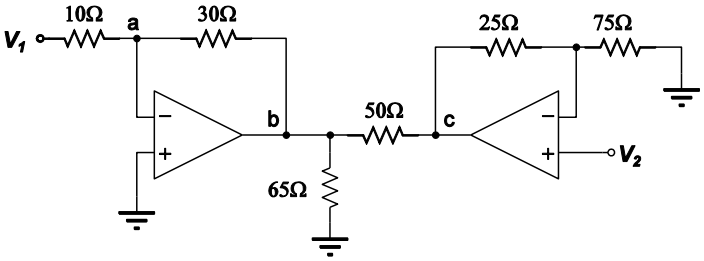
4. Please find R_f such that the power dissipated in the 6.8 kΩ resistor is 6.8 mW.



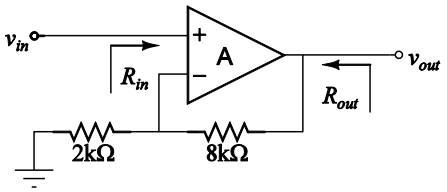
5. Please find the gain of the following circuit. [Note: *Gain*=V_o/V_i]



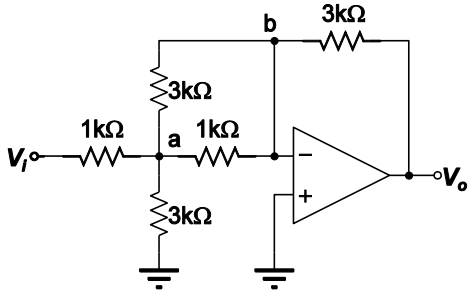
6. Please find V_2 when V_1=5V and the power dissipated in the 50Ω resistor equals to the power dissipated in the 65Ω resistor.



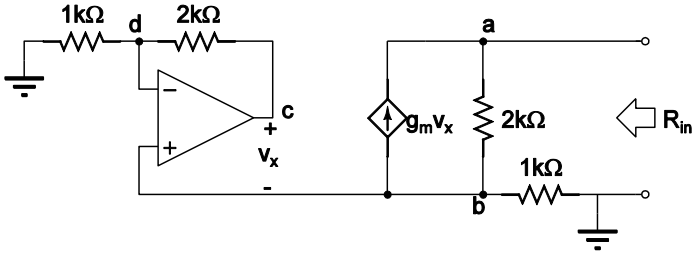
7. For the following feedback amplifier, what are the input (R_{in}) and output (R_{out}) resistances if the voltage gain of A is 150, the input and output resistances of A are 50 kΩ and 1 kΩ, respectively.



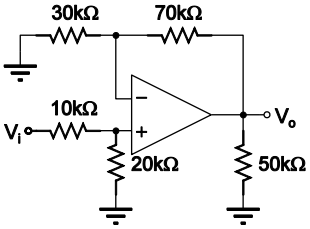
8. If the OPAMP of the following circuit has supply voltages of ±5V, Please the range of V_i such that V_o does not saturate.



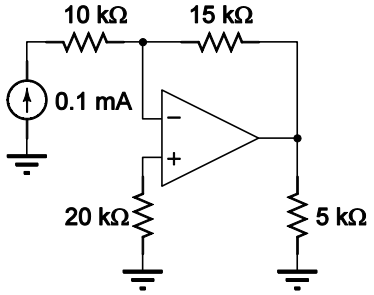
9. Please find the equivalent resistance of the following circuit, where g_m=1mS.



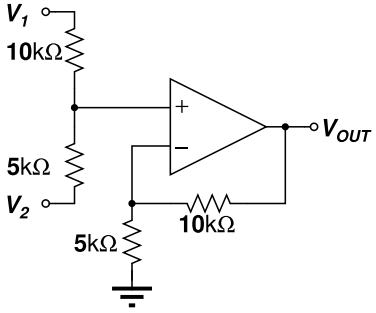
10. Please find V_i when the power dissipated by the 70kΩ resistor equals to 2800μW.



11. Please find the power dissipated in the 5kΩ resistor.

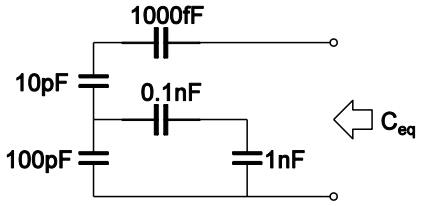


12. For the following circuit, $V_{OUT} = aV_1 + bV_2$ .Please find ***a*** and ***b***.

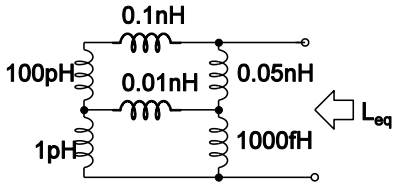


Exercises for Chapter 5

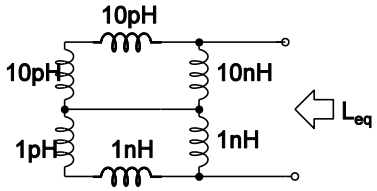
1. Please find the equivalent capacitance (in pF) of the following circuit.



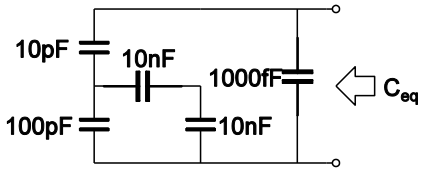
2. Please find the equivalent inductance of the following circuit at 1 MHz.



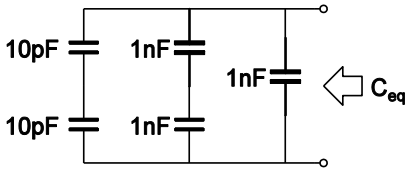
3. P Please find the equivalent inductance of the following circuit at 1 MHz.



4. Please find the equivalent capacitance of the following circuit (in pF).

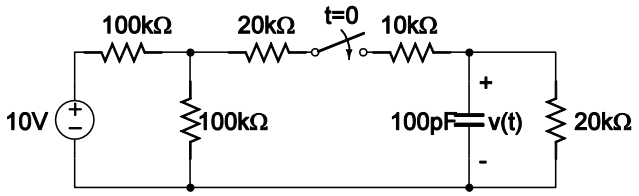


5. Please find the equivalent **<u>capacitance</u>** of the following circuit (in **fF**).

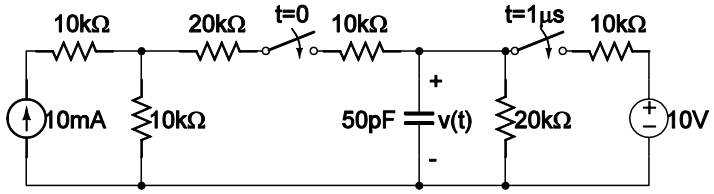


Exercises for Chapters 6

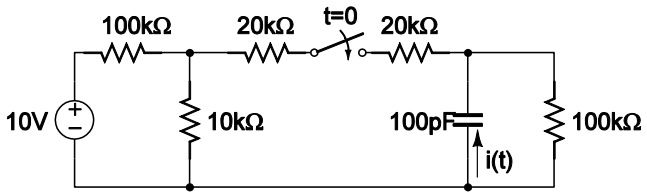
1. Please find v(t) of the following circuit and plot v(t) versus time.



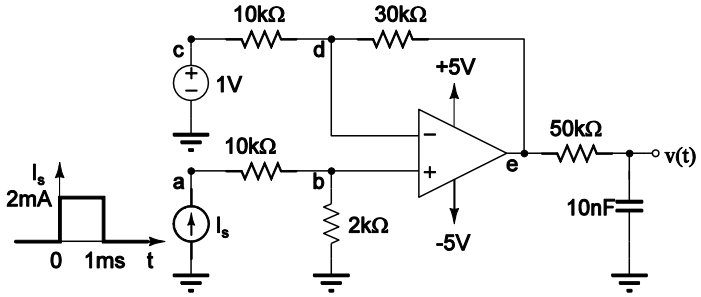
2. Please find v(t) of the following circuit and plot v(t) versus time.



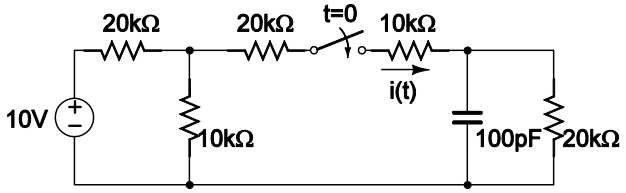
3. Please find i(t) of the following circuit and plot i(t) versus time.



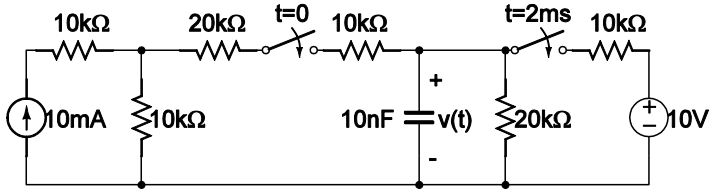
4. For the following circuit, please find and make plots of v(t) and voltage at node d.



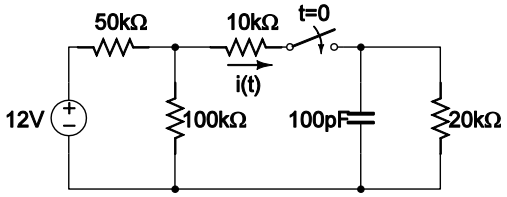
5. Please find v(t) of the following circuit and plot v(t) versus time.



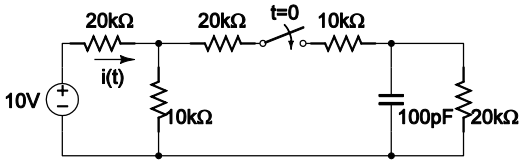
6. Please find v(t) of the following circuit and plot v(t) versus time.



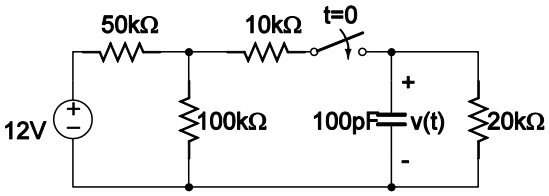
7. For the following circuit, please find and "PLOT" i(t) versus t for all t.



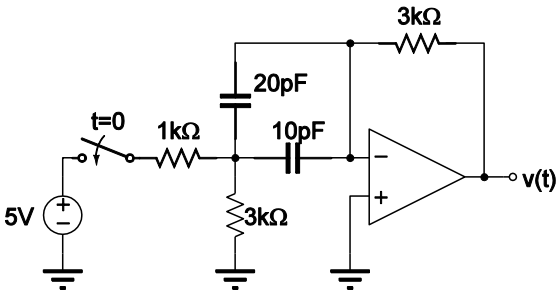
8. Please <u>find</u> i(t) of the following circuit and <u>plot</u> i(t) versus time.



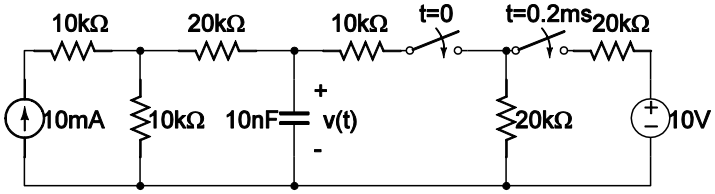
9. For the following circuit, please find and PLOT v(t) vs. t for all t. (steady state for t<0)



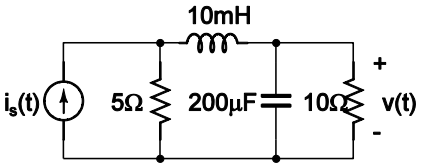
10. For the following circuit, please find and PLOT v(t) versus t for all t. (steady state for t<0)



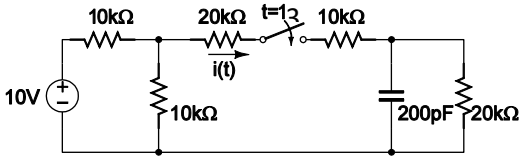
11. For the following circuit, please find and PLOT v(t) vs. t for all t. (steady state for t<0)



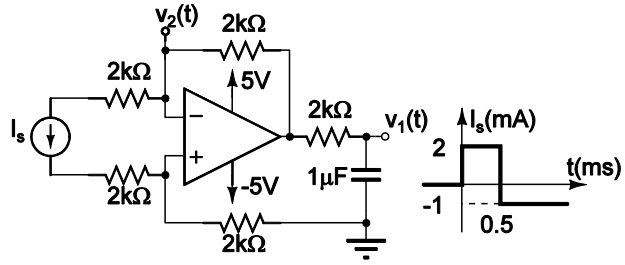
12. Please find the differential equation that can be used to solve v(t) [no need to solve].



13. Please <u>find</u> i(t) of the following circuit and <u>plot</u> i(t) versus time.

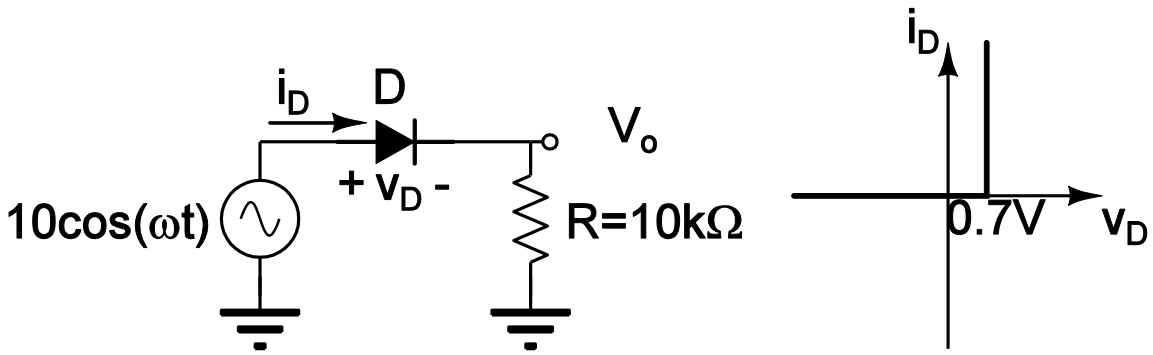


14. For the following circuit, please find and make plots of $v_1(t)$ and $v_2(t)$. (steady state for t<0)



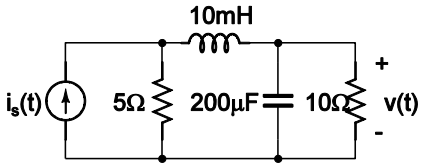
Exercises for Chapter 7

1. If the diode in the lower left figure has a characteristic curve as the figure in the lower right ◦
   (a) Please find the maximum value of Vo.
   (b) Please find the maximum instantaneous power dissipated in R.
   (c) Please find the average power dissipated in R.
   (d) Please find the maximum instantaneous power dissipated in D.
   (e) Please find the average power dissipated in D.



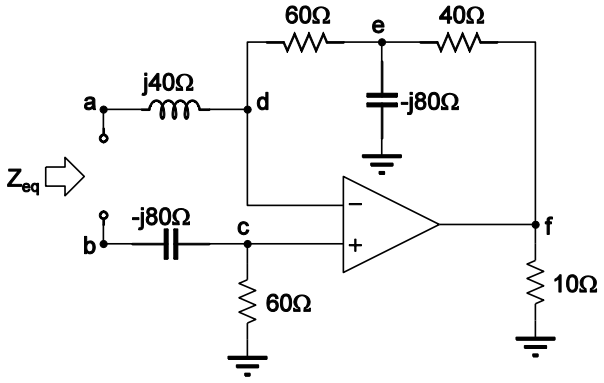
Exercises for Chapter 8

1. Assume $i_s(t)=2\cos(1000t)$ (Ampere) in the following circuit, find v(t).

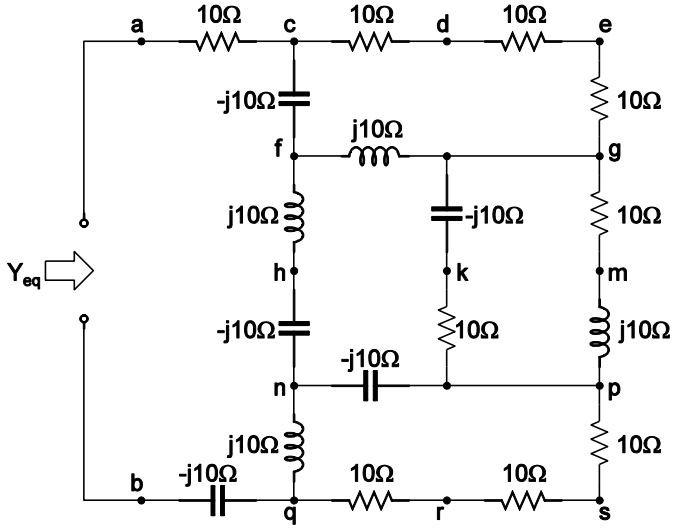


Exercises for Chapter 9

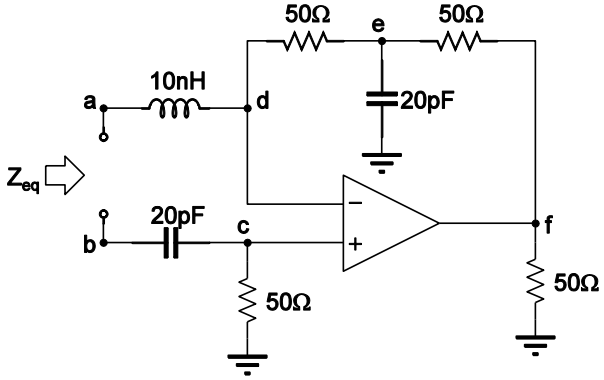
1. Please find the equivalent impedance of the following circuit.



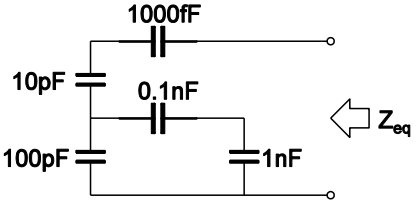
2. Please find the equivalent admittance of the following circuit.



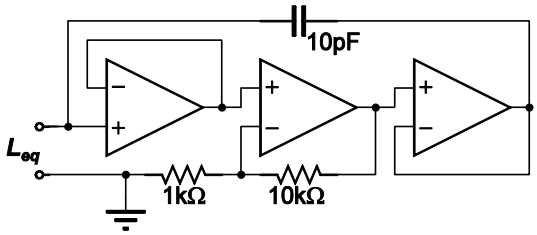
3. Please find the equivalent impedance of the following circuit at 10MHz.



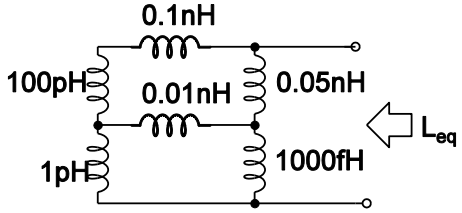
4. Please find the equivalent impedance of the following circuit at 1 MHz.



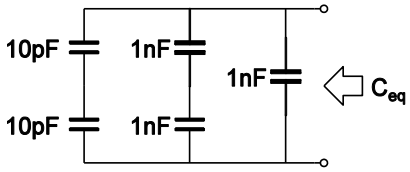
5. The following circuit is an active inductor, please find the inductance at 10MHz.



6. Please find the equivalent inductance (in nH) and the equivalent impedance of the following circuit at 1 MHz.

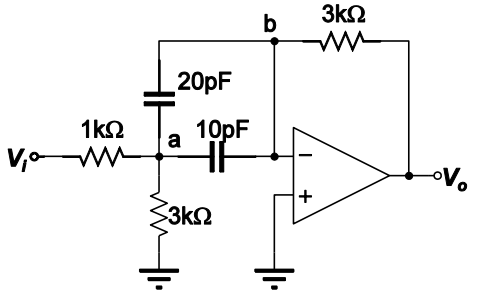


7. Please find the equivalent **impedance** at **1 GHz** for the following circuit.

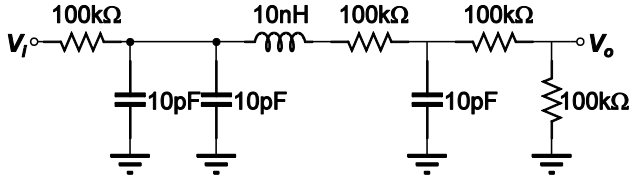


Exercises for Chapter 10

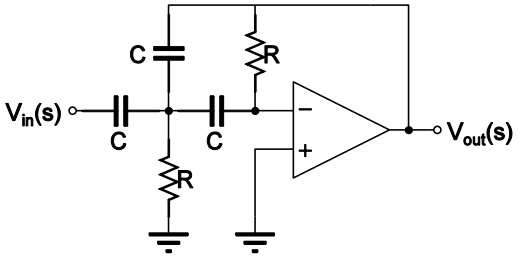
1. Please (a) identify the following filter (type and order) (b) find the transfer function [$H(s)=V_o(s)/V_i(s)$] and (c) cutoff frequency or frequencies.



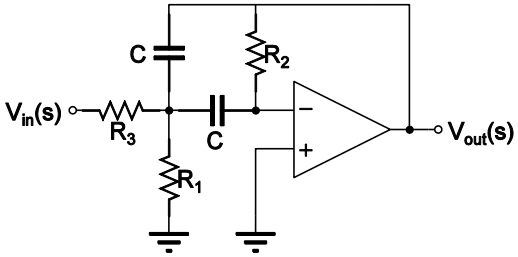
2. Please (a) identify the following filter (type and order) and (b) find the transfer function.



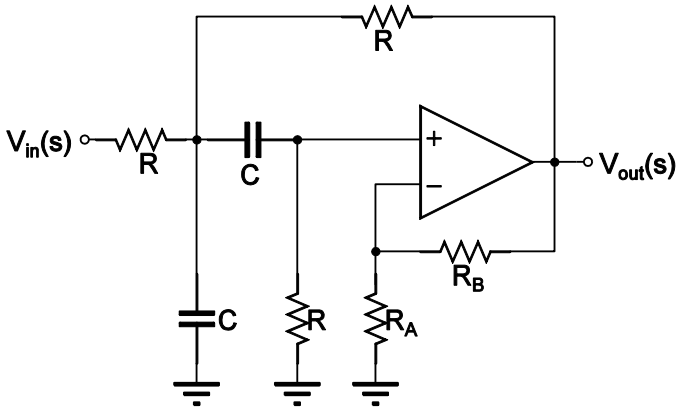
3. Please (a) identify the following filter (type and order), (b) find the transfer function [$H(s)=V_o(s)/V_i(s)$], and (c) find the cut-off frequency or frequencies. [Assume: R=10kΩ and C=10pF]



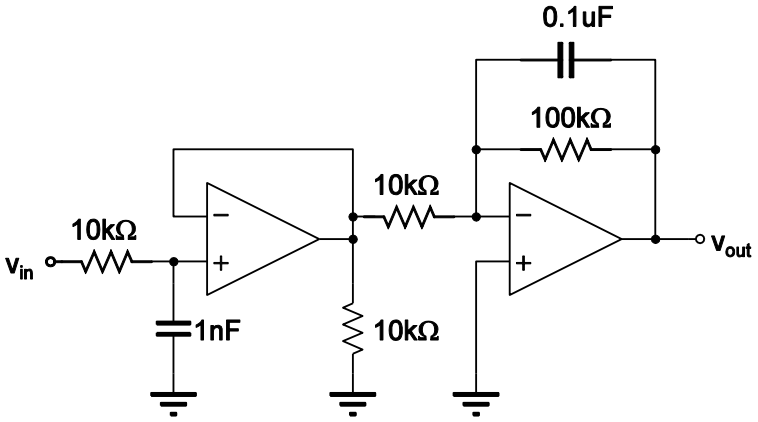
4. Please (a) identify the following filter (type and order), (b) find the transfer function [$H(s)=V_o(s)/V_i(s)$], and (c) find the cut-off frequency or frequencies. [Assume: $R_1=R_2=R_3=10k\Omega$ and C=10pF]



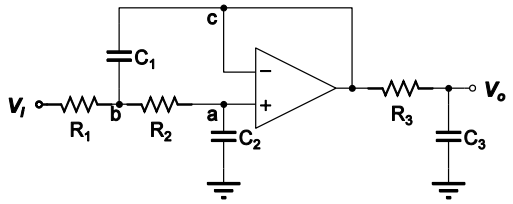
5. The following circuit is a second-order band-pass filter. Please find the following parameters: (a) center frequency, (b) quality factor, (c) bandwidth, and (d) gain. (Hint: find the transfer function first)



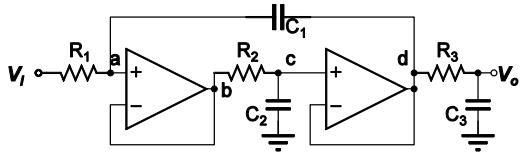
6. Please find the transfer function of the following circuit and sketch the Bode plot (both magnitude and phase versus angular frequency). (Note: Please label properly)



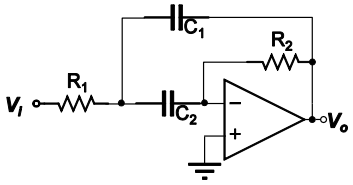
7. For the following circuit, please find the transfer function [$H(s) = \frac{a_1}{s+b_1} \quad \frac{a_2}{s^2+b_2 s+b_3}$].



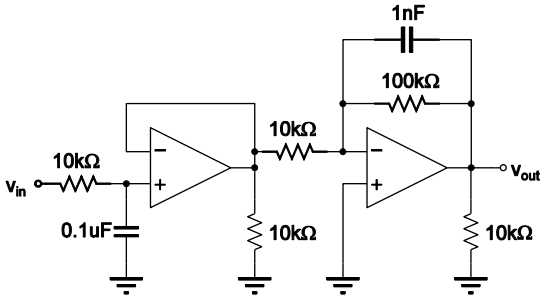
8. Please use the previous circuit to design a third-order butterworth lowpass filter with a cut-off frequency of 1MHz and a DC gain of 1. [Assume R_1=R_2=R_3=1kOhm]
9. For the following circuit, please find the transfer function [$H(s) = \frac{a_1}{s+b_1} \quad \frac{a_2}{s^2+b_2 s+b_3}$].



10. Please use the previous circuit to design a third-order butterworth lowpass filter with a cut-off frequency of 2MHz and a DC gain of 1. [Assume R_1=R_2=R_3=1kOhm]
11. For the following second-order bandpass filter circuit, please find the transfer function [$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{a_0 s}{s^2+b_0 s+b_1}$].

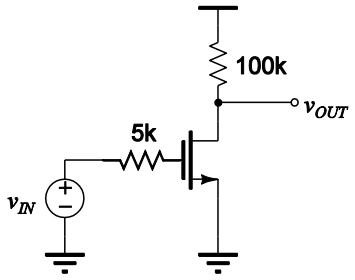


12. For the previous circuit, assume C_1=C_2=10nF, the bandwidth of the filter is 50kHz and the center frequency is 1MHz. Please find R_1, R_2 and $|H_{max}|$.
13. Please find the <u>transfer function</u> [$H(s) = \frac{v_{out}}{v_{in}} = \frac{A_0}{(1+s/\omega_1)(1+s/\omega_2)}$] of the following circuit and sketch the <u>Bode plot</u> (both magnitude in dB and phase in degrees versus angular frequency).

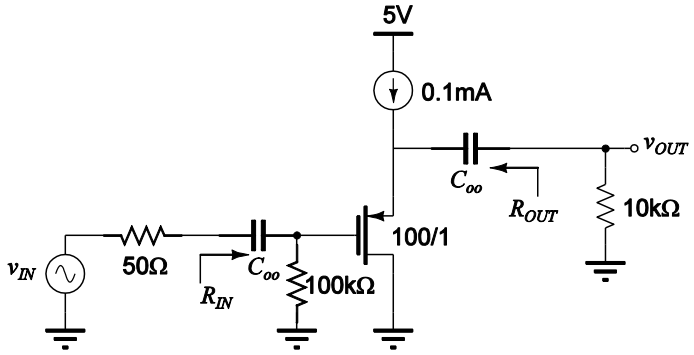


Exercises for Chapter 11

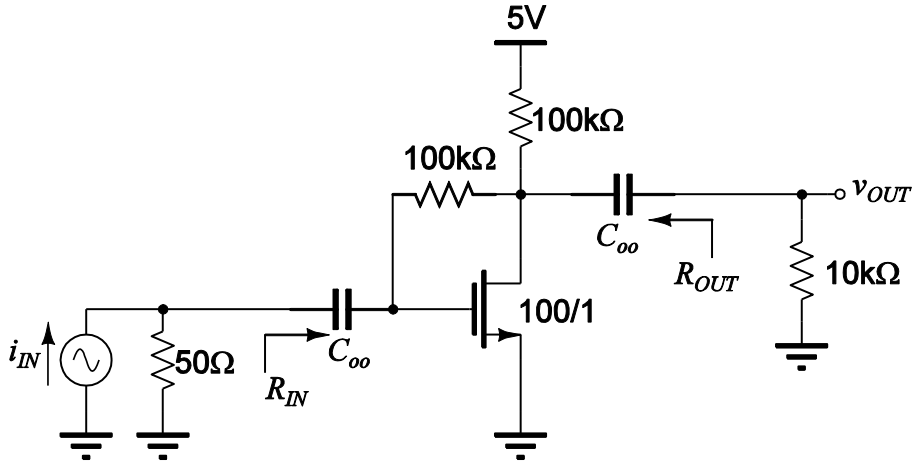
1. For the following amplifier circuit, find the location of the two poles using Miller's theorem assuming the transistor has W=100μm, L=1μm, L_{ov}=0.1μm and the transistor is biased in the saturation region at 100μA. [V_A=50V, $\mu_n C_{ox}$=120μA/V^2, the electron mobility is 400cm^2/V·s]



2. For the following amplifier circuit, Please (a) find the DC operating point of the transistor ($|I_{DS}|$ & $|V_{GS}|$, neglect λ for DC), (b) calculate the small signal parameters (g_m & r_o) and plot the small-signal equivalent circuit, (c) find the small-signal gain (v_{OUT}/v_{IN}), R_{IN}, and R_{OUT}.[$\mu_o C_{ox}$ = 1 mA/V^2, λ = 0.05 V^{-1}, and V_{tn} = -V_{tp} = 1V]



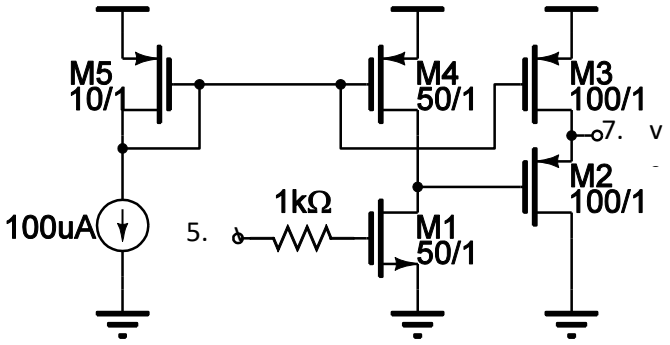
3. For the following trans-resistance amplifier circuit, Please
   (a) (10%) find the DC operating point of the transistor (I_{DS} & V_{GS}, neglect λ for DC),
   (b) (20%) sketch the small signal equivalent circuit,
   (c) (10%) find the small-signal gain (v_{OUT}/i_{IN}),
   (d) (10%) fint the input resistance R_{IN},
   (e) (10%) find the output resistance R_{OUT}.
   [note: i_{IN} is a small-signal current source, $\mu_n C_{ox}$=120μA/V^2, V_{tn}=0.5V, and λ_n= 0.02V^{-1}]



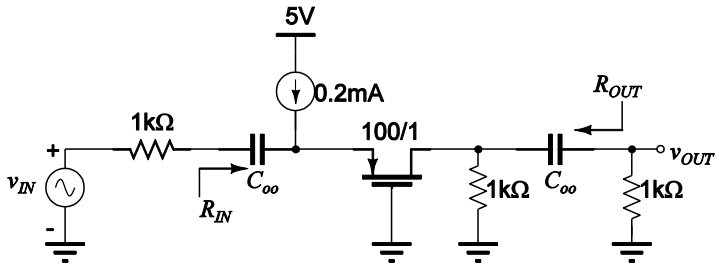
4. Please find
   (a) the DC voltage of v_{IN} (neglect channel length modulation effect for DC)
   (b) the small-signal voltage gain of the following circuit (v_{out}/v_{in})
   (c) the output resistance

(d) the minimum supply voltage required for the following circuit such that all transistors operate in the saturation region.
(e) the total power consumption

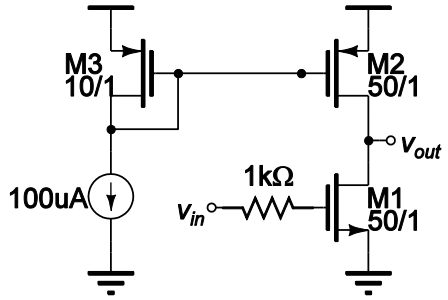
[$\mu_n C_{ox}$=120μA/V^2, $\mu_p C_{ox}$=50μA/V^2, V_{tn}= -V_{tp}=0.7V, and λ_n=λ_p=0.05V^{-1}]



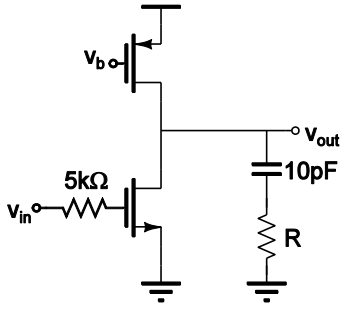
5. For the following circuit, Please (a) find the DC operating point of the transistor (I_{DS} & V_{GS}), (b) find the transconductance (g_m) and plot the small-signal equivalent circuit, (c) find the small-signal gain (v_{OUT}/v_{IN}), R_{IN}, and R_{OUT}. [assume λ = 0]



6. Please find for the following circuit (a) the bias currents I_1, I_2, and I_3 (neglect λ for DC) (b) the small-signal voltage gain (v_{out}/v_{in}), and (c) the output resistance. Assume that all transistors operate in the saturation region. [$\mu_n C_{ox}$=120μA/V^2, $\mu_p C_{ox}$=50μA/V^2, V_{tn}= -V_{tp}=0.7V, and λ_n=λ_p=0.05V^{-1}] (25%)

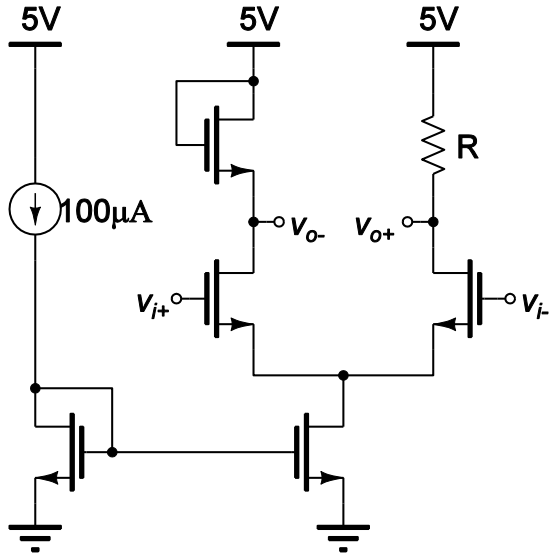


7. (a) Please find the small-signal transfer function of the following circuit assuming Cgs of the NMOS is 1 pF and R=0.
(b) If R is not zero, a LHP zero is created. Please find R such that the pole created by Cgs is cancelled.
[$\mu_n C_{ox}(W_n/L_n)$=12 mA/V^2, $\mu_p C_{ox}(W_p/L_p)$=10 mA/V^2, V_{tn}= - V_{tp} =0.7 V, I_D=0.3 mA, λ_n=0.05 V^{-1}, and λ_p=0.04 V^{-1}]

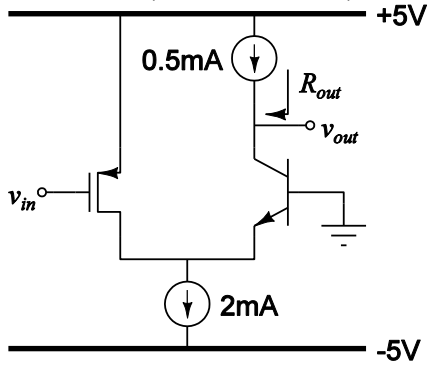


8. Assume $\mu_n C_{ox}$W/L=1600μA/V^2 , V_T=0.5V, and λ=0.01(neglect λ for (a)~(c)) for all transistors in the following circuit. Please find:

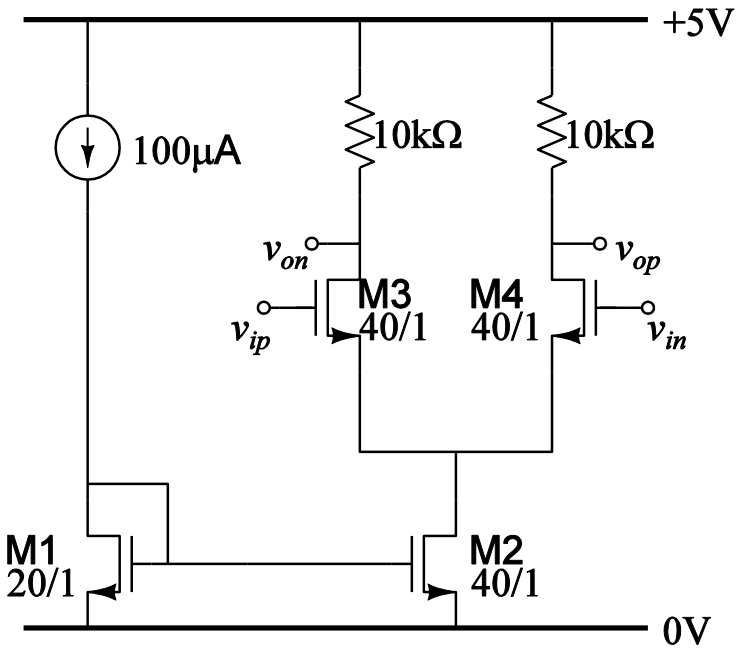
(a)The value of R such that the output voltage (v_{o+}-v_{o-}) has zero DC offset
(b)The input common-mode range (ICMR)
(c)The small-signal differential gain [Hint: find gain of two differential half circuits]
(d)The common-mode rejection ratio (CMRR)



9. Please find the small-signal voltage gain (v_{out}/v_{in}) and output resistance (R_{out}) for the following circuit. [assume W/L=15/1, $\mu_p C_{ox}$=50μA/V^2, V_{tp} = -0.5V, λ=0.05V^{-1} for the PMOS transistor and $|V_A|$=50V, β=50 for the NPN transistor]

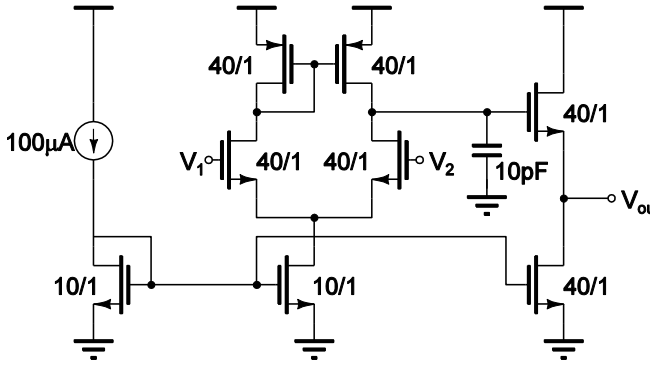


10. For the following circuit, assume $\mu_n C_{ox}$ = 100 μA/V^2 and V_t = 0.7 V for all NMOS transistors.
(a)Find the bias currents for M1, M2, and M3. (Please neglect body effect and channel length modulation effect. All transistors are assumed to be in saturation.)
(b)Find the gain of the amplifier, where the gain is defined as A_v=(v_{op}-v_{on})/(v_{ip}-v_{in}). (Please neglect body effect and channel length modulation effect. All transistors are assumed to be in saturation.)
(c)Will the gain increase, decrease, or stay the same if channel length modulation effect is considered in M3 and M4? (All transistors are assumed to be in saturation.)
(d)Will the gain increase, decrease, or stay the same if channel length modulation effect is considered in M1 and M2? (Assume the transistors are biased such that the V_{DS} of M2 is 2V.)

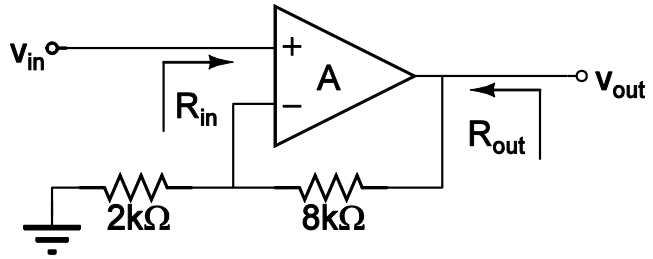

+5V
100μA
10kΩ
10kΩ
v_{on}
v_{op}
M3
40/1
M4
40/1
v_{ip}
v_{in}
M1
20/1
M2
40/1
0V

Exercises for Chapters 12 & 13

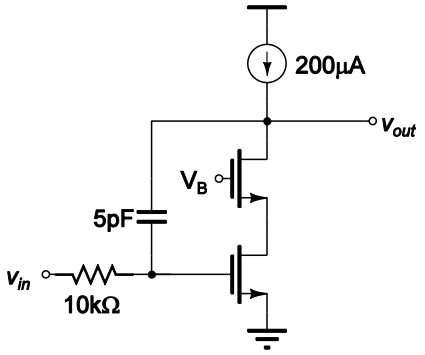
1. For the following circuit, please (a) identify the non-inverting input node (V_1 or V_2), (b) gain, (c) ICMR, and (d) the bandwidth of the amplifier. [V_{DD}=5V, $\mu_n C_{ox}$=120μA/V^2, $\mu_p C_{ox}$=50μA/V^2, V_{tn}= - V_{tp} =0.7V, and λ=0.02. Please assume all transistors are biased correctly in the saturation region.]



2. For the following feedback amplifier, what are the input resistance (**R_{in}**) and output resistance (**R_{out}**) if the voltage gain of A is 500, the input resistance and output resistance of A are 50 kΩ and 1 kΩ, respectively?

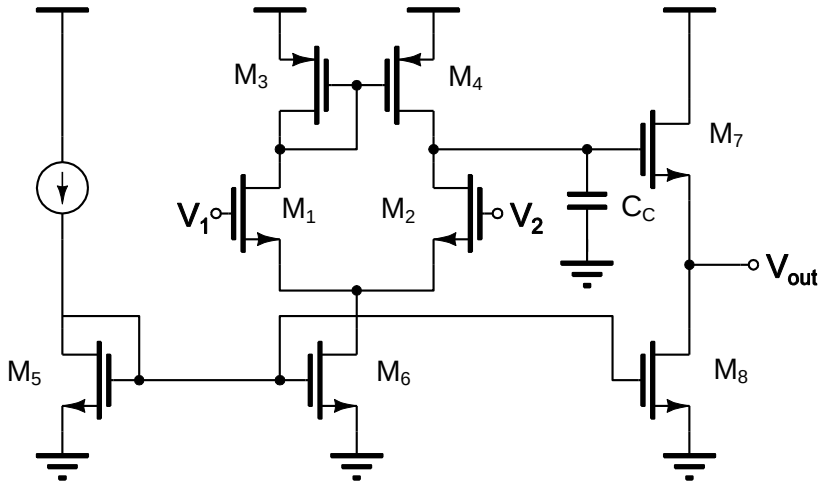


3. Please find the small-signal transfer function (***v_{out}*(s)/*v_{in}*(s)**) of the lower-left circuit using Miller's method. [assume both transistors are in saturation, neglect capacitance within transistors, $\mu_n C_{ox}(W_n/L_n)$=12mA/V^2, V_{tn}=0.7V, λ_n=0.05V^{-1}]

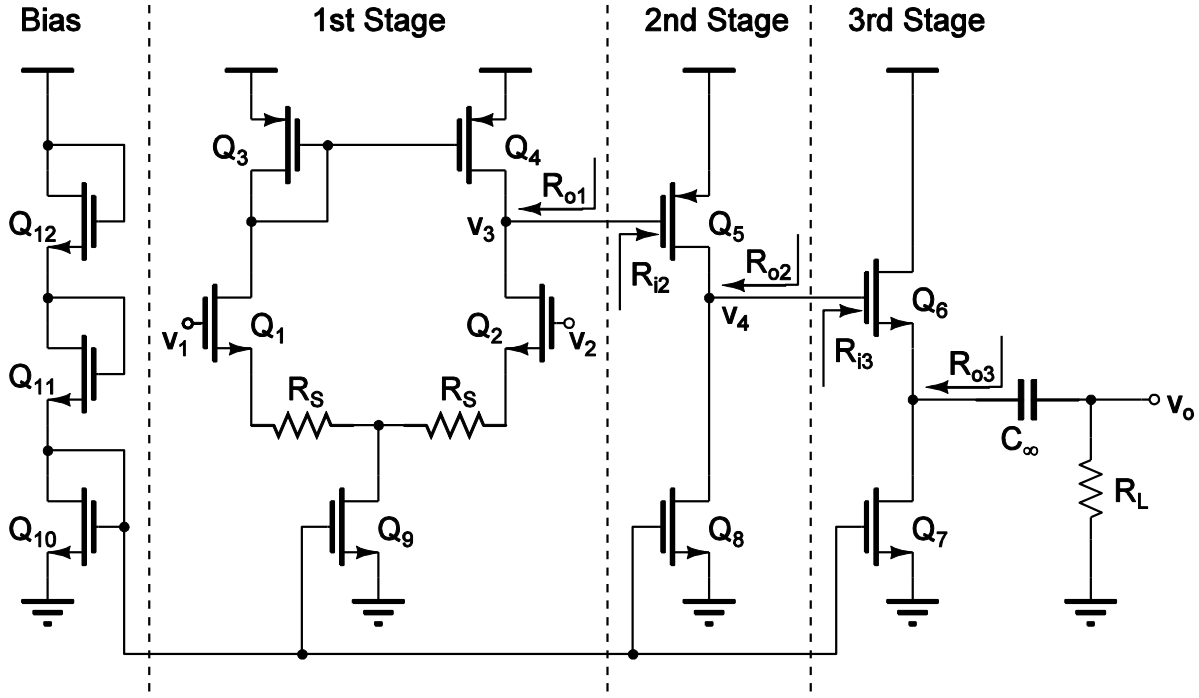


4. An amplifier has a low-frequency gain of 80 dB and three poles at 1 kHz, 1 MHz, and 100 MHz, respectively. (a) Please plot the Bode plot of the amplifier (both gain and phase) (b) find the phase margin of the amplifier (c) find β such that the closed-loop amplifier has a phase margin of 45º.

5. For the following circuit, please (a) identify the non-inverting input node for the following circuit (V_1 or V_2), (b) find the gain of the two-stage OP Amp, (c) find the input common mode range of the amplifier, (d) the dominant pole of the amplifier. [Please write your answers of (b), (c), and (d) in terms of C_C, V_{DD}, V_{ovx}, g_{mx}, r_{ox}, V_{tn}, and V_{tp}, where x is the transistor number. Please assume all transistors are biased correctly in the saturation region.]



6.



Assume: $\mu_n C_{ox}=100\mu A/V^2$, $\mu_p C_{ox}=50\mu A/V^2$, $V_{tn}= - V_{tp} =0.7V$, $|V_A|=50V$, $V_{DD}=3.3V$, $I_{10}=0.5I_9=0.25I_8=0.125I_7=200\mu A$, $W_1/L_1=W_2/L_2=100$, $W_3/L_3=W_4/L_4=50$, $W_5/L_5=100$, $W_6/L_6=225$, and $R_L= R_S=1kOhm$.

(a) Find the non-inverting input terminal of this three-stage amplifier. (v_1 or v_2)

(b) Find the W/L ratios for Q_7~Q_{10} while neglecting channel length modulation effect for DC calculations and assuming Q_{10}~Q_{12} have the same dimensions.

(c) Find the differential-mode output resistance of the 1st stage (R_{o1}).

(d) Find the differential-mode gain of the 1st stage $|v_3/v_{id}|$, where $v_{id}= (v_2-v_1)$.

(e) Find the common-mode gain of the 1st stage $|v_3/v_{cm}|$, where $v_{cm}=(v_2+v_1)/2$.

(f) Find the ICMR of the 1st stage of the amplifier.

(g) What topology is the 2nd stage of this amplifier? (CS, CG, CD…….)

(h) Find the gain (v_4/v_3), input resistance (R_{i2}), and output resistance (R_{o2}) of the 2nd stage.

(i) What topology is the 3rd stage of this amplifier? (CS, CG, CD…….)

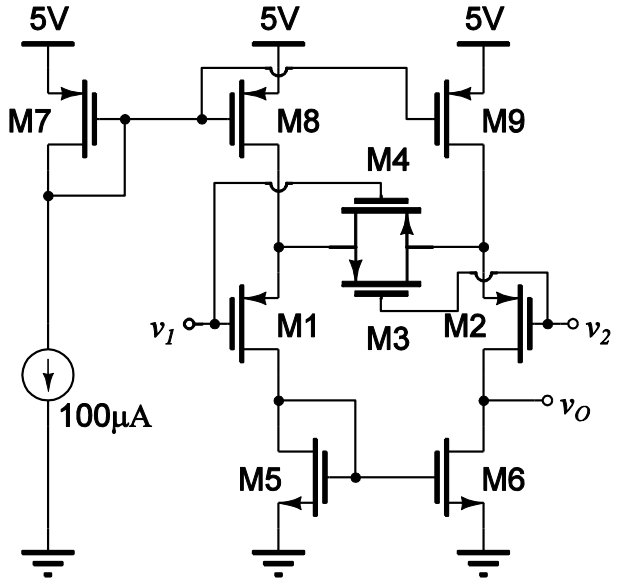
(j) Find the gain (v_o/v_4), input resistance (R_{i3}), and output resistance (R_{o3}) of the 3rd stage.

7. For the following circuit, please

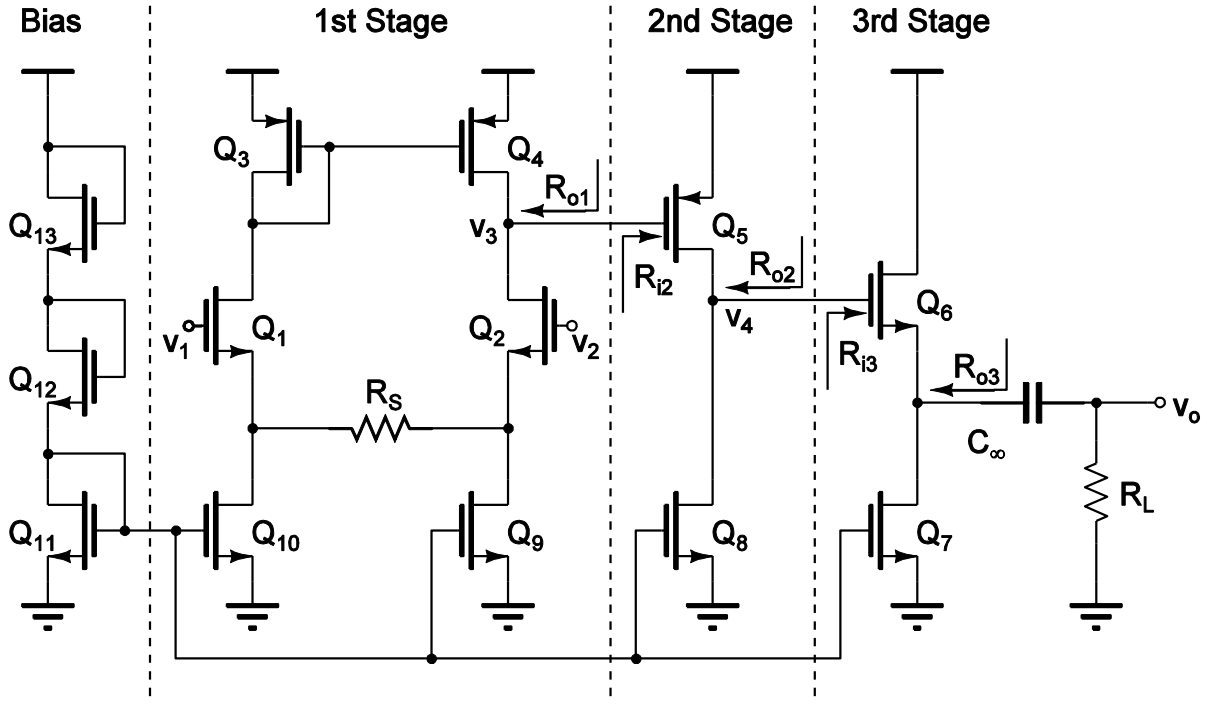
(a) identify the non-inverting input node for the following circuit (v_1 or v_2),

(b) find the equivalent resistance R_{eq} of M3 and M4 combined (neglect λ for DC calculations),

(c) sketch the differential-mode small-signal equivalent circuit assuming M8 as r_{o8}, M9 as r_{o9}, M3 and M4 as a single resistor R_{eq},
(d) find the differential-mode gain of the amplifier,
(e) find the differential-mode output resistance of the amplifier,
(f) find the input common mode range of the amplifier.
[$\mu_n C_{ox}$=120μA/V^2, $\mu_p C_{ox}$=50μA/V^2, V_{tn}= - V_{tp} =0.7V, and λ=0.02. Please assume all transistors are biased correctly in the saturation region and W/L is 100 for all transistors.]



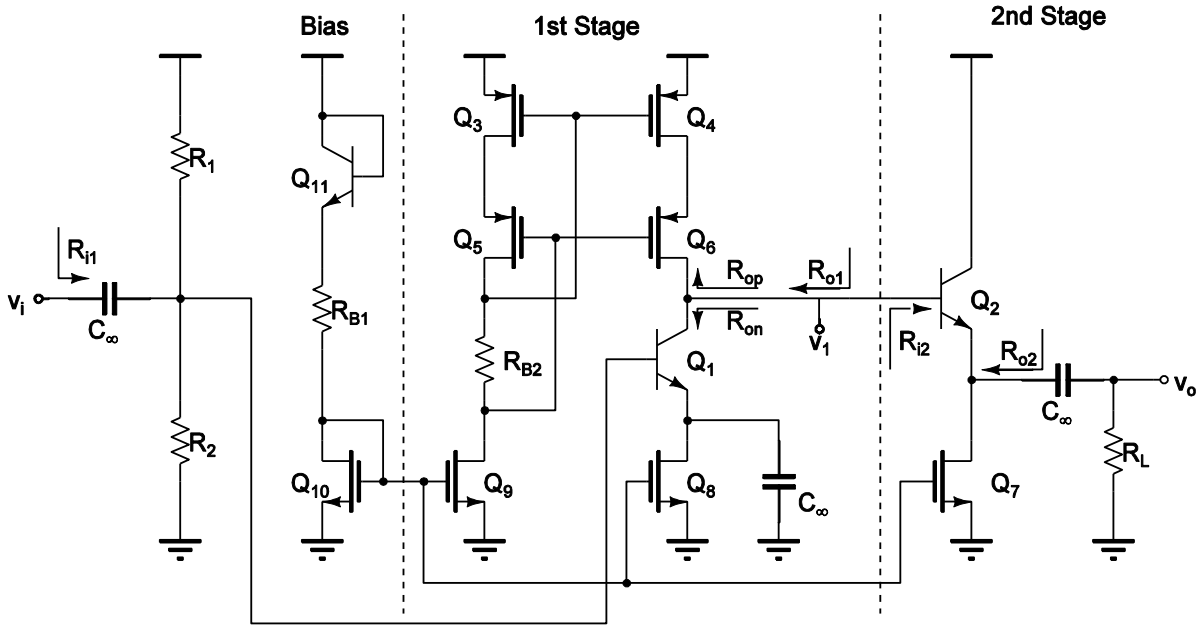
8.



Assume: $\mu_n C_{ox}$=100μA/V^2, $\mu_p C_{ox}$=50μA/V^2, V_{tn}= - V_{tp} =0.7V, $|V_A|$=50V, V_{DD}=3.3V, I_{11}=0.5I_{10}=0.5I_9=0.25I_8=0.125I_7=100μA, W_1/L_1=W_2/L_2=100, W_3/L_3=W_4/L_4=50, W_5/L_5=100, W_6/L_6=225, and R_L= R_S=10kOhm.
(a) Find the non-inverting input terminal of this three-stage amplifier. (v_1 or v_2)
(b) Find the W/L ratios for Q_7~Q_{11} while neglecting channel length modulation effect for DC calculations and assuming Q_{11}~Q_{13} have the same dimensions.
(c) Find the output resistance of the 1st stage (R_{o1}).
(d) Find the gain of the 1st stage $|v_3/(v_2-v_1)|$.
(e) Find the ICMR of the 1st stage of the amplifier.

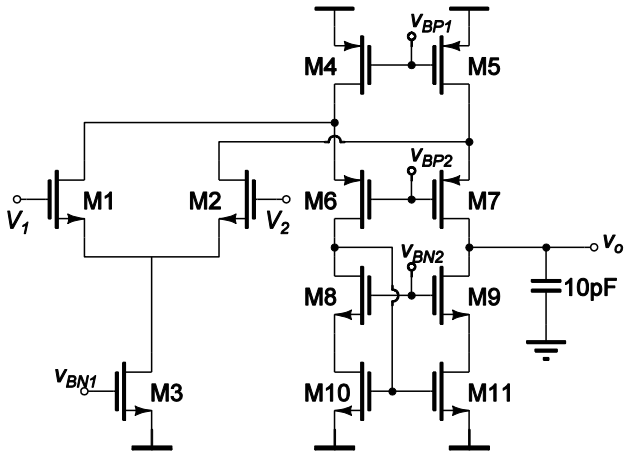
(f) What topology is the 2nd stage of this amplifier? (CS, CG, CD…….)
(g) Find the gain (v_4/v_3), input resistance (R_{i2}), and output resistance (R_{o2}) of the 2nd stage using **small-signal analysis**. (you have to sketch the small signal equivalent circuit and solve with KCL/KVL)
(h) What topology is the 3rd stage of this amplifier? (CS, CG, CD…….)
(i) Find the gain (v_o/v_4), input resistance (R_{i3}), and output resistance (R_{o3}) of the 3rd stage.

9.

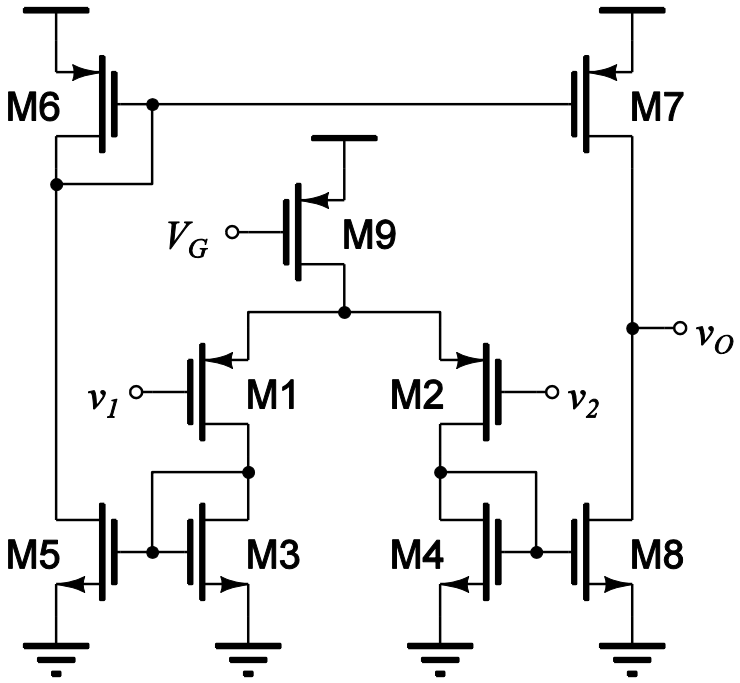


Assume: $\mu_n C_{ox}=100\mu A/V^2$, $\mu_p C_{ox}=50\mu A/V^2$, $V_{tn}= - V_{tp} =0.8V$, $|V_A|=50V$ for MOSFETs, $\beta=200$, $|V_A|=50V$, and $|V_{CE,sat}|=0.3V$ for BJTs, $I_{10}=0.25I_9=0.25I_8=0.125I_7=100\mu A$, $W_3/L_3=W_4/L_4= W_5/L_5=W_6/L_6=100$, $V_{DD}=5V$, $R_2=3kOhm$, and $R_L= R_{B1}=30kOhm$.
(a) Find the W/L ratios for Q_7~Q_{10} while neglecting channel length modulation effect for DC calculations.
(b) Find the maximum value of R_1 such that Q_8 remains in saturation.
(c) Find the value of R_{B2} such that the output of the 1st stage (v_1) has the maximum signal swing. What is the maximum signal swing of v_1 ($v_{1,max}$-$v_{1,min}$)?
(d) Find the output resistance (R_{op}) of the active load made of Q_7~Q_{10}.
(e) Find the gain (v_o/v_1), input resistance (R_{i2}), and output resistance (R_{o2}) of the 2nd stage using **small-signal analysis**. (Sketch the small signal equivalent circuit first. R_{o1} can be considered as an open circuit here).
(f) Find the gain (v_1/v_i), input resistance (R_{i1}), and output resistance (R_{o1}) of the 1st stage using **small-signal analysis.** (Use the equivalent resistances R_{op} and R_{i2}. You should only have one transistor in your small-signal equivalent circuit.)

10. For the following circuit, please
(a) identify the non-inverting input node for the following circuit (V_1 or V_2),
(b) find V_{BN1} and V_{BP1} such that I_3=200uA and I_4=I_5=250uA
(c) find the input common mode range of the amplifier,
(d) find V_{BP2} and V_{BN2} such that the output voltage range can be maximized, and
(e) plot the Bode plot (both gain and phase).
[V_{DD}=+5V, V_{SS}=-5V, $\mu_n C_{ox}=100\mu A/V^2$, $\mu_p C_{ox}=50\mu A/V^2$, $V_{tn}= -V_{tp} =0.5V$, and $\lambda=0.05$. Please assume all transistors are biased correctly in the saturation region and all have ratios of 16/1.]



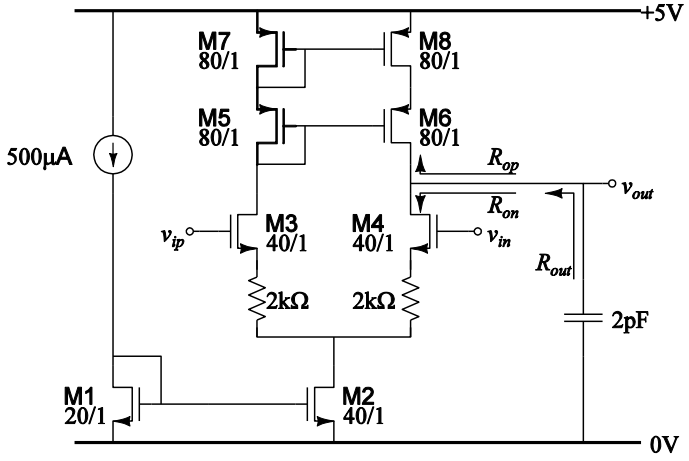
11. Assume $\mu_n C_{ox}$=120 μA/V^2, $\mu_p C_{ox}$=50 μA/V^2, V_{tn}= -V_{tp}=0.7 V, λ_n=λ_p=0.05 V^{-1}, and a supply voltage of 5 V. The transistor sizes (W/L) are all 10 μm/1 μm, and the quiescent current is 40 uA for the following CMOS operational amplifier (OPA).



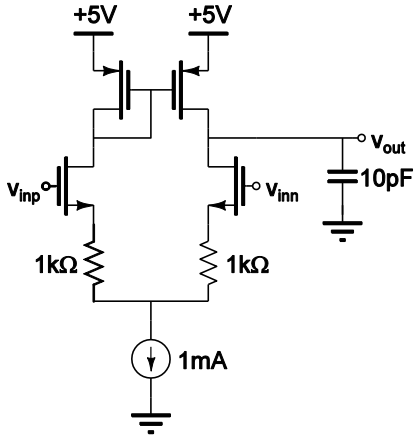
(a)What is the non-inverting input of the OPA? (v_1 or v_2)
(b)What is the bias voltage V_G? (Please neglect channel length modulation effect.)
(c)What is the input resistance of the OPA?
(d)What is the output resistance of the OPA?
(e)What is the small-signal gain of the OPA ($v_o/|v_1-v_2|$)?
(f)What is the slew rate if the OPA has a load capacitance of 10 pF at v_O?
(g)What is the maximum input common-mode voltage ($V_{CM\max}$) of the OPA?
(h)What is the minimum input common-mode voltage ($V_{CM\min}$) of the OPA?
(i)What is the unity gain bandwidth of the OPA if the load capacitance is 10 pF at v_O?
(j)What is the total power dissipation of the OPA when the output voltage (v_O) is 2.5 V and the load is a 10 pF capacitance.

12. For the following amplifier:
(a) Find the slew rate of the amplifier.
(b) Find the output resistances R_{op}, R_{on}, and R_{out}.
(c) Find the small-signal voltage gain ($v_{out}/(v_{ip}-v_{in})$)

[Please ignore channel length modulation effect when calculating bias currents, assume all transistors are biased correctly in the saturation region, and assume $\mu_n C_{ox}$=100μA/V^2, $\mu_p C_{ox}$=50μA/V^2, V_{tn}= -V_{tp} =0.5V, and λ=0.05V^{-1}]



13. Please find the unity-gain bandwidth for the following amplifier. [$\mu_n C_{ox}$=100μA/V^2, $\mu_p C_{ox}$=50μA/V^2, V_{tn}= -V_{tp} =0.5V, and λ=0.05V^{-1}. Please assume all transistors are biased correctly in the saturation region and all have ratios of 10/1.]



14. For the lower-left source-degenerated differential amplifier, all transistors have W/L of 100/1, $\mu_n C_{ox} = 120\ \mu\text{A/V}^2$, $V_{tn} = 0.7$ V, and $\lambda_n = 0.04\ \text{V}^{-1}$. Please find
(a) the equivalent resistance R_{eq} of M3 and M4 in parallel (hint: M3&M4 are in the triode region),
(b) the differential small-signal gain ($A_d = v_{od}/v_{id}$) if M1&M2 are in the saturation region,
(c) the power dissipation P_{diss} if the amplifier has a supply voltage of 5V,
(d) the input common-mode range (ICMR).
(Hint: the lower-right circuit is the equivalent circuit of the lower-left one)