Junior Design

555 Timer

Design Improvements

Samuel Dickerson, Ph.D.

ECE Department

University of Pittsburgh

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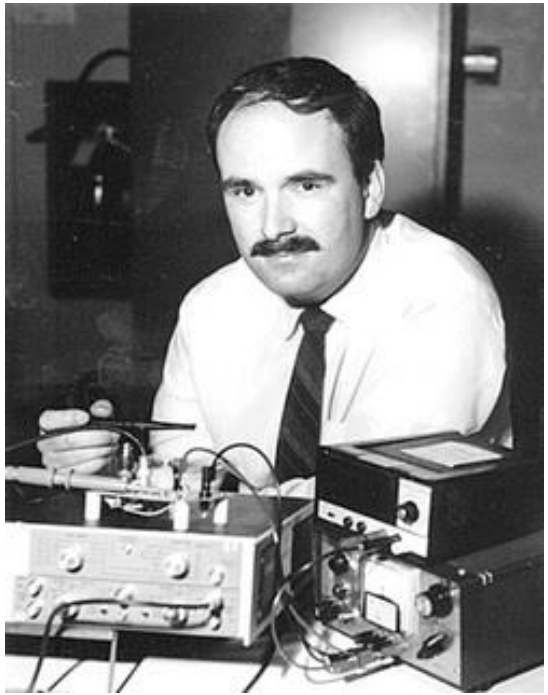
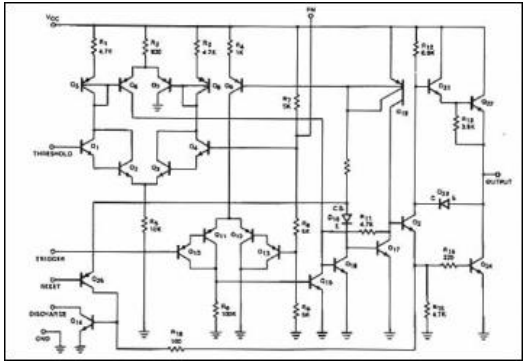
555 Timer Reflection
Hans Camenzind



Any final comments on why the 555 design has been so resilient for so long?



http://www.semiconductormuseum.com/Transistors/LectureHall/Camenzind/Camenzind_Index.htm

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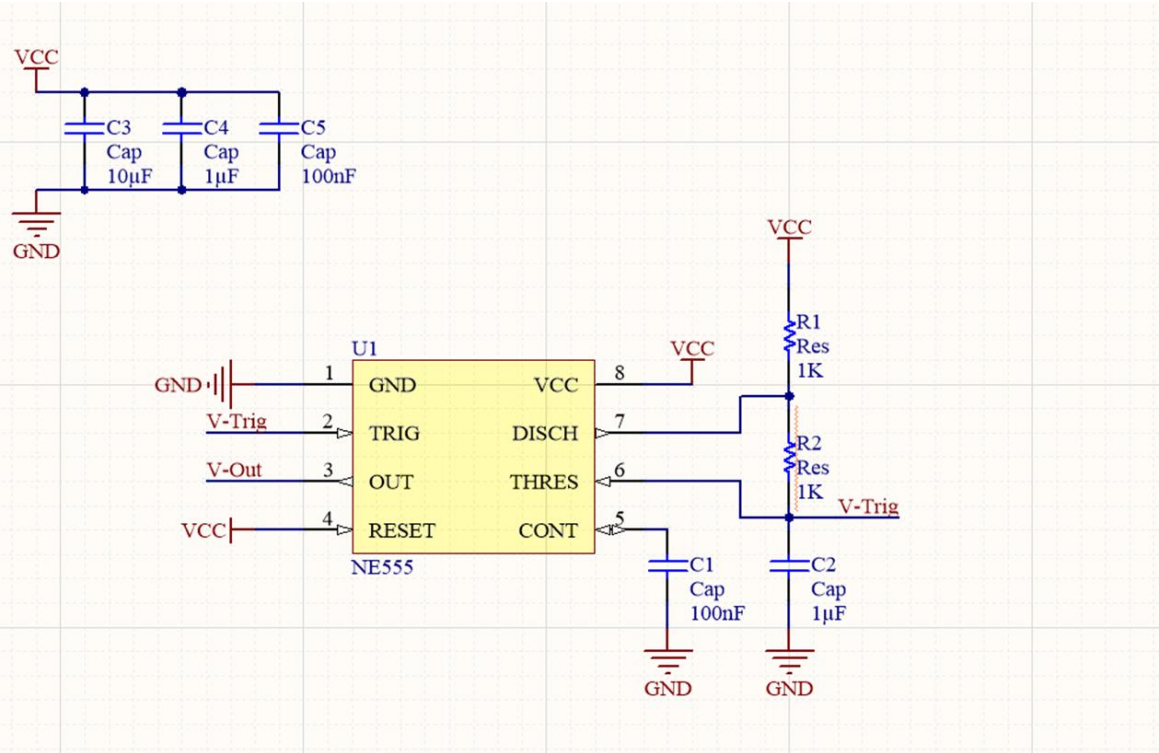
555 Timer Lessons

- A “perfect” design is not possible
- A “perfect” design is also not always necessary
- Always room for improvements and design iterations

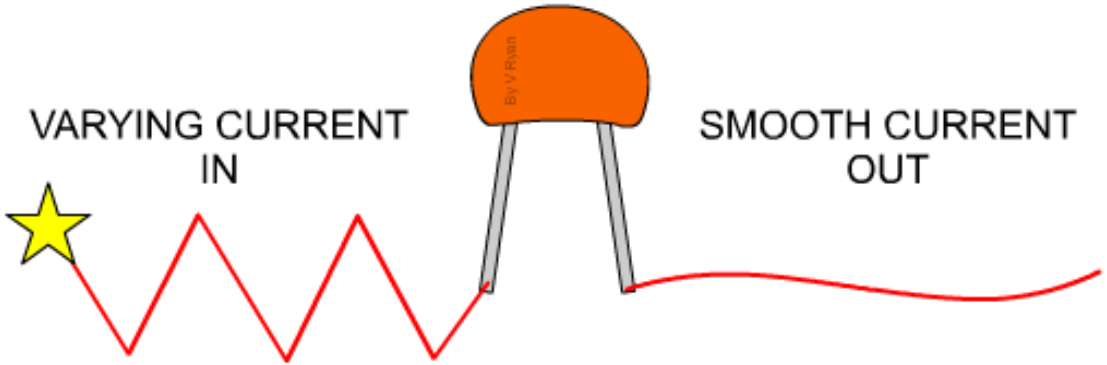
Is there anything you would like to redo with your 555 timer design?

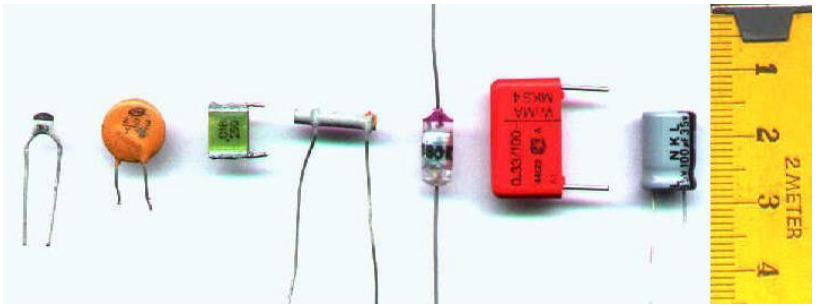
555 Timer Design Reflection



Design courtesy of Nicholas Franconi

Decoupling Capacitors





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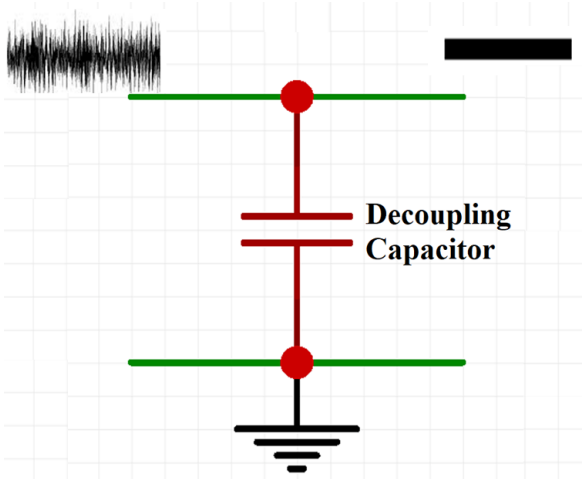
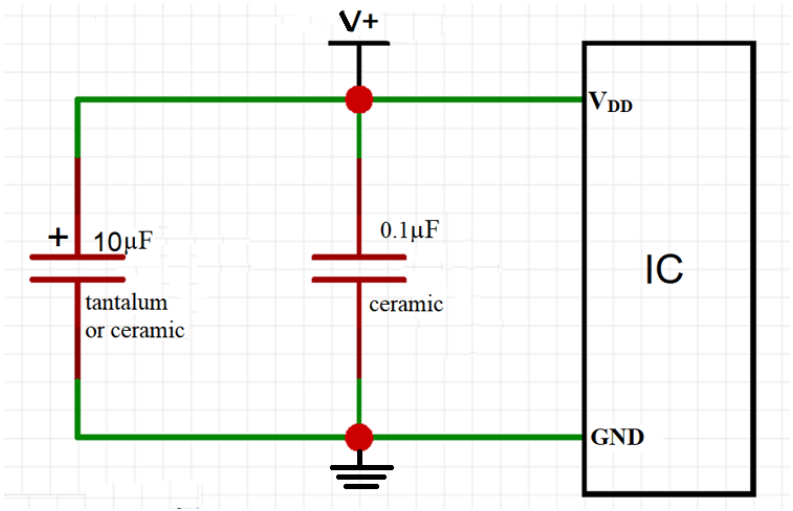
http://www.autodesk.com/products/eagle/blog/everything-need-know-capacitors
https://en.wikipedia.org/wiki/Capacitor

Decoupling Capacitors

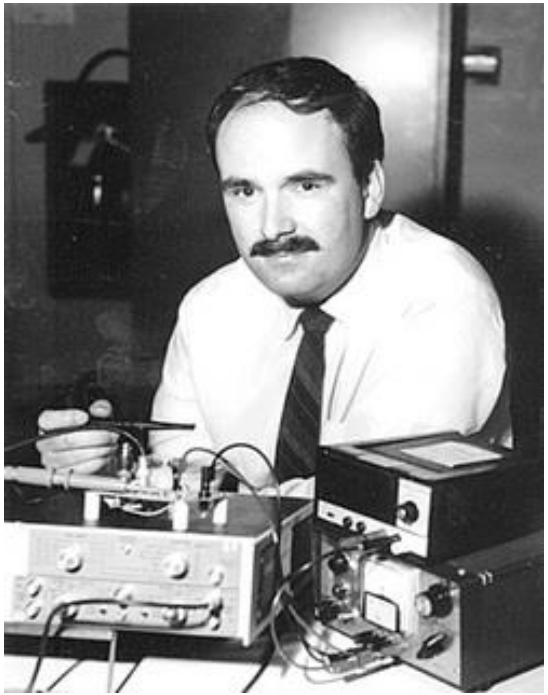




- **Large capacitor placed away from IC to smooth out low frequency changes**
- **Small capacitors placed closer to the IC to smooth high frequency changes**

https://components101.com/articles/decoupling-capacitor-vs-bypass-capacitors-working-and-applications

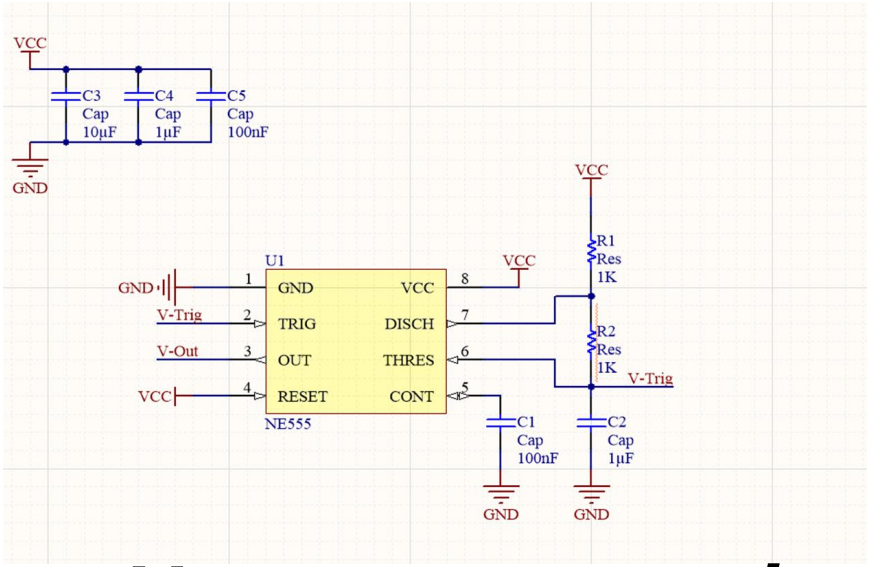
Design Reviews

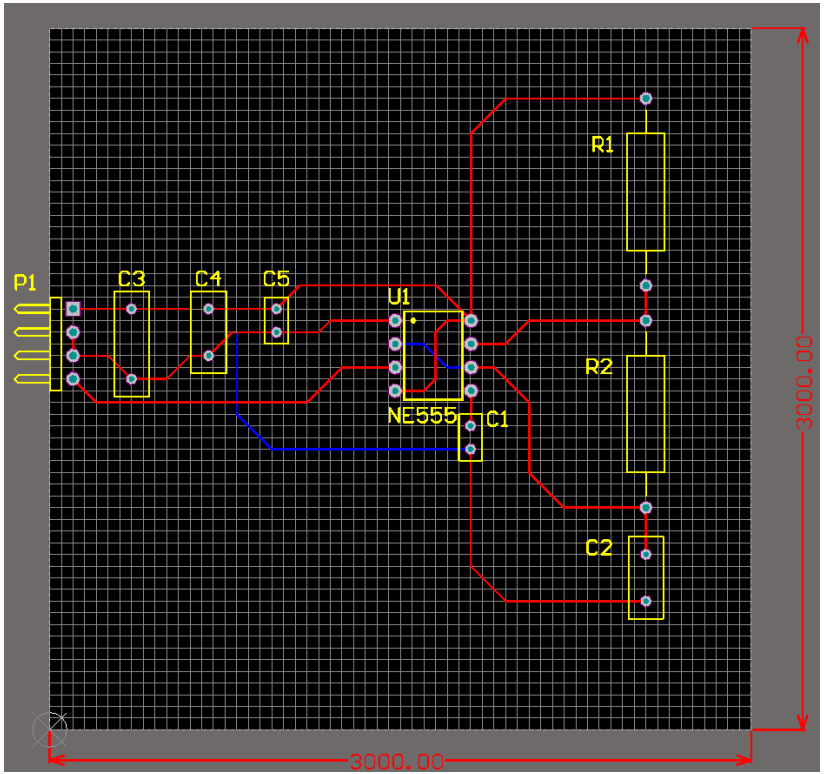


In the IEEE Article, you mentioned that there was a design review at Signetics. Was that a contractual obligation?

No. I just thought it was a good idea. I've always had design reviews for all my designs. Get feedback, bounce off ideas with colleagues. But, just how laborious the design was. First, the breadboarding of the circuit. The one thing you want to do is make sure the circuit works well in production, and in production you have parameter variation - high gain, low gain for transistors, high resistor values, low resistor values, all sorts of combinations.

555 Timer Design Review





How can we make this design better?

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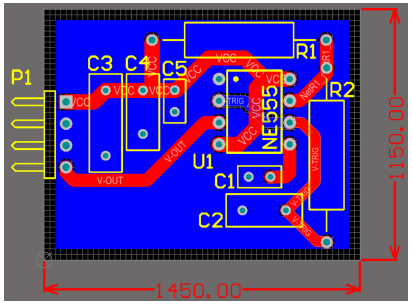
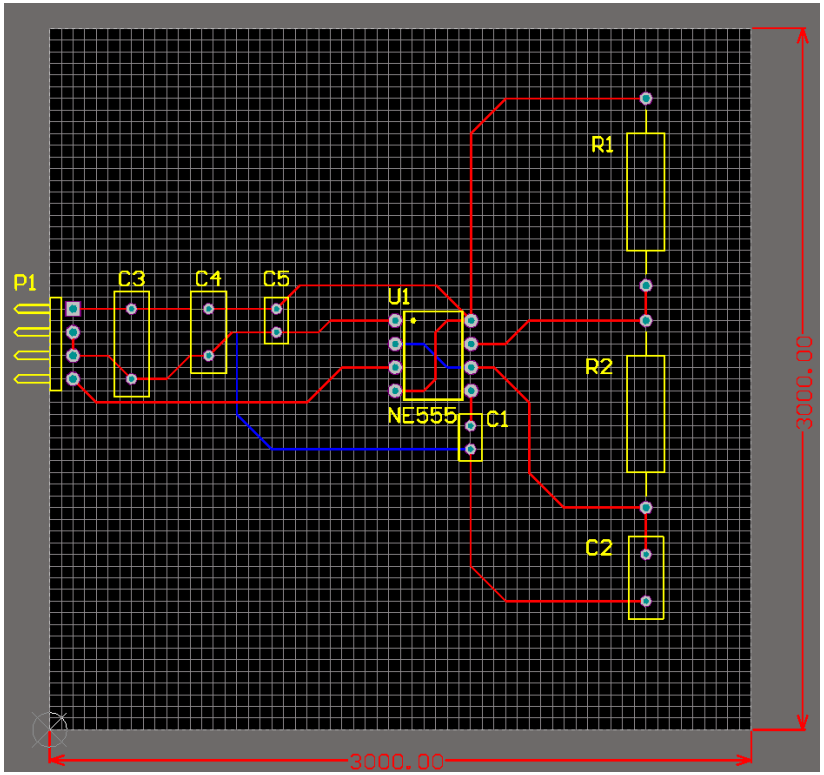
Design courtesy of Nicholas Franconi

555 Timer Design Review



Vs.



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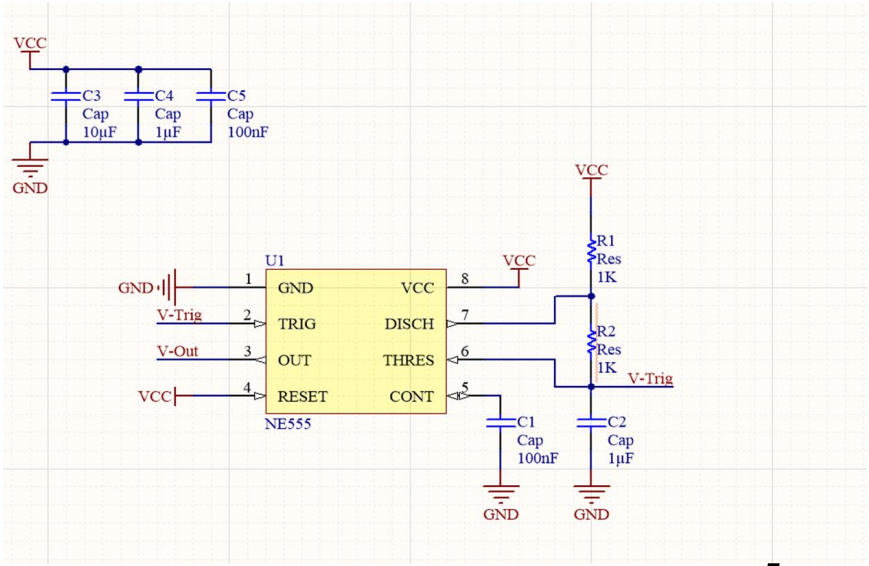

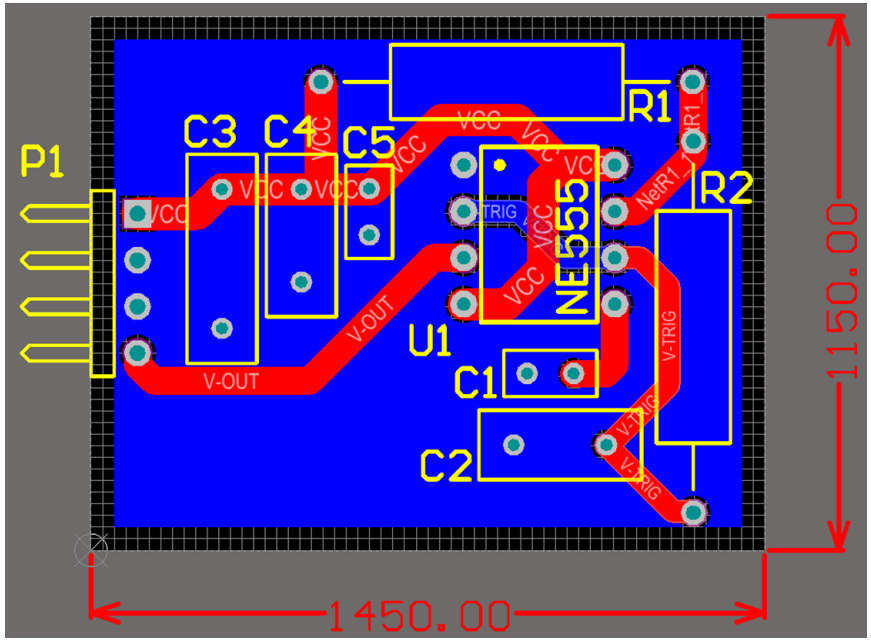

How can we make this design better?

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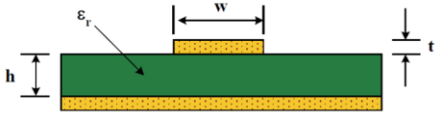
Trace Impedance

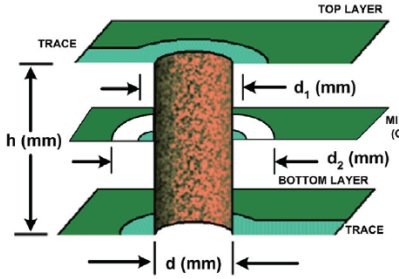


x = length of trace (cm)
w = width of trace (cm)
h = height of trace (cm)
t = thickness of trace (cm)
e_r = PCB Permeability

$$L(nH) \approx 2x \ ln\left(\frac{5.98\ h}{0.8\ w + t}\right)$$

$$C(pF) \approx \frac{0.264x\ (\varepsilon_r + 1.41)}{ln\left(\frac{5.98\ h}{0.8\ w + t}\right)}$$

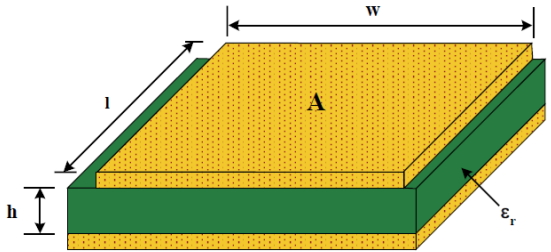
$$Z_0(\Omega) = 31.6\sqrt{\frac{L(nH)}{C(pF)}} \qquad T_p(\ ps/cm\ ) = 31.6\sqrt{L(nH)C(pF)}$$



$$L(nH) \approx \frac{h}{5}\left[1 + ln\left(\frac{4h}{d}\right)\right]$$

$$C(pF) \approx \frac{0.0555\ \varepsilon_r\ h\ d_1}{d_2 - d_1}$$

$$Z_0(\Omega) = 31.6\sqrt{\frac{L(nH)}{C(pF)}} \qquad T_p(\ ps/cm\ ) = 31.6\sqrt{L(nH)C(pF)}$$



$$C(pF) \approx \frac{0.0886\ \varepsilon_r\ A}{h}$$

h = separation between planes (cm)
A = area of common planes = l*w (cm^2)
e_r = PCB Permeability

- Every trace, plane, and via has an associated inductance, capacitance, and resistance
- Impact on PCB depends on both frequency and dimensions

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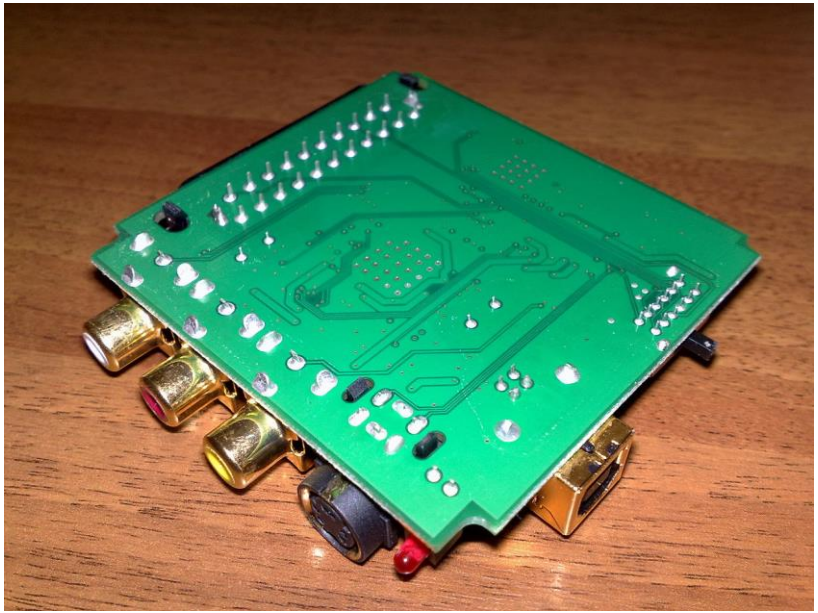
Ground Planes



Light green area is the “ground plane”

PCB’s often contain “Ground Planes”

- **Makes layout easier**
- **Ensure’s ground is consistent**
- **Reduces elective noise / crosstalk and ground loops**

Can we make the design better?

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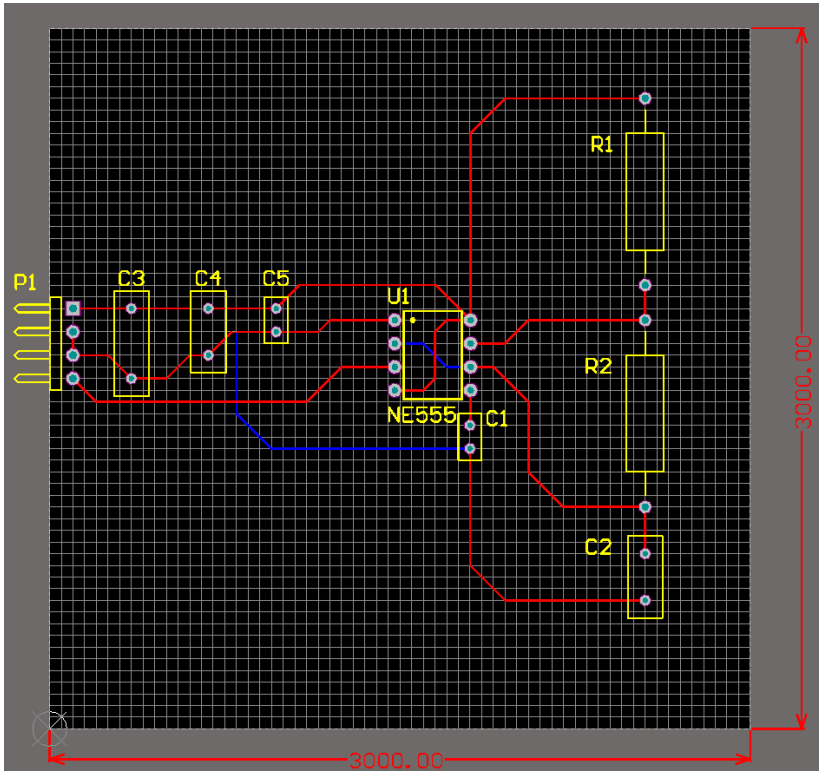
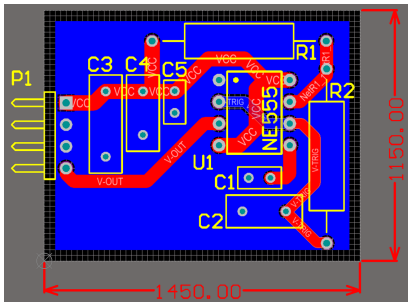


Vs.



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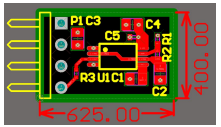

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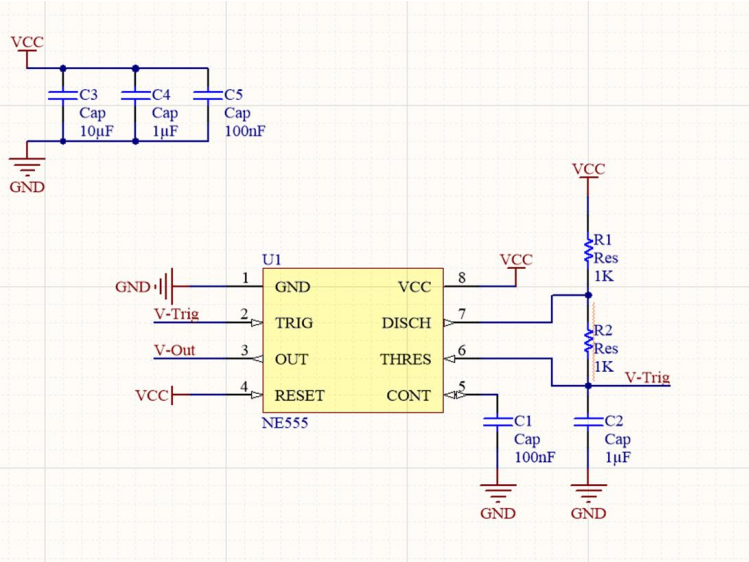

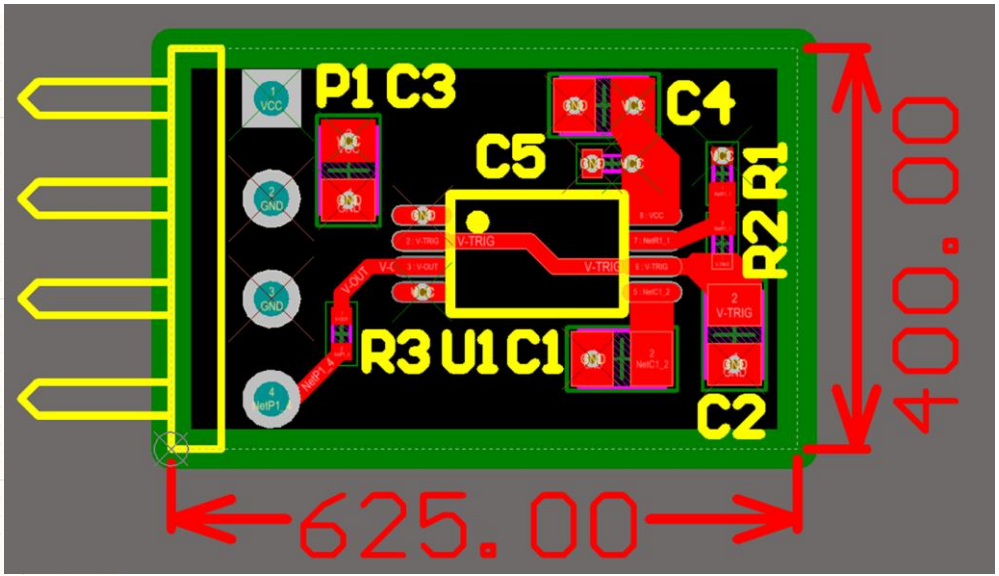

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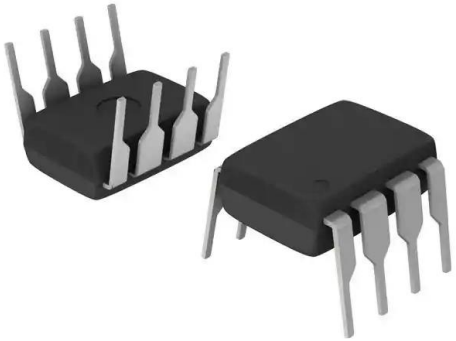
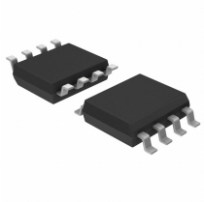
Surface Mount Components



$0.45



$0.36

Current Tasks

1. Review your project proposal

2. Prepare Bill of materials for your design project (Digikey)

3. Start Constructing Schematic

4. Verify your design