Project 2 - Test Case

Parameters:

Set associativity: L1: 4, L2:8

Latency: L1: 1, L2:50, Memory:100

Address is written as this format:

(tag) (L2-L1 index) (L1 index) (offset)

Translate it into binary code by your preferred setting.

Cache Warmup (cycle doesn't matter)

r $(001)_{10}(00)_{10}(00)_{10}(x)_{10}$ 1

r $(002)_{10}(00)_{10}(00)_{10}$ $(x)_{10}$ 2

r $(003)_{10}(00)_{10}(00)_{10}$ $(x)_{10}$ 3

r $(004)_{10}(00)_{10}(00)_{10}$ $(x)_{10}$ 4

r $(005)_{10}(00)_{10}(00)_{10}$ $(x)_{10}$ 5

r $(006)_{10}(00)_{10}(00)_{10}$ $(x)_{10}$ 6

r $(007)_{10}(00)_{10}(00)_{10}$ $(x)_{10}$ 7

r $(008)_{10}(00)_{10}(00)_{10}$ $(x)_{10}$ 8

r $(001)_{10}(00)_{10}(01)_{10}$ $(x)_{10}$ 9

r $(002)_{10}(00)_{10}(01)_{10}$ $(x)_{10}$ 10

r $(003)_{10}(00)_{10}(01)_{10}$ $(x)_{10}$ 11

r $(004)_{10}(00)_{10}(01)_{10}$ $(x)_{10}$ 12

r $(005)_{10}(00)_{10}(01)_{10}$ $(x)_{10}$ 13

r $(006)_{10}(00)_{10}(01)_{10}$ $(x)_{10}$ 14

r $(007)_{10}(00)_{10}(01)_{10}$ $(x)_{10}$ 15

r $(008)_{10}(00)_{10}(01)_{10}$ $(x)_{10}$ 16

r $(001)_{10}(01)_{10}(00)_{10}(x)_{10}$ 17

r $(002)_{10}(01)_{10}(00)_{10}$ $(x)_{10}$ 18

r $(003)_{10}(01)_{10}(00)_{10}$ $(x)_{10}$ 19

r $(004)_{10}(01)_{10}(00)_{10}$ $(x)_{10}$ 20

r $(005)_{10}(01)_{10}(00)_{10}$ $(x)_{10}$ 21

r $(006)_{10}(01)_{10}(00)_{10}$ $(x)_{10}$ 22

r $(007)_{10}(01)_{10}(00)_{10}$ $(x)_{10}$ 23

r $(008)_{10}(01)_{10}(00)_{10}$ $(x)_{10}$ 24

r $(001)_{10}(01)_{10}(01)_{10}$ $(x)_{10}$ 25

r $(002)_{10}(01)_{10}(01)_{10}$ $(x)_{10}$ 26

r $(003)_{10}(01)_{10}(01)_{10}$ $(x)_{10}$ 27

r $(004)_{10}(01)_{10}(01)_{10}$ $(x)_{10}$ 28

r $(005)_{10}(01)_{10}(01)_{10}$ $(x)_{10}$ 29

r $(006)_{10}(01)_{10}(01)_{10}$ $(x)_{10}$ 30

r $(007)_{10}(01)_{10}(01)_{10}$ $(x)_{10}$ 31

r $(008)_{10}(01)_{10}(01)_{10}$ $(x)_{10}$ 32

L1: (5~8) $(01)_{10}$ $(1\sim2)_{10}$, L2: (1~8) $(1\sim2)_{10}$ $(1\sim2)_{10}$

Case 1: Read Test - L1 Miss

Shuffle LRU

r $(007)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10000

r $(005)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10003

r $(008)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10005

r $(006)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10007

Random Read test

r $(003)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10009 Miss

r $(001)_{10}(00)_{10}$ $(01)_{10}(x)_{10}$ 10011 Miss

r $(008)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 11000 Hit

r $(005)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 11003 Miss

r $(004)_{10}(00)_{10}$ $(01)_{10}(x)_{10}$ 11005. Miss

r $(006)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 12000 Miss

Case 2: Read Test - L2 Miss (be careful about cycle)

Shuffle LRU

r $(007)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10000

r $(005)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10003

r $(008)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10005

r $(006)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10007

Random Test

r $(003)_{10}(02)_{10}$ $(01)_{10}(x)_{10}$ 10100 Miss in L2

r $(008)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10105 Hit

r $(010)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 11000 Miss in L2

r $(010)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 11000 Hit

r $(011)_{10}(00)_{10}$ $(01)_{10}(x)_{10}$ 11001. Miss in L2

r $(010)_{10}(02)_{10}$ $(01)_{10}(x)_{10}$ 11003. Miss in L2

r $(004)_{10}(00)_{10}$ $(01)_{10}(x)_{10}$ 12000 Miss in L1

r $(011)_{10}(00)_{10}$ $(01)_{10}(x)_{10}$ 12001 Miss in L1

r $(004)_{10}(00)_{10}$ $(01)_{10}(x)_{10}$ 12003 Hit

Case 3: Write Test, L1 Miss, L2 Hit

Write Hit

w $(007)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10000

r $(005)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10003

w $(008)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10005

r $(006)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10007

Write Miss in L1 but Hit in L2

w $(007)_{10}(00)_{10}$ $(01)_{10}(x)_{10}$ 10100. Miss in L1

eviction $(007)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$

r $(004)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10103. Miss in L1

w $(007)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 11000. Miss in L1

eviction $(008)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$

r $(001)_{10}(00)_{10}$ $(01)_{10}(x)_{10}$ 11003 Miss in L1

w $(007)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 11005. Hit

r $(005)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 12003 Miss in L1

eviction $(007)_{10}(00)_{10}$ $(01)_{10}(x)_{10}$

w $(002)_{10}(00)_{10}$ $(01)_{10}(x)_{10}$ 12005. Miss in L1

r $(007)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 12007. Hit

Case 4: Write Test, L1 Miss, L2 Miss

Write Hit

w $(007)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10000

r $(005)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10003

w $(008)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10005

r $(006)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10007

Write Miss in L1 and L2

w $(010)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 10100. Miss in L2

eviction $(007)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$

r $(005)_{10}(02)_{10}$ $(01)_{10}(x)_{10}$ 10103. Miss in L2

w $(009)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 11000. Miss in L2

eviction $(008)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$

r $(005)_{10}(02)_{10}$ $(01)_{10}(x)_{10}$ 11003 Hit

r $(010)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 11005. Hit

r $(001)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 11007. Miss in L2

w $(010)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 12003. Hit

w $(010)_{10}(02)_{10}$ $(01)_{10}(x)_{10}$ 12005. Miss in L2

eviction $(009)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$

w $(009)_{10}(01)_{10}$ $(01)_{10}(x)_{10}$ 12007. Miss in L1

r $(010)_{10}(02)_{10}$ $(01)_{10}(x)_{10}$ 13003. Hit