Project 3: Dynamically Changing Cache Associativity and Size in L1/L2

In this project you will study how **cache associativity** and **cache size** can affect the processor efficiency or target functions (**IPC/power, IPC^2/power**) during different phases of an application. You are required to run a set of simulations with **different L1 and L2 configurations**. You are also required to obtain the L1 and L2 cache power dissipation using **CACTI**.

The only modification that you are required to make to the smtsim code is to make it capable of **reporting the statistics periodically**. Then you need to generate a table that contains all IPCs and cache power numbers for all samples. Afterwards, **traversing the table**, you are required to find the **most efficient cache configuration through the application completion**. This means that you need to minimize the target functions.

Off-line Simulation:
In order to create the table, you need to simulate the processor with different memory subsystems as follows:

L1 (I-cache, D-cache) size	32KB, 64KB
L1 (I-cache, D-cache) associativity	1-way, 2-way
L2 size	128KB, 256KB
L2 associativity	4-way, 8-way

Creating the table, you need to calculate the efficiency or target functions (IPC/power & IPC^2/power) across all intervals with all configurations. Then, you are required to find the total efficiency by traversing the table.

* Please choose 3 benchmarks out of the available benchmarks.
**You need to run the simulations for 10 million institutions. Please fast-forward 10 million instructions as well for your simulations.
***You need to do the sampling every 10K instructions. Therefore you will have 1000 samples.
****Please consider the dynamic and static power dissipation of L1 and L2 caches to calculate the power.

Processor specification:

Please consider a single-core processor for your simulations. Please use the array below as for the processor configuration in you r python file:
c0 = [32, 32, 64, 64, 64, 24, 2, 32, 2, 32, 2, 1, 1, 8, 4]

L3 cache size and associativity should be set to 4MB and 16 respectively.

List of deliverables:

1- **Codes**

- Shell scripts for SMTSIM.
- SMTSIM source files.
- The code to traverse the table.
- Code or script to gather output data.

2- **Tables**

- For each benchmark: Any presentation of the table as long as being readable is acceptable. Both XLS and TXT files are fine.

3- **Report.** Your report should include the followings:

- A brief explanation of the project, your implementation and methodology. Please do not put any code in the report. You are required to explain about your implementation.
- **Results with explanations and observation.**
    - For each workload: two graphs showing the performance improvement of the adaptive configuration (most efficient) compared to all 16 base configurations for both target functions (one graph per target function).
- **Conclusion**

* Please explain the graphs thoroughly. All graphs should have a caption and a legend.
* *Please use separate folders for the shells and SMTSIMs source files. The report should be submitted in PFD format.