



EMV®

Terminal Type Approval

PCD Level 1

Interoperability Testing

Requirements

Version 1.1
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1 Introduction

This document describes how to perform EMVCo Terminal product Interoperability testing.

The purpose of the Interoperability Testing is to verify that the Terminal product sufficiently operates with a representative set of EMVCo approved PICC products, for multiple test positions in its Operating Volume.

During a first phase, EMVCo will define a **Set of EMVCo Approved Mobiles** to be used during the Interoperability test session. Additional devices may be added in the future as new models, new form factor and next technologies may be approved by EMVCo.

1.1 Audience

This document is intended for test tool providers, product providers and Laboratories that offer EMVCo Terminal interoperability testing services.

1.2 Scope

This document provides a technical description of the Interoperability Testing process Laboratories shall implement.

For the applicability of testing requirements, refer to [TTA ADM].

1.3 Revision History

Table 1-1: Revision History

Version	Changes From Previous Version
1.0	<ul style="list-style-type: none">Initial version
1.1	<ul style="list-style-type: none">Update of Interoperability test Pass Criteria

2 Normative References

The version numbers identified in the references below are valid at the time of release of this document. Nevertheless, the latest versions available from EMVCo shall apply as per their applicability dates

2.1 EMV Specifications

EMV Specifications are publicly available on the EMVCo website: www.emvco.com.

Table 2-1: EMV Specifications

Publication Name	Version	Reference
EMV Contactless Specifications for Payment Systems – Book D – EMV Contactless Communication Protocol Specification	Latest available since 2.6 – March 2016	[CCPS]
EMV Contactless Specifications for Payment Systems – Book A – Architecture and General Requirements	Latest available since 2.6 – April 2016	[CTL BOOKA]
All Specification Update Bulletins as published on the EMVCo website	Latest available	

Note: the applicability date of a new EMV specification is defined by EMVCo on a regular basis.

2.2 Related EMV Documents

Table 2-2: Related EMV Documents

Publication Name	Version	Reference	Availability
EMVCo Terminal Type Approval PCD Level 1 Administrative Process	Latest Available	[TTA ADM]	EMVCo Website
EMVCo_TTA_Laboratory Process Guide for Terminal Level 1 Interoperability Testing	Latest Available	[TIT LAB GUID]	Laboratories only
EMVCo Type Approval Contactless Terminal Level 1 Device Test Environment	Latest Available	[L1DTE]	EMVCo Website
EMV Terminal Type Approval Bulletin 195	Latest Available	[L1NDTE]	EMVCo Website

Publication Name	Version	Reference	Availability
All Terminal Type Approval Update Bulletins as published on the EMVCo website	Latest Available		

Note: the applicability date of a new EMV specification and any related documents is defined by EMVCo on a regular basis.

2.3 Terminal Product Level 1 Type Approval Forms

Table 2-3: Terminal Product Level 1 Type Approval Forms

Publication Name	Version	Distribution
EMVCo Terminal Level 1 PCD Implementation Conformance Statement	Latest Available	[L1ICS]

3 Abbreviations & Definitions

3.1 Abbreviations

Abbreviation	Description
CCPS	Contactless Communication Protocol Specification; see Table 2-1.
DUT	Device Under Test
EE	Execution Environment. The environment where the payment application is executed, e.g. UICC, eSE, HCE.
HCE	Host-based Card Emulation
ICS	Implementation Conformance Statement: A form completed by the Product Provider identifying the Product, the EMV mandatory functions, the EMV optional functions supported, and (if any) the non-EMV proprietary functions.
L1	One of the two levels of EMV testing: Testing the proximity contactless communication interface of a mobile product according to [CCPS].
UICC	Universal Integrated Circuit Card
DTE	Device Test Environment

3.2 Definitions

Term	Definition
Analogue Test	Set of tests that checks the Radio Frequency of the hardware and software/firmware of the PCD against the EMV Specifications.
Card Reader	Reader, to be connected to a Terminal, to allow the Terminal to perform a financial transaction, when the Terminal does not embed the implementation(s) needed for its intended use.
Device Test Environment	Part of the Test Environment needed to perform the Type Approval Test, which the Vendor needs to develop and submit to the Test Laboratory at the same time as the Samples.
Device Under Test (DUT)	Sample within which the PCD submitted for Type Approval is actually tested.
EMV Specifications	Set of documents defining the requirements, which the PCD shall comply with for PCD Type Approval (and listed in the “Normative References” section of the PCD Type Approval Administrative Process document).

EMVCo	Organization established to maintain the EMV specifications and administer Type Approvals against those specifications.
Environment	Part(s) of the product constituted of components that are not part of the PCD - as they are not involved in PCD functionality - but interface with the PCD (for example used by, connected to,..) or have a direct impact on the behavior of the PCD.
Landing Plane	The identified area where a cardholder must 'tap' their contactless card or device to achieve a successful read.
Operating Volume	3-dimensional space in which the PCD can communicate with a PICC by means of a magnetic field.
Proximity Coupling Device (PCD)	Peripheral device of the terminal, that uses inductive coupling to provide power to the PICC and also to control the data exchange with the PICC, up to the transport layer (included), as specified in the EMV Specifications.
Test	Any activity that aims at verifying the conformance of a selected product or process to a given requirement under a given set of conditions.
Test Bench	Defined combination of a set of test methods and test equipment used when performing a Test and owned by the Test Laboratory.
Test Case	Description of the actions required to achieve a specific Test objective.
Test Environment	Environment needed to perform the Test. It is constituted of a Test Bench in combination with a Device Test Environment for PCD Type Approval Test.
Test Laboratory	Facility accredited by EMVCo to perform PCD Type Approval Test.
Test Report	Document provided by the Test Laboratory containing the Test results.

4 Testing Methodology

The testing process is a two-stage process, an initial validation testing followed by interoperability testing stage.

This testing process is included in the EMVCo Level 1 PCD approval

4.1 Device Under Test

The Device Under Test (DUT) is defined in [TTA ADM]. At least three samples are to be provided by the product provider.

The DUT shall be preloaded with a DTE application defined in [L1NDTE].

During Validation and Interoperability Testing:

- DUT with External Power Source shall be connected to its Power supply during all the testing Process.
- For portable equipment, fully charged internal batteries shall be used. The batteries used shall be as supplied or recommended by the vendor. If internal batteries are used, the test power source voltages shall remain within the vendor tolerance and is checked by the Laboratory. The battery load must be at least 50% of its capacity until the end of the interoperability test session.

Note: if during a test session the battery load is lower than 50%, the Laboratory is authorized to reload it

4.2 Mobiles

Mobiles used for Validation and Interoperability Testing are EMVCo Approved Mobiles. The number of mobiles will be defined and managed by EMVCo.

During Validation and Interoperability tests, to support the testing environment, Mobiles have to be configured:

- Either with an HCE test application
- Or with an UICC Type B containing a test application

The test applications allow interaction with the Interoperability Loop Back Application defined in [L1NDTE]

4.3 Validation Testing

4.3.1 Description

Validation Testing consists of performing a successful transaction between the DUT and the Mobiles defined by EMVCo, these mobiles can be updated at any time by EMVCo . Validation testing may be performed manually or by utilizing an automatic positioning system.

- Validation Testing shall be performed on three DUT samples.

- Five transactions shall be performed at a single test position ($r=0$, $\phi=0$, $z=1$). Not more than 5 taps shall be attempted in order to meet the pass conditions. The test position is defined in [CCPS] Annex C.
- Only one Mobile orientation is used for testing ($\theta = 0$).
- The Z reference ($z=0\text{cm}$) is the landing plane.

4.3.2 Pass Criteria

The validation pass criteria are defined as:

- At minimum, three out of five transactions per mobile are successful, for all mobiles (not necessarily consecutive successful transactions) and for each DUT sample.

The DUT shall pass Validation Testing to be eligible for Interoperability Testing and for a Letter of Approval

Note : A successful transaction is identified by one of the three indicators generated by the DTE Interoperability loopback:

- Sound Indicators.
- LED Indicators.
- TTL Signals.

4.4 Interoperability Testing

4.4.1 Description

Interoperability Testing shall be performed on each mobile specified by EMVCo using an automatic positioning system to ensure accuracy of the test positions and movements.

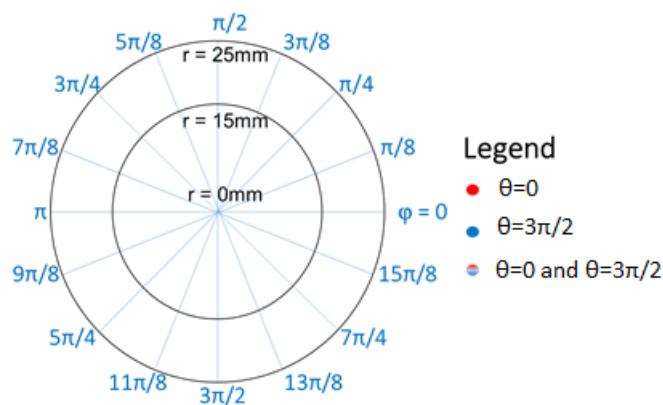
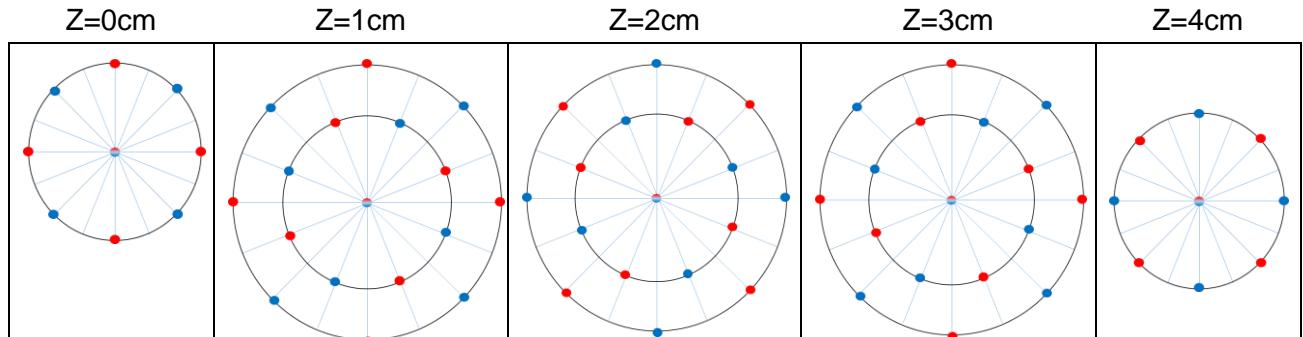
The Laboratory shall use the same DUT sample used for EMVCo Analogue L1 Type Approval Test sessions.

The automatic positioning system shall present the mobile to the DUT once at each position defined in Figure 4-1.

The mobile shall be presented to the DUT using two orientations: $\theta = 0$ and $\theta = -\pi/2$ (Refer to [CCPS] Annex C2 for definition of θ).

Each orientation θ shall be tested at the test positions indicated in Figure 4-1.

Figure 4-1: Test Positions



- There is a total of 74 positions defined and 2 orientations.
- The mobile shall be present at each test position for a maximum duration of 1.5 seconds before being removed.
- The test bench shall implement a delay between each transaction to allow the DUT to restart the transaction for the next test position. Laboratories are advised to carefully define this value to optimize test duration.

4.4.2 Pass Criteria

Each test position is designated with a weighted value. The weighted values per mobile are provided in [TIT LAB GUID].

The Success Rate of a mobile is defined by the following formula:

- W_i is the weight of position i
- R_i is the Result of the transaction at position i ($R_i = 1$ if success or $R_i=0$ if transaction failed)
- TWV is the total weighted value $TWV = \sum W_i$
- TR is the test result for one mobile $TR = \sum (R_i * W_i)$

- Success Rate = TR/TWV

In case the PCD Under Test cannot be tested in all the positions of the operating volume defined in chapter 4, Laboratories shall follow the following procedure:

- Untestable positions at $z=0\text{cm}$:
 - If position (z_0,r,f) can be tested with $z_0 \leq 5\text{mm}$: The product is tested at the closest testable position (z_0,r,f) to the $(0,r,f)$ position using the weights defined for position $(0,r,f)$.
 - If product cannot be tested at (z_0,r,f) with $z_0 \leq 5\text{mm}$: Product is not tested for position $(0,r,f)$
- Untestable positions at $z \geq 1\text{ cm}$
 - Positions inaccessible due to terminal shape are reported as not tested
- In case of untestable positions, the weight of untested positions will not be taken into account in the Success Rate calculation.

Based on the number and the location of untested positions EMVCo will decide to issue or not the LOA.

The pass criteria for Interoperability Testing are defined below:

1. The Success Rate shall be greater than or equal to 83% for each mobile.
2. At least 50% of the test positions at $z=0\text{ cm}$ shall be PASS.

The DUT shall pass the Interoperability Testing to be eligible for a contactless Level 1 Letter of Approval

Note 1: A successful transaction is identified by one the three indicators generated by the DTE Interoperability loopback

- a. Sound Indicators.
- b. LED Indicators.
- c. TTL Signals.

Note 2: The pass criteria and weighted values are subject to change over time.

5 Requirements for Testing Laboratories

5.1 Testing Conditions

The DUT shall be tested in the following conditions:

- Without the use of any external RF device that could have an impact e.g. RF spy tool.
- The same DUT as the one used for EMVCo Analogue L1 Type Approval Test sessions shall be used.
- The DUT shall be securely positioned for the automatic positioning system. The DUT must be provided with a Contactless Symbol representing the reference testing point.
- The DUT may be connected to an external power supply.
- The DUT may be connected to a PC.
- DUT shall be switched on for a minimum of 5 minutes before testing begins.
- The mobile shall be switched on.
- The mobile display shall be on.
- The mobile battery must not be in a charging mode during test session. If necessary the mobile can be recharged between test sessions.
- When multiple batteries for PCDs Under Test are used during the test, the Laboratory shall clearly indicate which battery was used for which test session and which DUT.
- If the interoperability testing fails, the Laboratory shall verify the mobile is not in power saving mode. If it is the case, the test shall be run again with a recharged battery.
- Bluetooth, Wi-Fi and GPS technologies shall be disabled on the mobile.
- All the mobile contactless protocols shall be enabled (e.g. Type A, Type B, NFC-F, P2P, R/W mode etc....)
- The default configuration shall be open or normal mobile NFC payment usage.

5.2 Forms

As this process is part of the EMVCo Contactless Level 1 Type Approval process, the existing L1 ICS must be submitted when the Level 1 process is initiated.

5.3 Normal Temperature and Humidity

The normal temperature and humidity conditions for Validation and Interoperability Testing shall be any convenient combination of temperature and humidity within the following ranges:

- Temperature between: $23^{\circ}\text{C} \pm 3^{\circ}\text{C}$
- Relative humidity: 40 % to 60 %.

When it is impractical to carry out tests under these conditions, a note to this effect, stating the ambient temperature and relative humidity during the tests, shall be added to the test report.

6 Positioning Conventions

6.1 DUT Positioning Conventions

6.1.1 Terminal Z Axis

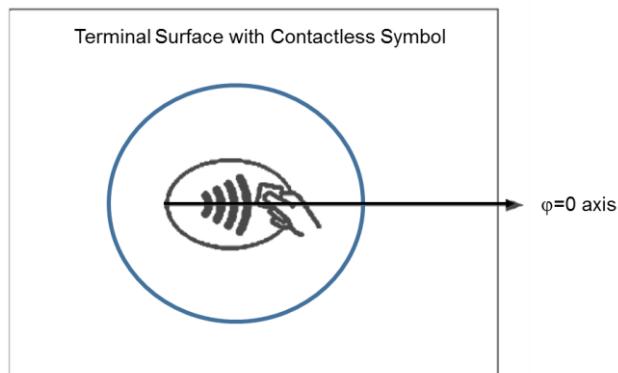
The following characteristics are introduced to support the positioning convention:

- The centre of the landing plane is the centre of the contactless symbol
- The Z axis of the DUT is the axis which passes through the centre of the Contactless Symbol, orthogonal to the landing plane or to the tangent of the landing plane and directed outwards from the terminal surface.

6.1.2 $\varphi = 0$ Axis

The $\varphi = 0$ axis of the DUT is indicated by the Contactless Symbol

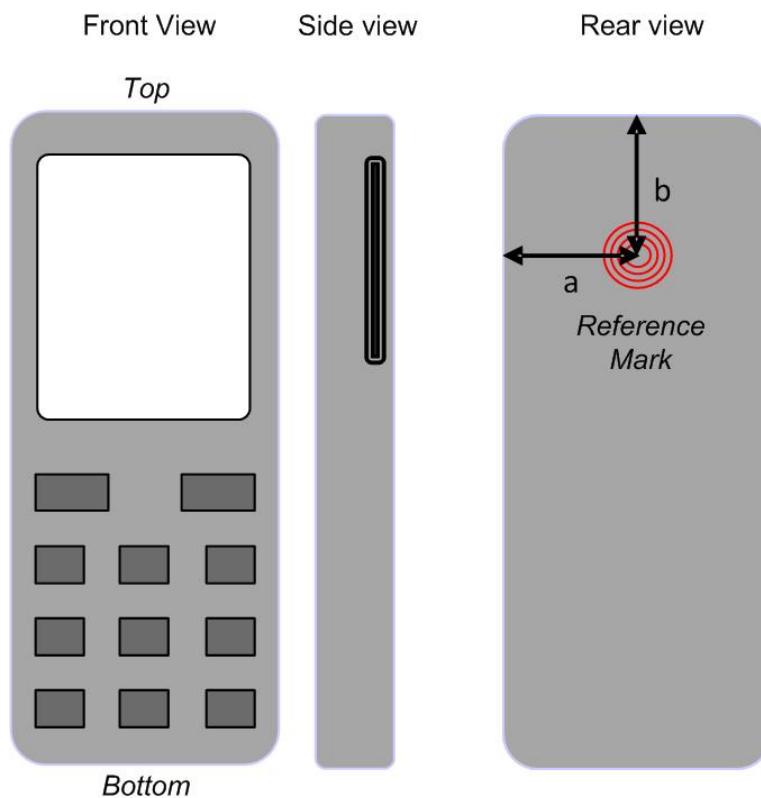
Figure 6-1: $\varphi = 0$ axis on the Test DUT



6.2 Mobile Positioning Conventions

Positioning conventions used in this document are compliant with [CCPS] Annex C.

Figure 6-2: Mobile Reference Mark



6.2.1 Mobile Z Axis

The following characteristics are introduced to support the positioning convention:

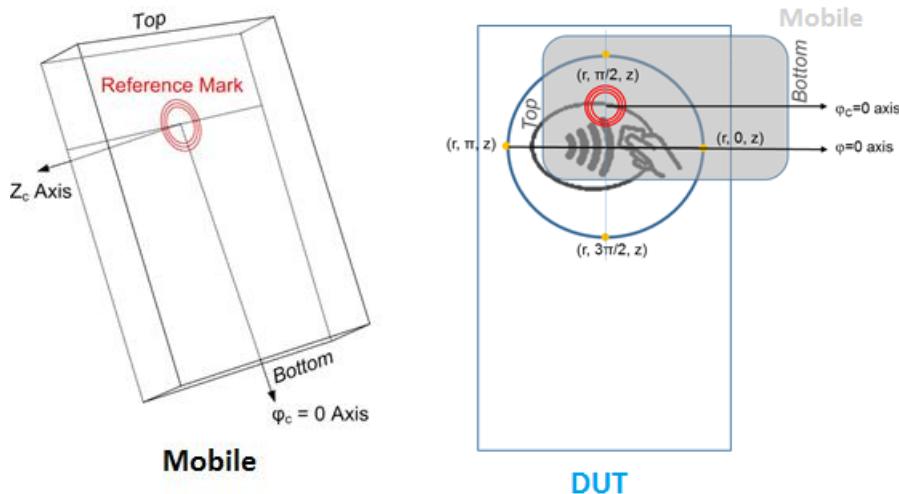
- The presentation plane is the outer part of the mobile that is presented over the landing plane of the DUT.
- The z axis of the mobile is the axis going through the reference mark, vertical to the presentation plane and directed outwards from the surface of the mobile.

6.2.2 Mobile orientation θ

The mobile orientation $\theta=0$ is defined by:

- The mobile $\varphi_c = 0$ axis must be aligned with the DUT $\varphi = 0$ axis.
- The top of the mobile must be placed on the DUT (r, π, z) position side as shown in below diagram:

Figure 6-3: DUT $\theta = 0$ Definition



The following pictures present examples of position and orientation of the mobile when φ and θ vary

Figure 6-4: Positioning for $\theta = 0$, $\varphi = \pi/2$, $r \neq 0$

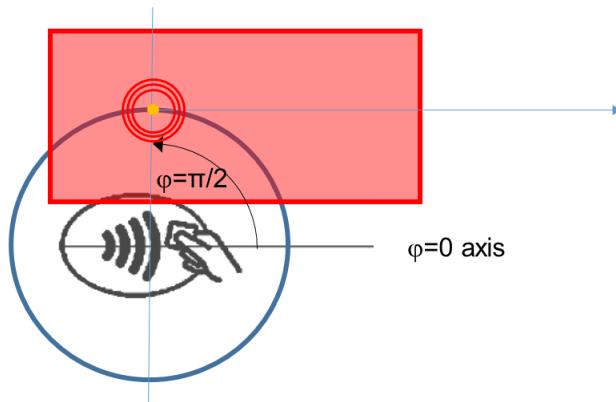


Figure 6-5: Positioning for $\theta = 0$, $\varphi = 3\pi/2$, $r \neq 0$

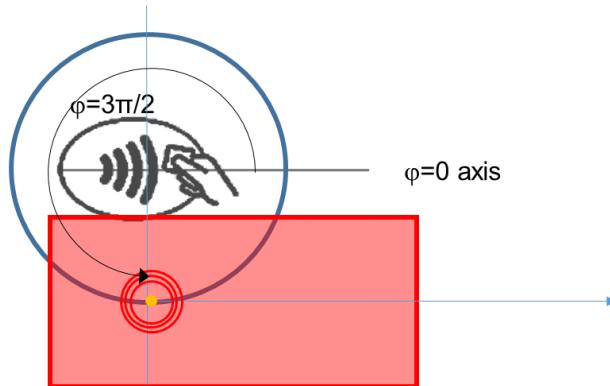
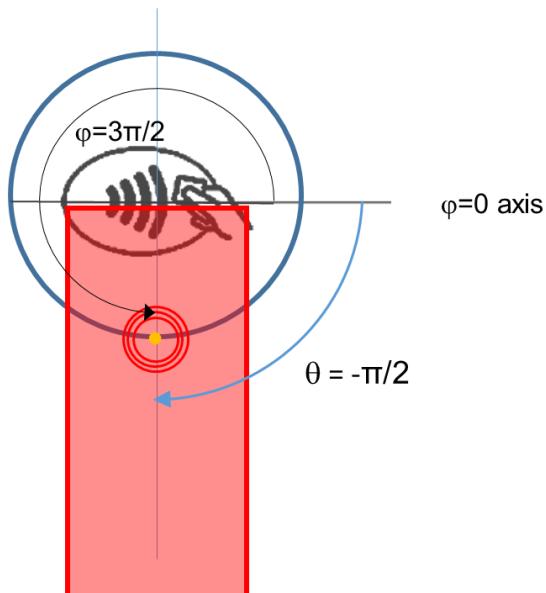


Figure 6-6: Positioning for $\theta = -\pi/2$, $\varphi = 3\pi/2$, $r \neq 0$

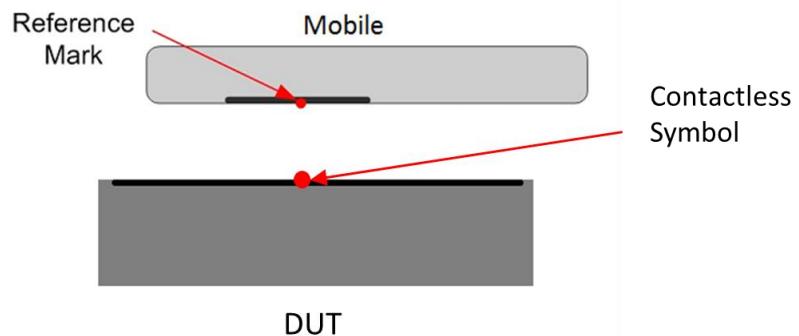


6.3 Mobile Presentation Rules

In order to avoid positioning inconsistencies between Laboratories, the following rules shall be followed:

- The presentation plane of a mobile shall always be parallel to the landing plane of the DUT as per Figure 6-7
- The mobile must be presented to the DUT on the side of the Reference Mark.

Figure 6-7: Mobile positioning on the DUT



7 Requirements for the Positioning System

7.1 Introduction

The Positioning System used for the Interoperability Testing, shall be automatic and programmable to carry out specific actions to place the mobile in the various test positions of the DUT's Operating Volume, repeatedly, with acceptable variation and with a high degree of accuracy. These actions are determined by programmed routines that specify the direction, acceleration, velocity, deceleration, and distance of a series of coordinated motions.

The automatic positioning system shall consist of a fixed chassis and at least one arm, for holding and moving small objects. Three axes are required to reach any point in space.

The automatic positioning system shall be connected to a computer via a communication port in order to be correctly configured with a dedicated software

7.2 General Requirements

- The positioning system shall be able to position the mobile attached to its moving arm at all test positions defined in section 4.4.1 of the DUT's Operating Volume.
- The positioning system shall be capable to handle any mobile device.
- The DUT is securely positioned.
- When the mobile is presented to the DUT, there shall be no metallic object in the vicinity of the mobile & the DUT, to ensure that the electro-magnetic field is not disturbed. A distance of at least 15 cm shall be met between the mobile and any metallic object pertaining to the positioning system.
- A distance of at least 15 cm shall be met between the DUT and any metallic object pertaining to the positioning system.
- When the mobile is presented to the DUT, the presentation plane of a mobile shall always be parallel to the landing plane of the DUT.

7.3 Positioning Requirements

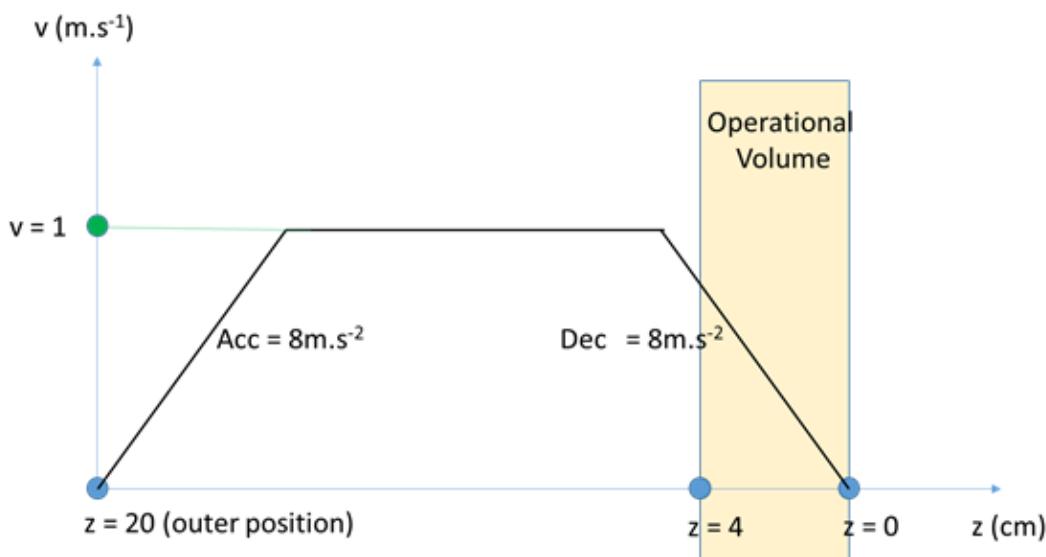
- For each mobile in the test pool, the positioning system shall be calibrated so that the test position (0,0,0) called origin, is defined as the centre of the contactless symbol on the landing plane of the DUT.
- The positioning system shall be programmable with at least three coordinates (r, φ, z) relative to the origin

7.4 Motion Requirements

- The mobile shall be presented in a vertical movement as specified in section 7.6.
- The positioning system shall move the mobile during the vertical movement, excluding the start and end, at a speed of 1 m/s.
- The mobile shall not be moving in the operating volume for more than 100ms. Consequently, the positioning system shall decelerate the mobile at the end of the vertical movement at a rate of minimum 8 m/s².

The expected movement is represented in the Figure 7-1 below

Figure 7-1: Mobile movement to position for target z=0



7.5 Physical Alignment of DUT, Mobile and Automatic Positioning System

7.5.1 Alignment of the z Axis

The purpose of this procedure is to align the z axis of the automatic positioning system and the z axis of the DUT. An automated process using laser measurement and automatic placing is possible and recommended.

Step	Actions
1	<ul style="list-style-type: none"> Identify the z axis of the positioning system.

	<ul style="list-style-type: none"> • Prepare the positioning system to ensure the z axis is visible.
2	<ul style="list-style-type: none"> • Identify the z axis of the DUT and if possible, make the z axis of the DUT visible. • Identify the $\varphi=0$ axis of the DUT.
3	<ul style="list-style-type: none"> • Mount the DUT and the positioning system next to each other so that the z axis of the positioning system is nearly parallel to the z axis of the DUT. • Verify that the positioning system will be able to cover the operating volume of the DUT.
4	<ul style="list-style-type: none"> • Move the DUT and the positioning system so that the z axis of the positioning system is parallel to the z axis of the DUT.
5	<ul style="list-style-type: none"> • Mechanically secure the DUT and the positioning system in this position.
6	<ul style="list-style-type: none"> • Secure the z axis of the positioning system in this position.

7.5.2 Mounting Mobile on the Positioning System

The purpose of this procedure is to ensure that the orientation of the mobile conforms to the requirements listed in 4.4.1, with the value of the θ being 0 or $-\pi/2$

Step	Actions
1	<p>Fix the mobile to the arm of the positioning system to fulfil the following conditions:</p> <p>The z axis of the mobile is parallel to the z axis of the positioning system and points in the opposite direction.</p> <p>The angle between the $\varphi=0$ axis of the DUT and the $\varphi_c=0$ axis of the mobile is 0 degrees (or $-\pi/2$).</p>

7.5.3 Installation of the Origin (0,0,0)

The purpose of this procedure is to ensure that at position (0,0,0), the reference Mark of the mobile is as close as possible to the centre of the Contactless Symbol of the DUT.

Step	Actions
1	Program the positioning system to move the mobile so that the Z axis of the DUT crosses the reference mark (Figure 6-2).
2	Reset the coordinating system for the positioning system so that $r = 0$ for this position.
3	Carefully let the positioning system move the mobile down until it is just one vertical increment away from touching the terminal landing plane. (The mobile shall not touch the DUT landing plane). This can be verified by placing a sheet of paper between the mobile and the DUT such that it is still possible to move the paper).
4	Raise the mobile again by 0.05 cm (to compensate for the tolerance in positioning of the positioning system).
5	Reset the coordinating system of the positioning system so that the z axis for this position is 0 (except if DUT cannot be positioned at $z=0$: see 7.3). .

7.6 Vertical Presentation of the Mobile

This section describes how the positioning system shall be programmed to:

1. Bring the mobile into the Operating Volume of the DUT.
2. Keep the mobile at the programmed position for the required time defined in section 4.4.1.
3. Remove it again from the Operating Volume of the DUT.

For each of the programmed positions, the positioning system will begin the presentation from a position with the same values of (r, φ) as the programmed position, but with $z_{\text{initial}} = z + 20$ cm (the outer position).

The positioning system shall move the mobile along a straight line parallel to the z axis until the programmed position is reached. The positioning system shall then maintain the mobile in that programmed position for 1.5 second, and subsequently withdraw it again along a line parallel to the z axis.

When moving the mobile to or from the programmed position, the positioning system shall be programmed to move the mobile in a precise way compliant with the motion requirements described in section 7.4. This applies to all movement including acceleration, and deceleration of the DUT along the z axis. This is to ensure timing repeatability of the presentation.

7.7 Tolerance

This section describes the tolerance for the various measurements:

Item	Tolerance value
Duration of stay at a test position before the mobile is positioned back to the outer position	+/- 0.1s
Position (r , φ , z). Tolerance in any direction between the programmed position and the actual position obtained	+/- 0.05 cm
Vertical Acceleration or Deceleration	+/- 1.5m/s ²
Vertical Speed	+/- 0.1 m/s
Orientation of the mobile (θ)	+/- 3°
Deviation between z axis of the positioning system and Z axis of the DUT	+/- 3°
Deviation between the landing plane of the DUT and the presentation plane of the mobile	+/- 5°
Deviation between z axis of the positioning system and z axis of the mobile	+/- 3°
Deviation between $\varphi=0$ axis of the positioning system and $\varphi_c=0$ axis of the mobile	+/- 3°

*** END OF DOCUMENT ***

MP45 mPOS 国际金融部分认证目录

EMVCo Type Approval Contact Terminal Level 1

EMVCo Letter of Approval- Contact Terminal Level 1

EMVCo Type Approval Contact Terminal Level 2

EMVCo Letter of Approval- Contact Terminal Level 2

EMVCo Type Approval Contactless Terminal Level 1

EMVCo Letter of Approval- Contactless Terminal Level 1

PCI PTS TERMINAL V4.1 Evaluation Report of Tianyu MP45

Payment Card Industry(PCI) Security Standards Council Letter of Approval





Report

EMVCo®* Type Approval Contact Terminal Level 1

Report No. : TEMC1601174

Oct. 27, 2016

Ref.: EMVCo Terminal Type Approval Version 4.3a

November 2015

Performed for : Wuhan Tianyu Information Industry Co.,Ltd.

Test object: MP45 V1.0

Serial number : 1312B13410243492

Bank Card Test Center Shenzhen Branch

1-6F Finance Center, No.8 Kefa Road, Nanshan Science Park, Shenzhen, China

TEL: (+86) 755-33372905

FAX: (+86) 755-33372900

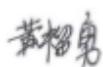
www.bctest.com

* EMV is a registered trademark in the U.S. and other countries and an unregistered trademark elsewhere. The EMV trademark is owned by EMVCo.

Title	EMVCo Type Approval Contact Terminal Level 1
Report NO.	TEM C1601174
Test object	MP45 V1.0
Test period	from 2016-10-18 to 2016-10-19
Laboratory	Bank Card Test Center Shenzhen Branch
Address	1-6F Finance Center, No.8 Kefa Road, Nanshan Science Park, Shenzhen, China
Client	Wuhan Tianyu Information Industry Co.,Ltd.
Client Address	Tianyu Building, S&T Park, HUST, East-Lake Development, Wuhan 430223, Hubei, China
Contact person	Li Xiao jun Tel: 027-87920300 Fax: 027-87920306 Email: lxj@whty.com.cn
Manufacture	Wuhan Tianyu Information Industry Co.,Ltd.
Specifications	[1] EMV 4.3 Integrated Circuit Card Specification for Payment Systems, Book 1, Version 4.3, November 2011. [2] EMV 4.3 Integrated Circuit Card Specification for Payment Systems, Book 2, Version 4.3, November 2011. [3] EMV 4.3 Integrated Circuit Card Specification for Payment Systems, Book 3, Version 4.3, November 2011. [4] EMV 4.3 Integrated Circuit Card Specification for Payment Systems, Book 4, Version 4.3, November 2011 [5] EMVCo Terminal Type Approval: Level 1 Mechanical and Electrical Test Cases, Version 4.3a, November 2015 [6] EMVCo Terminal Type Approval: Level 1 Protocol Test Cases, Version 4.3a, November 2015

Date 2016-10-27

Edited by 

Reviewed by 

Approved by 



Xiaojun Li

Wuhan Tianyu Information Industry Co., Ltd.
Tianyu building, S&T Park, HUST
East-Lake Development Zone
Wuhan 430223
CHINA

Re: **EMVCo Letter of Approval – Contact Terminal Level 1**

Approval Number: **15395 1116 430 43a 43a BCTS**

IFM Identification: **MP45** Version: **V1.0**

Hardware: **MP45 mainboard** Version: **V1.0**

Software: **MP45 firmware** Version: **V1.0**

As tested in: **MP45**

Renewal Date: **October 27, 2020**

Dear Xiaojun Li,

EMVCo, LLC ("EMVCo"), a Delaware limited liability company, has received your request for Level 1 terminal type approval for the interface module identified above. In connection with your request, we have reviewed your report, identified by file number TEMC1601174 Version V1.0 which was generated by Beijing Unionpay Card Technology Co., Ltd. Shenzhen Branch.

After assessing such file, EMVCo has found reasonable evidence that the submitted samples of the above referenced interface module sufficiently conform to EMV Integrated Circuit Card, Specifications for Payment Systems, Version 4.3, November 2011.

EMVCo hereby grants your interface module EMVCo Type Approval for Terminal Level 1, based on the requirements stated in the EMV 4.3 Specifications. Please note that EMVCo may publicly identify your interface module as an approved interface module, including in EMVCo's published list of approved interface modules.

EMVCo's grant to your interface module is subject to and specifically incorporates (i) the General Terms and Conditions to the Letter of Approval enclosed as Exhibit A, and (ii) the Specific Terms and Conditions to the Letter of Approval attached hereto as Attachment 1. Because EMVCo's grant is subject to such limitations, including certain events of termination, you and any third parties should confirm that such approval is current and has not been terminated by referring to the list of approved interface modules published on the EMVCo website (www.emvco.com).

Please note that EMVCo makes certain logos available for use in connection with an interface module that has received EMVCo approval. To obtain permission to use the "EMV Approved" certification mark, please contact EMVCo to request a license agreement

This Letter of Approval is valid while the approval number is posted on the EMVCo website.

EMVCo, LLC, a Delaware limited liability company

By: **Frederic Fortin**
2016.11.17 13:12:24 +01'00'

Name: **Frédéric Fortin**

Title: **EMVCo Terminal Type Approval**



Report

EMVCo Type Approval Contact Terminal Level 2

Report No. : TEMV1602181

Nov. 28, 2016

Ref.: EMV Version 4.3

November 2011

Performed for : Wuhan Tianyu Information Industry Co., Ltd

Test object: MP45

IFM(L 1) Approval No. : 15395 1116 430 43a 43a BCTS

Bank Card Test Center Shenzhen Branch

1-6F Finance Center, No.8 Kefa Road, Nanshan Science Park, Shenzhen, China

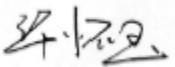
TEL: (+86) 755 33372905

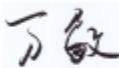
FAX: (+86) 755 33372900

www.bctest.com

Title	EMVCo Type Approval Contact Terminal Level 2
Report NO.	TEMV1602181
Test object	MP45
Test period	From 2016-11-23 to 2016-11-28
Laboratory	Bank Card Test Center Shenzhen Branch
Address	1-6F Finance Center, No.8 Kefa Road, Nanshan Science Park, Shenzhen, China
Client	Wuhan Tianyu Information Industry Co., Ltd
Client Address	Tianyu building, S&T Park, HUST East-Lake Development Zone 430223 Wuhan
Contact person	Guest: Xiaojun Li PHONE: +86 27 87920300 FAX: +86 27 87920306 EMAIL: lxj@whty.com.cn
Manufacture	Wuhan Tianyu Information Industry Co., Ltd
Specifications	[1] EMV 4.3 Integrated Circuit Card Specification for Payment Systems, Book 1, Version 4.3, November 2011. [2] EMV 4.3 Integrated Circuit Card Specification for Payment Systems, Book 2, Version 4.3, November 2011. [3] EMV 4.3 Integrated Circuit Card Specification for Payment Systems, Book 3, Version 4.3, November 2011. [4] EMV 4.3 Integrated Circuit Card Specification for Payment Systems, Book 4, Version 4.3, November 2011 [5] EMVCo Type Approval Terminal Level 2 Test Cases, Version 4.3e, November, 2015

Date 2016-11-28

Edited by 

Reviewed by 

Approved by 



December 28, 2016



Xiaojun Li

Wuhan Tianyu Information Industry Co., Ltd.

Tianyu building, S&T Park, HUST

East-Lake Development Zone

Wuhan 430223

CHINA

Re: **EMVCo Letter of Approval - Contact Terminal Level 2**

EMV Application Kernel: **TYEMVKERNEL Version V1.0**

Approval Number(s): **2-03826-1-1C-BCTS-1216-4.3.e**

2-03826-1-1OS-BCTS-1216-4.3.e

The EMV Application Kernel has been tested on the following terminal

Terminal: **MP45**

PinPad: **n/a**

Operating System: **1OS = TYOS Version V1.0**

Renewal Date: **28-Nov-2019**

Report ID **Session 1: TEMV1602181 - Beijing Unionpay Card Technology Co., Ltd. Shenzhen Branch**

Kernel Checksum:

CC D4 29 1E 22 3E 9F 0D BD 97

Configurations Checksums:

Config	Vendor Config ID	Terminal	Checksum
1C	C1	22	B0 03 ED 17 12 E8 C7 96 B0 1A



EMVCo®* Type Approval Contactless Terminal Level 1

MP45_PCD Test Report

EMV Contactless Communication Protocol Specification v2.5

Report reference:	TEML1601029
Report version:	V1.0
Report issue date:	03/Nov/2016
Number of pages:	95
Vendor identification:	WuHan Tianyu Information Industry Co.,Ltd.
PCD identification:	MP45_PCD
PCD version:	V1.0
As tested in:	MP45
Product configuration:	Fully integrated terminal
Testing dates:	From 10 Oct to 11 Oct, 2016
Test Bench identification:	TB107
Edited by:	Jiang Zuochen
Reviewed by:	Zheng Chao
Approved by:	Zhang Yongfeng

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Date: 03-11-2016

Edited by:

Reviewed by:

Approved by:



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Revision History

Date	Version	Author	Comments
03/11/2016	V1.0	Jiang Zuochen	Initial Version

Xiaojun Li

Wuhan Tianyu Information Industry Co., Ltd.
Tianyu building, S&T Park, HUST
East-Lake Development Zone
Wuhan 430223
CHINA

Re: EMVCo Letter of Approval – Contactless Terminal Level 1

Approval Number: 15396 1116 250 25a 25a BCTS

PCD Identification: MP45_PCD Version: V1.0

Hardware: MP45 mainboard Version: V1.0

Software: MP45 firmware Version: V1.0

As tested in: MP45 Version V1.0

PCD/Terminal Configuration: Samples are Fully Integrated Terminals (FIT)

Analog Test Cases: 2.5a *Digital Test Cases:* 2.5a

Renewal Date: November 3, 2020

Dear Xiaojun Li,

EMVCo, LLC ("EMVCo"), a Delaware limited liability company, has received your request for Level 1 terminal type approval for the proximity coupling device identified above. In connection with your request, we have reviewed your report, identified by file number TEML1601029 Version V1.0 which was generated by Beijing Unionpay Card Technology Co., Ltd (Bank Card Test Center).

After assessing such file, EMVCo has found reasonable evidence that the submitted samples of the above referenced proximity coupling device sufficiently conform to Book D - EMV Contactless Communication Protocol Specification, Version 2.5 of March 2015.

EMVCo hereby (a) grants your proximity coupling device EMVCo Type Approval for Terminal Level 1, based on the requirements stated in the EMV 2.5 Specifications, and (b) agrees to include your proximity coupling device in EMVCo's approved proximity coupling device list.

EMVCo's grant to your proximity coupling device is subject to and specifically incorporates (i) the General Terms and Conditions to the Letter of Approval enclosed as Exhibit A, and (ii) the Specific Terms and Conditions to the Letter of Approval attached hereto as Attachment 1. Because EMVCo's grant is subject to such limitations, including certain events of termination, you and any third parties should confirm that such approval is current and has not been terminated by referring to the list of approved proximity coupling devices published on the EMVCo website (www.emvco.com).

Analog performance being evaluated using Contactless Symbol as reference for the center of the operational volume this LoA is contingent on the EMVCo Contactless Symbol being present and in the "correct" location.

The "correct" location being the Center of the operating volume as identified by the vendor for EMVCo Type Approval unless especially agreed by EMVCo.

This Letter of Approval is valid while the approval number is posted on the EMVCo website.

EMVCo, LLC, a Delaware limited liability company

By: Frederic Fortin

2016.11.28 11:51:03 +01'00'

Name: Frédéric Fortin

Title: EMVCo Terminal Type Approval



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CoC 30105045

PCI PTS TERMINAL v4.1 Evaluation Report of Tianyu MP45

date	20 July 2017
author	Exurville Ingrid, Alejandro Ferrer, Chao Qu, Henko Aantjes
project manager	Shu Gao
number of pages	218
number of appendices	
customer	Tianyu
report ID	16-RPT-543
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project name	Tianyu MP45
project number	09070

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Authors	Ingrid Exurville, Alejandro Ferrer, Chao Qu, Henko Aantjes
Release officer	Shu Gao
Technical reviewer	Razvan Venter

Summary

Compliance assessment

Module 1	Core Requirements	Verified
	<i>Core Physical Security Requirements</i>	Brightsight was able to verify compliance with all the applicable Core Physical requirements.
	<i>Core Logical Security Requirements</i>	Brightsight was able to verify compliance with all the applicable Logical Security Core requirements.
	<i>Online PIN Security Requirements</i>	Brightsight was able to verify compliance with all the applicable Online requirements.
	<i>Offline PIN Security Requirements</i>	Brightsight confirmed that Offline requirements are not applicable .
Module 2	POS Terminal Integration Requirements	N/A
Module 3	Open Protocol Requirements	Verified
	Brightsight was able to verify compliance with all the applicable requirements.	
Module	Core Configuration and maintenance security	Verified
	Brightsight was able to verify compliance with all the applicable requirements.	
Module 4	Secure Reading and Exchange of Data	Verified
	Brightsight was able to verify compliance with all the applicable requirements.	
Module 5	Device Management Security Requirements	Verified
	Brightsight was able to verify compliance with all the applicable requirements.	

Payment Card Industry (PCI) Security Standards Council
Letter of Approval
PCI PIN Transaction Security Testing Program

10 Aug 2017

Xuedong Su

Wuhan Tianyu Information Industry Co., Ltd.

Tianyu Building, Huazhong, University of Science and Technology, Industry Park, East Lake Zone
Wuhan City, Hubei Province 430223
China

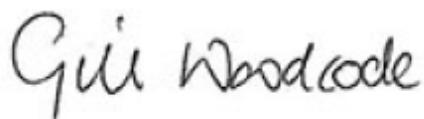
PCI SSC PTS Approval Number:	4-30274	Approval Class:	PED
Manufacturer:	Wuhan Tianyu Information Industry Co., Ltd.		
Name & Model Number:	MP45		
Hardware Version Number:	V1.00		
Firmware Number:	V2.00		
Application Version Number if applicable:			
PIN Support:	Online		
Key Management TDES:	MK/SK		
Key Management AES:	N/A		
Prompt Control:	Vendor-controlled		
PIN Entry Technology:	Physical Keypad		
Functions Provided:	Display,ICCR,MSR,CTLS,PIN Entry,OP,SRED		
Approved Components:			
Approved to meet PCI Device Security Requirements POI V 4.			

This Letter of Approval is effective upon dispatch from PCI SSC, LLC.

Effective Date:	10 Aug 2017
Expiry Date:	30 Apr 2023

PCI Security Standards Council, LLC

By:



Name: Gill Woodcock

Title: Director of Certification Programs, The PCI Security Standards Council

EMV® Type Approval

Contactless Terminal Level 1

PCD Analogue Test Bench and Test Case Requirements

Version 2.6b
December 2016

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Revision Log – Version 2.6b

The following changes have been made to the document since the publication of Version 2.5a. Some of the numbering and cross references in this version have been updated to reflect changes introduced by the published bulletins. The numbering of existing requirements did not change, unless explicitly stated otherwise.

Incorporated changes described in the following Specification Updates:

See section 1.3.2

PCD screen shall be turned ON during testing

New DTE including Transaction Send functions

Change in V₁ and V₂ levels measurement

Test coverage improvements

Other editorial changes:

Minor clarifications and typographical corrections

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1. Using this Manual

1.1. Purpose

The *EMVCo Contactless Type Approval: PCD Analogue Test Bench and Test Case Requirements* manual provides the requirements for procedures and test equipment used for testing the analogue interface PCDs. These requirements are in accordance with the *EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification Version 2.6, March 2016*.

1.2. Audience

This manual is provided to:

- x PCD Vendors
- x Testing laboratories accredited to perform the type approval tests

1.3. Reference Documents

EMV documents are available on the EMVCo web site:

<http://www.emvco.com/approvals.aspx> and
<http://www.emvco.com/specifications.aspx>

1.3.1. Standards Documents

Document	Version Issue Date
ISO/IEC 17025:2005 : General Requirements for the Competence of Calibration and Testing Laboratories	2005
ISO/IEC Guide 98-3:2008 : Uncertainty of measurement — Part 3 — Guide to the expression of uncertainty in measurement, ISO/IEC, corrected version 2010.	2008

1.3.2. Specification Documents

EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification	Version 2.6, March 2016
EMV Contactless Symbol Reproduction Requirements	Version 2.0, 7 November 2016
“Type B Modulation Index”, EMV Specification Bulletin No.183	First edition, December 2016

"Type B Bit Boundaries Tolerance", EMV Specification Bulletin No. 188	First edition, December 2016
EMV Contactless Specifications for Payment Systems – Level 1 – Test Equipment Specifications – PICC Manual	Version 2.1, February 2012
EMV Contactless Specifications for Payment Systems – Level 1 – Test Equipment Specifications – PCD Manual	Version 2.1, February 2012
EMV Contactless Specifications for Payment Systems – Level 1 – Test Equipment Specifications – CMR Manual	Version 2.1, February 2012
<i>EMVCo Type Approval Accreditation Requirements for EMVCo Terminal Type Approval Laboratories.</i>	
<i>IEEE Standard on transitions, Pulses and related Waveforms, IEEE Std 181-2011.</i>	

1.3.3. Laboratory Test Documents

The test documents to be applied by EMVCo accredited laboratories when performing an EMV Contactless Terminal Type Approval Level 1 session are listed in the following document:

**EMVCo Type Approval
Contactless Terminal Level 1
Laboratories Documentation**

Check the last version of this document for any update of the test documents.

1.4. Definitions

In addition of terms already defined in the reference documentation, the following terms are used in this document:

Term	Definition
Analogue Test	Set of tests that check the Radio Frequency of the hardware and software/firmware of the PCD against the EMV Specifications.
Device Test Environment	Part of the Test Environment needed to perform the PCD Type Approval Test, which the Vendor needs to develop and submit to the Test Laboratory at the same time as the Samples.
EMV – TEST CMR	A hardware device qualified as reference equipment which is used with other EMV Test Equipment. Its purpose is to condition and switch signals between its inputs and outputs.
EMV – TEST PCD	A hardware device qualified as reference equipment which is used with other EMV Test Equipment. Its purpose is to simulate a PCD.
EMV – TEST PICC	A hardware device qualified as reference equipment which is used with other EMV Test Equipment. Its purpose is to simulate a PICC.

Term	Definition
Envelope	Waveform connecting positive or negative peaks of oscillating signal.
Landing Plane	The designated surface area of a PCD where a user should place a PICC to obtain a successful transaction.
Loopback Application	Test application that the vendor needs to develop and implement in the Device Test Environment.
Loopback mode	Loopback involves cycling back information in a channel. Any data transmitted through such a channel is immediately received by the same channel. A device is in loopback mode after such a mode has been activated.
Modulation Index	The modulation Index of an amplitude modulated signal is defined as $mi = ([A(t)]MAX - [A(t)]MIN)/([A(t)]MAX + [A(t)]MIN)$ where $A(t)$ is the envelope of the modulated carrier.
Operating Volume	The 3-dimensional space in which the PCD shall reliably communicate with an PICC by means of a magnetic field.
PCD Type Approval	Acknowledgment by EMVCo that a specified PCD within a specified Contactless Product has demonstrated sufficient conformance to the EMV Specification.
PCD Under Test	PCD embedded in the Sample that is actually tested during Type Approval Test.
PCD Vendor	Entity that submits the PCD for PCD Type Approval.
Pre-validation Test	Defined set of tests that checks whether a transaction takes place when a series of PICCs are presented in a series of parameterized positions at the PCD Under Test.
Pre-validation Test Application	Test application that the vendor needs to develop and to implement in the Device Test Environment.
Polling	Sequence during which the PCD sends alternatively WUPA and WUPB commands until a response is received.
Presentation Plane	The plane on the EMV – TEST PICC that faces the EMV – TEST PCD.
Proximity Coupling Device (PCD)	A hardware device that uses inductive coupling to provide power to the PICC and exchange data with the PICC.
Proximity Integrated Circuit Card (PICC)	A hardware device containing an integrated circuit and capable of inductive coupling in the proximity of a coupling device.
Sample	A physical implementation of a PICC or a PCD delivered to the Testing Laboratory for testing.
Set-up	Procedure to follow to prepare EMV Test Equipment before starting a test.

Term	Definition
Terminal	Any device used to interact with a PICC and which operates to the requirements of the EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification. This includes the PCD and may also include other components and interfaces.
Test Bench	A specific test bench as described in the in the EMVCo Contactless Type Approval: PCD Analogue Test Bench and Test Case Requirements manual.
Test Case	Test to verify a requirement at a specific position in the Operating Volume.
Test Code	Code to identify a Test Case.
Test Environment	Environment needed to perform the Test. It is constituted of a Test Bench in combination with a Device Test Environment for PCD Type Approval Test.
Testing Laboratory	A facility accredited by EMVCo for performing EMV Contactless testing of the analogue interface for PICCs and PCDs.
Test Report	Document provided by the Test Laboratory containing the Test results.
Transaction	A sequence of logic interactions that the PICC and the Terminal shall execute as foreseen by the EMV Contactless application. The transaction starts with the first logic message from the PCD to the PICC.

1.5. Notational Conventions

The following abbreviations and notations are used in this document:

Abbreviation	Description
z, r, ϕ , θ	<p>These four coordinates define the position of the PICC in the Operating Volume.</p> <p>The coordinates z, r, and ϕ are the coordinates of the center of the Presentation Plane.</p> <p>The coordinate θ is the angle between the $\phi=0$ axis of the PCD, and the $\phi=0$ axis of the PICC.</p>
(zrf)	Position label indicating the values for coordinates z, r, ϕ .
xx	Value.

1.5.1. Acronyms and Abbreviations

Abbreviation	Description
Abbreviation	Description
A/D	Analogue to Digital
AC CLn	Anticollision Cascade Level n, Type A
ASK	Amplitude Shift Keying
ATQA	Answer To reQuest, Type A
ATQB	Answer To reQuest, Type B
ATTRIB	PICC Selection Command, Type B
BPSK	Binary Phase Shift Keying
CH0	Channel 0
CH1	Channel 1
CLK	Clock
CMR	Common Mode Rejection
DIV	Division
DSO	Digital Sampling Oscilloscope
DTE	Device Test Environment
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EoF	End of Frame
EoS	End of Sequence
EOT	End of Test
etu	Elementary time unit
f _c	Carrier Frequency
f _s	Subcarrier Frequency
HLTA	Halt Command, Type A
HLTB	Halt Command, Type B
I2C	Inter Integrated Circuit
IC	Integrated Circuit
ICS	Implementation Conformance Statement
ID-1	Identification Card Format
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronic Engineers
MSa/s	Mega Samples / Second
PAN	Primary Account Number

Abbreviation	Description
PCD	Proximity Coupling Device
PICC	Proximity IC Card
PUT	PCD Under Test
RATS	Request for Answer to Select, Type A
RF	Radio Frequency
RH	Relative Humidity
rms	Root mean square
SELECT CLn	Select Cascade Level n, Type A
SMA	Subminiature version A
SoF	Start of Frame
SoS	Start of Sequence
TRG	Trigger
TTA	Terminal Type Approval
TTL	Transistor-Transistor Logic
UID	Unique Identifier, Type A
Vpp	Peak to Peak Amplitude Voltage
VSWR	Voltage Standing Wave Ratio
WUPA	Wake UP command, Type A
WUPB	Wake UP command, Type B

1.6. Terminology and Conventions

The following words are used often in this specification and have a specific meaning:

Shall

Defines a product or system capability which is mandatory.

May

Defines a product or system capability which is optional or a statement which is informative only and is out of scope for this specification.

Should

Defines a product or system capability which is recommended.

1.7. Support

For support regarding EMV Contactless analogue testing, refer to www.emvco.com.

2. Requirements for Testing Laboratories

2.1. Overview and Requirements

The EMVCo Contactless Type Approval: PCD Analogue Test Bench and Test Case Requirements manual provides the Test Cases for testing of the analogue interface of terminals.

Analogue interface testing is one of the phases related to EMVCo Terminal Type Approval (TTA).

2.2. Accreditation Requirements

This section describes the requirements for passing full accreditation. Replacing the test equipment by any other devices voids accreditation for testing of the analogue interface for EMV Contactless products.

2.2.1. Using EMV Test Equipment

The EMV Test Equipment comprises the following:

2.2.1.1. EMV TEST Proximity Integrated Circuit Card

The EMV – TEST Proximity Integrated Circuit Card (PICC) emulates the radio frequency (RF) interface of an EMV Contactless card.

2.2.1.2. EMV TEST Proximity Coupling Device

The EMV – TEST Proximity Coupling Device (PCD) emulates the RF interface of a EMV Contactless terminal.

2.2.1.3. EMV TEST Common Mode Rejection Circuit Board

The EMV – TEST Common Mode Rejection (CMR) circuit board aims at conditioning signals and switching them between its inputs and outputs for Test Bench set-ups.

2.2.2. Creation of the Test Bench

Each Testing Laboratory shall create its own proprietary test bench connected to three test devices:

- x The EMV – TEST PICC
- x The EMV – TEST PCD
- x The EMV – TEST CMR

2.2.3. Approval of the Test Bench

The complete test bench shall be approved by EMVCo before the Testing Laboratory is allowed to provide official type approval testing services to PCD vendors.

2.2.4. Test Bench Organization

The Test Bench shall be governed by standard operating procedures. These procedures shall include:

- x Calibration
- x Operator training
- x Test bench operation
- x Test bench maintenance

2.2.4.1. Calibration

Each item of measurement equipment shall be calibrated according to its calibration guidelines once a year.

In any case, calibration shall be performed and documented in compliance with *ISO /IEC 17025:2005 - General Requirements for the Competence of Calibration and Testing Laboratories*.

2.2.4.2. Operator Training

The Testing Laboratory shall ensure operator training to establish the required level of skills and expertise prior to any testing operations.

To ensure the quality of testing, it is recommended that additional training be provided to personnel at least once per year and that close attention be paid to customer requirements.

2.2.4.3. Test Bench Operation

The Testing Laboratory shall prepare and maintain documentation covering all relevant aspects of the design, implementation and operation of its proprietary Test Bench and its interaction with EMV Test Equipment that are necessary for correct operation.

The Testing Laboratory shall operate the Test Bench in accordance with this documentation.

2.2.4.4. Test Bench Maintenance

Each piece of measuring equipment shall undergo regular preventive maintenance, as required by its operating specifications. Written records of such maintenance operations shall be kept by the Testing Laboratory.

In case of test bench failure, corrective maintenance shall take place to repair the test bench. The repaired test bench instruments and accessories shall be restored to their original Testing Laboratory approved standard performance levels. Written records of maintenance operations shall also be kept by the Testing Laboratory.

2.2.5. Accreditation by EMVCo

Only Testing Laboratories that are accredited by EMVCo are authorized to perform EMV analogue interface testing.

2.2.6. Official Compliance to ISO 17025

The Testing Laboratory shall prove to EMVCo that they operate their test bench in compliance with *ISO/IEC 17025:2005 - General Requirements for the Competence of Calibration and Testing Laboratories*.

Also refer to the *EMVCo Type Approval Accreditation Requirements for EMVCo Terminal Type Approval Laboratories* document for additional accreditation requirements.

2.3. Controlled Test Conditions

Analogue Interface testing shall be carried out under controlled test conditions. Refer to ISO/IEC 17025, section 5.3 and 5.4 for details.

2.3.1. Power Supply Conditions

At the beginning of a test session, the Testing Laboratory shall ensure that all electrical power supplies are within the range required for their purpose.

Power Supply voltage shall be measured with calibrated measurement equipment while the Power Supply is connected to the load.

2.3.2. Temperature and Humidity

The normal temperature and humidity conditions for analogue tests should be any convenient combination of temperature and humidity within the following ranges:

- x Temperature: 23°C ± 3°C
- x Relative humidity: 40 % to 60 %

When it is impossible to perform tests under these conditions, a note to this effect, stating the ambient temperature and relative humidity during the tests, shall be added to the test report.

2.3.3. RF Environment

2.3.3.1. Interference Issues

Electromagnetic Interference (EMI) appears in many different forms. The most prominent in Testing Laboratories are the intentional radiators, such as other PCDs under test and other communication devices in the 1 to 100 MHz range of the RF spectrum. In addition, cordless telephones and mobile telephones can be significant interferers in Testing Laboratories.

Another form of interference is EMI radiated from incidental sources: devices and/or systems that are not designed to transmit intentionally. Such interference is also known as broadband emission or "noise," and may be generated by any electronic or electrical device and/or system. This interference may lead to incorrect measurements.

Extraneous noise may radiate from many sources. These are so numerous that it is virtually impossible for all of these suspected devices to be completely managed or controlled. However, efforts must be made to restrict the level of interference signals coming from these sources. The laboratory shall have ISO/IEC 17025 compliant procedures in place to monitor and control the RF environment to ensure that it does not adversely affect the quality of the measurements covered in this document.

2.3.3.2. Managing the RF Environment

The RF spectrum (from 1 to 100 MHz) should be managed by documenting all frequencies as follows:

- x Using a spectrum analyzer for initial benchmarking of the level, nature, and impact of conducted and radiated RF signals that may affect the reliability of measurements.
- x Recording critical frequencies of other Testing Laboratory devices and/or systems.

- x Preventing the intrusion of interfering sources into vulnerable test frequencies (always scan for noise as well as intentional transmitters).
- x Managing this information and knowing which frequencies are in use in the environment.
- x Scanning the Testing Laboratory environment regularly for possible broadband emissions, especially in areas where PCDs are in use or under test.

Note: Equipment such as computers and power supplies should be selected to be as quiet as possible in terms of electro-magnetic disturbances towards the Test bench.

Note: Cables connected to Test Bench equipment shall be as short as possible, ideally less than 50 cm. However, cables connected to computers and power supplies may have a length of up to 100 cm. This allows physical separation of the equipment to minimize coupling of electromagnetic disturbances to sensitive components of the Test Bench.

3. Positioning Conventions and Requirements

3.1. Importance of Positioning

The correct positioning of PICCs and PCDs during testing is of critical importance with EMV Contactless technology, due to the fact that:

- x PCDs come in many forms, such as a standard terminal in a retail location, a card reader in front of a public transport turnstile, a wireless hand-held device, etc.
- x The cardholder can either tap the PICC onto the PCD or simply wave it in front of the PCD.

It is very important to understand the positioning characteristics applied to PICCs and PCDs and the relationship of these positioning characteristics to the Operating Volume. This ensures successful and repeatable testing of the various PICCs and PCDs available on the market.

3.2. Conventions Regarding Positioning

For best accuracy and consistency in testing PCDs, the position of the device must be precisely set. This section explains this using the EMV – TEST PCD and the EMV – TEST PICC during the set-up. The same conventions apply to testing of PCDs in general.

3.2.1. Positioning Characteristics for the EMV TEST PCD

The EMV – TEST PCD clearly identifies where a user should position a PICC to obtain a successful transaction. The designated surface area of a EMV – TEST PCD near which a PICC user should position a PICC to obtain a successful transaction is referred to as the Landing Plane.

Figure 3-1 shows the EMV – TEST PCD positioning characteristics :

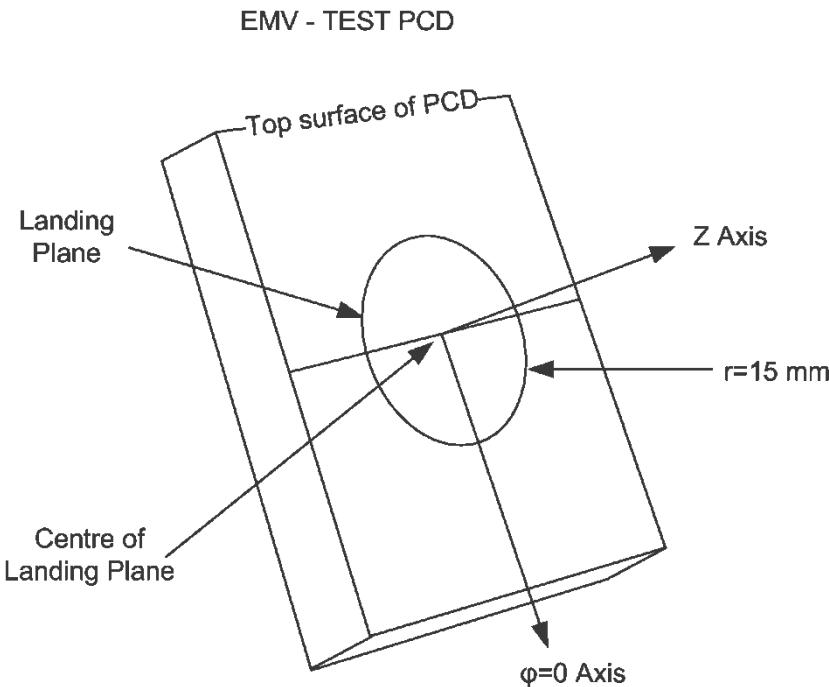


Figure 3-1—EMV – TEST PCD Positioning Characteristics

Note: The conventions used in this chapter relate to Appendix C of the *EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification*.

The Z axis of the EMV – TEST PCD is the axis which passes through the center of the Landing Plane. The Z axis is orthogonal to the Landing Plane and points outwards from the EMV – TEST PCD Landing Plane top surface.

The $\phi=0$ axis is an axis defined on the Landing Plane to support the indication of the orientation of the EMV – TEST PICC versus the EMV – TEST PCD. In theory, the $\phi=0$ axis is the writing direction of the EMV – TEST PCD.

Note: For testing, the PCD under test shall have markings for the center of the Landing Plane (Contactless symbol) and the direction of the $\phi=0$ axis.

3.2.2. Positioning Characteristics for the EMV TEST PICC

When the EMV – TEST PICC is presented over the Landing Plane of the EMV – TEST PCD, the plane on the EMV – TEST PICC that faces the EMV – TEST PCD is called the Presentation Plane.

Figure 3-2 shows the EMV – TEST PICC positioning characteristics :

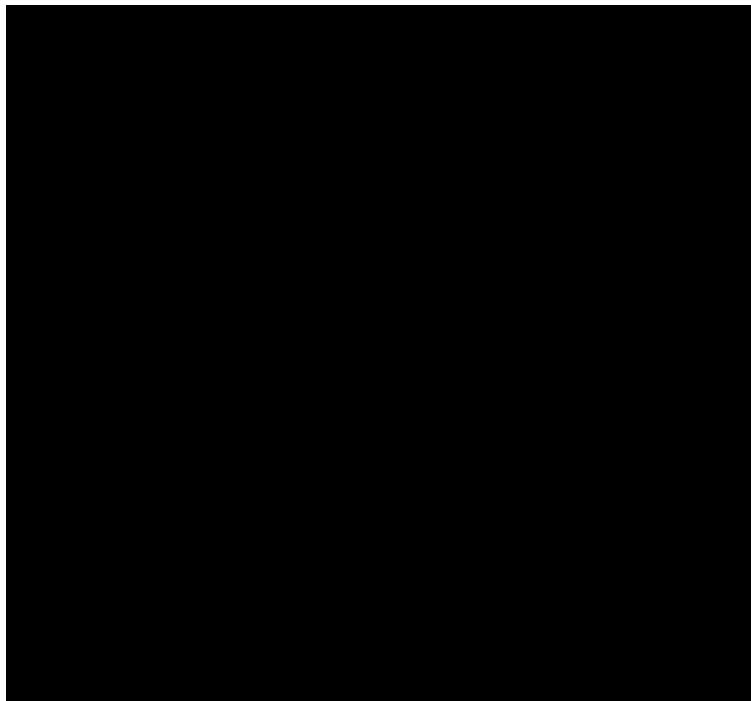


Figure 3-2—EMV – TEST PICC Positioning Characteristics

The Presentation Plane is on the bottom surface of the PICC (dotted lines).

The Z_c axis of the EMV – TEST PICC is an axis which passes through the center of the Presentation Plane. This axis is also orthogonal to the Presentation Plane and points outwards from the EMV – TEST PICC Presentation Plane's bottom surface.

The point on the Presentation Plane where the Z_c axis begins is called the center of the Presentation Plane.

The $\phi_c=0$ axis is the axis defined on the Presentation Plane to identify the orientation of the EMV – TEST PICC versus the EMV – TEST PCD.

3.2.3. Relative Positioning of the EMV TEST PICC and EMV TEST PCD

When an EMV – TEST PICC is placed directly above an EMV- TEST PCD, communication is ideally obtained when both the Landing Plane of the PCD and Presentation Plane of the EMV – TEST PICC are perfectly parallel and aligned. This means that the Z axis of the EMV – TEST PCD passes through the center of the Presentation Plane of the EMV – TEST PICC and that the Z_c axis of the EMV – TEST PICC passes through the center of the Landing Plane of the EMV – TEST PCD.

Figure 3-3 shows the relative positioning of an EMV – TEST PICC and EMV – TEST PCD when both are perfectly aligned and parallel :

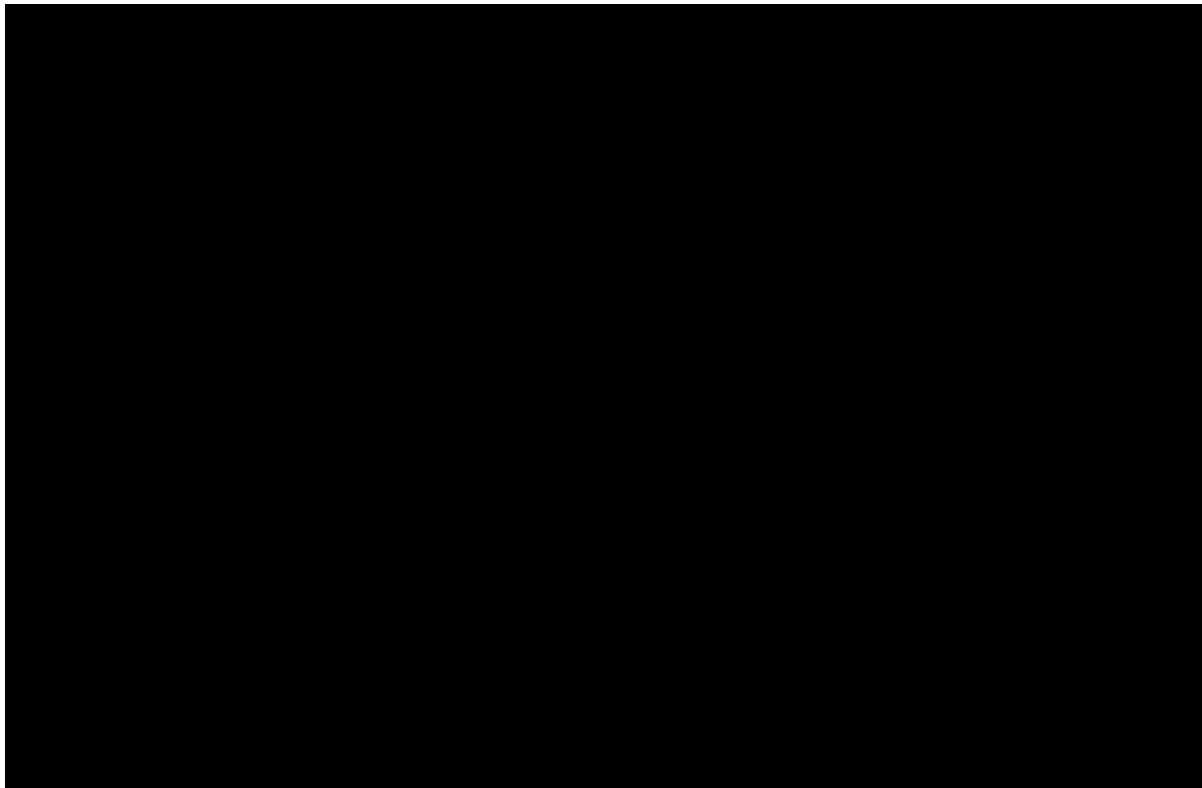


Figure 3-3—Relative Positioning of Perfectly Aligned and Parallel EMV – TEST PICC and EMV – TEST PCD

The position of the EMV – TEST PICC relative to the EMV – TEST PCD is defined with four coordinates (z , r , θ and ϕ), as shown in Table 3-1 :

Coordinate	Description	Unit
z	Coordinate starting at the center of the Presentation Plane: a point along the Z axis.	mm
r	Coordinate starting at the center of the Presentation Plane: a point along the radius defined from the center of the Presentation Plane (for example 25 mm).	mm
	Coordinate starting at the center of the Presentation Plane: this coordinate is explained in section 3.2.3.1	Radians
	Angle defining the orientation of the EMV – TEST PICC with respect to the EMV – TEST PCD. This coordinate is explained in section 3.2.3.2	Radians

Table 3-1—Positioning Coordinate Definitions

3.2.3.1. 'HILQ Angle Coordinate R I 3'

Figure 3-4 shows four possible positions of an EMV – TEST PICC :

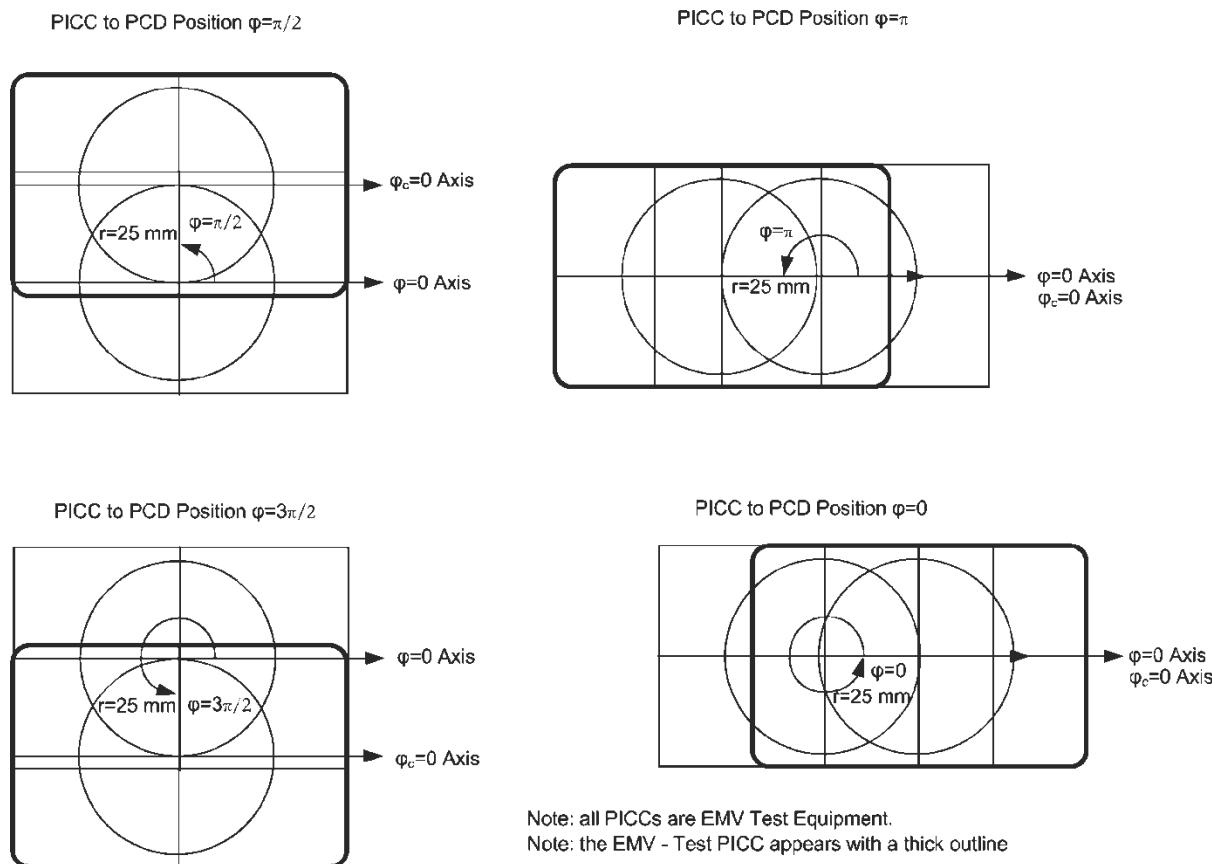


Figure 3-4—Four Possible Positions of an EMV – TEST PICC

This is a typical example where we have chosen to show certain positions of the EMV – TEST PICC. The coordinate values are:

- × The z coordinate is a fixed value for all four positions of the EMV – TEST PICC.
- × The r coordinate is 25 mm for all four positions of the EMV – TEST PICC.
- × The ϕ coordinate varies for all four positions of the EMV – TEST PICC.
- × The θ angle is 0 radians for all four positions of the EMV – TEST PICC. As a result, the EMV – TEST PICC is perfectly parallel to the EMV – TEST PCD in any of the four positions.

In this example, to clearly indicate the effect of the ϕ coordinate, all other coordinates have fixed values. Only the position of the center point of the coordinate changes. The r and ϕ coordinates identify the center of the EMV – TEST PICC that is horizontal to the Landing Plane of the EMV – TEST PCD. When the values for the r and ϕ coordinates vary over their complete range, the entire surface of the EMV – TEST PCD can be swept by the EMV – TEST PICC.

3.2.3.2. ' H I L Q L W L R Q R I W K H \$ Q J O H & R R

When an EMV – TEST PICC is placed directly above an EMV – TEST PCD, valid communication is also required when the Landing Plane of the EMV – TEST PCD and the Presentation Plane of the EMV – TEST PICC do not perfectly match but are rotated with respect to each other.

This means that an angle θ is created between the $\varphi=0$ axis of the EMV – TEST PCD and the $\varphi_c=0$ axis of the EMV – TEST PICC.

Figure 3-5 shows what happens when the relationship between the $\varphi=0$ axis of the EMV – TEST PCD and the $\varphi_c=0$ axis of the EMV – TEST PICC changes :

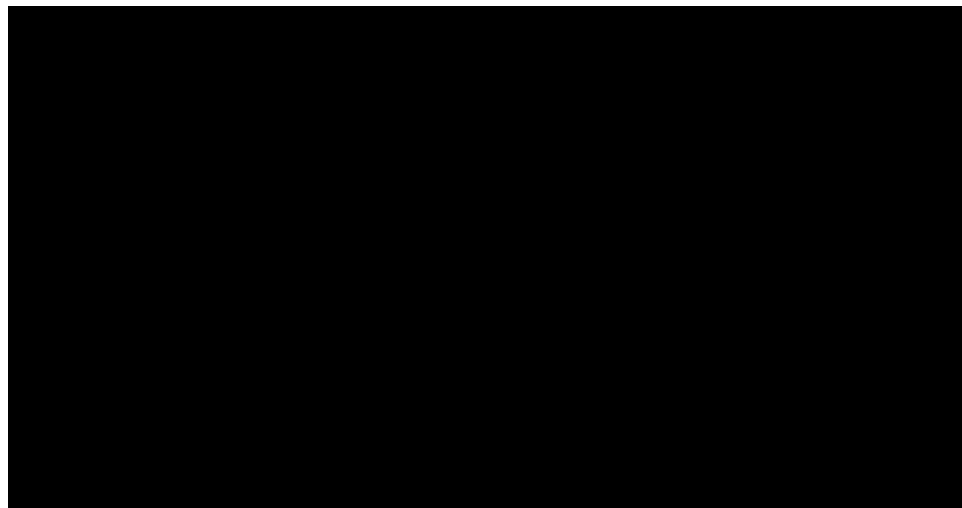


Figure 3-5— & K D Q J H R I W K H 5 H O D W L ~~REQT FCB~~ L S E I
D Q G W K H 3 F TEST PICC [L V R I W K H (

The angle θ expresses the difference between the two axes.

To completely define all acceptable positions for the EMV – TEST PICC, the position of the center point of its Presentation Plane shall be within a defined Operating Volume above the EMV – TEST PCD Landing Plane. The origin of the Operating Volume is the point in the center of the contactless symbol of the EMV – TEST PCD. The Operating Volume is explained in the next section.

3.3. Operating Volume

The Operating Volume defines all the positions for valid testing measurements. The Operating Volume for an EMV – TEST PICC and EMV – TEST PCD is the 3-dimensional space in which the EMV – TEST PCD can reliably communicate with an EMV – TEST PICC by means of a magnetic field. Figure 3-6 shows the Operating Volume :

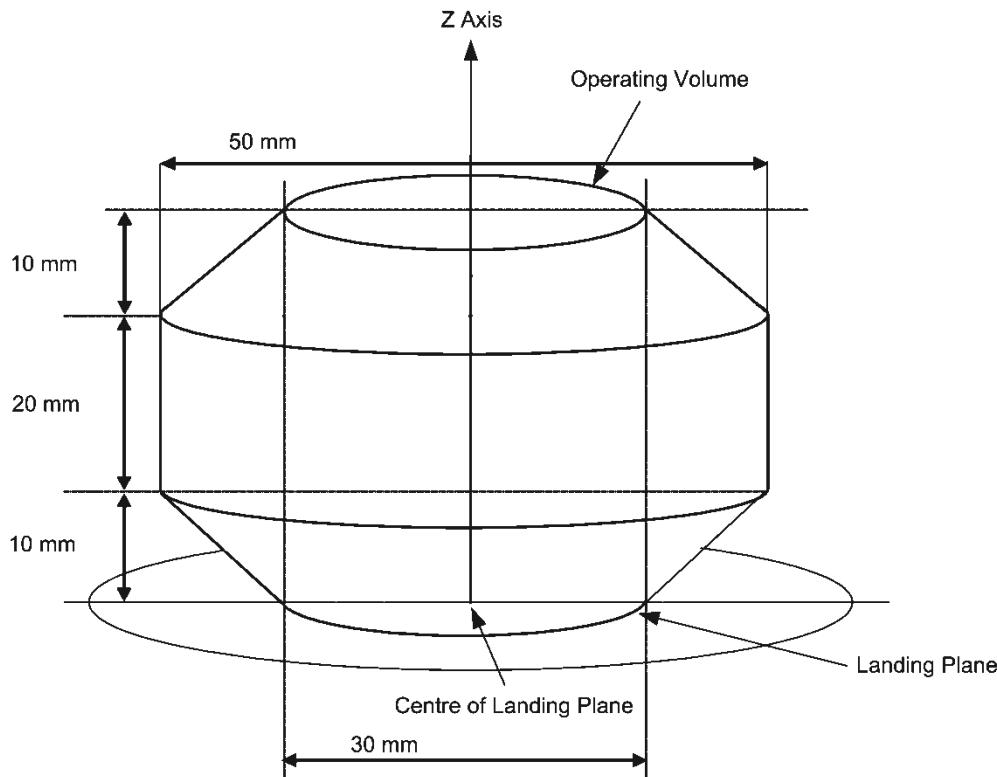


Figure 3-6—Operating Volume

The Operating Volume is measured from the center of the Landing Plane, along an axis perpendicular to the Landing Plane (the Z axis).

The requirements relating to the Operating Volume assume that the EMV – TEST PCD is stationary (fixed Landing Plane) and that the EMV – TEST PICC moves through the Operating Volume.

Note: For further information, see section 2.4 of *EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification*.

Note: The Operating Volume for an EMV – TEST PICC and EMV – TEST PCD also applies to all PCDs under test.

3.4. Positioning During Actual Setups and Tests

Note: From here on in this chapter, the term EMV – TEST PICC refers to the EMV Test Equipment only while the term PCD refers to generic devices including devices used in tests.

The exact position of any EMV – TEST PICC or PCD during setup and testing is defined by two basic aspects:

- x The position of these devices, as explained in section 3.2
- x The Operating Volume, as explained in section 3.3
- x In actual PCD testing, two additional factors shall be taken into account:
 - x The EMV – TEST PICC is not rotated with respect to the PCD.
 - x Target Position Conventions are used for the location points on the positioning tool. This simplifies position labeling.

3.4.1. Target Position Conventions

While four coordinates fully define the exact position of any EMV – TEST PICC, the θ angle is not necessary as it is a fixed value used for all testing operations ($\theta=0$).

The Presentation Plane (z, r, φ) coordinates are the only ones needed.

To further simplify the labels corresponding to the coordinates, the position of any PICC is described with the coordinates of the Presentation Plane (z, r, φ) converted to a position label (z, r, f) using simple identifiers.

Table 3-2, Table 3-3 and Table 3-4 show the equivalences between the values for the z , r and φ coordinates and the identifiers used for labels :

Value of Coordinate <i>z</i>	Value of <i>z</i> Identifiers for Label Points
0 mm	0
10 mm	1
20 mm	2
30 mm	3
40 mm	4

Table 3-2—z Values and Associated z Identifiers

The identifier z is a code for the distance z .

Value of Coordinate r	Value of r Identifiers for Label Points
0 mm	0
15 mm	1
25 mm	2

Table 3-3—r Values and Associated r Identifiers

The identifier r is a code for the distance r.

Value of Coordinate 3	Value of f Identifiers for Label Points
0	0
$\pi/2$	3
π	6
$3\pi/2$	9

Table 3-4— 3 9 D O X H V D Q G \$ V V R F L D W H G

The identifier f is a code for the angle ϕ .

For example, Figure 3-1 shows nine identifiers corresponding to the label points in a plane of the target position for a given value of z with respect to the Landing Plane of the PCD :

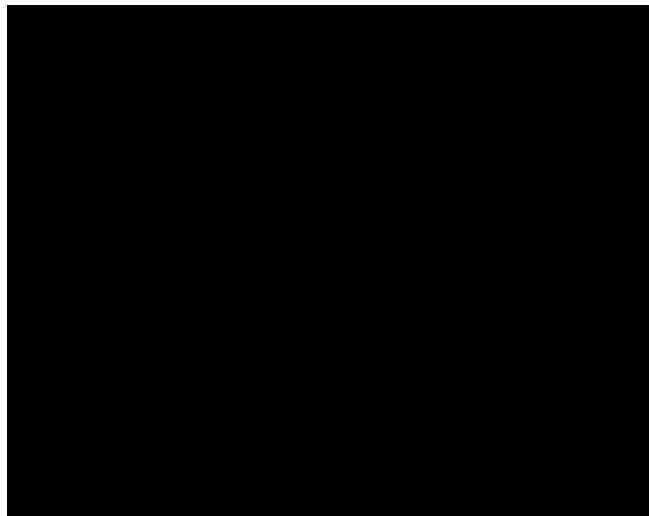


Figure 3-7 Label Points in a Plane of the Target Position

Table 3-5 shows how the various points defined by a label point identifier match the previously described EMV – TEST PICC positions :

Label Point Identifier	3 9 D O X H
z00	—
z10, z20	0
z13, z23	$\pi/2$
z16, z26	π
z19, z29	$3\pi/2$

Table 3-5— / D E H O 3 R L Q W , G H Q W L I L H U V D

3.4.2. Summary

For the purpose of the tests described in this manual, the PCDs under test shall be used with these recommendations:

- x The Presentation Plane of an EMV – TEST PICC shall always be parallel to the Landing Plane of the PCD.
- x The EMV – TEST PICC is not rotated with respect to the PCD.

3.5. Positioning Accuracy

The accuracy of the positioning during the test session shall be as follows:

- x Accuracy on z and r = ± 1 mm
- x Accuracy on ϕ and θ = ± 0.1 radian

A non-metallic positioning tool shall be used to avoid influencing electro-magnetic fields.

4. EMV Test Equipment

4.1. EMV TEST PICC

4.1.1. Description

Figure 4-1 shows the EMV – TEST PICC, Version 2.1 :

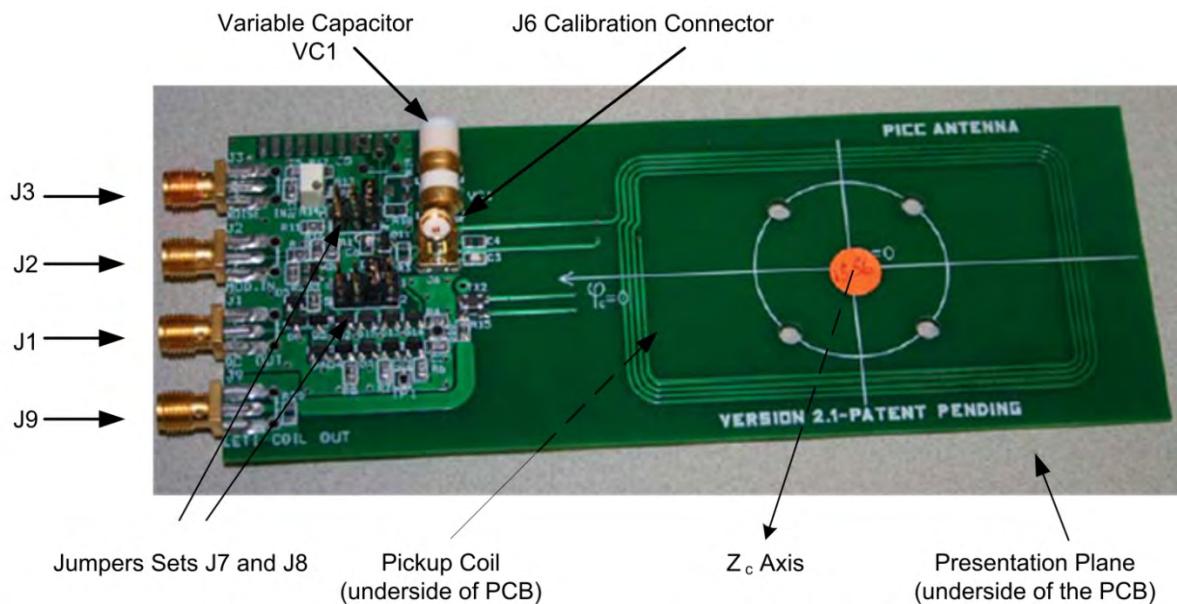


Figure 4-1 EMV – TEST PICC, Version 2.1

The EMV – TEST PICC comprises the PICC pickup coil (based on a design by the LETI laboratory) and the EMV – TEST PICC antenna.

The EMV – TEST PICC antenna has a circuit that tunes the antenna, rectifies the RF signal, provides a series of load circuits and allows load modulation of the RF field.

On the underside of the EMV – TEST PICC, a C-shaped PICC pickup coil allows signal acquisition through a $50\ \Omega$ SMA socket connector (J9). Section 4.1.2 explains the underside of the EMV – TEST PICC.

All signal connections are made using a set of $50\ \Omega$ SMA socket connectors at the end farthest away from the coils.

Note: EMVCo currently does not allow the replacement of a qualified EMV Test PCD or EMV Test PICC unit by a spare unit.

4.1.2. Electrical Connectivity

The EMV – TEST PICC features 8 connectors: two inputs, two outputs, and four additional output connectors. Of the four additional output connectors, only one is used for calibration purpose; the others are not currently used.

The features and functions of the input connectors are shown in Table 4-1 :

Input Connectors	Description
J2	Allows sending PICC emulated data to the PCD being tested.
J3	Not used with the EMV – TEST PICC. Do not connect anything to it.

Table 4-1—EMV – TEST PICC Input Connectors

Note: All inputs are internally terminated with 50Ω loads.

The features and functions of the output connectors are shown in Table 4-2 :

Output Connectors	Description
J1	Allows measurement of the field strength of a PCD. This field strength is measured into a high impedance load with a passive or active probe.
J9	Allows sensing the PCD signal through the PICC pickup coil.

Table 4-2—EMV – TEST PICC Output Connectors

The features and functions of the additional connectors are shown in Table 4-3 :

Output Connectors	Description
J6	Allows calibration and calibration verification of the EMV – TEST PICC. The method for calibration verification is described later in this document as well as in the EMV – TEST PICC manual.
J3, J5, J5B.	Not currently used.

Table 4-3—EMV – TEST PICC Additional Connectors

Note: Do not make any connection to J6 during testing as its ground is not connected to local ground.

4.1.3. Positioning Characteristics

Figure 4-2 shows the underside of the EMV – TEST PICC, Version 2.1 :



Figure 4-2—Underside of the EMV – TEST PICC, Version 2.1.

The C-shaped PICC pickup coil forms the presentation plane. The central point of the presentation plane is the geometric center of the C-shaped PICC pickup coil of the EMV – TEST PICC.

The orientation of the Z_c axis is indicated in Figure 4-1.

The $\varphi_c=0$ axis is the direction from the center of the presentation plane towards the edge with the connectors.

4.1.4. On-board Adjustment

Note: Tuning the VC1 capacitor changes the calibration status of the EMV – TEST PICC. It shall only be done if allowed by EMVCo.

On the EMV – TEST PICC, three parameters are adjustable:

1. Variable capacitor (VC1) is used to adjust the EMV – TEST PICC resonant frequency.
2. Jumper set J7 is used to adjust the EMV – TEST PICC load. The jumper positions determine how many pairs of diodes are placed in series with the stepped load :

Output Connectors	Description
Removed	4 diode pairs are in series with the load.
1 – 2	3 diode pairs are in series with the load.
1 – 3 (default setting)	2 diode pairs are in series with the load.
1 – 4	1 diode pair is in series with the load.
1 – 5	No diode pairs are in series with load.

Table 4-4—Jumper Set J7 Settings

3. Jumper set J8 is used to adjust the EMV – TEST PICC load type :

Jumpers	Provides
Removed	No load
1 – 2	Fixed load 330 Ω
1 – 3	Alternate fixed load – not used in the current version
1 – 4 (default setting)	Non-linear load

Table 4-5—Jumper Set J8 Settings

Note: Unless otherwise specified, jumper set J7 shall be used to select 2 diode pairs in series with the load. Jumper set J8 shall be used to enable the non-linear load.

4.2. EMV TEST PCD

4.2.1. Description

Figure 4-3 shows the EMV - PCD, Version 1.2 :

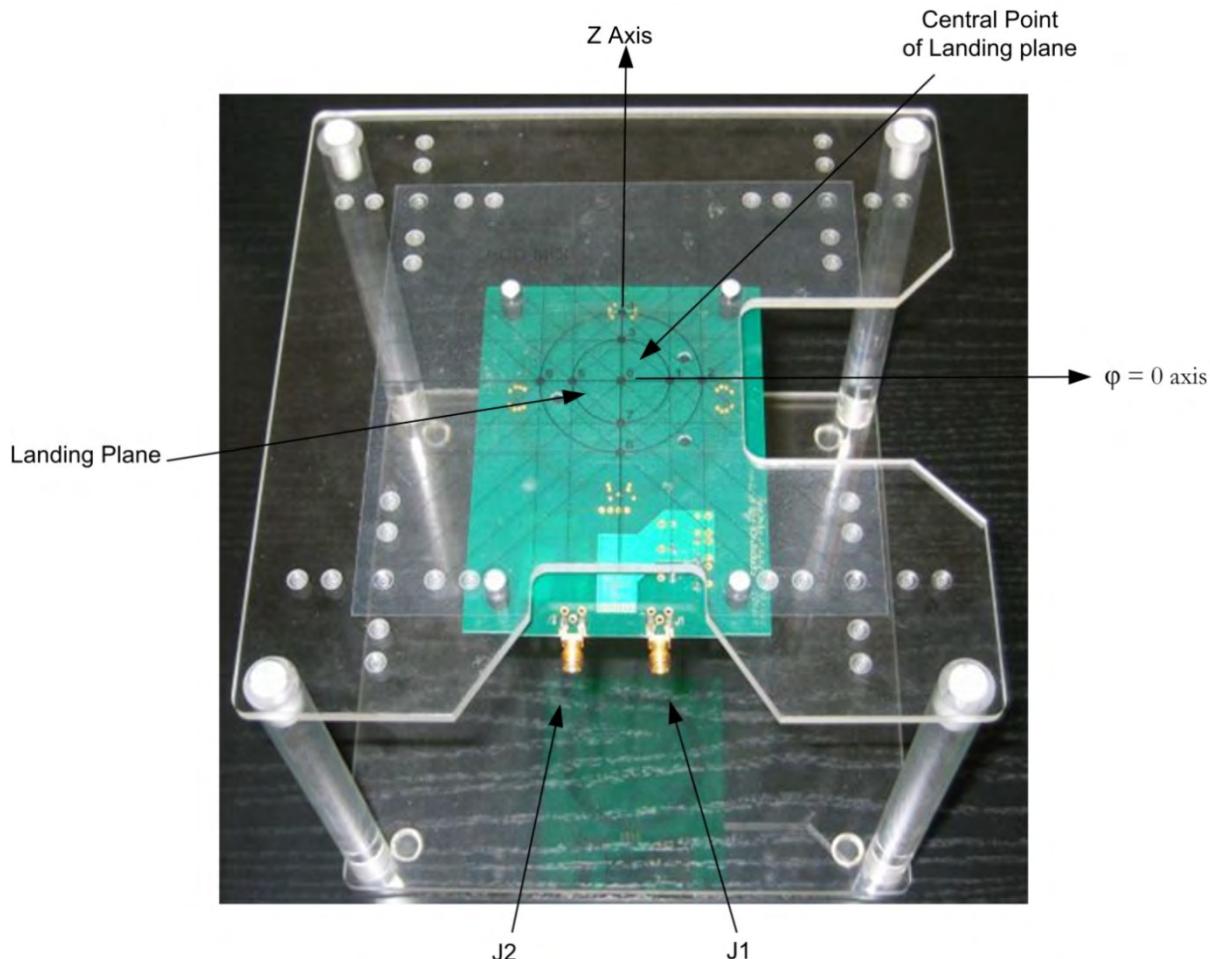


Figure 4-3—EMV – TEST PCD, Version 1.2

The EMV – TEST PCD comprises a PCB and a stand.

The PCB forms the antenna and has two 50Ω SMA sockets for connecting to test equipment.

The stand elevates the PCB above the bench, which provides a defined separation for the Landing Plane and incorporates a set of location points for accurate positioning of the EMV – TEST PICC or PICC under test.

Note: To ensure the best spatial repartition of the RF field, the EMV Test PCD board shall be mounted under its Perspex® stand with components side downwards, as shown on the above picture.

Note: EMVCo currently does not allow the replacement of a qualified EMV Test PCD or EMV Test PICC unit by a spare unit.

4.2.2. Electrical Connectivity

The EMV – TEST PCD features two connectors :

Connectors	Description
J1	Allows reception of the PCD carrier. When the EMV -Test PCD is calibrated, the input impedance at J1 is 50 Ω at 13.56 MHz when no PICC is in the field of the PCD.
J2	Allows signal acquisition by sending out a 1 Ω source impedance output signal. J2 shall be connected to equipment featuring 50 Ω input impedance.

Table 4-6—EMV – TEST PCD Connectors

4.2.3. Positioning Characteristics

Positioning characteristics are defined with respect to the landing plane:

- x The landing plane is the circle on the Perspex® stand above the EMV – TEST PCD antenna.
- x The central point of the landing plane is the geometric center of the circle drawn on the Perspex.
- x The Z axis of the EMV – TEST PCD is the axis through the central point of the landing plane and pointing from the antenna PCB up through the face of the Perspex cover.
- x The $\varphi=0$ axis of the EMV – TEST PCD is the axis through the central point of the landing plane, parallel to the line formed by connectors J1 and J2, and oriented in the direction of J1.

4.2.4. On-board Adjustment

The two variable capacitors (VC1 and VC2) on the EMV – TEST PCD set the input impedance and the resonant frequency. The PCB is always mounted as shown in Figure 4-3. Capacitors VC1 and VC2 are mounted on the component side of the PCB.

Note: Tuning the VC1 and VC2 capacitors changes the calibration status of the EMV – TEST PCD. It shall only be done if allowed by EMVCo.

4.3. EMV TEST Common Mode Rejection Circuit Board

4.3.1. Description

The EMV – TEST CMR is used to condition and switch signals between its inputs and outputs. This allows added flexibility in the Test Bench.

Figure 4-4 shows the EMV – TEST Common Mode Rejection circuit board, Version 2.1 :

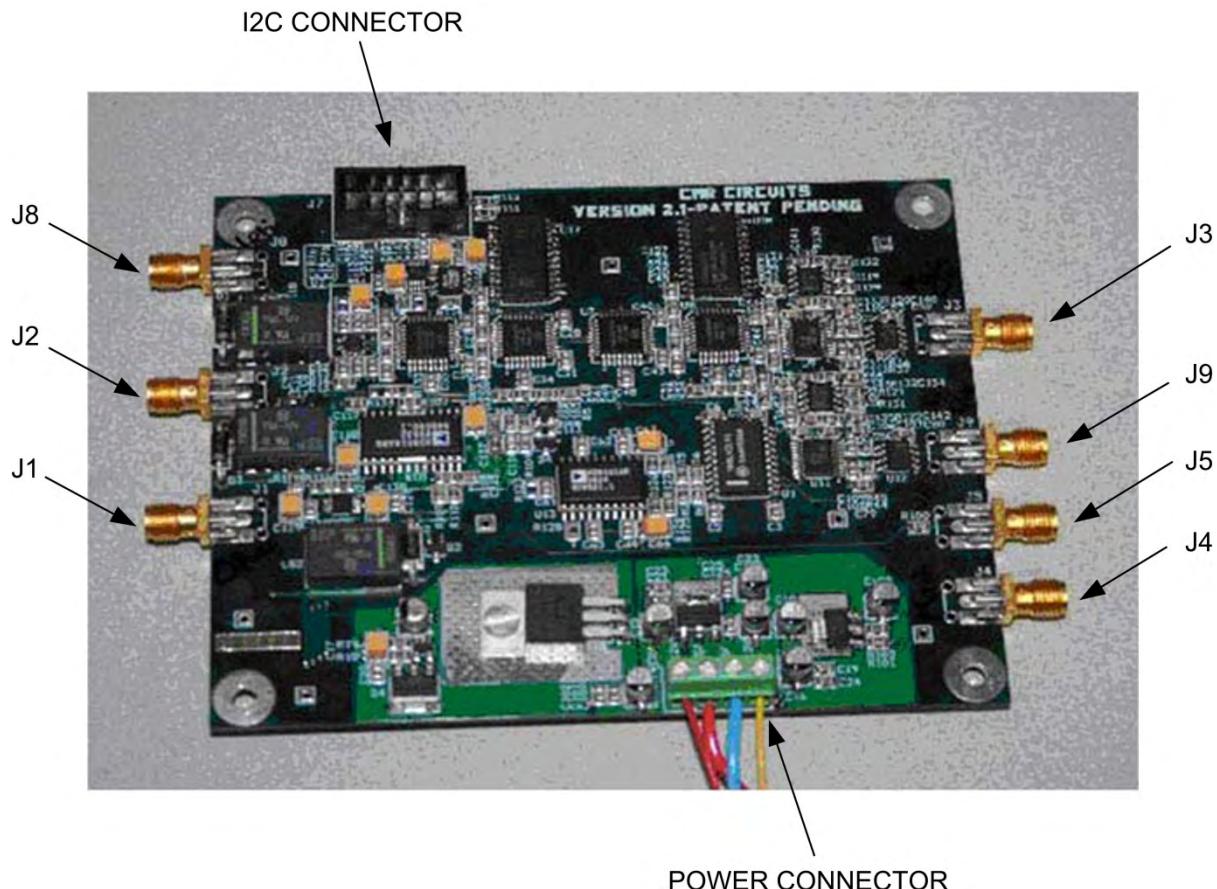


Figure 4-4—EMV – TEST CMR Circuit Board, Version 2.1

The EMV – TEST CMR circuit board is the interface between EMV – TEST PCD output or the EMV – TEST PICC pickup coil output and the test equipment.

Note: The EMV – TEST CMR should be switched on five minutes before using it and should be left powered up during a test session.

Laboratories are allowed to use a spare EMV Test CMR device for Type Approval testing, provided that the three conditions below are met :

1. The spare unit has a valid calibration certificate, issued by an authorized entity less than one year before;
2. The spare unit is used for the whole test session, from the initial verifications to the final test;

3. The specific gain of the spare unit is used during all relevant tests, in place of the gain from the replaced unit.

Note: EMVCo currently does not allow the replacement of a qualified EMV Test PCD or EMV Test PICC unit by a spare unit.

4.3.2. Electrical Connectivity

Connectors

The EMV – TEST CMR circuit board features three input connectors and four output connectors.

All signal connectors on the EMV – TEST CMR circuit board are $50\ \Omega$ SMA socket connectors.

The features and functions of the input connectors are shown in Table 4-7:

Input Connectors	Description
J1	Receives an external clock signal which is neither J2 nor J8. This input presents a $50\ \Omega$ load to the source regardless of which input is selected via the relays. For normal operation, this input signal should be up to $\pm 2\ V$ for normal operation and shall not exceed $\pm 3\ V$.
J2	Receives the signal coming from the EMV – TEST PCD antenna. This input presents a $50\ \Omega$ load to the source regardless of which input is selected via the relays. For normal operation, this input signal should be up to $\pm 2\ V$ for normal operation and shall not exceed $\pm 3\ V$.
J8	Receives the signal coming from the EMV – TEST PICC pickup coil. This input presents a $50\ \Omega$ load to the source regardless of which input is select via the relays. For normal operation, this input signal should be up to $\pm 2\ V$ for normal operation and shall not exceed $\pm 3\ V$.

Table 4-7—EMV – TEST CMR Input Connectors

Note: All these inputs are internally connected to $50\ \Omega$ loads.

The features and functions of the output connectors are shown in Table 4-8:

Output Connectors	Description
J3	<p>Recover the clock signal from a signal coming from either J1, J2 or J8.</p> <p>The recovered clock will be delayed as required by the delay lines. This is explained in section 4.3.3</p>
J4	<p>Recover a copy of an input signal with almost unity gain.</p> <p>In normal use, the output will be up to 1.5 V peak to peak without using the clipper block.</p> <p>Note: the input signal can also be amplified using the clipper block, but this option is not used in the current version of the document.</p>
J5	<p>Samples and holds an input signal.</p> <p>Note: Do not use this connector for PCD or PICC capability testing.</p>
J9	<p>Sends a clock signal for the sample and hold feature.</p> <p>Note: Do not use this connector for PCD or PICC capability testing.</p>

Table 4-8—EMV – TEST CMR Output Connectors

Note: All CMR board outputs shall be connected to equipment which features 50 Ω input impedance.

Note: When not used, J4 shall be connected to a 50 Ω load.

Relays

The EMV – TEST CMR circuit board features three relays.

The features and functions of the relays are shown in Table 4-9:

Output Connectors	Description
Relay 1	<p>Selects the EMV – TEST CMR input between J2 (signal coming from EMV – TEST PCD output J2) and J8 (signal coming from the EMV – TEST PICC output J9).</p>

Output Connectors	Description
Relay 2	Selects which input signal will be used to derive the clock signal that is sent to the Acquisition Device (either the chosen input or the signal coming from the signal generator producing the carrier frequency).
Relay 3	Selects if the EMV – TEST CMR input is sent via a buffer amplifier or if the signal has been processed via the clipper amplifier. Note: Do not use the clipper amplifier in the current version of the document.

Table 4-9—EMV – TEST CMR Relay Features

Delay lines

The delay lines consist of four delay chips in series. The four delay lines are organized in two pairs of two chips referred to as DL1+DL2 and DL3+DL4. Note that the output from DL3+DL4 includes any delay introduced by DL1+DL2. Each pair of delay lines provides a programmable delay of between 4.4 ns and 24.4 ns.

4.3.3. Other Common Mode Rejection Circuit Board Connections

In addition, two more connection groups are available:

- x Four power terminals (12 V, 5 V, 0 V and -12 V) requiring an external regulated Power Supply.
- x An Inter Integrated Circuit (IIC), also known as I2C connector which can receive control data from an external source.

4.3.4. Common Mode Rejection Circuit Board Control

The EMV – TEST CMR circuit board shall be controlled through the I2C connector. The controls affect three relays and four delay lines. Table 4-10 shows the EMV – TEST CMR functions and associated controls :

Function	Settings	Description	Controlled by
Input	J2, J8	Input signals into the EMV – TEST CMR.	Relay
Output	J4	Output signals from the EMV – TEST CMR.	Uncontrolled (permanently available)
Clock	J1, J2, J8	J1: A clock signal based on an external clock signal. J2, J8: A clock signal based on a recovered clock signal depending on the input signal.	Relay
Main clock selection	DL1 + DL2 DL3 + DL4 DL1 + DL2 (180 degrees) DL3 + DL4 (180 degrees)	Sets the delay of the main clock.	Delay lines and Multiplexers
S/H clock selection	DL1 + DL2 DL3 + DL4 DL1 + DL2 (180 degrees) DL3 + DL4 (180 degrees)	DL1 + DL2 + DL3 + DL4 sets the delay of the sample and hold clock. As the sample and hold clock is not used in the tests described in this document, the delay lines shall always be set to DL1 + DL2.	Delay lines and Multiplexers

Table 4-10—EMV – TEST CMR Functions and Associated Controls

5. Requirements for the Test Bench

5.1. Overview

The proprietary Test Bench is connected to the EMV Test Equipment provided by EMVCo. Figure 5-1 shows a block diagram of the Test Bench :

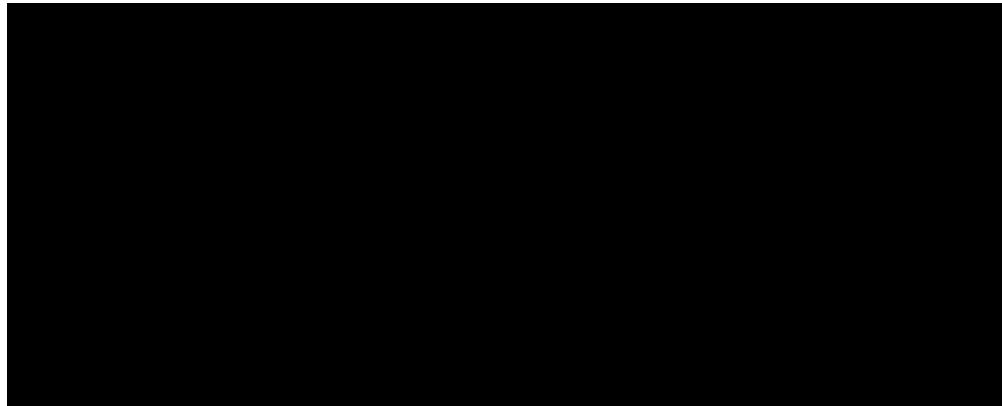


Figure 5-1—Block Diagram of the Test Bench

Note: The term proprietary refers to a Test Bench assembled using equipment chosen by the Testing Laboratory as meeting all requirements described in this chapter.

There are two steps in using the Test Bench:

- x Set-up of the EMV Test Equipment.
- x Test PCDs from a vendor.

5.1.1. Test Bench Functions for Set-up

Figure 5-2 shows the test functions of the EMV Analogue Test Bench used during the setup of the EMV Test Equipment:

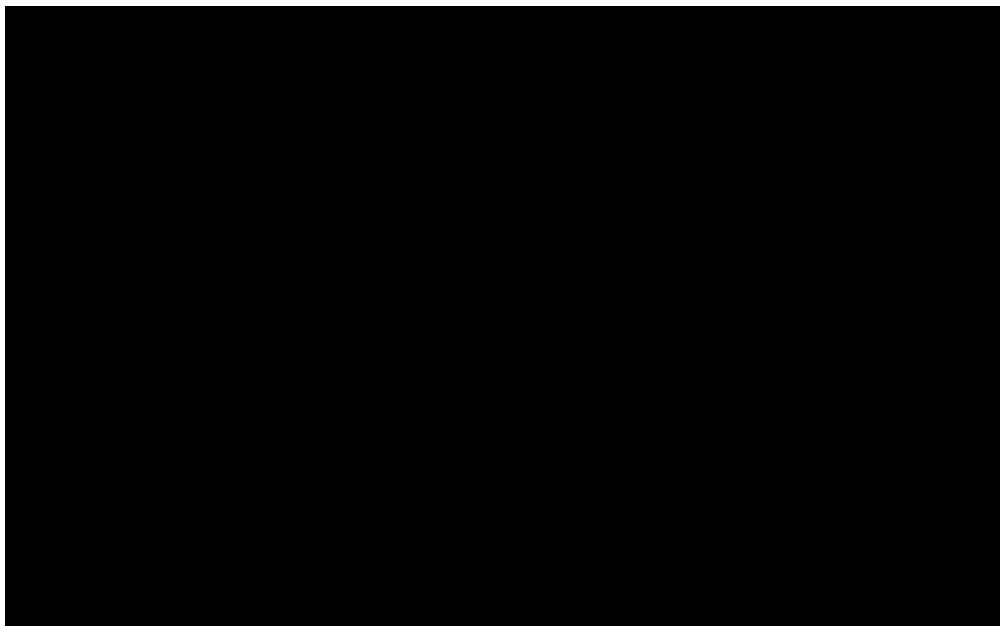


Figure 5-2—Test Functions of the EMV Analogue Test Bench

5.1.1.1. PICC Emulation

Emulation of the PICC consists in a simulation of the answer of an EMV Contactless compliant PICC. Emulation should be representative of a real PICC therefore different load modulation amplitudes are generated to provide representative emulation.

5.1.1.2. Signal Acquisition and Measurement on EMV TEST PICC

The Test Bench, using the EMV – TEST PICC, measures PCD parameters such as magnetic field strength, waveform characteristics and carrier frequency.

5.1.1.3. EMV TEST CMR Control

For tests using the EMV – TEST CMR, the Test Bench controls the various configuration settings of the EMV – TEST CMR using the EMV – TEST CMR control software.

5.1.1.4. PCD Emulation

The Test Bench, used with the EMV – TEST PCD, emulates a real PCD. Various characteristics of the emulated PCD such as magnetic field strength and carrier frequency can be adjusted.

Note: PCD Emulation is only used during set-up.

5.1.1.5. Signal Acquisition and Measurement on the EMV TEST PCD

The Test Bench used with the EMV – TEST PCD measures PICC parameters such as load modulation.

Note: Signal Acquisition and Measurement on EMV – TEST PCD is only used during set-up.

5.1.2. Test Bench Functions for Testing

When testing PCDs from a vendor, a PCD under test replaces the EMV – TEST PCD. Figure 5-3 shows a block diagram for PCD testing:



Figure 5-3—Block Diagram for PCD Testing

5.2. Test Bench Functions

This section describes the test functions of the Test Bench. Each test function description comprises its purpose (including any necessary parameters and signal names), the requirements to meet the purpose and a description of the functionalities used to meet the requirements.

While the test bench functions are individually described, the Testing Laboratory does not have to implement each function as an individual entity. The Testing Laboratory may integrate functions provided that the overall test bench meets the performance requirements.

5.2.1. PICC Emulation

The PICC emulation function sends an emulated PICC answer to the PCD under test. The EMV – TEST PICC uses this signal to modify the load it presents to the electromagnetic field generated by the PCD. Using with various load modulation amplitudes, PCD receptivity can be evaluated.

5.2.1.1. Purpose

The PICC emulation function delivers an electrical signal to input J2 of the EMV – TEST PICC. This signal is called the PICC Analogue Transmission signal. Adjusting the voltage level of the PICC Analogue Transmission signal changes the load modulation amplitude.

5.2.1.2. Requirements

The PICC emulation function shall feature the following quality characteristics for the PICC Analogue Transmission signal:

- x The logic content and the timing of the Analogue Transmission Signal (implementing the PICC emulation function) shall be compliant to the one defined in Appendix C.
- x The amplitude shall be adjustable from 0.5 to 5 V.
- x The overshoots shall not exceed 5 % of the amplitude.
- x The rise and fall times shall not exceed 30 ns.
- x When measured on the connector J2 of the EMV – TEST PCD, load modulation shall be adjustable with a resolution $\leq \pm 1$ mV.
- x The output impedance shall be nominally $50\ \Omega$ to match the $50\ \Omega$ input impedance on input J2 of the EMV – TEST PICC.
- x The PICC answer shall be sent with a delay adjustable by steps of 20 ns or better.
- x The emulated PICC responses shall be synchronized with the PCD commands to provide the required timing interval according to Appendix C. The accuracy shall be $\pm 1/f_C$ or better.
- x The PICC emulation function shall deliver a trigger to the Acquisition Device (not shown in Figure 5-4).

5.2.1.3. PICC Emulation Implementation

Figure 5-4 shows the conceptualized block diagram for PICC emulation:

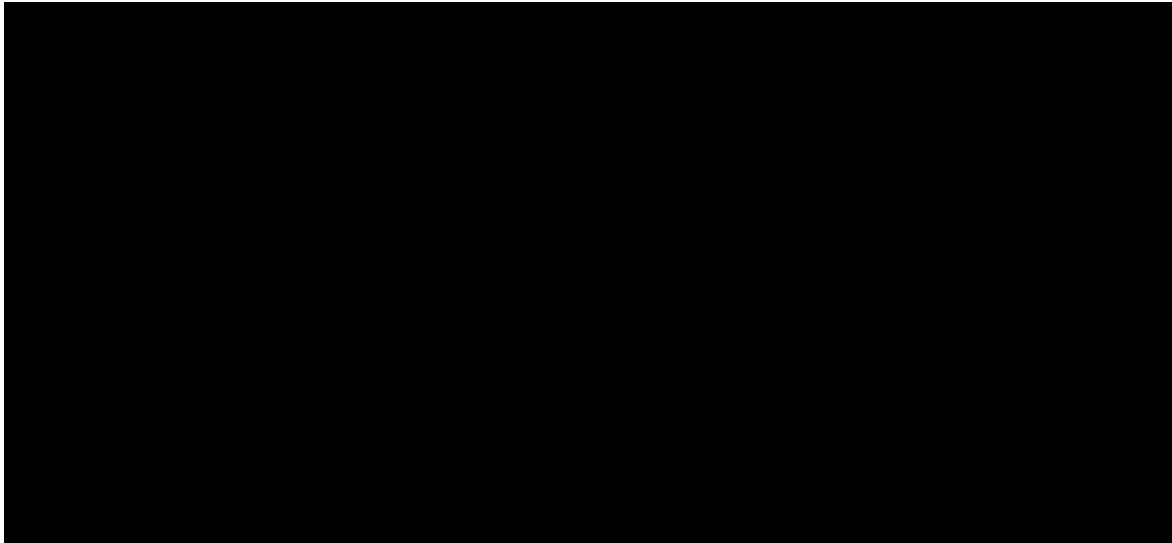


Figure 5-4—Block Diagram for PICC Emulation

The PICC emulation function comprises two functional blocks, these are:

- x PICC Signal Generation
- x PICC Synchronization System

PICC Signal Generation

The PICC Signal Generation system sends PICC coding to the PCD under test. It comprises:

- x PICC Coding Generator
- x Load Modulation Adjustment

PICC Coding Generator

The PICC Coding Generator produces a digital signal that carries the information for the bit-level coded answer of the PICC. One logic state encodes an absence of the load while the other logic state encodes the presence of the load. This signal is called the PICC Digital Transmission signal.

The basic performance criteria of the PICC Coding Generator shall be the following:

- x Timing resolution: 20 ns or better
- x Overall accuracy of $f_c/16$ subcarrier < 10 ppm
- x Low jitter ≤ 1 ns

Load Modulation Adjustment

The Load Modulation Adjustment system varies the signal voltage coming from the output of the PICC Coding Generator to set the load modulation amplitude at the level required by the test. The output signal is called the PICC Analogue Transmission signal.

The basic performance criteria of the Load Modulation Adjustment shall be the following:

- x The voltage output shall be adjustable from 0.5 to 5 V.

Note: The PICC Signal Generation function may be implemented by a single device that combines PICC Coding Generation and a Load Modulation Adjustment. The

presentation of these two functionalities as separate is only used for the sake of clarity in the requirements.

PICC Synchronization System

The PICC Synchronization System provides a trigger to the PICC Coding Generator at the end of the PCD under test command. This signal is called the PCD Synchronization signal.

The basic performance criteria of the PICC Synchronization System shall be the following:

- x The synchronization system shall be capable of detecting all the PCD commands and shall deliver a trigger signal in a format suited to the PICC Coding Generator and synchronized to the end of sequence (EoS) of the PCD frame.
- x The trigger signal shall be provided to the PICC Coding Generator in sufficient time for the PICC Coding Generator to emulate PICC responses within the timing requirements of Appendix C.
- x At the end of a PCD command, the PICC answer following the trigger pulse shall be sent with a delay adjustable by steps of 20 ns or better.
- x The synchronization system shall not affect measurements.
- x The synchronization device antenna shall be placed at the farthest convenient position that maintains consistent readings and does not influence the measurement. This position must be identical throughout testing with the standard positioning tool.

Table 5-1 shows a summary of the signal name and its characteristics :

Signal Name	Description	Measured at	Built From
PICC Analogue Transmission	Provides a signal that the EMV – TEST PICC uses to modify the load on the PCD electromagnetic field	Input J2 of the EMV – TEST PICC.	<ul style="list-style-type: none">x PCD Synchronizationx PICC Digital Transmission

Table 5-1—Summary of the Signal Name and its Characteristics

5.2.2. Signal Acquisition and Measurement on the EMV TEST PICC

The signal acquisition and measurement on the EMV – TEST PICC uses the signals available on the J9 and J1 connectors of the EMV – TEST PICC.

5.2.2.1. Purpose

This acquisition and measurement system serves the following purposes:

- x Measure the field strength generated by the PCD under test.
- x Measure the critical parameters of the waveform generated by the PCD under test.

5.2.2.2. Requirements

This acquisition and measurement system shall feature the following characteristics:

- x The equipment shall be able to provide a graphic display of the digitally formatted signal for visual analysis. The signal capture shall be over at least 20 ms.
- x The equipment shall be able to display all small envelope variations (greater than 5 mV) that allow the evaluation of monotonicity.
- x The equipment should self-trigger on Type A and Type B commands. If the equipment is not capable of self-triggering on Type A and Type B commands, the Testing Laboratory shall ensure that the external triggering (with a DSO or other equipment) does not affect the measurements.
- x The equipment shall be able to measure the following:
 - o The mean amplitude of a signal ranging from 0 to 10 V, averaged over not less than 10 µs, with DC and AC components, within a 30 MHz bandwidth and with an accuracy of $\pm 2\%$ or better.
 - o The nominal frequency of 13.56 MHz $\pm 7\text{ kHz}$ with an accuracy of $\pm 100\text{ Hz}$ or better.
 - o A timing resolution on the waveform signal of at least one cycle of the carrier frequency.
 - o The modulation index of a Type B PCD signal with an accuracy of $\pm 0.5\%$ (absolute precision).
- x The equipment shall convert the analogue signal to a digital format as early as possible in the process. Conversion may be peak detection or asynchronous sampling.

Note: The PICC Signal Generation function may be implemented by a single device that combines PICC Coding Generation and a Load Modulation Adjustment. The presentation of these two functionalities as separate is only used for the sake of clarity in the requirements.

Note The equipment may decode the digital bit string sent by the PCD, but the Device Test Environment (DTE) provided with the sample to check PCD receptivity can be used.

Note The use of a low-pass filter fitted between the PICC and the EMV – TEST CMR is highly recommended. The filter shall feature less than 1 dB attenuation at 20 MHz and more than 40 dB attenuation at 40 MHz.

5.2.2.3. Signal Acquisition and Measurement on the EMV TEST PICC Implementation

The signal acquisition and measurement on EMV – TEST PICC comprises two functional blocks:

- x Power Parameter Acquisition and Measurement device
- x AC Parameters Acquisition and Measurement device

Figure 5-5 shows the functional blocks for signal acquisition/measurement on the EMV – TEST PICC:

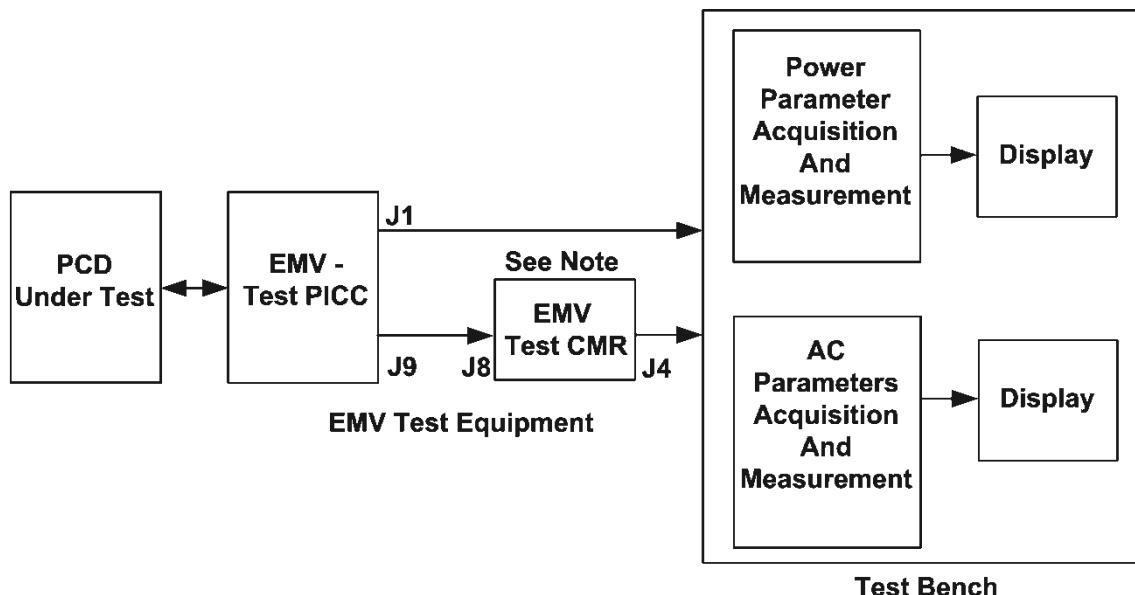


Figure 5-5—Block Diagram for Signal Acquisition/Measurement on the EMV – TEST PICC

Note: The EMV – TEST CMR control is explained in section 5.2.3, and the EMV – TEST CMR is described in Chapter 4.

Power Parameter Acquisition and Measurement

The power parameter acquisition and measurement device determines the DC voltage at the output of the J1 connector of the EMV – TEST PICC. This signal is called the PICC Analogue Power Sensing signal.

The basic performance criteria of the power parameter acquisition and measurement device shall be the following:

- x The input impedance of the acquisition system shall present a high impedance ($\geq 1 \text{ M}\Omega$ and less than 15 pF for a frequency between 0 and 30 MHz) to the EMV – TEST PICC output J1.
- x At least 10 mV resolution in the range 0 - 10 V
- x Minimum sampling rate: 100 MSa/s
- x Automated calculation of the mean value of all samples
- x Sampling shall be carried out during the absence of PCD modulation.

AC Parameters Acquisition and Measurement

The AC parameters acquisition and measurement device senses the PCD parameters of the waveform at the J4 connector of the EMV – TEST CMR (which provides a flexible interface) from the source waveform appearing at the J9 connector of the EMV – TEST PICC. The signal at J9 is called the Unprocessed PICC Analogue Sensing signal.

- x The input impedance of the acquisition system shall present a 50Ω load to EMV – TEST CMR output J4.
- x The equipment shall be able to measure a nominal frequency of $13.56 \text{ MHz} \pm 7 \text{ kHz}$ with an accuracy of $\pm 100 \text{ Hz}$ or better.
- x Any possible DC offset of the signal shall be compensated before performing the computation of the final result, for example regarding the Reset voltage, the Power-off voltage and the Type B modulation index.

If this device uses the peak sampling method, it shall have the following characteristics:

- x The test equipment shall feature at least 14-bit resolution.

If this measurement is carried out using the asynchronous sampling method, it shall have the following characteristics:

- x The test equipment shall feature at least 14-bit resolution.
- x Minimum sampling rate: 100 MSa/s. However, note that this sampling rate is only acceptable if appropriate digital post-processing is used.

Table 5-2 shows a summary of the signal names and their characteristics :

Signal Name	Description	Measured at	Built from
PICC Analogue Power Sensing	PCD carrier power evaluation	Output J1 of the EMV – TEST PICC	None, this is a basic signal from the EMV – TEST PICC
Unprocessed PICC Analogue Sensing	PCD waveform evaluation	While the source waveform appears at the J9 connector of the EMV – TEST PICC, it is measured at output J4 of the EMV – TEST CMR	None, this is a basic signal from the EMV – TEST PICC provided through the EMV – TEST CMR

Table 5-2—Summary of the Signal Names and their Characteristics

Several parameters are measured when evaluating the signals in the previous table. Table 5-3 shows a summary of the parameters and the associated signal names:

Parameter	Symbol	Description	Measured at	Associated Signal Name
PCD field strength	V_{ov}	The field strength of a PCD is measured at the EMV – TEST PICC	Output J1 of the EMV – TEST PICC	PICC Analogue Power Sensing
PCD field strength during a reset	$V_{ov,RESET}$	The field strength of a PCD during a reset is measured at the EMV – TEST PICC	Output J9 of the EMV – TEST PICC	Unprocessed PICC Analogue Sensing

Parameter	Symbol	Description	Measured at	Associated Signal Name
Carrier frequency	fc	PCD frequency measured at the Unprocessed PICC Analogue Sensing signal	Output J9 of the EMV – TEST PICC	Unprocessed PICC Analogue Sensing
PCD signal timing	tx	Time between two defined levels of the Unprocessed PICC Analogue Sensing signal	Output J9 of the EMV – TEST PICC	Unprocessed PICC Analogue Sensing
Type B modulation index	mi	PCD Type B modulation index calculated between two defined levels of the Unprocessed PICC Analogue Sensing signal	Output J9 of the EMV – TEST PICC	Unprocessed PICC Analogue Sensing

Table 5-3—Summary of the Parameters and the Associated Signal Names

5.2.3. EMV TEST CMR Control

The EMV – TEST CMR contains relays and delay lines that switch its inputs and set internal signal conditioning features. An external device sends the control signals for switching and setting through the I2C connector.

5.2.3.1. Purpose

For the purposes of the tests in this document, the EMV – TEST CMR control aims to define the CMR input and the clock recovery. The EMV – TEST CMR control writes data to the I2C bus but for the tests described in this manual, does not need to read data.

5.2.3.2. Requirements

The EMV – TEST CMR control shall feature the following characteristics:

- x Control of the relays selecting inputs J2 or J8 (mutually exclusive).
- x Control of the relay selecting the clipper amplifier or the buffer amplifier (mutually exclusive).
- x Control of main clock selection and S/H clock selection.
- x No data transmission from the PC to the EMV – TEST CMR shall occur during measurements.
- x Data sent to the I2C connector shall meet the I2C specification.
- x If synchronous sampling is used, the clock sampling shall be adjustable with a resolution of 10 ps with a range from zero to one carrier cycle.

5.2.3.3. EMV TEST CMR Control Implementation

Figure 5-6 shows the functional blocks for the EMV – TEST CMR control:

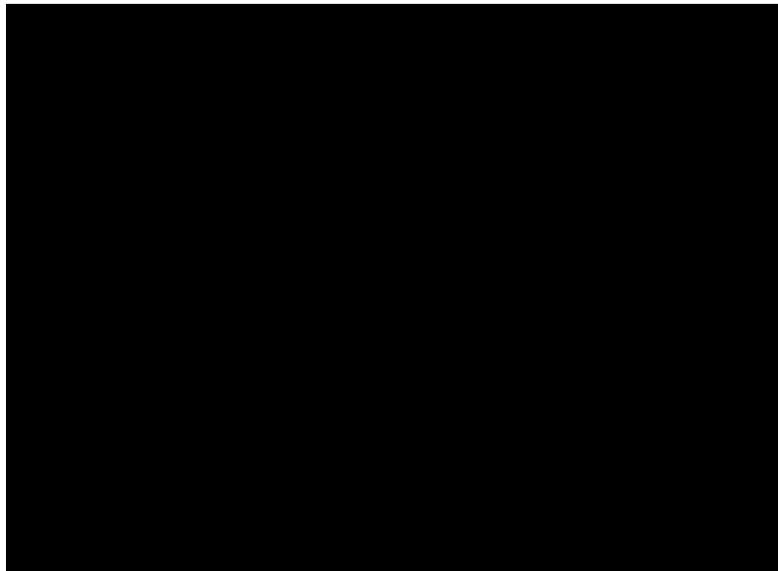


Figure 5-6—Functional Blocks for the EMV – TEST CMR Control

EMV – TEST CMR control software accompanies the EMV – TEST CMR circuit board. This software is adapted to the peak sampling method.

If the acquisition device connected to the EMV – TEST CMR uses the peak sampling method, the CMR control shall be able to adjust the delay lines and clock sources of the EMV – TEST CMR.

If the Acquisition Device connected to the EMV – TEST CMR uses the asynchronous sampling method, it shall have control software that meets the requirements described in section 5.2.3.2

For more information on how to control the EMV – TEST CMR, see the *EMV – TEST CMR* manual.

5.2.4. PCD Emulation

PCD emulation shall be used in the set-up phase of testing operations. Once the EMV Test Equipment is properly set up, the PCD from a vendor shall be used in testing.

5.2.4.1. Purpose

This test function produces an amplified modulated carrier for the EMV – TEST PCD at connector J1. This signal is called the PCD Power Output signal.

It is a source signal used in EMV – TEST PICC set-up.

Note: Modulation is not necessary for tests performed in this document.

5.2.4.2. General Requirements

The PCD emulation function shall feature the following quality characteristics:

- x The generated frequency shall be 13.56 MHz with an accuracy of ± 100 Hz or better.

- x When connected to the EMV – TEST PCD Antenna, the voltage at connector J1 shall be adjustable up to a maximum of 20 V peak to peak. This maximum shall not be exceeded. In the free air condition, the voltage shall be stable within $\pm 1\%$ over the period when it is being used for set-up.
- x When measured on connector J1 of the EMV – TEST PICC, the PCD emulation voltage shall be adjustable to achieve the desired signal level with an accuracy of $\pm 2\%$ including measurement uncertainty.
- x The output impedance shall be nominally $50\ \Omega$ to match the input impedance at input J1 of the EMV – TEST PCD Antenna ($50\ \Omega$ at 13.56 MHz).

5.2.4.3. PCD Emulation Implementation

The PCD emulation is composed of two functional blocks:

- x Signal Generation
- x RF Amplification

Figure 5-7 shows the functional blocks for a PCD emulator:

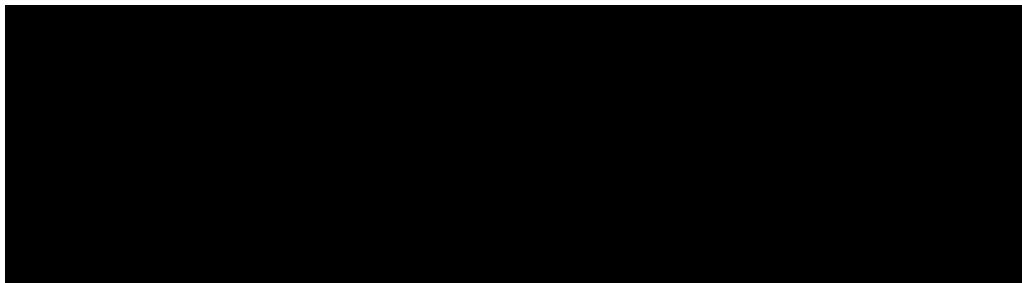


Figure 5-7—Functional Blocks for a PCD Emulator Signal Generation

The Waveform Generator sends a low-power analogue electrical signal with a waveform corresponding to the waveform of the electromagnetic field that needs to be generated. This signal is called the PCD Analogue Transmission signal.

The basic performance criteria of the Waveform Generator shall be the following:

- x Frequency range 13.5 to 13.6 MHz
- x Frequency resolution and accuracy of 100 Hz or better
- x Spurious distortion less than -60 dBc in the vicinity of the carrier or its sidebands; the sum of all distortions shall be less than -50 dB so as not to swamp card modulation measurements.

RF Amplification

In this second functional block, one component amplifies the signal received from the signal generation block.

The RF Power Amplifier converts the low-power PCD Analogue Transmission signal into a higher power signal that is fed to the J1 input of the EMV – TEST PCD. This signal is called the PCD Power Output signal.

The basic performance criteria of the RF Amplifier after any additional attenuation shall be the following:

- x Power output at 1dB compression point : 1W minimum
- x Low harmonic distortion (better than -50 dBc)

- x Suitable bandwidth ($13.56\text{ MHz} \pm 2\text{ MHz}$)
- x For EMV Contactless testing, the power output of the RF Amplifier shall be from 0.5 W to 1 W into an impedance of $50\text{ }\Omega$.
- x $\text{VSWR} < 1.2:1$

Note The RF power amplifier must be able to operate with a high VSWR without damage, as VSWR will increase when the EMV – TEST PICC under test is placed close to the EMV – TEST PCD.

Table 5-4 shows a summary of the signal name and its characteristics :

Signal Name	Description	Measured at	Built From
PCD Power Output	Amplified carrier signal	Input J1 of the EMV – TEST PCD	PCD Analogue Transmission signal

Table 5-4—Summary of the Signal Name and its Characteristics

5.2.5. Signal Acquisition and Measurement on EMV TEST PCD

During load modulation measurement of the EMV – TEST PICC set-up, signal acquisition and measurement on the EMV – TEST PCD plays an important role and its parameters shall be evaluated.

5.2.5.1. Purpose

This function acquires and measures PICC load modulation to be used in PCD receptivity testing.

5.2.5.2. Requirements

The signal acquisition shall feature the following general characteristics:

- x The equipment shall be able to acquire a signal with an amplitude up to 2 V peak to peak.
- x The equipment shall provide a graphic display of the digitally formatted signal for visual analysis. The signal shall be measured for at least 1 ms and shall be displayed with a load modulation amplitude accuracy of 10 \% with a minimum of 1 mV or better.
- x The input impedance of the acquisition equipment shall present a $50\text{ }\Omega$ load to the EMV – TEST CMR output.
- x The equipment shall convert the analogue signal to a digital format as early as possible in the process (conversion may be peak detection or asynchronous sampling).
- x The equipment shall be able to make automated measurements of the load modulation and shall measure down to 3 mV of load modulation coming from the EMV – TEST PICC.

Over at least seven successive subcarrier cycles of the same phase state, the automated measurement shall calculate the difference between the average value of all the positive peaks and the average value of all the negative peaks that correspond to the positive and negative peaks of the subcarrier cycles

5.2.5.3. Signal Acquisition and Measurement on EMV TEST PCD Implementation

Figure 5-8 shows the block diagram for signal acquisition and measurement on the EMV – TEST PCD:

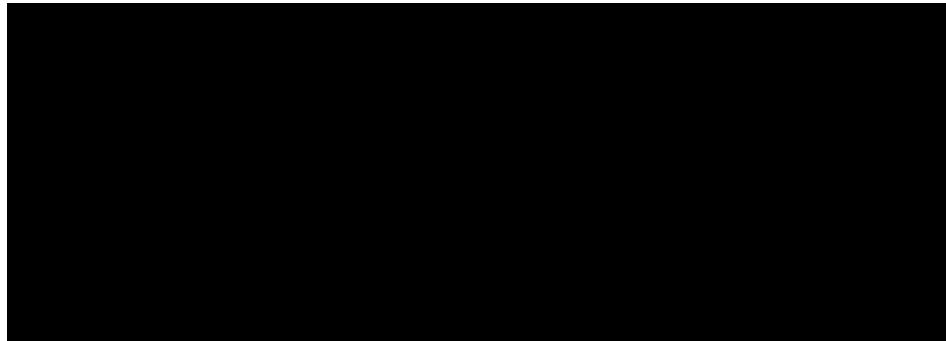


Figure 5-8—Block Diagram for Signal Acquisition and Measurement on the EMV – TEST PCD EMV TEST PCD

EMV TEST PCD

The EMV – TEST PCD sends a signal to the EMV – TEST CMR. This signal is called the Unprocessed PCD Analogue Sensing signal.

Acquisition Device

The Acquisition Device achieves the test function requirements by signal acquisition and measurement on output J4 of the EMV – TEST CMR (Relay 1 of the EMV – TEST CMR is set to enable signal flow from J2 to J4). This signal is called the Processed PCD Analogue Sensing signal.

If this device uses the peak sampling method, it shall have the following characteristics:

- x The equipment shall feature at least 14-bit resolution.

If this measurement is carried out using the asynchronous sampling method, it shall have the following characteristics:

- x The equipment shall feature at least 14-bit resolution.
- x The minimum sampling rate shall be 100 MSa/s.

Note The minimum sampling rate of 100 MSa/ s is only acceptable if suitable digital post processing is performed.

Table 5-5 shows a summary of the signal name and its characteristics.

Signal Name	Description	Measured at	Built From
Processed PCD Analogue Sensing	Signal used for PICC load modulation measurement	Output J4 of the EMV – TEST CMR	Unprocessed PCD Analogue Sensing

Table 5-5—Summary of the Signal Name and its Characteristics

Table 5-6 shows a summary of the parameter and its characteristics :

Parameter Name	Symbol	Description	Measured at
Load Modulation	V _{pp}	Difference (over at least seven successive subcarrier cycles of the same phase state) between the average of the high peak values and the average of the low peak values of the subcarrier visible in the Processed PCD Analogue Sensing signal	Output J4 of the EMV – TEST CMR

Table 5-6—Summary of the Parameter and its Characteristics

5.3. Test Bench Environment

The Test Bench requires additional hardware to be functionally complete, operate efficiently and facilitate operator duties.

5.3.1. Purpose

The Test Bench shall be supplied with appropriate electrical power, environmental monitoring tools and data storing/reporting devices for simple and efficient operation.

5.3.2. Requirements

The Test Bench shall feature the following characteristics:

Test Bench Powering

The PCD under test shall use the Power Supply required by the vendor of the PCDs to be tested. In the case where the Power Supply required by the vendor is specified as one provided by the Testing Laboratory (a stabilized Power Supply), monitoring of voltages shall be performed during the test sessions.

Environmental Monitoring

- ✗ AC voltage monitoring in the following range 0 to 250 V AC, with an absolute total error of less than ± 500 mV.
- ✗ DC voltage monitoring in the following range 0 to 50 V DC, with an absolute total error of less than ± 100 mV.
- ✗ Temperature monitoring in the following range 20°C to 26°C, with an absolute total error of less than $\pm 1.0^\circ\text{C}$.
- ✗ Humidity monitoring in the following range 40% to 60%, with an absolute total error of less than $\pm 3\%$ RH.

Data Storing

- ✗ Data Storage

5.4. Summary of Signals Names and Parameters

This section presents the signal names and parameters, along with their definitions, which are used in analogue testing operations.

5.4.1. Signal Names

Each test function corresponds to a signal of interest that is measured or used in testing. A signal of interest is created with Test Bench equipment that produce component signals directly related to the nature of the signal of interest.

Table 5-7 shows the signals and their components in the PCD EMV Contactless Test Bench :

Signal Name	Description	Measured at	Built from
PICC Analogue Transmission	Signal used by the EMV – TEST PICC to modify the load on the PCD electromagnetic field	Input J2 of the EMV – TEST PICC	PCD Synchronization PICC Digital Transmission
PICC Analogue Power Sensing	PCD carrier power evaluation	Output J1 of the EMV – TEST PICC	None, this is a basic signal from the EMV – TEST PICC
Unprocessed PICC Analogue Sensing	PCD waveform evaluation	Output J9 (pickup coil) of the EMV – TEST PICC	None, this is a basic signal from the EMV – TEST PICC
PCD Power Output	Amplified carrier signal	Input J1 of the EMV – TEST PCD	PCD Analogue Transmission
Processed PCD Analogue Power Sensing	Signal used for PICC output Load Modulation Measurement	Output J4 of the EMV – TEST CMR	Unprocessed PCD Analogue Sensing

Table 5-7—Summary of the Signals and their Components in the PCD EMV Contactless Test Bench

Table 5-8 shows the component signals from which test function signals of the PCD EMV Contactless Test Bench are made :

Signal Name	Description	Available at
PCD Synchronization	Trigger signal for PICC coding generation	Output of the synchronization circuit Input trigger of the PICC Coding Generator
PICC Digital Transmission	Digital code stream signal at the output of the PICC Coding Generator used to implement the PICC emulation function.	Output of the PICC Coding Generator Input of Load Modulation Adjustment
PCD Analogue Transmission	Un-amplified carrier	Output of the Waveform Generator Input of the RF Amplifier
Unprocessed PCD Analogue Sensing	PICC load modulation before passing through the EMV – TEST CMR	Output J2 of the EMV – TEST PCD

Table 5-8—Summary of Component Signals in the PCD EMV Contactless Test Bench

While the component signals are not measured in the tests found in this document, their familiarity allows accurate description of a Test Bench implementation.

Note: Component signals shall be measured in the Acceptance Testing document EMVCo Contactless Type Approval: PCD Analogue Test Bench Acceptance Testing manual.

5.4.2. Parameters

Table 5-9 shows a summary of the parameters applicable to the PCD EMV Contactless Test Bench :

Parameter Name	Symbol	Description
PCD field strength	V_{ov}	The field strength of a PCD measured at the J1 connector of the EMV – TEST PICC. This is an average voltage over 10 μ s to 200 μ s of the PICC Analogue Power Sensing signal
PCD field strength during a reset	$V_{ov,RESET}$	The field strength of a PCD during a reset is measured at the J9 connector of the EMV – TEST PICC

Parameter Name	Symbol	Description
Load modulation	Vpp	Difference (over at least seven successive subcarrier cycles of the same phase state) between the average of the high peak values and the average of the low peak values of the subcarrier visible in the Processed PCD Analogue Sensing signal
Carrier frequency	fc	PCD frequency measured at the Unprocessed PICC Analogue Sensing signal
PCD signal timing	tx	Time between two defined levels of the Unprocessed PICC Analogue Sensing signal
Type B modulation index	mi	PCD Type B modulation index calculated between two defined levels of the Unprocessed PICC Analogue Sensing signal

Table 5-9—Parameters Applicable to the PCD EMV Contactless Test Bench

6. Executing an EMV Analogue Interface Test Session

Several steps are necessary to ensure accurate and repeatable EMV analogue interface sample testing. Test samples shall be representative and properly prepared for testing. The results of the various tests shall then be properly reported including deviations from the standard procedures.

6.1. Preparation for Testing

Before starting any testing campaign or receiving test samples, several important requirements shall be verified:

- x The Testing Laboratory shall implement a Test Bench with all test functions described in Chapter 5.
- x The personnel operating the Test Bench shall be appropriately trained and qualified.
- x The Testing Laboratory shall write standard operating procedures providing detailed methods on the EMV Analogue PCD tests and how results are recorded.
- x The testing laboratory shall calculate and maintain records of measurement uncertainty estimates prepared using internationally accepted methodology for all Test Cases.

6.2. Verifying Appropriateness

This section contains verifications and requirements to ensure that a PCD test sample is appropriate for testing. It also contains recommendations that shall be followed for dealing with a PCD without a perfectly flat landing plane.

6.2.1. General Requirements

The first step in testing the EMV analogue interface shall be to verify that the sample submission is complete and appropriate.

When samples arrive from the vendor, the Testing Laboratory shall compare the items and their markings with the delivery documentation to ensure that they match. Any discrepancy shall be resolved with the vendor before beginning any testing.

If the submission is not complete, the Testing Laboratory shall also contact the vendor and request completion. Carefully note the reasons for discrepancies, delays and incompleteness in sample delivery to the Testing Laboratory.

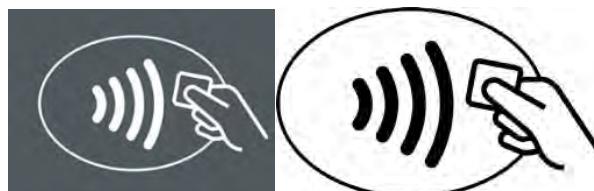
Before starting PCD testing, the qualified operator shall carry out the following actions:

1. Select one PCD sample according to the sampling rules of the Testing Laboratory.
2. Verify that the sample is properly identified and labeled (manufacturer, type, serial number, revision).

3. Verify that the PCD features a correct EMV Contactless symbol as defined in the specifications. All the following items shall be verified :
 - a) The symbol drawing shows the contactless indicator (four circular arc lines from smallest to largest in size, left to right) at the center of the symbol, the hand holding a generic contactless form factor device and an oval key line that wraps the indicator and the hand



- b) The drawing is in white reversed line drawing against any medium to dark background, or in black line drawing against a white or light-colored background.



- c) The background is a solid color. It does not feature any graphic pattern.



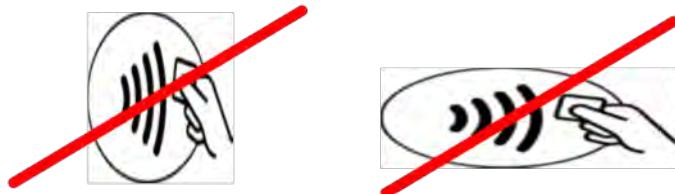
- d) No additional nor modified item is present.



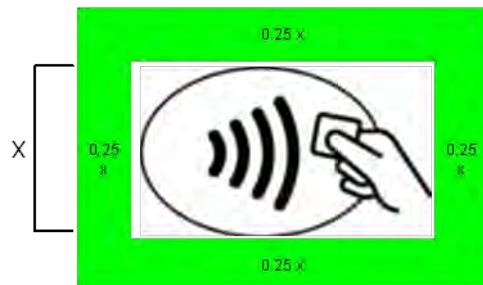
- e) The minimum size of the symbol is 13 mm height by 22 mm width.



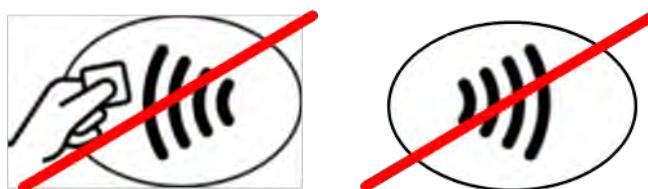
- f) The size of the symbol features a height/width ratio of 0.59 ± 0.05 .



- g) A clear space band having a width of at least a quarter of the height of the symbol exists all around the four sides of the contactless symbol. No other text or graphic element appears in this zone.



- h) The symbol is neither rotated nor flipped. The hand is present on the right side of the symbol



- i) There is no text message with the symbol.



The appropriate section of the test report must be filled with the result of this verification.

4. Verify that the positioning characteristics have been defined properly.
5. Verify that the PCD sample has been subjected to the pre-validation test. Refer to the *EMVCo Contactless Type Approval: PCD Pre-validation Prior to Level 1 testing* manual for details. Two cases are possible depending on the pre-validation test results:
 - If the results are pass, the laboratory continues the analogue tests of the Contactless Terminal Type Approval Level 1 testing process as described in Chapter 8 of *the EMVCo Contactless Type Approval: PCD Analogue Test Bench and Test Case Requirements* manual.
 - If some results are fail, the laboratory informs the vendor and waits for the decision of the vendor to either continue the Contactless Terminal Type

Approval Level 1 testing or stop the process unless the vendor already requested to continue testing regardless of the results.
In the situation where the vendor decides to stop, the test report shall be made available for the Vendor.

6. Verify the presence of a vendor-provided Device Test Environment (DTE) meeting the requirements described in the EMVCo Device Testing Environment document. For further information on this DTE, see Appendix A of the EMVCo Type Approval Contactless Terminal Level 1/ Device Test Environment document.
7. Verify the presence of vendor-provided Device Testing Environment (DTE) documentation
 - That is identified in the ICS (make sure that you have received everything that you are supposed to receive)
 - That is complete thereby allowing the performance of all necessary tests.
8. Verify that the vendor-provided DTE is understood by the operator.
9. Verify the presence of supplementary documentation with respect to:
 - Documentation of the electrical interface between the sample and the terminal, when these two units are separate hardware items.
 - Documentation of the setup information describing the normal operating conditions of the PCD under test and the conditions for powering and activating the PCD sample.
 - Documentation of any operator-defined settings influencing analogue behavior.
 - A troubleshooting manual, describing common abnormalities and their remedies.
10. Take a photograph of the side of the sample with the positioning characteristics.

For testing purposes, the $\varphi=0$ axis is oriented as shown in Figure 6-1 :

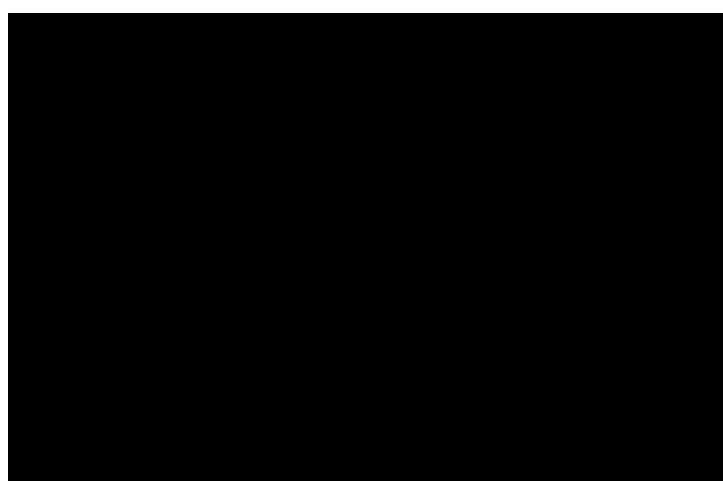


Figure 6-1— $\varphi=0$ Axis Orientation

6.2.2. Recommendations for a PCD without a perfectly flat Landing Plane

PCDs with ridges or uneven landing planes shall be handled and tested using special precautions to ensure consistent test results. The recommendations are:

- x In all cases, the plane of the EMV – TEST PICC shall remain perpendicular to the z axis at all times.
- x If the EMV – TEST PICC can be placed against the landing plane at test positions within the area defined by a ridged, concave or concave-like PCD test area, the actual level z=0 cm (specifically, the surface at the center of the landing plane) is used.
- x If the EMV – TEST PICC is larger than this area and therefore sits on a ridge or one of its edges touches a concave PCD surface, the space between the elevated EMV – TEST PICC plane and the actual level z=0 cm surface is treated as follows:
 - o All points between the actual level z=0 cm and the point where the EMV – TEST PICC sits on the ridge will be reported as "Not tested because of terminal shape". In these cases, the Test Cases are performed using all the usually required higher positions in the Test Position tables and additionally at the closest achievable level to z=0 cm.

Note: If you cannot reach below 5 mm, contact EMVCo to obtain help in determining new test positions to be performed.

- o In the testing report, include the actual distance at which the first valid results were made next to the 0 positions in the "Value for z" columns. This ensures that these exceptions are duly noted. All other measurements shall be made from the landing plane containing the contactless symbol.
- o The testing report shall include these results and the actual distance at which they were obtained. The distance is taken from the center of the EMV – Test PICC. When acceptance criteria are depending upon the value of z, they shall be adjusted using the actual z value used during testing ($0 < z < 5\text{mm}$).

6.3. Identifying the Sample

The configuration of the sample shall be identified unambiguously. Any modification to the sample (mechanical, electrical, functional) during the test session shall require complete re-testing of the modified sample, regardless of the nature of the modified part.

6.4. Powering the Sample

Where the sample needs a power source to operate, it shall be tested according to the conditions provided by the vendor. Where the sample can be powered using either external

or internal power sources, it shall be tested using the internal power source as specified by the vendor.

The power source used and the supply voltage provided during the test session shall be recorded in the test report.

6.4.1. PCD Tests with External Power Source provided by the Vendor

During tests, the external power source provided with the equipment shall be used. The Testing Laboratory shall be capable of producing high AC voltage as required by the vendor.

During tests, the test power source voltages shall remain within the vendor tolerance.

6.4.2. PCD Tests with External Power Source provided by the Testing Laboratory

During tests, the external power source provided with the equipment shall be replaced by an external test power source provided by the Testing Laboratory and capable of producing normal test operating voltages as specified by the vendor. The internal impedance of the external test power source shall be low enough for its effect on the test results to be negligible. For the purpose of analogue tests, the voltage of the external test power source shall be measured at the input connections of the PCD. The external test power source shall be suitably decoupled so as to be located as far away from the PCD as possible. All external power leads shall be arranged so as not to affect measurements.

During tests the test power source voltages shall remain within the vendor tolerance.

6.4.3. PCD Test with Internal Power Source

For radiated (RF or electromagnetic) measurements on portable equipment, fully charged internal batteries shall be used. The batteries used shall be as supplied or recommended by the PCD vendor. If internal batteries are used, the test power source voltages shall remain within the vendor tolerance.

The power source voltage at the beginning and at the end of the tests shall be recorded in the test report.

6.4.4. Other Power Sources

For operation from other power sources or types of battery, the normal test voltage shall be that declared by the PCD vendor and agreed by the accredited Testing Laboratory. Such values should be recorded in the test report when possible.

6.5. Preparing the EMV Test Equipment

Before starting the test on a sample, the operator shall perform a preparatory verification of the EMV Test Equipment for the test according to the procedures described in this manual.

The only critical verification that shall be performed periodically is the EMV – TEST PCD and EMV – TEST PICC cross verification. See Chapter 6 for more information.

The Testing Laboratory can also use the required monitoring equipment to confirm that the Test Bench is properly powered and stable. See the section Test Bench Support Functions in Chapter 7.

6.6. Sample Testing

6.6.1. Sequence of Execution

The execution of an EMV analogue test involves performing all Test Cases under different test conditions, as specified in this document.

The PCD under test shall be challenged using the Test Bench equipment and according to external conditions. The challenge shall be conducted in a non-destructive fashion, which primarily means that the Test Bench shall not exceed the sample PCD limits.

After verifying appropriateness, a specific order of Test Cases or conditions is not required during EMV analogue testing with the exception of measuring the carrier frequency, as long as all Test Cases are performed for all specified test conditions on the sample. Any deviation shall be properly recorded in the test report.

6.6.2. Test Results

The test results shall be recorded as an ordered collection of pass/fail values, related to the PCDs under test and the test conditions. This is called detailed report data.

The Testing Laboratory shall also provide screenshots and traces resulting from test failures or intermittent results.

6.6.3. Failed Procedures

If one or more of the following situations appears:

- x A specified test condition cannot be attained during test execution.
- x A test procedure cannot be executed exactly as indicated.
- x A test procedure cannot be completed.

Two cases are possible depending on test bench automation:

- x If the test bench is automated, the test bench shall report a failed procedure. Operator action is necessary to correct the situation.
- x If the test bench is not automated, then the operator shall report a failed procedure situation and shall, for example, repeat the Test Case.

6.7. Generating a Report

The results of all individual Test Cases that were carried out shall be gathered into a single detailed report.

If it was not possible for any reason to carry out all the Test Cases then this shall be clearly documented.

A summary report based on detailed report data shall then be prepared and shall fulfill all the requirements of the EMV PCD report template.

6.8. Tasks after Completing a Test Campaign

The Testing Laboratory shall store all forms and reports to ensure security and confidentiality in accordance to client requirements.

Onsite report and documentation storage shall comply with ISO/IEC 17025:2005 standards.

Test samples shall be safely stored on premises to facilitate future testing or unexpected requirements.

7. Preparation of the EMV Test Equipment

7.1. General Requirements

The operator shall use the procedures described in this chapter to determine and document the correct functionality of the EMV Test Equipment used for all tests.

These procedures shall be carried out before starting tests on PICCs or PCDs. The data obtained from these procedures shall be included in the test report for the product.

In the event of EMV – TEST PICC or EMV – TEST PCD preparation failure, the test equipment shall be re-calibrated

Note: Do not perform any EMV Analogue Interface test until the test equipment has been calibrated by a Tool Vendor or Laboratory authorized by EMVCo to specifically perform calibration of these devices.

Note: The following preparation procedures allow verification of the test equipment calibration with a Vector Network Analyzer (VNA). Testing Laboratories may use other procedures described in the section Verification Procedure of the documents *EMV – TEST PCD manual*, *EMV – TEST CMR manual* and *EMV – TEST PICC manual*.

7.2. Preparing the EMV TEST PICC

The procedure for EMV – TEST PICC verification shall take place in an environment where the temperature is $23^{\circ}\text{C} \pm 3^{\circ}\text{C}$ and the relative humidity is $50\%\text{RH} \pm 10\%\text{RH}$.

Note: The verification of the EMV – TEST PICC shall be performed using a suitable Calibration Kit.

Note: For all connections, the standard cable is a high quality coaxial cable, such as RG-316, terminated by SMA connectors. The cable ends are then fitted with appropriate adaptors for the connections to be made.

7.2.1. Verifying the EMV TEST PICC

Follow this procedure for EMV – TEST PICC verification:

1. Refer to the diagram in Figure 7-1

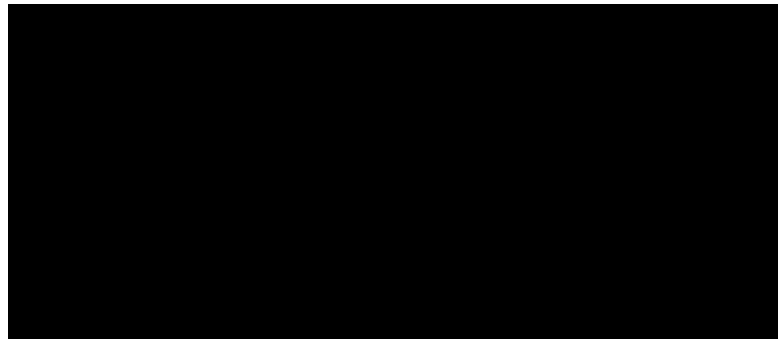


Figure 7-1—Diagram for EMV – TEST PICC

2. Connect a cable to Port 1 of the VNA but do not yet connect the other end of this cable to the EMV – TEST PICC at J6.
3. Set the frequency range of the VNA from 10 MHz to 20 MHz with at least 1000 points in the sweep and the power sweep generator at an output corresponding to 0 dBm/50 Ω.

Note: If it is not possible for the sweep to comprise at least 1000 points, the sweep must be reduced until the VNA step size is at most 10 kHz.

4. Perform an Open/Short/Load (OSL) calibration of the VNA and its built-in bridge at the unconnected end of the cable. This establishes the reference plane for Port 1.
5. Connect the unconnected end of the cable to the EMV – TEST PICC at J6.

6. Set the VNA to the S₁₁ measurement mode and the impedance format. The screen shown in Figure 7-2 appears on the VNA display:

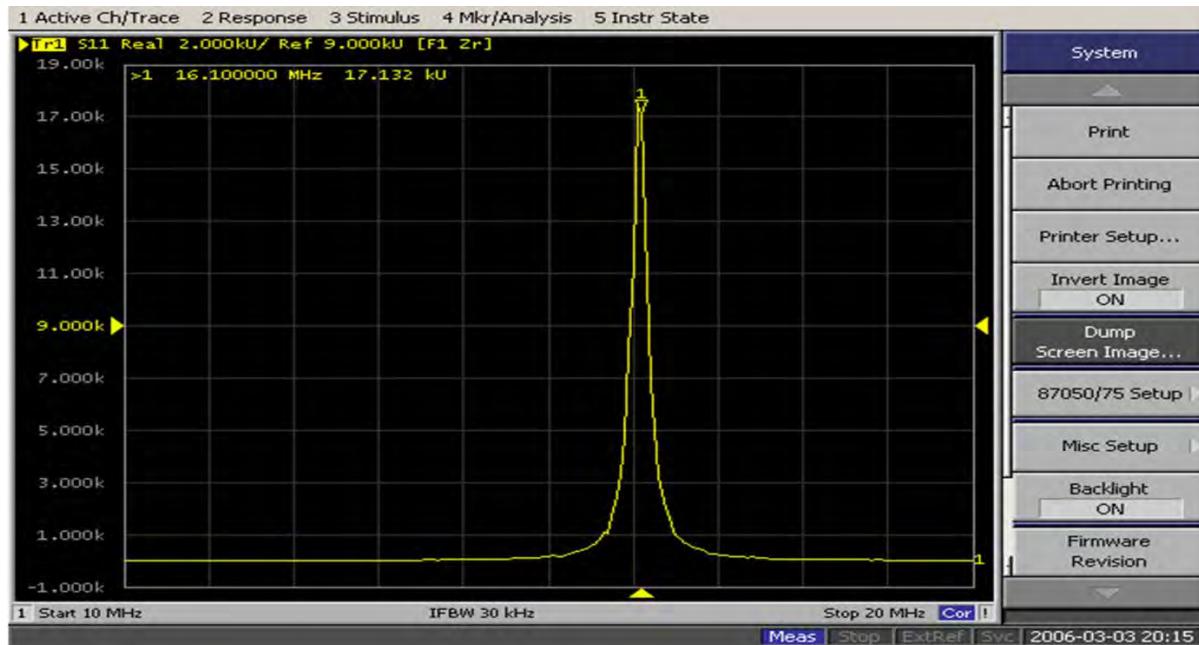


Figure 7-2 - TEST PICC Resonant Frequency

At the resonant frequency of the EMV – TEST PICC antenna, note the presence of a peak of the impedance and zero degrees phase shift.

7. Measure the resonant frequency.

Acceptance Criteria

Verification is successful if the resonant frequency is 16.100 MHz \pm 100 kHz.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

Failure Action

A fail message requires the following actions:

- Request calibration of the EMV – TEST PICC.
- Report failure to EMVCo and request advice.
- Wait until EMVCo gives feedback before starting any such test.

7.3. Preparing the EMV TEST PCD Antenna

The procedure for EMV – TEST PCD verification shall take place in an environment where the temperature is $23^{\circ}\text{C} \pm 3^{\circ}\text{C}$ and the relative humidity is $50\%\text{RH} \pm 10\%\text{RH}$.

Note: The verification of the EMV – TEST PCD antenna shall be performed using a suitable Calibration Kit.

7.3.1. Verifying the EMV TEST PCD Antenna

Follow this procedure for verification of a previously calibrated EMV – TEST PCD using a VNA:

1. Refer to the diagram in Figure 7-3:

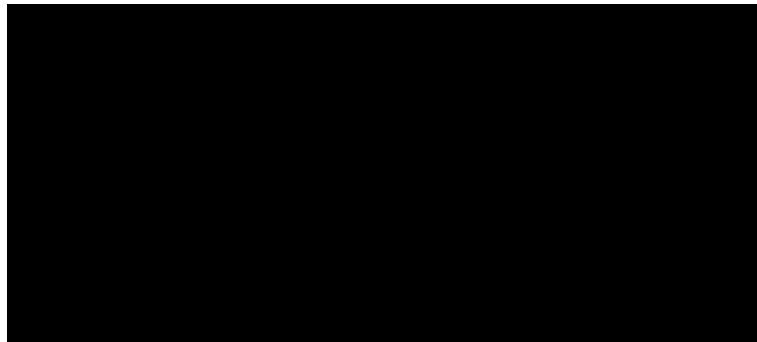


Figure 7-3 – Connectivity for EMV – TEST PCD

2. Connect a 50Ω load to the EMV – TEST PCD at J2.
3. Connect a cable to Port 1 of the VNA but do not yet connect the other end of this cable to the EMV – TEST PCD at J1.
4. Set the frequency range of the VNA from 13 MHz to 14 MHz with at least 1000 points in the sweep and the power level set to 0 dBm/ 50Ω .
5. Perform an Open/Short/Load (OSL) calibration of the VNA and its built-in bridge at the unconnected end of the cable coming from Port 1. This establishes the reference plane for Port 1.
6. Connect the unconnected end of the cable coming from Port 1 of the VNA to the EMV – TEST PCD at J1.
7. Set the VNA to S_{11} measurement mode at Port 1.

8. Set the VNA in Smith Chart format ($R+jX$). Figure 7-4 shows measurements executed on the VNA at 13.56 MHz :

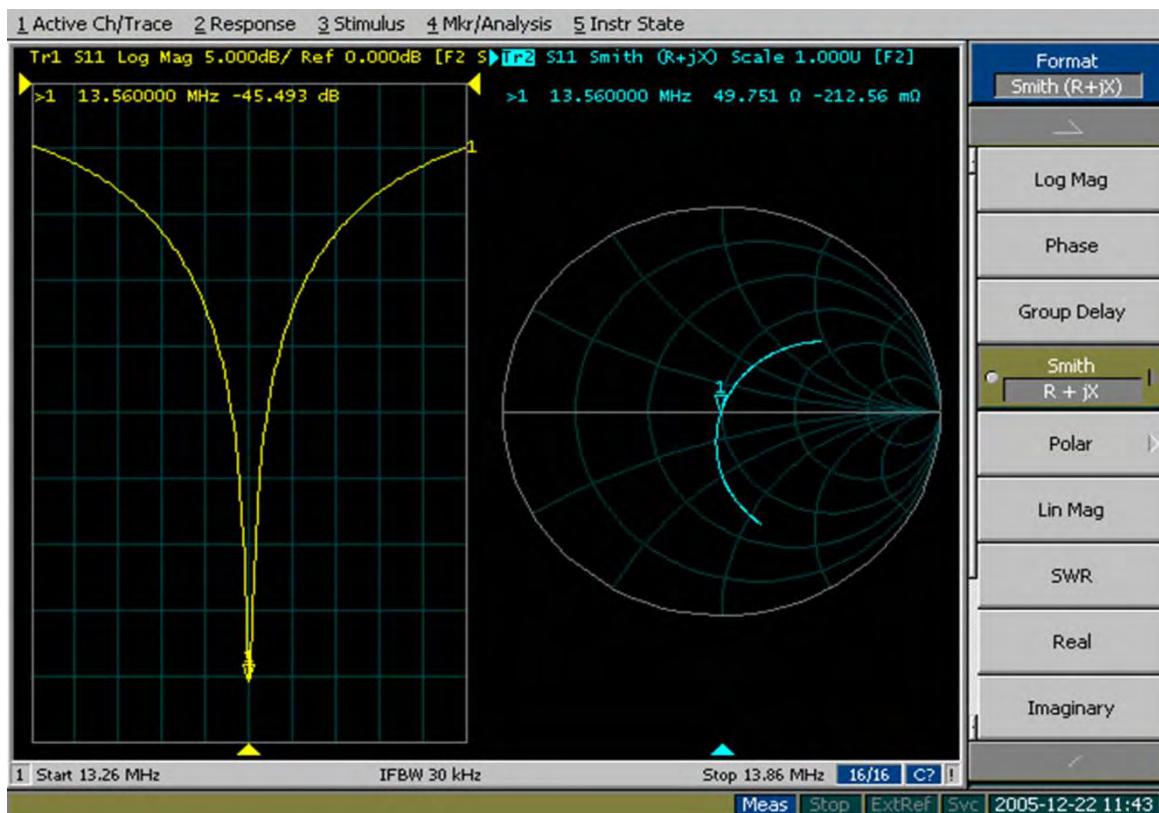


Figure 7-4 – EMV – TEST PCD Verification

Note: The impedance magnitude may be computed using the formula

$$Z = \sqrt{R^2 + X^2}$$

Note: The impedance phase may be computed using the formula

$$\phi = \tan^{-1}(X/R)$$

Acceptance Criteria

Verification is successful if the resonant frequency is $13.560 \text{ MHz} \pm 7 \text{ kHz}$

(the frequency with maximum return loss) and the impedance at 13.560 MHz has a magnitude of $50 \Omega \pm 5 \Omega$ with a phase of $0^\circ \pm 10^\circ$.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

Failure Action

A fail message requires the following actions:

- x Request calibration of the EMV – TEST PCD.
- x Report failure to EMVCo and request advice.
- x Wait until EMVCo gives feedback before starting any such test.

7.4. Preparing the EMV TEST CMR

The procedure for EMV – TEST CMR verification shall take place in an environment where the temperature is $23^{\circ}\text{C} \pm 3^{\circ}\text{C}$ and the relative humidity is $50\%\text{RH} \pm 10\%\text{RH}$.

7.4.1. Verifying the EMV TEST CMR

The EMV – TEST CMR does not require any calibration, but instead requires that the gain obtained from the input to the output is measured and recorded during the verification procedure.

The EMV – TEST CMR shall successfully pass three tests to verify that it has suitable signal transmission, delay line and gain. Perform all three verification procedures in this section for EMV – TEST CMR preparation.

7.4.1.1. J2 to J4 Signal Transmission Verification

Follow this procedure for the signal transmission verification:

1. Refer to the diagram in Figure 7-5:

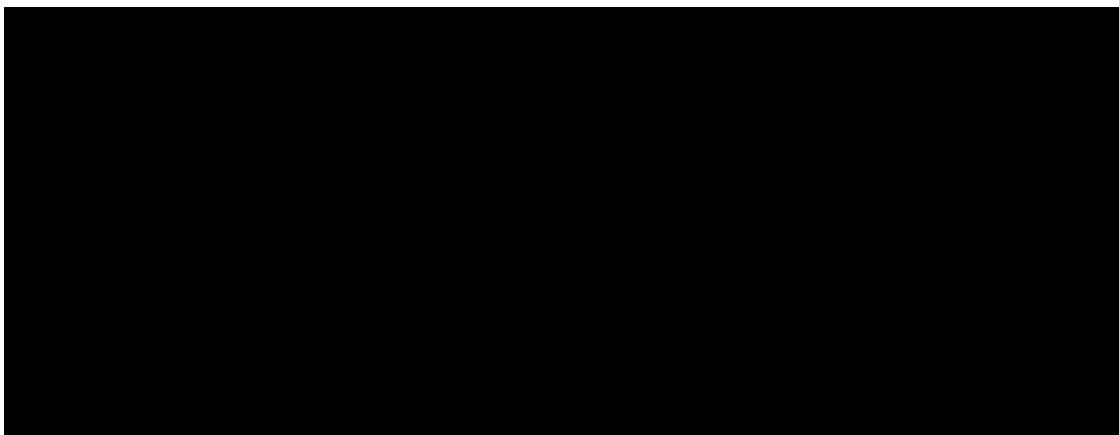


Figure 7-5- Diagram for the EMV – TEST CMR Signal Transmission Verification

Connect appropriate devices so as to implement the functionalities shown.

2. Connect the power supplies to the appropriate voltage connection points, switch on the power supplies and check that the current drawn is within the limits shown in Table 7-1 :

Voltage	Current
+12 V	150 mA
-12 V	350 mA
+5 V	1300 mA

Table 7-1—Power Supply Parameters

3. Set up the EMV – TEST CMR relays as shown in Table 7-2 :

Relay	
Input	J2
Clock	Internal recovery
Amplifier	Buffer

Table 7-2—EMV – TEST CMR settings

4. Set the Waveform Generator to 13.56 MHz with an amplitude of 300 mV peak to peak into $50\ \Omega$.
5. Measure the amplitude on CH0 of the DSO.
6. Measure the amplitude and frequency of the signal on CH1 of the DSO.

Acceptance Criteria

The amplitude on CH0 of the DSO is between 285 and 300 mV peak to peak.

A square wave on CH1 of the DSO has an amplitude of approximately 2 V peak to peak.

The signal frequency on CH1 of the DSO is $13.560\ \text{MHz} \pm 7\ \text{kHz}$.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

Failure Action

A fail message requires the following actions:

- x Report failure to EMVCo and request advice.
- x Wait until EMVCo gives feedback before starting any such test.

7.4.1.2. Delay Line Verification

Follow this procedure for delay line verification:

1. Refer to the diagram in Figure 7-6:

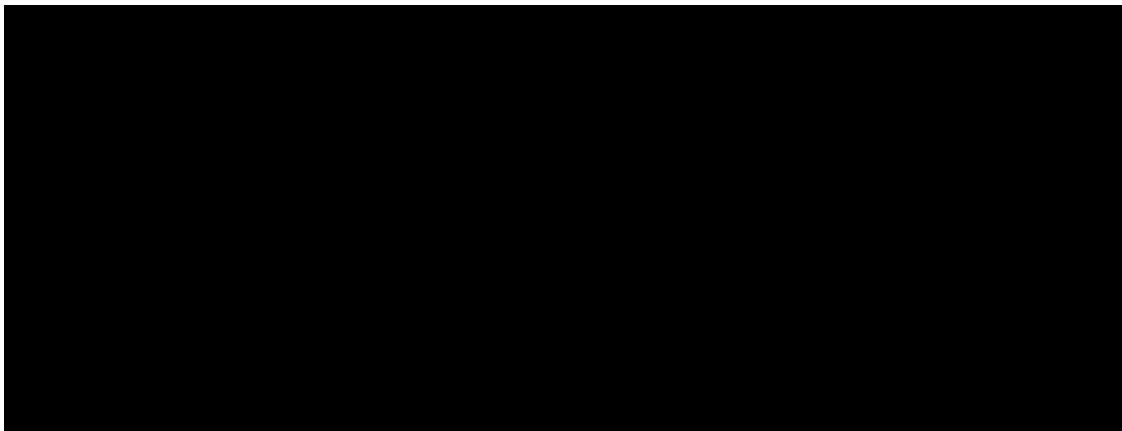


Figure 7-6 - Diagram for the EMV – TEST CMR Delay Line Verification

Connect appropriate devices so as to implement the functionalities shown.

2. Connect the power supplies to the appropriate voltage connection points, switch on the power supplies and check that the current drawn is within the limits shown in Table 7-3 :

Voltage	Current
+12 V	150 mA
-12 V	350 mA
+5 V	1300 mA

Table 7-3—Power Supply Parameters

3. Set up the EMV – TEST CMR relays as shown in Table 7-4:

Relay	
Input	J2
Clock	Internal recovery
Amplifier	Buffer

Table 7-4—Test CMR Settings

4. Set the Waveform Generator to 13.56 MHz with an amplitude of 300 mV peak to peak.
5. Using the I2C interface, adjust the delay settings for DL1 and DL2.

Acceptance Criteria

The phase of the main clock signal on CH1 of the DSO shall be modified by steps according to the adjustment made to the delay lines.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

Failure Action

A fail message requires the following actions:

- x Report failure to EMVCo and request advice.
- x Wait until EMVCo gives feedback before starting any such test.

7.4.1.3. Main Clock Verification

1. Refer to the diagram in Figure 7-7:

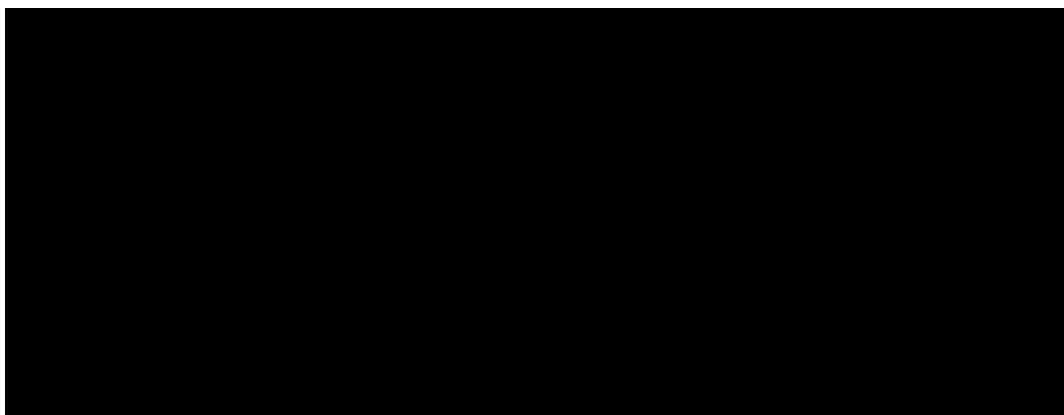


Figure 7-7—Diagram for the EMV – TEST CMR Main Clock Verification

Connect appropriate devices so as to implement the functionalities shown.

2. Connect the power supplies to the appropriate voltage connection points, switch on the power supplies and check that the current drawn is within the limits shown in Table 7-5 :

Voltage	Current
+12 V	150 mA
- 12 V	350 mA
+5 V	1300 mA

Table 7-5—Power Supply Parameters

3. Set up the EMV – TEST CMR relays as shown in Table 7-6:

Relay	
Input	J2
Clock	External recovery (input J1)
Amplifier	Buffer

Table 7-6—EMV – TEST CMR Settings

4. Set the Waveform Generator to 13.56 MHz with an amplitude of 300 mV peak to peak.
5. Observe the signal on CH1 of the DSO.

Acceptance Criteria

If the signal on CH1 of the DSO is a square wave with an amplitude of approximately 2 V peak to peak, the verification is successful.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

Failure Action

A fail message requires the following actions:

- x Report failure to EMVCo and request advice.
- x Wait until EMVCo gives feedback before starting any such test.

7.4.2. EMV TEST CMR Gain Measurement

Follow this procedure for the EMV – TEST CMR gain measurement:

1. Refer to the diagram in Figure 7-8:

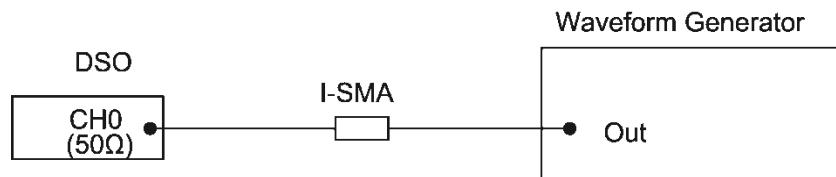


Figure 7-8—First Diagram for the EMV – TEST Gain Measurement

Connect appropriate devices so as to implement the functionalities shown.

Note: The connection between the DSO and the Waveform Generator is made with two SMA cables of 50 cm or less, interconnected by an I-SMA adaptor which is a female to female SMA adaptor.

2. Set the Waveform Generator to 13.56 MHz with an amplitude of 1 V peak to peak into 50Ω .
3. Measure the peak to peak amplitude on CH0 of the DSO.

- Refer to the diagram in Figure 7-9

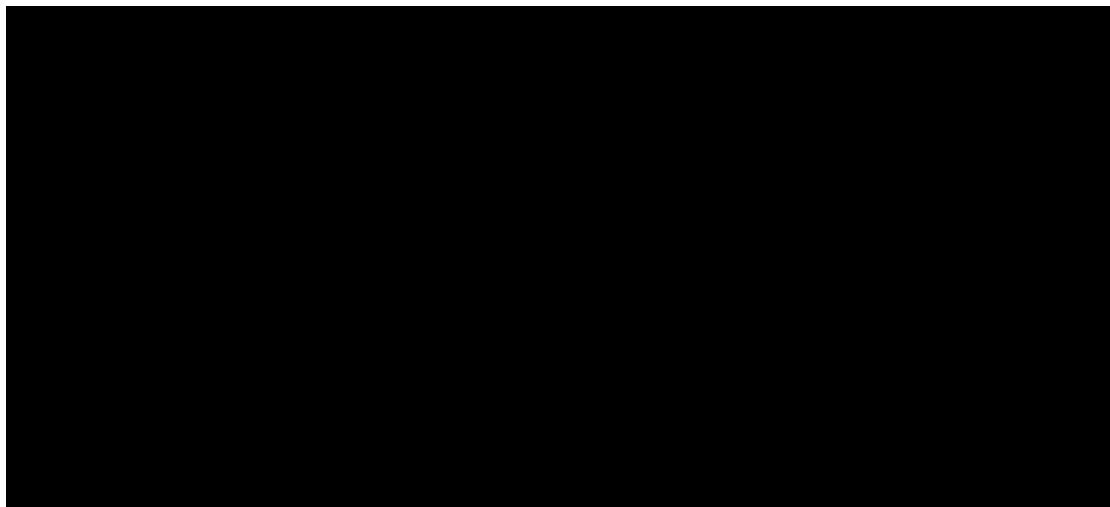


Figure 7-9—Second Diagram for the EMV – TEST Gain Measurement

- Using the same cables used in previous steps, remove the I-SMA adaptor and substitute the CMR in its place, using input J2 and output J4, to implement the functionalities shown.

Note: The accuracy of the gain measurement strongly depends on using the same cables in the same positions.

- Switch on the power supplies and check that the current drawn is within the limits shown in Table 7-7.

Voltage	Current
+12 V	150 mA
- 12 V	350 mA
+5 V	1300 mA

Table 7-7—Power Supply Parameters

- Wait 5 minutes for the EMV – TEST CMR to reach operating temperature.
- Set up the EMV – TEST CMR relays as shown in Table 7-8 :

Relay	
Input	J2
Clock	Internal recovery
Amplifier	Buffer

Table 7-8—EMV – TEST CMR settings

- Make sure that the Waveform Generator is still set to generate a 13.56 MHz sine wave with an amplitude of 1 V peak to peak into 50Ω .
- Measure the peak to peak amplitude on CH0 of the DSO.

11. Calculate the gain by dividing the voltage measured in step 10 by the voltage measured in step 3.

Acceptance Criteria

The EMV – TEST CMR gain shall be within 1% of the value specified in the EMV – TEST CMR verification report provided by the EMV – TEST CMR supplier.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

Failure Action

A fail message requires the following actions:

- x Report failure to EMVCo and request advice.
- x Wait until EMVCo gives feedback before starting any such test.

7.5. EMV TEST PCD and EMV TEST PICC Cross Verification

The following procedure shall take place in an environment where the temperature is $23^{\circ}\text{C} \pm 3^{\circ}\text{C}$ and the relative humidity is $50\%\text{RH} \pm 10\%\text{RH}$.

Note: To avoid the possibility of damaging the DSO used in this procedure, make sure that the voltage provided by the signal generator and entering DSO does not exceed the power handling limits of the DSO.

7.5.1. Cross Verifying the EMV TEST PCD and the EMV TEST PICC

Follow this procedure for the cross verification:

1. Refer to the diagram in Figure 7-10 :

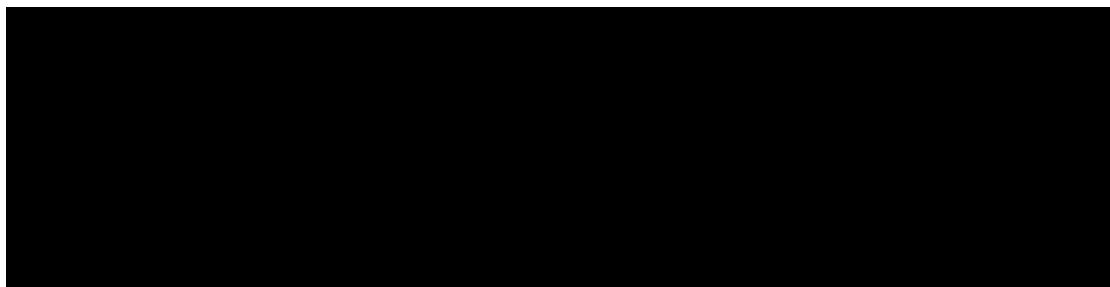


Figure 7-10—Diagram for the EMV – TEST PCD and EMV – TEST PICC Cross Verification

2. Connect appropriate devices so as to implement the functionalities shown.
3. Set the Waveform Generator frequency to 13.56 MHz.
4. Set the signal generator to obtain 15.5 Vpp on CH0 of the DSO.

5. Switch the amplifier off and disconnect the cable to CH0 of the DSO.

6. Refer to the diagram in Figure 7-11 :

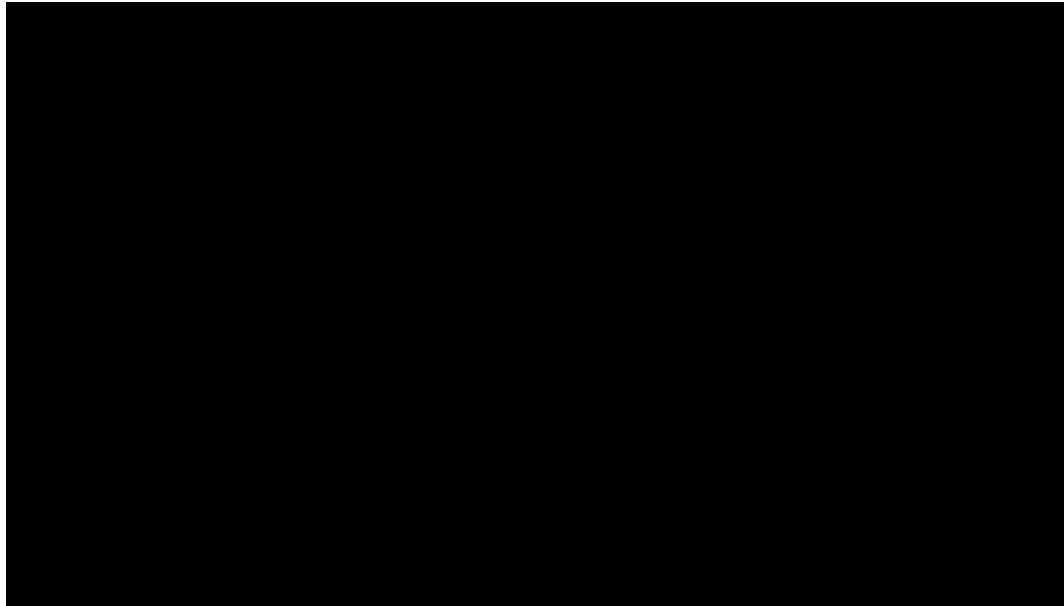


Figure 7-11—Diagram for the EMV – TEST PCD and EMV – TEST PICC Cross Verification

7. Connect appropriate devices so as to implement the functionalities shown.

8. Place the EMV – TEST PICC at position (2, 0, 0) above the EMV – TEST PCD.

9. Measure the voltage at J1 of the EMV – TEST PICC.

10. Repeat steps 1 to 9 five times and calculate the average value of the five voltage measurements obtained.

Acceptance Criteria

Verification is successful if the voltage measured at input J1 of the EMV – TEST PICC is 5.53 ± 0.10 V DC.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

Failure Action

A fail message requires the following actions:

- x Request another verification of the EMV – TEST PCD.
- x Request another verification of the EMV – TEST PICC

8. PCD Analogue Test Plan

8.1. Prerequisites

Before proceeding with the PCD analogue test plan and its Test Cases, the Testing Laboratory shall use the knowledge acquired in previous chapters to construct a test environment.

Before performing Test Cases for PCDs, make sure that Test Laboratory staff:

- x Is familiar with the positioning conventions and requirements (see Chapter 3).
- x Is familiar with the EMV Test Equipment (see Chapter 4).
- x Is familiar with the recommendations for Frame Delay Time Measurements (see Appendix E).
- x Has built a Test Bench for PCD testing that conforms to specifications (see Chapter 5).
- x Has verified the EMV Test Equipment (see Chapter 7).
- x Has established and maintains measurement uncertainty calculations as described in the ISO/IEC 17025 standard.

Note: If necessary, refer to Appendix D for a detailed description of a specific Test Bench implementation.

8.2. Understanding the Two Types of Modulation

Before performing the Test Cases and set up the EMV Test Equipment, the Testing Laboratory shall become familiar with the two types of load modulation used in the tests found in this manual.

8.2.1. Type A Load Modulation

Figure 8-1 shows the Type A load modulation envelope signal:

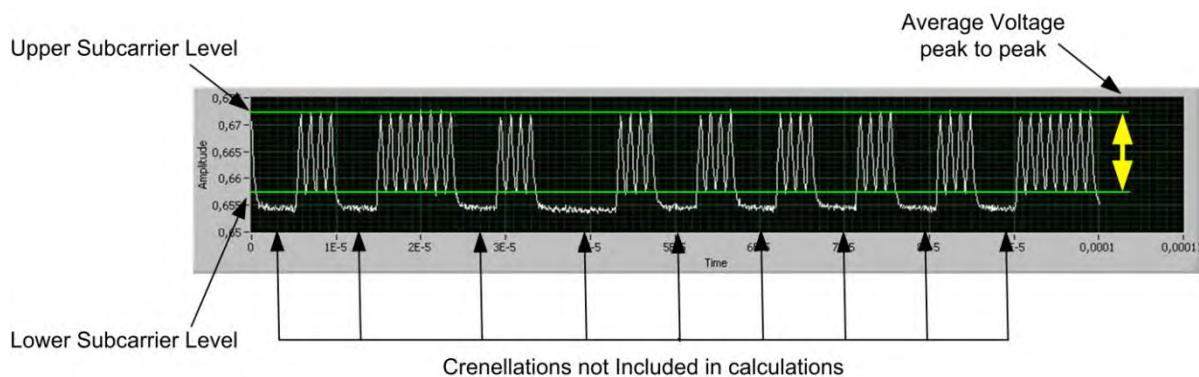


Figure 8-1—Type A Load Modulation Signal

An Acquisition Device acquires the Type A load modulation signal at the output J4 of the EMV – TEST CMR.

Note: The crenellations in Figure 8-1 are not included in the calculations.

Figure 8-2 shows a close-up of the 7 cycles subject to calculation by the automated measurement:

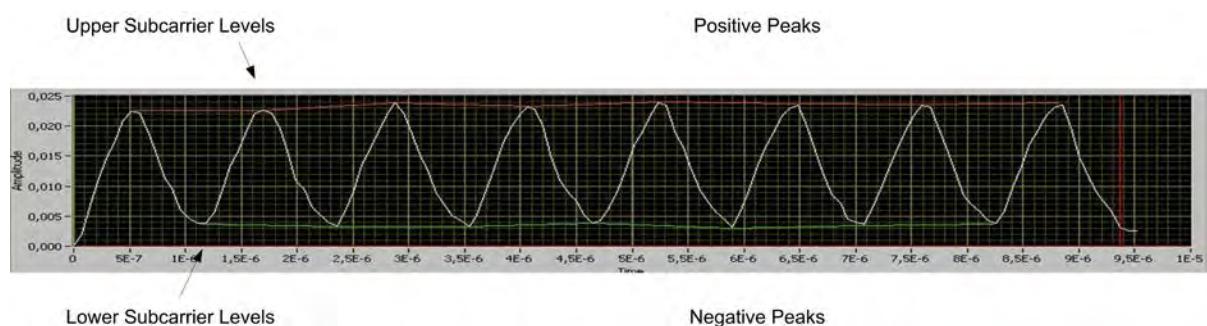


Figure 8-2—Type A Load Modulation

Over at least seven successive subcarrier cycles of the same phase state, the automated measurement shall calculate the difference between the average value of all the positive peaks (upper carrier levels) and the average value of all the negative peaks (lower carrier levels).

8.2.2. Type B Load Modulation

Figure 8-3 shows the Type B load modulation signal after synchronous peak sampling:

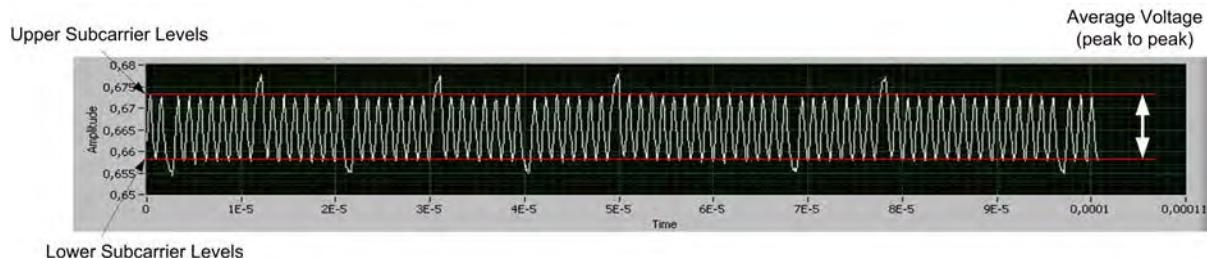


Figure 8-3—Type B Load Modulation Signal

An Acquisition Device acquires the Type B load modulation signal at the output J4 of the EMV – TEST CMR.

See Figure 8-4 for a close-up of the 8 cycles subject to calculation by the automated measurement for Type B load modulation.

Note: Peaks due to phase transitions shall not be taken into account for the load modulation measurement.

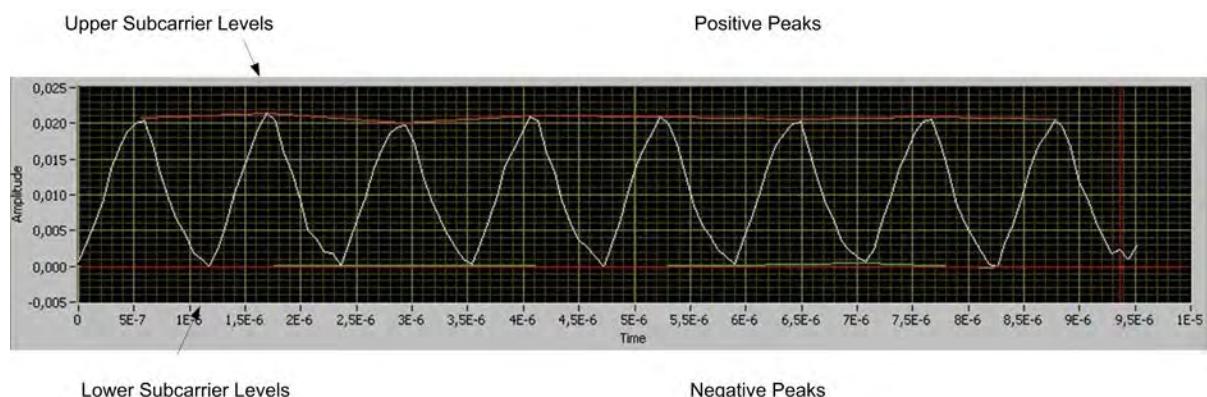


Figure 8-4—Type B Load Modulation

Over at least seven successive subcarrier cycles of the same phase state, the automated measurement shall calculate the difference between the average value of all the positive peaks (upper carrier levels) and the average value of all the negative peaks (lower carrier levels).

8.3. Preliminary Set-ups

Before performing the Test Cases, it is necessary to set up the EMV Test Equipment.

Note: The EMV – TEST CMR does not require any set-up.

The set-up of the EMV Test Equipment for PCD testing comprises two steps:

- x Setting up the EMV – TEST PCD
- x Setting up the EMV – TEST PICC

The EMV – TEST PCD field strength shall be a known value to allow subsequent set-up of the EMV – TEST PICC. These two steps shall be performed sequentially as described and as a single pass procedure as they are dependent

Note: Unless specified otherwise in the test case description, a positive load modulation shall be used.

Note: Even when a specific DTE mode is mentioned in a Test Case procedure, the “loopback” mode may be used during all Type Approval test cases, provided that the software of the Test Bench is capable of correctly setting the required test conditions and of correctly measuring the requested signal(s) at the appropriate moment.

8.3.1. Setting up the EMV TEST PCD Power/EMV TEST PICC Positive Load Modulation Intensity

This set-up involves two steps:

- x Setting up the power of the EMV – TEST PCD
- x Setting up the EMV – TEST PICC positive load modulation intensity

A PCD emulation provides a carrier signal to the EMV – TEST PCD. A Power Sensing Device connected to J1 on the EMV – TEST PICC measures the power sent by the PCD emulation through the EMV – TEST PCD.

Note: When setting up the EMV – TEST PCD, the power sent by the RF Amplifier output shall never exceed 1 W. For example, when connecting the RF Amplifier output to a DSO channel set to 50 Ω, the output shall never measure more than 20 V peak to peak.

Follow this procedure for the EMV – TEST PCD power set-up and EMV – TEST PICC positive load modulation intensity set-up:

1. Refer to Figure 8-5:

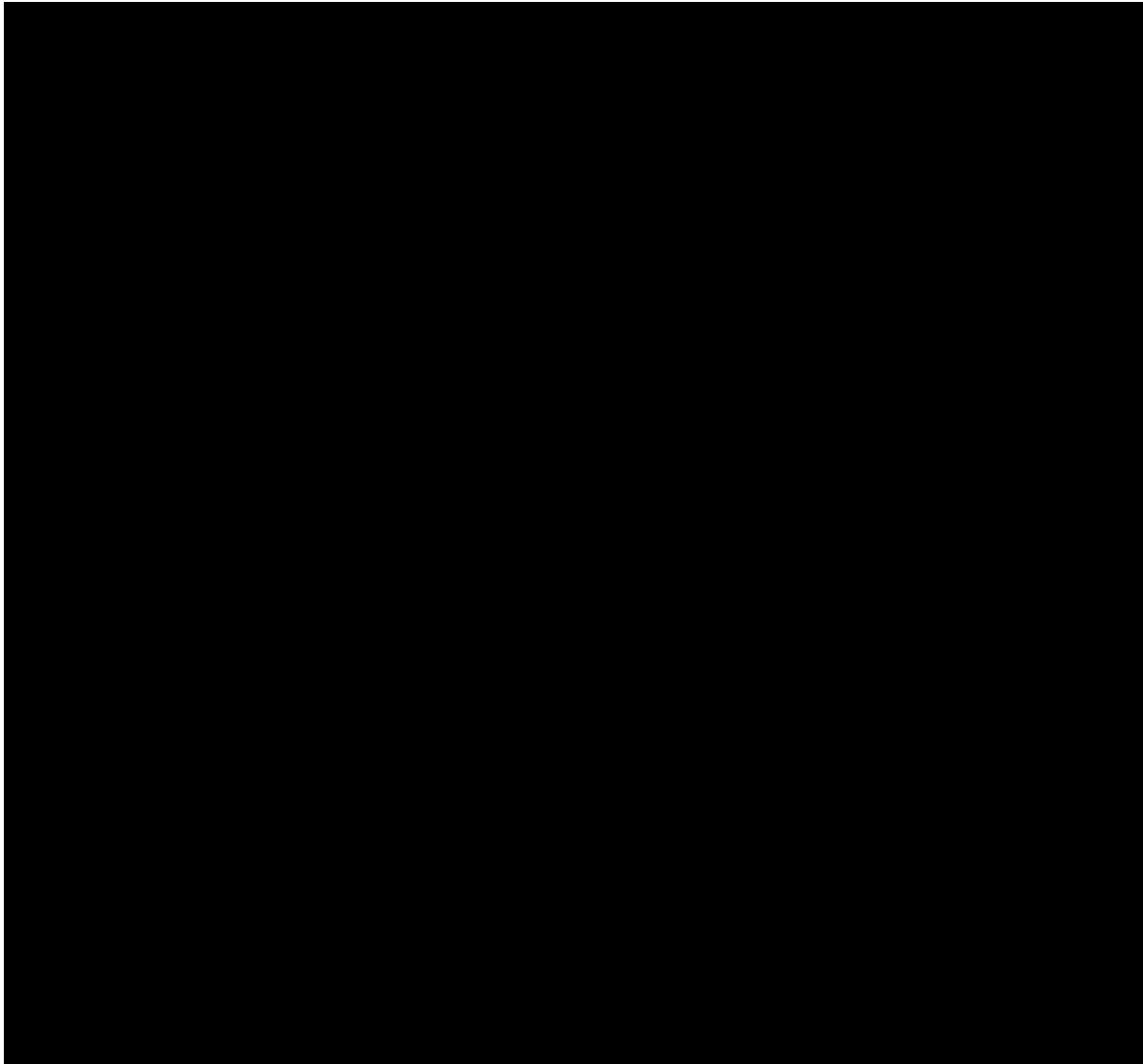


Figure 8-5—Block Diagram for the EMV – TEST PCD Power Set-up and EMV- Test PICC Positive Load Modulation Intensity Set-up

Note: In this set-up procedure, if the PICC Emulation Device needs an external trigger to generate PICC answers, this signal is not issued by the Synchronization Device but by a Waveform Generator. Such a component shall generate a trigger signal with a delay between triggers equal to or greater than 100 ms and with a format matching the specification of the PICC emulation trigger input.

2. Connect appropriate Test Bench devices so as to implement the functionalities shown in Figure 7.5 except the connection to J2 of the EMV – TEST PICC.
3. Set up the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Place the EMV – TEST PICC at position ($z=2$, $r=0$, $\varphi=0$) on the EMV – TEST PCD.

5. Adjust the PCD Emulation Device to send a 13.56 MHz sine wave.
6. Set the Power Sensing Device time scale to allow averaging over 10 μ s to 200 μ s and the voltage scale to an appropriate level and offset to give best accuracy.
7. Measure the average voltage V_{OV} at output connector J1 of the EMV – TEST PICC.
8. If the measured V_{OV} is the value $V_{N,OV}$ defined in Table B.1 of Appendix B, go to step 9. If it is not, adjust the waveform amplitude of the PCD Emulation Device and repeat steps 6 and 7.
9. Remove the EMV – TEST PICC from the Operating Volume of the EMV – TEST PCD.
10. Connect the end of the cable installed in step 2 to J2 of the EMV – TEST PICC.
11. Set the EMV – TEST CMR with the control software as shown in Table 8-1:

Function	Setting
Input	J2
Clock	CLK IN (internal recovery)
Amplifier	Buffer

Table 8-1—CMR Parameter Settings

12. Place the EMV – TEST PICC in the appropriate position on the EMV – TEST PCD. The exact position depends on the test being performed:
 - a) For the $V_{S1,pp}$, test, the position is ($z=0$, $r=0$, $\varphi=0$).
 - b) For the $V_{S2,pp}$ test, the position is ($z=2$, $r=0$, $\varphi=0$).
13. Set the PICC Emulation device to generate negative load modulation.
14. Send a correct Type A or Type B PICC answer with a content equivalent to a Response to Select PPSE Command as defined in Appendix C.
15. Set the EMV – TEST CMR delay lines DL1+DL2 until the maximum amplitude is observed on the Acquisition Device.
16. In case of minimum load modulation setup, set the Acquisition Device x-axis to capture the last 7 contiguous subcarrier cycles without phase change of the PICC response to Select PPSE command.

In case of nominal or maximum load modulation setup, set the Acquisition Device x-axis to capture the first 7 contiguous subcarrier cycles of the PICC response to Select PPSE command.
17. Set the Acquisition Device vertical scale to maximum.

The automated test bench set-up measures the load modulation as the difference between the average value of upper subcarrier peaks and the average value of subsequent lower subcarrier peaks at the output J4 of the EMV – TEST CMR.

18. If the measured load modulation level is not the one required for the test, set the amplitude of the signal on input J2 of the EMV – TEST PICC.
19. Repeat step 17 and 18 until the required value for load modulation is reached.
20. Remove the EMV – TEST PICC from the Operating Volume of the EMV – TEST PCD.

Note: The PICC Emulation device works properly if the output J2 of the EMV – TEST PCD shows an increasing voltage above the unmodulated carrier when the subcarrier is switched on, as shown in Figure 7.6. Unless specified in the Test Cases, the envelope of the output J2 of the EMV – TEST PCD shows an increasing voltage above the unmodulated carrier when the subcarrier is switched on, as shown in Figure 8-6. In some test cases, inverted load modulation is applied as shown in Figure 8-8.

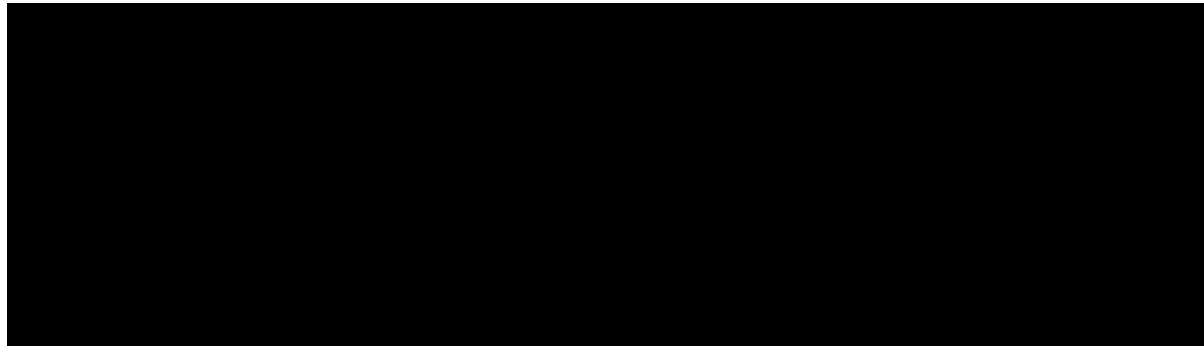


Figure 8-6—Positive load modulation

8.3.2. Setting up the EMV TEST PCD Power/EMV TEST PICC Negative Load Modulation Intensity

This set-up involves two steps:

- x Setting up the power of the EMV – TEST PCD
- x Setting up the EMV – TEST PICC negative load modulation intensity

A PCD emulation provides a carrier signal to the EMV – TEST PCD. A Power Sensing Device connected to J1 on the EMV – TEST PICC measures the power sent by the PCD emulation through the EMV – TEST PCD.

Note: When setting up the EMV – TEST PCD, the power sent by the RF Amplifier output shall never exceed 1 W. For example, when connecting the RF Amplifier output to a DSO channel set to 50 Ω, the output shall never measure more than 20 V peak to peak.

Follow this procedure for the EMV – TEST PCD power set-up and EMV – TEST PICC negative load modulation intensity set-up:

1. Refer to Figure 8-7:

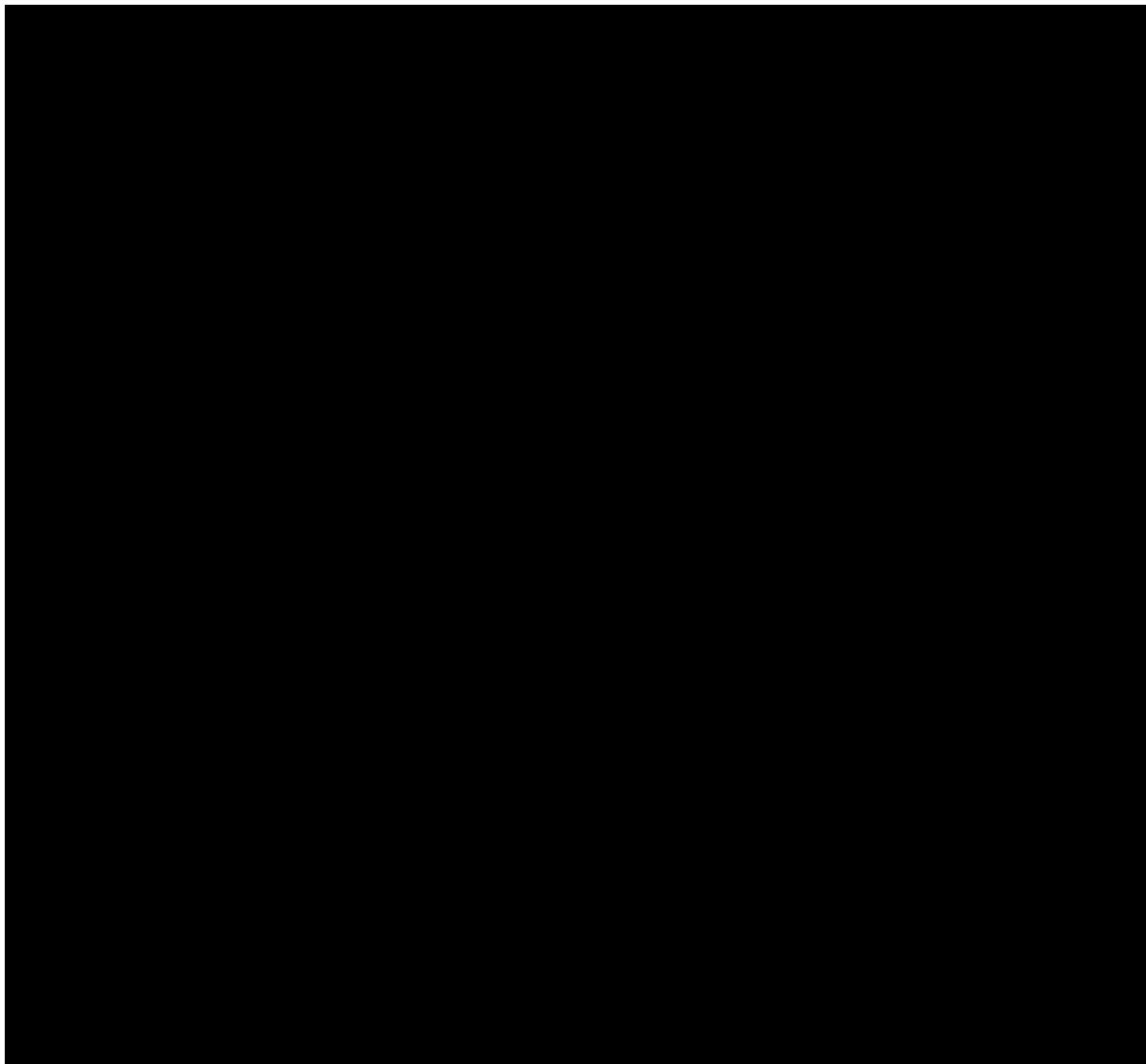


Figure 8-7—Block Diagram for the EMV – TEST PCD Power Set-up and EMV- Test PICC Negative Load Modulation Intensity Set-up

Note: In this set-up procedure, if the PICC Emulation Device needs an external trigger to generate PICC answers, this signal is not issued by the Synchronization Device but by a Waveform Generator. Such a component shall generate a trigger signal with a delay between triggers equal to or greater than 100 ms and with a format matching the specification of the PICC emulation trigger input.

2. Connect appropriate Test Bench devices so as to implement the functionalities shown in Figure 8-7 except the connection to J2 of the EMV – TEST PICC.
3. Set up the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Place the EMV – TEST PICC at position ($z=2$, $r=0$, $\varphi=0$) on the EMV – TEST PCD.

5. Adjust the PCD Emulation Device to send a 13.56 MHz sine wave.
6. Set the Power Sensing Device time scale to allow averaging over 10 μ s to 200 μ s and the voltage scale to an appropriate level and offset to give best accuracy.
7. Measure the average voltage V_{OV} at output connector J1 of the EMV – TEST PICC.
8. If the measured V_{OV} is the value $V_{N,OV}$ defined in Table B.1 of Appendix B, go to step 9. If it is not, adjust the waveform amplitude of the PCD Emulation Device and repeat steps 6 and 7.
9. Remove the EMV – TEST PICC from the Operating Volume of the EMV – TEST PCD.
10. Connect the end of the cable installed in step 2 to J2 of the EMV – TEST PICC.
11. Set the EMV – TEST CMR with the control software as shown in Table 8-2:

Function	Setting
Input	J2
Clock	CLK IN (internal recovery)
Amplifier	Buffer

Table 8-2—CMR Parameter Settings

12. Place the EMV – TEST PICC in the appropriate position on the EMV – TEST PCD. The exact position depends on the test being performed:
 - a) For the $V_{S1,pp}$ test, the position is ($z=0, r=0, \varphi=0$).
 - b) For the $V_{S2,pp}$ test, the position is ($z=2, r=0, \varphi=0$).
13. Set the PICC Emulation device to generate negative load modulation.
14. Send a correct Type A or Type B PICC answer with a content equivalent to a Response to Select PPSE Command as defined in Appendix C.
15. Set the EMV – TEST CMR delay lines DL1+DL2 until the maximum amplitude is observed on the Acquisition Device.
16. In case of minimum load modulation setup, set the Acquisition Device x-axis to capture the last 7 contiguous subcarrier cycles without phase change of the PICC response to Select PPSE command.
In case of nominal or maximum load modulation setup, set the Acquisition Device x-axis to capture the first 7 contiguous subcarrier cycles of the PICC response to Select PPSE command.
17. Set the Acquisition Device vertical scale to maximum.
The automated test bench set-up measures the load modulation as the difference between the average value of upper subcarrier peaks and the average value of subsequent lower subcarrier peaks at the output J4 of the EMV – TEST CMR.
18. If the measured load modulation level is not the one required for the test, set the amplitude of the signal on input J2 of the EMV – TEST PICC.

19. Repeat step 17 and 18 until the required value for load modulation is reached.
20. Remove the EMV – TEST PICC from the Operating Volume of the EMV – TEST PCD.

Note: The PICC Emulation device works properly if the output J2 of the EMV – TEST PCD shows a decreasing voltage below the unmodulated carrier when the subcarrier is switched on, as shown in Figure 8-8—Negative load modulation.

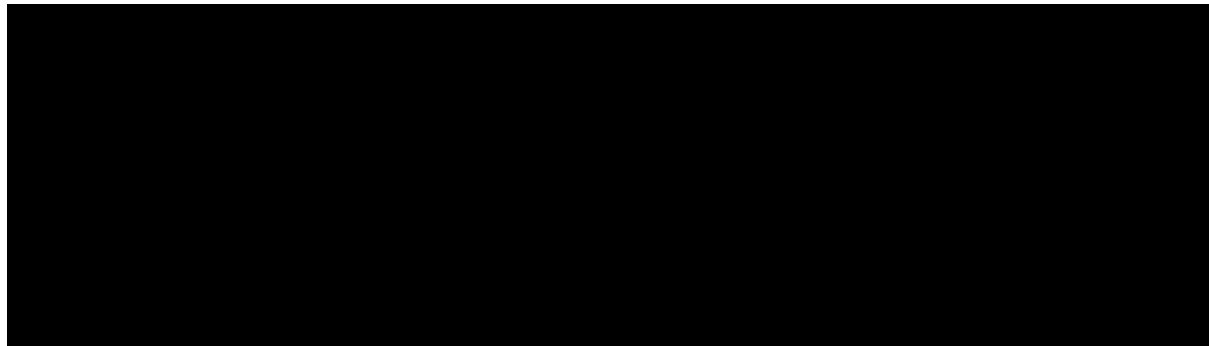


Figure 8-8—Negative load modulation

8.4. Set-up of the PCD Under Test

By default, all PCD functions shall be considered deactivated and the polling for technologies (different from Type A and Type B transactions) disabled. The PCD set-up required for each Test Case is described in the test procedures.

When present on the PCD Under Test, the screen of the PCD Under Test shall remain turned on during all the Test Session.

Before any test, the PCD Under Test shall be set up with one of the different control possibilities described below:

- x Continuous sending of the carrier with no polling (CARRIER mode).
- x The PCD polls (POLLING mode) in two ways:
 - o The PCD polls as described in section 9.2 of the *EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification*, if the polling for other technologies is enabled.
 - o The PCD polls between Type A and Type B, sending WUPA and WUPB commands only if the polling for other technologies is disabled.
- x The PCD generates a RESET (RESET Mode).
- x The PCD sends a WUPA command (WUPA mode).
- x The PCD sends a WUPB command (WUPB mode).
- x The PCD sends the commands of the Collision Detection procedure as described in section 9.3.2 of the *EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification*, and the commands of the activation procedure described in section 9.4.1 of the *EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification (RATS Mode)*.
- x The PCD sends the commands of the Collision Detection procedure as described in section 9.3.3 of the *EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification* and the commands of the activation procedure described in section 9.4.2 of the *EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification (ATTRIB Mode)*.
- x The PCD activates the Loopback application (LOOPBACK mode).
- x The PCD activates the Transaction Send application, either for Type A (TRANSAC_A mode) or for type B (TRANSAC_B mode).

Otherwise unless specified in the Test Cases, other technologies shall be disabled.

For further information on this DTE, see Appendix A of the *EMVCo Type Approval Contactless Terminal Level 1/ Device Test Environment* document.

When Type A or Type B transactions are used, the following factors must be taken into account:

- x Polling for other technologies is disabled.
- x The WUPA, WUPB, RATS and ATTRIB modes all require that a carrier be active prior to the polling activity.

8.5. Identifying PCD Test Cases

To facilitate future referencing, all PCD Test Cases shall be identified by a unique label according to the following format:

ZLCN. zrf

Where:

- x Z is the PCD data transmission type:

TAB = both PCD data transmission Type A and Type B

TA = PCD data transmission Type A

TB = PCD data transmission Type B

- x L is the level of the test (level 1 Type Approval Tests described).

- x C is the test category:

1 = Radio frequency power tests

2 = Signal interface PCD to PICC tests

3 = Signal interface PICC to PCD tests

4 = Sequence, Frame bit coding and synchronization tests

- x N is the number of the test in the specified category

z, r and f are identifiers for label points, as defined in Chapter 3, section 3.4.1 Target Position Conventions.

8.6. Measurement Uncertainty

Testing Laboratories shall have and shall apply procedures for estimating uncertainty of measurement. The ISO/IEC 17025, ISO 5725 and the Guide to the expression of Uncertainty of Measurement requirements allow the Testing Laboratory to evaluate the accuracy, repeatability and reproducibility of its own test results and to properly determine and quantify sources of error.

These procedures are essential feedback mechanisms enabling the Test Laboratory to improve the quality of its measurements. This is done by minimizing the identified sources of error through optimization of methods and procedures.

For each test method, according to the present document, the Testing Laboratory shall calculate measurement uncertainty figures. These shall correspond to an expansion factor (coverage factor) of $k = 1.96$ (which provides a confidence level of 95 % in the case where the distributions characterizing the actual measurement uncertainties are normal (Gaussians). Table 8-3, Table 8-4 and Table 8-5 are based on such expansion factors.

The estimation of measurement uncertainties shall be done according to recognized international methods. When estimating the uncertainty of measurement, all uncertainty components which are relevant and significant in the given situation shall be taken into account using appropriate methods of analysis.

Sources contributing to uncertainty include, but are not limited to:

- x Reference standards
- x Methods and equipment
- x Environmental conditions
- x Effects of positional accuracy
- x Mismatches
- x Cable losses
- x Sampling rates and timing factor
- x Operator skills
- x Properties and condition of the tested samples

For further information, see the Guide to the Expression of Uncertainty in Measurement, ISO/IEC Guide 98:1995.

Parameter	Uncertainty
$V_{S,ov}$	$\pm 2 \%$
Carrier frequency	$\pm 100 \text{ Hz}$
Load modulation (V_{S1}, V_{S2})	$\pm 1 \text{ mV}$
Bit rate (PICC Load Modulation)	$\pm 0.2 \%$
Type B PICC bit coding set-up ($t_{\text{PICC},S,1}, t_{\text{PICC},S,2}, t_{\text{PICC},E}, EGT_{\text{PICC}}$)	$\pm 2/fc$
Type B PICC TR0, TR1, t_{FSOFF}	$\pm 2/fc$
$FDT_{A,\text{PICC}}$	$\pm 1/fc$

Table 8-3—Parameter and Signal Generation Uncertainty Range

Parameter	Uncertainty
Positioning (z, r)	$\pm 1 \text{ mm}$
Positioning (ϕ, θ)	$\pm 0.1 \text{ rad}$
Temperature	$\pm 1^\circ\text{C}$
Humidity	$\pm 3 \%$

Table 8-4— Parameter and Environmental Condition Uncertainty Range

Parameter	Uncertainty
V_{ov}	$\pm 2 \%$
Carrier frequency	$\pm 100 \text{ Hz}$
Load modulation (V_{pp})	$\pm 10\% \text{ with a minimum of } 1 \text{ mV}$
Type A timing (t_1, t_2, t_3, t_4, t_5)	$\pm 2/\text{fc}$
Type A ringing level	$\pm 0.5 \% \text{ of } V_1$
Type A overshoots	$\pm 0.5 \% \text{ of } V_1$
Bit rate (PCD Type A / Type B modulation)	$\pm 0.5 \%$
Type B modulation index	$\pm 0.5 \%$
Type B rise and fall times	$\pm 2/\text{fc}$
Type B overshoots and undershoots	$\pm 1 \% \text{ of } (V_1 - V_2)$
Type B bit coding ($t_{PCD,S,1}, t_{PCD,S,2}, t_{PCD,E}, EGT_{PCD}$)	$\pm 2/\text{fc}$

Table 8-5— Parameter and Measurement Uncertainty Range

Note: The previous tables include the mismatch effects and the effects on measurements in the near field due to positional accuracy.

Note: For the peak sampling method using the EMV – TEST CMR, the delay line shall be adjusted until the maximum amplitude is reached on the Acquisition Device.

Note: When establishing measurement points with a cursor (or its equivalent), unless otherwise stated in the test procedure, always use the reference points as specified in Appendix E. Do this consistently to maintain measurement accuracy.

8.7. Interpretation of the Measurement Results

The interpretation of the results recorded in a test report for the measurements described in the present document shall be as follows:

- x The value of the measurement uncertainty for the measurement of each parameter shall be included in the test report.
- x The recorded value of the measurement uncertainty shall be, for each measurement, equal to or lower than the values in Table 8-3, Table 8-4 and Table 8-5.
- x The shared risk approach shall be applied for the interpretation of measurement results.

Note: The shared risk approach is an agreement on limits between the vendor and the regulator.

8.8. Performing PCD Test Cases

When Test Cases are performed, results are normally a PASS or a FAIL verdict.

The following procedure applies to each test case from TA131 up to and including TA138 for Type A and from TB131 up to and including TB138 for Type B (i.e. for each position and each test subcase):

- x It is allowed to run each test subcase a maximum of six times.
 - x When three consecutive runs of the same test subcase succeed, record a PASS message and proceed to the next test subcase.
 - x After performing the sixth test run of the same test subcase without three consecutive successes, record a FAIL message and proceed to the next test subcase.

It is not allowed to run any test subcase from TA131 up to and including TA138 for Type A and from TB131 up to and including TB138 for Type B more than six times during one Type Approval session.

For all other Test Cases, the following procedure applies (i.e. for each position and each test subcase):

- x It is allowed to run each test subcase a maximum of three times.
 - x When one run of the same test subcase succeed, record a PASS message and proceed to the next test subcase.
 - x After performing the third test run of the same test subcase without success, record a FAIL message and proceed to the next test subcase.

It is not allowed to run any of these test subcases more than three times during one Type Approval session.

In the above text, the counting of test times is incremented by one unit each time that the test bench at least starts answering a WUP command from the PCD under test, sent with the modulation type that is concerned by the test case performed.

- x When the PCD under test polls using a modulation type that is not concerned by the test case run, the number of test times shall not be incremented. For example, when running the test TB132, all occurrences of WUPA commands shall be discarded.
- x When the PCD under test polls using the modulation type that is concerned by the test case but the test bench does not answer, the number of test times shall not be incremented. For example, a WUPA command that is not answered by the test bench running test TA124 shall be discarded.
- x Each time that the test bench starts answering a WUP command sent by the PCD under test using the modulation type concerned by the test case performed, the number of test times shall be incremented by one unit.

Note: If the Test PCD has a concave surface to place against the EMV – TEST PICC, you shall follow the recommendations in the "Recommendations for a PCD without a perfectly flat Landing Plane" section in Chapter 6.

The following sections present all the PCD Test Cases. They are presented in the sequence defined in the specifications. Test Cases may be performed in any order unless otherwise specified in a Test Case.

To perform the Test Cases, a Test Bench implementing essential functionalities shall be constructed. Figure 8-9—Block Diagram of the Test Bench to Perform the Test Casesshows the necessary functionalities:

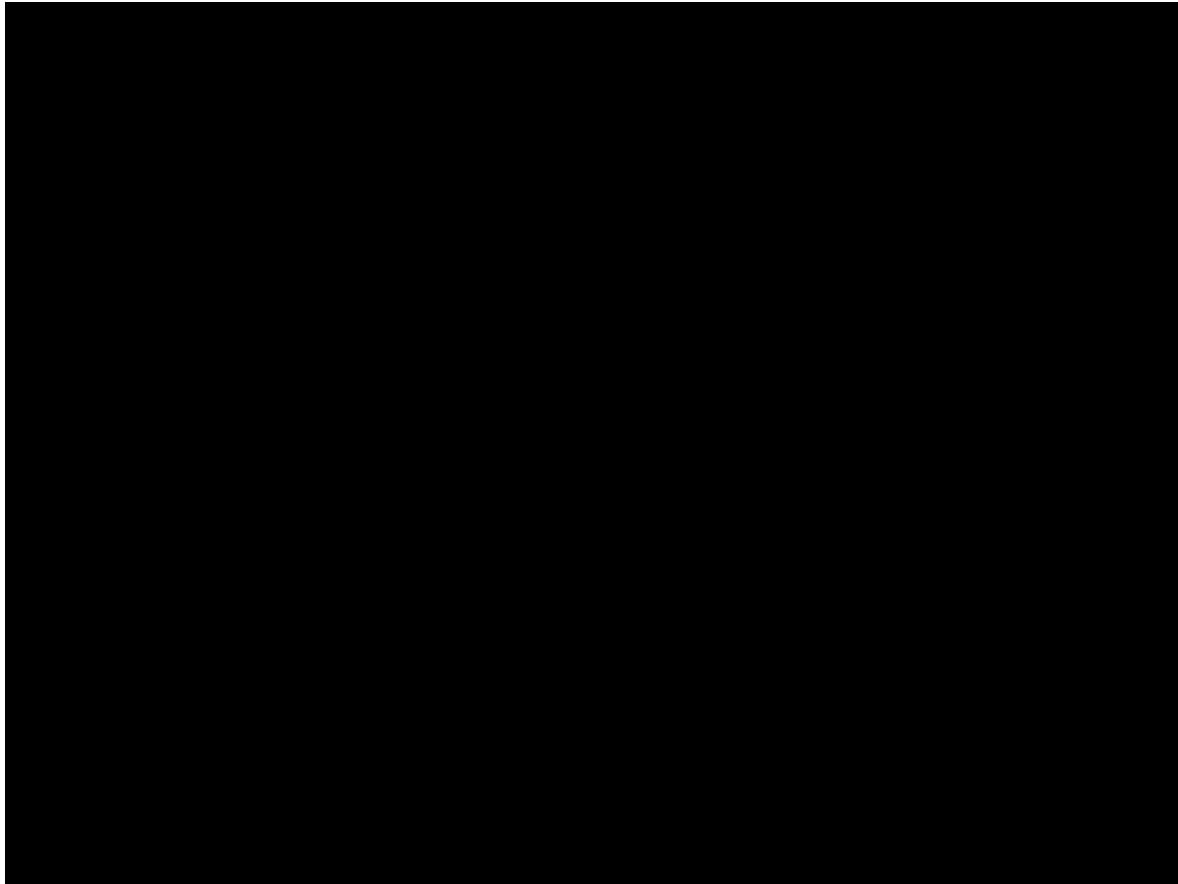


Figure 8-9—Block Diagram of the Test Bench to Perform the Test Cases

Note: Make sure that you carry out any special connections as described in individual Test Cases.

Note: All Test Cases shall be completed without regard to individual test failure.

Note: The use of a low-pass filter fitted between the PICC and the EMV – TEST CMR is highly recommended. The filter shall feature less than 1 dB attenuation at 20 MHz and more than 40 dB attenuation at 40 MHz.

8.8.1. Radio Frequency Power

These tests determine the quality of the radio frequency fields of the PCD under test.

8.8.1.1. TAB111.zrf Verifying the PCD to PICC Power Transfer

This test verifies the power transmission from the PCD to the PICC.

Test Code

TAB111.zrf

Reference

This test refers to requirement 3.2.1.1.

Test Positions

Use Table 8-6 for the test positions during verification of the power transmission from the PCD to the PICC:

Value for z	Value for r	Value for f
0	0	0
0	1	0
0	1	3
0	1	6
0	1	9
1	0	0
1	2	0
1	2	3
1	2	6
1	2	9
2	0	0
2	2	0
2	2	3
2	2	6
2	2	9
3	0	0
3	2	0
3	2	3
3	2	6
3	2	9
4	0	0
4	1	0

Value for z	Value for r	Value for f
4	1	3
4	1	6
4	1	9

Table 8-6—Test Positions of Test TAB111.zrf

Procedure

Follow this procedure to verify the power transmission from the PCD to the PICC:

1. Connect the Power Sensing Device to output J1 of the EMV – TEST PICC.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1 - 3 and J8 1- 4).
5. Make sure that the CARRIER is switched on.
6. Place the EMV – TEST PICC in the first position of Table 8-6—Test Positions of Test TAB111.zrf.
7. Set the Power Sensing Device to capture 10 μ s of the full level unmodulated signal.
8. Optimize the Power Sensing Device settings for the accurate measurement of amplitude.
9. Launch the acquisition.
10. Determine the true mean value of voltage V_{OV} at output J1 of the EMV – TEST PICC.
11. Repeat steps 8 to 10 for all other positions of Table 8-6

Acceptance Criteria

Within the Operating Volume, the PCD shall generate a DC voltage V_{OV} at J1 of the EMV – TEST PICC. Refer to Table A.1 in Appendix A for the applicable range of V_{OV} mean values.

Note: When testing PCDs without a perfectly flat landing plane, refer to section 6.2.2. above and adjust the acceptance criteria according to the actual z distance used during testing. The distance is taken from the center of the EMV – Test PICC.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met

8.8.1.2. TAB112.200 Verifying the PCD Carrier Frequency

This test verifies the carrier frequency emitted by the PCD under test.

Note: This test requires the use of a Frequency Counter or its functional equivalent in an instrument such as a DSO.

Test Code

TAB112.200

Reference

This test refers to requirement 3.2.4.1.

Procedure

Follow this procedure to verify the carrier frequency emitted by the PCD under test:

1. Connect the Frequency Counter to output J9 of the EMV – TEST PICC.

Note: Alternatively, the laboratory may use the following connection scheme:
Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.

2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a non-linear load (jumper setting J7 1-3 and J8 1-4).
5. Make sure that the CARRIER is switched on.
6. Place the EMV – TEST PICC at position ($z=2$, $r=0$, $\phi=0$).
7. Optimize the Acquisition Device settings for the accurate measurement of frequency.
8. Launch the acquisition.
9. Determine the mean value during the acquisition period of the carrier frequency on connector J9 of the EMV – TEST PICC.

Acceptance Criteria

The frequency of the Operating Field (carrier frequency) provided by the PCD shall be $13.560\text{ MHz} \pm 7\text{ kHz}$.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.1.3. TAB113.z00 Verifying the PCD Operating Field Resetting

This test verifies how the PCD resets the Operating Field.

Test Code

TAB113.z00

Reference

This test refers to requirement 3.2.6.1.

Test Positions

Use Table 8-7 for the test positions during verification of the power transmission from the PCD to the PICC:

Value for z	Value for r	Value for f
0	0	0
1	0	0
2	0	0

Table 8-7—Test Positions of Test TAB113.z00

Procedure

Follow this procedure for verification of the PCD Operating Field reset:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
5. Place the EMV – TEST PICC in the first position of Table 8-7.
6. Make sure that the CARRIER is switched on.
7. Set the Acquisition Device to capture more than 20 ms of signal from the start of the PCD reset of the Operating Field.
8. Optimize the Acquisition Device settings for the accurate measurement of amplitude.
9. Launch the acquisition.
10. Make the PCD under test reset the PCD Operating Field.
11. Measure the RMS voltage of a 20 MHz band limited signal at the output of the EMV – TEST CMR during the reset of the PCD.

12. Measure the time of the reset t_{RESET} from the point at which the voltage of the envelope first falls below $V_{OV,RESET,MAX} \times \sqrt{2}$ until it last rises above $V_{OV,RESET,MAX} \times \sqrt{2}$ at the end of the reset period. The appropriate value of $V_{OV,RESET,MAX}$ is shown in the maximum column of $V_{OV,RESET}$ in Table A.1 in Appendix A.

13. Repeat steps 8 to 12 for all other positions of Table 8-7.

Acceptance Criteria

When the PCD resets the Operating Field, then within the Operating Volume, the PCD shall generate for a time t_{RESET} a voltage less than or equal to the RMS value of $V_{OV,RESET}$ at the output of the pickup coil of the EMV – TEST PICC. The time interval t_{RESET} shall conform to the values shown in Table A.5 in Appendix A and the value of $V_{OV,RESET}$ shall conform to the values shown in Table A.1 in Appendix A

Note: As a low pass filter is used, the measurement of the signal shall be corrected according to its insertion loss at 13.56 MHz.

Note: The measurement should take into account any DC offset introduced by the EMV TEST CMR. This can be achieved for example by measuring the CMR J4 output voltage when no signal is generated, and using a compensated threshold voltage formula : threshold = CMR_{offset} + ($V_{OV,RESET,MAX} \times \sqrt{2}$).

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.1.4. TAB114.200 Verifying the PCD Power-Off of the Operating Field

This test verifies how the PCD performs a power-off of the Operating Field.

Test Code

TAB114.200

Reference

This test refers to requirement 3.2.9.1.

Procedure

Follow this procedure for verification of the PCD power-off of the Operating Field:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a nominal positive load modulation $V_{S1,pp}$. See Chapter 8, section 8.3.1 for details and Table B.1 in Appendix B for the value of $V_{S1,pp}$. In this test case, the EOT Command must be set to “Power-Off procedure”.
5. Place the EMV – TEST PICC at position ($z=2$, $r=0$, $\varphi=0$).
6. Set the DTE in LOOPBACK mode.
7. Set the Acquisition Device to capture more than 20 ms of signal from the start of the PCD power-off of the Operating Field at the end of the transaction.
8. Optimize the Acquisition Device settings for the accurate measurement of amplitude.
9. Launch the acquisition.
10. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests. The second byte of the EOT Command shall be equal to ‘72’.
11. Place an X-cursor or its equivalent to identify the time when the voltage of the envelope first falls below $V_{OV,POWEROFF,MAX} \times \sqrt{2}$. This cursor shall be referenced as X1.
12. Place an X-cursor or its equivalent to identify the time ($X1 + t_{POWEROFF,MIN}$) after the X1 start cursor. This cursor shall be referenced as X2.
13. Place an Y-cursor or its equivalent to identify the voltage $V_{OV,POWEROFF,MAX}$. This cursor shall be referenced as Y1.
14. Measure the RMS voltage of a 20 MHz band limited signal at the output of the EMV – TEST CMR during the power-off of the Operating Field, i.e. between the cursors X1 and X2.

Acceptance Criteria

When the PCD performs a power-off of the Operating Field, the PCD shall, during a time $t_{POWEROFF,MIN}$, generate a RMS voltage less than or equal to $V_{OV,POWEROFF,MAX}$ at the output of the pickup coil of the EMV – TEST PICC. The value of $V_{OV,POWEROFF,MAX}$ shall conform to the values shown in Table A.1 in Appendix A.

Note: As a low pass filter is used, the measurement of the signal shall be corrected according to its insertion loss at 13.56 MHz.

Note: The measurement should take into consideration any DC offset introduced by the EMV TEST CMR. This can be achieved for example by measuring the CMR J4 output voltage when no signal is generated, and using a compensated threshold voltage formula : threshold = CMR_{offset} + ($V_{OV,POWEROFF,MAX} \times \sqrt{2}$).

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met

8.8.1.5. TAB115.200 Polling sequence when supporting other technologies

This test verifies if a PCD is polling correctly when other technologies than Type A and Type B are supported.

This test case is applicable only if the PCD supports other technologies.

Test Code

TAB115.200

Reference

This test refers to requirements 9.2.1.1, 9.2.1.3, 9.2.1.4 and 9.2.1.7.

Procedure

Follow this procedure to verify a PCD is polling correctly when other technologies than Type A and Type B are supported :

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
3. Place the EMV – TEST PICC at position (200).
4. Set the DTE in LOOPBACK mode with other technologies activated.
5. Set the Acquisition Device to capture 60 ms of signal starting 21 ms before the beginning of the WUPA of the polling loop.
6. Record the viewable trace on EMV Test PICC J9 output.
7. Observe the PCD polling sequence and verify that:
 - a) The polling loop is ending with a reset, and measure its duration.
 - b) This reset is followed by the WUPA command of the polling sequence.
 - c) There is no ASK modulation between reset and WUPA.
 - d) This WUPA command is followed by the WUPB command of the polling sequence.
 - e) There is no ASK modulation between WUPA and WUPB.
 - f) There is no ASK modulation after WUPB for at least FWTATQB.

Note: We consider that there is no ASK modulation when the signal does not decrease below $V_1 \times 95\%$ during more than 1 μs and does not increase over $V_1 \times 105\%$ during more than 1 μs , with V_1 being the level of the upper signal envelope between two PCD commands.

Acceptance Criteria

When the PCD supports other technologies :

- × The PCD shall reset the Operating Field during a time t_{RESET} before restarting the polling loop. Refer to Table A.5 in Appendix A.1 for the minimum and maximum t_{RESET} values.
- × The PCD shall wait a time FWT_{ATQB} with unmodulated carrier before sending any proprietary command. Refer to Table A.4 in Appendix A.1 for the minimum FWT_{ATQB} value.

Expected Results

Results are recorded with one of two statements:

- × Pass message
- × Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.2. PCD to PICC Signal Interface for Type A Communications

PCD to PICC Type A communication uses the modulation principle of 100% ASK. The carrier is switched on and off, creating the lower level when switched off. In practice, it results in a modulation index of 90% or higher.

Figure 8-10 shows the lower level for Type A communications:

Figure 8-10—Lower level for Type A communications

In this section, V (voltage) represents the envelope of the signal measured at the output of the pickup coil of the EMV – TEST PICC within the Operating Volume of the PCD. The envelope (V) is obtained by applying a moving average with a period of $1/f_c$ on the magnitude of the complex Hilbert transform of the signal.

V_1 is the level measured immediately before the falling edge preceding a lower level of modulation from PCD. The V_1 level shall be obtained by applying an arithmetic average of the signal envelope over a duration of $20/f_c$ preceding the signal decay.

V_2 , V_3 and V_4 are defined as follows:

$$\begin{aligned}x V_2 &= 0.05 \times V_1 \\x V_3 &= 0.6 \times V_1 \\x V_4 &= 0.9 \times V_1\end{aligned}$$

Note: It is strongly recommended to perform these test cases using the same acquisitions to avoid any random behavior of the PCD under test.

8.8.2.1. TA121.z00 Verifying the t_1 Timing

This test verifies the time between V_4 of the falling edge to V_2 of the rising edge within a given time t_1 .

Test Code

TA121.z00

Reference

This test refers to requirement 3.3.2.1.

Test Positions

Use Table 8-8 for the test positions during verification of the time t_1 between V_4 of the falling edge to V_2 of the rising edge.

Value for z	Value for r	Value for f
0	0	0
1	0	0
2	0	0
3	0	0
4	0	0

Table 8-8—Test Positions of Test TA121.z00

Procedure

Follow this procedure to verify the time t_1 between V_4 of the falling edge to V_2 of the rising edge.

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC in the first position defined in Table 8-8.
6. Make sure that the CARRIER is switched on and set the PCD under test in TRANSAC_A mode.
7. Set the Acquisition Device to capture 50 ms of the PCD signal starting just before the first WUPA command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.

9. Launch the acquisition.
10. Measure, using a cursor or its equivalent, the upper level amplitude V_1 preceding the first falling edge of the PCD command
11. Calculate V_4 as equal to $0.9 \times V_1$ and place a Y-cursor (or its equivalent) to determine the corresponding level.
12. Measure V_2 as equal to $0.05 \times V_1$ and place a Y-cursor (or its equivalent) to determine the corresponding level.
13. Place an X-cursor (or its equivalent) to determine the time where the PCD carrier envelope crosses V_4 for the first time as the carrier envelope decays.
14. Place an X-cursor (or its equivalent) to determine the time where the PCD carrier crosses cursor V_2 for the first time as the carrier envelope increases (excluding any temporary increase above V_2 due to ringing).
15. Determine the timing t_1 , when V decreases through V_4 to when V increases through V_2 , as the difference between the times identified by the two X-cursors.
16. Repeat steps 10 to 15 for all PCD commands.
17. Repeat steps 8 to 16 for all positions defined in Table 8-8.

Acceptance Criteria

V shall decrease from V_4 to less than V_2 and subsequently increase to greater than V_2 in time interval t_1 . The time interval t_1 shall conform to the values shown in Table A.2 in Appendix A.

Expected Results

Results for each position including the minimum, maximum and average of all measurements performed (i.e. the sum of all results at the concerned position divided by the number of results) are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.2.2. TA122.z00 Verifying the Monotonic Decrease from V₄ to V₂

This test verifies the monotonic decrease of V from V₄ to less than V₂.

Test Code

TA122.z00

Reference

This test refers to requirement 3.3.2.1.

Test Positions

Use Table 8-9 for the test positions during verification that the monotonic decrease of V is from V₄ to less than V₂:

Value for z	Value for r	Value for f
0	0	0
1	0	0
2	0	0
3	0	0
4	0	0

Table 8-9—Test Positions of Test TA122.z00

Procedure

Follow this procedure to verify that the monotonic decrease of V is from V₄ to less than V₂:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC in the first position defined in Table 8-9.
6. Make sure that the CARRIER is switched on and set the PCD under test in TRANSAC A mode
7. Set the Acquisition Device to capture 50 ms of the PCD signal starting just before the first WUPA command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

Figure 8-11 shows a typical waveform envelope display:

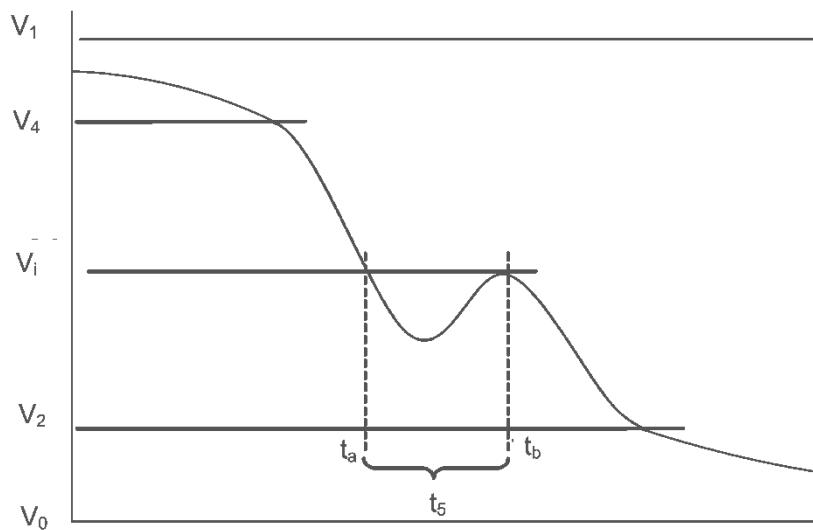


Figure 8-11—Non Monotonic Decrease

10. Measure, using a cursor or its equivalent, the upper level amplitude V_1 preceding the first falling edge of the PCD command.
11. Calculate V_4 as equal to $0.9 \times V_1$ and place a Y-cursor (or its equivalent) to determine the corresponding level.
12. Calculate V_2 as equal to $0.05 \times V_1$ and place a Y-cursor (or its equivalent) to determine the corresponding level.
13. Determine when the PCD carrier envelope decreases through V_4 on the first falling edge.
14. Determine when the PCD carrier envelope decreases through V_2 on the first falling edge.
15. Observe V decreasing from V_4 to less than V_2 on the first falling edge on the PCD carrier envelope. If the carrier envelope decreases continuously between V_4 and V_2 , go to step 17. Otherwise go to step 16.
16. Measure (using cursors or their equivalents) the time elapsed between a local maximum value and the previous time that this value was reached. This elapsed time shall be identified as t_5 . This shall only apply if the local maximum is greater than V_2 . See Figure 8-11 for details.
17. Repeat steps 10 to 16 for all PCD commands.
18. Repeat steps 8 to 17 for all positions defined in Table 8-9

Acceptance Criteria

If V does not decrease monotonically, the time t_5 between a local maximum and the time of passing the same value before the local maximum shall conform to appropriate values shown in Table A.2 in Appendix A.

When multiple t_5 times happen within one signal decrease period, each individual t_5 time shall conform to appropriate values shown in Table A.2 in Appendix A.

Expected Results

Results for each position including the minimum, maximum and average of all measurements performed (i.e. the sum of all results at the concerned position divided by the number of results) are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.2.3. TA123.z00 Verifying the Ringing

This test verifies the ringing following the falling edge, where the falling edge is the part of the envelope V, where V decreases from V_4 to V_2 .

Test Code

TA123.z00

Reference

This test refers to requirement 3.3.2.1.

Test Positions

Use Table 8-10 for the test positions during verification of the ringing following the falling edge:

Value for z	Value for r	Value for f
0	0	0
1	0	0
2	0	0
3	0	0
4	0	0

Table 8-10—Test Positions of Test TA123.z00

Procedure

Follow this procedure to verify the ringing following the falling edge:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC in the first position defined in Table 8-10.
6. Make sure that the CARRIER is switched on and set the PCD under test in TRANSAC_A mode.
7. Set the Acquisition Device to capture 50 ms of the PCD signal starting just before the first WUPA command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

Figure 8-12 shows the acquired signal:

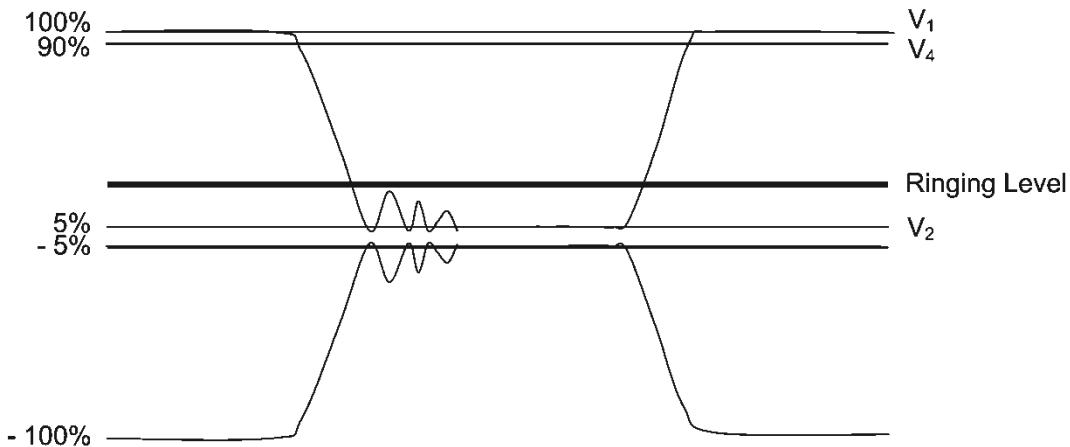


Figure 8-12—Acquired Signal

10. Measure, using a cursor or its equivalent, the upper level amplitude V_1 preceding the first falling edge of the PCD command.
11. Calculate V_2 as equal to $0.05 \times V_1$ and place a Y-cursor (or its equivalent) to determine the corresponding level.
12. If there is no signal peak over the level V_2 , occurring after the carrier envelope has initially reached this level, then go to step 13. Otherwise, the maximum amplitude due to ringing of any peaks above level V_2 and occurring after the carrier envelope has initially reached this level shall be measured (using cursors or their equivalents).
13. Repeat steps 10 to 12 for all PCD commands.
14. Repeat steps 8 to 13 for all positions defined in Table 8-10.

Acceptance Criteria

When no ringing is observed, the result shall be “Pass”. When ringing is observed, the signal amplitude following the falling edge shall remain below $V_{OU,A} \times V_1$. The falling edge is that part of the envelope V where V decreases from V_4 to V_2 . See Table A.2 in Appendix A for the appropriate values of $V_{OU,A}$.

Expected Results

Results for each position including the minimum, maximum and average of all measurements performed (i.e. the sum of all results at the concerned position divided by the number of results) are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.2.4. TA124.z00 Verifying the t_2 Timing

This test verifies lower level timing during a Type A modulation.

Test Code

TA124.z00

Reference

This test refers to requirement 3.3.2.1.

Test Positions

Use Table 8-11 for the test positions during verification of the t_2 timing:

Value for z	Value for r	Value for f
0	0	0
1	0	0
2	0	0
3	0	0
4	0	0

Table 8-11—Test Positions of Test TA124.z00

Procedure

Follow this procedure to verify the t_2 timing:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at the first position defined in Table 8-11.
6. Make sure that the CARRIER is switched on and set the PCD under test in TRANSAC_A mode.
7. Set the Acquisition Device to capture 50 ms of the PCD signal starting just before the first WUPA command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.
10. Measure, using a cursor or its equivalent, the upper level amplitude V_1 preceding the first falling edge of the PCD command.

11. Calculate V_2 as equal to $0.05 \times V_1$ and place a Y-cursor (or its equivalent) to identify the corresponding level.
12. Place an X-cursor (or its equivalent) to identify the time where the PCD carrier envelope crosses V_2 for the last time preceding the first rising edge.
13. Place an X-cursor (or its equivalent) to identify the time where the PCD carrier envelope crosses V_2 for the first time as the carrier envelope increases.
14. Determine the timing t_2 when V decreases through V_2 to when V increases through V_2 as the difference between the times identified by the two X-cursors.
15. Repeat steps 10 to 14 for all PCD commands.
16. Repeat steps 8 to 15 for all points defined in Table 8-11.

Acceptance Criteria

V shall remain less than V_2 for a time t_2 . The time interval t_2 shall conform to appropriate values shown in Table A.2 in Appendix A.

Expected Results

Results for each position including the minimum, maximum and average of all measurements performed (i.e. the sum of all results at the concerned position divided by the number of results) are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.2.5. TA125.z00 Verifying the t_3 and t_4 Timings

This test verifies the increase of V from V_2 to V_4 within a given time t_3 and from V_2 to V_3 within a given time t_4 .

Test Code

TA125.z00

Reference

This test refers to requirement 3.3.2.1.

Test Positions

Use Table 8-12 for the test positions during verification of the increase of V from V_2 to V_3 within a given time t_4 :

Value for z	Value for r	Value for f
0	0	0
1	0	0
2	0	0
3	0	0
4	0	0

Table 8-12—Test Positions of Test TA125.z00

Procedure

Follow this procedure to verify the increase of V from V_2 to V_4 within a given time t_3 and the increase of V from V_2 to V_3 within a given time t_4 :

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at the first position defined in Table 8-12.
6. Make sure that the CARRIER is switched on and set the PCD under test in TRANSAC_A mode.
7. Set the Acquisition Device to capture 50 ms of the PCD signal starting just before the first WUPA command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

10. Measure, using a cursor or its equivalent, the upper level amplitude V_1 preceding the first falling edge of the PCD command.
11. Calculate V_2 as equal to $0.05 \times V_1$ and place a Y-cursor Y1 at the corresponding level.
12. Calculate V_3 as equal to $0.6 \times V_1$ and place a Y-cursor Y2 at the corresponding level.
13. Calculate V_4 as equal to $0.9 \times V_1$ and place a Y-cursor Y3 at the corresponding level.
14. Place an X-cursor X1 (or its equivalent) to identify the time where the PCD carrier envelope increases through V_2 .
15. Place an X-cursor X2 (or its equivalent) to identify the time where the PCD carrier envelope increases through V_3 .
16. Place an X-cursor X3 (or its equivalent) to identify the time where the PCD carrier envelope increases through V_4 .
17. Determine the timing t_4 as the difference between the times identified by the X1 and X2 cursors.
18. Determine the timing t_3 as the difference between the times identified by the X1 and X3 cursors.
19. Repeat steps 10 to 18 for all PCD commands.
20. Repeat steps 8 to 19 for all points defined in Table 8-12.

Acceptance Criteria

V shall increase from V_2 to V_4 within a given time t_3 . V shall increase from V_2 to V_3 within a given time t_4 . The time intervals t_3 and t_4 shall conform to appropriate values shown in Table A.2 in Appendix A.

Expected Results

Results for each position including the minimum, maximum and average of all measurements performed (i.e. the sum of all results at the concerned position divided by the number of results) are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.2.6. TA127.z00 Verifying the Monotonic Increase from V₂ to V₄

This test verifies the monotonic increase of V from V₂ to V₄.

Test Code

TA127.z00

Reference

This test refers to requirement 3.3.2.1.

Test Positions

Use Table 8-13 for the test positions during verification of the monotonic increase of V from V₂ to V₄:

Value for z	Value for r	Value for f
0	0	0
1	0	0
2	0	0
3	0	0
4	0	0

Table 8-13—Test Positions of Test TA127.z00

Procedure

Follow this procedure to verify the monotonic increase of V from V₂ to V₄:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at the first position defined in Table 8-13.
6. Make sure that the CARRIER is switched on and set the PCD under test in TRANSAC_A mode.
7. Set the Acquisition Device to capture 50 ms of the PCD signal starting just before the first WUPA command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

10. Measure, using a cursor or its equivalent, the upper level amplitude V_1 preceding the first falling edge of the PCD command.
11. Calculate V_2 as equal to $0.05 \times V_1$ and place a Y-cursor Y1 at the corresponding level.
12. Calculate V_4 as equal to $0.9 \times V_1$ and place a Y-cursor Y2 at the corresponding level.
13. Identify when the PCD carrier envelope increases through V_2 .
14. Identify when the PCD carrier envelope increases through V_4 .
15. Observe V increasing from V_2 to V_4 on the PCD carrier envelope. If the carrier envelope increases continuously between V_2 and V_4 , the increase is monotonic.
16. Repeat steps 10 to 15 for all PCD commands.
17. Repeat steps 8 to 16 for all points defined in Table 8-13.

Acceptance Criteria

V shall increase monotonically from V_2 to V_4 .

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.2.7. TA128.z00 Verifying the Overshoot

This test verifies the overshoot immediately following the rising edge, which is that part of the envelope V, where V increases from V_2 to V_4 .

Test Code

TA128.z00

Reference

This test refers to requirement 3.3.2.1.

Test Positions

Use Table 8-14 for the test positions during verification of the overshoot immediately following the rising edge:

Value for z	Value for r	Value for f
0	0	0
1	0	0
2	0	0
3	0	0
4	0	0

Table 8-14—Test Positions of Test TA128.z00

Procedure

Follow this procedure to verify the overshoot immediately following the rising edge:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at the first position defined in Table 8-14.
6. Make sure that the CARRIER is switched on and set the PCD under test in TRANSAC_A mode.
7. Set the Acquisition Device to capture 50 ms of the PCD signal starting just before the first WUPA command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

10. Measure, using a cursor or its equivalent, the upper level amplitude V_1 preceding the first falling edge of the PCD command.
11. Calculate V_4 as equal to $0.9 \times V_1$ and place a Y-cursor (or its equivalent) to identify the corresponding level.
12. Observe V after that the envelope has increased through V_4 .
13. Identify and measure (using cursors or their equivalent) the maximum and the minimum peak following the rising edge from V_2 to V_4 .
14. Repeat steps 10 to 13 for all PCD commands.
15. Repeat steps 8 to 14 for all points defined in Table 8-14.

Acceptance Criteria

Overshoots immediately following the rising edge shall remain within $(1 \pm V_{OU,A}) \times V_1$. See Table A.2 in Appendix A for the value of $V_{OU,A}$.

Expected Results

Results for each position including the minimum, maximum and average of all measurements performed (i.e. the sum of all results at the concerned position divided by the number of results)are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.3. PICC to PCD Signal Interface for Type A Communications

This section presents the verifications applicable for Type A communications.

Note: The tests in this section should have their timings adjusted for the actual carrier frequency of the PCD under test.

8.8.3.1. TA131.zrf Verifying the Load Modulation VS1,pp at Minimum Positive Modulation

This test verifies if a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is α cm in height in the positioning tool.

Test Code

TA131.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 8-15 for the test positions during verification that a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is α cm in height in the positioning tool.

Value for z	Value for r	Value for f
0	0	0
0	1	0
0	1	3
0	1	6
0	1	9
1	0	0
2	0	0
2	2	0
2	2	3
2	2	6
2	2	9

Table 8-15—Test Positions of Test TA131.zrf

Procedure

Follow this procedure to verify that a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is α cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a minimum positive load modulation $vs_{1,pp}$. See Chapter 8, section 8.3.1 for details and Table B.1 in Appendix B for the value of $vs_{1,pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 8-15.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 8-15.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC applies minimum positive load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.3.2. TA132.zrf Verifying the Load Modulation $V_{S2,pp}$ at Minimum Positive Modulation

This test verifies whether a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool.

Test Code

TA132.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 8-16 for the verification that a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool:

Value for z	Value for r	Value for f
3	0	0
3	2	0
3	2	3
3	2	6
3	2	9
4	0	0
4	1	0
4	1	3
4	1	6
4	1	9

Table 8-16—Test Positions of Test TA132.zrf

Procedure

Follow this procedure to verify that a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a minimum positive load modulation $V_{S2,pp}$. See Chapter 8, section 8.3.1 for details and Table B.1 in Appendix B for the value of $V_{S2,pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 8-16.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 8-16.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position z which is ≥ 3 cm in height in the positioning tool, applies minimum positive load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.3.3. TA133.zrf Verifying the Load Modulation $V_{S1,pp}$ at Maximum Positive Modulation

This test verifies if a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is 2 cm in height in the positioning tool.

Test Code

TA133.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 8-17 for the test positions during verification that a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is 2 cm in height in the positioning tool:

Value for z	Value for r	Value for f
0	0	0
0	1	0
0	1	3
0	1	6
0	1	9
1	0	0
2	0	0
2	2	0
2	2	3
2	2	6
2	2	9

Table 8-17—Test Positions of Test TA133.zrf

Procedure

Follow this procedure to verify that a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is 2 cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a maximum positive load modulation $V_{S1,pp}$. See Chapter 8, section 8.3.1 for details and Table B.1 in Appendix B for the value of $V_{S1,pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 8-17.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with the each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 8-17.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position z which is $d2$ cm in height in the positioning tool, applies maximum positive load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.3.4. TA134.zrf Verifying the Load Modulation $V_{S2,pp}$ at Maximum Positive Modulation

This test verifies if a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool.

Test Code

TA134.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 8-18 for the test positions during verification of proper operation of a PCD when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool:

Value for z	Value for r	Value for f
3	0	0
3	2	0
3	2	3
3	2	6
3	2	9
4	0	0
4	1	0
4	1	3
4	1	6
4	1	9

Table 8-18—Test Positions of Test TA134.zrf

Procedure

Follow this procedure to verify proper operation of a PCD when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a maximum positive load modulation $V_{S2,pp}$. See Chapter 8, section 8.3.1 for details and Table B.1 in Appendix B for the value of $V_{S2,pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 8-18.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with the each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 8-18.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position z which is ≥ 3 cm in height in the positioning tool, applies maximum positive load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.3.5. TA135.zrf Verifying the Load Modulation $V_{S1,pp}$ at Minimum Negative Modulation

This test verifies if a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≤ 2 cm in height in the positioning tool.

Test Code

TA135.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 8-19 for the test positions during verification that a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≤ 2 cm in height in the positioning tool.

Value for z	Value for r	Value for f
0	0	0
0	1	0
0	1	3
0	1	6
0	1	9
1	0	0
2	0	0
2	2	0
2	2	3
2	2	6
2	2	9

Table 8-19—Test Positions of Test TA135.zrf

Procedure

Follow this procedure to verify a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≤ 2 cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a minimum negative load modulation $V_{S1,pp}$. See Chapter 8, section 8.3.2 for details and Table B.1 in Appendix B for the value of $V_{S1,pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 8-19.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 8-19.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position z which is ≤ 2 cm in height in the positioning tool, applies minimum negative load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.3.6. TA136.zrf Verifying the Load Modulation $V_{S2,pp}$ at Minimum Negative Modulation

This test verifies if a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool.

Test Code

TA136.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 8-20 for test positions during the verification that a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool.

Value for z	Value for r	Value for f
3	0	0
3	2	0
3	2	3
3	2	6
3	2	9
4	0	0
4	1	0
4	1	3
4	1	6
4	1	9

Table 8-20—Test Positions of Test TA136.zrf

Procedure

Follow this procedure to verify a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a minimum negative load modulation $V_{S2,pp}$. See Chapter 8, section 8.3.2 for details and Table B.1 in Appendix B for the value of $V_{S2,pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 8-20.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 8-20.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position z which is ≥ 3 cm in height in the positioning tool, applies minimum negative load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.3.7. TA137.zrf Verifying the Load Modulation $V_{S1,pp}$ at Maximum Negative Modulation

This test verifies if a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≤ 2 cm in height in the positioning tool.

Test Code

TA137.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 8-21 for the test positions during verification that a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≤ 2 cm in height in the positioning tool.

Value for z	Value for r	Value for f
0	0	0
0	1	0
0	1	3
0	1	6
0	1	9
1	0	0
2	0	0
2	2	0
2	2	3
2	2	6
2	2	9

Table 8-21—Test Positions of Test TA137.zrf

Procedure

Follow this procedure to verify a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≤ 2 cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a maximum negative load modulation $V_{S1,pp}$. See Chapter 8, section 8.3.2 for details and Table B.1 in Appendix B for the value of $V_{S1,pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 8-21.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 8-21.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position z which is ≤ 2 cm in height in the positioning tool, applies maximum negative load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.3.8. TA138.zrf Verifying the Load Modulation $V_{S2,pp}$ at Maximum Negative Modulation

This test verifies if a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool.

Test Code

TA138.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 8-22 for test positions during the verification that a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool.

Value for z	Value for r	Value for f
3	0	0
3	2	0
3	2	3
3	2	6
3	2	9
4	0	0
4	1	0
4	1	3
4	1	6
4	1	9

Table 8-22—Test Positions of Test TA138.zrf

Procedure

Follow this procedure to verify a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a maximum negative load modulation $V_{S2,pp}$. See Chapter 8, section 8.3.2 for details and Table B.1 in Appendix B for the value of $V_{S2,pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 8-22.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 8-22.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position z which is ≥ 3 cm in height in the positioning tool, applies maximum negative load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.3.9. TA139.000 Verifying the FDT_{A,PICC} tolerance

This test verifies if a PCD functions correctly when type A PICC responses occur at minimum and maximum values of the acceptable FDT_{A,PICC} time window.

Test Code

TA139.000

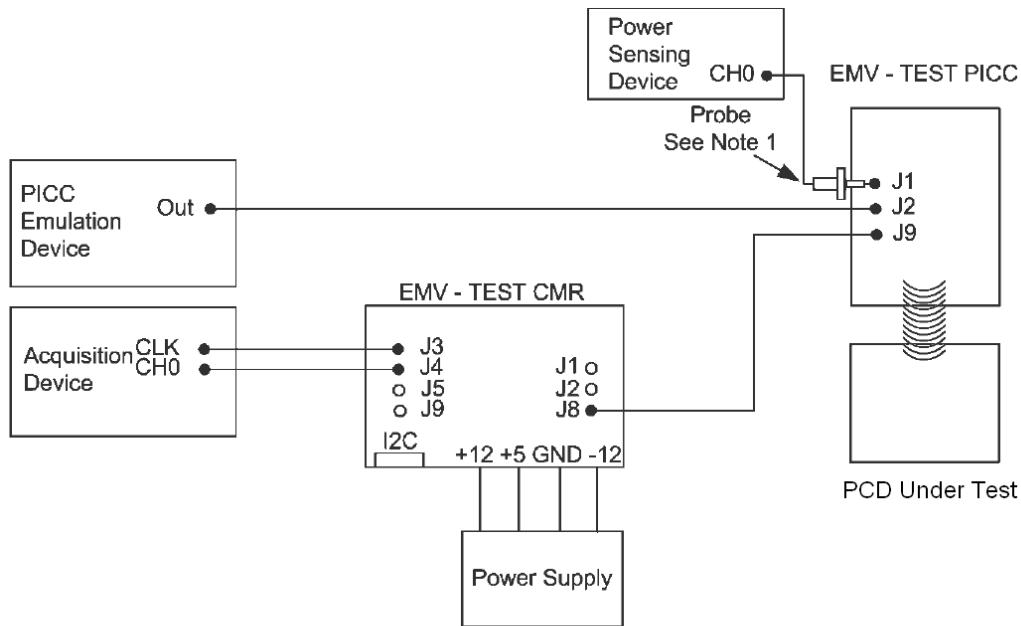
Reference

This test refers to requirement 4.8.1.1.

Procedure

Follow this procedure to verify that a PCD functions correctly when type A PICC responses occur at minimum and maximum values of the acceptable FDT_{A,PICC} time window.

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
3. Set up the EMV – TEST PICC to generate a nominal positive load modulation V_{S1,pp}. See Chapter 8, section 8.3.1 for details and Table B.1 in Appendix B for the value of V_{S1,pp}.
4. Refer to Figure 8-13 to set-up the PICC Emulation Device FDT_{A,PICC}:



Note 1: Probe can be passive or active, $>1M\Omega$, <15 pF.

Figure 8-13 F % O R F N ' L D J U D P I R U_{A,PICC} Set-up H 3 , & &

5. Set the EMV – TEST CMR with the control software as shown in Table 8-23

Function	Setting
Input	J8 (LETI)
Clock	CLK IN
Amplifier	Buffer

Table 8-23—CMR Parameter Settings

6. Place the EMV – TEST PICC at position ($z=0$, $r=0$, $\varphi=0$).
7. Display the TTA L1 - Analogue menu using the DTE.
8. Set the DTE in WUPA mode.
9. Set the Acquisition Device to capture 10 ms of signal at the start of the WUPA command.
10. Set the PICC Emulation Device to generate $FDT_{A,PICC,MIN}$ as required in Table C-2, without any correction.
11. Optimize the Acquisition Device settings for accurate measurement of type A waveform level and timing.
12. Send a correct ATQA answer.
13. Measure the $FDT_{A,PICC}$ between the start of the WUPA last rising edge and the start of the PICC load modulation. Figure 8-14 shows the correct start cursor position, and Figure 8-15 shows the correct end cursor position.

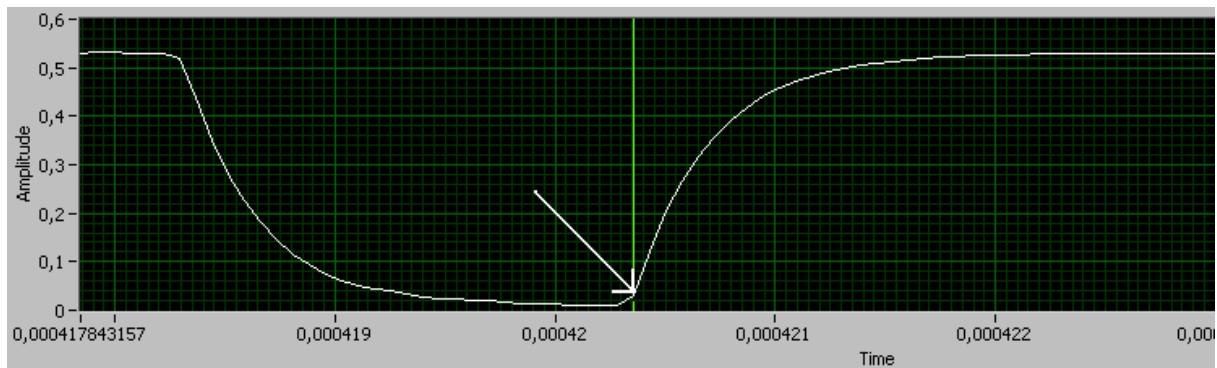


Figure 8-14 F 6 W D U W & X U V_{A,PICC} Measurement L W L R Q I R r

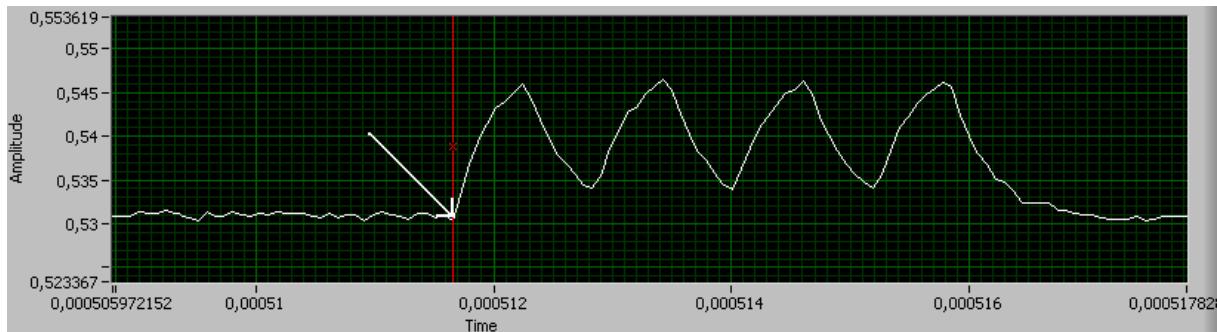


Figure 8-15 F (Q G & X U V R U_{A,PICO} 3MBasement L R Q I R U

14. If the measured $FDT_{A,PICC}$ is not the one required for the test, set the PICC Emulation Device to generate the required one.

Note: The setup of the $FDT_{A,PICC,MIN}$ performed on the ATQA is enough to ensure that the next $FDT_{A,PICC}$ values (UID, SAK for $FDT_{A,PICC,MIN}$ and ATS Response to Select PPSE Command, etc. for $FDT_{A,PICC,NOM}$) should be correct if the $FDT_{A,PICC,MIN}$ performed on the ATQA is correctly set up. There is no need to adjust the other $FDT_{A,PICC}$ values in the frame trail.

15. Repeat steps 12 to 14 until the required value for $FDT_{A,PICC}$ is reached.
16. Display the TTA L1 - Digital menu using the DTE.
17. Set the DTE in LOOPBACK mode.
18. Make the EMV – TEST PICC return the responses described in Table C.1 of Appendix C, Frame Trail for PCD Type A tests using an $FDT_{A,PICC}$ without any additional delay on all PICC responses.
19. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
20. Repeat steps 18 and 19 using an $FDT_{A,PICC}$ with an additional delay of 400 ns on all PICC responses.

Note: You shall set the PICC Emulation Device to generate $FDT_{A,PICC,MIN}$ as required in Table C-2 without any correction on the first iteration, then with a 400 ns delay (Step 19)

Acceptance Criteria

The PCD shall function correctly when type A PICC responses occur at minimum and maximum values of the acceptable $FDT_{A,PICC}$ time window. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.4. Bit Level Coding Signal Interface for Type A Communications

This section presents the verifications applicable for Type A communications.

8.8.4.1. TA141.200 Verifying the PCD Transmitted Bit Rate

This test verifies the PCD to PICC bit rate during initialization.

Test Code

TA141.200

Reference

This test refers to requirement 4.2.1.1.

Procedure

Follow this procedure to verify the PCD to PICC bit rate during initialization:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at position ($z=2$, $r=0$, $\phi=0$).
6. Make sure that the CARRIER is switched on and set the PCD under test in WUPA mode.
7. Set the Acquisition Device to trigger to capture one WUPA command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

Figure 8-16 shows the bit rate for the WUPA command:

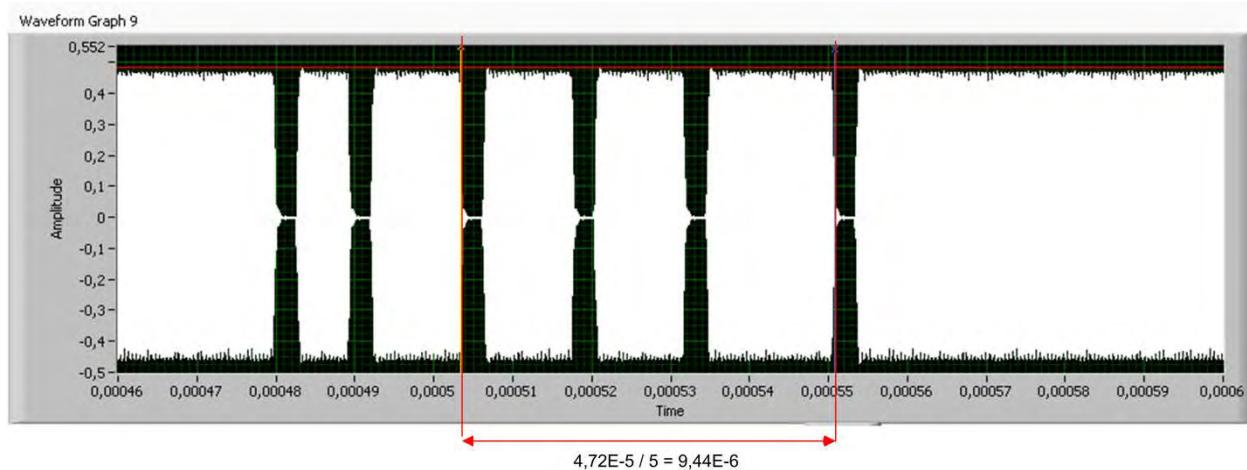


Figure 8-16—Bit Rate for the WUPA Command

10. Place an X-cursor (or its equivalent) to identify the time when the PCD carrier envelope is at the start of the third pause within the WUPA command.
11. Place an X-cursor (or its equivalent) to identify the time when the PCD carrier envelope is at the identical point at the start of the sixth pause within the WUPA command.
12. Calculate the bit rate as $5 / (\text{the difference between the times identified by the two X-cursors})$.

Acceptance Criteria

The bit rate shall be between $f_C / 128 \pm 0.5\%$.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.4.2. TA142.200 Verifying the Bit Coding and De-synchronization PCD to PICC

This test verifies the PCD coding.

Test Code

TA142.200

Reference

This test refers to requirements 4.4.1.1 and 4.6.1.1.

Procedure

Follow this procedure to verify the PCD coding:

1. Confirm that the content of WUPA coded by the PUT is the value '52' using EMV L1 digital tests.
2. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
3. Display the TTA L1 - Analogue menu using the DTE.
4. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
5. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
6. Place the EMV – TEST PICC at position ($z=2$, $r=0$, $\phi=0$).
7. Make sure that the CARRIER is switched on and set the PCD under test in WUPA mode.
8. Set the Acquisition Device to trigger to capture one WUPA command sent by the PCD.
9. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
10. Launch the acquisition.
11. Place an X-cursor or its equivalent to identify the time when the PCD carrier envelope is at the start of the first pause within the WUPA. This cursor shall be referenced as X1.
12. Place an X-cursor or its equivalent to identify the time when the PCD carrier envelope is at the start of the second pause within the WUPA. This cursor shall be referenced as X2. The time between X1 and X2 is defined as the bit duration.
13. Identify the symbol between X1 and X2 using the following rules:
 - a) if a low level occurs after a time of half a bit duration, identify the symbol as X.
 - b) if no modulation occurs for a full bit duration, identify the symbol as Y.
 - c) if a low level occurs at the beginning of the bit duration, identify the symbol as Z.
 - d) if none of the previous cases has been identified, identify the symbol as an invalid symbol.

14. Complete Table 8-24 for the symbol you have identified.
15. Move the cursors X1 and X2 by the bit duration identified in step 12 to identify the Symbol over the next bit duration.
16. Repeat step 13 to 15 for all the other symbols in the sequence.
17. Compare the identified symbols with the expected ones. The sequence of expected symbols corresponds to a WUPA (0x52 Modified Miller coded with ASK 100% modulation).

Identified Symbol	Expected Symbol	WUPA Bit Coding Correspondence
	Z	Start of Frame
	Z	0
	X	1
	Y	0
	Z	0
	X	1
	Y	0
	X	1
	Y	End of Frame

Table 8-24—Symbols Identified

Acceptance Criteria

The PCD shall code a WUPA according to the sequence of expected symbols given in Table 8-24.

The symbols used shall be as follows:

- x Symbol X: after a time of half the bit duration, a lower level occurs.
- x Symbol Y: for the full bit duration, no modulation occurs.
- x Symbol Z: at the beginning of the bit duration, a lower level occurs.

Figure 8-17 shows the WUPA bit coding:

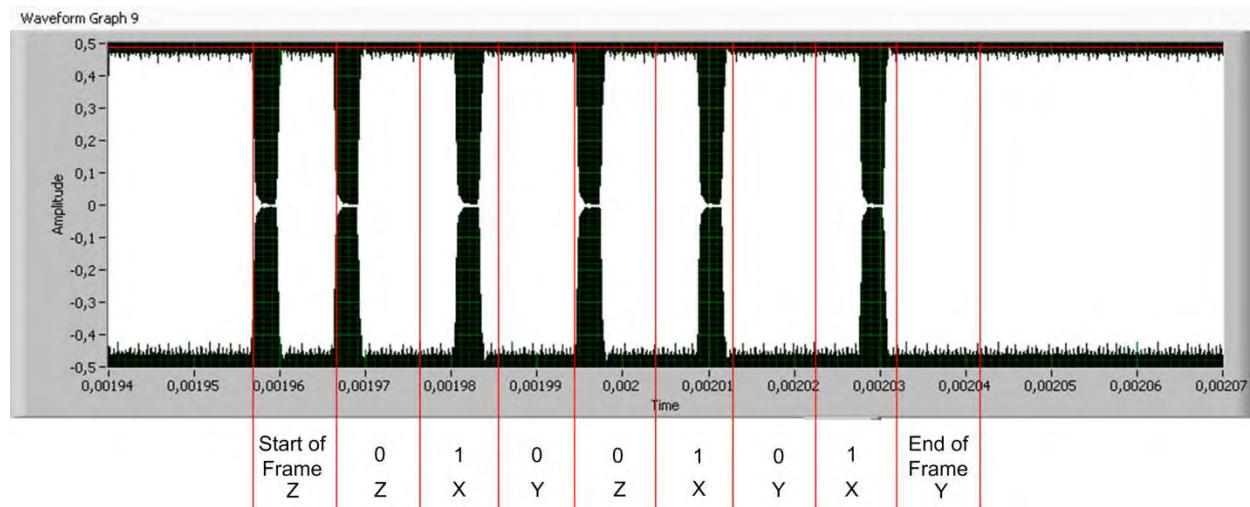


Figure 8-17—WUPA Bit Coding

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.4.3. TA143.200 Verifying the Bit Coding and De-synchronization PICC to PCD

This test verifies the PCD behavior when receiving a correct PICC answer.

Test Code

TA143.200

Reference

This test refers to requirements 4.4.2.2 and 4.6.1.3.

Procedure

Follow this procedure to verify the PCD behavior when receiving a correct PICC answer:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a nominal positive load modulation $V_{S1,pp}$. See Chapter 8, section 8.3.1 for details and Table B.1 in Appendix B for the value of $V_{S1,pp}$.
5. Place the EMV – TEST PICC at position ($z=2$, $r=0$, $\phi=0$).
6. Make sure that the CARRIER is switched on and set the PCD under test in RATS mode.
7. Detect when the PCD sends a WUPA command.
8. Send a correct PICC ATQA answer with the content and timing as defined in Appendix C.
9. Observe if the PCD responds with the next command and confirm that the next command (AC CL1) is a valid command.

Acceptance Criteria

The PCD shall continue with the next command when receiving a correct PICC answer. This next command shall be a valid Type A command.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.5. PCD to PICC Signal Interface for Type B Communications

This section presents the verifications applicable for Type B communications.

Figure 8-18 shows a typical PCD to PICC Type B modulation waveform. This waveform appears when the EMV – TEST PICC is positioned in the Operating Volume of the PCD.

Figure 8-18—Typical PCD to PICC Type B Modulation Waveform

The V (voltage) represents the envelope of the signal measured at the output of the pickup coil of the EMV – TEST PICC. If you are using asynchronous sampling, the envelope (V) is obtained by applying a moving average with a period of $1/f_C$ on the magnitude of the complex Hilbert transform of the signal.

V_1 is the level measured immediately before the falling edge preceding a lower level of modulation from PCD. V_2 is the level measured immediately before the rising edge that follows the lower level.

The V_1 level shall be obtained by applying an average of the signal envelope over a duration of $20/f_C$ preceding the signal decay. The V_2 level shall be obtained by applying an average of the signal envelope over a duration of $20/f_C$ preceding the signal increase.

The modulation index (m_i), V_3 and V_4 are defined as follows:

$$m_i = \frac{V_1 - V_2}{V_1 + V_2}$$

$$V_3 = V_1 - 0.1 \times (V_1 - V_2)$$

$$V_4 = V_2 + 0.1 \times (V_1 - V_2)$$

Note: It is strongly recommended to perform these test cases using the same acquisitions to avoid any random behavior of the PCD under test.

8.8.5.1. TB121.z00 Verifying the Modulation Index

This test verifies the modulation index.

Test Code

TB121.z00

Reference

This test refers to requirement 3.3.4.1.

Test Positions

Use Table 8-25 for the test positions during verification of the modulation index:

Value for z	Value for r	Value for f
0	0	0
1	0	0
2	0	0
3	0	0
4	0	0

Table 8-25—Test Positions of Test TB121.z00

Procedure

Follow this procedure to verify the modulation index:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC in the first position defined in Table 8-25.
6. Make sure that the CARRIER is switched on and set the PCD under test in TRANSAC_B mode.
7. Set the Acquisition Device to capture 50 ms of the PCD signal starting just before the first WUPB command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

10. Measure, using a cursor or its equivalent, the upper level amplitude V_1 preceding each falling edge of the PCD command.

11. Measure, using a cursor or its equivalent, the lower level amplitude V_2 preceding each rising edge.

12. Calculate the modulation index for each V_1 level and the immediately following related V_2 level : $| \frac{V_2 - V_1}{V_2 + V_1} |$

13. Repeat steps 10 to 12 for all PCD commands

14. Repeat steps 8 to 13 for all positions defined in Table 8-25.

Note: Any possible DC offset of the signal shall be compensated before performing the computation of the modulation index.

Acceptance Criteria

The modulation index values m_i of the signal shall be mod_i . Refer to Table A.3 in Appendix A, Signal Interface for Type B for the applicable range of values for mod_i .

Note: When testing PCDs without a perfectly flat landing plane, refer to section 6.2.2. above and adjust the maximum acceptance criteria according to the actual z distance used during testing. The distance is taken from the center of the EMV – Test PICC.

Expected Results

Results for each position including the minimum, maximum and average of all measurements performed (i.e. the sum of all results at the concerned position divided by the number of results) are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.5.2. TB122.z00 Verifying the Fall Time

This test verifies the fall time.

Test Code

TB122.z00

Reference

This test refers to requirement 3.3.4.1.

Test Positions

Use Table 8-26 for the test positions during verification of the fall time for Type B communications:

Value for z	Value for r	Value for f
0	0	0
1	0	0
2	0	0
3	0	0
4	0	0

Table 8-26—Test Positions of Test TB122.z00

Procedure

Follow this procedure to verify the fall time:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC in the first position defined in Table 8-27.
6. Make sure that the CARRIER is switched on and set the PCD under test in TRANSAC_B mode.
7. Set the Acquisition Device to capture 50 ms of the PCD signal starting just before the first WUPB command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

10. Measure, using a cursor or its equivalent, the upper level amplitude V_1 preceding the first falling edge of the PCD command.
11. Measure, using a cursor or its equivalent, the lower level amplitude V_2 preceding the first rising edge of the PCD command..
12. Calculate $V_3 = V_1 - 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) Y1 to identify the corresponding level.
13. Calculate $V_4 = V_2 + 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) Y2 to identify the corresponding level.
14. Place an X-cursor (or its equivalent) X1 at the timing corresponding to the first time that the voltage V crosses the Y1 cursor level.
15. Place an X-cursor (or its equivalent) X2 at the timing corresponding to the first time that the voltage V crosses the Y2 cursor level.
16. Determine the fall time t_f as the difference between the timing indicated by X2 and the timing indicated by X1.
17. Repeat steps 10 to 16 for all PCD commands.
18. Repeat steps 8 to 17 for all positions defined in Table 8-26.

Acceptance Criteria

V shall decrease from V_3 to V_4 within a given time t_f . Refer to Table A.3 in Appendix A, Signal Interface for Type B for the applicable range of values for t_f .

Expected Results

Results for each position including the minimum, maximum and average of all measurements performed (i.e. the sum of all results at the concerned position divided by the number of results) are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.5.3. TB123.z00 Verifying the Rise Time

This test verifies the rise time.

Test Code

TB123.z00

Reference

This test refers to requirement 3.3.4.1.

Test Positions

Use Table 8-27 for the test positions during verification of the rise time:

Value for z	Value for r	Value for f
0	0	0
1	0	0
2	0	0
3	0	0
4	0	0

Table 8-27—Test Positions of Test TB123.z00

Procedure

Follow this procedure to verify the rise time:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC in the first position defined in Table 8-27.
6. Make sure that the CARRIER is switched on and set the PCD under test in TRANSAC_B mode.
7. Set the Acquisition Device to capture 50 ms of the PCD signal starting just before the first WUPB command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

10. Measure, using a cursor or its equivalent, the upper level amplitude V_1 preceding the last falling edge of the PCD command.
11. Measure, using a cursor or its equivalent, the lower level amplitude V_2 preceding the last rising edge of the PCD command.
12. Calculate $V_3 = V_1 - 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) Y1 to identify the corresponding level.
13. Calculate $V_4 = V_2 + 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) Y2 to identify the corresponding level.
14. Place an X-cursor (or its equivalent) X1 at the timing corresponding to the last time the voltage V crosses the Y1 cursor level.
15. Place an X-cursor (or its equivalent) X2 at the timing corresponding to the last time the voltage V crosses the Y2 cursor level.
16. Determine the rise time t_r as the difference between the timing indicated by X1 and the timing indicated by X2.
17. Repeat steps 10 to 16 for all PCD commands.
18. Repeat steps 8 to 17 for all positions defined in Table 8-27.

Acceptance Criteria

V shall increase from V_4 to V_3 within a given time t_r . Refer to Table A.3 in Appendix A, Signal Interface for Type B for the applicable range of values for t_r .

Expected Results

Results for each position including the minimum, maximum and average of all measurements performed (i.e. the sum of all results at the concerned position divided by the number of results) are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.5.4. TB124.z00 Verifying the Monotonic Rising Edge

This test verifies that the rising edge is monotonic.

Test Code

TB124.z00

Reference

This test refers to requirement 3.3.4.1.

Test Positions

Use Table 8-28 for the test positions during verification that the rising edge is monotonic:

Value for z	Value for r	Value for f
0	0	0
1	0	0
2	0	0
3	0	0
4	0	0

Table 8-28—Test Positions of Test TB124.z00

Procedure

Follow this procedure to verify that the rising edge is monotonic:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at the first position defined in Table 8-28.
6. Make sure that the CARRIER is switched on and set the PCD under test in TRANSAC_B mode.
7. Set the Acquisition Device to capture 50 ms of the PCD signal starting just before the first WUPB command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

10. Measure, using a cursor or its equivalent, the upper level amplitude V_1 preceding the last falling edge of the PCD command.
11. Measure, using a cursor or its equivalent, the lower level amplitude V_2 preceding the last rising edge of the PCD command.
12. Calculate $V_3 = V_1 - 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) Y_1 to identify the corresponding level.
13. Calculate $V_4 = V_2 + 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) Y_2 to identify the corresponding level.
14. Observe V increasing on the last rising edge from V_4 to V_3 for each PCD command. If the increase is continuous between V_4 and V_3 , the increase is monotonic.
15. Repeat steps 10 to 14 for all PCD commands.
16. Repeat steps 8 to 15 for all points defined in Table 8-28.

Acceptance Criteria

The rising edge of the modulation shall be monotonic.

Note: If you are using asynchronous sampling, verify the monotonic parameter on the envelope (V) obtained by applying a moving average with a period of $1/f_C$ on the magnitude of the complex Hilbert transform of the signal. No deviation is permitted.

If you are using synchronous sampling, the edge could deviate from monotonic:

- x Only strictly below $z=1$
- x For two successive peaks (1 cycle maximum)
- x Less than 8% of $(V_1 - V_2)$ between two peaks

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.5.5. TB125.z00 Verifying the Monotonic Falling Edge

This test verifies that the falling edge is monotonic.

Test Code

TB125.z00

Reference

This test refers to requirement 3.3.4.1.

Test Positions

Use Table 8-29 for the test positions during verification that the falling edge is monotonic:

Value for z	Value for r	Value for f
0	0	0
1	0	0
2	0	0
3	0	0
4	0	0

Table 8-29—Test Positions of Test TB125.z00

Procedure

Follow this procedure to verify that the falling edge is monotonic:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at the first position defined in Table 8-29.
6. Make sure that the CARRIER is switched on and set the PCD under test in TRANSAC_B mode.
7. Set the Acquisition Device to capture 50 ms of the PCD signal starting just before the first WUPB command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

10. Measure, using a cursor or its equivalent, the upper level amplitude V_1 preceding the first falling edge of the PCD command.
11. Measure, using a cursor or its equivalent, the lower level amplitude V_2 preceding the first rising edge of the PCD command.
12. Calculate $V_3 = V_1 - 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) Y1 to identify the corresponding level.
13. Calculate $V_4 = V_2 + 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) Y2 to identify the corresponding level.
14. Observe V decreasing on the first falling edge from V_3 to V_4 for each PCD command. If the decrease is continuous between V_3 to V_4 , the decrease is monotonic.
15. Repeat steps 10 to 14 for all PCD commands.
16. Repeat steps 8 to 15 for all points defined in Table 8-29.

Acceptance Criteria

The falling edge of the modulation shall be monotonic.

Note: If you are using asynchronous sampling, verify the monotonic parameter on the envelope (V) obtained by applying a moving average with a period of $1/f_C$ on the magnitude of the complex Hilbert transform of the signal. No deviation is permitted.

If you are using synchronous sampling, the edge could deviate from monotonic:

- x Only strictly below $z=1$
- x For two successive peaks (1 cycle maximum)
- x Less than 8% of $(V_1 - V_2)$ between two peaks

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.5.6. TB126.z00 Verifying Overshoots

This test verifies the overshoots.

Test Code

TB126.z00

Reference

This test refers to requirement 3.3.4.1.

Test Positions

Use Table 8-30 for the test positions during verification of the overshoots:

Value for z	Value for r	Value for f
0	0	0
1	0	0
2	0	0
3	0	0
4	0	0

Table 8-30—Test Positions of Test TB126.z00

Procedure

Follow this procedure to verify the overshoots:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at the first position defined in Table 8-30.
6. Make sure that the CARRIER is switched on and set the PCD under test in TRANSAC_B mode.
7. Set the Acquisition Device to capture 50 ms of the PCD signal starting just before the first WUPB command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

10. Measure, using a cursor or its equivalent, the upper level amplitude V_1 preceding the first falling edge of the PCD command.
11. Measure, using a cursor or its equivalent, the lower level amplitude V_2 preceding the first rising edge of the PCD command.
12. Calculate $V_3 = V_1 - 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) to identify the corresponding level.
13. Calculate $V_4 = V_2 + 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) to identify the corresponding level.
14. Determine (using a cursor or its equivalent) the maximum peak following the first falling edge from V_3 to V_4 and measure the overshoot.
15. Measure, using a cursor or its equivalent, the upper level amplitude V_1 preceding the last falling edge of the PCD command.
16. Measure, using a cursor or its equivalent, the lower level amplitude V_2 preceding the last rising edge of the PCD command.
17. Calculate $V_3 = V_1 - 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) to identify the corresponding level.
18. Calculate $V_4 = V_2 + 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) to identify the corresponding level.
19. Determine (using a cursor or its equivalent) the maximum peak following the last rising edge from V_4 to V_3 and measure the overshoot.
20. Repeat steps 10 to 19 for all PCD commands.
21. Repeat steps 8 to 20 for all points defined in Table 8-30.

Acceptance Criteria

Overshoots immediately following the rising and falling edge shall be less than $V_{OU,B} \times (V_1 - V_2)$. Refer to Table A.3 in Appendix A, Signal Interface for Type B for the applicable range of values for $V_{OU,B}$.

Expected Results

Results for each position including the minimum, maximum and average of all measurements performed (i.e. the sum of all results at the concerned position divided by the number of results) are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.5.7. TB127.z00 Verifying Undershoots

This test verifies the undershoots.

Test Code

TB127.z00

Reference

This test refers requirement 3.3.4.1.

Test Positions

Use Table 8-31 for the test positions during verification of the undershoots:

Value for z	Value for r	Value for f
0	0	0
1	0	0
2	0	0
3	0	0
4	0	0

Table 8-31—Test Positions of Test TB127.z00

Procedure

Follow this procedure to verify the undershoots:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at the first position defined in Table 8-31.
6. Make sure that the CARRIER is switched on and set the PCD under test in TRANSAC_B mode.
7. Set the Acquisition Device to capture 50 ms of the PCD signal starting just before the first WUPB command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

10. Measure, using a cursor or its equivalent, the upper level amplitude V_1 preceding the first falling edge of the PCD command.
11. Measure, using a cursor or its equivalent, the lower level amplitude V_2 preceding the first rising edge of the PCD command.
12. Calculate $V_3 = V_1 - 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) to identify the corresponding level.
13. Calculate $V_4 = V_2 + 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) to identify the corresponding level.
14. Determine (using a cursor or its equivalent) the minimum peak following the first falling edge from V_3 to V_4 and measure the undershoot.
15. Measure, using a cursor or its equivalent, the upper level amplitude V_1 preceding the last falling edge of the PCD command.
16. Measure, using a cursor or its equivalent, the lower level amplitude V_2 preceding the last rising edge of the PCD command.
17. Calculate $V_3 = V_1 - 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) to identify the corresponding level.
18. Calculate $V_4 = V_2 + 0.1 \times (V_1 - V_2)$ and place a Y-cursor (or its equivalent) to identify the corresponding level.
19. Determine (using a cursor or its equivalent) the minimum peak following the last rising edge from V_4 to V_3 and measure the undershoot.
20. Repeat steps 10 to 19 for all PCD commands.
21. Repeat steps 8 to 20 for all points defined in Table 8-31.

Acceptance Criteria

Undershoots immediately following the falling and rising edge shall be less than $V_{OU,B} \times (V_1 - V_2)$. Refer to Table A.3 in Appendix A, Signal Interface for Type B for the applicable range of values for $V_{OU,B}$.

Expected Results

Results for each position including the minimum, maximum and average of all measurements performed (i.e. the sum of all results at the concerned position divided by the number of results) are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.6. PICC to PCD Signal Interface for Type B Communications

This section presents the verifications applicable for Type B communications.

Note: The tests in this section should have their timings adjusted for the actual carrier frequency of the PCD under test.

8.8.6.1. TB131.zrf Verifying the Load Modulation $V_{S1,pp}$ at Minimum Positive Modulation

This test verifies if a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is α cm in height in the positioning tool.

Test Code

TB131.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 8-32 for the test positions during verification that a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is α cm in height in the positioning tool:

Value for z	Value for r	Value for f
0	0	0
0	1	0
0	1	3
0	1	6
0	1	9
1	0	0
2	0	0
2	2	0
2	2	3
2	2	6
2	2	9

Table 8-32—Test Positions of Test TB131.zrf

Procedure

Follow this procedure to verify that a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is d_2 cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a minimum positive load modulation $V_{S1,pp}$. See Chapter 8, section 8.3.1 for details and Table B.1 in Appendix B for the value of $V_{S1,pp}$.
5. Place the EMV – TEST PICC at the first position defined Table 8-32.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.3 of Appendix C, Frame Trail for PCD Type B tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 8-32.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position z which is d_2 cm in height in the positioning tool, applies minimum positive load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.6.2. TB132.zrf Verifying the Load Modulation $V_{S2,pp}$ at Minimum Positive Modulation

This test verifies if a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool:

Test Code

TB132.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 8-33 for the test positions during verification that a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool.

Value for z	Value for r	Value for f
3	0	0
3	2	0
3	2	3
3	2	6
3	2	9
4	0	0
4	1	0
4	1	3
4	1	6
4	1	9

Table 8-33—Test Positions of Test TB132.zrf

Procedure

Follow this procedure to verify that a PCD functions correctly when minimum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a minimum positive load modulation $V_{S2,pp}$. See Chapter 8, section 8.3.1 for details and Table B.1 in Appendix B for the value of $V_{S2,pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 8-33.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.3 of Appendix C, Frame Trail for PCD Type B tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 8-33.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position z which is ≥ 3 cm in height in the positioning tool, applies minimum positive load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.6.3. TB133.zrf Verifying the Load Modulation $V_{S1,pp}$ at Maximum Positive Modulation

This test verifies if a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is α cm in height in the positioning tool.

Test Code

TB133.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 8-34 for the test positions during verification that a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is α cm in height in the positioning tool.

Value for z	Value for r	Value for f
0	0	0
0	1	0
0	1	3
0	1	6
0	1	9
1	0	0
2	0	0
2	2	0
2	2	3
2	2	6
2	2	9

Table 8-34—Test Positions of Test TB133.zrf

Procedure

Follow this procedure to verify that a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is α cm in height in the positioning tool.

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a maximum positive load modulation $V_{S1,pp}$. See Chapter 8, section 8.3.1 for details and Table B.1 in Appendix B for the value of $V_{S1,pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 8-34.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.3 of Appendix C, Frame Trail for PCD Type B tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 8-34.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position z which is $d2$ cm in height in the positioning tool, applies maximum positive load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.6.4. TB134.zrf Verifying the Load Modulation $V_{S2,pp}$ at Maximum Positive Modulation

This test verifies if a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool.

Test Code

TB134.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 8-35 for the test positions during verification that a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool:

Value for z	Value for r	Value for f
3	0	0
3	2	0
3	2	3
3	2	6
3	2	9
4	0	0
4	1	0
4	1	3
4	1	6
4	1	9

Table 8-35—Test Positions of Test TB134.zrf

Procedure

Follow this procedure to verify that a PCD functions correctly when maximum positive load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a maximum positive load modulation $V_{S2,pp}$. See Chapter 8, section 8.3.1 for details and Table B.1 in Appendix B for the value of $V_{S2,pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 8-35.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.3 of Appendix C, Frame Trail for PCD Type B tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 8-35.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position z which is ≥ 3 cm in height in the positioning tool, applies maximum positive load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.6.5. TB135.zrf Verifying the Load Modulation $V_{S1,pp}$ at Minimum Negative Modulation

This test verifies if a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≤ 2 cm in height in the positioning tool.

Test Code

TB135.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 8-36 for the test positions during verification that a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≤ 2 cm in height in the positioning tool.

Value for z	Value for r	Value for f
0	0	0
0	1	0
0	1	3
0	1	6
0	1	9
1	0	0
2	0	0
2	2	0
2	2	3
2	2	6
2	2	9

Table 8-36 F 7 H V W 3 R V L W L R Q V R I 7 H V W

Procedure

Follow this procedure to verify a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≤ 2 cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a minimum negative load modulation $V_{S1,pp}$. See Chapter 8, section 8.3.2 for details and Table B.1 in Appendix B for the value of $V_{S1,pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 8-36.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.3 of Appendix C, Frame Trail for PCD Type B tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 8-36.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position z which is ≤ 2 cm in height in the positioning tool, applies minimum negative load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.6.6. TB136.zrf Verifying the Load Modulation $V_{S2,pp}$ at Minimum Negative Modulation

This test verifies if a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool.

Test Code

TB136.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 8-37 for the test positions during verification that a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool.

Value for z	Value for r	Value for f
3	0	0
3	2	0
3	2	3
3	2	6
3	2	9
4	0	0
4	1	0
4	1	3
4	1	6
4	1	9

Table 8-37—Test Positions of Test TB136.zrf

Procedure

Follow this procedure to verify a PCD functions correctly when minimum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).

4. Set up the EMV – TEST PICC to generate a minimum negative load modulation $V_{S2,pp}$. See Chapter 8, section 8.3.2 for details and Table B.1 in Appendix B for the value of $V_{S2,pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 8-37.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.3 of Appendix C, Frame Trail for PCD Type B tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 8-37.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position z which is ≥ 3 cm in height in the positioning tool, applies minimum negative load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.6.7. TB137.zrf Verifying the Load Modulation $V_{S1,pp}$ at Maximum Negative Modulation

This test verifies if a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≤ 2 cm in height in the positioning tool.

Test Code

TB137.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 8-38 for the test positions during verification that a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≤ 2 cm in height in the positioning tool.

Value for z	Value for r	Value for f
0	0	0
0	1	0
0	1	3
0	1	6
0	1	9
1	0	0
2	0	0
2	2	0
2	2	3
2	2	6
2	2	9

Table 8-38—Test Positions of Test TB137.zrf

Procedure

Follow this procedure to verify a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≤ 2 cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a maximum negative load modulation $V_{S1,pp}$. See Chapter 8, section 8.3.2 for details and Table B.1 in Appendix B for the value of $V_{S1,pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 8-38.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.3 of Appendix C, Frame Trail for PCD Type B tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 8-38.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position z which is ≤ 2 cm in height in the positioning tool, applies maximum negative load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.6.8. TB138.zrf Verifying the Load Modulation $V_{S2,pp}$ at Maximum Negative Modulation

This test verifies if a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool.

Test Code

TB138.zrf

Reference

This test refers to requirement 3.4.5.1.

Test Positions

Use Table 8-39 for the test positions during verification that a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool.

Value for z	Value for r	Value for f
3	0	0
3	2	0
3	2	3
3	2	6
3	2	9
4	0	0
4	1	0
4	1	3
4	1	6
4	1	9

Table 8-39—Test Positions of Test TB138.zrf

Procedure

Follow this procedure to verify a PCD functions correctly when maximum negative load modulation characteristics are applied using the EMV – TEST PICC placed in a position z which is ≥ 3 cm in height in the positioning tool:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Digital menu using the DTE.

3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a maximum negative load modulation $V_{S2,pp}$. See Chapter 8, section 8.3.2 for details and Table B.1 in Appendix B for the value of $V_{S2,pp}$.
5. Place the EMV – TEST PICC at the first position defined in Table 8-39.
6. Set the DTE in LOOPBACK mode.
7. Make the EMV – TEST PICC return the response described in Table C.3 of Appendix C, Frame Trail for PCD Type B tests.
8. Observe the PCD behavior with the DTE or by other means. If the PCD continues with each next valid command described in the Frame Trail then the PCD is considered to function correctly.
9. Repeat steps 7 to 8 for all points defined in Table 8-39.

Acceptance Criteria

The PCD shall function correctly when the EMV – TEST PICC, placed in a position z which is ≥ 3 cm in height in the positioning tool, applies maximum negative load modulation characteristics. All responses shall be observed.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.7. Bit Level Coding Signal Interface for Type B Communications

This section presents the verifications applicable for Type B communications.

8.8.7.1. TB141.200 Verifying the PCD Transmitted Bit Rate

This test verifies the PCD to PICC bit rate during initialization.

Test Code

TB141.200

Reference

This test refers to requirement 4.2.1.1.

Procedure

Follow this procedure to verify the PCD to PICC bit rate during initialization:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at position ($z=2$, $r=0$, $\phi=0$).
6. Make sure that the CARRIER is switched on and set the PCD under test in WUPB mode.
7. Set the Acquisition Device to capture one WUPB command sent by the PCD.
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.

Figure 8-19 shows the bit rate for the WUPB command:

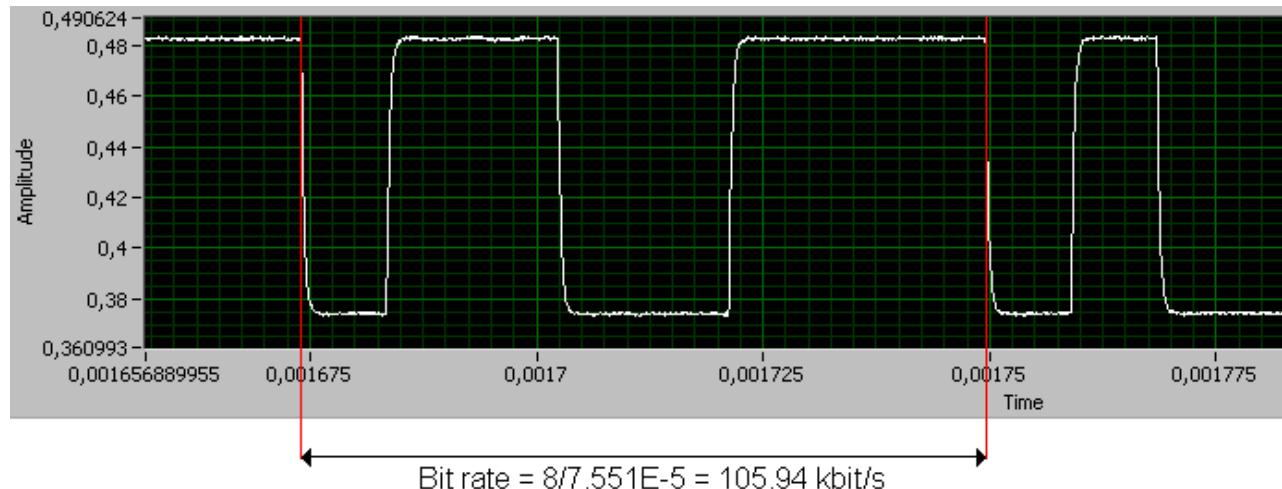


Figure 8-19—Bit Rate for the WUPB Command

10. Place an X-cursor (or its equivalent) to identify the falling edge when the PCD carrier envelope is at the beginning of the low level of the start bit of the second CRC byte ('73') within the WUPB command.
11. Place an X-cursor (or its equivalent) to identify the time when the PCD carrier envelope is at the equivalent point on the falling edge, at the start of a subsequent lower level within the WUPB command, where the two falling edges are 8 bit periods apart.
12. Calculate the bit rate as $8 / (\text{the difference between the times identified by the two X-cursors})$.

Acceptance Criteria

The bit rate shall be between $f_C / 128 \pm 0.5\%$.

Expected Results

Results are recorded with one of two statements:

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.7.2. TB142.200 Verifying the Synchronization, Bit Coding and De-synchronization of PCD to PICC

This test verifies the PCD command coding.

Test Code

TB142.200

Reference

This test refers to requirements 4.3.2.1, 4.4.3.1, 4.5.1.1 and 4.6.2.1.

Procedure

Follow this procedure to verify the PCD command coding:

1. Confirm that the content of WUPB coded by the PUT is the value '05' using EMV L1 digital tests.
2. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
3. Display the TTA L1 - Analogue menu using the DTE.
4. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
5. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
6. Place the EMV – TEST PICC at position ($z=2$, $r=0$, $\phi=0$).
7. Make sure that the CARRIER is switched on and set the PCD under test in WUPB mode.
8. Set the Acquisition Device to trigger to capture one WUPB command sent by the PCD.
9. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
10. Place an X-cursor or its equivalent to identify the time when the PCD carrier envelope is at the start of the first level change from high to low within the WUPB. This cursor shall be referenced as X1.
11. Place an X-cursor or its equivalent to identify the time - after X1 - when the PCD carrier envelope starts to change from low to high within the WUPB. This cursor shall be referenced as X2.
12. Measure the delay between X1 and X2. This duration is referenced as $t_{PCD,S,1}$.
13. Place X1 at the end of $t_{PCD,S,1}$ and place X2 to identify the time when the PCD carrier envelope starts to change from high to low after X1 within the WUPB.
14. Measure the delay between X1 and X2. This duration is referenced as $t_{PCD,S,2}$.

15. Place X1 at the end $t_{PCD,S,2}$ and place X2 at $X1 + 1$ etu, derived from the bit rate calculated in section 8.8.7.1 (TB141.z00). The time between X1 and X2 is defined as the bit duration.

16. Identify the symbol between X1 and X2 as follows:

- a) If the carrier is low (modulation applied) for the full bit duration, identify the symbol as L.
- b) If the carrier is high (no modulation applied) for the full bit duration, identify the symbol as H.
- c) If none of the previous cases has been identified, identify as an invalid symbol.

17. Complete Table 8-40 for the symbol you have identified.

Note: If there is a difference between X2 and the start of the next bit - named as bit boundaries - do not take it into account, it shall be verified in section 8.8.7.5 (TB147.z00).
Also do not take into account the rising and falling edges, or overshoots and undershoots. These are verified in sections 8.8.5.2 to 8.8.5.7 (TB122.z00 to TB127.z00).

18. Move the cursors X1 and X2 by 1 etu to identify the symbol over the next bit duration.

19. Repeat steps 16 to 18 for all the other symbols in Table 8-40.

20. Compare the identified symbols with the expected ones. The sequence of expected symbols corresponds to the first byte of the WUPB (0x05 NRZ-L coded with ASK 10% modulation).

21. Place X1 at the start of the falling edge of the first start bit of the PCD command and place X2 at the start of the falling edge of the start bit of the second character of the PCD command.

22. Measure $EGT_{PCD} = (X2 - X1 - 1280/f_C)$.

23. Place X1 at the start of the falling edge of the last start bit of the PCD command and place X2 at the start of the EoS falling edge.

24. Measure $EGT_{PCD,EoS} = (X2 - X1 - 1280/f_C)$.

25. Place X1 at the start of the EoS rising edge.

26. Measure the delay between X2 and X1. This duration is referenced as $t_{PCD,E}$.

Identified Symbol	Expected Symbol	First WUPB Bit Coding Correspondence
	L	Start Bit
	H	1
	L	0
	H	1

Identified Symbol	Expected Symbol	First WUPB Bit Coding Correspondence
	L	0
	L	0
	L	0
	L	0
	L	0
	H	Stop Bit

Table 8-40—Symbols Identified

Acceptance Criteria

The time between two consecutive characters sent by the PCD to the PICC shall be EGT_{PCD} . Refer to Table A.4 in Appendix A, Sequences and Frames for the applicable range of values for EGT_{PCD} .

The PCD shall code Start of Sequence (SoS) as follows:

- x $t_{PCD,S,1}$ with carrier low applied
- x $t_{PCD,S,2}$ with carrier high (no modulation applied)

The PCD shall code End of Sequence (EoS) as follows:

- x A time $t_{PCD,E}$ with carrier low (modulation applied) followed by a transition to carrier high.
- x The EoS shall come immediately after the last bit of the last data character (i.e. $EGT_{PCD,EoS} = 0$).

Refer to Table A.4 in Appendix A, Signal Interface for Type B for the applicable range of values for $t_{PCD,S,1}$, $t_{PCD,S,2}$ and $t_{PCD,E}$. Figure 8-20 shows an example of correct bit coding of the WUPB command.

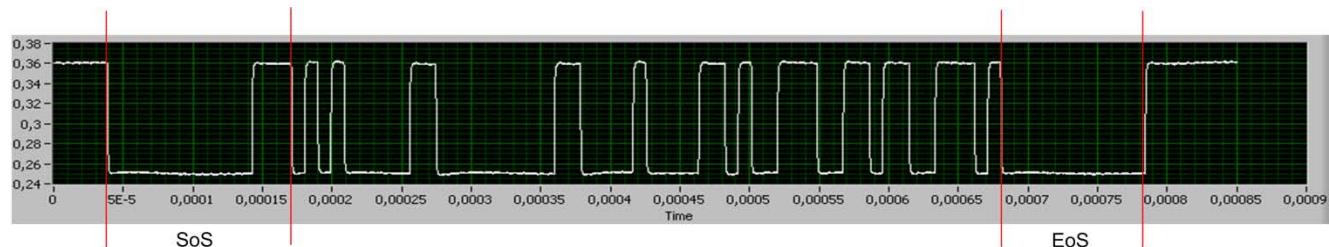


Figure 8-20—WUPB Bit Coding

The PCD shall code the first byte of WUPB command according to the sequence of expected symbols given in Table 8-40 .Figure 8-21 shows an example of correct coding of the first byte of WUPB command.

The symbols used shall be as follows:

- x Symbol H: the carrier is high for the full bit duration.
- x Symbol L: the carrier is low for the full bit duration.

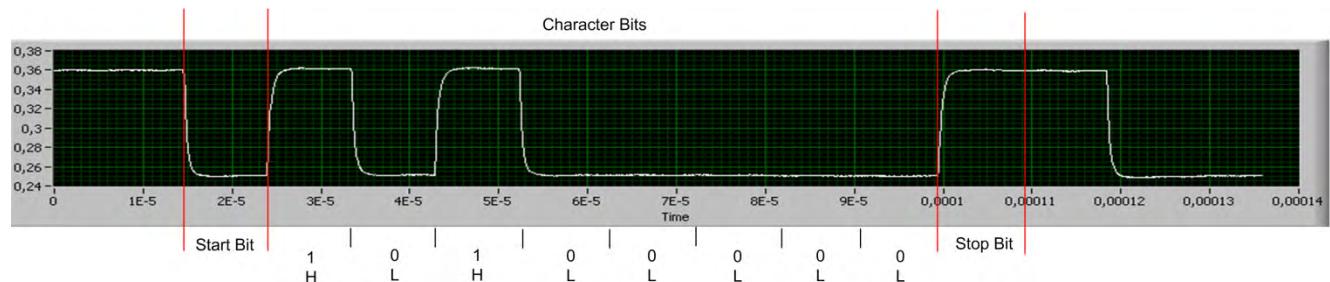


Figure 8-21—First Byte of WUPB Command Coding

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.7.3. TB145.200 Verifying the Maximum Limit De-synchronization PICC to PCD (t_{FSOFF,MAX})

This test verifies the PCD behavior when receiving a PICC answer with a maximum limit de-synchronization parameter.

Test Code

TB145.200

Reference

This test refers to requirement 4.6.2.5.

Procedure

Follow this procedure to verify the PCD behavior when receiving a PICC answer with a maximum limit de-synchronization parameter:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a nominal positive load modulation V_{S1,pp}. See Chapter 8, section 8.3.1 for details and Appendix B for the value of for V_{S1,pp}.
5. Place the EMV – TEST PICC at position (z=2, r=0, φ=0).
6. Make sure that the CARRIER is switched on and set the PCD under test in ATTRIB mode.
7. Detect when the PCD sends a WUPB command.
8. Send a PICC answer ATQB with correct format and timings as defined in Appendix C with a maximum limit t_{FSOFF} value of 272/f_C.
9. Observe if the PCD continues with the next command (ATTRIB).

Acceptance Criteria

The PCD shall be capable of supporting a PICC that maintains the subcarrier on for a time t_{FSOFF}.

The PCD shall continue with the next command when receiving a correct ATQB with a maximum limit t_{FSOFF} of 272/f_C.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.7.4. TB146.200 Verifying the Synchronization, Bit Coding and De-synchronization of PICC to PCD

This test verifies the PCD understanding of a correct PICC answer.

Test Code

TB146.200

Reference

This test refers to requirement 4.3.2.5, 4.4.4.1, 4.4.4.3 and 4.6.2.3.

Procedure

Follow this procedure to verify the PCD understanding of a correct PICC answer:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a nominal positive load modulation $V_{S1,pp}$. See Chapter 8, section 8.3.1 for details and Appendix B for the value of for $V_{S1,pp}$.
5. Place the EMV – TEST PICC at position ($z=2$, $r=0$, $\varphi=0$).
6. Make sure that the CARRIER is switched on and set the PCD under test in ATTRIB mode.
7. Detect when the PCD sends a WUPB command.
8. Send a correct PICC ATQB answer as defined in Appendix C.
9. Observe if the PCD continues with the next command (ATTRIB).

Acceptance Criteria

The PCD shall continue with the next command when receiving a correct PICC answer.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.7.5. TB147.200 Verifying the Bit Boundaries with Type B Communications

This test verifies the PCD bit boundaries.

Test Code

TB147.200

Reference

This test refers to requirement 4.5.1.3.

Procedure

Follow this procedure to verify the PCD bit boundaries:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input.
Connect the low-pass filter output to the input J8 of the EMV – TEST CMR.
Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device.
Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Make sure that there is no modulation applied to input J2 of the EMV – TEST PICC.
4. Configure the EMV – TEST PICC with a linear load (jumper settings J7 1-3 and J8 1-2).
5. Place the EMV – TEST PICC at position ($z=2$, $r=0$, $\varphi=0$).
6. Make sure that the CARRIER is switched on and set the PCD under test in WUPB mode.
7. Set the Acquisition Device to capture one WUPB command sent by the PCD
8. Optimize the Acquisition Device settings for accurate measurement of waveform level and timing.
9. Launch the acquisition.
10. Identify and select the first character within the WUPB command.

11. Figure 8-22 shows the bit boundaries:

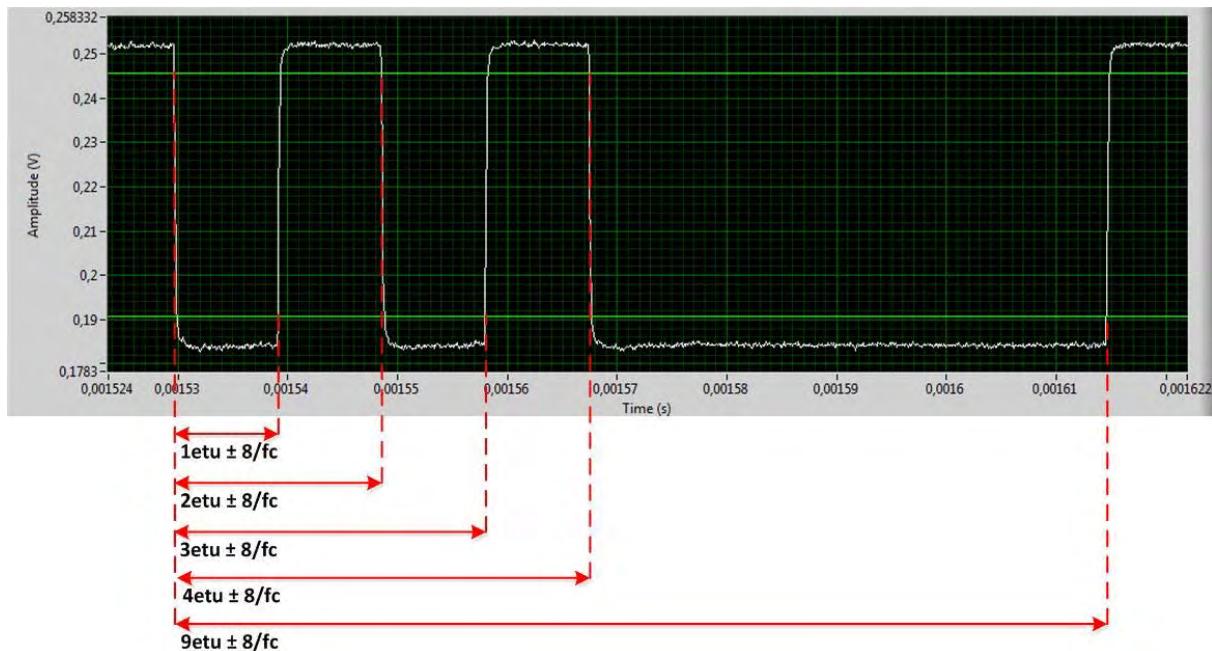


Figure 8-22—Bit Boundaries

12. Place an X-cursor (or its equivalent) at the start of the falling edge of the first start bit of the WUPB command.
13. Place an X-cursor (or its equivalent) at the start of the first rising edge of the character.
14. Determine the timing as the difference between the times identified by the two X-cursors.
15. Repeat steps 13 to 14 to determine the intervals between the start of the start bit and the start of all edges of the selected character.
16. Repeat steps 12 to 15 for all characters of the WUPB command.

Acceptance Criteria

The PCD shall apply bit boundaries within a character that are between $(n \text{ etu} - 4/f_C)$ and $(n \text{ etu} + 4/f_C)$, where n is the number of bit boundaries after the start bit falling edge ($1 \leq n \leq 9$).

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

8.8.7.6. TB148.200 Verifying the Minimum Limit De-synchronization PICC to PCD ($t_{FSOFF,MIN}$)

This test verifies the PCD behavior when receiving a PICC answer with a minimum limit de-synchronization parameter.

Test Code

TB148.200

Reference

This test refers to requirement 4.6.2.5.

Procedure

Follow this procedure to verify the PCD behavior when receiving a PICC answer with a minimum limit de-synchronization parameter:

1. Connect the output J9 of the EMV – TEST PICC to the low-pass filter input. Connect the low-pass filter output to the input J8 of the EMV – TEST CMR. Connect the output J4 of the EMV – TEST CMR to the CH0 input of the Acquisition Device. Connect the output J3 of the EMV – TEST CMR to the Clock input of the Acquisition Device.
2. Display the TTA L1 - Analogue menu using the DTE.
3. Configure the EMV – TEST PICC with a non-linear load (jumper settings J7 1-3 and J8 1-4).
4. Set up the EMV – TEST PICC to generate a nominal positive load modulation $V_{S1,pp}$. See Chapter 8, section 8.3.1 for details and Appendix B for the value of for $V_{S1,pp}$.
5. Place the EMV – TEST PICC at position ($z=2, r=0, \phi=0$).
6. Make sure that the CARRIER is switched on and set the PCD under test in ATTRIB mode.
7. Detect when the PCD sends a WUPB command.
8. Send a PICC answer ATQB with correct format and timings as defined in Appendix C with a minimum limit t_{FSOFF} value of $0/f_C$.

Note: If $t_{FSOFF} = 0$, it means that the subcarrier is turned off at the time of the phase transition from Φ_{0+180° to Φ_0 , as a result the stopping of the subcarrier represents the end of the EoS.

9. Observe if the PCD continues with the next command (ATTRIB).

Acceptance Criteria

The PCD shall be capable of supporting a PICC that maintains the subcarrier on for a time t_{FSOFF} .

The PCD shall continue with the next command when receiving a correct ATQB with a minimum limit t_{FSOFF} of $0/f_C$.

Expected Results

Results are recorded with one of two statements:

- x Pass message
- x Fail message including a list of all failed conditions and reference details of the acceptance criterion not met.

A. PCD Acceptance Criteria

A.1 Power and Parameters

Note: As a low pass filter is used, the measurement of the signal shall be corrected according to its insertion loss at 13.56 MHz

Table A.1 shows the RF parameters to measure on the unmodulated PCD under test carrier and associated values:

Topic	Parameter	Minimum	Nominal	Maximum	Unit
Power Transfer PCD → PICC	V _{OV} (0 ϑ)	3.10 – 0.05z		8.1	V
	V _{OV} (2 ϑ)	3.45 – 0.225z		8.1	V
	V _{SENSE,MAX}	0		0.7	V
	V _{OV,RESET}	0		3.5	mV RMS
	V _{OV,POWEROFF}	0		3.5	mV RMS
Carrier frequency	f _C	13.553	13.560	13.567	MHz

Table A.1—RF Power

Table A.2 shows the parameters to measure on the signal interface for Type A communications:

Topic	Parameter	Minimum	Nominal	Maximum	Unit
Type A	t ₁	2.06		2.99	μs
	t ₂	0.52		t ₁	μs
	t ₃	0		1.18	μs
	t ₄	0		minimum (0.44, t ₃ / 1.5)	μs
	t ₅	0		0.50	μs
	V _{OU,A}	0		0.10	-

Table A.2—Signal Interface for Type A

Table A.3 shows the parameters to measure on the signal interface for Type B communications:

Topic	Parameter	Minimum	Nominal	Maximum	Unit
PCD → PICC modulation	mod _i	9.0		15.0-0.25z	%
	t _f	0		1.18	\$P
	t _r	0		1.18	\$P
	V _{OU,B}	0		0.1	-

Table A.3—Signal Interface for Type B

Table A.4 shows the parameters which are measured in the Chapter 8 tests relative to the Sequences and Frames section of the EMV Contactless specification:

Topic	Parameter	Minimum	Nominal	Maximum	Unit
Type B	t _{PCD,S,1}	1280		1416	1/f _C
	t _{PCD,S,2}	248		392	1/f _C
	t _{PCD,S,E}	1280		1416	1/f _C
	EGT _{PCD}	0		752	1/f _C
	EGT _{PCD,EOS}			0	1/f _C
	FWT _{ATQB}	7680			1/f _C

Table A.4—Sequences and Frames

Table A.5 shows the parameters which are measured in the Chapter 8 tests relative to the PCD processing section of the EMV Contactless specification:

Topic	Parameter	Minimum	Nominal	Maximum	Unit
Reset	t _{RESET}	5.1		10	ms
Power-off	t _{POWEROFF}	15			ms

Table A.5—PCD processing

B. Set-up Values for EMV Test Equipment

B.1. Load Modulation Parameters

Table B.1 shows the load modulation amplitude parameters for EMV – TEST PICC tuning when testing the PCD for receptivity.

Topic	Parameter	Minimum	Nominal	Maximum	Unit
PCD Nominal Power	$V_{N,OV}$		5.53		V
Load Modulation	$V_{S1,pp}$	5.5	20	85	mV
	$V_{S2,pp}$	3.5	20	40	mV

Table B.1—Load Modulation Parameters

C. PICC Emulation: Frame Trail

C.1. Frame Trail for Type A PCD Tests

Table C.1 shows the frame trail for Type A PCD tests:

Step	Exchanges		Comments
1	PCD ► '52' (short frame)	► PICC	WUPA during polling
2	PCD ▲ '08 03' (no CRC_A) sent using the delay FDT _{A,PICC,MIN}	◀ PICC	ATQA
3	PCD ► '50 00'	► PICC	HLTA
4	PCD ► '05 00 08' (Type B frame)	► PICC	WUPB
o1	PCD ► The PCD is allowed to support other technologies than EMV CL Type A and B. These optional commands are disregarded by the test tool	PICC	Optional polling for other technologies than EMV Contactless Type A and B
o2	PCD If the PCD has sent at least one command for another technology than EMV CL Type A and B at step o1, then it <u>shall</u> perform a PICC Reset	PICC	Optional PICC Reset
5	PCD ► '52' (short frame)	► PICC	WUPA
6	PCD ▲ '08 03' (no CRC_A) sent using the delay FDT _{A,PICC,MIN}	◀ PICC	ATQA
7	PCD ► '93 20' (no CRC_A)	► PICC	ANTICOLLISION CL1
8	PCD ▲ '27 E9 3B 11' + 'E4' (no CRC_A) sent using the delay FDT _{A,PICC,MIN}	◀ PICC	UID
9	PCD ► '93 70' + '27 E9 3B 11' + 'E4'	► PICC	SEL1 + UID CL1 + BCC
10	PCD ▲ '20' sent using the delay FDT _{A,PICC,MIN}	◀ PICC	SAK
11	PCD ► 'E0 80'	► PICC	RATS
12	PCD ▲ '05 72 80 40 02' sent using the delay FDT _{A,PICC,NOM}	◀ PICC	ATS
13	PCD ► I(0) ₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	► PICC	Select PPSE Command
14	PCD ▲ I(0) ₀ ['00 A4 04 00 0C' + '01 02 ... 0C' + '00' + '90 00'] sent using the delay FDT _{A,PICC,NOM}	◀ PICC	Correct response frame
15	PCD ► I(0) ₁ ['00 A4 04 00 0C' + '01 02 ... 0C' + '00']	► PICC	Loop-back

Step	Exchanges	Comments
16	PCD \leftarrow I(0) ₁ ["EOT Command" + '90 00'] sent using the delay FDT _{A,PICC,NOM}	\leftarrow PICC End of Test command
17	PCD \rightarrow The PUT performs a PICC Reset (i.e. stops sending the carrier)	\rightarrow PICC PICC Reset
18	PUT \rightarrow '52' (short frame)	\rightarrow PICC WUPA to poll for the PICC
19	PUT \rightarrow '52' (short frame)	\rightarrow PICC WUPA to poll for the PICC
20	PUT \rightarrow '52' (short frame)	\rightarrow PICC WUPA to poll for the PICC

Table C.1—Frame Trail for Type A PCD Tests

Unless specified otherwise in the Test Cases, the Testing Laboratory shall use the values from Table C.2 during the tests:

Parameter	PICC	Unit
FDT _{A,PICC,MIN}	1236 if last logic state 1 1172 if last logic state is 0	1/f _C
FDT _{A,PICC,NOM}	3156 if last logic state 1 3092 if last logic state is 0	1/f _C
Bit rate	f _C /128	bps

Table C.2—Parameter Values

Note: Unless specified in the test case, the EOT Command shall be set to "Removal procedure".

C.2.FDT_{A,PICC}

FDT_{A,PICC} is a measurement starting from the rising edge of the last lower level of the PCD command to the start of the SoF of the PICC response.

The FDT_{A,PICC} depends on the logic state of the last data bit transmitted by the PCD before the EoF.

Note: The Contactless Specification prohibits FDT_{A,PICC} timing that falls below the nominal values in Table C.2. Unless specified otherwise in the test procedure, the laboratory shall increase the FDT_{A,PICC} timing value used by an amount equal to half the FDT_{A,PICC} time window.

Figure C-1 shows the timing diagram for FDT_{A,PICC} measurement:

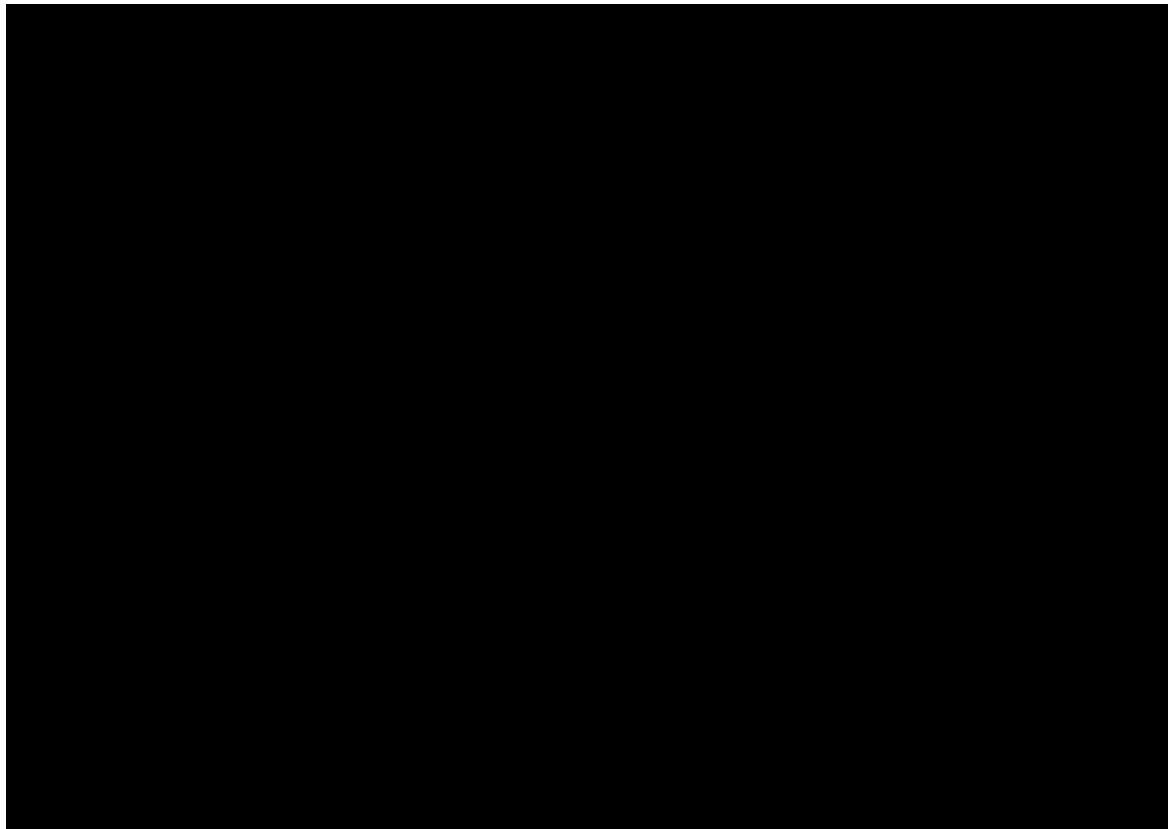


Figure C-1—Timing Diagram for FDT_{A,PICC}

Note: When establishing measurement points with a cursor (or its equivalent), unless otherwise stated in the test procedure, always use the reference points as specified in Appendix E. Do this consistently to maintain measurement accuracy.

C.3.Frame Trail for Type B PCD Tests

Table C.3 shows the frame trail for Type B PCD tests:

Step	Exchanges		Comments
1	PCD ► '05 00 08'	► PICC	WUPB during polling
2	PCD ▲ '50' + '46 B5 C7 A0' + '00 00 00 00' + '00 21 81' sent using the delay FDT _{B,PICC,NOM}	◀ PICC	ATQB
3	PCD ► '52' (Type A short frame)	► PICC	WUPA
o1	PCD ► The PCD is allowed to support other technologies than EMV CL Type A and B. These optional commands are disregarded by the test tool	II PICC	Optional polling for other technologies than EMV Contactless Type A and B
o2	PCD II If the PCD has sent at least one command for another technology than EMV CL Type A and B at step o1, then it shall perform a PICC Reset	II PICC	Optional PICC Reset
4	PCD ► '05 00 08'	► PICC	WUPB
5	PCD ▲ '50' + '46 B5 C7 A0' + '00 00 00 00' + '00 21 81' sent using the delay FDT _{B,PICC,NOM}	◀ PICC	ATQB
6	PCD ► '1D' + '46 B5 C7 A0' + '00 08 01 00'	► PICC	ATTRIB
7	PCD ▲ '00' sent using the delay FDT _{B,PICC,NOM}	◀ PICC	ATTRIB Response
8	PCD ► I(0) ₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	► PICC	Select PPSE Command
9	PCD ▲ I(0) ₀ ['00 A4 04 00 0C' + '01 02 ... 0C' + '00' + '90 00'] sent using the delay FDT _{B,PICC,NOM}	◀ PICC	Correct response frame
10	PCD ► I(0) ₁ ['00 A4 04 00 0C' + '01 02 ... 0C' + '00']	► PICC	Loop-back
11	PCD ▲ I(0) ₁ ["EOT Command" + '90 00'] sent using the delay FDT _{B,PICC,NOM}	◀ PICC	End of Test command
12	PCD II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II PICC	PICC Reset
13	PUT ► '05 00 08'	► PICC	WUPB to poll for the PICC
14	PUT ► '05 00 08'	► PICC	WUPB to poll for the PICC
15	PUT ► '05 00 08'	► PICC	WUPB to poll for the PICC

Table C.3—Frame Trail for Type B PCD Tests

Unless specified otherwise in the Test Cases, the Testing Laboratory shall use the values from Table C.4—Parameter Values during the tests:

Parameter	PICC	Unit
$FDT_{B,PICC,NOM}$	3072	$1/f_c$
TR0	1536	$1/f_c$
TR1	1536	$1/f_c$
Bit rate	$f_c / 128$	bps
$t_{PICC,S,1}$	1344	$1/f_c$
$t_{PICC,S,2}$	320	$1/f_c$
$t_{PICC,E}$	1344	$1/f_c$
t_{FSOFF}	8	$1/f_c$
EGT_{PICC}	0	$1/f_c$
$EGT_{PICC,MAX}$	272	$1/f_c$
$EGT_{PICC,EoS}$	0	$1/f_c$
$EGT_{PICC,EoS,MAX}$	272	$1/f_c$

Table C.4—Parameter Values

Note: Unless specified in the test case, the EOT Command shall be set to “Removal procedure”.

C.4. $FDT_{B,PICC}$

For Type B communications, $FDT_{B,PICC}$ measurement starts at the end of the EoS of the PCD command and goes to the beginning of the SoS of the PICC response.

$$FDT_{B,PICC} = TR0 + TR1$$

C.4.1. PICC Start of Sequence

Figure C-2 shows the timing diagram between the end of a command sent to a PICC and the beginning of the PICC sequence response:

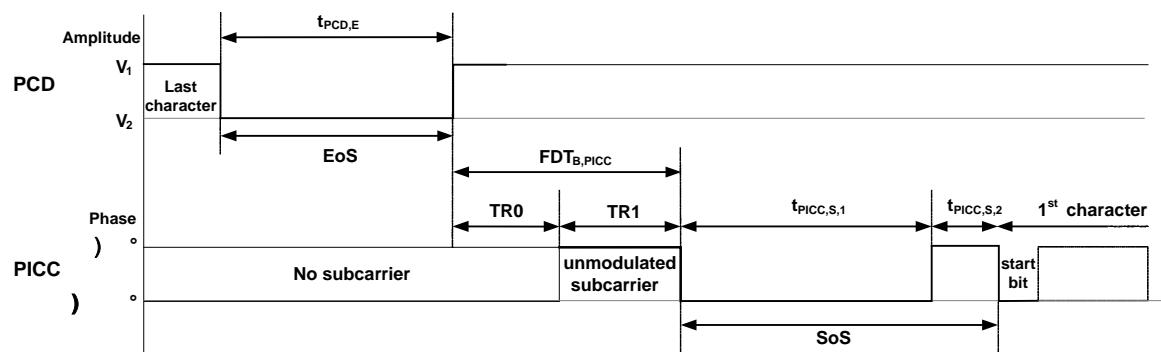


Figure C-2—PICC Start of Sequence

Note: When establishing measurement points with a cursor (or its equivalent), unless otherwise stated in the test procedure, always use the reference points as specified in Appendix E. Do this consistently to maintain measurement accuracy.

C.4.2. PCD Start of Sequence

Figure C-3 shows the timing diagram between the end of a PICC response and the beginning of a PCD command sequence:

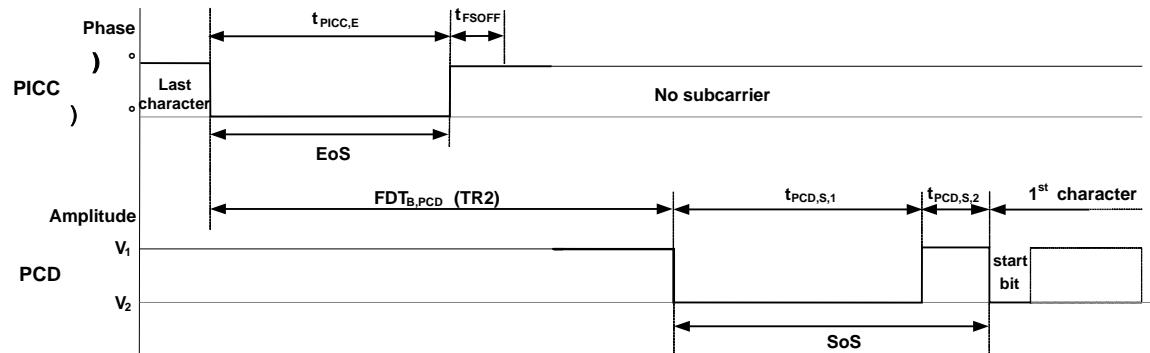


Figure C-3—PCD Start of Sequence

Note: When establishing measurement points with a cursor (or its equivalent), unless otherwise stated in the test procedure, always use the reference points as specified in Appendix E. Do this consistently to maintain measurement accuracy.

D. Reference Implementation

D.1. Reference Implementation Using Peak Sampling

The implementation defined in this appendix was used during the development of the Test cases described in this document. Other implementations are possible but all test functionalities must be correctly implemented according to specifications.

A step by step procedure for cabling and a functional overview accompanies each connectivity diagram. Refer to Chapter 5 for more information on the requirements with respect to the reference implementation.

Note: For all connections in the reference implementation, the standard cable is a high quality coaxial cable, such as RG-316, terminated by SMA connectors. The cable ends are then fitted with appropriate adaptors for the connections to be made. However, adaptors are not shown in the connectivity diagrams.

Note: Cables connected to Test Bench equipment shall be as short as possible, ideally less than 50 cm. However, cables connected to computers and power supplies may have a length of up to 100 cm. This allows physical separation of the equipment to minimize coupling of electromagnetic disturbances to sensitive components of the Test Bench.

D.1.1. Set Up of the EMV TEST PICC

Follow this procedure to set up the EMV – TEST PICC for PCD testing:

1. Refer to the connectivity diagram in Figure D-1:

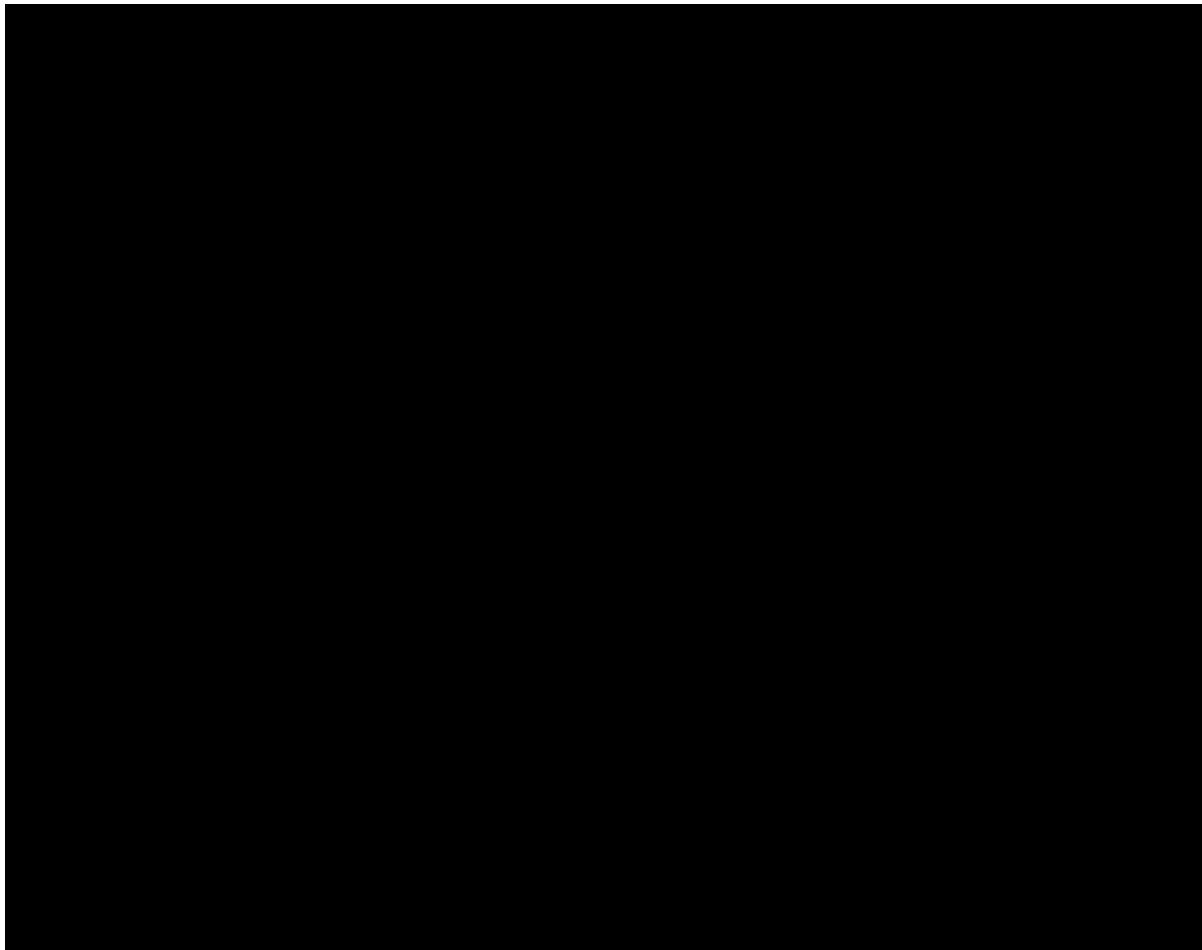


Figure D-1—Connectivity Diagram to Set up the EMV – TEST PICC for PCD Testing

2. Connect a cable to the Out 1 connector of the PICC Coding Generator.
3. Connect the other end of the cable to the In connector of the Load Modulation Adjustment.
4. Connect a cable to the Out connector of the Load Modulation Adjustment.
5. Connect the other end of the cable to the input J2 connector of the EMV – TEST PICC.
6. Connect a probe to CH0 of a DSO.
7. Connect the other end of the probe to J1 of the EMV – TEST PICC.

Note: To improve measurements repeatability and coherency, the cable connecting J1 of the EMV – Test PICC to CH0 of the DSO shall remain connected at all times during testing.

8. Connect a cable to the CLK input of the A/D converter.

9. Connect the other end of the cable to the output J3 of the EMV – TEST CMR.
10. Connect a cable to the input CH0 of the A/D converter.
11. Connect the other end of the cable to the output J4 of the EMV – TEST CMR.
12. Connect a cable to the input J2 of the EMV – TEST CMR.
13. Connect the other end of the cable to the output J2 of the PCD.
14. Connect a USB cable to the PC.
15. Connect the other end of the cable to the USB/I2C Converter.
16. Connect a cable to the other side of the USB/I2C Converter.
17. Connect the other end of the cable to the I2C connector on the EMV – TEST CMR.
18. Connect a cable to Out 1 connector of the Waveform Generator.
19. Connect the other end of the cable to the input of the RF Amplifier.
20. Connect a cable to the output of the RF Amplifier.
21. Connect the other end of the cable to input J1 of the PCD.
22. Connect all power supplies as required.

D.1.2. Implementation Set-up Overview

This implementation is based on an A/D converter using a peak sampling acquisition system. The EMV – TEST CMR generates the A/D converter CLK signal for peak sampling.

PICC signal generation comprises the PICC Coding Generator and the Load Modulation Adjustment. The output of the Load modulation Adjustment connects to the input J2 of the EMV – TEST PICC.

The PCD signal generator comprises the Waveform Generator and the RF Amplifier. The output of the Waveform Generator connects to the input of the RF Amplifier. The output of the RF Amplifier is connected on connector J1 of the EMV – TEST PCD.

The acquisition system comprises the EMV – TEST CMR and an A/D converter circuit board located in a PC. Connector J2 of the EMV – TEST PCD connects to the input J2 of the EMV – TEST CMR. The EMV – TEST CMR generates a clock on its output J3, which is connected on the CLK input of the A/D converter.

The output J4 of the EMV – TEST CMR is connected on CH0 of the A/D circuit board. The field strength of the EMV – TEST PCD is measured on the output J1 of the EMV – TEST PICC. This output connects to CH0 of the DSO, passing through a probe. The example Virtual Instrument (VI) provided with the EMV Test Equipment controls the EMV – TEST CMR.

D.1.3. Test Bench for the PCD Test

Follow this procedure to set up the test bench for PCD testing:

1. Refer to the connectivity diagram in Figure D-2 :

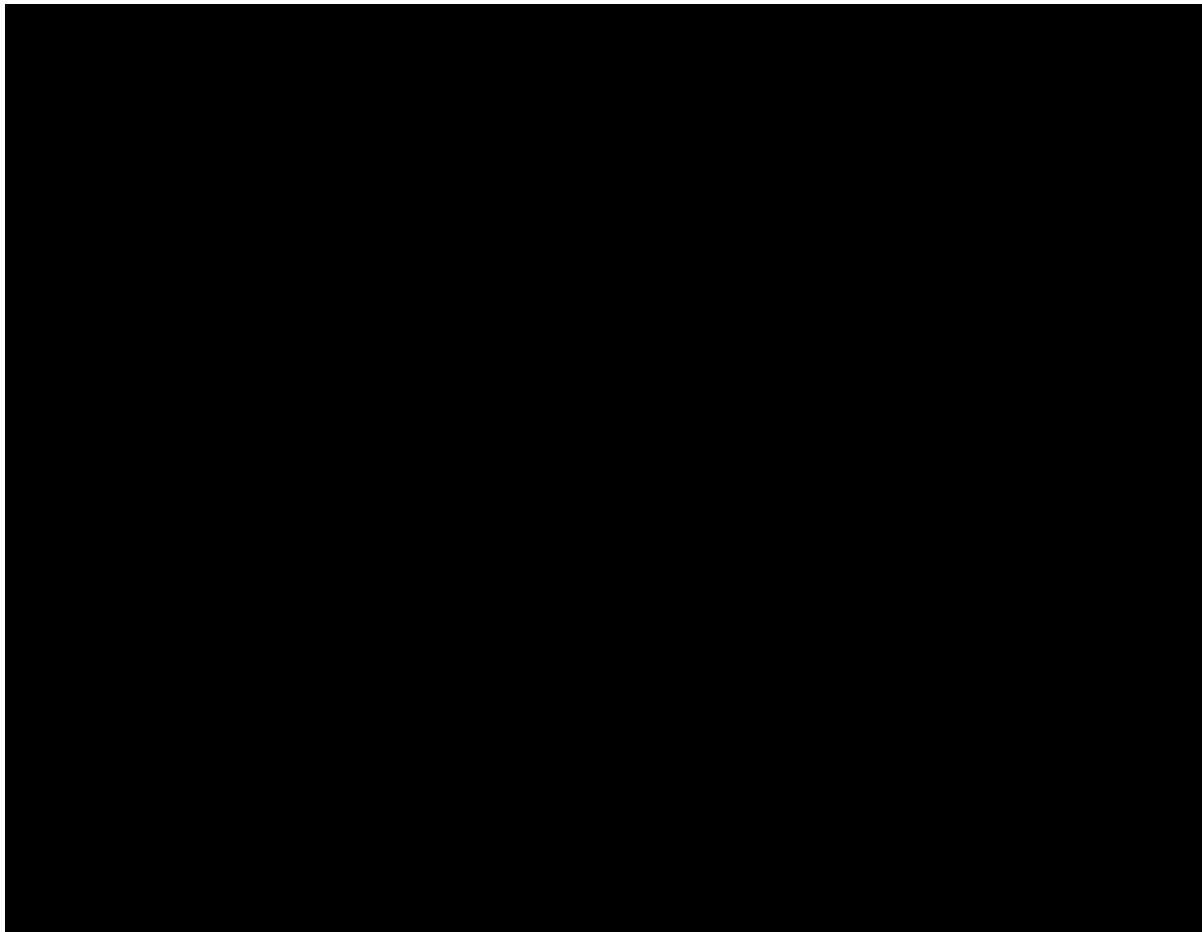


Figure D-2—Connectivity Diagram to Set up the Test Bench for PCD Testing

In this implementation, the PICC Synchronization Device is controlled by the PC. The PICC Sync Device is capable of generating a trigger for both Type A and Type B transactions, as appropriate.

Since the PICC Coding Generator only features a single trigger (Trg A) input, either Trg A or Trg B shall be connected to it depending on the transaction Type for the test case. The connection depends on the PICC answer to be sent.

For a Type A PICC answer, connect Trg A to the PICC Coding Generator. For a Type B PICC answer, connect Trg B.

2. Depending on the Test Case, connect a cable to the Trg A connector of the PICC Coding Generator and connect the other end of the cable to the Trg A connector of the PICC Sync Device.

Or

Connect a cable to the Trg B connector of the PICC Coding Generator and connect the other end of the cable to the Trg B connector of the PICC Sync Device.

3. Connect the antenna to the PICC Sync Device.

4. Connect a USB cable from the PC to the PICC Sync Device.
5. Connect a cable to the Out 1 connector of the PICC Coding Generator.
6. Connect the other end of the cable to the IN connector of the Load Modulation Adjustment.
7. Connect a cable to the Out connector of the Load Modulation Adjustment.
8. Connect the other end of the cable to the input J2 connector of the EMV – TEST PICC.
9. Connect a probe to CH0 of a DSO.
10. Connect the other end of the probe to J1 of the EMV – TEST PICC.

Note: To improve measurements repeatability and coherency, the cable connecting J1 of the EMV – Test PICC to CH0 of the DSO shall remain connected at all times during testing.

11. Connect a cable to the CLK input of the A/D converter.
12. Connect the other end of the cable to the output J3 of the EMV – TEST CMR.
13. Connect a cable to the input CH0 of the A/D converter.
14. Connect the other end of the cable to the output J4 of the EMV – TEST CMR.
15. Connect a cable to the input J8 of the EMV – TEST CMR.
16. Connect the other end of the cable to the output of a 20 MHz filter.
17. Connect a cable to the input of the 20 MHz filter.
18. Connect the other end of the cable to the output J9 of the EMV – TEST PICC.
19. Connect a USB cable to the PC.
20. Connect the other end of the cable to the USB/I2C Converter.
21. Connect a cable to the other side of the USB/I2C Converter.
22. Connect the other end of the cable to the I2C connector on the EMV – TEST CMR.
23. Connect all power supplies as required.

D.1.4. Implementation Set-up Overview

A PCD under test replaces the EMV – TEST PCD during actual testing. A PICC Synchronization device properly synchronizes the emulated PICC answer with the PCD commands.

PICC signal generation is composed of the PICC Coding Generator connected to a Load Modulation Adjustment. The output of the Load modulation Adjustment goes to input J2 of the EMV – TEST PICC.

The output J1 of the EMV – TEST PICC connects to CH0 of the DSO, passing through a probe, and allows measurement of the field strength of the PCD under test.

Connector J9 of the EMV – TEST PICC connects to input J8 of the EMV – TEST CMR, passing through a 20 MHz filter, and allows measurement of all other parameters.

The CMR generates a clock on its output J3 which connects to the input CLK of the A/D converter.

The output J4 of the EMV – TEST CMR connects to CH0 of the A/D board. An example VI is provided with the EMV Test Equipment and controls the EMV -TEST CMR.

Note: As the correct measurement result is the value of the signal at the input of the EMV – TEST CMR and not the one measured on the output, the EMV – TEST CMR gain shall be measured before a complete test session, as described in Chapter 7.

E. Timing Measurements Methods

E.1. Setup of Cursors and their Positioning

To maintain consistency across all laboratories in timing measurements, it is important to follow the guidelines described in this appendix.

For all these measurements, the test bench must capture the start and the end of the FDT in a single acquisition.

E.1.1. Summary Tables

Table E-1 summarizes the timing measurement methods regarding Type A :

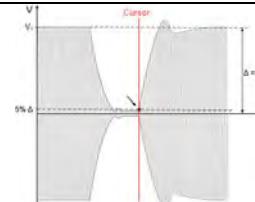
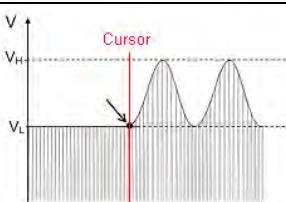
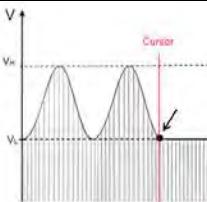
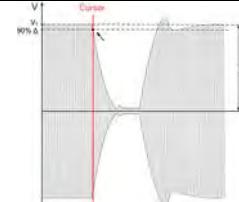
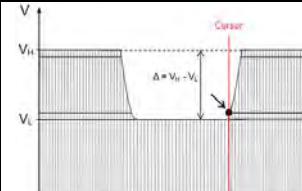
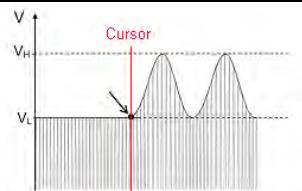
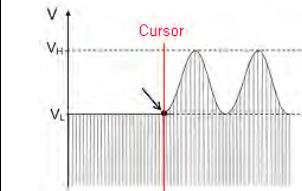
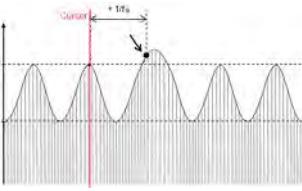
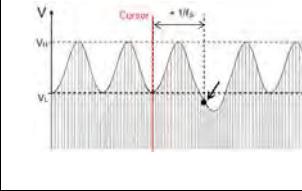
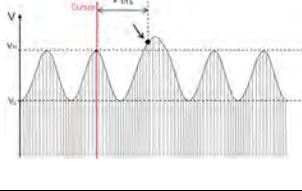
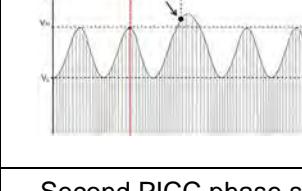
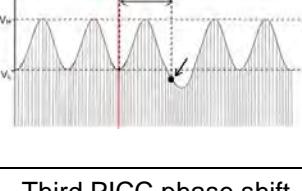
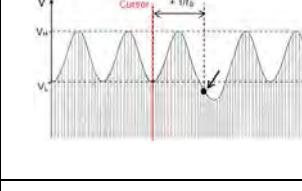
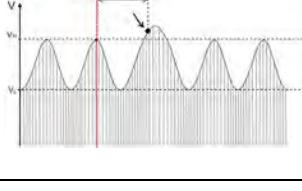
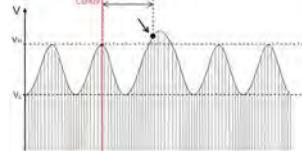
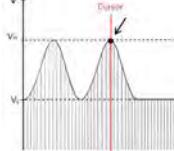
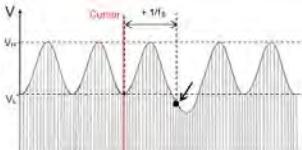
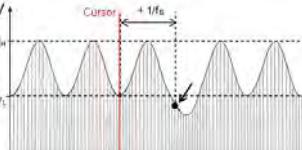
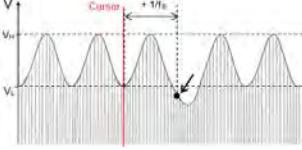
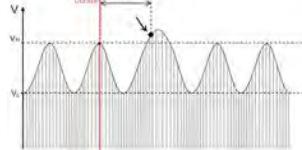
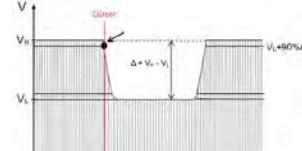
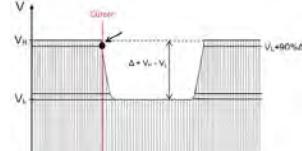
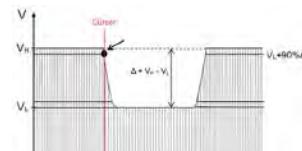
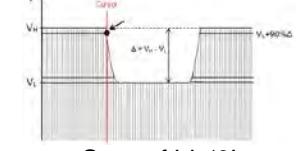
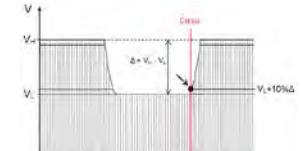
Type A Summary Table		
Parameter	Start	End
$FDT_{A,PICC}$		
	Last PCD rising edge	First PICC rising edge
	$FDT_{A,PICC} = t_{END} - t_{START}$	
$FDT_{A,PCD}$		
	Last PICC detectable edge	First PCD falling edge
	$FDT_{A,PCD} = t_{END} - t_{START}$	

Table E-1—Type A Summary Table

Table E-2 summarizes the timing measurement methods regarding Type B :

Type B Summary Table		
Parameter	Start	End
TR0		
	Last PCD rising edge	First PICC rising edge
	$TR0 = t_{END} - t_{START}$	
TR1		
	First PICC rising edge	First PICC phase shift
	$TR1 = t_{END} - t_{START} + 16/f_c$	
$t_{PICC,S,1}$		
	First PICC phase shift	Second PICC phase shift
	$t_{PICC,S,1} = t_{END} - t_{START}$	
$t_{PICC,S,2}$		
	Second PICC phase shift	Third PICC phase shift
	$t_{PICC,S,2} = t_{END} - t_{START}$	
$t_{PICC,E}$		
	PICC phase shift preceding last phase shift or PICC last phase shift if $t_{FSOFF} = 0$	Last PICC phase shift or last subcarrier peak if $t_{FSOFF} = 0$
	$t_{PICC,E} = t_{END} - t_{START} \text{ if } t_{FSOFF} \neq 0$ $t_{PICC,E} = t_{END} - t_{START} - 16/f_c \text{ if } t_{FSOFF} = 0$	

Type B Summary Table		
Parameter	Start	End
t_{FSOFF}		
	Last PICC phase shift if $t_{FSOFF} \neq 0$	Last PICC subcarrier peak
	$t_{FSOFF} = t_{END} - t_{START} - 16/f_c$	
EGT_{PICC}		
	Phase shift preceding character n start bit	Phase shift preceding character n+1 start bit
	$EGT_{PICC} = t_{END} - t_{START} - 1280/f_c$	
PICC Bit Boundaries		
	Phase shift preceding character n start bit	Phase shift of each character bit
	$\text{PICC Bit Boundary} = t_{END} - t_{START}$	
EGT_{PCD}		
	Start bit of character n	Start bit of character n+1
	$EGT_{PCD} = t_{END} - t_{START} - 1280/f_c$	
PCD Bit Boundaries		 Start of bit '0'
	$\Delta = V_u - V_l = V_u + 90\% \Delta$	
	Start bit of character n	 Start of bit '1'
$\Delta = V_u - V_l = V_u + 10\% \Delta$		Start of each character bit

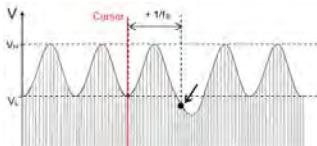
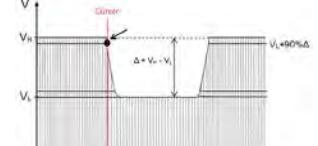
Type B Summary Table		
Parameter	Start	End
PCD Bit Boundary = $t_{\text{END}} - t_{\text{START}}$		
$FDT_{B,\text{PCD}}$		
	Last PICC phase shift if $t_{\text{FSOFF}} = 0$, else previous phase shift (Start of EoS)	First PCD falling edge
	$FDT_{\text{PCD}} = t_{\text{END}} - t_{\text{START}} - 16/f_c$	

Table E-2—Type B Summary Table

E.1.2. Cursors Positioning details

The start of the lower level of the SoF of a PCD command is the point where the falling edge of the signal envelope passes through the 90% threshold as shown Figure E-1:

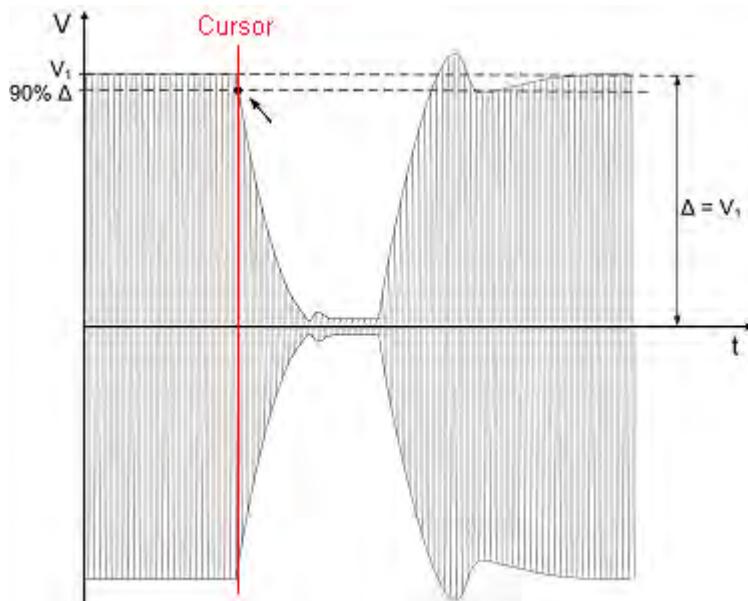


Figure E-1— Type A PCD Start

The end of the last lower level of a PCD command is the point where the rising edge of the last lower level of the signal envelope passes through the 5% threshold as shown in Figure E-2

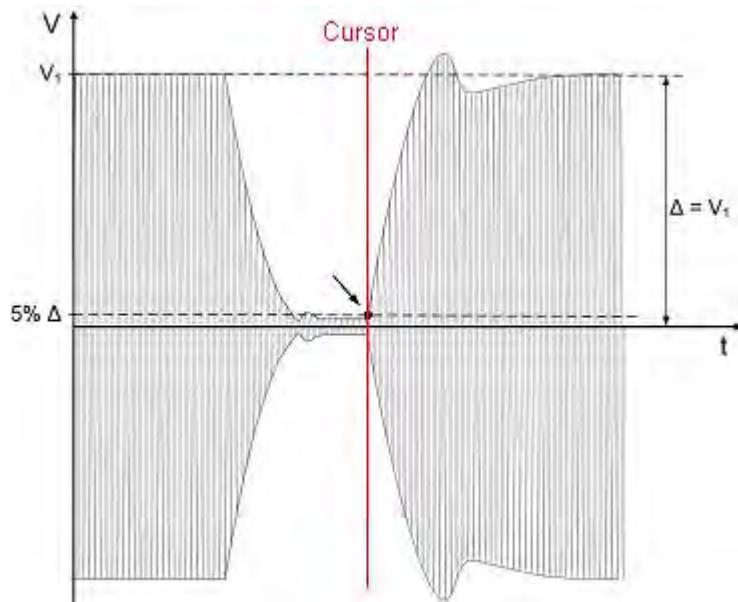


Figure E-2— Type A PCD Start

The start of the SoF of the PICC response begins at the start of the first detectable edge of the modulation of the signal envelope. Three cases are represented in Figure E-3 start for positive modulation, negative modulation and modulation that is not purely negative or positive.

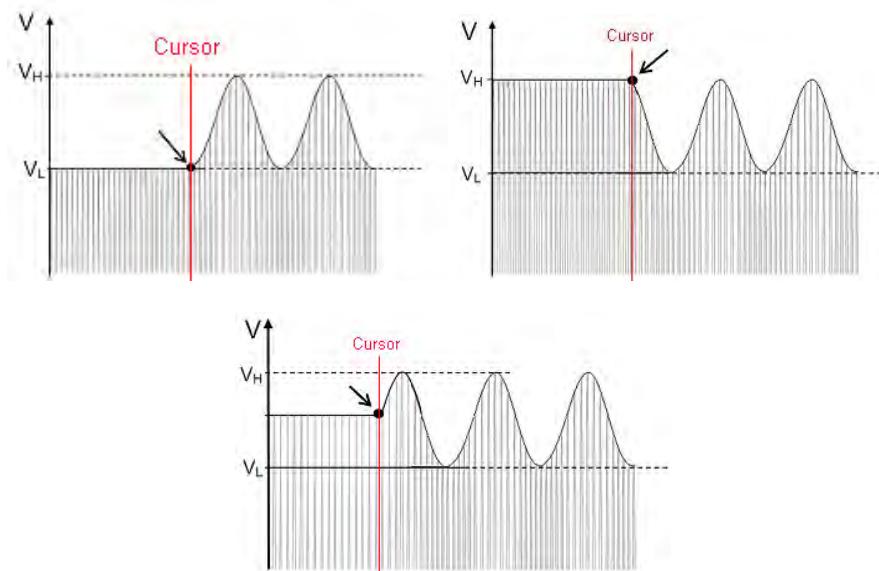


Figure E-3— Type A PICC Start

The end of the last subcarrier modulation transmitted by the PICC corresponds to the end of the last detectable edge of the modulation of the signal envelope. Three cases are represented in Figure E-4: end for positive modulation, negative modulation and modulation that is not purely negative or positive.

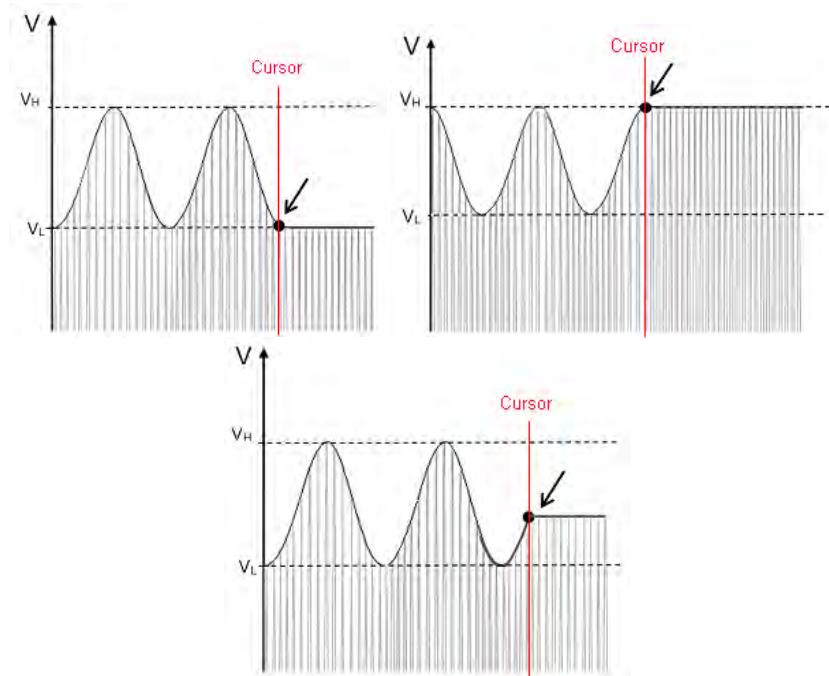


Figure E-4— Type A PICC End

The start of the SoS of a PCD command is when the first modulation of the signal envelope passes through the 90% level of the Δ threshold (Δ is the difference between modulated and unmodulated signal levels) as shown in Figure E-5:

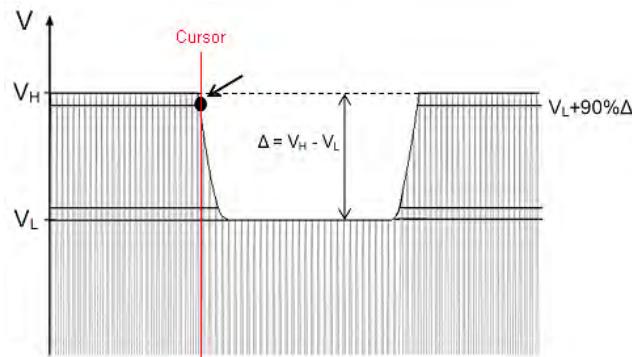


Figure E-5— Type B PCD Start

Figure E-6 indicates the end of the EoS of the PCD command. It is the point where the last modulation of the signal envelope passes through the 10% level of the Δ threshold (Δ is the difference between modulated and unmodulated signal levels).

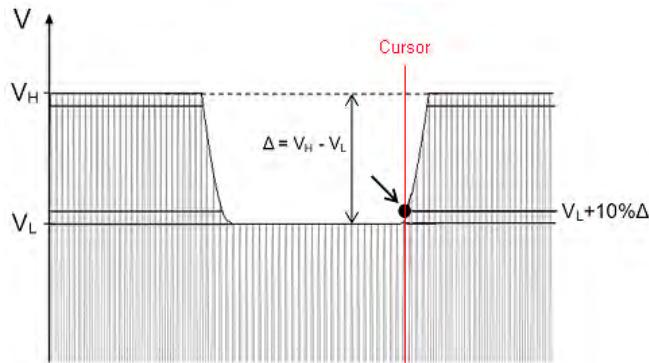


Figure E-6— Type B PCD End

The start of the PICC response begins at the start of the first detectable edge of the modulation of the signal envelope. Three cases are represented in Figure E-7 start for positive modulation, negative modulation and modulation that is not purely negative or positive.

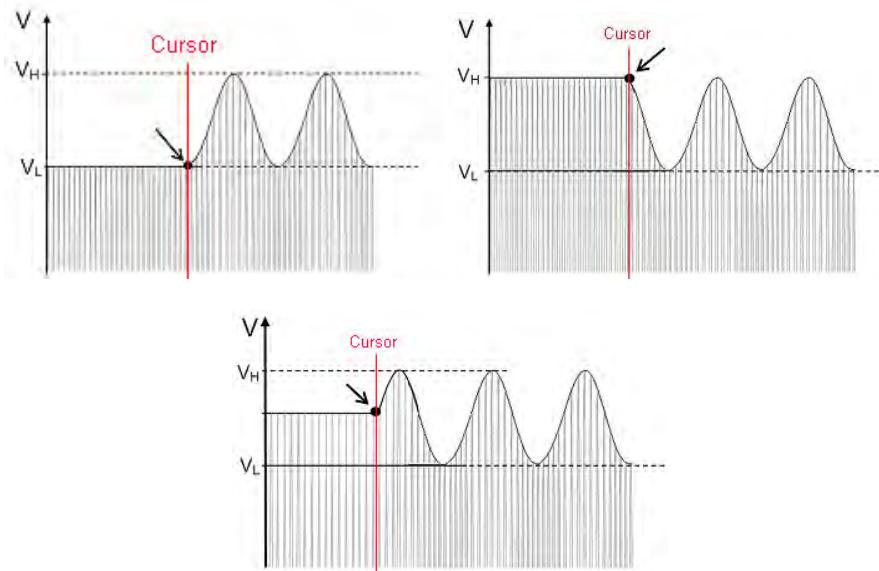


Figure E-7— Type B PICC Start

The end of the last subcarrier modulation transmitted by the PICC corresponds to the last peak of the modulation of the signal envelope. Three cases are represented in Figure E-8: end for positive modulation, negative modulation and modulation that is not purely negative or positive.

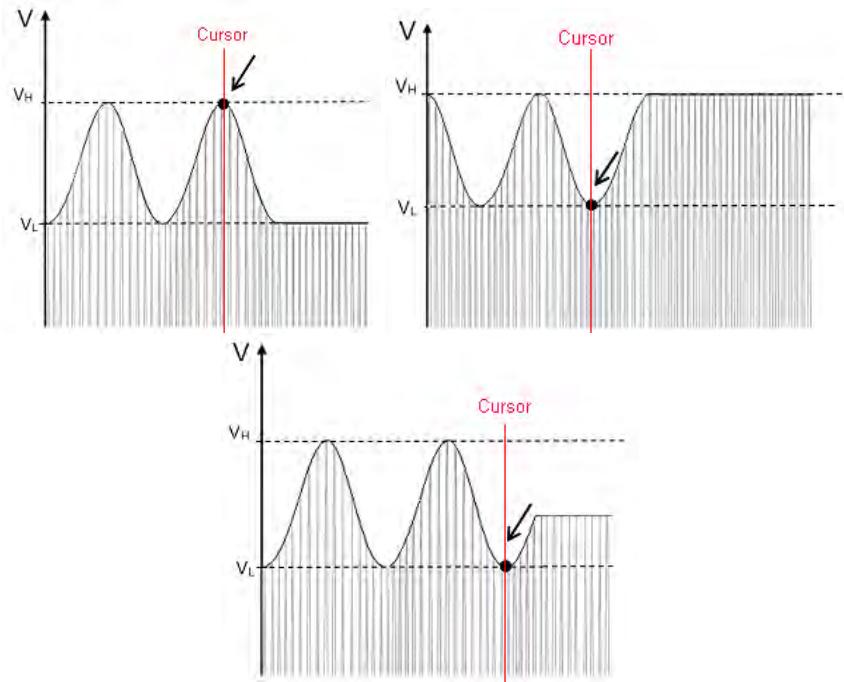


Figure E-8— Type B PICC End

As represented in Figure E-9, the nominal position of a phase shift is defined as the point where the signal envelope of the preceding subcarrier cycle passes through the local minimum (for a low phase shift) or the local maximum (for a high phase shift) plus the addition of $1/f_s$ (or $16/f_c$).

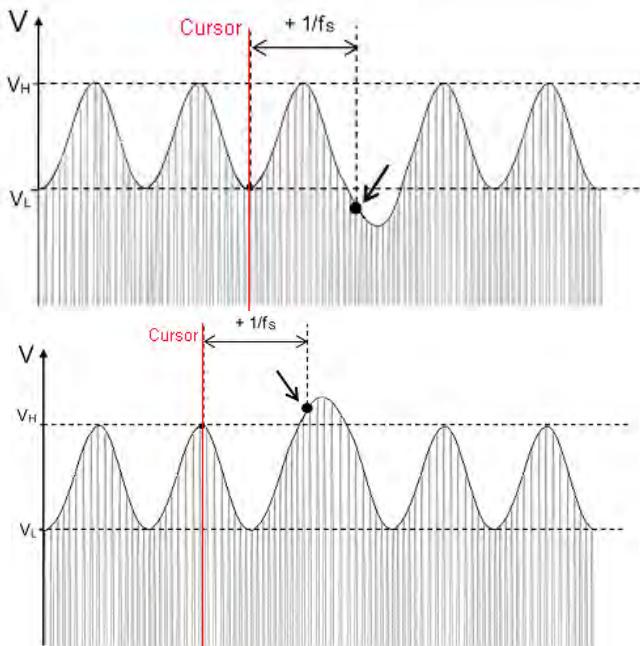


Figure E-9— Type B PICC Phase Shift

***** END OF DOCUMENT *****

EMV® Type Approval

Contactless Terminal Level 1

PCD Digital Test Bench and Test Case Requirements

Version 2.6b
December 2016

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Revision Log – Version 2.6b

The following changes have been made to the document since the publication of Version 2.5a. Some of the numbering and cross references in this version have been updated to reflect changes introduced by the published bulletins. The numbering of existing requirements did not change, unless explicitly stated otherwise.

Changes based on Specification Updates:

SB168 – Amended Timing Requirements

Version	Date	Revision Description
Version 2.6b	December 2016	<p>In Parameter Values: In table “parameters common to Type A and Type B”, add value for $t_{MIN,RETRANSMISSION}$</p> <p>In TA307: In acceptance criteria: update to “is at least $[FWT_{ACTIVATION} + t_{MIN,RETRANSMISSION}]$ and at most $[FWT_{ACTIVATION} + t_{RETRANSMISSION}]$” In the scenario: change “sent within $[FWT_{ACTIVATION} + t_{RETRANSMISSION}]$” into “sent between $[FWT_{ACTIVATION} + t_{MIN,RETRANSMISSION}]$ and $[FWT_{ACTIVATION} + t_{RETRANSMISSION}]$”</p> <p>In TA310: In acceptance criteria: update to “is at least $[FDT_{A,PICC,ANTICOLLISION} + t_{MIN,RETRANSMISSION}]$ and at most $[FDT_{A,PICC,ANTICOLLISION} + t_{RETRANSMISSION}]$” In the scenario: change “sent within $[FDT_{A,PICC,ANTICOLLISION} + t_{RETRANSMISSION}]$” into “sent between $[FDT_{A,PICC,ANTICOLLISION} + t_{MIN,RETRANSMISSION}]$ and $[FDT_{A,PICC,ANTICOLLISION} + t_{RETRANSMISSION}]$”</p> <p>In TA311: In acceptance criteria: update to “is at least $[FDT_{A,PICC,ANTICOLLISION} + t_{MIN,RETRANSMISSION}]$ and at most $[FDT_{A,PICC,ANTICOLLISION} + t_{RETRANSMISSION}]$” In the scenario: change “sent within $[FDT_{A,PICC,ANTICOLLISION} + t_{RETRANSMISSION}]$” into “sent between $[FDT_{A,PICC,ANTICOLLISION} + t_{MIN,RETRANSMISSION}]$ and $[FDT_{A,PICC,ANTICOLLISION} + t_{RETRANSMISSION}]$”</p> <p>In TA312: In acceptance criteria: update to “is at least $[FDT_{A,PICC,ANTICOLLISION} + t_{MIN,RETRANSMISSION}]$ and at most $[FDT_{A,PICC,ANTICOLLISION} + t_{RETRANSMISSION}]$” In the scenario: change “sent within $[FDT_{A,PICC,ANTICOLLISION} + t_{RETRANSMISSION}]$” into “sent between $[FDT_{A,PICC,ANTICOLLISION} + t_{MIN,RETRANSMISSION}]$ and $[FDT_{A,PICC,ANTICOLLISION} + t_{RETRANSMISSION}]$”</p> <p>In TA313: In acceptance criteria: update to “is at least $[FWT_{ACTIVATION} + t_{MIN,RETRANSMISSION}]$ and at most $[FWT_{ACTIVATION} + t_{RETRANSMISSION}]$”</p>

Version	Date	Revision Description
		<p>In the scenario: change “sent within [FWT_{ACTIVATION} + t_{RETRANSMISSION}]” into “sent between [FWT_{ACTIVATION} + t_{MIN,RETRANSMISSION}] and [FWT_{ACTIVATION} + t_{RETRANSMISSION}]”</p> <p>In TB305:</p> <p>In acceptance criteria: update to “is at least [FWT_{ACTIVATION} + t_{MIN,RETRANSMISSION}] and at most [FWT_{ACTIVATION} + t_{RETRANSMISSION}]”</p> <p>In the scenario: change “sent within [FWT_{ACTIVATION} + t_{RETRANSMISSION}]” into “sent between [FWT_{ACTIVATION} + t_{MIN,RETRANSMISSION}] and [FWT_{ACTIVATION} + t_{RETRANSMISSION}]”</p> <p>In TB311:</p> <p>In acceptance criteria: update to “is at least [(FWT_{ATQB}) + t_{MIN,RETRANSMISSION}] and at most [(FWT_{ATQB}) + t_{RETRANSMISSION}]”</p> <p>In the scenario: change “sent within [FWT_{ACTIVATION} + t_{RETRANSMISSION}]” into “sent between [(FWT_{ATQB}) + t_{MIN,RETRANSMISSION}] and [(FWT_{ATQB}) + t_{RETRANSMISSION}]”</p> <p>In TB312:</p> <p>In acceptance criteria: update to “is at least [FWT_{ACTIVATION} + t_{MIN,RETRANSMISSION}] and at most [FWT_{ACTIVATION} + t_{RETRANSMISSION}]”</p> <p>In the scenario: change “sent within [FWT_{ACTIVATION} + t_{RETRANSMISSION}]” into “sent between [FWT_{ACTIVATION} + t_{MIN,RETRANSMISSION}] and [FWT_{ACTIVATION} + t_{RETRANSMISSION}]”</p>

SB172 – EMD Handling Clarification

Version	Date	Revision Description
Version 2.6b	December 2016	<p>Creation of new Test Case TA440:</p> <p>Type A Parity error in the first 4 bytes of a sequence in response to an I-Block not indicating chaining</p> <p>Creation of new Test Case TA441:</p> <p>Type A Parity error in the first 4 bytes of a sequence in response to an I-Block indicating chaining</p> <p>Creation of new Test Case TA442:</p> <p>Type A Parity error in the first 4 bytes of a sequence in response to an R(ACK) Block</p> <p>Creation of new Test Case TA443:</p> <p>Type A Parity error in the first 4 bytes of a sequence in response to an S(WTX) Response Block</p>

Other changes (test coverage, editorial):

Version	Date	Revision Description
Version 2.6b	December 2016	<p>In TA301:</p> <p>Delete xy= 02, “no SOF” error is redundant with parity error</p>

Version	Date	Revision Description
		<p>Deletion of the last step of the scenario “The PCD returns to the initial polling phase and behaves as described in the Test Case TC001”</p> <p>In TA302:</p> <p>Delete xy= 06, “no SOF” error is redundant with parity error</p> <p>Delete xy=10, PCDs shall not examine the values returned by the PICC in bits b₈ to b₇ of ATQA</p> <p>In TA304:</p> <p>Delete xy= 03, “no SOF” error is redundant with parity error</p> <p>Delete xy= 15, Bits b₅-b₈ of byte B2 of ATQA are considered as RFU bits</p> <p>In TA305:</p> <p>Delete xy= 04, “no SOF” error is redundant with parity error</p> <p>In TA306:</p> <p>Delete xy= 03, “no SOF” error is redundant with parity error</p> <p>In TA403:</p> <p>Delete x= 4, “no SOF” error is redundant with parity error</p> <p>In TA404:</p> <p>Delete xy=12, Not compliant with EMV CL requirement 10.2.1 about the Power Level Indicator</p> <p>Legacy behavior supported by some PCDs taken into account in xy=11, depending on ICS</p> <p>In TA407:</p> <p>Delete x= 3, “no SOF” error is redundant with parity error</p> <p>In TA408:</p> <p>Delete xy=10, Not compliant with EMV CL requirement 10.2.1 about the Power Level Indicator</p> <p>Legacy behavior supported by some PCDs taken into account in xy=09, depending on ICS</p> <p>In TA410:</p> <p>Delete x= 3, “no SOF” error is redundant with parity error</p> <p>In TA411:</p> <p>Delete xy=12, Not compliant with EMV CL requirement 10.2.1 about the Power Level Indicator</p> <p>Legacy behavior supported by some PCDs taken into account in xy=11, depending on ICS</p> <p>In TA414:</p> <p>In the procedure: FWI value has been updated to 7 to be compliant with the EMV CL specification</p> <p>In TA415:</p> <p>In the procedure: FWI value has been updated to 7 to be compliant with the EMV CL specification</p> <p>In TA416:</p>

Version	Date	Revision Description
		<p>In the procedure: FWI value has been updated to 7 to be compliant with the EMV CL specification</p> <p>In TA417:</p> <p>Delete xy=08, Not compliant with EMV CL requirement 10.2.1 about the Power Level Indicator</p> <p>Legacy behavior supported by some PCDs taken into account in xy=07, depending on ICS</p> <p>In TA420:</p> <p>Deletion of the last step of the scenario “The PUT returns to the initial polling phase and behaves as described in the Test Case TC001</p> <p>In TA430:</p> <p>In the procedure: FWI value has been updated to 7 to be compliant with the EMV CL specification</p> <p>In the procedure, for x=2, FDT_{A, PICC} timing has been updated as follows: 499968 x 1/f_c + 20/f_c if the last bit transmitted by the PUT is (0)_b and 499968 x 1/f_c + 84/f_c if the last bit transmitted by the PUT is (1)_b</p> <p>In TB301:</p> <p>For xy=02, clarify residual bits</p> <p>In TB304:</p> <p>For xy=02, clarify residual bits</p> <p>In TB305:</p> <p>For x=1, clarify residual bits</p> <p>In the procedure: FWI value has been updated to 7 to be compliant with the EMV CL specification</p> <p>In TB306:</p> <p>For xy=13, clarify residual bits</p> <p>Rename 13 into 02</p> <p>In TB335:</p> <p>For y=3, clarify residual bits and EoS duration</p> <p>In the procedure: FWI value has been updated to 7 to be compliant with the EMV CL specification</p> <p>In TB403:</p> <p>For x=2 and x=3, clarify residual bits</p> <p>For x=3, clarification about EoS duration</p> <p>In TB404:</p> <p>Delete xy=12, Not compliant with EMV CL requirement 10.2.1 about the Power Level Indicator</p> <p>Legacy behavior supported by some PCDs taken into account in xy=11, depending on ICS</p> <p>In TB407:</p> <p>clarify residual bits</p> <p>In TB408:</p>

Version	Date	Revision Description
		<p>Update xy=07, WTXM value changed from 0 to 1</p> <p>Delete xy=10, Not compliant with EMV CL requirement 10.2.1 about the Power Level Indicator</p> <p>Legacy behavior supported by some PCDs taken into account in xy=09, depending on ICS</p>
		<p>In TB410:</p> <p>For x=1, clarify residual bits</p> <p>Minor editorial update in the title and in the test codification</p>
		<p>In TB411:</p> <p>Delete xy=12, Not compliant with EMV CL requirement 10.2.1 about the Power Level Indicator.</p> <p>Legacy behavior supported by some PCDs taken into account in xy=11, depending on ICS</p>
		<p>In TB414:</p> <p>For x=1, clarify residual bits</p> <p>In the procedure: FWI value has been updated to 7 to be compliant with the EMV CL specification</p>
		<p>In TB415:</p> <p>For x=1, clarify residual bits*</p> <p>In the procedure: FWI value has been updated to 7 to be compliant with the EMV CL specification</p>
		<p>In TB416:</p> <p>For x=1, clarify residual bits</p> <p>In the procedure: FWI value has been updated to 7 to be compliant with the EMV CL specification</p>
		<p>In TB417:</p> <p>Delete xy=08, Not compliant with EMV CL requirement 10.2.1 about the Power Level Indicator.</p> <p>Legacy behavior supported by some PCDs taken into account in xy=07, depending on ICS</p>
		<p>In TB430:</p> <p>For y=3, clarify residual bits and EoS duration</p> <p>In the procedure: FWI value has been updated to 7 to be compliant with the EMV CL specification</p> <p>In the procedure, for x=2, TR0 timing is updated as follows: $499968 \times 1/f_c$</p>

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1. About this Document

1.1. Introduction

The present document, 'EMV® Type Approval Contactless Terminal Level 1 PCD Digital Test Bench and Test Case Requirements Version 2.6b December 2016', describes the detailed organization and requirements of the executable tests the vendors has to comply with, to allow the digital part of the Contactless Terminal Level 1 Type Approval Testing.

The intended audience of this document includes test tool vendors, accredited test laboratories and auditors.

Describing the executable tests and the associated procedures is necessary to ensure reproducibility of the test results, even across different test laboratories.

1.2. Scope

For each individual executable test in this document, the following information is available:

- The test number,
- The objective of the test,
- The related reference specification section(s) of the Test Case,
- The conditions of the test,
- The procedure of the test,
- The acceptance criteria(s),
- The failure actions,
- The scenario of the test presented as a flow chart.

1.3. Reference Documents

EMV documents are available on the EMVCo web site:

<http://www.emvco.com/approvals.aspx> and
<http://www.emvco.com/specifications.aspx>

1.3.1. Specification Documents

Document	Version Issue date
EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification	2.6, March 2016
Specification Bulletin No. 168 — Amended Timing Requirements	First edition, May 2015
Draft Specification Bulletin No. 172 — EMD Handling Clarification	First edition, August 2015

Table 1: Specification Documents

1.3.2. Laboratory Test Documents

The test documents to be applied by EMVCo accredited laboratories when performing an EMV Contactless Terminal Type Approval Level 1 session are listed in the following document:

- **EMVCo Type Approval**
- **Contactless Terminal Level 1**
- **Laboratories Documentation**

Check the last version of this document for any update of the test documents.

1.4. Acronyms and Abbreviations

The following abbreviations and notations are used in this document:

Abbreviation	Description
ACK	Positive ACKnowledgement
ADC	Application Data Coding, Type B
AFI	Application Family Identifier, Type B
ANTICOLLISION	Collision detection command, Type A
Apf	Anticollision prefix f, Type B
ASK	Amplitude Shift Keying
ATQA	Answer To reQuest, Type A
ATQB	Answer To reQuest, Type B
ATS	Answer To Select, Type A
ATTRIB	Selection command, Type B
BCC	Check byte, Type A
BPSK	Binary Phase Shift Keying
CID	Card IDentifier
CLn	Cascade Level n, Type A
CT	Cascade Tag, Type A
CRC_A	Cyclic Redundancy Check error detection code for Type A
CRC_B	Cyclic Redundancy Check error detection code for Type B
CUT	Card Under Test. When the Instance Under Test as defined in ISO 9646 is a EMVCo Proximity IC Card
DR	Divisor Receive (PCD, PICC)
DRI	Divisor Receive Integer (PCD, PICC)
DS	Divisor Send (PICC, PCD)
DSI	Divisor Send Integer (PICC, PCD)
DUT	Device Under Test
EGT	Extra Guard Time, Type B
EMD	ElectroMagnetic Disturbance (= 'noise')
EoF	End of Frame
EoS	End of Sequence
etu	Elementary time unit (= 'bit duration')
FDT	Frame Delay Time
f _c	Carrier frequency
FO	Frame Option, Type B

Abbreviation	Description
f_s	Subcarrier frequency
FSC	Frame Size for proximity Card
FSCI	Frame Size for proximity Card Integer
FSD	Frame Size for proximity coupling Device
FSDI	Frame Size for proximity coupling Device Integer
FWI	Frame Waiting time Integer
FWT	Frame Waiting Time
HLTA	Halt Command, Type A
HLTB	Halt Command, Type B
INF	INFormation field
ISO	International Organization for Standardization
LSB	Least Significant Bit
LT	Lower Tester.
MBL	Maximum Buffer Length
MBLI	Maximum Buffer Length Integer
MSB	Most Significant Bit
NAD	Node ADdress
NAK	Negative Acknowledgment
NRZ-L	Non-Return to Zero, (L for Level)
OOK	On-Off Keying
OSI	Open Systems Interconnection
PCB	Protocol Control Byte
PCD	Proximity Coupling Device (reader)
PI	Protocol Information field of the ATQB, Type B
PICC	Proximity IC Card
PPS	Protocol and Parameter Selection, Type A
PUPI	Pseudo-Unique PICC Identifier, Type B
PUT	PCD Under Test. When the Instance Under Test as defined in ISO 9646 is an EMV Contactless Proximity Coupling Device (reader)
RATS	Request for Answer To Select
REQA	REQuest command, Type A
REQB	REQuest command, Type B
RF	Radio Frequency
RFU	Reserved for Future Use
SAK	Select AcKnowledge, Type A

Abbreviation	Description
SELECT	SELECTION command, Type A
SFGT	Minimum Frame Delay Time after ATS (for Type A) or ATTRIB Response (for Type B)
SoF	Start of Frame
SoS	Start of Sequence
UID	Unique IDentifier, Type A
uidn	Byte number n of Unique Identifier
UT	Upper Tester
WTX	Waiting Time eXtension
WTXM	Waiting Time eXtension Multiplier
WUPA	Wake UP command, Type A
WUPB	Wake UP command, Type B

Table 2: List of Abbreviations

2. Generic Information about the Tests

2.1. Default Environmental Test Conditions

The following environmental conditions shall be used for all the tests described in the present document:

- The Reference PICC Antenna shall be placed in the EMV Contactless operating volume of the PCD under Test (as defined in section “Operating Volume” of the EMV Contactless specification) so that the transaction can be performed correctly (some manual positioning should be performed to obtain the best test results).
- The external perturbations shall be suppressed: no metal objects or other perturbing elements in a volume of 30 centimeters around the Test System and no other antennas (contactless terminals, cell phones ...) in a volume of 1 meter around the Test System.

2.2. Default Protocol Test Conditions

Unless specified in the test description (i.e. for exception processing tests), the blocks sent by the LT shall never contain a CID or a NAD field as it is not supported by an EMV Contactless terminal.

Unless specified in the test description (i.e. to perform a PICC Reset), the PUT shall never stop sending the carrier during an EMV Contactless transaction.

Unless specified in the test description, the LT shall apply the default EMV Contactless timings and the default EMV Contactless parameter values (as defined in the present section).

2.3. Test Tool Requirements

When, for Type Approval, a Test Tool is used as a LT, the following requirements should be applied:

- Any executed subcase shall generate traces, logs and a test report.
- The generation of traces, logs and test reports shall indicate whether the acceptance criterias have been met. All acceptance criterias and related values shall be visible in the traces, logs or test reports (e.g. for a timing measurement, the timing measured by the Test Tool shall be present, so shall be the tolerance used by the Test Tool and the expected value or expected range of values for this timing).
- Any applied timing shall be visible in the traces, logs or test reports.

2.4. Default Timings

For the time parameters given below, when a test description does not indicate a specific value which has to be used to perform the test, then the default time value shall be used by the Lower Tester to send sequences (i.e. the LT shall reply to the PUT with delays equal to the default value).

The concerned parameters and their default values are as follows:

In Type A:

- After WUPA, ANTICOLLISION and SELECT commands:
 - $FDT_{A,PICC} = (1152 \times 1/f_c + 20/f_c) [-1/f_c; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PCD is (0)_b
 - $FDT_{A,PICC} = (1152 \times 1/f_c + 84/f_c) [-1/f_c; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PCD is (1)_b
- After all other commands and after all Blocks:
 - $FDT_{A,PICC} = (3200 \times 1/f_c + 20/f_c) [-1/f_c; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PCD is (0)_b
 - $FDT_{A,PICC} = (3200 \times 1/f_c + 84/f_c) [-1/f_c; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PCD is (1)_b

In Type B:

- $FDT_{B,PICC} = 3840 \times 1/f_c$ after all commands and all Blocks ($TR_0 = 1920 \times 1/f_c$ with no subcarrier generated by the LT and $TR_1 = 1920 \times 1/f_c$ with subcarrier with no phase transition generated by the LT)
- $EGT_{PICC} = 128/f_c$ between two consecutive characters within any sequence.
- Start of Sequence (SoS) = $1344 \times 1/f_c$ of logical state low (i.e. a subcarrier phase transition followed by the subcarrier with phase ϕ_0+180°) followed by $320 \times 1/f_c$ of logical state high (i.e. a subcarrier phase transition followed by the subcarrier with phase ϕ_0)
- End of Sequence (EoS) = $1344 \times 1/f_c$ of logical state low (i.e. a subcarrier phase transition followed by the subcarrier with phase ϕ_0+180°) followed by a logical state transition (i.e. a subcarrier phase transition to phase ϕ_0) and $136 \times 1/f_c$ with subcarrier on (then the LT turns the subcarrier off)

Notation: in the EMV Contactless specification, the Frame Delay Time (FDT) is defined as the delay between the end of a sequence sent by the PUT and the beginning of a sequence sent by the LT.

2.5. Definitions for Sequences Timings Application and Measurement

When a Test Case asks for the measurement or the application of a delay between two consecutive sequences sent in the same direction or in opposite directions, the delay shall be measured or applied using the following definitions:

- Beginning of a sequence sent by a Type A PICC: the start (i.e. the first modulation transmitted) of the Start of Frame (SoF) of the PICC sequence.
- Beginning of a sequence sent by a Type A PCD: the start of the lower level within the Start of Frame (SoF) of the PCD sequence.
- Beginning of a sequence sent by a Type B PICC: the start of the Start of Sequence (SoS) of the PICC sequence.
- Beginning of a sequence sent by Type B PCD: the start of the Start of Sequence (SoS) of the PCD sequence.
- End of a sequence sent by a Type A PICC: the last modulation transmitted in the PICC sequence.
- End of a sequence sent by a Type A PCD: the rising edge of the last lower level of the PCD sequence (within the last data bit sent by the PCD if this last data bit is a Logic "1" or within the End of Frame if the last data bit sent by the PCD is a Logic "0").

- End of a sequence sent by a Type B PICC: the **start** of the End of Sequence (EoS) of the PICC sequence.
- End of a sequence sent by a Type B PCD: the end of the End of Sequence (EoS) of the PCD sequence.

2.6. Scenario Notations during Half-Duplex Protocol

Notation	Description
I(0) _x ['HH ... HH']	Not chained I-Block or last I-Block of a chain with block number x and containing the hexadecimal data bytes 'HH ... HH' (i.e. transmitted APDUs)
I(1) _x ['HH ... HH']	Chained I-Block (except the last I-Block of a chain) with block number x and containing the hexadecimal data bytes 'HH ... HH' (i.e. transmitted APDUs)
R(ACK) _x	R-Block indicating a positive acknowledgment with block number x
R(NAK) _x	R-Block indicating a negative acknowledgment with block number x
S(...)	S-Block

2.7. Types of Frames in the Scenarios

In the present document, when describing the EMV Contactless transactions within the test scenarios, the following rules apply:

In Type A tests, if nothing is indicated, the bytes are transported within a Type A standard frame with the 2 bytes of CRC_A (i.e. a valid CRC_A is automatically added after the bytes by the Test Tool).

In Type A tests, if “(*short frame*)” is indicated, the bytes are transported within a Type A short frame.

In Type A tests, if “(*no CRC_A*)” is indicated, the bytes are transported within a Type A standard frame with no CRC_A bytes.

In Type A tests, if “(*Type B frame*)” is indicated, the bytes are transported within a Type B frame with 2 bytes of CRC_B (i.e. a valid CRC_B is automatically added after the bytes by the Test Tool).

In Type B tests, if nothing is indicated, the bytes are transported within Type B frames with 2 bytes of CRC_B (i.e. a valid CRC_B is automatically added after the bytes by the Test Tool).

In Type B tests, if “(*no CRC_B*)” is indicated, the bytes are transported within a Type B frame with no CRC_B bytes (exception processing tests).

In Type B tests, if “(*Type A short frame*)” is indicated, the bytes are transported within a Type A short frame (WUPA command sent during collision detection).

2.8. Notational Conventions

The following notations apply:

'00' to 'FF' or "00...00" to "FF...FF": hexadecimal values (sometimes the hexadecimal values are indicated between parenthesis and followed by a lower case "h").

(0)_b or ("1001")_b: binary notation. Values expressed in binary form are followed by a lower case "b".

u: any value (e.g. byte A = ("1u11 0101")_b means that b7 of byte A can take any value).

UID Size 1, 2 or 3: refers to the single, double or triple size Type A UID as defined in the EMV specification.

2.9. Test References

The tests described in the following sections are referenced this way:

Test codification:

T	-	-	-	-	.	-	-
-	a	b	c		.	d	

a: Frame Type:

- A = Type A tests
- B = Type B tests
- C = Common tests to Type A and Type B (i.e. Polling Tests)

b: Test Type:

- 0 = Basic tests
- 1 = Installation Tests
- 2 = Half Duplex Block Protocol Exchanges and Removal Tests
- 3 = Installation with Exception Processing Tests
- 4 = Block Protocol and Removal with Exception Processing Tests

c: Test Number (within the Test Type):

- From 00 to 99

d: Optional Subcase Reference xy:

- From 0 to 99

e.g. TA223.2 represents the Subcase 2 of the Test number 23 within the tests concerning the Half Duplex Block Protocol Exchanges in Type A.

2.10. Test Bench

A Test Platform (on the PC) and a Protocol Contactless Card Simulator are used for conducting the tests (Lower Tester):

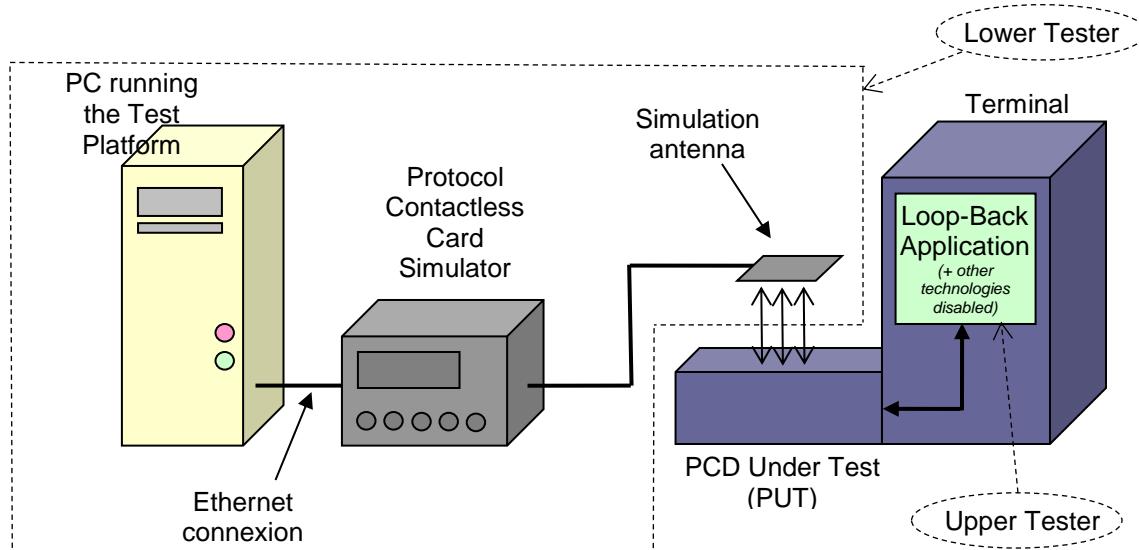


Figure 1: Test Bench

2.11. Loop-Back application and End Of Test Command

The Test Bench which is used to implement the EMV Contactless Terminal Type Approval tests is based on the use of the Loop-Back Application (and a function to disable the optional polling for other technologies than EMV Contactless Type A and B, if needed) in the terminal containing the PCD Under Test (Upper Tester).

The PCD Under Test shall allow for the Loop-Back application to be used during the Level 1 digital tests. This test application becomes active when the PCD Under Test reports to the Upper Tester that a (single) card is present. When it becomes active, it sends a defined first Command APDU and then any received Response APDU is derived into the next Command APDU.

The Lower Tester can indicate the end of a test scenario to the PCD Under Test by sending an I-Block containing a specific command referred to as the End Of Test command. When the terminal receives this command, it shall immediately initiate the removal procedure by performing a PICC Reset. The End Of Test command is a specific Response APDU sent by the Lower Tester within an I-Block (Response APDU with the INS field equal to '70').

In the scenarios of this document, whenever, there is a step:

1	PUT ↳ I(0) ₀ [“EOT Command” + ‘90 00’]	↳ LT	End Of Test command
---	---	------	---------------------

Table 3: End Of Test command step

It shall be understood as:

1	PUT ↳ I(0) ₀ [‘00 70 04 04 00’ (EOT Command) + ‘90 00’]	↳ LT	End Of Test command with Removal procedure
---	--	------	--

Table 4: End Of Test command with Removal procedure step

Indicating that the Lower Tester shall send an I-Block with an R-APDU containing ‘00 70 04 04 00’ (EOT Command) + ‘90 00’ i.e. an EOT Command requesting to the Loop-Back application to initiate the Removal Procedure (2nd byte of the R-APDU set to ‘70’).

The Loop-Back application and the End of Test command are detailed in the ‘Device Test Environment’ vendor form provided by EMVCo.

2.12. Parameter Values

This section defines the parameter values to be applied or observed during the PCD digital tests unless identified in the test descriptions otherwise.

The timing values in the table below are as given in the EMV Contactless specification and do not take the test margins induced by the tool inaccuracy into account.

When a timing value is applied by the test tool (e.g. $FDT_{A,PICC}$ or $FDT_{B,PICC}$), the test implementation should be as close as possible to the timing given in the table and the following rules shall be respected by the test tool:

- In the case where a minimum timing value shall be supported by the PCD under test, the applied timing value shall never be lower than the specification value given in the table.
- In the case where a maximum timing value shall be supported by the PCD under test, the applied timing value shall never be higher than the specification value given in the table.

When a timing value is measured during a test, the tolerances of the test tool shall be used. The following is the maximum tolerance p accepted for a test tool:

- If T is defined in ' $1/f_c$ ' and $T \leq 12800 \times 1/f_c$ then $p = 12.8 \times 1/f_c$
- If T is defined in ' $1/f_c$ ' and $12800 < T \leq 128000 \times 1/f_c$ then $p = 64 \times 1/f_c$
- If T is defined in ' $1/f_c$ ' and $128000 < T \leq 1280000 \times 1/f_c$ then $p = 128 \times 1/f_c$
- If T is defined in ' $1/f_c$ ' and $T > 1280000 \times 1/f_c$ then $p = 0.001 * T$
- If T is defined in 'ms' then $p = 0.001 * T$ (e.g. $T = 10 \text{ ms} \Rightarrow p = 10 \mu\text{s}$)

Notation: T is the timing which shall be measured within a Test Case and p is the time precision needed for this Test Cases.

Parameters common to Type A and Type B:

Parameter name	Parameter value	Comments
$t_{P,MIN}$	5.1 ms	
$t_{P,MAX}$	10 ms	
$t_{RESET,MIN}$	5.1 ms	
$t_{RESET,MAX}$	10 ms	
$t_{MIN,RETRANSMISSION}$	3 ms	
$t_{RETRANSMISSION}$	33 ms	
$t_{RESETDELAY}$	33 ms	
$t_{RECOVERY}$	$1280/f_c$	
$FWT + \Delta FWT$	$n \times 128/f_c = (4096 \times 2^{FWI} + 49152) \times 1/f_c$	Detailed in the test description
$(FWT + \Delta FWT)_{DEFAULT}$	$114688 \times 1/f_c$	Corresponding to the basic installation: FWI = 4
FWT_{MAX}	$67108864 \times 1/f_c$	Corresponds to FWI _{MAX} = 14

Parameter name	Parameter value	Comments
FSC	n bytes	Detailed in the test description
FSD	256 bytes	

Table 5: Parameter values Common Type A and Type B

Parameters specific to Type A:

Parameter name	Parameter value	Comments
$FDT_{A,PICC,ANTICOLLISION}$ and $FDT_{A,PICC,MIN}$	$9 \times 128/f_c + 20/f_c [-1/f_c ; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PCD is $(0)_b$ $9 \times 128/f_c + 84/f_c [-1/f_c ; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PCD is $(1)_b$	
$FDT_{A,PICC,MAX}$	$n \times 128/f_c + 20/f_c [-1/f_c ; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PCD is $(0)_b$ $n \times 128/f_c + 84/f_c [-1/f_c ; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PCD is $(1)_b$	$(n+1) \times 128/f_c = FWT + \Delta FWT$ Detailed in the test description
$FDT_{A,PICC,ACTIV,MAX}$	$559 \times 128/f_c + 20/f_c [-1/f_c ; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PCD is $(0)_b$ $559 \times 128/f_c + 84/f_c [-1/f_c ; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PCD is $(1)_b$	
$FDT_{A,PCD,MIN}$	$6780 \times 1/f_c$	
$FWT_{ACTIVATION}$	$71680 \times 1/f_c$	
$(SFGT + \Delta SFGT)$	$[(256 \times 16/f_c) \times 2^{SFGI}] + [384/f_c \times 2^{SFGI}]$	$SFGI \leq SFGI_{MAX} = 14$ Detailed in the test description

Table 6: Parameter values Specific Type A

Parameters specific to Type B:

Parameter name	Parameter value	Comments
$TR0_{MIN}$	$1008 \times 1/f_c$	With no subcarrier generated by the LT
$TR0_{MAX,ATQB}$	$6416 \times 1/f_c$	
$TR1_{MIN}$	$1264 \times 1/f_c$	Subcarrier with no phase transition generated by the LT

Parameter name	Parameter value	Comments
$TR1_{PUTMIN}$	Minimum value of TR1 supported by pre-test TB000 and used to initialize some subcases in the tests TB340 and TB435	Determined by performing the
$TR1_{MAX}$	$3216 \times 1/f_c$	Subcarrier with no phase transition generated by the LT
$FDT_{B,PICC,MIN}$	$2272 \times 1/f_c$	$= TR0_{MIN} + TR1_{MIN}$ $= (1008 + 1264) \times 1/f_c$
$FDT_{B,PICC,MAX}$	$n \times 128/f_c = FWT + \Delta FWT$	Detailed in the test description
FWT_{ATQB}	$7680 \times 1/f_c$	
$FDT_{B,PCD,MIN}$	$6780 \times 1/f_c$	
$EGT_{PICC,MIN}$ and $EGT_{PCD,MIN}$	$0 \times 1/f_c$	
$EGT_{PICC,MAX}$	$272 \times 1/f_c$	
$EGT_{PCD,MAX}$	$752 \times 1/f_c$	
$t_{PICC,S,1,MIN}$	$1264 \times 1/f_c$	With subcarrier with phase ϕ_0
$t_{PICC,S,1,MAX}$	$1424 \times 1/f_c$	$+180^\circ$
$t_{PICC,S,2,MIN}$	$240 \times 1/f_c$	With subcarrier with phase ϕ_0
$t_{PICC,S,2,MAX}$	$400 \times 1/f_c$	
$t_{PICC,E,MIN}$	$1264 \times 1/f_c$	With subcarrier with phase ϕ_0
$t_{PICC,E,MAX}$	$1424 \times 1/f_c$	$+180^\circ$
$t_{FSOFF,MIN}$	$0 \times 1/f_c$	With subcarrier with phase ϕ_0
$t_{FSOFF,MAX}$	$272 \times 1/f_c$	(optional)
$t_{PCD,S,1,MIN}$	$1280 \times 1/f_c$	With carrier low (modulation applied)
$t_{PCD,S,1,MAX}$	$1416 \times 1/f_c$	
$t_{PCD,S,2,MIN}$	$248 \times 1/f_c$	With carrier high (no modulation applied)
$t_{PCD,S,2,MAX}$	$392 \times 1/f_c$	
$t_{PCD,E,MIN}$	$1280 \times 1/f_c$	With carrier low (modulation applied)
$t_{PCD,E,MAX}$	$1416 \times 1/f_c$	

Table 7: Parameter values Specific Type B

3. POLLING TEST CASES

3.1. Polling Observation and Timings Verification [TC001]

Test codification:

TC001

Test objective:

To ensure that the PCD respects the frame format, the timings and the series of commands during polling.

References Requirements:

4.2.1.1, 9.1.2.2, 9.1.2.3, 9.2.1.1, 9.2.1.2, 9.2.1.3, 9.2.1.4, 9.2.1.5

Conditions:

Respect of the Generic Information about the Tests (see section 2).

Procedure:

The LT shall observe the series of commands generated during polling by the PUT and verify its conformance with the following scenario (the observation may start on any step of the scenario).

The LT measures the time during which the PUT sends the carrier before every WUPA and WUPB command sent by the PUT.

Acceptance criteria:

The PUT performs the EMV Contactless polling loop (at least 10 repetitions of the following scenario shall be observed).

The polling loop starts with the mandatory WUPA command (first poll command; Type A short frame format) followed by the mandatory WUPB command (second poll command; Type B frame format). Then, the PUT restarts the polling loop (observed at least 10 consecutive times).

The PUT sends the carrier during at least $t_{P,MIN}$ and at most $t_{P,MAX}$ before each WUPA and WUPB command.

The PUT uses the default bit rate of $f_c/128$ to send the EMV Contactless polling commands (~ 106 kbit/s as $f_c = 13,56$ MHz).

Failure action:

Stop further testing.

Scenario:

Step	Exchanges		Comments
→ 1	PUT ▶ The PUT sends the carrier during at least $t_{P,MIN}$ and at most $t_{P,MAX}$	↔ LT	The LT stays mute
	PUT ▶ '52' (Type A short frame)	↔ LT	WUPA
	PUT ▶ The PUT sends the carrier during at least $t_{P,MIN}$ and at most $t_{P,MAX}$	↔ LT	The LT stays mute
	PUT ▶ '05 00 08' (Type B frame)	↔ LT	WUPB
This series of commands (from step 1 to step 4) is repeated as long as the terminal is powered-on			

Scenario 1: Polling Observation and Timings Verification

3.2. Polling Loop for PCD that supports Other Technologies [TC002]

Test codification:

TC002

Test objective:

To ensure that the PCD does not send any WUPA or WUPB command as per EMV CL and REQA or REQB command as per ISO during polling for other technologies

References Requirements:

9.2.1.6, 9.2.1.7

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test is performed only if the PCD supports other technologies (see ICS).

The polling for other technologies shall not be deactivated in the DTE.

Procedure:

The LT shall capture the signal until it has captured at least 2 WUPA and 2 WUPB commands.

Acceptance criteria:

When the PUT sends a WUPA command as defined by the EMV CL specification (i.e. '52'):

- the WUPA command is preceded by
 - a RESET of at least $t_{RESET,MIN}$ to at most $t_{RESET,MAX}$ and
 - carrier ON with no modulation for at least $t_{P,MIN}$ to at most $t_{P,MAX}$
- the WUPA command is followed by
 - carrier ON with no modulation for at least $t_{P,MIN}$ to at most $t_{P,MAX}$ and
 - a WUPB command as defined by the EMV CL specification (i.e.'05 00 08')

When the PUT sends a WUPB command as defined by the EMV CL specification (i.e. '05 00 80'):

- the WUPB command is preceded by
 - a WUPA command as defined by the EMV CL specification (i.e. '52') and
 - carrier ON with no modulation for at least $t_{P,MIN}$ to at most $t_{P,MAX}$
- the WUPB command is followed by:
 - carrier ON with no modulation for at least F_{WTATQB}

When the PUT sends a sequence with the Type A short frame format, if the sequence does not contain a WUPA command as defined by the EMV CL specification (i.e. '52'), then the sequence does not contain a REQA as defined by the ISO specification (i.e. '26' and '35').

When the PUT sends a sequence with the Type B frame format, if the sequence does not contain a WUPB command as defined by the EMV CL specification (i.e. '05 00 08'), then the sequence does not contain a REQB as defined by the ISO specification (i.e. '05 XX'+
 $000x0xxx_b$ with X or x being any value).

Failure action:

Proceed with Type A and Type B tests.

Scenario:

Step	Exchanges		Comments
1	PUT II	The PUT keeps the carrier off during at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$	II LT PICC Reset
2	PUT ▶	The PUT sends the carrier during at least $t_{P,MIN}$ and at most $t_{P,MAX}$	II LT The LT stays mute
3	PUT ▶	'52' (Type A short frame)	II LT WUPA/REQA
4	PUT ▶	The PUT sends the carrier during at least $t_{P,MIN}$ and at most $t_{P,MAX}$	II LT The LT stays mute
5	PUT ▶	'05 00 08' (Type B frame)	II LT WUPB/REQB
6	PUT ▶	The PUT sends the carrier during at least FWT_{ATQB}	II LT The LT stays mute
7		Any Reset and Other Technology(ies) Polling command(s)	Anything
8	PUT II	The PUT keeps the carrier off during at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$	II LT PICC Reset
9	PUT ▶	The PUT sends the carrier during at least $t_{P,MIN}$ and at most $t_{P,MAX}$	II LT The LT stays mute
10	PUT ▶	'52' (Type A short frame)	II LT WUPA/REQA
11	PUT ▶	The PUT sends the carrier during at least $t_{P,MIN}$ and at most $t_{P,MAX}$	II LT The LT stays mute
12	PUT ▶	'05 00 08' (Type B frame)	II LT WUPB/REQB
13	PUT ▶	The PUT sends the carrier during at least FWT_{ATQB}	II LT The LT stays mute

Scenario 2: Polling Loop for PCD that supports Other Technologies

4. Type A TEST CASES

4.1. Basic Type A Exchange (single size UID) and timings measurement [TA001]

Test codification:

TA001

Test objective:

To ensure that the PCD respects the frame format, the timings and the series of commands during a basic exchange (installation and block protocol) with a Type A PICC with a Single size UID.

References Requirements:

4.2.1.1, 4.6.1.1, 4.7.1.1, 4.7.1.2, 4.7.1.3, 4.7.3.3, 4.8.2.1, 5.2.1.1, 5.2.1.2, 5.6.2.1, 5.7.1.1, 5.7.1.3, 5.7.2.8, 9.1.2.1, 9.1.2.3, 9.2.1.2, 9.2.1.3, 9.2.1.4, 9.3.1.1, 9.3.1.2, 9.3.2.1, 9.3.2.2, 9.3.2.3, 9.4.1.1, 9.4.1.2, 10.3.1.1, 10.3.1.3, 10.3.3.1, 10.3.3.3, 10.3.4.1

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

Until the End Of Test command, when a sequence sent by the LT is followed by a sequence sent by the PUT, the LT measures the delay between the end of the sequence sent by the LT and the beginning of the sequence replied by the PUT.

Until the End Of Test command, when two consecutive sequences are sent by the PUT, the LT measures the delay between the end of the first sequence sent by the PUT and the beginning of the second sequence sent by the PUT.

Until the End Of Test command, the LT observes the format and coding of the sequences transmitted by the PUT (Start of Frame and End of Sequence included).

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to all the sequences sent by the LT).

The PUT uses the default bit rate of $f_d/128$ during installation (~ 106 kbit/s as $f_c = 13.56$ MHz).

The PUT continues the EMV Contactless session using the default bit rate.

The PUT uses the Type A short frame format to transmit the WUPA command, the Type B frame format to transmit the WUPB command and the Type A standard frame format to transmit all other commands and blocks.

The PUT sends the WUPA and the ANTICOLLISION CL1 commands in sequences not containing any CRC_A bytes (data bytes only).

The PUT sends the SELECT, HLTA and RATS commands and the blocks in sequences ending with two CRC_A bytes calculated as defined in ISO/IEC 13239 specification (initial register value = '6363').

The Type A short frames sent by the PUT are composed of a Start of Frame (SoF = Logic "0") followed by 7 data bits and followed by an End of Frame (EoF = Logic "0"). The Type A standard frames sent by the PUT are composed of a Start of Frame (SoF = Logic"0") followed by the data bits grouped in bytes with an odd parity bit at the end of each byte (= 8 data bits + 1 parity bit) and followed by an End of Frame (EoF = Logic"0").

The Type B frames sent by the PUT are composed of the data bits grouped in characters. A Type B character is composed of a start bit (= Logic "0"), a byte (= 8 data bits) and a stop bit (= Logic "1").

The bytes are transmitted most significant byte first and the bits are transmitted least significant bit first.

The Type A frames sent by the PUT are contained in sequences ending with an End of Sequence (EoS) i.e. a full bit duration with no modulation applied.

The Type B frames sent by the PUT are contained in sequences starting with a Start of Sequence (SoS) i.e. $t_{PCD,S,1,MIN}$ to $t_{PCD,S,1,MAX}$ with carrier low (modulation applied) followed by $t_{PCD,S,2,MIN}$ to $t_{PCD,S,2,MAX}$ with carrier high (no modulation applied), and ending with an End of Sequence (EoS) i.e. $t_{PCD,E,MIN}$ to $t_{PCD,E,MAX}$ with carrier low (modulation applied) followed by a logical state transition (= transition to carrier high).

The delay between the end of a sequence sent by the LT and the beginning of the sequence replied by the PUT is at least $FDT_{A,PCD,MIN}$ during installation and block protocol.

The delay between the end of the HLTA command sequence and the beginning of the WUPB command sequence is at least $t_{P,MIN}$ and at most $t_{P,MAX}$ with carrier on.

The delay between the end of the WUPB command sequence and the beginning of the next WUPA command sequence is at least $t_{P,MIN}$ and at most $t_{P,MAX}$ with carrier on.

The PUT sends a RATS command having the value 'E0 80'.

The Block number of the first I-Block sent by the PCD is equal to 0.

The Blocks sent by the PCD contain no NAD or CID.

Failure action:

Proceed with Type B tests.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00' sent after FDT_{A,PCD,MIN}	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame) sent between t _{P,MIN} and t _{P,MAX}	▶ LT WUPB
5	PUT ▶ '52' (short frame) sent between t _{P,MIN} and t _{P,MAX}	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A) sent after FDT_{A,PCD,MIN}	▶ LT ANTICOLLISION CL1
8	PUT ◀ '27 E9 3B 11' + 'E4' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '27 E9 3B 11' + 'E4' sent after FDT_{A,PCD,MIN}	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80' sent after FDT_{A,PCD,MIN}	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] sent after FDT_{A,PCD,MIN}	▶ LT Select PPSE
14	PUT ◀ I(0)₀ ['00 B2 01 04 00' + '90 00']	◀ LT
15	PUT ▶ I(0)₁ ['00 B2 01 04 00'] sent after FDT_{A,PCD,MIN}	▶ LT Loop-back
16	PUT ◀ I(0)₁ ['00 B2 02 04 00' + '90 00']	◀ LT
17	PUT ▶ I(0)₀ ['00 B2 02 04 00'] sent after FDT_{A,PCD,MIN}	▶ LT Loop-back
18	PUT ◀ I(0)₀ ['00 A4 04 00 17' + '01 02 ... 17' + '00' + '90 00']	◀ LT
19	PUT ▶ I(0)₁ ['00 A4 04 00 17' + '01 02 ... 17' + '00'] sent after FDT_{A,PCD,MIN}	▶ LT Loop-back (32 bytes frame)
20	PUT ◀ I(0)₁ ['00 B2 03 04 00' + '90 00']	◀ LT
21	PUT ▶ I(0)₀ ['00 B2 03 04 00'] sent after FDT_{A,PCD,MIN}	▶ LT Loop-back
22	PUT ◀ I(0)₀ ['00 B2 04 04 00' + '90 00']	◀ LT
23	PUT ▶ I(0)₁ ['00 B2 04 04 00'] sent after FDT_{A,PCD,MIN}	▶ LT Loop-back
24	PUT ◀ I(0)₁ ['00 A4 04 00 17' + '18 19 ... 2E' + '00' + '90 00']	◀ LT
25	PUT ▶ I(0)₀ ['00 A4 04 00 17' + '18 19 ... 2E' + '00'] sent after FDT_{A,PCD,MIN}	▶ LT Loop-back (32 bytes frame)
26	PUT ◀ I(0)₀ ["EOT Command" + '90 00']	◀ LT End Of Test command
27	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset

Step	Exchanges	Comments
28	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
29	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
30	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 3: Basic Type A Exchange (single size UID) and timings measurement

4.2. Type A Correct Removal [TA002]

Test codification:

TA002

Test objective:

To ensure that the PCD respects the timings and the series of commands during the removal of a Type A PICC.

References Requirements:

4.8.2.1, 9.5.1.1, 9.5.1.2, 9.5.1.3, 9.5.1.4

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

After the end of the 'End Of Test command' sequence, the LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

The LT measures the delay during which the PUT sends the unmodulated carrier between the end of the PICC Reset and the beginning of the first WUPA command sequence of the removal procedure.

After the PICC Reset, when a sequence sent by the LT is followed by a sequence sent by the PUT, the LT measures the delay between the end of the sequence sent by the LT and the beginning of the sequence replied by the PUT.

After the PICC Reset, when two consecutive sequences are sent by the PUT, the LT measures the delay between the end of the first sequence sent by the PUT and the beginning of the second sequence sent by the PUT.

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (upon receipt of the ‘End Of Test command’, the PUT performs a PICC Reset and ensures that the PICC is removed from the field).

The time during which the PUT stops the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$.

After the PICC Reset, the delay between the end of a sequence sent by the LT and the beginning of the sequence replied by the PUT is at least $FDT_{A,PCD,MIN}$ during removal.

After the PICC Reset, the delay between the end of the HLTA command sequence and the beginning of the WUPA command sequence is at least $t_{P,MIN}$ and at most $t_{P,MAX}$ with carrier on.

After the PICC Reset, when two consecutive WUPA commands are sent by the PUT, the delay between the end of the first WUPA command sequence and the beginning of the second WUPA command sequence is at most $[FDT_{A,PICC,ANTICOLLISION} + t_{RETRANSMISSION}]$.

Failure action:

Proceed with Type B tests.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ ‘52’ (short frame) ▶ LT	WUPA during polling
2	PUT ◀ ‘01 00’ (no CRC_A) ◀ LT	ATQA
3	PUT ▶ ‘50 00’ ▶ LT	HLTA
4	PUT ▶ ‘05 00 08’ (Type B frame) ▶ LT	WUPB
5	PUT ▶ ‘52’ (short frame) ▶ LT	WUPA
6	PUT ◀ ‘01 00’ (no CRC_A) ◀ LT	ATQA
7	PUT ▶ ‘93 20’ (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ◀ ‘11 6F 58 95’ + ‘B3’ (no CRC_A) ◀ LT	UID
9	PUT ▶ ‘93 70’ + ‘11 6F 58 95’ + ‘B3’ ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ◀ ‘20’ ◀ LT	SAK
11	PUT ▶ ‘E0 80’ ▶ LT	RATS
12	PUT ◀ ATS ◀ LT	ATS
13	PUT ▶ I(0)0 [‘00 A4 04 00 0E’ + “2PAY.SYS.DDF01” + ‘00’] ▶ LT	Select PPSE
14	PUT ◀ I(0)0 [“EOT Command” + ‘90 00’] ◀ LT	End Of Test command
15	PUT II The PUT keeps the carrier off during at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$ II LT	PICC Reset
16	PUT ▶ ‘52’ (short frame) sent between $t_{P,MIN}$ and $t_{P,MAX}$ ▶ LT	WUPA to poll for the PICC
17	PUT ◀ ‘01 00’ (no CRC_A) ◀ LT	ATQA
18	PUT ▶ ‘50 00’ sent after $FDT_{A,PCD,MIN}$ ▶ LT	HLTA

Step	Exchanges	Comments
19	PUT ▶ '52' (short frame) sent between $t_{P,MIN}$ and $t_{P,MAX}$	▶ LT WUPA to poll for the PICC
20	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
21	PUT ▶ '50 00' sent after $FDT_{A,PCD,MIN}$	▶ LT HLTA
22	PUT ▶ '52' (short frame) sent between $t_{P,MIN}$ and $t_{P,MAX}$	▶ LT WUPA to poll for the PICC
23	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
24	PUT ▶ '50 00' sent after $FDT_{A,PCD,MIN}$	▶ LT HLTA
25	PUT ▶ '52' (short frame) sent between $t_{P,MIN}$ and $t_{P,MAX}$	▶ LT WUPA to poll for the PICC
26	PUT ▶ '52' (short frame) sent within $[FDT_{A,PICC,ANTICOLLISION} + t_{RETRANSMISSION}]$	▶ LT WUPA to poll for the PICC
27	PUT ▶ '52' (short frame) sent within $[FDT_{A,PICC,ANTICOLLISION} + t_{RETRANSMISSION}]$	▶ LT WUPA to poll for the PICC

Scenario 4: Type A Correct Removal

4.3. Basic Type A Exchange with the minimum and the default maximum Frame Delay Time PCD→PICC [TA003.x]

Test codification:

TA003.x

Test objective:

To ensure that the PCD accepts sequences received with the minimum or the maximum Frame Delay Time $FDT_{A,PICC}$ during a basic exchange (installation and block protocol).

References Requirements:

4.8.1.1, 4.8.1.8, 4.8.1.10, 4.8.1.12

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

For $x=0$:

After reception of the RATS command and until the End Of Test command (included), the LT replies to all commands and blocks using the minimum Frame Delay Time $FDT_{A,PICC,MIN}$ between the end of the sequence sent by the PUT and the beginning of the sequence replied by the LT.

Remark: before reception of the RATS command, the LT uses the default Frame Delay Time $FDT_{A,PICC,ANTICOLLISION}$.

For $x=1$:

The LT replies to the RATS commands using the maximum Frame Delay Time $FDT_{A,PICC,ACTIV,MAX}$ between the end of the sequence sent by the PUT and the beginning of the sequence replied by the LT.

After reception of the RATS command and until the End Of Test command (included), the LT replies to all the blocks using the default maximum Frame Delay Time $FDT_{A,PICC,MAX}$ between the end of the sequence sent by the PUT and the beginning of the sequence replied by the LT, with:

- $FDT_{A,PICC,MAX} = (114688 - 128)/f_c + 20/f_c [-1/f_c; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PUT is $(0)_b$,
- $FDT_{A,PICC,MAX} = (114688 - 128)/f_c + 84/f_c [-1/f_c; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PUT is $(1)_b$,

As $(FWT + \Delta FWT)$ takes the default value of $114688 \times 1/f_c$ in this test.

Remark: before reception of the RATS command, the LT uses the default Frame Delay Time $FDT_{A,PICC,ANTICOLLISION}$.

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						(FWT+ΔFWT)
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	114688 x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to the sequences sent by the LT with the minimum or the maximum Frame Delay Time).

Failure action:

Proceed with Type B tests.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ▲ 'C3 EE 59 63' + '17' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + 'C3 EE 59 63' + '17'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ▲ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ▲ ATS sent using the Frame Delay Time in function of 'x'	◀ LT ATS
13	PUT ▶ I(0) ₀ ['00 A4 04 00 0E' + '2PAY.SYS.DDF01' + '00']	▶ LT Select PPSE
14	PUT ▲ I(0) ₀ ['00 B2 05 04 00' + '90 00'] sent using the Frame Delay Time in function of 'x'	◀ LT
15	PUT ▶ I(0) ₁ ['00 B2 05 04 00']	▶ LT Loop-back
16	PUT ▲ I(0) ₁ ['00 B2 06 04 00' + '90 00'] sent using the Frame Delay Time in function of 'x'	◀ LT
17	PUT ▶ I(0) ₀ ['00 B2 06 04 00']	▶ LT Loop-back
18	PUT ▲ I(0) ₀ ['00 A4 04 00 17' + '2F 30 ... 45' + '00' + '90 00'] sent using the Frame Delay Time in function of 'x'	◀ LT
19	PUT ▶ I(0) ₁ ['00 A4 04 00 17' + '2F 30 ... 45' + '00']	▶ LT Loop-back (32 bytes frame)

Step	Exchanges	Comments
20	PUT ↪ I(0)₁ ['00 B2 07 04 00' + '90 00'] sent using the Frame Delay Time in function of 'x' ↪ LT	
21	PUT ↳ I(0)₀ ['00 B2 07 04 00'] ↳ LT	Loop-back
22	PUT ↪ I(0)₀ ['00 B2 08 04 00' + '90 00'] sent using the Frame Delay Time in function of 'x' ↪ LT	
23	PUT ↳ I(0)₁ ['00 B2 08 04 00'] ↳ LT	Loop-back
24	PUT ↪ I(0)₁ ['00 A4 04 00 17' + '46 47 ... 5C' + '00' + '90 00'] sent using the Frame Delay Time in function of 'x' ↪ LT	
25	PUT ↳ I(0)₀ ['00 A4 04 00 17' + '46 47 ... 5C' + '00'] ↳ LT	Loop-back (32 bytes frame)
26	PUT ↪ I(0)₀ ["EOT Command" + '90 00'] sent using the Frame Delay Time in function of 'x' ↪ LT	End Of Test command
27	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
28	PUT ↳ '52' (short frame) ↳ LT	WUPA to poll for the PICC
29	PUT ↳ '52' (short frame) ↳ LT	WUPA to poll for the PICC
30	PUT ↳ '52' (short frame) ↳ LT	WUPA to poll for the PICC

Scenario 5: Basic Type A Exchange with the minimum and the default maximum Frame Delay Time PCD→PICC (x=0 and 1)

4.4. Type A Installation with double and triple UID size [TA101.x]

Test codification:

TA101.x

Test objective:

To ensure that the PCD respects the series of commands during the basic installation of a Type A PICC with a Double or a Triple UID size.

References Requirements:

5.3.2.2, 9.3.2.4, 9.3.2.5, 9.3.2.6, 9.3.2.7

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenarios.

The LT replies to the WUPA command with an ATQA indicating a double (for x=0) or a triple (for x=1) UID size.

When the sequences sent by the LT are followed by a sequence sent by the PUT containing ANTICOLLISION CL2, SEL2, ANTICOLLISION CL3, SEL3 commands , the LT measures the delay between the end of the sequence sent by the LT and the beginning of the sequence replied by the PUT.

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenarios (the PUT accepts and replies to all the sequences sent by the LT).

The delay between the end of a sequence sent by the LT and the beginning of a sequence replied by the PUT containing the ANTICOLLISION CL2, SEL2, ANTICOLLISION CL3 or SEL3 command is at least FDT_{A,PCD,MIN}.

Failure action:

Proceed with the next test.

Scenarios:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '41 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '41 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ '88 3A A6 9F' + '8B' (no CRC_A)	◀ LT UID CL1 + BCC
9	PUT ▶ '93 70' + '88 3A A6 9F' + '8B'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '24'	◀ LT SAK
11	PUT ▶ '95 20' (no CRC_A) sent after FDT_{A,PCD,MIN}	▶ LT ANTICOLLISION CL2
12	PUT ◀ '89 25 11 D2' + '6F' (no CRC_A)	◀ LT UID CL2 + BCC
13	PUT ▶ '95 70' + '89 25 11 D2' + '6F' sent after FDT_{A,PCD,MIN}	▶ LT SEL2 + UID CL2 + BCC
14	PUT ◀ '20'	◀ LT SAK
15	PUT ▶ 'E0 80'	▶ LT RATS
16	PUT ◀ ATS	◀ LT ATS
17	PUT ▶ I(0)o ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
18	PUT ◀ I(0)o ["EOT Command" + '90 00']	◀ LT End Of Test command
19	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
20	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
21	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
22	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 6: Basic Type A Installation (double UID size; x=0)

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '81 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '81 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ '88 72 B8 29' + '6B' (no CRC_A)	◀ LT UID CL1 + BCC
9	PUT ▶ '93 70' + '88 72 B8 29' + '6B'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '24'	◀ LT SAK
11	PUT ▶ '95 20' (no CRC_A)	▶ LT ANTICOLLISION CL2
12	PUT ◀ '88 F1 3C 48' + '0D' (no CRC_A)	◀ LT UID CL2 + BCC
13	PUT ▶ '95 70' + '88 F1 3C 48' + '0D'	▶ LT SEL2 + UID CL2 + BCC
14	PUT ◀ '24'	◀ LT SAK
15	PUT ▶ '97 20' (no CRC_A) sent after FDT_{A,PCD,MIN}	▶ LT ANTICOLLISION CL3
16	PUT ◀ '00 01 3E DA' + 'E5' (no CRC_A)	◀ LT UID CL3 + BCC
17	PUT ▶ '97 70' + '00 01 3E DA' + 'E5' sent after FDT_{A,PCD,MIN}	▶ LT SEL3 + UID CL3 + BCC
18	PUT ◀ '20'	◀ LT SAK
19	PUT ▶ 'E0 80'	▶ LT RATS
20	PUT ◀ ATS	◀ LT ATS
21	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
22	PUT ◀ I(0)₀ [“EOT Command” + '90 00']	◀ LT End Of Test command
23	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
24	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
25	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
26	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 7: Basic Type A Installation (triple UID size; x=1)

4.5. Type A Installation with supported values of ATQA [TA102.x]

Test codification:

TA102.x

Test objective:

To ensure that the PCD accepts all the possible values of the ATQA.

References Requirements:

5.3.2.1

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenarios.

The following ATQA responses are successively sent by the LT:

- x=0: ATQA = '01 0A' (no CRC_A)
- x=1: ATQA = '02 0F' (no CRC_A)
- x=2: ATQA = '04 05' (no CRC_A)
- x=3: ATQA = '08 0A' (no CRC_A)
- x=4: ATQA = '10 03' (no CRC_A)
- x=5: ATQA = '21 0C' (no CRC_A)
- x=6: ATQA = '44 00' (no CRC_A)
- x=7: ATQA = '90 00' (no CRC_A)
- x=8: ATQA = '40 00' (no CRC_A)
- x=9: ATQA = 'D1 00' (no CRC_A)

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to ATQA).

Failure action:

Proceed with the next test.

Scenarios:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	ATQA (no CRC_A) in function of 'x' For x=0: ATQA = '01 0A' (no CRC_A) For x=1: ATQA = '02 0F' (no CRC_A) For x=2: ATQA = '04 05' (no CRC_A) PUT ◀ For x=3: ATQA = '08 0A' (no CRC_A) ◀ LT For x=4: ATQA = '10 03' (no CRC_A) For x=5: ATQA = '21 0C' (no CRC_A) For x=8: ATQA = '40 00' (no CRC_A) For x=9: ATQA = 'D1 00' (no CRC_A)	ATQA in function of 'x'
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	ATQA (no CRC_A) in function of 'x' For x=0: ATQA = '01 0A' (no CRC_A) For x=1: ATQA = '02 0F' (no CRC_A) For x=2: ATQA = '04 05' (no CRC_A) PUT ◀ For x=3: ATQA = '08 0A' (no CRC_A) ◀ LT For x=4: ATQA = '10 03' (no CRC_A) For x=5: ATQA = '21 0C' (no CRC_A) For x=8: ATQA = '40 00' (no CRC_A) For x=9: ATQA = 'D1 00' (no CRC_A)	ATQA in function of 'x'
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ◀ 'C3 EE 59 63' + '17' (no CRC_A) ◀ LT	UID CL1 + BCC
9	PUT ▶ '93 70' + 'C3 EE 59 63' + '17' ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ◀ '20' ◀ LT	SAK
11	PUT ▶ 'E0 80' ▶ LT	RATS
12	PUT ◀ ATS ◀ LT	ATS
13	PUT ▶ I(0)_0 ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
14	PUT ◀ I(0)_0 [“EOT Command” + '90 00'] ◀ LT	End Of Test command

Step	Exchanges	Comments
15	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
16	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
17	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
18	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 8: Type A Installation with supported values of ATQA (x=0 to 5, 8 and 9)

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ↴ ATQA (no CRC_A) in function of 'x' For x=6: ATQA = '44 00' (no CRC_A) ◀ LT	ATQA in function of 'x'
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ↴ ATQA (no CRC_A) in function of 'x' For x=6: ATQA = '44 00' (no CRC_A) ◀ LT	ATQA in function of 'x'
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ↴ '88 3A A6 9F' + '8B' (no CRC_A) ◀ LT	UID CL1 + BCC
9	PUT ▶ '93 70' + '88 3A A6 9F' + '8B' ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ↴ '24' ◀ LT	SAK
11	PUT ▶ '95 20' (no CRC_A) ▶ LT	ANTICOLLISION CL2
12	PUT ↴ '89 25 11 D2' + '6F' (no CRC_A) ◀ LT	UID CL2 + BCC
13	PUT ▶ '95 70' + '89 25 11 D2' + '6F' ▶ LT	SEL2 + UID CL2 + BCC
14	PUT ↴ '20' ◀ LT	SAK
15	PUT ▶ 'E0 80' ▶ LT	RATS
16	PUT ↴ ATS ◀ LT	ATS
17	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
18	PUT ↴ I(0)₀ ["EOT Command" + '90 00'] ◀ LT	End Of Test command
19	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
20	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
21	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
22	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC

Scenario 9: Type A Installation with supported values of ATQA (x=6)

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ↴ ATQA (no CRC_A) in function of 'x' For x=7: ATQA = '90 00' (no CRC_A) ◀ LT	ATQA in function of 'x'
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ↴ ATQA (no CRC_A) in function of 'x' For x=7: ATQA = '90 00' (no CRC_A) ◀ LT	ATQA in function of 'x'
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ↴ '88 72 B8 29' + '6B' (no CRC_A) ◀ LT	UID CL1 + BCC
9	PUT ▶ '93 70' + '88 72 B8 29' + '6B' ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ↴ '24' ◀ LT	SAK
11	PUT ▶ '95 20' (no CRC_A) ▶ LT	ANTICOLLISION CL2
12	PUT ↴ '88 F1 3C 48' + '0D' (no CRC_A) ◀ LT	UID CL2 + BCC
13	PUT ▶ '95 70' + '88 F1 3C 48' + '0D' ▶ LT	SEL2 + UID CL2 + BCC
14	PUT ↴ '24' ◀ LT	SAK
15	PUT ▶ '97 20' (no CRC_A) ▶ LT	ANTICOLLISION CL3
16	PUT ↴ '00 01 3E DA' + 'E5' (no CRC_A) ◀ LT	UID CL3 + BCC
17	PUT ▶ '97 70' + '00 01 3E DA' + 'E5' ▶ LT	SEL3 + UID CL3 + BCC
18	PUT ↴ '20' ◀ LT	SAK
19	PUT ▶ 'E0 80' ▶ LT	RATS
20	PUT ↴ ATS ◀ LT	ATS
21	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
22	PUT ↴ I(0)₀ ["EOT Command" + '90 00'] ◀ LT	End Of Test command
23	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
24	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
25	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
26	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC

Scenario 10: Type A Installation with supported values of ATQA (x=7)

4.6. Type A Installation with supported values of SAK and of the TA(1) byte of the ATS [TA103.x]

Test codification:

TA103.x

Test objective:

To ensure that the PCD accepts all the possible values of the SAK and of the byte TA(1) of the ATS.

References Requirements:

5.5.2.1, 5.5.2.3, 5.7.2.8, 5.7.2.9a

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenarios.

The LT replies to the WUPA command with an ATQA indicating a triple UID size.

The following SAK responses are successively sent by the LT:

- x=0: SAK = 'B6' following the SELECT CL1 command, SAK = 'E4' following the SELECT CL2 command and SAK = '7B' following the SELECT CL3 command
- x=1: SAK = '6D' following the SELECT CL1 command, SAK = '3C' following the SELECT CL2 command and SAK = 'A3' following the SELECT CL3 command
- x=2: SAK = 'FF' following the SELECT CL1 command, SAK = '27' following the SELECT CL2 command and SAK = 'F0' following the SELECT CL3 command
- x=3: SAK = '04' following the SELECT CL1 command, SAK = 'DF' following the SELECT CL2 command and SAK = '20' following the SELECT CL3 command
- x=4: SAK = '28' following the SELECT CL1 command
- x=5: SAK = 'FB' following the SELECT CL1 command

In this test, the following ATS shall be used:

	ATS						Comments
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
x=0	'05'	'72'	'88'	'40'	'02'	-	Different correct values of TA(1)
x=1	'05'	'72'	'00'	'40'	'02'	-	
x=2	'05'	'72'	'08'	'40'	'02'	-	
x=3	'05'	'72'	'FF'	'40'	'02'		
x=4	'05'	'72'	'00'	'40'	'02'		
x=5	'05'	'72'	'00'	'40'	'02'		

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to the successive SAK and to the ATS).

Failure action:

Proceed with the next test.

Scenarios:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ▲ '81 00' (no CRC_A) ◀ LT	ATQA
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ▲ '81 00' (no CRC_A) ◀ LT	ATQA
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ▲ '88 23 A7 9C' + '90' (no CRC_A) ◀ LT	UID CL1 + BCC
9	PUT ▶ '93 70' + '88 23 A7 9C' + '90' ▶ LT	SEL1 + UID CL1 + BCC
10	SAK in function of 'x' For x=0: 'B6' PUT ▲ For x=1: '6D' For x=2: 'FF' For x=3: '04' ◀ LT	SAK in function of 'x'
11	PUT ▶ '95 20' (no CRC_A) ▶ LT	ANTICOLLISION CL2
12	PUT ▲ '88 C6 48 E3' + 'E5' (no CRC_A) ◀ LT	UID CL2 + BCC
13	PUT ▶ '95 70' + '88 C6 48 E3' + 'E5' ▶ LT	SEL2 + UID CL2 + BCC
14	SAK in function of 'x' For x=0: 'E4' PUT ▲ For x=1: '3C' For x=2: '27' For x=3: 'DF' ◀ LT	SAK in function of 'x'
15	PUT ▶ '97 20' (no CRC_A) ▶ LT	ANTICOLLISION CL3

Step	Exchanges	Comments
16	PUT ↳ '22 5D F2 69' + 'E4' (no CRC_A)	◀ LT UID CL3 + BCC
17	PUT ↴ '97 70' + '22 5D F2 69' + 'E4'	▶ LT SEL3 + UID CL3 + BCC
18	PUT ↳ SAK in function of 'x' For x=0: '7B' For x=1: 'A3' For x=2: 'F0' For x=3: '20'	◀ LT SAK in function of 'x'
19	PUT ↴ 'E0 80'	▶ LT RATS
20	PUT ↳ ATS with TA(1) in function of 'x'	◀ LT ATS in function of 'x'
21	PUT ↴ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
22	PUT ↳ I(0)₀ ["EOT Command" + '90 00']	◀ LT End Of Test command
23	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
24	PUT ↴ '52' (short frame)	▶ LT WUPA to poll for the PICC
25	PUT ↴ '52' (short frame)	▶ LT WUPA to poll for the PICC
26	PUT ↴ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 11: Type A Installation with supported values of SAK and of the TA(1) byte of the ATS (x=0 to 3)

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ '87 23 A7 9C' + '9F' (no CRC_A)	◀ LT UID CL1 + BCC
9	PUT ▶ '93 70' + '87 23 A7 9C' + '9F'	▶ LT SEL1 + UID CL1 + BCC
10	SAK in function of 'x' PUT ◀ For x=4: '28' For x=5: 'FB'	◀ LT SAK in function of 'x'
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS with TA(1) in function of 'x'	◀ LT ATS in function of 'x'
13	PUT ▶ I(0)o ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ◀ I(0)o ["EOT Command" + '90 00']	◀ LT End Of Test command
15	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
16	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
17	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
18	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 12: Type A Installation with supported values of SAK (x=4 to 5)

4.7. Type A Installation with supported values of the TL byte (and historical bytes) of the ATS [TA104.xy]

Test codification:

TA104.xy

Test objective:

To ensure that the PCD accepts all the possible ATS sizes and any value of the historical bytes of the ATS.

References Requirements:

5.7.2.2, 5.7.2.6, 5.7.2.14

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

In this test, the following ATS shall be used:

	ATS						ATS size
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
xy=00	'05'	'72'	'80'	'40'	'02'	-	5 bytes
xy=01	'06'	'72'	'80'	'40'	'02'	'FF'	6 bytes
xy=02	'07'	'72'	'80'	'40'	'02'	'02 0F'	7 bytes
xy=03	'08'	'72'	'80'	'40'	'02'	'3C 5A 69'	8 bytes
xy=04	'09'	'72'	'80'	'40'	'02'	'BD 32 1F ED'	9 bytes
xy=05	'0A'	'72'	'80'	'40'	'02'	'0A 72 80 40 02'	10 bytes
xy=06	'0B'	'72'	'80'	'40'	'02'	'01 24 80 FE DB 7F'	11 bytes
xy=07	'0C'	'72'	'80'	'40'	'02'	'00 00 00 00 00 00 00 00'	12 bytes
xy=08	'0D'	'72'	'80'	'40'	'02'	'89 C3 5E 72 1D 88 F5 87'	13 bytes
xy=09	'0E'	'72'	'80'	'40'	'02'	'20 24 20 24 20 24 20 24 20'	14 bytes
xy=10	'0F'	'72'	'80'	'40'	'02'	'C3 EE 59 63 17 C3 EE 59 63 17'	15 bytes
xy=11	'10'	'72'	'80'	'40'	'02'	'E0 80 E0 80 E0 80 E0 80 E0 80 E0'	16 bytes
xy=12	'11'	'72'	'80'	'40'	'02'	'00 01 02 03 04 05 06 07 08 09 0A 0B'	17 bytes
xy=13	'12'	'72'	'80'	'40'	'02'	'00 10 20 30 40 50 60 70 80 90 A0 B0 C0'	18 bytes

	ATS						ATS size
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
xy=14	'13'	'72'	'80'	'40'	'02'	'13 12 80 40 02 13 72 80 FF 02 04 62 FF 11'	19 bytes
xy=15	'14'	'72'	'80'	'40'	'02'	'FF FF FF'	20 bytes
xy=16	'01'	-	-	-	-	-	1 bytes
xy=17	'02'	'02'	-	-	-	-	2 bytes
xy=18	'03'	'12'	'80'	-	-	-	3 bytes
xy=19	'04'	'32'	'80'	'40'	-	-	4 bytes
xy=20	'11'	'02'	-	-	-	'FF FF FF 78 9A BC DE F1 23 45 67 89 AB CD EF'	17 bytes
xy=21	'0E'	'22'	-	'40'	-	'AC 35 5A C3 CA 3C 35 53 A5 A3 3A'	14 bytes

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to the ATS).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ 'C3 EE 59 63' + '17' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + 'C3 EE 59 63' + '17'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS with TL and historical bytes in function of 'xy'	◀ LT ATS in function of 'xy'
13	PUT ▶ I(0)0 ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ◀ I(0)0 ["EOT Command" + '90 00']	◀ LT End Of Test command
15	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
16	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
17	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
18	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 13: Type A Installation with supported values of the TL byte (and historical bytes) of the ATS (xy=00 to 21)

4.8. Type A Installation with supported values of SFGI in the TB(1) byte of the ATS [TA105.xy]

Test codification:

TA105.xy

Test objective:

To ensure that the PCD accepts all the possible values of SFGI in the byte TB(1) of the ATS and applies the corresponding minimum Frame Delay Time before sending the first I-Block of the Block Protocol.

References Requirements:

4.8.2.1, 4.8.2.3, 4.8.2.5, 4.8.2.6, 5.7.2.6, 5.7.2.11, 5.7.2.11a

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

After having sent the ATS, the LT measures the delay between the end of the sequence containing the ATS and the beginning of the sequence containing the first I-Block of an EMV Contactless transaction.

In this test, the following ATS shall be used:

	ATS						(SFGT+ΔSFGT)
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
xy=00	'05'	'72'	'80'	'40'	'02'	-	FDT _{A,PCD,MIN}
xy=01	'05'	'72'	'80'	'41'	'02'	-	8960 x 1/f _c
xy=02	'05'	'72'	'80'	'42'	'02'	-	17920 x 1/f _c
xy=03	'05'	'72'	'80'	'43'	'02'	-	35840 x 1/f _c
xy=04	'05'	'72'	'80'	'44'	'02'	-	71680 x 1/f _c (default value)
xy=05	'05'	'72'	'80'	'45'	'02'	-	143360 x 1/f _c
xy=06	'05'	'72'	'80'	'46'	'02'	-	286720 x 1/f _c
xy=07	'05'	'72'	'80'	'47'	'02'	-	573440 x 1/f _c
xy=08	'05'	'72'	'80'	'48'	'02'	-	1146880 x 1/f _c
xy=09	'03'	'42'	-	-	'02'	-	FDT _{A,PCD,MIN}
xy=10	'05'	'72'	'80'	'49'	'02'	-	2293760 x 1/f _c
xy=11	'05'	'72'	'80'	'4A'	'02'	-	4587520 x 1/f _c
xy=12	'05'	'72'	'80'	'4B'	'02'	-	9175040 x 1/f _c
xy=13	'05'	'72'	'80'	'4C'	'02'	-	18350080 x 1/f _c

	ATS						(SFGT+ΔSFGT)
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
xy=14	'05'	'72'	'80'	'4D'	'02'	-	36700160 x 1/f _c
xy=15	'05'	'72'	'80'	'4E'	'02'	-	73400320 x 1/f _c
xy=16	'05'	'72'	'80'	'4F'	'02'	-	FDT _{A,PCD,MIN}

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts the ATS and correctly applies the minimum Frame Delay Time specific to the first I-Block of a Type A transaction).

The delay between the end of the sequence containing the ATS and the beginning of the sequence containing the first I-Block of an EMV Contactless transaction is at least equal to (SFGT+ΔSFGT) as requested by the LT in the ATS (see table above).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ '03 49 A7 B5' + '58' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '03 49 A7 B5' + '58'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS with TB(1) in function of 'xy'	◀ LT ATS in function of 'xy'
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] sent after (SFGT+ΔSFGT) in function of 'xy'	▶ LT Select PPSE
14	PUT ◀ I(0)₀ ["EOT Command" + '90 00']	◀ LT End Of Test command
15	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
16	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
17	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
18	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 14: Type A Installation with supported values of SFGI in the TB(1) byte of the ATS (xy=00 to 16)

4.9. Type A Installation with supported values of the TC(1) byte of the ATS [TA106.x]

Test codification:

TA106.x

Test objective:

To ensure that the PCD accepts all the possible values of the byte TC(1) of the ATS.

References Requirement:

5.7.2.13

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

In this test, the following ATS shall be used:

	ATS						Comments
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
x=0	'05'	'72'	'80'	'40'	'00'	-	CID and NAD not supported
x=1	'05'	'72'	'80'	'40'	'01'	-	NAD only supported
-	'05'	'72'	'80'	'40'	'02'	-	<i>CID only supported already tested in TA001 (default value)</i>
x=2	'05'	'72'	'80'	'40'	'03'	-	CID and NAD supported
x=3	'05'	'72'	'80'	'40'	'FC'	-	RFU bits not to zero
x=4	'05'	'72'	'80'	'40'	'A8'	-	
x=5	'05'	'72'	'80'	'40'	'54'	-	

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts the ATS and sends all its Blocks with no CID/NAD bytes in the prologue field).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ 'BE 13 E4 A4' + 'ED' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + 'BE 13 E4 A4' + 'ED'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS with TC(1) in function of 'x'	◀ LT ATS in function of 'x'
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + '2PAY.SYS.DDF01' + '00']	▶ LT Select PPSE
14	PUT ◀ I(0)₀ ["EOT Command" + '90 00']	◀ LT End Of Test command
15	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
16	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
17	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
18	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

**Scenario 15: Type A Installation with supported values of the TC(1) byte of the ATS
(x=0 to 5)**

4.10.Type A Installation with Type A frame answered to HLTA command [TA108]

Test codification:

TA108

Test objective:

To ensure that the PCD always considers the HLTA command as acknowledged.

References Requirement:

5.6.2.1

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

Upon receipt of the HLTA command sent by the PUT, the LT sends a Type A frame containing '01 00' using the default Type A PICC Frame Delay Time between the end of the HLTA command sequence and the beginning of the Type A frame containing '01 00'.

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenarios (the PUT disregards the Type A frame containing '01 00' answered to the HLTA command).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ◀ '01 00' sent using the default Type A PICC Frame Delay Time	◀ LT Error
5	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
6	PUT ▶ '52' (short frame)	▶ LT WUPA
7	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
8	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
9	PUT ◀ 'BE 13 E4 A4' + 'ED' (no CRC_A)	◀ LT UID CL1 + BCC
10	PUT ▶ '93 70' + 'BE 13 E4 A4' + 'ED'	▶ LT SEL1 + UID CL1 + BCC
11	PUT ◀ '20'	◀ LT SAK
12	PUT ▶ 'E0 80'	▶ LT RATS
13	PUT ◀ ATS	◀ LT ATS
14	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT PPSE selection
15	PUT ◀ I(0)₀ ["EOT Command" + '90 00']	◀ LT End Of Test command
16	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
17	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
18	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
19	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 16: Type A Installation with Type A frame answered to HLTA command

4.11.Type A Installation with different values of ATQA [TA110.x]

Test codification:

TA110.x

Test objective:

To ensure that the PCD does not compare the different ATQA received during polling and collision detection and only takes the value of the second ATQA into account.

References Requirement:

9.2.1.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

During the polling procedure and during the collision detection procedure, the LT sends ATQA responses having different values (ATQA indicating different UID sizes, with different Bit frame anticollision fields or with different values of the Byte 2).

The following ATQA responses are successively sent by the LT during the polling procedure (following the first WUPA command received from the PUT):

- x=0: ATQA = '41 00' (no CRC_A)
- x=1: ATQA = '81 00' (no CRC_A)
- x=2: ATQA = '10 F0' (no CRC_A)
- x=3: ATQA = '04 0F' (no CRC_A)

And for x=0 to 3, the LT sends the standard ATQA response during the collision detection procedure (following the first WUPB command received from the PUT): ATQA = '01 00' (no CRC_A).

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to ATQA and takes only the value of the second ATQA into account).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	ATQA in function of 'x' For x=0: ATQA = '41 00' (no CRC_A) For x=1: PUT ◀ ATQA = '81 00' (no CRC_A) ◀ LT For x=2: ATQA = '10 F0' (no CRC_A) For x=3: ATQA = '04 0F' (no CRC_A)	ATQA in function of 'x'
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ◀ '78 04 15 6F' + '06' (no CRC_A) ◀ LT	UID
9	PUT ▶ '93 70' + '78 04 15 6F' + '06' ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ◀ '20' ◀ LT	SAK
11	PUT ▶ 'E0 80' ▶ LT	RATS
12	PUT ◀ ATS ◀ LT	ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
14	PUT ◀ I(0)₀ ["EOT Command" + '90 00'] ◀ LT	End Of Test command
15	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
16	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
17	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
18	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC

Scenario 17: Type A installation with different values of ATQA (x=0 to 3)

4.12.Type A Error free non-chained I-Blocks exchanges for all possible values of FWT [TA201.xy]

Test codification:

TA201.xy

Test objective:

To ensure that the PCD accepts all the possible values of FWI in the byte TB(1) of the ATS and accepts sequences received with the corresponding maximum Frame Delay Time.

References Requirements:

4.8.1.8, 4.8.1.10, 5.7.2.6, 5.7.2.10b

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

During the Half-Duplex Block Protocol and until the End Of Test command, the LT replies to all the blocks sent by the PUT using the maximum Frame Delay Time $FDT_{A,PICC,MAX}$ between the end of the sequence sent by the PUT and the beginning of the sequence replied by the LT, with:

- $FDT_{A,PICC,MAX} = (FWT + \Delta FWT) - 128/f_c + 20/f_c [-1/f_c; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PUT is $(0)_b$
- $FDT_{A,PICC,MAX} = (FWT + \Delta FWT) - 128/f_c + 84/f_c [-1/f_c; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PUT is $(1)_b$

In this test, the following ATS and Frame Waiting Time shall be used:

	ATS						FWT + ΔFWT
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
xy=00	'05'	'72'	'80'	'00'	'02'	-	$53248 \times 1/f_c$
xy=01	'05'	'72'	'80'	'10'	'02'	-	$57344 \times 1/f_c$
xy=02	'05'	'72'	'80'	'20'	'02'	-	$65536 \times 1/f_c$
xy=03	'05'	'72'	'80'	'30'	'02'	-	$81920 \times 1/f_c$
-	'05'	'72'	'80'	'40'	'02'	-	<i>Already tested in TA003.1 (default value)</i>
xy=04	'05'	'72'	'80'	'50'	'02'	-	$180224 \times 1/f_c$
xy=05	'05'	'72'	'80'	'60'	'02'	-	$311296 \times 1/f_c$
xy=06	'05'	'72'	'80'	'70'	'02'	-	$573440 \times 1/f_c$
xy=07	'05'	'72'	'80'	'80'	'02'	-	$1097728 \times 1/f_c$
xy=08	'05'	'72'	'80'	'90'	'02'	-	$2146304 \times 1/f_c$
xy=09	'05'	'72'	'80'	'A0'	'02'	-	$4243456 \times 1/f_c$

	ATS						FWT+ΔFWT
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
xy=10	'05'	'72'	'80'	'B0'	'02'	-	8437760 x 1/f _c
xy=11	'05'	'72'	'80'	'C0'	'02'	-	16826368 x 1/f _c
xy=12	'05'	'72'	'80'	'D0'	'02'		33603584 x 1/f _c
xy=13	'05'	'72'	'80'	'E0'	'02'		67158016 x 1/f _c
xy=14	'04'	'52'	'80'	-	'02'	-	114688 x 1/f _c
xy=15	'05'	'72'	'80'	'F0'	'02'	-	114688 x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts all the sequences sent by the LT with the maximum Frame Delay Time).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ◀ '01 00' (no CRC_A) ▲ LT	ATQA
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ◀ '01 00' (no CRC_A) ▲ LT	ATQA
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ◀ 'AD B1 C8 D6' + '02' (no CRC_A) ▲ LT	UID
9	PUT ▶ '93 70' + 'AD B1 C8 D6' + '02' ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ◀ '20' ▲ LT	SAK
11	PUT ▶ 'E0 80' ▶ LT	RATS
12	PUT ◀ ATS with TB(1) in function of 'xy' ▲ LT	ATS in function of 'xy'
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
14	PUT ◀ I(0)₀ ['00 B2 01 04 00' + '90 00'] sent using FDT _{A,PICC,MAX} in function of 'xy' ▲ LT	
15	PUT ▶ I(0)₁ ['00 B2 01 04 00'] ▶ LT	Loop-back
16	PUT ◀ I(0)₁ ['00 B2 02 04 00' + '90 00'] sent using FDT _{A,PICC,MAX} in function of 'xy' ▲ LT	
17	PUT ▶ I(0)₀ ['00 B2 02 04 00'] ▶ LT	Loop-back

Step	Exchanges	Comments
18	PUT ↪ I(0)₀ ['00 A4 04 00 17' + '01 02 ... 17' + '00' + '90 00'] sent using FDT_{A,PICC,MAX} in function of 'xy' ↪ LT	
19	PUT ↪ I(0)₁ ['00 A4 04 00 17' + '01 02 ... 17' + '00'] ↪ LT	Loop-back (32 bytes frame)
20	PUT ↪ I(0)₁ ['00 B2 03 04 00' + '90 00'] sent using FDT_{A,PICC,MAX} in function of 'xy' ↪ LT	
21	PUT ↪ I(0)₀ ['00 B2 03 04 00'] ↪ LT	Loop-back
22	PUT ↪ I(0)₀ ['00 B2 04 04 00' + '90 00'] sent using FDT_{A,PICC,MAX} in function of 'xy' ↪ LT	
23	PUT ↪ I(0)₁ ['00 B2 04 04 00'] ↪ LT	Loop-back
24	PUT ↪ I(0)₁ ['00 A4 04 00 17' + '18 19 ... 2E' + '00' + '90 00'] sent using FDT_{A,PICC,MAX} in function of 'xy' ↪ LT	
25	PUT ↪ I(0)₀ ['00 A4 04 00 17' + '18 19 ... 2E' + '00'] ↪ LT	Loop-back (32 bytes frame)
26	PUT ↪ I(0)₀ ['EOT Command' + '90 00'] sent using FDT_{A,PICC,MAX} in function of 'xy' ↪ LT	End Of Test command
27	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) ↪ LT	PICC Reset
28	PUT ↪ '52' (short frame) ↪ LT	WUPA to poll for the PICC
29	PUT ↪ '52' (short frame) ↪ LT	WUPA to poll for the PICC
30	PUT ↪ '52' (short frame) ↪ LT	WUPA to poll for the PICC

Scenario 18: Type A Error free non-chained I-Blocks exchanges for all possible values of FWT (xy=00 to 15)

4.13.Type A Error free chained I-Blocks in both directions for FSC = 256 bytes [TA202.xy]

Test codification:

TA202.xy

Test objective:

To ensure that the PCD accepts the values FSCI = '8' to 'F' in the byte T0 of the ATS and is able to correctly send and receive chained I-Blocks of sizes up to 256 bytes.

References Requirements:

4.7.3.1, 4.7.4.1, 4.7.4.3, 5.7.2.5, 10.1.1.1, 10.1.1.3, 10.3.2.1, 10.3.2.2, 10.3.3.3, 10.3.4.5

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Run y=0, if the PCD does not send empty I-Block after chained blocks (see ICS).

Run y=1, if the PCD may send empty I-blocks after a chain of I-Blocks (see ICS)

Procedure:

Run the following scenarios.

When the sequences sent by the LT are followed by a sequence sent by the PUT containing R(ACK)-Blocks, the LT measures the delay between the end of the sequence sent by the LT and the beginning of the sequence replied by the PUT.

During the Half-Duplex Block Protocol and until the End Of Test command, the LT replies to all the blocks sent by the PUT using a Frame Delay Time as follows between the end of a sequence sent by the PUT and the beginning of the next sequence replied by the LT:

- $FDT_{A,PICC} = n \times 128/f_c + 20/f_c [-1/f_c; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PCD is (0)_b
- $FDT_{A,PICC} = n \times 128/f_c + 84/f_c [-1/f_c; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PCD is (1)_b

For x=0 to 7, n=15.

For x=8, n=9 (i.e. $FDT_{A,PICC} = FDT_{A,PICC,MIN}$)

In this test, the following ATS shall be used:

	ATS						Maximum Frame Size for the PICC (FSC)
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
x=0	'05'	'78'	'80'	'40'	'02'	-	256 bytes
x=1	'05'	'79'	'80'	'40'	'02'	-	
x=2	'05'	'7A'	'80'	'40'	'02'	-	
x=3	'05'	'7B'	'80'	'40'	'02'	-	
x=4	'05'	'7C'	'80'	'40'	'02'	-	
x=5	'05'	'7D'	'80'	'40'	'02'	-	
x=6	'05'	'7E'	'80'	'40'	'02'	-	
x=7	'05'	'7F'	'80'	'40'	'02'	-	
x=8	'05'	'78'	'80'	'40'	'02'	-	

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts the chained I-Blocks, sends sequences containing up to 256 bytes and uses chaining when necessary).

The delay between the end of a sequence sent by the LT and the beginning of the sequence replied by the PUT containing a R(ACK)-Block is at least FDT_{A,PCD,MIN}.

Failure action:

Proceed with the next test.

Scenarios:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ◀ '01 00' (no CRC_A) ▲ LT	ATQA
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ◀ '01 00' (no CRC_A) ▲ LT	ATQA
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ◀ 'EB 39 A7 61' + '14' (no CRC_A) ▲ LT	UID
9	PUT ▶ '93 70' + 'EB 39 A7 61' + '14' ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ◀ '20' ▲ LT	SAK
11	PUT ▶ 'E0 80' ▶ LT	RATS
12	PUT ◀ ATS with T0 in function of 'x' ▲ LT	ATS in function of 'x'
13	PUT ▶ I(0)0 ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE

Step	Exchanges	Comments
14	PUT \leftarrow I(1) ₀ ['00 A4 04 00 18' + '01 02 03 ... 06 07 08'] \leftarrow LT	16 bytes frame
15	PUT \rightarrow R(ACK) ₁ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
16	PUT \leftarrow I(1) ₁ ['09 0A 0B ... 13 14 15'] \leftarrow LT	16 bytes frame
17	PUT \rightarrow R(ACK) ₀ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
18	PUT \leftarrow I(0) ₀ ['16 17 18' + '00' + '90 00'] \leftarrow LT	9 bytes last Block of chain
19	PUT \rightarrow I(0) ₁ ['00 A4 04 00 18' + '01 02 03 ... 16 17 18' + '00'] \rightarrow LT	Loop-back
20	PUT \leftarrow I(1) ₁ ['00 A4 04 00 47' + '01 02 03 ... 16 17 18'] \leftarrow LT	32 bytes frame
21	PUT \rightarrow R(ACK) ₀ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
22	PUT \leftarrow I(1) ₀ ['19 1A 1B ... 33 34 35'] \leftarrow LT	32 bytes frame
23	PUT \rightarrow R(ACK) ₁ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
24	PUT \leftarrow I(0) ₁ ['36 37 ... 46 47' + '00' + '90 00'] \leftarrow LT	24 bytes last Block of chain
25	PUT \rightarrow I(0) ₀ ['00 A4 04 00 47' + '01 02 03 ... 45 46 47' + '00'] \rightarrow LT	Loop-back
26	PUT \leftarrow I(1) ₀ ['00 A4 04 00 87' + '01 02 03 ... 36 37 38'] \leftarrow LT	64 bytes frame
27	PUT \rightarrow R(ACK) ₁ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
28	PUT \leftarrow I(1) ₁ ['39 3A 3B ... 73 74 75'] \leftarrow LT	64 bytes frame
29	PUT \rightarrow R(ACK) ₀ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
30	PUT \leftarrow I(0) ₀ ['76 77 78 ... 85 86 87' + '00' + '90 00'] \leftarrow LT	24 bytes last Block of chain
31	PUT \rightarrow I(0) ₁ ['00 A4 04 00 87' + '01 02 03 ... 85 86 87' + '00'] \rightarrow LT	Loop-back
32	PUT \leftarrow I(1) ₁ ['00 A4 04 00 F7' + '01 02 03 ... 76 77 78'] \leftarrow LT	128 bytes frame
33	PUT \rightarrow R(ACK) ₀ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
34	PUT \leftarrow I(1) ₀ ['79 7A 7B ... F3 F4 F5'] \leftarrow LT	128 bytes frame
35	PUT \rightarrow R(ACK) ₁ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
36	PUT \leftarrow I(1) ₁ [] \leftarrow LT	Empty I-block indicating chaining
37	PUT \rightarrow R(ACK) ₀ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
38	PUT \leftarrow I(0) ₀ ['F6 F7' + '00' + '90 00'] \leftarrow LT	8 bytes frame

Step	Exchanges	Comments
39	PUT ▶ I(0)₁ ['00 A4 04 00 F7' + '01 02 03 ... F5 F6 F7' + '00'] ▶ LT	Loop-back (256 bytes non chained block)
40	PUT ◀ I(1)₁ ['00 A4 04 00 F8' + '01 02 03 ... F6 F7 F8'] ◀ LT	256 bytes chained block
41	PUT ▶ R(ACK)₀ sent after FDT_{A,PCD,MIN} ▶ LT	Acknowledgment R-Block
42	PUT ◀ I(0)₀ ['00' + '90 00'] ◀ LT	6 bytes frame
43	PUT ▶ I(1)₁ ['00 A4 04 00 F8' + '01 02 03 ... F6 F7 F8'] ▶ LT	Loop-back (256 bytes chained block)
44	PUT ◀ R(ACK)₁ ◀ LT	Acknowledgment R-Block
45	PUT ▶ I(0)₀ ['00'] ▶ LT	Loop-back (4 bytes frame)
46	PUT ◀ I(0)₀ ["EOT Command" + '90 00'] ◀ LT	End Of Test command
47	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) □ LT	PICC Reset
48	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
49	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
50	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC

**Scenario 19: Type A Error free chained I-Blocks in both directions for FSC = 256 bytes
(x=0 to 8, y=0)**

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ◀ 'EB 39 A7 61' + '14' (no CRC_A) ◀ LT	UID
9	PUT ▶ '93 70' + 'EB 39 A7 61' + '14' ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ◀ '20' ◀ LT	SAK
11	PUT ▶ 'E0 80' ▶ LT	RATS
12	PUT ◀ ATS with T0 in function of 'x' ◀ LT	ATS in function of 'x'
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE

Step	Exchanges	Comments
14	PUT \leftarrow I(1) ₀ ['00 A4 04 00 18' + '01 02 03 ... 06 07 08'] \leftarrow LT	16 bytes frame
15	PUT \rightarrow R(ACK) ₁ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
16	PUT \leftarrow I(1) ₁ ['09 0A 0B ... 13 14 15'] \leftarrow LT	16 bytes frame
17	PUT \rightarrow R(ACK) ₀ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
18	PUT \leftarrow I(0) ₀ ['16 17 18' + '00' + '90 00'] \leftarrow LT	9 bytes last Block of chain
19	PUT \rightarrow I(0) ₁ ['00 A4 04 00 18' + '01 02 03 ... 16 17 18' + '00'] \rightarrow LT	Loop-back
20	PUT \leftarrow I(1) ₁ ['00 A4 04 00 47' + '01 02 03 ... 16 17 18'] \leftarrow LT	32 bytes frame
21	PUT \rightarrow R(ACK) ₀ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
22	PUT \leftarrow I(1) ₀ ['19 1A 1B ... 33 34 35'] \leftarrow LT	32 bytes frame
23	PUT \rightarrow R(ACK) ₁ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
24	PUT \leftarrow I(0) ₁ ['36 37 ... 46 47' + '00' + '90 00'] \leftarrow LT	24 bytes last Block of chain
25	PUT \rightarrow I(0) ₀ ['00 A4 04 00 47' + '01 02 03 ... 45 46 47' + '00'] \rightarrow LT	Loop-back
26	PUT \leftarrow I(1) ₀ ['00 A4 04 00 87' + '01 02 03 ... 36 37 38'] \leftarrow LT	64 bytes frame
27	PUT \rightarrow R(ACK) ₁ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
28	PUT \leftarrow I(1) ₁ ['39 3A 3B ... 73 74 75'] \leftarrow LT	64 bytes frame
29	PUT \rightarrow R(ACK) ₀ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
30	PUT \leftarrow I(0) ₀ ['76 77 78 ... 85 86 87' + '00' + '90 00'] \leftarrow LT	24 bytes last Block of chain
31	PUT \rightarrow I(0) ₁ ['00 A4 04 00 87' + '01 02 03 ... 85 86 87' + '00'] \rightarrow LT	Loop-back
32	PUT \leftarrow I(1) ₁ ['00 A4 04 00 F7' + '01 02 03 ... 76 77 78'] \leftarrow LT	128 bytes frame
33	PUT \rightarrow R(ACK) ₀ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
34	PUT \leftarrow I(1) ₀ ['79 7A 7B ... F3 F4 F5'] \leftarrow LT	128 bytes frame
35	PUT \rightarrow R(ACK) ₁ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
36	PUT \leftarrow I(1) ₁ [] \leftarrow LT	Empty I-block indicating chaining
37	PUT \rightarrow R(ACK) ₀ sent after FDT _{A,PCD,MIN} \rightarrow LT	Acknowledgment R-Block
38	PUT \leftarrow I(0) ₀ ['F6 F7' + '00' + '90 00'] \leftarrow LT	8 bytes frame

Step	Exchanges	Comments
39	PUT ▶ I(1)₁ ['00 A4 04 00 F7' + '01 02 03 ... F5 F6 F7' + '00'] ▶ LT	Loop-back (256 bytes indicating chaining block)
40	PUT ◀ R(ACK)₁ ▲ LT	Acknowledgment R-Block
41	PUT ▶ I(0)₀ [] ▶ LT	Empty I-block
42	PUT ◀ I(1)₀ ['00 A4 04 00 F8' + '01 02 03 ... F6 F7 F8'] ▲ LT	256 bytes chained block
43	PUT ▶ R(ACK)₁ sent after FDT_{A,PCD,MIN} ▶ LT	Acknowledgment R-Block
44	PUT ◀ I(0)₁ ['00' + '90 00'] ▲ LT	6 bytes frame
45	PUT ▶ I(1)₀ ['00 A4 04 00 F8' + '01 02 03 ... F6 F7 F8'] ▶ LT	Loop-back (256 bytes chained block)
46	PUT ◀ R(ACK)₀ ▲ LT	Acknowledgment R-Block
47	PUT ▶ I(0)₁ ['00'] ▶ LT	Loop-back (4 bytes frame)
48	PUT ◀ I(0)₁ ["EOT Command" + '90 00'] ▲ LT	End Of Test command
49	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) □ LT	PICC Reset
50	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
51	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
52	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC

**Scenario 20: Type A Error free chained I-Blocks in both directions for FSC = 256 bytes
(x=0 to 8, y=1)**

4.14.Type A Error free chained I-Blocks transmission for FSC = 16 to 128 bytes [TA203.xy]

Test codification:

TA203.xy

Test objective:

To ensure that the PCD accepts the values FSCI = '0' to '7' in the byte T0 of the ATS and is able to send chained I-Blocks respecting the corresponding values of FSC.

References Requirements:

4.7.4.1, 4.7.4.3, 10.1.1.1, 10.1.1.3, 10.3.2.2, 10.3.4.5

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Run y=0, if the PCD does not send empty I-Block after chained blocks (See ICS).

Run y=1, if the PCD may send empty I-blocks after a chain of I-Blocks (See ICS).

Procedure:

Run the following scenarios.

In this test, the following ATS shall be used:

	ATS						Maximum Frame Size for the PICC (FSC)
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
x=0	'05'	'72'	'80'	'40'	'02'	-	32 bytes
x=1	'05'	'73'	'80'	'40'	'02'	-	40 bytes
x=2	'05'	'74'	'80'	'40'	'02'	-	48 bytes
x=3	'05'	'75'	'80'	'40'	'02'	-	64 bytes
x=4	'05'	'76'	'80'	'40'	'02'	-	96 bytes
x=5	'05'	'77'	'80'	'40'	'02'	-	128 bytes
x=6	'01'	-	-	-	-	-	32 bytes
x=7	'05'	'70'	'80'	'40'	'02'	-	16 bytes
x=8	'05'	'71'	'80'	'40'	'02'	-	24 bytes

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenarios (the PUT uses chaining when sending an APDU too long to be transmitted within a frame of size FSC).

Failure action:

Proceed with the next test.

Scenarios:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ▲ '4E 23 7A 1B' + '0C' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '4E 23 7A 1B' + '0C'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ▲ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ▲ ATS with T0 = '72' or with no T0 byte	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ▲ I(0)₀ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00']	◀ LT
15	PUT ▶ I(1)₁ ['00 A4 04 00 3B' + '01 02 ... 18']	▶ LT 32 bytes frame
16	PUT ▲ R(ACK)₁	◀ LT Acknowledgment R-Block
17	PUT ▶ I(1)₀ ['19 1A 1B ... 33 34 35']	▶ LT 32 bytes frame
18	PUT ▲ R(ACK)₀	◀ LT Acknowledgment R-Block
19	PUT ▶ I(0)₁ ['36 37 38 39 3A 3B' + '00']	▶ LT 10 bytes frame
20	PUT ▲ I(0)₁ ['00 A4 04 00 34' + '01 02 ... 34' + '00' + '90 00']	◀ LT
21	PUT ▶ I(1)₀ ['00 A4 04 00 34' + '01 02 ... 18']	▶ LT 32 bytes frame
22	PUT ▲ R(ACK)₀	◀ LT Acknowledgment R-Block
23	PUT ▶ I(0)₁ ['19 1A 1B ... 33 34' + '00']	▶ LT 32 bytes frame
24	PUT ▲ I(0)₁ ["EOT Command" + '90 00']	◀ LT End Of Test command
25	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset

Step	Exchanges	Comments
26	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
27	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
28	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 21: Type A Error free chained I-Blocks transmission (FSC = 32 bytes; x=0 and 6, y=0)

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ▲ '4E 23 7A 1B' + '0C' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '4E 23 7A 1B' + '0C'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ▲ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ▲ ATS with T0 = '72' or with no T0 byte	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ▲ I(0)₀ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00']	◀ LT
15	PUT ▶ I(1)₁ ['00 A4 04 00 3B' + '01 02 ... 18']	▶ LT 32 bytes frame
16	PUT ▲ R(ACK)₁	◀ LT Acknowledgment R-Block
17	PUT ▶ I(1)₀ ['19 1A 1B ... 33 34 35']	▶ LT 32 bytes frame
18	PUT ▲ R(ACK)₀	◀ LT Acknowledgment R-Block
19	PUT ▶ I(0)₁ ['36 37 38 39 3A 3B' + '00']	▶ LT 10 bytes frame
20	PUT ▲ I(0)₁ ['00 A4 04 00 34' + '01 02 ... 34' + '00' + '90 00']	◀ LT
21	PUT ▶ I(1)₀ ['00 A4 04 00 34' + '01 02 ... 18']	▶ LT 32 bytes frame
22	PUT ▲ R(ACK)₀	◀ LT Acknowledgment R-Block
23	PUT ▶ I(1)₁ ['19 1A 1B ... 33 34' + '00']	▶ LT 32 bytes frame

Step	Exchanges	Comments
24	PUT ↳ R(ACK)₁	◀ LT Acknowledgment R-Block
25	PUT ↷ I(0)₀ []	▶ LT Empty I-Block
26	PUT ↳ I(0)₀ [“EOT Command” + ‘90 00’]	◀ LT End Of Test command
27	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
28	PUT ↷ ‘52’ (short frame)	▶ LT WUPA to poll for the PICC
29	PUT ↷ ‘52’ (short frame)	▶ LT WUPA to poll for the PICC
30	PUT ↷ ‘52’ (short frame)	▶ LT WUPA to poll for the PICC

Scenario 22: Type A Error free chained I-Blocks transmission (FSC = 32 bytes; x=0 and 6, y=1)

Step	Exchanges	Comments
1	PUT ↷ ‘52’ (short frame)	▶ LT WUPA during polling
2	PUT ↳ ‘01 00’ (no CRC_A)	◀ LT ATQA
3	PUT ↷ ‘50 00’	▶ LT HLTA
4	PUT ↷ ‘05 00 08’ (Type B frame)	▶ LT WUPB
5	PUT ↷ ‘52’ (short frame)	▶ LT WUPA
6	PUT ↳ ‘01 00’ (no CRC_A)	◀ LT ATQA
7	PUT ↷ ‘93 20’ (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ↳ ‘1C 8A 37 48’ + ‘E9’ (no CRC_A)	◀ LT UID
9	PUT ↷ ‘93 70’ + ‘1C 8A 37 48’ + ‘E9’	▶ LT SEL1 + UID CL1 + BCC
10	PUT ↳ ‘20’	◀ LT SAK
11	PUT ↷ ‘E0 80’	▶ LT RATS
12	PUT ↳ ATS with T0 = ‘73’	◀ LT ATS
13	PUT ↷ I(0)₀ [‘00 A4 04 00 0E’ + “2PAY.SYS.DDF01” + ‘00’]	▶ LT Select PPSE
14	PUT ↳ I(0)₀ [‘00 A4 04 00 50’ + ‘01 02 ... 50’ + ‘00’ + ‘90 00’]	◀ LT
15	PUT ↷ I(1)₁ [‘00 A4 04 00 50’ + ‘01 02 ... 19 20’]	▶ LT 40 bytes frame
16	PUT ↳ R(ACK)₁	◀ LT Acknowledgment R-Block
17	PUT ↷ I(1)₀ [‘21 22 23 ... 43 44 45’]	▶ LT 40 bytes frame
18	PUT ↳ R(ACK)₀	◀ LT Acknowledgment R-Block
19	PUT ↷ I(0)₁ [‘46 47 ... 4F 50’ + ‘00’]	▶ LT 15 bytes frame

Step	Exchanges	Comments
20	PUT ↳ I(0)₁ ['00 A4 04 00 44' + '01 02 ... 44' + '00' + '90 00'] ↲ LT	
21	PUT ↷ I(1)₀ ['00 A4 04 00 44' + '01 02 ... 19 20'] ↷ LT	40 bytes frame
22	PUT ↳ R(ACK)₀ ↲ LT	Acknowledgment R-Block
23	PUT ↷ I(0)₁ ['21 22 23 ... 43 44' + '00'] ↷ LT	40 bytes frame
24	PUT ↳ I(0)₁ ['EOT Command' + '90 00'] ↲ LT	End Of Test command
25	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
26	PUT ↷ '52' (short frame) ↷ LT	WUPA to poll for the PICC
27	PUT ↷ '52' (short frame) ↷ LT	WUPA to poll for the PICC
28	PUT ↷ '52' (short frame) ↷ LT	WUPA to poll for the PICC

Scenario 23: Type A Error free chained I-Blocks transmission (FSC = 40 bytes, x=1, y=0)

Step	Exchanges	Comments
1	PUT ↷ '52' (short frame) ↷ LT	WUPA during polling
2	PUT ↳ '01 00' (no CRC_A) ↲ LT	ATQA
3	PUT ↷ '50 00' ↷ LT	HLTA
4	PUT ↷ '05 00 08' (Type B frame) ↷ LT	WUPB
5	PUT ↷ '52' (short frame) ↷ LT	WUPA
6	PUT ↳ '01 00' (no CRC_A) ↲ LT	ATQA
7	PUT ↷ '93 20' (no CRC_A) ↷ LT	ANTICOLLISION CL1
8	PUT ↳ '1C 8A 37 48' + 'E9' (no CRC_A) ↲ LT	UID
9	PUT ↷ '93 70' + '1C 8A 37 48' + 'E9' ↷ LT	SEL1 + UID CL1 + BCC
10	PUT ↳ '20' ↲ LT	SAK
11	PUT ↷ 'E0 80' ↷ LT	RATS
12	PUT ↳ ATS with T0 = '73' ↲ LT	ATS
13	PUT ↷ I(0)₀ ['00 A4 04 00 0E' + '2PAY.SYS.DDF01' + '00'] ↷ LT	Select PPSE
14	PUT ↳ I(0)₀ ['00 A4 04 00 50' + '01 02 ... 50' + '00' + '90 00'] ↲ LT	
15	PUT ↷ I(1)₁ ['00 A4 04 00 50' + '01 02 ... 19 20'] ↷ LT	40 bytes frame
16	PUT ↳ R(ACK)₁ ↲ LT	Acknowledgment R-Block
17	PUT ↷ I(1)₀ ['21 22 23 ... 43 44 45'] ↷ LT	40 bytes frame

Step	Exchanges	Comments
18	PUT ↳ R(ACK)₀ ↲ LT	Acknowledgment R-Block
19	PUT ↷ I(0)₁ ['46 47 ... 4F 50' + '00'] ↷ LT	15 bytes frame
20	PUT ↳ I(0)₁ ['00 A4 04 00 44' + '01 02 ... 44' + '00' + '90 00'] ↲ LT	
21	PUT ↷ I(1)₀ ['00 A4 04 00 44' + '01 02 ... 19 20'] ↷ LT	40 bytes frame
22	PUT ↳ R(ACK)₀ ↲ LT	Acknowledgment R-Block
23	PUT ↷ I(1)₁ ['21 22 23 ... 43 44' + '00'] ↷ LT	40 bytes frame
24	PUT ↳ R(ACK)₁ ↲ LT	Acknowledgment R-Block
25	PUT ↷ I(0)₀ [] ↷ LT	Empty I-Block
26	PUT ↳ I(0)₀ ["EOT Command" + '90 00'] ↲ LT	End Of Test command
27	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) ↲ LT	PICC Reset
28	PUT ↷ '52' (short frame) ↷ LT	WUPA to poll for the PICC
29	PUT ↷ '52' (short frame) ↷ LT	WUPA to poll for the PICC
30	PUT ↷ '52' (short frame) ↷ LT	WUPA to poll for the PICC

Scenario 24: Type A Error free chained I-Blocks transmission (FSC = 40 bytes, x=1, y=1)

Step	Exchanges	Comments
1	PUT ↷ '52' (short frame) ↷ LT	WUPA during polling
2	PUT ↳ '01 00' (no CRC_A) ↲ LT	ATQA
3	PUT ↷ '50 00' ↷ LT	HLTA
4	PUT ↷ '05 00 08' (Type B frame) ↷ LT	WUPB
5	PUT ↷ '52' (short frame) ↷ LT	WUPA
6	PUT ↳ '01 00' (no CRC_A) ↲ LT	ATQA
7	PUT ↷ '93 20' (no CRC_A) ↷ LT	ANTICOLLISION CL1
8	PUT ↳ '95 CC 88 A9' + '78' (no CRC_A) ↲ LT	UID
9	PUT ↷ '93 70' + '95 CC 88 A9' + '78' ↷ LT	SEL1 + UID CL1 + BCC
10	PUT ↳ '20' ↲ LT	SAK
11	PUT ↷ 'E0 80' ↷ LT	RATS
12	PUT ↳ ATS with T0 = '74' ↲ LT	ATS
13	PUT ↷ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ↷ LT	Select PPSE

Step	Exchanges	Comments
14	PUT \leftarrow I(0) ₀ ['00 A4 04 00 60' + '01 02 ... 60' + '00' + '90 00'] \leftarrow LT	
15	PUT \rightarrow I(1) ₁ ['00 A4 04 00 60' + '01 02 ... 27 28'] \rightarrow LT	48 bytes frame
16	PUT \leftarrow R(ACK) ₁ \leftarrow LT	Acknowledgment R-Block
17	PUT \rightarrow I(1) ₀ ['29 2A 2B ... 53 54 55'] \rightarrow LT	48 bytes frame
18	PUT \leftarrow R(ACK) ₀ \leftarrow LT	Acknowledgment R-Block
19	PUT \rightarrow I(0) ₁ ['56 57 ... 5F 60' + '00'] \rightarrow LT	15 bytes frame
20	PUT \leftarrow I(0) ₁ ['00 A4 04 00 54' + '01 02 ... 54' + '00' + '90 00'] \leftarrow LT	
21	PUT \rightarrow I(1) ₀ ['00 A4 04 00 54' + '01 02 ... 27 28'] \rightarrow LT	48 bytes frame
22	PUT \leftarrow R(ACK) ₀ \leftarrow LT	Acknowledgment R-Block
23	PUT \rightarrow I(0) ₁ ['29 2A 2B ... 53 54' + '00'] \rightarrow LT	48 bytes frame
24	PUT \leftarrow I(0) ₁ ['EOT Command' + '90 00'] \leftarrow LT	End Of Test command
25	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) \rightarrow LT	PICC Reset
26	PUT \rightarrow '52' (short frame) \rightarrow LT	WUPA to poll for the PICC
27	PUT \rightarrow '52' (short frame) \rightarrow LT	WUPA to poll for the PICC
28	PUT \rightarrow '52' (short frame) \rightarrow LT	WUPA to poll for the PICC

Scenario 25: Type A Error free chained I-Blocks transmission (FSC = 48 bytes, x=2, y=0)

Step	Exchanges	Comments
1	PUT \rightarrow '52' (short frame) \rightarrow LT	WUPA during polling
2	PUT \leftarrow '01 00' (no CRC_A) \leftarrow LT	ATQA
3	PUT \rightarrow '50 00' \rightarrow LT	HLTA
4	PUT \rightarrow '05 00 08' (Type B frame) \rightarrow LT	WUPB
5	PUT \rightarrow '52' (short frame) \rightarrow LT	WUPA
6	PUT \leftarrow '01 00' (no CRC_A) \leftarrow LT	ATQA
7	PUT \rightarrow '93 20' (no CRC_A) \rightarrow LT	ANTICOLLISION CL1
8	PUT \leftarrow '95 CC 88 A9' + '78' (no CRC_A) \leftarrow LT	UID
9	PUT \rightarrow '93 70' + '95 CC 88 A9' + '78' \rightarrow LT	SEL1 + UID CL1 + BCC
10	PUT \leftarrow '20' \leftarrow LT	SAK
11	PUT \rightarrow 'E0 80' \rightarrow LT	RATS

Step	Exchanges	Comments
12	PUT \leftarrow ATS with T0 = '74'	\leftarrow LT ATS
13	PUT \rightarrow I(0) ₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	\rightarrow LT Select PPSE
14	PUT \leftarrow I(0) ₀ ['00 A4 04 00 60' + '01 02 ... 60' + '00' + '90 00']	\leftarrow LT
15	PUT \rightarrow I(1) ₁ ['00 A4 04 00 60' + '01 02 ... 27 28']	\rightarrow LT 48 bytes frame
16	PUT \leftarrow R(ACK) ₁	\leftarrow LT Acknowledgment R-Block
17	PUT \rightarrow I(1) ₀ ['29 2A 2B ... 53 54 55']	\rightarrow LT 48 bytes frame
18	PUT \leftarrow R(ACK) ₀	\leftarrow LT Acknowledgment R-Block
19	PUT \rightarrow I(0) ₁ ['56 57 ... 5F 60' + '00']	\rightarrow LT 15 bytes frame
20	PUT \leftarrow I(0) ₁ ['00 A4 04 00 54' + '01 02 ... 54' + '00' + '90 00']	\leftarrow LT
21	PUT \rightarrow I(1) ₀ ['00 A4 04 00 54' + '01 02 ... 27 28']	\rightarrow LT 48 bytes frame
22	PUT \leftarrow R(ACK) ₀	\leftarrow LT Acknowledgment R-Block
23	PUT \rightarrow I(1) ₁ ['29 2A 2B ... 53 54' + '00']	\rightarrow LT 48 bytes frame
24	PUT \leftarrow R(ACK) ₁	\leftarrow LT Acknowledgment R-Block
25	PUT \rightarrow I(0) ₀ []	\rightarrow LT Empty I-Block
26	PUT \leftarrow I(0) ₀ ["EOT Command" + '90 00']	\leftarrow LT End Of Test command
27	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
28	PUT \rightarrow '52' (short frame)	\rightarrow LT WUPA to poll for the PICC
29	PUT \rightarrow '52' (short frame)	\rightarrow LT WUPA to poll for the PICC
30	PUT \rightarrow '52' (short frame)	\rightarrow LT WUPA to poll for the PICC

Scenario 26: Type A Error free chained I-Blocks transmission (FSC = 48 bytes, x=2, y=1)

Step	Exchanges	Comments
1	PUT \rightarrow '52' (short frame)	\rightarrow LT WUPA during polling
2	PUT \leftarrow '01 00' (no CRC_A)	\leftarrow LT ATQA
3	PUT \rightarrow '50 00'	\rightarrow LT HLTA
4	PUT \rightarrow '05 00 08' (Type B frame)	\rightarrow LT WUPB
5	PUT \rightarrow '52' (short frame)	\rightarrow LT WUPA
6	PUT \leftarrow '01 00' (no CRC_A)	\leftarrow LT ATQA

Step	Exchanges	Comments
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ '9F 42 BB A2' + 'C4' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '9F 42 BB A2' + 'C4'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS with T0 = '75'	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ◀ I(0)₀ ['00 A4 04 00 7F' + '01 02 ... 7F' + '00' + '90 00']	◀ LT
15	PUT ▶ I(1)₁ ['00 A4 04 00 7F' + '01 02 ... 37 38']	▶ LT 64 bytes frame
16	PUT ◀ R(ACK)₁	◀ LT Acknowledgment R-Block
17	PUT ▶ I(1)₀ ['39 3A 3B ... 73 74 75']	▶ LT 64 bytes frame
18	PUT ◀ R(ACK)₀	◀ LT Acknowledgment R-Block
19	PUT ▶ I(0)₁ ['76 77 ... 7E 7F' + '00']	▶ LT 14 bytes frame
20	PUT ◀ I(0)₁ ['00 A4 04 00 74' + '01 02 ... 74' + '00' + '90 00']	◀ LT
21	PUT ▶ I(1)₀ ['00 A4 04 00 74' + '01 02 ... 37 38']	▶ LT 64 bytes frame
22	PUT ◀ R(ACK)₀	◀ LT Acknowledgment R-Block
23	PUT ▶ I(0)₁ ['39 3A 3B ... 73 74' + '00']	▶ LT 64 bytes frame
24	PUT ◀ I(0)₁ ["EOT Command" + '90 00']	◀ LT End Of Test command
25	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
26	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
27	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
28	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 27: Type A Error free chained I-Blocks transmission (FSC = 64 bytes, x=3, y=0)

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ '9F 42 BB A2' + 'C4' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '9F 42 BB A2' + 'C4'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS with T0 = '75'	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ◀ I(0)₀ ['00 A4 04 00 7F' + '01 02 ... 7F' + '00' + '90 00']	◀ LT
15	PUT ▶ I(1)₁ ['00 A4 04 00 7F' + '01 02 ... 37 38']	▶ LT 64 bytes frame
16	PUT ◀ R(ACK)₁	◀ LT Acknowledgment R-Block
17	PUT ▶ I(1)₀ ['39 3A 3B ... 73 74 75']	▶ LT 64 bytes frame
18	PUT ◀ R(ACK)₀	◀ LT Acknowledgment R-Block
19	PUT ▶ I(0)₁ ['76 77 ... 7E 7F' + '00']	▶ LT 14 bytes frame
20	PUT ◀ I(0)₁ ['00 A4 04 00 74' + '01 02 ... 74' + '00' + '90 00']	◀ LT
21	PUT ▶ I(1)₀ ['00 A4 04 00 74' + '01 02 ... 37 38']	▶ LT 64 bytes frame
22	PUT ◀ R(ACK)₀	◀ LT Acknowledgment R-Block
23	PUT ▶ I(1)₁ ['39 3A 3B ... 73 74' + '00']	▶ LT 64 bytes frame
24	PUT ◀ R(ACK)₁	◀ LT Acknowledgment R-Block
25	PUT ▶ I(0)₀ []	▶ LT Empty I-Block
26	PUT ◀ I(0)₀ ["EOT Command" + '90 00']	◀ LT End Of Test command
27	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
28	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
29	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Step	Exchanges	Comments
30	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 28: Type A Error free chained I-Blocks transmission (FSC = 64 bytes, x=3, y=1)

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ▲ '00 00 00 00' + '00' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '00 00 00 00' + '00'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ▲ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ▲ ATS with T0 = '76'	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ▲ I(0)₀ ['00 A4 04 00 BF' + '01 02 ... BF' + '00' + '90 00']	◀ LT
15	PUT ▶ I(1)₁ ['00 A4 04 00 BF' + '01 02 ... 57 58']	▶ LT 96 bytes frame
16	PUT ▲ R(ACK)₁	◀ LT Acknowledgment R-Block
17	PUT ▶ I(1)₀ ['59 5A 5B ... B3 B4 B5']	▶ LT 96 bytes frame
18	PUT ▲ R(ACK)₀	◀ LT Acknowledgment R-Block
19	PUT ▶ I(0)₁ ['B6 B7 ... BE BF' + '00']	▶ LT 14 bytes frame
20	PUT ▲ I(0)₁ ['00 A4 04 00 B4' + '01 02 ... B4' + '00' + '90 00']	◀ LT
21	PUT ▶ I(1)₀ ['00 A4 04 00 B4' + '01 02 ... 57 58']	▶ LT 96 bytes frame
22	PUT ▲ R(ACK)₀	◀ LT Acknowledgment R-Block
23	PUT ▶ I(0)₁ ['59 5A 5B ... B3 B4' + '00']	▶ LT 96 bytes frame
24	PUT ▲ I(0)₁ ["EOT Command" + '90 00']	◀ LT End Of Test command
25	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset

Step	Exchanges	Comments
26	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
27	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
28	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 29: Type A Error free chained I-Blocks transmission (FSC = 96 bytes, x=4, y=0)

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ▲ '00 00 00 00' + '00' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '00 00 00 00' + '00'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ▲ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ▲ ATS with T0 = '76'	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + '2PAY.SYS.DDF01' + '00']	▶ LT Select PPSE
14	PUT ▲ I(0)₀ ['00 A4 04 00 BF' + '01 02 ... BF' + '00' + '90 00']	◀ LT
15	PUT ▶ I(1)₁ ['00 A4 04 00 BF' + '01 02 ... 57 58']	▶ LT 96 bytes frame
16	PUT ▲ R(ACK)₁	◀ LT Acknowledgment R-Block
17	PUT ▶ I(1)₀ ['59 5A 5B ... B3 B4 B5']	▶ LT 96 bytes frame
18	PUT ▲ R(ACK)₀	◀ LT Acknowledgment R-Block
19	PUT ▶ I(0)₁ ['B6 B7 ... BE BF' + '00']	▶ LT 14 bytes frame
20	PUT ▲ I(0)₁ ['00 A4 04 00 B4' + '01 02 ... B4' + '00' + '90 00']	◀ LT
21	PUT ▶ I(1)₀ ['00 A4 04 00 B4' + '01 02 ... 57 58']	▶ LT 96 bytes frame
22	PUT ▲ R(ACK)₀	◀ LT Acknowledgment R-Block
23	PUT ▶ I(1)₁ ['59 5A 5B ... B3 B4' + '00']	▶ LT 96 bytes frame

Step	Exchanges	Comments
24	PUT ↳ R(ACK)₁	◀ LT Acknowledgment R-Block
25	PUT ↷ I(0)₀ []	▶ LT Empty I-Block
26	PUT ↳ I(0)₀ [“EOT Command” + ‘90 00’]	◀ LT End Of Test command
27	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
28	PUT ↷ ‘52’ (short frame)	▶ LT WUPA to poll for the PICC
29	PUT ↷ ‘52’ (short frame)	▶ LT WUPA to poll for the PICC
30	PUT ↷ ‘52’ (short frame)	▶ LT WUPA to poll for the PICC

Scenario 30: Type A Error free chained I-Blocks transmission (FSC = 96 bytes, x=4, y=1)

Step	Exchanges	Comments
1	PUT ↷ ‘52’ (short frame)	▶ LT WUPA during polling
2	PUT ↳ ‘01 00’ (no CRC_A)	◀ LT ATQA
3	PUT ↷ ‘50 00’	▶ LT HLTA
4	PUT ↷ ‘05 00 08’ (Type B frame)	▶ LT WUPB
5	PUT ↷ ‘52’ (short frame)	▶ LT WUPA
6	PUT ↳ ‘01 00’ (no CRC_A)	◀ LT ATQA
7	PUT ↷ ‘93 20’ (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ↳ ‘FF FF FF FF’ + ‘00’ (no CRC_A)	◀ LT UID
9	PUT ↷ ‘93 70’ + ‘FF FF FF FF’ + ‘00’	▶ LT SEL1 + UID CL1 + BCC
10	PUT ↳ ‘20’	◀ LT SAK
11	PUT ↷ ‘E0 80’	▶ LT RATS
12	PUT ↳ ATS with T0 = ‘77’	◀ LT ATS
13	PUT ↷ I(0)₀ [‘00 A4 04 00 0E’ + “2PAY.SYS.DDF01” + ‘00’]	▶ LT Select PPSE
14	PUT ↳ I(0)₀ [‘00 A4 04 00 F5’ + ‘01 02 ... F5’ + ‘00’ + ‘90 00’]	◀ LT 256 bytes non-chained block
15	PUT ↷ I(1)₁ [‘00 A4 04 00 F5’ + ‘01 02 ... 77 78’]	▶ LT 128 bytes frame
16	PUT ↳ R(ACK)₁	◀ LT Acknowledgment R-Block
17	PUT ↷ I(1)₀ [‘79 7A 7B ... F3 F4 F5’]	▶ LT 128 bytes frame
18	PUT ↳ R(ACK)₀	◀ LT Acknowledgment R-Block

Step	Exchanges	Comments
19	PUT ▶ I(0)₁ ['00'] ▶ LT	4 bytes frame
20	PUT ◀ I(0)₁ ['00 A4 04 00 F4' + '01 02 ... F4' + '00' + '90 00'] ◀ LT	
21	PUT ▶ I(1)₀ ['00 A4 04 00 F4' + '01 02 ... 77 78'] ▶ LT	128 bytes frame
22	PUT ◀ R(ACK)₀ ◀ LT	Acknowledgment R-Block
23	PUT ▶ I(0)₁ ['79 7A 7B ... F3 F4' + '00'] ▶ LT	128 bytes frame
24	PUT ◀ I(0)₁ ['EOT Command' + '90 00'] ◀ LT	End Of Test command
25	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) □ LT	PICC Reset
26	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
27	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
28	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC

Scenario 31: Type A Error free chained I-Blocks transmission (FSC = 128; x=5, y=0)

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ◀ 'FF FF FF FF' + '00' (no CRC_A) ◀ LT	UID
9	PUT ▶ '93 70' + 'FF FF FF FF' + '00' ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ◀ '20' ◀ LT	SAK
11	PUT ▶ 'E0 80' ▶ LT	RATS
12	PUT ◀ ATS with T0 = '77' ◀ LT	ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
14	PUT ◀ I(0)₀ ['00 A4 04 00 F5' + '01 02 ... F5' + '00' + '90 00'] ◀ LT	256 bytes non-chained block
15	PUT ▶ I(1)₁ ['00 A4 04 00 F5' + '01 02 ... 77 78'] ▶ LT	128 bytes frame
16	PUT ◀ R(ACK)₁ ◀ LT	Acknowledgment R-Block

Step	Exchanges	Comments
17	PUT ▶ I(1)₀ ['79 7A 7B ... F3 F4 F5'] ▶ LT	128 bytes frame
18	PUT ◀ R(ACK)₀ ▲ LT	Acknowledgment R-Block
19	PUT ▶ I(0)₁ ['00'] ▶ LT	4 bytes frame
20	PUT ◀ I(0)₁ ['00 A4 04 00 F4' + '01 02 ... F4' + '00' + '90 00'] ▲ LT	
21	PUT ▶ I(1)₀ ['00 A4 04 00 F4' + '01 02 ... 77 78'] ▶ LT	128 bytes frame
22	PUT ◀ R(ACK)₀ ▲ LT	Acknowledgment R-Block
23	PUT ▶ I(1)₁ ['79 7A 7B ... F3 F4' + '00'] ▶ LT	128 bytes frame
24	PUT ◀ R(ACK)₁ ▲ LT	Acknowledgment R-Block
25	PUT ▶ I(0)₀ [] ▶ LT	Empty I-Block
26	PUT ◀ I(0)₀ ["EOT Command" + '90 00'] ▲ LT	End Of Test command
27	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) □ LT	PICC Reset
28	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
29	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
30	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC

Scenario 32: Type A Error free chained I-Blocks transmission (FSC = 128; x=5, y=1)

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ◀ '01 00' (no CRC_A) ▲ LT	ATQA
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ◀ '01 00' (no CRC_A) ▲ LT	ATQA
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ◀ 'F1 8A 44 91' + 'AE' (no CRC_A) ▲ LT	UID
9	PUT ▶ '93 70' + 'F1 8A 44 91' + 'AE' ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ◀ '20' ▲ LT	SAK
11	PUT ▶ 'E0 80' ▶ LT	RATS
12	PUT ◀ ATS with T0 = '70' ▲ LT	ATS

Step	Exchanges	Comments
13	PUT ▶ I(1)₀ ['00 A4 04 00 0E' + "2PAY.SYS"] ▶ LT	Select PPSE (16 bytes frames)
14	PUT ◀ R(ACK)₀ ◀ LT	Acknowledgment R-Block
15	PUT ▶ I(0)₁ [".DDF01" + '00'] ▶ LT	Select PPSE (10 bytes frames)
16	PUT ◀ I(0)₁ ['00 A4 04 00 1C' + '01 02 ... 1C' + '00' + '90 00'] ◀ LT	
17	PUT ▶ I(1)₀ ['00 A4 04 00 1C' + '01 02 ... 08'] ▶ LT	16 bytes frame
18	PUT ◀ R(ACK)₀ ◀ LT	Acknowledgment R-Block
19	PUT ▶ I(1)₁ ['09 0A 0B ... 13 14 15'] ▶ LT	16 bytes frame
20	PUT ◀ R(ACK)₁ ◀ LT	Acknowledgment R-Block
21	PUT ▶ I(0)₀ ['16 17 18 19 1A 1B 1C' + '00'] ▶ LT	11 bytes frame
22	PUT ◀ I(0)₀ ['00 A4 04 00 14' + '01 02 ... 14' + '00' + '90 00'] ◀ LT	
23	PUT ▶ I(1)₁ ['00 A4 04 00 14' + '01 02 ... 08'] ▶ LT	16 bytes frame
24	PUT ◀ R(ACK)₁ ◀ LT	Acknowledgment R-Block
25	PUT ▶ I(0)₀ ['09 0A 0B ... 13 14' + '00'] ▶ LT	16 bytes frame
26	PUT ◀ I(0)₀ [".EOT Command" + '90 00'] ◀ LT	End Of Test command
27	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
28	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
29	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
30	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC

Scenario 33: Type A Error free chained I-Blocks transmission (FSC = 16; x=7, y=0)

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ◀ 'F1 8A 44 91' + 'AE' (no CRC_A) ◀ LT	UID
9	PUT ▶ '93 70' + 'F1 8A 44 91' + 'AE' ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ◀ '20' ◀ LT	SAK
11	PUT ▶ 'E0 80' ▶ LT	RATS
12	PUT ◀ ATS with T0 = '70' ◀ LT	ATS
13	PUT ▶ I(1)₀ ['00 A4 04 00 0E' + "2PAY.SYS"] ▶ LT	Select PPSE (16 bytes frames)
14	PUT ◀ R(ACK)₀ ◀ LT	Acknowledgment R-Block
15	PUT ▶ I(0)₁ [".DDF01" + '00'] ▶ LT	Select PPSE (10 bytes frames)
16	PUT ◀ I(0)₁ ['00 A4 04 00 1C' + '01 02 ... 1C' + '00' + '90 00'] ◀ LT	
17	PUT ▶ I(1)₀ ['00 A4 04 00 1C' + '01 02 ... 08'] ▶ LT	16 bytes frame
18	PUT ◀ R(ACK)₀ ◀ LT	Acknowledgment R-Block
19	PUT ▶ I(1)₁ ['09 0A 0B ... 13 14 15'] ▶ LT	16 bytes frame
20	PUT ◀ R(ACK)₁ ◀ LT	Acknowledgment R-Block
21	PUT ▶ I(0)₀ ['16 17 18 19 1A 1B 1C' + '00'] ▶ LT	11 bytes frame
22	PUT ◀ I(0)₀ ['00 A4 04 00 14' + '01 02 ... 14' + '00' + '90 00'] ◀ LT	
23	PUT ▶ I(1)₁ ['00 A4 04 00 14' + '01 02 ... 08'] ▶ LT	16 bytes frame
24	PUT ◀ R(ACK)₁ ◀ LT	Acknowledgment R-Block
25	PUT ▶ I(1)₀ ['09 0A 0B ... 13 14' + '00'] ▶ LT	16 bytes frame
26	PUT ◀ R(ACK)₀ ◀ LT	Acknowledgment R-Block
27	PUT ▶ I(0)₁ [] ▶ LT	Empty I-Block
28	PUT ◀ I(0)₁ ["EOT Command" + '90 00'] ◀ LT	End Of Test command

Step	Exchanges		Comments
29	PUT II	The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
30	PUT ▶ '52' (short frame)	▶ LT	WUPA to poll for the PICC
31	PUT ▶ '52' (short frame)	▶ LT	WUPA to poll for the PICC
32	PUT ▶ '52' (short frame)	▶ LT	WUPA to poll for the PICC

Scenario 34: Type A Error free chained I-Blocks transmission (FSC = 16; x=7, y=1)

Step	Exchanges		Comments
1	PUT ▶ '52' (short frame)	▶ LT	WUPA during polling
2	PUT ▲ '01 00' (no CRC_A)	◀ LT	ATQA
3	PUT ▶ '50 00'	▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT	WUPB
5	PUT ▶ '52' (short frame)	▶ LT	WUPA
6	PUT ▲ '01 00' (no CRC_A)	◀ LT	ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT	ANTICOLLISION CL1
8	PUT ▲ 'FF A8 32 22' + '47' (no CRC_A)	◀ LT	UID
9	PUT ▶ '93 70' + 'FF A8 32 22' + '47'	▶ LT	SEL1 + UID CL1 + BCC
10	PUT ▲ '20'	◀ LT	SAK
11	PUT ▶ 'E0 80'	▶ LT	RATS
12	PUT ▲ ATS with T0 = '71'	◀ LT	ATS
13	PUT ▶ I(0)0 ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT	Select PPSE
14	PUT ▲ I(0)0 ['00 A4 04 00 2B' + '01 02 ... 2B' + '00' + '90 00']	◀ LT	
15	PUT ▶ I(1)1 ['00 A4 04 00 2B' + '01 02 ... 0F 10']	▶ LT	24 bytes frame
16	PUT ▲ R(ACK)1	◀ LT	Acknowledgment R-Block
17	PUT ▶ I(1)0 ['11 12 13 ... 23 24 25']	▶ LT	24 bytes frame
18	PUT ▲ R(ACK)0	◀ LT	Acknowledgment R-Block
19	PUT ▶ I(0)1 ['26 27 28 29 2A 2B' + '00']	▶ LT	10 bytes frame
20	PUT ▲ I(0)1 ['00 A4 04 00 24' + '01 02 ... 24' + '00' + '90 00']	◀ LT	
21	PUT ▶ I(1)0 ['00 A4 04 00 24' + '01 02 ... 0F 10']	▶ LT	24 bytes frame
22	PUT ▲ R(ACK)0	◀ LT	Acknowledgment R-Block

Step	Exchanges	Comments
23	PUT ▶ I(0)₁ ['11 12 13 ... 23 24' + '00'] ▶ LT	24 bytes frame
24	PUT ◀ I(0)₁ ['"EOT Command" + '90 00'] ◀ LT	End Of Test command
25	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) □ LT	PICC Reset
26	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
27	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
28	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC

Scenario 35: Type A Error free chained I-Blocks transmission (FSC = 24; x=8, y=0)

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ◀ 'FF A8 32 22' + '47' (no CRC_A) ◀ LT	UID
9	PUT ▶ '93 70' + 'FF A8 32 22' + '47' ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ◀ '20' ◀ LT	SAK
11	PUT ▶ 'E0 80' ▶ LT	RATS
12	PUT ◀ ATS with T0 = '71' ◀ LT	ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
14	PUT ◀ I(0)₀ ['00 A4 04 00 2B' + '01 02 ... 2B' + '00' + '90 00'] ◀ LT	
15	PUT ▶ I(1)₁ ['00 A4 04 00 2B' + '01 02 ... 0F 10'] ▶ LT	24 bytes frame
16	PUT ◀ R(ACK)₁ ◀ LT	Acknowledgment R-Block
17	PUT ▶ I(1)₀ ['11 12 13 ... 23 24 25'] ▶ LT	24 bytes frame
18	PUT ◀ R(ACK)₀ ◀ LT	Acknowledgment R-Block
19	PUT ▶ I(0)₁ ['26 27 28 29 2A 2B' + '00'] ▶ LT	10 bytes frame
20	PUT ◀ I(0)₁ ['00 A4 04 00 24' + '01 02 ... 24' + '00' + '90 00'] ◀ LT	
21	PUT ▶ I(1)₀ ['00 A4 04 00 24' + '01 02 ... 0F 10'] ▶ LT	24 bytes frame

Step	Exchanges	Comments
22	PUT ↣ R(ACK)₀ ↪ LT	Acknowledgment R-Block
23	PUT ↢ I(1)₁ ['11 12 13 ... 23 24' + '00'] ↢ LT	24 bytes frame
24	PUT ↣ R(ACK)₁ ↪ LT	Acknowledgment R-Block
25	PUT ↢ I(0)₀ [] ↢ LT	Empty I-Block
26	PUT ↣ I(0)₀ ['EOT Command' + '90 00'] ↪ LT	End Of Test command
27	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) ↪ LT	PICC Reset
28	PUT ↢ '52' (short frame) ↢ LT	WUPA to poll for the PICC
29	PUT ↢ '52' (short frame) ↢ LT	WUPA to poll for the PICC
30	PUT ↢ '52' (short frame) ↢ LT	WUPA to poll for the PICC

Scenario 36: Type A Error free chained I-Blocks transmission (FSC = 24; x=8, y=1)

4.15.Type A Error free request for Frame Waiting Time Extension on non-chained I-Blocks [TA204]

Test codification:

TA204

Test objective:

To ensure that the PCD correctly manages a request for Frame Waiting Time Extension received in response to an I-Block not indicating chaining.

References Requirements:

10.2.2.1, 10.2.2.3, 10.2.2.5, 10.2.2.7, 10.3.4.2, 10.1.2.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

After each S(WTX) Response block, the LT replies using the Frame Delay Time $FDT_{A,PICC,EXT}$ between the end of the S(WTX) Response sequence sent by the PUT and the beginning of the sequence containing the next block sent by the LT.

In this test:

- $FDT_{A,PICC,EXT} = FWT_{TEMP} + \Delta FWT = [(FWT \times WTXM) + \Delta FWT] = [(4096 \times WTXM) + 49152] \times 1/f_c$ if $WTXM \leq 59$, as $FWT = 4096 \times 1/f_c$ and $\Delta FWT = 49152 \times 1/f_c$

And:

- $FDT_{A,PICC,EXT} = FWT_{TEMP} + \Delta FWT - 128/f_c + 20/f_c [-1/f_c; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PUT is $(0)_b$
- $FDT_{A,PICC,EXT} = FWT_{TEMP} + \Delta FWT - 128/f_c + 84/f_c [-1/f_c; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PUT is $(1)_b$

When the sequences sent by the LT are followed by a sequence sent by the PUT containing S(WTX) Responses, the LT measures the delay between the end of the sequence sent by the LT and the beginning of the sequence replied by the PUT

In this test, the following ATS shall be used:

ATS						FWT+ΔFWT
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'00'	'02'	-	$53248 \times 1/f_c$

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (each time the LT sends a S(WTX) Request, the PUT correctly grants the Frame Waiting Time Extension).

On reception of an S(WTX) Block, the PUT replies with an S(WTX) Block having a PCB field (i.e. first byte of the Block) equal to $('F2')_h$ (i.e. b2 of S-Block PCB is set to $(1)_b$).

The delay between the end of a sequence sent by the LT and the beginning of the sequence replied by the PUT containing a S(WTX) Response is at least FDT_{A,PCD,MIN}.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ◀ '3A BF 78 5C' + 'A1' (no CRC_A) ◀ LT	UID
9	PUT ▶ '93 70' + '3A BF 78 5C' + 'A1' ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ◀ '20' ◀ LT	SAK
11	PUT ▶ 'E0 80' ▶ LT	RATS
12	PUT ◀ ATS ◀ LT	ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
14	PUT ◀ I(0)₀ ['00 B2 01 04 00' + '90 00'] ◀ LT	
15	PUT ▶ I(0)₁ ['00 B2 01 04 00'] ▶ LT	Loop-back
16	PUT ◀ S(WTX Request) [WTXM='02'] ◀ LT	WTXM = 2
17	PUT ▶ S(WTX Response) [WTXM='02'] sent after FDT _{A,PCD,MIN} ▶ LT	WTX acknowledgment
18	PUT ◀ I(0)₁ ['00 A4 04 00 05' + '01 02 ... 05' + '00' + '90 00'] ◀ LT sent using FDT _{A,PICC,EXT} with WTXM = 2	
19	PUT ▶ I(0)₀ ['00 A4 04 00 05' + '01 02 ... 05' + '00'] ▶ LT	Loop-back (14 bytes frame)
20	PUT ◀ I(0)₀ ['00 A4 04 00 05' + '06 07 ... 0A' + '00' + '90 00'] ◀ LT	
21	PUT ▶ I(0)₁ ['00 A4 04 00 05' + '06 07 ... 0A' + '00'] ▶ LT	Loop-back (14 bytes frame)
22	PUT ◀ S(WTX Request) [WTXM='1B'] ◀ LT	WTXM = 27
23	PUT ▶ S(WTX Response) [WTXM='1B'] sent after FDT _{A,PCD,MIN} ▶ LT	WTX acknowledgment
24	PUT ◀ S(WTX Request) [WTXM='1B'] ◀ LT	WTXM = 27
25	PUT ▶ S(WTX Response) [WTXM='1B'] sent after FDT _{A,PCD,MIN} ▶ LT	WTX acknowledgment

Step	Exchanges	Comments
26	PUT ↘ S(WTX Request) [WTXM='1B'] ↗ LT	WTXM = 27
27	PUT ↗ S(WTX Response) [WTXM='1B'] sent after FDT_{A,PCD,MIN} ↘ LT	WTX acknowledgment
28	PUT ↘ S(WTX Request) [WTXM='1B'] ↗ LT	WTXM = 27
29	PUT ↗ S(WTX Response) [WTXM='1B'] sent after FDT_{A,PCD,MIN} ↘ LT	WTX acknowledgment
30	PUT ↘ S(WTX Request) [WTXM='1B'] ↗ LT	WTXM = 27
31	PUT ↗ S(WTX Response) [WTXM='1B'] sent after FDT_{A,PCD,MIN} ↘ LT	WTX acknowledgment
32	PUT ↘ S(WTX Request) [WTXM='1B'] ↗ LT	WTXM = 27
33	PUT ↗ S(WTX Response) [WTXM='1B'] sent after FDT_{A,PCD,MIN} ↘ LT	WTX acknowledgment
34	PUT ↘ S(WTX Request) [WTXM='1B'] ↗ LT	WTXM = 27
35	PUT ↗ S(WTX Response) [WTXM='1B'] sent after FDT_{A,PCD,MIN} ↘ LT	WTX acknowledgment
36	PUT ↘ I(0)₁ ['00 A4 04 00 05+ '0B 0C ... 0F' + '00' + '90 00'] sent using FDT _{A,PICC,EXT} with WTXM = 27 ↗ LT	
37	PUT ↗ I(0)₀ ['00 A4 04 00 05+ '0B 0C ... 0F' + '00'] ↘ LT	Loop-back (14 bytes frame)
38	PUT ↘ I(0)₀ ['00 A4 04 00 05' + '11 12 ... 15' + '00' + '90 00'] ↗ LT	
39	PUT ↗ I(0)₁ ['00 A4 04 00 05' + '11 12 ... 15' + '00'] ↘ LT	Loop-back (14 bytes frame)
40	PUT ↘ S(WTX Request) [WTXM='3B'] ↗ LT	WTXM = 59
41	PUT ↗ S(WTX Response) [WTXM='3B'] sent after FDT_{A,PCD,MIN} ↘ LT	WTX acknowledgment
42	PUT ↘ I(0)₁ ['00 A4 04 00 05+ '16 17 ... 1A' + '00' + '90 00'] sent using FDT _{A,PICC,EXT} with WTXM = 59 ↗ LT	
43	PUT ↗ I(0)₀ ['00 A4 04 00 05+ '16 17 ... 1A' + '00'] ↘ LT	Loop-back (14 bytes frame)
44	PUT ↘ I(0)₀ ['00 A4 04 00 05' + '1B 1C ... 1F' + '00' + '90 00'] ↗ LT	
45	PUT ↗ I(0)₁ ['00 A4 04 00 05' + '1B 1C ... 1F' + '00'] ↘ LT	Loop-back (14 bytes frame)
46	PUT ↘ S(WTX Request) [WTXM='12'] ↗ LT	WTXM = 18
47	PUT ↗ S(WTX Response) [WTXM='12'] sent after FDT_{A,PCD,MIN} ↘ LT	WTX acknowledgment
48	PUT ↘ I(0)₁ ['00 A4 04 00 05+ '20 21 ... 24' + '00' + '90 00'] sent using FDT _{A,PICC,EXT} with WTXM = 18 ↗ LT	
49	PUT ↗ I(0)₀ ['00 A4 04 00 05+ '20 21 ... 24' + '00'] ↘ LT	Loop-back (14 bytes frame)
50	PUT ↘ I(0)₀ ['00 A4 04 00 05' + '25 26 ... 29' + '00' + '90 00'] ↗ LT	

Step	Exchanges	Comments
51	PUT ▶ I(0)₁ ['00 A4 04 00 05' + '25 26 ... 29' + '00'] ▶ LT	Loop-back (14 bytes frame)
52	PUT ◀ I(0)₁ ["EOT Command" + '90 00'] ◀ LT	End Of Test command
53	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
54	PUT ▶ '52' (<i>short frame</i>) ▶ LT	WUPA to poll for the PICC
55	PUT ▶ '52' (<i>short frame</i>) ▶ LT	WUPA to poll for the PICC
56	PUT ▶ '52' (<i>short frame</i>) ▶ LT	WUPA to poll for the PICC

Scenario 37: Type A Error free request for Frame Waiting Time Extension on non-chained I-Blocks

4.16.Type A Error free request for Frame Waiting Time Extension during chaining in both directions [TA205]

Test codification:

TA205

Test objective:

To ensure that the PCD correctly manages a request for Frame Waiting Time Extension received in response to an R(ACK) Block or to an I-Block indicating chaining.

References Requirements:

10.2.2.1, 10.2.2.3, 10.2.2.5, 10.2.2.7, 10.3.4.2, 10.1.2.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

After each S(WTX) Response block, the LT replies using the Frame Delay Time $FDT_{A,PICC,EXT}$ between the end of the S(WTX) Response sequence sent by the PUT and the beginning of the sequence containing the next block sent by the LT.

In this test:

- $FDT_{A,PICC,EXT} = [(4096 \times WTXM) + 49152] \times 1/f_c - 128/f_c + 20/f_c [-1/f_c; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PUT is $(0)_b$
- $FDT_{A,PICC,EXT} = [(4096 \times WTXM) + 49152] \times 1/f_c - 128/f_c + 84/f_c [-1/f_c; +0.4 \mu s + 1/f_c]$ if the last bit transmitted by the PUT is $(1)_b$

As:

- $FWT = 4096 \times 1/f_c$
- and $\Delta FWT = 49152 \times 1/f_c$

In this test, the following ATS shall be used:

ATS						(FWT+ΔFWT)
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'00'	'02'	-	$53248 \times 1/f_c$

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (each time the LT sends a S(WTX) Request, the PUT correctly grants the Frame Waiting Time Extension).

On reception of an S(WTX) Block, the PUT replies with an S(WTX) Block having a PCB field (i.e. first byte of the Block) equal to $('F2')_h$ (i.e. b2 of S-Block PCB is set to $(1)_b$).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ '3A BF 78 5C' + 'A1' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '3A BF 78 5C' + 'A1'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + '2PAY.SYS.DDF01' + '00']	▶ LT Select PPSE
14	PUT ◀ I(1)₀ ['00 A4 04 00 39' + '51 52 53 ... 56 57 58']	◀ LT
15	PUT ▶ R(ACK)₁	▶ LT Acknowledgment R-Block
16	PUT ◀ S(WTX Request) [WTXM='05']	◀ LT WTXM = 5
17	PUT ▶ S(WTX Response) [WTXM='05']	▶ LT WTX acknowledgment
18	PUT ◀ I(1)₁ ['59 5A 5B ... 63 64 65'] sent using FDT _{A,PICC,EXT} with WTXM = 5	◀ LT
19	PUT ▶ R(ACK)₀	▶ LT Acknowledgment R-Block
20	PUT ◀ S(WTX Request) [WTXM='11']	◀ LT WTXM = 17
21	PUT ▶ S(WTX Response) [WTXM='11']	▶ LT WTX acknowledgment
22	PUT ◀ I(1)₀ ['66 67 68 ... 70 71 72'] sent using FDT _{A,PICC,EXT} with WTXM = 17	◀ LT
23	PUT ▶ R(ACK)₁	▶ LT Acknowledgment R-Block
24	PUT ◀ S(WTX Request) [WTXM='21']	◀ LT WTXM = 33
25	PUT ▶ S(WTX Response) [WTXM='21']	▶ LT WTX acknowledgment
26	PUT ◀ I(1)₁ ['73 74 75 ... 7D 7E 7F'] sent using FDT _{A,PICC,EXT} with WTXM = 33	◀ LT
27	PUT ▶ R(ACK)₀	▶ LT Acknowledgment R-Block
28	PUT ◀ S(WTX Request) [WTXM='2F']	◀ LT WTXM = 47

Step	Exchanges	Comments
29	PUT ▶ S(WTX Response) [WTXM='2F'] ▶ LT	WTX acknowledgment
30	PUT ↲ I(0)₀ ['80 81 82 ... 87 88 89' + '00' + '90 00'] sent using FDT_{A,PICC,EXT} with WTXM = 47 ↲ LT	
31	PUT ▶ I(1)₁ ['00 A4 04 00 39'+ '51 52 ... 67 68'] ▶ LT	Loop-back (32 bytes frame)
32	PUT ↲ S(WTX Request) [WTXM='07'] ↲ LT	WTXM = 7
33	PUT ▶ S(WTX Response) [WTXM='07'] ▶ LT	WTX acknowledgment
34	PUT ↲ R(ACK)₁ sent using FDT_{A,PICC,EXT} with WTXM = 7 ↲ LT	
35	PUT ▶ I(1)₀ ['69 6A 6B ... 83 84 85'] ▶ LT	Loop-back (32 bytes frame)
36	PUT ↲ S(WTX Request) [WTXM='32'] ↲ LT	WTXM = 50
37	PUT ▶ S(WTX Response) [WTXM='32'] ▶ LT	WTX acknowledgment
38	PUT ↲ R(ACK)₀ sent using FDT_{A,PICC,EXT} with WTXM = 50 ↲ LT	
39	PUT ▶ I(0)₁ ['86 87 88 89' + '00'] ▶ LT	Loop-back (8 bytes frame)
40	PUT ↲ I(0)₁ ['EOT Command' + '90 00'] ↲ LT	End Of Test command
41	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
42	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
43	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
44	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC

Scenario 38: Type A Error free request for Frame Waiting Time Extension during chaining in both directions

4.17.Type A Error free chained I-Blocks reception with rare frame sizes [TA210]

Test codification:

TA210

Test objective:

To ensure that the PCD is able to correctly receive and acknowledge chained I-Blocks of rare sizes (i.e. block sizes different from the ISO 14443 values of FSD and not constant within a single chain).

References Requirements:

10.1.1.3, 10.3.2.1

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

In this test, the following ATS shall be used:

ATS						Maximum Frame Size for the PICC (FSC)
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'78'	'80'	'40'	'02'	-	256 bytes

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to all the received chained I-Blocks).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ 'BB 15 AB 18' + '1D' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + 'BB 15 AB 18' + '1D'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + '2PAY.SYS.DDF01' + '00']	▶ LT Select PPSE
14	PUT ◀ I(1)₀ ['00 A4 04 00 40' + '01 02 03']	◀ LT 11 bytes frame
15	PUT ▶ R(ACK)₁	▶ LT Acknowledgment R-Block
16	PUT ◀ I(1)₁ ['04 05 06 ... 1F 20 21']	◀ LT 33 bytes frame
17	PUT ▶ R(ACK)₀	▶ LT Acknowledgment R-Block
18	PUT ◀ I(1)₀ ['22']	◀ LT 4 bytes frame
19	PUT ▶ R(ACK)₁	▶ LT Acknowledgment R-Block
20	PUT ◀ I(1)₁ ['23 24 25 ... 38 39 3A']	◀ LT 27 bytes frame
21	PUT ▶ R(ACK)₀	▶ LT Acknowledgment R-Block
22	PUT ◀ I(1)₀ ['3B 3C 3D 3E 3F']	◀ LT 8 bytes frame
23	PUT ▶ R(ACK)₁	▶ LT Acknowledgment R-Block
24	PUT ◀ I(1)₁ ['40' + '00' + '90']	◀ LT 6 bytes frame
25	PUT ▶ R(ACK)₀	▶ LT Acknowledgment R-Block
26	PUT ◀ I(0)₀ ['00']	◀ LT 4 bytes last Block of chain
27	PUT ▶ I(0)₁ ['00 A4 04 00 40' + '01 02 03 ... 3E 3F 40' + '00']	▶ LT Loop-back (73 bytes)
28	PUT ◀ I(1)₁ ['00 A4 04 00 87' + '01 02 03 ... 40 41 42']	◀ LT 74 bytes frame

Step	Exchanges	Comments
29	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgment R-Block
30	PUT ◀ I(1)₀ ['43 44'] ◀ LT	5 bytes frame
31	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgment R-Block
32	PUT ◀ I(1)₁ ['45 46 47 ... 6A 6B 6C'] ◀ LT	43 bytes frame
33	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgment R-Block
34	PUT ◀ I(1)₀ ['6D 6E 6F ... 72 73 74'] ◀ LT	11 bytes frame
35	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgment R-Block
36	PUT ◀ I(1)₁ ['75 76 77 ... 85 86 87'] ◀ LT	22 bytes frame
37	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgment R-Block
38	PUT ◀ I(0)₀ ['00' + '90 00'] ◀ LT	6 bytes last Block of chain
39	PUT ▶ I(0)₁ ['00 A4 04 00 87' + '01 02 03 ... 85 86 87' + '00'] ▶ LT	Loop-back (144 bytes)
40	PUT ◀ I(0)₁ ['EOT Command' + '90 00'] ◀ LT	End Of Test command
41	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
42	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
43	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
44	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC

Scenario 39: Type A Error free chained I-Blocks reception with rare frame sizes

4.18.Type A Error free exchange with the minimum Frame Delay Time PCD→PICC for different values of the Frame Waiting Time [TA215.x]

Test codification:

TA215.x

Test objective:

To ensure that the PCD accepts sequences received with the minimum Frame Delay Time $FDT_{A,PICC,MIN}$ for all possible values of the Frame Waiting Time (FWT).

References Requirement:

4.8.1.1

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

After reception of the RATS command and until the End Of Test command (included), the LT replies to all commands and blocks using the minimum Frame Delay Time $FDT_{A,PICC,MIN}$ between the end of the sequence sent by the PUT and the beginning of the sequence replied by the LT.

Remark: before reception of the RATS command, the LT uses the default Frame Delay Time $FDT_{A,PICC,ANTICOLLISION}$.

In this test, the following ATS and Frame Waiting Time shall be used:

ATS						FWT+ΔFWT
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'00'	'02'	-	$53248 \times 1/f_c$
'05'	'72'	'80'	'80'	'02'	-	$1097728 \times 1/f_c$
'05'	'72'	'80'	'E0'	'02'		$67158016 \times 1/f_c$

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to the sequences sent by the LT with the minimum Frame Delay Time).

Failure action:

Proceed with next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ▲ '56 F1 23 DD' + '59' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '56 F1 23 DD' + '59'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ▲ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ▲ ATS sent using FDT _{A,PICC,MIN}	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ▲ I(0)₀ ['00 B2 05 04 00' + '90 00'] sent using FDT _{A,PICC,MIN}	◀ LT
15	PUT ▶ I(0)₁ ['00 B2 05 04 00']	▶ LT Loop-back
16	PUT ▲ I(0)₁ ['00 B2 06 04 00' + '90 00'] sent using FDT _{A,PICC,MIN}	◀ LT
17	PUT ▶ I(0)₀ ['00 B2 06 04 00']	▶ LT Loop-back
18	PUT ▲ I(0)₀ ['00 A4 04 00 17' + '2F 30 ... 45' + '00' + '90 00'] sent using FDT _{A,PICC,MIN}	◀ LT
19	PUT ▶ I(0)₁ ['00 A4 04 00 17' + '2F 30 ... 45' + '00']	▶ LT Loop-back (32 bytes frame)
20	PUT ▲ I(0)₁ ['00 B2 07 04 00' + '90 00'] sent using FDT _{A,PICC,MIN}	◀ LT
21	PUT ▶ I(0)₀ ['00 B2 07 04 00']	▶ LT Loop-back
22	PUT ▲ I(0)₀ ['00 B2 08 04 00' + '90 00'] sent using FDT _{A,PICC,MIN}	◀ LT
23	PUT ▶ I(0)₁ ['00 B2 08 04 00']	▶ LT Loop-back
24	PUT ▲ I(0)₁ ['00 A4 04 00 17' + '46 47 ... 5C' + '00' + '90 00'] sent using FDT _{A,PICC,MIN}	◀ LT
25	PUT ▶ I(0)₀ ['00 A4 04 00 17' + '46 47 ... 5C' + '00']	▶ LT Loop-back (32 bytes frame)

Step	Exchanges	Comments
26	PUT ↪ I(0)₀ ["EOT Command" + '90 00'] sent using FDT_{A,PICC,MIN} ↪ LT	End Of Test command
27	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) ↩ LT	PICC Reset
28	PUT ↪ '52' (short frame) ↩ LT	WUPA to poll for the PICC
29	PUT ↪ '52' (short frame) ↩ LT	WUPA to poll for the PICC
30	PUT ↪ '52' (short frame) ↩ LT	WUPA to poll for the PICC

**Scenario 40: Type A Error free exchange with the minimum Frame Delay Time
PCD→PICC for different values of the Frame Waiting Time (x=0 to 2)**

4.19.Type A Polling with an error after WUPA [TA301.xy]

Test codification:

TA301.xy

Test objective:

To ensure that the PCD detects a Type A PICC and initiates a Type A transaction when it receives an error in response to the WUPA command sent during polling.

References Requirements:

4.7.1.3, 5.1.1.1, 6.1.1.1, 9.2.1.3, 9.6.1.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

During the polling procedure, the LT replies to the WUPA command sent by the PUT with an ATQA with error.

The following transmission errors on ATQA are generated successively by the LT:

- xy=00: ATQA with the carrier modulated with the subcarrier for the whole bit duration (equivalent to the result of the merging of two complementary bit patterns when 2 Type A cards are presented simultaneously to the PCD)
- xy=01: ATQA with parity error (corrupted parity bit) on the first byte of the frame

The following protocol errors are generated successively by the LT:

- xy=13: 1 byte long ATQA (too short ATQA)
- xy=14: ATQA in a Type A frame with 2 CRC_A bytes (i.e. too long ATQA)
- xy=15: ATQA= '01 F0'
- xy=16: SAK = '20'

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT continues polling upon receipt of an ATQA with error and then starts the Type A collision detection procedure).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	Error in function of 'xy' For x=0: ATQA = '01 00' (no CRC_A) with a transmission error in function of 'y' PUT ↲ For xy=13: ATQA = '01' (no CRC_A) ▲ LT For xy=14: ATQA = '01 00' (with CRC_A) For xy=15: ATQA = '01 F0' (no CRC_A) For xy=16: SAK = '20'	Error in function of 'xy'
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ↲ '01 00' (no CRC_A) ▲ LT	ATQA
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ↲ '22 29 FE FE' + '0B' (no CRC_A) ▲ LT	UID
9	PUT ▶ '93 70' + '22 29 FE FE' + '0B' ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ↲ '20' ▲ LT	SAK
11	PUT ▶ 'E0 80' ▶ LT	RATS
12	PUT ↲ ATS ▲ LT	ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
14	PUT ↲ I(0)₀ ["EOT Command" + '90 00'] ▲ LT	End Of Test command
15	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) □ LT	PICC Reset
16	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
17	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
18	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC

Scenario 41: Type A Collision Detection with an error after WUPA (xy=00, 01 and 13 to 16)

4.20. Type A Collision detection with an error after ANTCOLLISION CL1 [TA302.xy]

Test codification:

TA302.xy

Test objective:

To ensure that the PCD behaves correctly when it receives an error in response to the ANTCOLLISION CL1 command sent during collision detection.

References Requirements:

4.7.1.3, 4.8.1.3, 5.1.1.1, 5.4.2.1, 9.3.2.2, 9.6.1.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT measures the delay between the beginning of the sequence with error and the beginning of the PICC Reset.

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

The following transmission errors on UID CL1 are generated successively by the LT:

- xy=00: UID CL1 with the carrier modulated with the subcarrier for a whole bit duration (equivalent to the result of the merging of two complementary bit patterns when 2 Type A cards are presented simultaneously to the PCD)
- xy=01: UID CL1 with parity error (corrupted parity bit) on the 5th byte (last byte) of the frame
- xy=02: UID CL1 with a wrong check byte BCC
- xy=03: UID CL1 with parity error/wrong BCC combination
- xy=04: UID CL1 sent using a Frame Delay Time $FDT_{A,PICC} = (FDT_{A,PICC,ANTICOLLISION} - 256/f_c)$ between the end of the ANTCOLLISION CL1 sequence and the beginning of the UID CL1 sequence
- xy=05: UID CL1 with bit collision on b₃ of 2nd byte, on parity bit of 2nd byte, on b₃ of BCC and parity bit of BCC.
- xy=07: UID CL1 with 5 bits in the BCC (instead of 8 + parity)

The following protocol errors are generated successively by the LT:

- xy=11: 4 bytes long UID CL1 (too short UID CL1)
- xy=12: UID CL1 in a Type A frame with 2 CRC_A bytes (too long UID CL1)
- xy=13: SAK = '20'

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT performs a PICC Reset when it detects an error after ANTCOLLISION CL1).

The delay between the beginning of the sequence with error and the beginning of the PICC Reset is at most $t_{RESETDELAY}$.

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$.

Following the PICC Reset, the PUT restarts the initial polling procedure by sending a WUPA command followed by a WUPB command both preceded by a delay of at least $t_{P,MIN}$ and at most $t_{P,MAX}$ with carrier on (i.e. returns to step 1 of the Scenario of the Test Case TC001).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	Error in function of 'xy' For xy=00, 01, 04, 05, 07: UID CL1 = '27 E9 3B 11' + 'E4' (no CRC_A) with a transmission error in function of 'y' PUT ◀ For xy=02, 03: UID CL1 = '27 E9 3B 11' + 'FF' (no CRC_A) ◀ LT with a transmission error in function of 'y' For xy=11: UID CL1 = 'F3 56 3A' + '9F' (no CRC_A) For xy=12: UID CL1 = '27 E9 3B 11' + 'E4' (with CRC_A) For xy=13: SAK = '20'	Error in function of 'xy'
9	PUT II The PUT stops sending the carrier within $t_{RESETDELAY}$ The PUT keeps the carrier off during at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$ II LT	PICC Reset
The PUT restarts the initial polling procedure i.e. returns to step 1 of the Scenario of the Test Case TC001		

Scenario 42: Type A Collision detection with an error after ANTICOLLISION CL1 (xy=00 to 05, 07 and 11 to 13)

4.21.Type A Polling with detection of a Type A then a Type B PICC [TA303]

Test codification:

TA303

Test objective:

To ensure that the PCD behaves correctly when it detects a Type B PICC after having detected a Type A PICC during polling (*+ to ensure that the PCD grants enough time to detect a Type B PICC after having detected a Type A PICC during polling*).

References Requirement:

9.3.1.1

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

After having replied to a WUPA command during polling (first step of this Type A test), The LT responds to the next WUPB command sent by the PUT during polling with a valid ATQB sequence using the maximum Frame Delay Time $FDT_{B,PICC,ATQB,MAX} = FWT_{ATQB}$ between the end of the command sequence sent by the PUT and the beginning of the sequence replied by the LT.

The LT measures the delay between the beginning of the ATQB sequence and the beginning of the PICC Reset.

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT performs a PICC Reset when it receives an ATQB after having received an ATQA during polling).

The delay between the beginning of the ATQB sequence and the beginning of the PICC Reset is at most $t_{RESETDELAY}$.

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$.

Following the PICC Reset, the PUT restarts the initial polling procedure by sending a WUPA command followed by a WUPB command both preceded by a delay of at least $t_{P,MIN}$ and at most $t_{P,MAX}$ with carrier on (i.e. returns to step 1 of the Scenario of the Test Case TC001).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ◀ ATQB (Type B frame) = '50' + '5A 36 B9 F4' + '00 00 00 00 00 21 41' sent using FDT _{B,PICC,ATQB,MAX} ◀ LT	Default ATQB
6	PUT II The PUT stops sending the carrier within t _{RESETDELAY} II LT The PUT keeps the carrier off during at least t _{RESET,MIN} and at most t _{RESET,MAX}	PICC Reset
The PUT restarts the initial polling procedure i.e. returns to step 1 of the Scenario of the Test Case TC001		

Scenario 43: Type A Polling with detection of a Type A then a Type B PICC

4.22.Type A Collision detection with an error after WUPA [TA304.xy]

Test codification:

TA304.xy

Test objective:

To ensure that the PCD behaves correctly when it receives an error in response to the WUPA command sent during collision detection.

References Requirements:

4.7.1.3, 4.8.1.3, 5.1.1.1, 6.1.1.1, 9.3.2.1, 9.6.1.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT responds to a WUPA command sent by the PUT during polling with a valid ATQA (= '01 00').

The LT responds to the WUPA command sent by the PUT during collision detection (i.e. 2nd WUPA of the Scenario) with an erroneous ATQA.

The LT measures the delay between the beginning of the sequence with error and the beginning of the PICC Reset.

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

The following transmission errors on ATQA (activation) are generated successively by the LT:

- xy=00: ATQA with the carrier modulated with the subcarrier for the whole bit duration of b₁ of Byte 1 (equivalent to the result of the merging of two complementary bit patterns when 2 Type A cards are presented simultaneously to the PCD)
- xy=01: ATQA with parity error (corrupted parity bit) on the 2nd byte (last byte) of the frame
- xy=02: ATQA sent using a Frame Delay Time $FDT_{A,PICC} = (FDT_{A,PICC,ANTICOLLISION} - 256/f_c)$ between the end of the WUPA sequence and the beginning of the ATQA sequence

The following protocol errors are generated successively by the LT:

- xy=13: 1 byte long ATQA (too short ATQA)
- xy=14: ATQA with 2 CRC_A bytes (i.e. too long ATQA)
- xy=16: SAK = '20'

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT performs a PICC Reset when it detects an error after WUPA).

The delay between the beginning of the sequence with error and the beginning of the PICC Reset is at most $t_{RESETDELAY}$.

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$.

Following the PICC Reset, the PUT restarts the initial polling procedure by sending a WUPA command followed by a WUPB command both preceded by a delay of at least $t_{P,MIN}$ and at most $t_{P,MAX}$ with carrier on (i.e. returns to step 1 of the Scenario of the Test Case TC001).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ◀ '01 00' (no CRC_A and no error) ◀ LT	Valid ATQA
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ▲ Error in function of 'xy' For xy=0y: ATQA = '01 00' (no CRC_A) with a transmission error in function of 'y' PUT ▼ For xy=13: ATQA = '01' (no CRC_A) For xy=14: ATQA = '01 00' (with CRC_A) For xy=16: SAK = '20' ◀ LT	Error in function of 'xy'
7	PUT II The PUT stops sending the carrier within $t_{RESETDELAY}$ The PUT keeps the carrier off during at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$ II LT	PICC Reset
The PUT restarts the initial polling procedure i.e. returns to step 1 of the Scenario of the Test Case TC001		

Scenario 44: Type A Collision detection with an error after WUPA (xy=00 to 02, 13 to 14 and 16)

4.23.Type A Collision detection with an error after SELECT CL1 [TA305.xy]

Test codification:

TA305.xy

Test objective:

To ensure that the PCD behaves correctly when it receives an error in response to the SELECT CL1 command sent during Collision Detection.

References Requirements:

4.7.1.3, 4.8.1.3, 5.1.1.1, 5.2.1.1, 5.2.1.2, 9.6.1.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT responds to the SELECT CL1 command sent by the PUT during collision detection with an erroneous SAK.

The LT measures the delay between the beginning of the sequence with error and the beginning of the PICC Reset.

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

The following transmission errors on SAK are generated successively by the LT:

- xy=00: SAK with parity error (corrupted parity bit) on the 2nd byte (first CRC byte) of the frame
- xy=01: SAK with CRC error: the less significant bit of the 1st CRC byte is corrupted and the parity bit of this CRC byte is adapted in order to have only a CRC error
- xy=02: SAK with parity/CRC errors combination: a single bit of the 1st data byte of the frame is corrupted inducing both a parity and a CRC error
- xy=03: SAK sent using a Frame Delay Time $FDT_{A,PICC} = (FDT_{A,PICC,ANTICOLLISION} - 256/f_c)$ between the end of the SELECT CL1 sequence and the beginning of the SAK sequence

The following protocol errors are generated successively by the LT:

- xy=11: Type A frame containing only 2 CRC bytes (too short SAK)
- xy=12: SAK with no CRC byte

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT performs a PICC Reset when it detects an error after SELECT CL1).

The delay between the beginning of the sequence with error and the beginning of the PICC Reset is at most $t_{RESETDELAY}$.

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$.

Following the PICC Reset, the PUT restarts the initial polling procedure by sending a WUPA command followed by a WUPB command both preceded by a delay of at least $t_{P,MIN}$ and at most $t_{P,MAX}$ with carrier on (i.e. returns to step 1 of the Scenario of the Test Case TC001).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ◀ '2A 44 BF E7' + '36' (no CRC_A) ◀ LT	UID CL1 + BCC
9	PUT ▶ '93 70' + '2A 44 BF E7' + '36' ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ◀ Error in function of 'xy' For x=0: SAK = '20' with a transmission error in function of 'y' For xy=11: SAK = '63 63' (no CRC_A) For xy=12: SAK = '20' (no CRC_A) ◀ LT	Error in function of 'xy'
11	PUT II The PUT stops sending the carrier within $t_{RESETDELAY}$ The PUT keeps the carrier off during at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$ II LT	PICC Reset
The PUT restarts the initial polling procedure i.e. returns to step 1 of the Scenario of the Test Case TC001		

Scenario 45: Type A Collision detection with an error after SELECT CL1 (xy=00 to 03 and 11 to 12)

4.24. Type A Activation with an error after RATS [TA306.xy]

Test codification:

TA306.xy

Test objective:

To ensure that the PCD behaves correctly when it receives an error in response to the RATS command sent during activation.

References Requirements:

4.7.1.3, 5.1.1.1, 5.2.1.1, 5.2.1.2, 6.1.1.1, 9.6.1.1, 9.6.1.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT measures the delay between the beginning of the sequence with error and the beginning of the PICC Reset.

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

The following transmission errors on ATS are generated successively by the LT:

- xy=00: ATS (in a frame of at least 4 bytes) with parity error (corrupted parity bit) on the 5thbyte of the frame
- xy=01: ATS (in a frame of at least 4 bytes) with CRC error: the most significant bit of the 2nd CRC byte is corrupted and the parity bit of this CRC byte is adapted in order to have only a CRC error
- xy=02: ATS (in a frame of at least 4 bytes) with parity/CRC errors combination: a single bit of the 5th data byte of the frame is corrupted inducing both a parity and a CRC error
- xy=04: ATS sent using a Frame Delay Time $FDT_{A,PICC} = (FDT_{A,PICC,MIN} - 256/f_c)$ between the end of the RATS sequence and the beginning of the ATS
- xy=05: ATS (in a frame of at least 4 bytes) with some residual bits (i.e. the total number of bits is not a multiple of 8 = with 3 bits to (101)_b following the CRC bytes)

The following protocol errors are generated successively by the LT:

- xy=10: ATS with Length Byte TL = '00'
- xy=12: ATS with Length Byte TL = '02' and T0 = '72'
- xy=13: ATS with TL='05' and T0 ='72' and TA(1) absent
- xy=14: ATS with less historical bytes than indicated in the length byte TL (equivalent to: "ATS with no CRC byte")
- xy=15: I-Block

In this test, the following ATS with errors shall be used:

	ATS						Comments
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
xy= 00-02 and 04-05	'05'	'72'	'80'	'40'	'02'	-	Default value with a transmission error in function of 'y'
xy=10	'00'	-	-	-	-	-	TL byte only
xy=12	'02'	'72'	'80'	'40'	'02'	-	TL not compliant with T0
xy=13	'05'	'72'	-	'40'	'02'	-	Incorrect T0
xy=14	'07'	'72'	'80'	'40'	'02'	-	Incorrect TL
xy=15	'02'	'00'	'B2'	'01'	'04'	'00 90 00'	I(0) ₀ ['00 B2 01 04 00' + '90 00']

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT performs a PICC Reset when it detects an error after RATS).

The delay between the beginning of the sequence with error and the beginning of the PICC Reset is at most $t_{RESETDELAY}$.

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$.

Following the PICC Reset, the PUT restarts the initial polling procedure by sending a WUPA command followed by a WUPB command both preceded by a delay of at least $t_{P,MIN}$ and at most $t_{P,MAX}$ with carrier on (i.e. returns to step 1 of the Scenario of the Test Case TC001).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ '2A 44 BF E7' + '36' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '2A 44 BF E7' + '36'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS with error in function of 'xy'	◀ LT Error in function of 'xy'
13	PUT II The PUT stops sending the carrier within $t_{RESETDELAY}$ The PUT keeps the carrier off during at least t_{RESET}	II LT PICC Reset

The PUT restarts the initial polling procedure i.e. returns to step 1 of the Scenario of the Test Case TC001

Scenario 46: Type A Activation with an error after RATS (xy=00 to 02, 04-05, 10 and 12 to 15)

4.25. Type A Activation with ‘noise’ after RATS [TA307.x]

Test codification:

TA307.x

Test objective:

To ensure that the PCD behaves correctly when it receives some ‘noise’ (i.e. a frame with a transmission error to be processed as noise by the PCD) in response to the RATS command sent during activation.

References Requirements:

4.7.1.3, 5.2.1.1, 5.2.1.2, 9.6.1.3, 4.9.2.1

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT replies to RATS command sent by the PUT with a sequence inducing a ‘noise’ error using a delay of ($FDT_{A,PICC,MIN} + 128/f_c$) between the end of the RATS sequence sent by the PUT and the beginning of the ‘noise’ error generated by the LT.

The LT measures the delay between the end of the sequence sent by the PUT after which a ‘noise’ error is generated and the beginning of the next sequence sent by the PUT to process the error.

The following ‘noise’ errors are generated successively by the LT:

- $x=0$: Continuous modulation of the PUT carrier with a frequency equal to $f_s = f_0/16$, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of $5888 \times 1/f_c$ (i.e. duration of a 5 bytes frame in Type A)
- $x=1$: ATS of less than 4 bytes with parity error (a single parity bit is corrupted on any byte)
- $x=2$: ATS of less than 4 bytes with CRC error (the CRC bytes are corrupted and the parity bits of the CRC bytes are adapted in order to have only a CRC error)
- $x=3$: ATS of less than 4 bytes with some residual bits (i.e. the total number of bits is not a multiple of 8 = with 3 bits to $(101)_b$ following the CRC bytes)

In this test, the following ATS with errors shall be used:

	ATS						Comments
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
x=0	-	-	-	-	-	-	No ATS (replaced by a continuous subcarrier modulation)
x=1-2	'01'	-	-	-	-	-	1 byte long ATS (with an error in function of 'x')

	ATS						Comments
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
x=3	'01'	-	-	-	-	-	1 byte long ATS with 3 bits to (101) _b following the CRC bytes

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT ignores the ‘noise’ error, retransmits the RATS command and continues the transaction upon receipt of a correct ATS).

The delay between the end of the sequence sent by the PUT after which a ‘noise’ error is generated and the beginning of the next sequence sent by the PUT to process the error is at least [FWT_{ACTIVATION} + t_{MIN,RETRANSMISSION}] and at most [FWT_{ACTIVATION} + t_{RETRANSMISSION}].

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ 'BF 44 87 E7' + '9B' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + 'BF 44 87 E7' + '9B'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ 'Noise' error in function of 'x'	◀ LT Error in function of 'x'
13	'E0 80' sent between [FWT_ACTIVATION + t _{MIN.RETRANSMISSION}] and PUT ▶ [FWT_ACTIVATION + t_{RETRANSMISSION}] measured from the end of the last sequence from the PUT	▶ LT RATS
14	PUT ◀ ATS (without error)	◀ LT Default ATS
15	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
16	PUT ◀ I(0)₀ ["EOT Command" + '90 00']	◀ LT End Of Test command
17	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
18	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
19	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
20	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 47: Type A Activation with 'noise' after RATS (x=0 to 3)

4.26.Type A Collision detection with a time-out after ANTCOLLISION CL1 [TA310]

Test codification:

TA310

Test objective:

To ensure that the PCD behaves correctly when it does not receive any response to the ANTCOLLISION CL1 command sent during collision detection.

References Requirements:

4.8.1.4, 9.6.1.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT measures the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT retransmits the ANTCOLLISION CL1 command when it detects a time-out error).

The delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at least $[FDT_{A,PICC,ANTICOLLISION} + t_{MIN,RETRANSMISSION}]$ and at most $[FDT_{A,PICC,ANTICOLLISION} + t_{RETRANSMISSION}]$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ▶ '93 20' (no CRC_A) sent between [FDT _{A,PICC,ANTICOLLISION + t_{MIN.RETRANSMISSION}}] and [FDT _{A,PICC,ANTICOLLISION + t_{RETRANSMISSION}}]	▶ LT ANTICOLLISION CL1
9	PUT ◀ 'BB 15 04 78' + 'D2' (no CRC_A)	◀ LT UID CL1 + BCC
10	PUT ▶ '93 70' + 'BB 15 04 78' + 'D2'	▶ LT SEL1 + UID CL1 + BCC
11	PUT ◀ '20'	◀ LT SAK
12	PUT ▶ 'E0 80'	▶ LT RATS
13	PUT ◀ ATS	◀ LT ATS
14	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
15	PUT ◀ I(0)₀ ["EOT Command" + '90 00']	◀ LT End Of Test command
16	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
17	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
18	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
19	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 48: Type A Collision detection with a time-out after ANTICOLLISION CL1

4.27.Type A Collision detection with a time-out after WUPA [TA311.x]

Test codification:

TA311.x

Test objective:

To ensure that the PCD behaves correctly when it does not receive any response to the WUPA command sent during collision detection.

References Requirements:

4.8.1.4, 9.6.1.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenarios.

For x=0, the LT measures the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

For x=1, the LT measures the delay between the end of the second sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

For x=2, the LT measures the delay between the end of the third sequence to which the LT does not respond and the beginning of the PICC Reset and the time during which the PUT stops sending the carrier to perform a PICC Reset.

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenarios (the PUT retransmits the WUPA commands up to two times when it detects a time-out error and performs a PICC Reset when it detects a third consecutive time-out error).

For x=0, the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at least $[FDT_{A,PICC,ANTICOLLISION} + t_{MIN,RETRANSMISSION}]$ and at most $[FDT_{A,PICC,ANTICOLLISION} + t_{RETRANSMISSION}]$.

For x=1, the delay between the end of the second sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at least $[FDT_{A,PICC,ANTICOLLISION} + t_{MIN,RETRANSMISSION}]$ and at most $[FDT_{A,PICC,ANTICOLLISION} + t_{RETRANSMISSION}]$.

For $x=2$, the delay between the end of the third sequence to which the LT does not respond and the beginning of the PICC Reset is at most $[FDT_{A,PICC,ANTICOLLISION} + t_{RESETDELAY}]$.

For $x=2$ (only), following the PICC Reset, the PUT restarts the initial polling procedure by sending a WUPA command followed by a WUPB command both preceded by a delay of at least $t_{P,MIN}$ and at most $t_{P,MAX}$ with carrier on (i.e. returns to step 1 of the Scenario of the Test Case TC001).

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$.

Failure action:

Proceed with the next test.

Scenarios:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ↴ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ▶ '52' (short frame) sent between $[FDT_{A,PICC,ANTICOLLISION} + t_{MIN,RETRANSMISSION}]$ and $[FDT_{A,PICC,ANTICOLLISION} + t_{RETRANSMISSION}]$	▶ LT WUPA
7	PUT ↴ '01 00' (no CRC_A)	◀ LT ATQA
8	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
9	PUT ↴ '90 FE 01 5A' + '35' (no CRC_A)	◀ LT UID
10	PUT ▶ '93 70' + '90 FE 01 5A' + '35'	▶ LT SEL1 + UID CL1 + BCC
11	PUT ↴ '20'	◀ LT SAK
12	PUT ▶ 'E0 80'	▶ LT RATS
13	PUT ↴ ATS	◀ LT ATS
14	PUT ▶ I(0)o ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
15	PUT ↴ I(0)o ["EOT Command" + '90 00']	◀ LT End Of Test command
16	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
17	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
18	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
19	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 49: Type A Collision detection with a time-out after WUPA ($x=0$)

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ▶ '52' (short frame) ▶ LT	WUPA
7	PUT ▶ '52' (short frame) sent between [FDT _A ,PICC,ANTICOLLISION + t _{MIN,RETRANSMISSION}] and [FDT _A ,PICC,ANTICOLLISION + t _{RETRANSMISSION}] ▶ LT	WUPA
8	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
9	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
10	PUT ◀ '11 22 44 88' + 'FF' (no CRC_A) ◀ LT	UID
11	PUT ▶ '93 70' + '11 22 44 88' + 'FF' ▶ LT	SEL1 + UID CL1 + BCC
12	PUT ◀ '20' ◀ LT	SAK
13	PUT ▶ 'E0 80' ▶ LT	RATS
14	PUT ◀ ATS ◀ LT	ATS
15	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + '2PAY.SYS.DDF01' + '00'] ▶ LT	Select PPSE
16	PUT ◀ I(0)₀ ['EOT Command' + '90 00'] ◀ LT	End Of Test command
17	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
18	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
19	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
20	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC

Scenario 50: Type A Collision detection with a time-out after WUPA (x=1)

Step	Exchanges		Comments
1	PUT ▶ '52' (short frame)	▶ LT	WUPA during polling
2	PUT ↲ '01 00' (no CRC_A)	↳ LT	ATQA
3	PUT ▶ '50 00'	▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT	WUPB
5	PUT ▶ '52' (short frame)	▶ LT	WUPA
6	PUT ▶ '52' (short frame)	▶ LT	WUPA
7	PUT ▶ '52' (short frame)	▶ LT	WUPA
8	PUT II The PUT stops sending the carrier within $[FDT_{A,PICC,ANTICOLLISION} + t_{RESETDELAY}]$ The PUT keeps the carrier off during at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$	II LT	PICC Reset

The PUT restarts the initial polling procedure i.e. returns to step 1 of the Scenario of the Test Case TC001

Scenario 51: Type A Collision detection with a time-out after WUPA (x=2)

4.28.Type A Collision detection with a time-out after SELECT CL1 [TA312]

Test codification:

TA312

Test objective:

To ensure that the PCD behaves correctly when it does not receive any response to the SELECT CL1 command sent during collision detection.

References Requirements:

4.8.1.4, 9.6.1.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT measures the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT retransmits the SELECT CL1 command when it detects a time-out error).

The delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at least $[FDT_{A,PICC,ANTICOLLISION} + t_{MIN,RETRANSMISSION}]$ and at most $[FDT_{A,PICC,ANTICOLLISION} + t_{RETRANSMISSION}]$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ '0F 0F 0F 0F' + '00' (no CRC_A)	◀ LT UID CL1 + BCC
9	PUT ▶ '93 70' + '0F 0F 0F 0F' + '00'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ▶ '93 70' + '0F 0F 0F 0F' + '00' sent between [FDT _{A,PICC,ANTICOLLISION} + t _{MIN,RETRANSMISSION}] and [FDT _{A,PICC,ANTICOLLISION} + t _{RETRANSMISSION}]	▶ LT SEL1 + UID CL1 + BCC
11	PUT ◀ '20'	◀ LT SAK
12	PUT ▶ 'E0 80'	▶ LT RATS
13	PUT ◀ ATS	◀ LT ATS
14	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
15	PUT ◀ I(0)₀ ["EOT Command" + '90 00']	◀ LT End Of Test command
16	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
17	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
18	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
19	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 52: Type A Collision detection with a time-out after SELECT CL1

4.29. Type A Activation with a time-out after RATS [TA313]

Test codification:

TA313

Test objective:

To ensure that the PCD behaves correctly when it does not receive any response to the RATS command sent during activation.

References Requirements:

4.8.1.12, 9.6.1.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT measures the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT retransmits the RATS command when it detects a time-out error).

The delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at least $[FWT_{ACTIVATION} + t_{MIN,RETRANSMISSION}]$ and at most $[FWT_{ACTIVATION} + t_{RETRANSMISSION}]$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ 'F0 F0 F0 F0' + '00' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + 'F0 F0 F0 F0' + '00'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ▶ 'E0 80' sent between [FWT _{ACTIVATION} + t _{MIN,RETRANSMISSION}] and [FWT _{ACTIVATION} + t _{RETRANSMISSION}]	▶ LT RATS
13	PUT ◀ ATS	◀ LT ATS
14	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
15	PUT ◀ I(0)₀ ["EOT Command" + '90 00']	◀ LT End Of Test command
16	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
17	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
18	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
19	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 53: Type A Activation with a time-out after RATS

4.30. Type A Activation with respect of the EMD Suppression behavior after RATS [TA335.xy]

Test codification:

TA335.xy

Test objective:

To ensure that, following the RATS command sent during activation, the PCD correctly ignores all the transmission errors except the frames of at least 4 bytes with no residual bit and with a parity or/and a CRC error and is ready to process a correct sequence no later than $t_{RECOVERY}$ after reception of the last transmission error.

References Requirement:

4.9.2.1

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT responds to a RATS command sent by the PUT during activation with a transmission error (but not a frame of at least 4 bytes with no residual bit and with a parity or/and CRC error) using the following Frame Delay Time between the end of the sequence sent by the PUT and the beginning of the transmission error generated by the LT:

- $x=0: FDT_{A,PICC} = FDT_{A,PICC,MIN} - 256/f_c$
- $x=1: FDT_{A,PICC} = FDT_{A,PICC,MIN}$
- $x=2: FDT_{A,PICC} =$
 - $32768 \times 1/f_c + 20/f_c$ if the last bit transmitted by the PUT is $(0)_b$
 - $32768 \times 1/f_c + 84/f_c$ if the last bit transmitted by the PUT is $(1)_b$

Then, the LT sends a correct response sequence to the PUT using the following delay between the end of the transmission error and the beginning of the correct response sequence both sent by the LT:

- $t_{RECOVERY}$ if the transmission error sent by the LT is a continuous modulation with a duration $= n \times 128/f_c$ (i.e. $y=0$ to 2) or if the last bit of the transmission error sent by the LT is $(0)_b$
- $(t_{RECOVERY} + 64/f_c)$ if the last bit of the transmission error sent by the LT is $(1)_b$

Remarks:

- An additional delay of $64/f_c$ is added for the last bit value $(1)_b$ because no event can be observed during the second half of the last bit of the transmission error.
- If the test tool is not able to detect any event during the second half of the last subcarrier cycle of the transmission error, then an additional delay of $8/f_c$ shall be applied for both last bit values.

The following ‘noise’ errors are generated successively by the LT:

- y=0: Continuous modulation of the PUT carrier with a frequency equal to $f_s = f_c/16$, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of $512 \times 1/f_c$
- y=1: Continuous modulation of the PUT carrier with a frequency equal to $f_s = f_c/16$, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of $5888 \times 1/f_c$ (i.e. duration of a 5 bytes frame in Type A)
- y=2: Continuous modulation of the PUT carrier with a frequency equal to $f_s = f_c/16$, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of $11648 \times 1/f_c$ (i.e. duration of a 10 bytes frame in Type A)
- y=3: ATS of less than 4 bytes with parity error (a single parity bit is corrupted on any byte)
- y=4: ATS of less than 4 bytes with CRC error (the CRC bytes are corrupted and the parity bits of the CRC bytes are adapted in order to have only a CRC error)
- y=5: ATS of less than 4 bytes with some residual bits (i.e. the total number of bits is not a multiple of 8)

In this test, the default ATS (with default values for all parameters) shall be used:

	ATS						Comments
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
x=0-2 y=0-5	‘05’	‘72’	‘80’	‘40’	‘02’	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (after sending the RATS command, the PUT ignores the transmission error and accepts the next correct sequence sent by the LT).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ '07 F1 2A DC' + '00' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '07 F1 2A DC' + '00'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	<p>'Noise' error in function of 'y' sent using the Frame Delay Time in function of 'x'</p> <p>For y=0: $512 \times 1/f_c$ of continuous subcarrier modulation</p> <p>For y=1: $5888 \times 1/f_c$ of continuous subcarrier modulation</p> <p>PUT ◀ For y=2: $11648 \times 1/f_c$ of continuous subcarrier modulation</p> <p>For y=3: ATS = '01' with parity error (on any byte)</p> <p>For y=4: ATS= '01' with CRC error</p> <p>For y=5: ATS = '01' with 3 bits to (101)b following the CRC bytes</p>	◀ LT Error in function of 'y' sent with a Frame Delay Time in function of 'x'
13	PUT ◀ ATS (default ATS defined in the Procedure) sent using a delay of tRECOVERY or $(tRECOVERY + 64/f_c)$ from the end of the transmission error	◀ LT Correct ATS sequence sent with recovery delay
14	PUT ▶ I(0)o ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
15	PUT ◀ I(0)o ["EOT Command" + '90 00']	◀ LT End Of Test command
16	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
17	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
18	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
19	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 54: Type A Activation with respect of the EMD Suppression behavior after RATS (xy=00 to 05, xy=10 to 15 and xy=20 to 25)

4.31.Type A Activation with respect of the ‘deaf time’ after RATS [TA340.x]

Test codification:

TA340.x

Test objective:

To ensure that, following the RATS command sent during activation, the PCD is completely deaf (i.e. ignores any subcarrier generated by the PICC) until $FDT_{A,PICC,MIN} - 128/f_c$.

References Requirement:

4.8.1.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) on reception of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT responds to a RATS command sent by the PUT during activation with a sequence with no transmission error (i.e. a correct sequence or a sequence with protocol error) using the Frame Delay Time $FDT_{A,PICC} = FDT_{A,PICC,MIN} - 256/f_c$ between the end of the sequence sent by the PUT and the beginning of the sequence replied by the LT.

The following sequences are successively sent by the LT in response to the RATS command:

- x=0: 1 byte ATS (TL='01') with correct CRC
- x=1: 1 byte ATS (TL='01') with no CRC

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (after sending the RATS command, the PUT ignores the sequence received during the ‘deaf time’ and processes it as a time-out error i.e. resends the RATS command).

Failure action:

Proceed with next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ '98 3A E5 00' + '47' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '98 3A E5 00' + '47'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ Sequence in function of 'x' sent using the Frame Delay Time $FDT_{A,PICC} = (FDT_{A,PICC,MIN} - 256/f_c)$ For x=0: ATS = '01' with correct CRC For x=1: ATS = '01' with no CRC	◀ LT Sequence in function of 'x' sent using the Frame Delay Time $FDT_{A,PICC,MIN} - 256/f_c$
13	PUT ▶ 'E0 80'	▶ LT RATS
14	PUT ◀ ATS	◀ LT ATS
15	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
16	PUT ◀ I(0)₀ ["EOT Command" + '90 00']	◀ LT End Of Test command
17	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
18	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
19	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
20	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 55: Type A Activation with respect of the 'deaf time' after RATS (x=0 and 1)

4.32.Type A Error notification on an I-Block not indicating chaining [TA401.xy]

Test codification:

TA401.xy

Test objective:

To ensure that the PCD behaves correctly when it receives one to three consecutive error notification(s) on an I-Block not indicating chaining.

References Requirements:

4.8.1.8, 10.3.4.3, 10.3.4.4, 10.3.5.5, 10.3.5.9

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenarios.

For xy=00 to 14 and for each error notification during block protocol, the LT measures the delay between the end of the sequence on which the LT signals an error and the beginning of the next sequence sent by the PUT to process the time-out error.

For xy=15, the LT measures the delay between the beginning of the sequence containing the last R(ACK) Block sent by the LT and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier). And the LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

In this test, the following ATS shall be used:

	ATS						(FWT+ΔFWT)
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
xy=00	'05'	'72'	'80'	'00'	'02'	-	53248x 1/f _c
xy=01	'05'	'72'	'80'	'10'	'02'	-	57344x 1/f _c
xy=02	'05'	'72'	'80'	'20'	'02'	-	65536x 1/f _c
xy=03	'05'	'72'	'80'	'30'	'02'	-	81920x 1/f _c
xy=04 or 15	'05'	'72'	'80'	'40'	'02'	-	114688x 1/f _c (default value)
xy=05	'05'	'72'	'80'	'50'	'02'	-	180224x 1/f _c
xy=06	'05'	'72'	'80'	'60'	'02'	-	311296x 1/f _c
xy=07	'05'	'72'	'80'	'70'	'02'	-	573440x 1/f _c
xy=08	'05'	'72'	'80'	'80'	'02'	-	1097728x 1/f _c
xy=09	'05'	'72'	'80'	'90'	'02'	-	2146304x 1/f _c
xy=10	'05'	'72'	'80'	'A0'	'02'	-	4243456x 1/f _c

	ATS						(FWT+ΔFWT)
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
xy=11	'05'	'72'	'80'	'B0'	'02'	-	8437760x 1/f _c
xy=12	'05'	'72'	'80'	'C0'	'02'	-	16826368x 1/f _c
xy=13	'05'	'72'	'80'	'D0'	'02'	-	33603584x 1/f _c
xy=14	'05'	'72'	'80'	'E0'	'02'	-	67158016x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenarios (the PUT retransmits the I-Block on which is notified an error up to two times and initiates a PICC Reset upon receipt of a third error notification).

For xy=00 to 14 and for each error notification, the delay between the end of the sequence to which the LT does not respond and the beginning of the sequence sent by the PUT to process the time-out error is at most [(FWT+ΔFWT) + t_{RETRANSMISSION}].

For xy=15, the delay between the beginning of the sequence containing the last R(ACK) Block sent by the LT (protocol error) and the beginning of the PICC Reset initiated by the PUT is at most t_{RESETDELAY} (i.e. the PUT stops sending the carrier within t_{RESETDELAY}). And the time during which the PUT stops sending the carrier to perform a PICC Reset is at least t_{RESET,MIN}.

Failure action:

Proceed with the next test.

Scenarios:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ▲ '27 E9 3B 11' + 'E4' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '27 E9 3B 11' + 'E4'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ▲ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ▲ ATS	◀ LT ATS
13	PUT ▶ I(0) ₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ▲ I(0) ₀ ['00 B2 01 04 00' + '90 00']	◀ LT
15	PUT ▶ I(0) ₁ ['00 B2 01 04 00']	▶ LT Loop-back

Step	Exchanges	Comments
16	PUT ▶ R(NAK)₁ sent within [(FWT+ ΔFWT) + t _{RETRANSMISSION}] in function of 'xy' ▶ LT	Time-out error notification
17	PUT ◀ R(ACK)₀ ◀ LT	Request for Block repetition
18	PUT ▶ I(0)₁ ['00 B2 01 04 00'] ▶ LT	Error recovery
19	PUT ◀ I(0)₁ ['00 B2 02 04 00' + '90 00'] ◀ LT	
20	PUT ▶ I(0)₀ ['00 B2 02 04 00'] ▶ LT	Loop-back
21	PUT ▶ R(NAK)₀ sent within [(FWT+ ΔFWT) + t _{RETRANSMISSION}] in function of 'xy' ▶ LT	Time-out error notification
22	PUT ◀ R(ACK)₁ ◀ LT	Request for Block repetition
23	PUT ▶ I(0)₀ ['00 B2 02 04 00'] ▶ LT	Error recovery
24	PUT ◀ I(0)₀ ["EOT Command" + '90 00'] ◀ LT	End Of Test command
25	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
26	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
27	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
28	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC

Scenario 56: Type A Error notification on an I-Block not indicating chaining (xy=00 to 14)

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ◀ '01 00' (no CRC_A) ◀ LT	ATQA
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ◀ '72 9E B3 11' + '4E' (no CRC_A) ◀ LT	UID
9	PUT ▶ '93 70' + '72 9E B3 11' + '4E' ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ◀ '20' ◀ LT	SAK
11	PUT ▶ 'E0 80' ▶ LT	RATS
12	PUT ◀ ATS ◀ LT	ATS

Step	Exchanges	Comments
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
14	PUT ◀ I(0)₀ ['00 B2 5A 04 00' + '90 00'] ◀ LT	
15	PUT ▶ I(0)₁ ['00 B2 5A 04 00'] ▶ LT	Loop-back
16	PUT ▶ R(NAK)₁ ▶ LT	Time-out error notification
17	PUT ◀ R(ACK)₀ ◀ LT	Request for Block repetition
18	PUT ▶ I(0)₁ ['00 B2 5A 04 00'] ▶ LT	Error recovery
19	PUT ▶ R(NAK)₁ ▶ LT	Time-out error notification
20	PUT ◀ R(ACK)₀ ◀ LT	Request for Block repetition
21	PUT ▶ I(0)₁ ['00 B2 5A 04 00'] ▶ LT	Error recovery
22	PUT ◀ I(0)₁ ['00 B2 C3 04 00' + '90 00'] ◀ LT	
23	PUT ▶ I(0)₀ ['00 B2 C3 04 00'] ▶ LT	Loop-back
24	PUT ▶ R(NAK)₀ ▶ LT	Time-out error notification
25	PUT ◀ R(ACK)₁ ◀ LT	Request for Block repetition
26	PUT ▶ I(0)₀ ['00 B2 C3 04 00'] ▶ LT	Error recovery
27	PUT ▶ R(NAK)₀ ▶ LT	Time-out error notification
28	PUT ◀ R(ACK)₁ ◀ LT	Request for Block repetition
29	PUT ▶ I(0)₀ ['00 B2 C3 04 00'] ▶ LT	Error recovery
30	PUT ▶ R(NAK)₀ ▶ LT	Time-out error notification
31	PUT ◀ R(ACK)₁ (protocol error) ◀ LT	Request for Block repetition
32	The PUT performs a PICC Reset (i.e. stops sending the carrier) PUT II The PICC Reset is initiated within t _{RESETDELAY} The PUT keeps the carrier off during at least t _{RESET,MIN}	PICC Reset

Scenario 57: Type A Error notification on an I-Block not indicating chaining (xy=15)

4.33.Type A Time-out after an I-Block not indicating chaining [TA402]

Test codification:

TA402

Test objective:

To ensure that the PCD behaves correctly when it does not receive any response to an I-Block not indicating chaining.

References Requirements:

4.8.1.8, 10.3.5.5, 10.3.5.9

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

When two consecutive time-out errors are generated successively by the LT, the LT measures the delay between the end of the second sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

When three consecutive time-out errors are generated successively by the LT, the LT measures the delay between the end of the third sequence to which the LT does not respond and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						(FWT+ΔFWT)
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	114688 x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends an R(NAK) Block to ask for retransmission when it detects a first or a second consecutive time-out error after an I-Block not indicating chaining and initiates a PICC Reset when it detects a third consecutive time-out error).

When two consecutive time-out errors are generated successively by the LT, the delay between the end of the second sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error, is at most [(FWT+ΔFWT) + t_{RETRANSMISSION}].

When three consecutive time-out errors are generated successively by the LT, the delay between the end of the third sequence to which the LT does not respond and the beginning of

the PICC Reset initiated by the PUT is at most $[(FWT + \Delta FWT) + t_{RESETDELAY}]$ (i.e. the PUT stops sending the carrier within $[(FWT + \Delta FWT) + t_{RESETDELAY}]$).

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ '0E 81 96 D3' + 'CA' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '0E 81 96 D3' + 'CA'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ◀ I(0)₀ ['00 B2 01 04 00' + '90 00']	◀ LT
15	PUT ▶ I(0)₁ ['00 B2 01 04 00']	▶ LT Loop-back
16	PUT ▶ R(NAK)₁	▶ LT Time-out error notification
17	PUT ◀ I(0)₁ ['00 B2 02 04 00' + '90 00']	◀ LT Error recovery
18	PUT ▶ I(0)₀ ['00 B2 02 04 00']	▶ LT Loop-back
19	PUT ▶ R(NAK)₀	▶ LT Time-out error notification
20	PUT ◀ I(0)₀ ['00 B2 03 04 00' + '90 00']	◀ LT Error recovery
21	PUT ▶ I(0)₁ ['00 B2 03 04 00']	▶ LT Loop-back
22	PUT ▶ R(NAK)₁	▶ LT Time-out error notification
23	PUT ▶ R(NAK)₁ sent within $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$	▶ LT Time-out error notification
24	PUT ◀ I(0)₁ ['00 B2 04 04 00' + '90 00']	◀ LT Error recovery

Step	Exchanges	Comments
25	PUT ▶ I(0)₀ ['00 B2 04 04 00'] ▶ LT	Loop-back
26	PUT ▶ R(NAK)₀ ▶ LT	Time-out error notification
27	PUT ▶ R(NAK)₀ sent within [(FWT+ ΔFWT) + t_{RETRANSMISSION}] ▶ LT	Time-out error notification
28	PUT ◀ I(0)₀ ['00 B2 05 04 00' + '90 00'] ◀ LT	Error recovery
29	PUT ▶ I(0)₁ ['00 B2 05 04 00'] ▶ LT	Loop-back
30	PUT ▶ R(NAK)₁ ▶ LT	Time-out error notification
31	PUT ▶ R(NAK)₁ ▶ LT	Time-out error notification
32	The PUT performs a PICC Reset (i.e. stops sending the carrier) PUT II The PICC Reset is initiated within [(FWT+ ΔFWT) + t _{RESETDELAY}] The PUT keeps the carrier off during at least t _{RESET,MIN}	PICC Reset

Scenario 58: Type A time-out after an I-Block not indicating chaining

4.34.Type A Transmission error in response to an I-Block not indicating chaining [TA403.x]

Test codification:

TA403.x

Test objective:

To ensure that the PCD behaves correctly when it receives a transmission error in response to an I-Block not indicating chaining.

References Requirements:

4.7.1.3, 5.2.1.1, 5.2.1.2, 10.3.5.3, 10.3.5.9

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

When a single transmission error is generated, the LT measures the delay between the beginning of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When a single transmission error is generated, the LT measures the delay between the end of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When two consecutive transmission errors are generated, the LT measures the delay between the beginning of the second sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When two consecutive transmission errors are generated, the LT measures the delay between the end of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When three consecutive transmission errors are generated, the LT measures the delay between the beginning of the third sequence with transmission error and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

The following transmission errors are generated successively by the LT:

- x=0: I-Block (in a frame of at least 4 bytes) with CRC error: the less significant bit of the 1st CRC byte is corrupted for the 1st, 4th and 7th error generated, the less significant bit of the 2nd CRC byte is corrupted for the 2nd, 5th and 8th error generated, the most significant bit of the 2nd CRC byte is corrupted for the 3rd, 6th and 9th error generated and for each error generated, the parity bit of the corrupted CRC byte is adapted in order to have only a CRC error
- x=1: I-Block (in a frame of at least 4 bytes) with parity error (corrupted parity bit) on the following bytes: the 5th byte of the frame for the 1st and 7th errors generated, 5th byte of the INF field for the 2nd to 4th errors generated, the 1st CRC byte (one byte

- before the last byte of the frame) for the 5th and 8th error generated and the 2nd byte of the CRC (last byte of the frame) for the 6th and 9th error generated
- x=2: I-Block (in a frame of at least 4 bytes) with parity/CRC errors combination: a single bit is corrupted on the 5th byte (not the CRC bytes) at a different position from one frame with error to another inducing both a parity and a CRC error
 - x=5: I-Block of at least 4 bytes with some residual bits (i.e. the total number of bits is not a multiple of 8)

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends an R(NAK) Block when it detects a first or a second consecutive transmission error after an I-Block not indicating chaining and initiates a PICC Reset when it detects a third consecutive transmission error).

When a single transmission error is generated, the delay between the end of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at least FDT_{A,PCD,MIN}.

When a single transmission error is generated, the delay between the beginning of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at most t_{RETRANSMISSION}.

When two consecutive transmission errors are generated, the delay between the end of the second sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at least FDT_{A,PCD,MIN}.

When two consecutive transmission errors are generated, the delay between the beginning of the second sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at most t_{RETRANSMISSION}.

When three consecutive transmission errors are generated, the delay between the beginning of the third sequence with transmission error and the beginning of the PICC Reset initiated by the PUT is at most t_{RESETDELAY} (i.e. the PUT stops sending the carrier within t_{RESETDELAY}).

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least t_{RESET,MIN}.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ 'D7 EE 3B 98' + '9A' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + 'D7 EE 3B 98' + '9A'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + '2PAY.SYS.DDF01' + '00']	▶ LT Select PPSE
14	PUT ◀ I(0)₀ ['00 B2 01 04 00' + '90 00']	◀ LT
15	PUT ▶ I(0)₁ ['00 B2 01 04 00']	▶ LT Loop-back
16	PUT ◀ I(0)₁ ['00 B2 02 04 00' + '90 00'] with a transmission error in function of 'x'	◀ LT Error in function of 'x'
17	PUT ▶ R(NAK)₁ sent after FDT_{A,PCD,MIN} and within t_{RETRANSMISSION}	▶ LT Request for Block repetition
18	PUT ◀ I(0)₁ ['00 B2 02 04 00' + '90 00']	◀ LT Error recovery
19	PUT ▶ I(0)₀ ['00 B2 02 04 00']	▶ LT Loop-back
20	PUT ◀ I(0)₀ ['00 B2 03 04 00' + '90 00'] with a transmission error in function of 'x'	◀ LT Error in function of 'x'
21	PUT ▶ R(NAK)₀ sent after FDT_{A,PCD,MIN} and within t_{RETRANSMISSION}	▶ LT Request for Block repetition
22	PUT ◀ I(0)₀ ['00 B2 03 04 00' + '90 00']	◀ LT Error recovery
23	PUT ▶ I(0)₁ ['00 B2 03 04 00']	▶ LT Loop-back
24	PUT ◀ I(0)₁ ['00 B2 04 04 00' + '90 00'] with a transmission error in function of 'x'	◀ LT Error in function of 'x'
25	PUT ▶ R(NAK)₁	▶ LT Request for Block repetition
26	PUT ◀ I(0)₁ ['00 B2 04 04 00' + '90 00'] with a transmission error in function of 'x'	◀ LT Error in function of 'x'
27	PUT ▶ R(NAK)₁ sent after FDT_{A,PCD,MIN} and within t_{RETRANSMISSION}	▶ LT Request for Block repetition

Step	Exchanges	Comments
28	PUT \leftarrow I(0) ₁ ['00 B2 04 04 00' + '90 00']	\leftarrow LT Error recovery
29	PUT \rightarrow I(0) ₀ ['00 B2 04 04 00']	\rightarrow LT Loop-back
30	PUT \leftarrow I(0) ₀ ['00 B2 05 04 00' + '90 00'] with a transmission error in function of 'x'	\leftarrow LT Error in function of 'x'
31	PUT \rightarrow R(NAK) ₀	\rightarrow LT Request for Block repetition
32	PUT \leftarrow I(0) ₀ ['00 B2 05 04 00' + '90 00'] with a transmission error in function of 'x'	\leftarrow LT Error in function of 'x'
33	PUT \rightarrow R(NAK) ₀ sent after FDT _{A,PCD,MIN} and within t _{RETRANSMISSION}	\rightarrow LT Request for Block repetition
34	PUT \leftarrow I(0) ₀ ['00 B2 05 04 00' + '90 00']	\leftarrow LT Error recovery
35	PUT \rightarrow I(0) ₁ ['00 B2 05 04 00']	\rightarrow LT Loop-back
36	PUT \leftarrow I(0) ₁ ['00 B2 06 04 00' + '90 00'] with a transmission error in function of 'x'	\leftarrow LT Error in function of 'x'
37	PUT \rightarrow R(NAK) ₁	\rightarrow LT Request for Block repetition
38	PUT \leftarrow I(0) ₁ ['00 B2 06 04 00' + '90 00'] with a transmission error in function of 'x'	\leftarrow LT Error in function of 'x'
39	PUT \rightarrow R(NAK) ₁	\rightarrow LT Request for Block repetition
40	PUT \leftarrow I(0) ₁ ['00 B2 06 04 00' + '90 00'] with a transmission error in function of 'x'	\leftarrow LT Error in function of 'x'
41	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) The PICC Reset is initiated within t _{RESETDELAY} The PUT keeps the carrier off during at least t _{RESET,MIN}	\parallel LT PICC Reset

Scenario 59: Type A Transmission error in response to an I-Block not indicating chaining (x=0 to 2 and 5)

4.35.Type A Protocol error in response to an I-Block not indicating chaining [TA404.x]

Test codification:

TA404.xy

Test objective:

To ensure that the PCD behaves correctly when it receives a protocol error in response to an I-Block not indicating chaining.

References Requirements:

4.7.3.1, 10.1.1.3, 10.1.5.1, 10.2.1.1, 10.2.2.1, 10.3.4.5, 10.3.4.6, 10.3.5.4, 10.3.5.9, 10.1.2.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

xy=11 is Not Applicable if the PCD implements a legacy behavior by accepting I-Blocks with b6 of PCB set to '1' (see ICS).

Procedure:

Run the following scenario.

The LT measures the delay between the beginning of the sequence inducing a protocol error and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

The following protocol errors are generated successively by the LT:

- xy=00: I-Block with bit b₂ of the PCB equal to '0'
- xy=01: I-Block with bit b₄ of the PCB equal to '1' (i.e. CID following)
- xy=02: I-Block with bit b₃ of the PCB equal to '1' (i.e. NAD following)
- xy=03: I-Block with wrong Block number indicated in the PCB
- xy=04: I-Block of length > FSD
- xy=05: R(NAK) Block
- xy=06: R(ACK) Block with a Block number different from the one of the last Block sent by the LT
- xy=07: S(DESELECT) response
- xy=08: S(WTX) Request with WTXM = 0
- xy=09: S(WTX) Request with WTXM = 1 and with bit b₂ of PCB equal to (0)_b
- xy=10: S(WTX) Request with WTXM = 60
- xy=11: I-Block with bit b₆ of the PCB equal to '1' (See "Conditions")
- xy=13: S(WTX) Request with b₆-b₅ of PCB set to 01_b, with WTXM =1
- xy=14: S(WTX) Request with b₆-b₅ of PCB set to 10_b, with WTXM =1
- xy=15: I-Block with b₈-b₇ of the PCB set to 01_b

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT initiates a PICC Reset when it detects a protocol error after an I-Block not indicating chaining).

The delay between the beginning of the sequence inducing a protocol error and the beginning of the PICC Reset initiated by the PUT is at most $t_{RESETDELAY}$ (i.e. the PUT stops sending the carrier within $t_{RESETDELAY}$).

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ '9A 4E C5 6F' + '7E' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '9A 4E C5 6F' + '7E'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0) ₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ◀ I(0) ₀ ['00 B2 01 04 00' + '90 00']	◀ LT
15	PUT ▶ I(0) ₁ ['00 B2 01 04 00']	▶ LT Loop-back

Step	Exchanges	Comments
16	<p>Protocol error in function of 'xy'</p> <p>For xy=00: I(0)₁ ['00 B2 02 04 00' + '90 00'] with b₂=0 in PCB</p> <p>For xy=01: I(0)₁ ['00 B2 02 04 00' + '90 00'] with b₄=1 in PCB</p> <p>For xy=02: I(0)₁ ['00 B2 02 04 00' + '90 00'] with b₃=1 in PCB</p> <p>For xy=03: I(0)₀ ['00 B2 02 04 00' + '90 00']</p> <p>For xy=04: I(0)₁ ['00 A4 04 00 F7' + '00 ... F6' + '00' + '90 00']</p> <p>For xy=05: R(NAK)₁</p> <p>For xy=06: R(ACK)₁</p> <p>For xy=07: S(DESELECT) response</p> <p>PUT I</p> <p>For xy=08: S(WTX Request) [WTXM='00']</p> <p>For xy=09: S(WTX Request) [WTXM='01'] and with bit b₂ of PCB equal to (0)_b</p> <p>For xy=10: S(WTX Request) [WTXM='3C']</p> <p>For xy=11 - (See "Conditions"): I(0)₁ ['00 B2 02 04 00' + '90 00'] with b₆=1 in PCB</p> <p>For xy=13: S(WTX Request) with b₆-b₅ set to 01b in PCB, with WTXM =1</p> <p>For xy=14: S(WTX Request) with b₆-b₅ set to 10b in PCB, with WTXM =1</p> <p>For xy=15: I(0)₁ ['00 B2 02 04 00' + '90 00'] with b₈-b₇ set to 01_b in PCB</p>	◀ LT Error in function of 'x'
17	<p>PUT II</p> <p>The PUT performs a PICC Reset (i.e. stops sending the carrier)</p> <p>The PICC Reset is initiated within t_{RESETDELAY}</p> <p>The PUT keeps the carrier off during at least t_{RESET,MIN}</p>	II LT PICC Reset

**Scenario 60: Type A Protocol error in response to an I-Block not indicating chaining
(xy=00 to 11, 13 to15)**

4.36.Type A Error notification on an I-Block indicating chaining [TA405.xy]

Test codification:

TA405.xy

Test objective:

To ensure that the PCD behaves correctly when it receives an error notification on an I-Block indicating chaining.

References Requirements:

4.8.1.8, 10.3.4.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

For each error notification during block protocol, the LT measures the delay between the end of the sequence on which the LT signals an error and the beginning of the next sequence sent by the PUT to process the time-out error.

In this test, the following ATS shall be used:

	ATS						(FWT+ΔFWT)
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
xy=00	'05'	'72'	'80'	'00'	'02'	-	53248 x 1/f _c
xy=01	'05'	'72'	'80'	'10'	'02'	-	57344x 1/f _c
xy=02	'05'	'72'	'80'	'20'	'02'	-	65536x 1/f _c
xy=03	'05'	'72'	'80'	'30'	'02'	-	81920 x 1/f _c
xy=04	'05'	'72'	'80'	'40'	'02'	-	114688x 1/f _c (default value)
xy=05	'05'	'72'	'80'	'50'	'02'	-	180224x 1/f _c
xy=06	'05'	'72'	'80'	'60'	'02'	-	311296x 1/f _c
xy=07	'05'	'72'	'80'	'70'	'02'	-	573440x 1/f _c
xy=08	'05'	'72'	'80'	'80'	'02'	-	1097728x 1/f _c
xy=09	'05'	'72'	'80'	'90'	'02'	-	2146304x 1/f _c
xy=10	'05'	'72'	'80'	'A0'	'02'	-	4243456x 1/f _c
xy=11	'05'	'72'	'80'	'B0'	'02'	-	8437760x 1/f _c
xy=12	'05'	'72'	'80'	'C0'	'02'	-	16826368x 1/f _c
xy=13	'05'	'72'	'80'	'D0'	'02'	-	33603584x 1/f _c
xy=14	'05'	'72'	'80'	'E0'	'02'	-	67158016x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT retransmits the I-Block on which is notified an error).

For each error notification, the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at most $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ▲ '35 D0 6A 75' + 'FA' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '35 D0 6A 75' + 'FA'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ▲ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ▲ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ▲ I(0)₀ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00']	◀ LT
15	PUT ▶ I(1)₁ ['00 A4 04 00 3B' + '01 02 ... 18']	▶ LT Loop-back
16	PUT ▶ R(NAK)₁ sent within $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$ in function of 'xy'	▶ LT Time-out error notification
17	PUT ▲ R(ACK)₀	◀ LT Request for Block repetition
18	PUT ▶ I(1)₁ ['00 A4 04 00 3B' + '01 02 ... 18']	▶ LT Error recovery
19	PUT ▲ R(ACK)₁	◀ LT Acknowledgment R-Block
20	PUT ▶ I(1)₀ ['19 1A 1B ... 33 34 35']	▶ LT Loop-back
21	PUT ▶ R(NAK)₀ sent within $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$ in function of 'xy'	▶ LT Time-out error notification
22	PUT ▲ R(ACK)₁	◀ LT Request for Block repetition

Step	Exchanges		Comments
23	PUT ▶ I(1)₀ ['19 1A 1B ... 33 34 35']	▶ LT	Error recovery
24	PUT ◀ R(ACK)₀	◀ LT	Acknowledgment R-Block
25	PUT ▶ I(0)₁ ['36 37 38 39 3A 3B' + '00']	▶ LT	Last I-Block of the chain
26	PUT ◀ I(0)₁ ['EOT Command' + '90 00']	◀ LT	End Of Test command
27	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT	PICC Reset
28	PUT ▶ '52' (short frame)	▶ LT	WUPA to poll for the PICC
29	PUT ▶ '52' (short frame)	▶ LT	WUPA to poll for the PICC
30	PUT ▶ '52' (short frame)	▶ LT	WUPA to poll for the PICC

Scenario 61: Type A Error notification on an I-Block indicating chaining (xy=00 to 14)

4.37.Type A Time-out after an I-Block indicating chaining [TA406]

Test codification:

TA406

Test objective:

To ensure that the PCD behaves correctly when it does not receive any response to an I-Block indicating chaining.

References Requirements:

4.8.1.8, 10.3.4.3, 10.3.5.8

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

When a single time-out error is generated, the LT measures the delay between the end of the sequence with sent by the PUT before the time-out error and the beginning of the next sequence sent by the PUT to process the error.

When three consecutive time-out errors are generated, the LT measures the delay between the end of the sequence preceding the third time-out and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						(FWT+ΔFWT)
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	114688x 1/f _c (default value)

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends an R(NAK) Block to ask for retransmission when it detects a time-out error after an I-Block indicating chaining).

When a single time-out error is generated, the delay between the end of the sequence with sent by the PUT before the time-out error and the beginning of the next sequence sent by the PUT to process the error is at least $\text{FWT} + \Delta\text{FWT}$ and at most $t_{\text{TIMEOUT}} + t_{\text{RETRANSMISSION}} = \text{FWT} + \Delta\text{FWT} + t_{\text{RETRANSMISSION}}$.

When three consecutive transmission errors are generated, the delay between the end of the sequence preceding the third time-out and the beginning of the PICC Reset initiated by the PUT is at least $\text{FWT} + \Delta\text{FWT}$ at most $t_{\text{TIMEOUT}} + t_{\text{RESETDELAY}} = \text{FWT} + \Delta\text{FWT} + t_{\text{RESETDELAY}}$.

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{\text{RESET,MIN}}$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ▲ '15 04 19 78' + '70' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '15 04 19 78' + '70'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ▲ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ▲ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + '2PAY.SYS.DDF01' + '00']	▶ LT Select PPSE
14	PUT ▲ I(0)₀ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00']	◀ LT
15	PUT ▶ I(1)₁ ['00 A4 04 00 3B' + '01 02 ... 18']	▶ LT Loop-back
16	PUT ▶ R(NAK)₁ sent after FWT+ ΔFWT and before [(FWT+ ΔFWT) + t_{RETRANSMISSION}]	▶ LT Time-out error notification
17	PUT ▲ R(ACK)₁	◀ LT Error recovery
18	PUT ▶ I(1)₀ ['19 1A 1B ... 33 34 35']	▶ LT Loop-back
19	PUT ▶ R(NAK)₀ sent after FWT+ ΔFWT and before [(FWT+ ΔFWT) + t_{RETRANSMISSION}]	▶ LT Time-out error notification

Step	Exchanges	Comments
20	PUT \leftarrow R(ACK) ₀	\leftarrow LT Error recovery
21	PUT \rightarrow I(0) ₁ ['36 37 38 39 3A 3B' + '00']	\rightarrow LT Last I-Block of the chain
22	PUT \leftarrow I(0) ₁ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00']	\leftarrow LT
23	PUT \rightarrow I(1) ₀ ['00 A4 04 00 3B' + '01 02 ... 18']	\rightarrow LT Loop-back
24	PUT \rightarrow R(NAK) ₀	\rightarrow LT Request for Block repetition
25	PUT \rightarrow R(NAK) ₀	\rightarrow LT Request for Block repetition
26	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) The PICC Reset is initiated after FWT+ ΔFWT and before FWT+ ΔFWT + tRESETDELAY The PUT keeps the carrier off during at least tRESET,MIN.	II LT PICC Reset

Scenario 62: Type A time-out after an I-Block indicating chaining

4.38.Type A Transmission error in response to an I-Block indicating chaining [TA407.x]

Test codification:

TA407.x

Test objective:

To ensure that the PCD behaves correctly when it receives a sequence with transmission error in response to an I-Block indicating chaining.

References Requirements:

4.7.1.3, 5.2.1.1, 5.2.1.2, 10.3.5.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

When a single transmission error is generated, the LT measures the delay between the beginning of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When a single transmission error is generated, the LT measures the delay between the end of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When three consecutive transmission errors are generated, the LT measures the delay between the beginning of the third sequence with transmission error and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

The following transmission errors are generated successively by the LT:

- x=4: I-Block of at least 4 bytes with some residual bits (i.e. the total number of bits is not a multiple of 8)

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends an R(NAK) Block when it detects a transmission error after an I-Block indicating chaining and continues the transaction upon receipt of a correct block).

When a single transmission error is generated, the delay between the end of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at least $FDT_{A,PCD,MIN}$.

When a single transmission error is generated, the delay between the beginning of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at most $t_{RETRANSMISSION}$.

When three consecutive transmission errors are generated, the delay between the beginning of the third sequence with transmission error and the beginning of the PICC Reset initiated by the PUT is at most $t_{RESETDELAY}$ (i.e. the PUT stops sending the carrier within $t_{RESETDELAY}$).

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame) ▶ LT	WUPA during polling
2	PUT ↴ '01 00' (no CRC_A) ↴ LT	ATQA
3	PUT ▶ '50 00' ▶ LT	HLTA
4	PUT ▶ '05 00 08' (Type B frame) ▶ LT	WUPB
5	PUT ▶ '52' (short frame) ▶ LT	WUPA
6	PUT ↴ '01 00' (no CRC_A) ↴ LT	ATQA
7	PUT ▶ '93 20' (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ↴ 'EE 0A 3B D7' + '08' (no CRC_A) ↴ LT	UID
9	PUT ▶ '93 70' + 'EE 0A 3B D7' + '08' ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ↴ '20' ↴ LT	SAK
11	PUT ▶ 'E0 80' ▶ LT	RATS
12	PUT ↴ ATS ↴ LT	ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
14	PUT ↴ I(0)₀ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00'] ↴ LT	
15	PUT ▶ I(1)₁ ['00 A4 04 00 3B' + '01 02 ... 18'] ▶ LT	Loop-back
16	PUT ↴ S(WTX Request) [WTXM='01'] with a transmission error in function of 'x' ↴ LT	Error in function of 'x'
17	PUT ▶ R(NAK)₁ sent after FDT_{A,PCD,MIN} and within t_{RETRANSMISSION} ▶ LT	Request for Block repetition
18	PUT ↴ R(ACK)₁ ↴ LT	Error recovery
19	PUT ▶ I(1)₀ ['19 1A 1B ... 33 34 35'] ▶ LT	Loop-back
20	PUT ↴ S(WTX Request) [WTXM='01'] with a transmission error in function of 'x' ↴ LT	Error in function of 'x'

Step	Exchanges	Comments
21	PUT ▶ R(NAK)₀ sent after FDT_{A,PCD,MIN} and within t_{RETRANSMISSION}	▶ LT Request for Block repetition
22	PUT ◀ R(ACK)₀	◀ LT Error recovery
23	PUT ▶ I(0)₁ ['36 37 38 39 3A 3B' + '00']	▶ LT Last I-Block of the chain
24	PUT ◀ I(0)₁ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00']	◀ LT
25	PUT ▶ I(1)₀ ['00 A4 04 00 3B' + '01 02 ... 18']	▶ LT Loop-back
26	PUT ◀ S(WTX Request) [WTXM='01'] with a transmission error in function of 'x'	◀ LT Error in function of 'x'
27	PUT ▶ R(NAK)₀	▶ LT Request for Block repetition
28	PUT ◀ S(WTX Request) [WTXM='01'] with a transmission error in function of 'x'	◀ LT Error in function of 'x'
29	PUT ▶ R(NAK)₀	▶ LT Request for Block repetition
30	PUT ◀ S(WTX Request) [WTXM='01'] with a transmission error in function of 'x'	◀ LT Error in function of 'x'
31	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) The PICC Reset is initiated within t_{RESETDELAY} The PUT keeps the carrier off during at least t_{RESET,MIN}	II LT PICC Reset

**Scenario 63: Type A Transmission error in response to an I-Block indicating chaining
(x= 4)**

4.39.Type A Protocol error in response to an I-Block indicating chaining [TA408.xy]

Test codification:

TA408.xy

Test objective:

To ensure that the PCD behaves correctly when it receives a protocol error in response to an I-Block indicating chaining.

References Requirements:

10.1.5.1, 10.2.1.1, 10.2.2.1, 10.3.4.6, 10.3.5.7, 10.3.5.9, 10.1.2.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

xy=09 is Not Applicable if the PCD implements a legacy behavior by accepting R-Blocks with b2 of PCB set to '0' (see ICS).

Procedure:

Run the following scenario.

The LT measures the delay between the beginning of the sequence inducing a protocol error and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The following protocol errors are generated successively by the LT:

- xy=00: R(ACK) Block with bit b₆ of the PCB equal to '0'
- xy=01: R(NAK) Block (b₅=1 in PCB)
- xy=02: R(ACK) Block with bit b₄ of the PCB equal to '1' (i.e. CID following)
- xy=03: R(ACK) Block with bit b₃ of the PCB equal to '1' (i.e. NAD following)
- xy=04: I-Block
- xy=05: S(DESELECT) response
- xy=06: S(WTX) Request with WTXM = 0
- xy=07: S(WTX) Request with WTXM = 1 and with bit b₂ of PCB equal to (0)_b
- xy=08: S(WTX) Request with WTXM = 63
- xy=09: R(ACK) Block with bit b₂ of the PCB equal to '0' (See "Conditions")
- xy=11: S(WTX) Request with b₆-b₅ of the PCB set to 01_b, with WTXM =1
- xy=12: S(WTX) Request with b₆-b₅ of the PCB set to 10_b, with WTXM =1

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT initiates a PICC Reset when it detects a protocol error after an I-Block indicating chaining).

The delay between the beginning of the sequence inducing a protocol error and the beginning of the PICC Reset initiated by the PUT is at most $t_{RESETDELAY}$ (i.e. the PUT stops sending the carrier within $t_{RESETDELAY}$).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ 'DA 02 DE 12' + '14' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + 'DA 02 DE 12' + '14'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0)0 ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ◀ I(0)0 ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00']	◀ LT
15	PUT ▶ I(1)1 ['00 A4 04 00 3B' + '01 02 ... 18']	▶ LT Loop-back

Step	Exchanges	Comments
16	<p>Protocol error in function of 'x'</p> <p>For xy=00: R(ACK)₁ with b₆=0 in PCB</p> <p>For xy=01: R(NAK)₁</p> <p>For xy=02: R(ACK)₁ with b₄=1 in PCB</p> <p>For xy=03: R(ACK)₁ with b₃=1 in PCB</p> <p>For xy=04: I(0)₀ ['00 B2 01 04 00' + '90 00']</p> <p>For xy=05: S(DESELECT) Response</p> <p>PUT ↳ For xy=06: S(WTX Request) [WTXM='00'] ◀ LT</p> <p>For xy=07: S(WTX Request) [WTXM='01'] and bit b₂ of PCB equal to (0)_b</p> <p>For xy=08: S(WTX Request) [WTXM='3F']</p> <p>For xy=09: R(ACK)₁ with b₂=0 in PCB (See "Conditions")</p> <p>For xy=11: S(WTX Request) with b₆-b₅ set to 01_b in PCB, with WTXM =1</p> <p>For xy=12: S(WTX Request) with b₆-b₅ set to 10_b in PCB, with WTXM =1</p>	Error in function of 'xy'
17	<p>PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)</p> <p>The PICC Reset is initiated within tRESETDELAY LT</p>	PICC Reset

**Scenario 64: Type A Protocol error in response to an I-Block indicating chaining
(xy=00 to 09 and 11 to12)**

4.40.Type A Time-out after an R(ACK) Block (i.e. error notification) [TA409.xy]

Test codification:

TA409.xy

Test objective:

To ensure that the PCD behaves correctly when it does not receive any response to an R(ACK) Block sent to acknowledge a chained I-Block.

References Requirements:

4.8.1.8, 10.3.5.9

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

When a single time-out error is generated, the LT measures the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

When two consecutive time-out errors are generated, the LT measures the delay between the end of the second sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

When three consecutive time-out errors are generated, the LT measures the delay between the end of the third sequence to which the LT does not respond and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

In this test, the following ATS shall be used:

	ATS						(FWT+ΔFWT)
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
xy=00	'05'	'72'	'80'	'00'	'02'	-	53248 x 1/f _c
xy=01	'05'	'72'	'80'	'10'	'02'	-	57344x 1/f _c
xy=02	'05'	'72'	'80'	'20'	'02'	-	65536x 1/f _c
xy=03	'05'	'72'	'80'	'30'	'02'	-	81920 x 1/f _c
xy=04	'05'	'72'	'80'	'40'	'02'	-	114688x 1/f _c (default value)
xy=05	'05'	'72'	'80'	'50'	'02'	-	180224x 1/f _c
xy=06	'05'	'72'	'80'	'60'	'02'	-	311296x 1/f _c
xy=07	'05'	'72'	'80'	'70'	'02'	-	573440x 1/f _c
xy=08	'05'	'72'	'80'	'80'	'02'	-	1097728x 1/f _c
xy=09	'05'	'72'	'80'	'90'	'02'	-	2146304x 1/f _c

	ATS						$(FWT + \Delta FWT)$
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
xy=10	'05'	'72'	'80'	'A0'	'02'	-	4243456x 1/f _c
xy=11	'05'	'72'	'80'	'B0'	'02'	-	8437760x 1/f _c
xy=12	'05'	'72'	'80'	'C0'	'02'	-	16826368x 1/f _c
xy=13	'05'	'72'	'80'	'D0'	'02'	-	33603584x 1/f _c
xy=14	'05'	'72'	'80'	'E0'	'02'	-	67158016x 1/f _c
xy=15	'05'	'72'	'80'	'F0'	'02'	-	114688x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT retransmits the R(ACK) Block up to two times when it detects a time-out error after an R(ACK) Block and initiates a PICC Reset when it detects a third consecutive time-out error).

When a single time-out error is generated, the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at most $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$.

When two consecutive time-out errors are generated, the delay between the end of the second sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at most $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$.

When three consecutive time-out errors are generated, the delay between the end of the third sequence to which the LT does not respond and the beginning of the PICC Reset initiated by the PUT is at most $[(FWT + \Delta FWT) + t_{RESETDELAY}]$ (i.e. the PUT stops sending the carrier within $[(FWT + \Delta FWT) + t_{RESETDELAY}]$).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ▲ '11 7C E5 88' + '00' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '11 7C E5 88' + '00'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ▲ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS

Step	Exchanges	Comments
12	PUT ↣ ATS ↣ LT	ATS
13	PUT ↢ I(0)₀ ['00 A4 04 00 0E' + '2PAY.SYS.DDF01' + '00'] ↣ LT	Select PPSE
14	PUT ↣ I(1)₀ ['00 A4 04 00 50' + '01 02 03 ... 06 07 08'] ↣ LT	
15	PUT ↢ R(ACK)₁ ↣ LT	Acknowledgment R-Block
16	PUT ↢ R(ACK)₁ sent within [(FWT+ ΔFWT) + t _{RETRANSMISSION}] in function of 'xy' ↣ LT	Time-out error notification
17	PUT ↣ I(1)₁ ['09 0A 0B ... 13 14 15'] ↣ LT	Error recovery
18	PUT ↢ R(ACK)₀ ↣ LT	Acknowledgment R-Block
19	PUT ↢ R(ACK)₀ sent within [(FWT+ ΔFWT) + t _{RETRANSMISSION}] in function of 'xy' ↣ LT	Time-out error notification
20	PUT ↣ I(1)₀ ['16 17 18 ... 20 21 22'] ↣ LT	Error recovery
21	PUT ↢ R(ACK)₁ ↣ LT	Acknowledgment R-Block
22	PUT ↢ R(ACK)₁ ↣ LT	Time-out error notification
23	PUT ↢ R(ACK)₁ sent within [(FWT+ ΔFWT) + t _{RETRANSMISSION}] in function of 'xy' ↣ LT	Time-out error notification
24	PUT ↣ I(1)₁ ['23 24 25 ... 2D 2E 2F'] ↣ LT	Error recovery
25	PUT ↢ R(ACK)₀ ↣ LT	Acknowledgment R-Block
26	PUT ↢ R(ACK)₀ ↣ LT	Time-out error notification
27	PUT ↢ R(ACK)₀ sent within [(FWT+ ΔFWT) + t _{RETRANSMISSION}] in function of 'xy' ↣ LT	Time-out error notification
28	PUT ↣ I(1)₀ ['30 31 32 ... 3A 3B 3C'] ↣ LT	Error recovery
29	PUT ↢ R(ACK)₁ ↣ LT	Acknowledgment R-Block
30	PUT ↢ R(ACK)₁ ↣ LT	Time-out error notification
31	PUT ↢ R(ACK)₁ ↣ LT	Time-out error notification
32	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) The PICC Reset is initiated within [(FWT+ ΔFWT) + t _{RESETDELAY}] in function of 'xy'	II LT PICC Reset

Scenario 65: Type A Time-out after an R(ACK) Block (i.e. error notification) (xy=00 to 15)

4.41.Type A Transmission error in response to an R(ACK) Block [TA410.x]

Test codification:

TA410.x

Test objective:

To ensure that the PCD behaves correctly when it receives a transmission error in response to an R(ACK) Block sent to acknowledge a chained I-Block.

References Requirements:

4.7.1.3, 5.2.1.1, 5.2.1.2, 10.3.5.6, 10.3.5.9

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

When a single transmission error is generated, the LT measures the delay between the beginning of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When a single transmission error is generated, the LT measures the delay between the end of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When two consecutive transmission errors are generated, the LT measures the delay between the beginning of the second sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When two consecutive transmission errors are generated, the LT measures the delay between the end of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When three consecutive transmission errors are generated, the LT measures the delay between the beginning of the third sequence with transmission error and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The following transmission errors are generated successively by the LT:

- x=0: I-Block (in a frame of at least 4 bytes) with CRC error: the less significant bit of the 1st CRC byte is corrupted for the 1st, 4th and 7th error generated, the less significant bit of the 2nd CRC byte is corrupted for the 2nd, 5th and 8th error generated, the most significant bit of the 2nd CRC byte is corrupted for the 3rd, 6th and 9th error generated and for each error generated, the parity bit of the corrupted CRC byte is adapted in order to have only a CRC error
- x=1: I-Block (in a frame of at least 4 bytes) with parity error (corrupted parity bit) on the following bytes: the 5th byte of the frame for the 1st and 7th errors generated, the 5th byte of the INF field for the 2nd to 4th errors generated, the 1st CRC byte (one byte before the last byte of the frame) for the 5th and 8th error generated and the 2nd byte of the CRC (last byte of the frame) for the 6th and 9th error generated

- x=2: I-Block (in a frame of at least 4 bytes) with parity/CRC errors combination: a single bit is corrupted on the 5th byte (not the CRC bytes) at a different position from one frame with error to another inducing both a parity and a CRC error
- x=4: I-Block of at least 4 bytes with some residual bits (i.e. the total number of bits is not a multiple of 8)

In this test, the following ATS shall be used:

ATS						Maximum Frame Size for the PICC (FSC)
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'78'	'80'	'40'	'02'	-	256 bytes

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT retransmits the R(ACK) Block up to two times when it detects a transmission error and initiates a PICC Reset when it detects a third consecutive transmission error).

When a single transmission error is generated, the delay between the end of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at least FDT_{A,PCD,MIN}.

When a single transmission error is generated, the delay between the beginning of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at most t_{RETRANSMISSION}.

When two consecutive transmission errors are generated, the delay between the end of the second sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at least FDT_{A,PCD,MIN}.

When two consecutive transmission errors are generated, the delay between the beginning of the second sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at most t_{RETRANSMISSION}.

When three consecutive transmission errors are generated, the delay between the beginning of the third sequence with transmission error and the beginning of the PICC Reset initiated by the PUT is at most t_{RESETDELAY} (i.e. the PUT stops sending the carrier within t_{RESETDELAY}).

The delay between the end of a sequence sent by the LT and the beginning of the sequence replied by the PUT is at least FDT_{A,PCD,MIN} during installation and block protocol.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ '44 3B EC 10' + '83' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '44 3B EC 10' + '83'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + '2PAY.SYS.DDF01' + '00']	▶ LT Select PPSE
14	PUT ◀ I(1)₀ ['00 A4 04 00 50' + '01 02 03 ... 06 07 08']	◀ LT
15	PUT ▶ R(ACK)₁	▶ LT Acknowledgement R-Block
16	PUT ◀ I(1)₁ ['09 0A 0B ... 13 14 15'] with a transmission error in function of 'x'	◀ LT Error in function of 'x'
17	PUT ▶ R(ACK)₁ sent after FDT_{A,PCD,MIN} and within t_{RETRANSMISSION}	▶ LT Error notification
18	PUT ◀ I(1)₁ ['09 0A 0B ... 13 14 15']	◀ LT Error recovery
19	PUT ▶ R(ACK)₀	▶ LT Acknowledgement R-Block
20	PUT ◀ I(1)₀ ['16 17 18 ... 20 21 22'] with a transmission error in function of 'x'	◀ LT Error in function of 'x'
21	PUT ▶ R(ACK)₀ sent after FDT_{A,PCD,MIN} and within t_{RETRANSMISSION}	▶ LT Error notification
22	PUT ◀ I(1)₀ ['16 17 18 ... 20 21 22']	◀ LT Error recovery
23	PUT ▶ R(ACK)₁	▶ LT Acknowledgement R-Block
24	PUT ◀ I(1)₁ ['23 24 25 ... 2D 2E 2F'] with a transmission error in function of 'x'	◀ LT Error in function of 'x'
25	PUT ▶ R(ACK)₁	▶ LT Error notification
26	PUT ◀ I(1)₁ ['23 24 25 ... 2D 2E 2F'] with a transmission error in function of 'x'	◀ LT Error in function of 'x'
27	PUT ▶ R(ACK)₁ sent after FDT_{A,PCD,MIN} and within t_{RETRANSMISSION}	▶ LT Error notification
28	PUT ◀ I(1)₁ ['23 24 25 ... 2D 2E 2F']	◀ LT Error recovery

Step	Exchanges	Comments
29	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgement R-Block
30	PUT ↴ I(1)₀ ['30 31 32 ... 3A 3B 3C'] with a transmission error in function of 'x' ↴ LT	Error in function of 'x'
31	PUT ▶ R(ACK)₀ ▶ LT	Error notification
32	PUT ↴ I(1)₀ ['30 31 32 ... 3A 3B 3C'] with a transmission error in function of 'x' ↴ LT	Error in function of 'x'
33	PUT ▶ R(ACK)₀ sent after FDT_{A,PCD,MIN} and within t_{RETRANSMISSION} ▶ LT	Error notification
34	PUT ↴ I(1)₀ ['30 31 32 ... 3A 3B 3C'] ↴ LT	Error recovery
35	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgement R-Block
36	PUT ↴ I(1)₁ ['3D 3E 3F ... 47 48 49'] with a transmission error in function of 'x' ↴ LT	Error in function of 'x'
37	PUT ▶ R(ACK)₁ ▶ LT	Error notification
38	PUT ↴ I(1)₁ ['3D 3E 3F ... 47 48 49'] with a transmission error in function of 'x' ↴ LT	Error in function of 'x'
39	PUT ▶ R(ACK)₁ ▶ LT	Error notification
40	PUT ↴ I(1)₁ ['3D 3E 3F ... 47 48 49'] with a transmission error in function of 'x' ↴ LT	Error in function of 'x'
41	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) The PICC Reset is initiated within t _{RESETDELAY}	II LT PICC Reset

Scenario 66: Type A Transmission error in response to an R(ACK) Block (x=0 to 2 and 4)

4.42.Type A Protocol error in response to an R(ACK) Block [TA411.xy]

Test codification:

TA411.xy

Test objective:

To ensure that the PCD behaves correctly when it receives a protocol error in response to an R(ACK) Block.

References Requirements:

4.7.3.1, 10.1.1.3, 10.1.5.1, 10.2.1.1, 10.2.2.1, 10.3.4.5, 10.3.4.6, 10.3.5.4, 10.3.5.9, 10.1.2.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

xy=11 is Not Applicable if the PCD implements a legacy behavior by accepting I-Blocks with b6 of PCB set to '1' (see ICS).

Procedure:

Run the following scenario.

The LT measures the delay between the beginning of the sequence inducing a protocol error and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The following protocol errors are generated successively by the LT:

- xy=00: I-Block with bit b₂ of the PCB equal to '0'
- xy=01: I-Block with bit b₄ of the PCB equal to '1' (i.e. CID following)
- xy=02: I-Block with bit b₃ of the PCB equal to '1' (i.e. NAD following)
- xy=03: I-Block with wrong Block number indicated in the PCB
- xy=04: I-Block of length > FSD
- xy=05: R(NAK) Block
- xy=06: R(ACK) Block with a Block number different from the one of the last Block sent by the LT
- xy=07: S(DESELECT) response
- xy=08: S(WTX) Request with WTXM = 0
- xy=09: S(WTX) Request with WTXM = 1 and with bit b₂ of PCB equal to (0)_b
- xy=10: S(WTX) Request with WTXM = 61
- xy=11: I-Block with bit b₆ of the PCB equal to '1' (See "Conditions")
- xy=13: S(WTX) Request with b₆-b₅ of the PCB set to 01_b, with WTXM =1
- xy=14: S(WTX) Request with b₆-b₅ of the PCB set to 10_b, with WTXM =1
- xy=15: I-Block with b₈-b₇ of the PCB set to 01_b

In this test, the following ATS shall be used:

ATS						Maximum Frame Size for the PICC (FSC)
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'78'	'80'	'40'	'02'	-	256 bytes

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT initiates a PICC Reset when it detects a protocol error after an R(ACK) Block).

The delay between the beginning of the sequence inducing a protocol error and the beginning of the PICC Reset initiated by the PUT is at most $t_{RESETDELAY}$ (i.e. the PUT stops sending the carrier within $t_{RESETDELAY}$).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ '80 88 E5 B2' + '5F' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '80 88 E5 B2' + '5F'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0) ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ◀ I(1) ['00 A4 04 00 14' + '01 02 03 ... 06 07 08']	◀ LT
15	PUT ▶ R(ACK)	Acknowledgement R-Block

Step	Exchanges	Comments
16	<p>Protocol error in function of 'xy'</p> <p>For xy=00: I(0)₁ ['00 B2 02 04 00' + '90 00'] with b₂=0 in PCB</p> <p>For xy=01: I(0)₁ ['00 B2 02 04 00' + '90 00'] with b₄=1 in PCB</p> <p>For xy=02: I(0)₁ ['00 B2 02 04 00' + '90 00'] with b₃=1 in PCB</p> <p>For xy=03: I(0)₀ ['00 B2 02 04 00' + '90 00']</p> <p>For xy=04: I(0)₁ ['00 A4 04 00 F7' + '00 ... F6' + '00' + '90 00']</p> <p>For xy=05: R(NAK)1</p> <p>For xy=06: R(ACK)1</p> <p>For xy=07: S(DESELECT) response</p> <p>PUT I</p> <p>For xy=08: S(WTX Request) [WTXM='00'] ◀ LT</p> <p>For xy=09: S(WTX Request) [WTXM='01'] and bit b₂ of PCB equal to (0)_b</p> <p>For xy=10: S(WTX Request) [WTXM='3D']</p> <p>For xy=11: I(0)₁ ['00 B2 02 04 00' + '90 00'] with b₆=1 in PCB (See "Conditions")</p> <p>For xy=13: S(WTX Request) with b₆-b₅ set to 01_b in PCB, with WTXM =1</p> <p>For xy=14: S(WTX Request) with b₆-b₅ set to 10_b in PCB, with WTXM =1</p> <p>For xy=15: I(0)₁ ['00 B2 02 04 00' + '90 00'] with b₈-b₇ set to 01_b in PCB</p>	Error in function of 'x'
17	<p>PUT II</p> <p>The PUT performs a PICC Reset (i.e. stops sending the carrier)</p> <p>The PICC Reset is initiated within t_{RESETDELAY}</p>	PICC Reset

Scenario 67: Type A Protocol error in response to an R(ACK) Block (xy=00 to 11 and 13 to 15)

4.43.Type A Single time-out after an S(WTX) Response Block (several values of WTXM) [TA412.xy]

Test codification:

TA412.xy

Test objective:

To ensure that the PCD behaves correctly when it does not receive any response to a S(WTX) Response Block.

References Requirements:

10.2.2.7, 10.3.5.5

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

For each time-out error generated, the LT measures the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

In this test, the following ATS shall be used:

	ATS						(FWT+ΔFWT)
	TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
xy=00	'05'	'72'	'80'	'00'	'02'	-	53248 x 1/f _c
xy=01	'05'	'72'	'80'	'10'	'02'	-	57344x 1/f _c
xy=02	'05'	'72'	'80'	'20'	'02'	-	65536x 1/f _c
xy=03	'05'	'72'	'80'	'30'	'02'	-	81920 x 1/f _c
xy=04	'05'	'72'	'80'	'40'	'02'	-	114688x 1/f _c (default value)
xy=05	'05'	'72'	'80'	'50'	'02'	-	180224x 1/f _c
xy=06	'05'	'72'	'80'	'60'	'02'	-	311296x 1/f _c
xy=07	'05'	'72'	'80'	'70'	'02'	-	573440x 1/f _c
xy=08	'05'	'72'	'80'	'80'	'02'	-	1097728x 1/f _c
xy=09	'05'	'72'	'80'	'90'	'02'	-	2146304x 1/f _c
xy=10	'05'	'72'	'80'	'A0'	'02'	-	4243456x 1/f _c
xy=11	'05'	'72'	'80'	'B0'	'02'	-	8437760x 1/f _c
xy=12	'05'	'72'	'80'	'C0'	'02'	-	16826368x 1/f _c
xy=13	'05'	'72'	'80'	'D0'	'02'	-	33603584x 1/f _c
xy=14	'05'	'72'	'80'	'E0'	'02'	-	67158016x 1/f _c

The corresponding extended Frame Waiting Time is as follows:

- $FWT_{EXT} + \Delta FWT = (FWT \times WTXM) + \Delta FWT$ with $FWT \times WTXM \leq FWT_{MAX}$

And we define:

- $FWT_{EXT1} + \Delta FWT$ corresponding to $WTXM_1$
- $FWT_{EXT2} + \Delta FWT$ corresponding to $WTXM_2$
- $FWT_{EXT3} + \Delta FWT$ corresponding to $WTXM_3$

Which leads to:

xy	WTXM₁	FWT_{EXT1+ΔFWT}	WTXM₂	FWT_{EXT2+ΔFWT}	WTXM₃	FWT_{EXT3+ΔFWT}
00	59	$290816 \times 1/f_c$	57	$282624 \times 1/f_c$	56	$278528 \times 1/f_c$
01	59	$532480 \times 1/f_c$	54	$491520 \times 1/f_c$	51	$466944 \times 1/f_c$
02	58	$999424 \times 1/f_c$	55	$950272 \times 1/f_c$	53	$917504 \times 1/f_c$
03	52	$1753088 \times 1/f_c$	50	$1687552 \times 1/f_c$	48	$1622016 \times 1/f_c$
04	47	$3129344 \times 1/f_c$	45	$2998272 \times 1/f_c$	42	$2801664 \times 1/f_c$
05	40	$5292032 \times 1/f_c$	38	$5029888 \times 1/f_c$	36	$4767744 \times 1/f_c$
06	35	$9224192 \times 1/f_c$	33	$8699904 \times 1/f_c$	30	$7913472 \times 1/f_c$
07	29	$15253504 \times 1/f_c$	27	$14204928 \times 1/f_c$	26	$13680640 \times 1/f_c$
08	25	$26263552 \times 1/f_c$	22	$23117824 \times 1/f_c$	20	$21020672 \times 1/f_c$
09	18	$37797888 \times 1/f_c$	15	$31506432 \times 1/f_c$	12	$25214976 \times 1/f_c$
10	10	$41992192 \times 1/f_c$	9	$37797888 \times 1/f_c$	8	$33603584 \times 1/f_c$
11	7	$58769408 \times 1/f_c$	6	$50380800 \times 1/f_c$	5	$41992192 \times 1/f_c$
12	4	$67158016 \times 1/f_c$	3	$50380800 \times 1/f_c$	2	$33603584 \times 1/f_c$
13	2	$67158016 \times 1/f_c$	2	$67158016 \times 1/f_c$	1	$33603584 \times 1/f_c$
14	1	$67158016 \times 1/f_c$	1	$67158016 \times 1/f_c$	1	$67158016 \times 1/f_c$

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends an R(NAK) Block to ask for retransmission when it detects a time-out error after an S(WTX) Response).

At step 18 of the following scenario, the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at most $[FWT_{EXT1} + \Delta FWT + t_{RETRANSMISSION}]$.

At step 23 of the following scenario, the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at most $[FWT_{EXT2} + \Delta FWT + t_{RETRANSMISSION}]$.

At step 28 of the following scenario, the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at most $[FWT_{EXT3} + \Delta FWT + t_{RETRANSMISSION}]$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ 'FB 29 EF 53' + '6E' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + 'FB 29 EF 53' + '6E'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ◀ I(0)₀ ['00 B2 01 04 00' + '90 00']	◀ LT
15	PUT ▶ I(0)₁ ['00 B2 01 04 00']	▶ LT Loop-back
16	PUT ◀ S(WTX Request) [WTXM₁] with WTXM ₁ in function of 'xy'	◀ LT WTXM ₁ in function of 'xy'
17	PUT ▶ S(WTX Response) [WTXM₁]	▶ LT WTX acknowledgment
18	PUT ▶ R(NAK)₁ sent within [FWT _{EXT1} +ΔFWT + t _{RETRANSMISSION}] in function of 'xy'	▶ LT Time-out error notification
19	PUT ◀ I(0)₁ ['00 A4 04 00 05+ 'C1 C2 ... C5' + '00' + '90 00']	◀ LT Error recovery
20	PUT ▶ I(0)₀ ['00 A4 04 00 05+ 'C1 C2 ... C5' + '00']	▶ LT Loop-back
21	PUT ◀ S(WTX Request) [WTXM₂] with WTXM ₂ in function of 'xy'	◀ LT WTXM ₂ in function of 'xy'
22	PUT ▶ S(WTX Response) [WTXM₂]	▶ LT WTX acknowledgment
23	PUT ▶ R(NAK)₀ sent within [FWT _{EXT2} +ΔFWT + t _{RETRANSMISSION}] in function of 'xy'	▶ LT Time-out error notification
24	PUT ◀ I(0)₀ ['00 A4 04 00 05+ 'C6 C7 ... CA' + '00' + '90 00']	◀ LT Error recovery
25	PUT ▶ I(0)₁ ['00 A4 04 00 05+ 'C6 C7 ... CA' + '00']	▶ LT Loop-back
26	PUT ◀ S(WTX Request) [WTXM₃] with WTXM ₃ in function of 'xy'	◀ LT WTXM ₃ in function of 'xy'
27	PUT ▶ S(WTX Response) [WTXM₃]	▶ LT WTX acknowledgment

Step	Exchanges	Comments
28	PUT ▶ R(NAK)₁ sent within [FWT _{EXT3} +ΔFWT + t _{RETRANSMISSION}] in function of 'xy' ▶ LT	Time-out error notification
29	PUT ◀ I(0)₁ ['00 A4 04 00 05+ 'CB CC ... CF' + '00' + '90 00'] ◀ LT	Error recovery
30	PUT ▶ I(0)₀ ['00 A4 04 00 05+ 'CB CC ... CF' + '00'] ▶ LT	Loop-back
31	PUT ◀ I(0)₀ ["EOT Command" + '90 00'] ◀ LT	End Of Test command
32	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
33	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
34	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
35	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC

Scenario 68: Type A Single time-out after an S(WTX) Response Block (i.e. several values of WTXM) (xy=00 to 14)

4.44. Type A Repeated use of a FWT Extension after a single S(WTX) Request [TA413]

Test codification:

TA413

Test objective:

To ensure that the PCD applies the Frame Waiting Time Extension only until the next Block has been received.

References Requirements:

10.2.2.9, 10.3.5.5

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

After reception of a S(WTX) Response, the LT sends the next Block within the extended Frame Waiting Time $FWT_{EXT} + \Delta FWT = [(4096 \times WTXM) + 49152] \times 1/f_c$ as $FWT_{EXT} = 4096 \times 1/f_c$ and $\Delta FWT = 49152 \times 1/f_c$.

Remark: the next block is sent using a Frame Delay Time aligned to the grid defined by EMV Contactless for a Type A PICC.

Upon receipt of the next Block sent by the PUT, the LT stays mute and exceeds the Frame Waiting Time ($FWT + \Delta FWT$) (as if the LT uses the FWT extension a 2nd time).

For each time-out error generated, the LT measures the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

In this test, the following ATS shall be used:

ATS						(FWT+ΔFWT)
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'00'	'02'	-	53248x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends an R(NAK) Block to signal an error when the LT uses the Frame Waiting Time Extension a second consecutive time).

When a time-out error is generated, the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at most $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ 'B0 23 BA 19' + '30' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + 'B0 23 BA 19' + '30'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + '2PAY.SYS.DDF01' + '00']	▶ LT Select PPSE
14	PUT ◀ I(0)₀ ['00 B2 01 04 00' + '90 00']	◀ LT
15	PUT ▶ I(0)₁ ['00 B2 01 04 00']	▶ LT Loop-back
16	PUT ◀ S(WTX Request) [WTXM='14']	◀ LT WTXM = 20
17	PUT ▶ S(WTX Response) [WTXM='14']	▶ LT WTX acknowledgment
18	PUT ◀ I(0)₁ ['00 A4 04 00 05+ 'E1 E2 ... E5' + '00' + '90 00']	◀ LT Sent with the default FDT
19	PUT ▶ I(0)₀ ['00 A4 04 00 05+ 'E1 E2 ... E5' + '00']	▶ LT Loop-back
20	PUT ▶ R(NAK)₀ sent within [(FWT+ΔFWT) + t_{RETRANSMISSION}]	▶ LT Time-out error notification
21	PUT ◀ I(0)₀ ['00 A4 04 00 05' + 'E6 E7 ... EA' + '00' + '90 00']	◀ LT Error recovery
22	PUT ▶ I(0)₁ ['00 A4 04 00 05' + 'E6 E7 ... EA' + '00']	▶ LT Loop-back
23	PUT ◀ S(WTX Request) [WTXM='28']	◀ LT WTXM = 40
24	PUT ▶ S(WTX Response) [WTXM='28']	▶ LT WTX acknowledgment
25	PUT ◀ I(0)₁ ['00 A4 04 00 05+ 'EB EC ... EF' + '00' + '90 00']	◀ LT Sent with the default FDT
26	PUT ▶ I(0)₀ ['00 A4 04 00 05+ 'EB EC ... EF' + '00']	▶ LT Loop-back
27	PUT ▶ R(NAK)₀ sent within [(FWT+ΔFWT) + t_{RETRANSMISSION}]	▶ LT Time-out error notification
28	PUT ◀ I(0)₀ ['00 A4 04 00 05' + 'F1 F2 ... F5' + '00' + '90 00']	◀ LT Error recovery
29	PUT ▶ I(0)₁ ['00 A4 04 00 05' + 'F1 F2 ... F5' + '00']	▶ LT Loop-back

Step	Exchanges	Comments
30	PUT ↪ S(WTX Request) [WTXM='3B'] ↪ LT	WTXM = 59
31	PUT ↪ S(WTX Response) [WTXM='3B'] ↪ LT	WTX acknowledgment
32	PUT ↪ I(0)₁ ['00 A4 04 00 05+ 'F6 F7 ... FA' + '00' + '90 00'] ↪ LT	Sent with the default FDT
33	PUT ↪ I(0)₀ ['00 A4 04 00 05+ 'F6 F7 ... FA' + '00'] ↪ LT	Loop-back
34	PUT ↪ R(NAK)₀ sent within [(FWT+ΔFWT) + t_{RETRANSMISSION}] ↪ LT	Time-out error notification
35	PUT ↪ I(0)₀ ['00 A4 04 00 05' + 'FB FC ... FF' + '00' + '90 00'] ↪ LT	Error recovery
36	PUT ↪ I(0)₁ ['00 A4 04 00 05' + 'FB FC ... FF' + '00'] ↪ LT	Loop-back
37	PUT ↪ I(0)₁ ["EOT Command" + '90 00'] ↪ LT	End Of Test command
38	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) ↪ LT	PICC Reset
39	PUT ↪ '52' (short frame) ↪ LT	WUPA to poll for the PICC
40	PUT ↪ '52' (short frame) ↪ LT	WUPA to poll for the PICC
41	PUT ↪ '52' (short frame) ↪ LT	WUPA to poll for the PICC

Scenario 69: Type A Repeated use of a FWT Extension after a single S(WTX) Request

4.45.Type A ‘Noise’ in response to an I-Block not indicating chaining [TA414.x]

Test codification:

TA414.x

Test objective:

To ensure that the PCD behaves correctly when it receives some ‘noise’ (i.e. a frame with a transmission error to be processed as noise by the PCD) in response to an I-Block not indicating chaining.

References Requirements:

4.9.2.1, 5.2.1.1, 5.2.1.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT replies to an I-Block not indicating chaining sent by the PUT with a sequence inducing a ‘noise’ error sent using a delay of ($FDT_{A,PICC,MIN} + 128/f_c$) between the end of the sequence sent by the PUT and the beginning of the ‘noise’ error generated by the LT.

The LT measures the delay between the end of the sequence sent by the PUT after which a ‘noise’ error is generated and the beginning of the next sequence sent by the PUT to process the error.

The following ‘noise’ errors are generated successively by the LT:

- x=0: Erroneous block of less than 4 bytes (PCB inducing a protocol error) with CRC error (the CRC bytes are corrupted and the parity bits of the CRC bytes are adapted in order to have only a CRC error)
- x=1: Erroneous block of less than 4 bytes (PCB inducing a protocol error) with parity error (a single parity bit is corrupted on any byte)
- x=2: Erroneous block of less than 4 bytes (PCB inducing a protocol error) with some residual bits (i.e. the total number of bits is not a multiple of 8)
- x=4: Continuous modulation of the PUT carrier with a frequency equal to $f_s = f_c/16$, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of $4736 \times 1/f_c$ (i.e. duration of a 4 bytes frame in Type A)

In this test, the following ATS shall be used:

ATS						(FWT+ΔFWT)
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	(FWT+ΔFWT)
‘05’	‘72’	‘80’	‘70’	‘02’	-	573440x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT ignores the ‘noise’ error, notifies a time-out error and continues the transaction upon receipt of a correct block).

The delay between the end of the sequence sent by the PUT after which a ‘noise’ error is generated and the beginning of the next sequence sent by the PUT to process the error is at least $(FWT + \Delta FWT)$ and at most $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ▲ 'E7 98 3B DE' + '9A' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + 'E7 98 3B DE' + '9A'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ▲ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ▲ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ▲ I(0)₀ ['00 B2 01 04 00' + '90 00']	◀ LT
15	PUT ▶ I(0)₁ ['00 B2 01 04 00']	▶ LT Loop-back
16	PUT ▲ For x=0 to 1: 'FF' with a transmission error in function of 'x' For x=2: 'FF' with 3 bits to $(101)_b$ following the CRC bytes For x=4: Block replaced by a continuous subcarrier modulation with a duration of $4736 \times 1/f_c$	◀ LT Error in function of 'x'
17	PUT ▶ R(NAK)₁ sent between $(FWT + \Delta FWT)$ and $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$ measured from the end of the last sequence from the PUT	▶ LT Request for Block repetition
18	PUT ▲ I(0)₁ ['00 B2 02 04 00' + '90 00']	◀ LT Error recovery
19	PUT ▶ I(0)₀ ['00 B2 02 04 00']	▶ LT Loop-back

Step	Exchanges	Comments
20	<p>'Noise' error in function of 'x' sent using a delay of ($FDT_{A,PICC,MIN} + 128/f_c$) between the end of the sequence sent by the PUT and the beginning of the error</p> <p>PUT ↶ For $x=0$ to 1: 'FF' with transmission error in function of 'x' For $x=2$: 'FF' with 3 bits to $(101)_b$ following the CRC bytes For $x=4$: Block replaced by a continuous subcarrier modulation with a duration of $4736 \times 1/f_c$</p>	◀ LT Error in function of 'x'
21	PUT ↷ $R(NAK)_0$ sent between $(FWT+\Delta FWT)$ and $[(FWT+\Delta FWT) + t_{RETRANSMISSION}]$ measured from the end of the last sequence from the PUT	▶ LT Request for Block repetition
22	PUT ↶ $I(0)_0$ ['00 B2 03 04 00' + '90 00']	◀ LT Error recovery
23	PUT ↷ $I(0)_1$ ['00 B2 03 04 00']	▶ LT Loop-back
24	PUT ↶ $I(0)_1$ ["EOT Command" + '90 00']	◀ LT End Of Test command
25	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
26	PUT ↷ '52' (short frame)	▶ LT WUPA to poll for the PICC
27	PUT ↷ '52' (short frame)	▶ LT WUPA to poll for the PICC
28	PUT ↷ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 70: Type A 'Noise' in response to an I-Block not indicating chaining (x=0 to 2 and4)

4.46.Type A ‘Noise’ in response to an I-Block indicating chaining [TA415.x]

Test codification:

TA415.x

Test objective:

To ensure that the PCD behaves correctly when it receives some ‘noise’ (i.e. a frame with a transmission error to be processed as noise by the PCD) in response to an I-Block indicating chaining

References Requirements:

4.7.1.3, 4.9.2.1, 5.2.1.1, 5.2.1.2, 10.3.4.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT replies to an I-Block indicating chaining sent by the PUT with a sequence inducing a ‘noise’ error sent using a delay of ($FDT_{A,PICC,MIN} + 128/f_c$) between the end of the sequence sent by the PUT and the beginning of the ‘noise’ error generated by the LT.

For each transmission error generated, the LT measures the delay between the end of the sequence sent by the PUT after which a transmission error is generated and the beginning of the next sequence sent by the PUT to process the error.

The following ‘noise’ errors are generated successively by the LT:

- x=0: R(ACK) Block with CRC error (the CRC bytes are corrupted and the parity bits of the CRC bytes are adapted in order to have only a CRC error)
- x=1: R(ACK) Block with parity error (a single parity bit is corrupted on any byte)
- x=2: R(ACK) Block with some residual bits (i.e. the total number of bits is not a multiple of 8)
- x=4: Continuous modulation of the PUT carrier with a frequency equal to $f_s = f_c/16$, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of $4736 \times 1/f_c$ (i.e. duration of a 4-bytes frame in Type A)

In this test, the following ATS shall be used:

ATS						(FWT+ΔFWT)
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
‘05’	‘72’	‘80’	‘70’	‘02’	-	573440x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT ignores the ‘noise’ error, notifies a time-out error and continues the transaction upon receipt of a correct block).

For each transmission error generated, the delay between the end of the sequence sent by the PUT after which a ‘noise’ error is generated and the beginning of the next sequence sent by the PUT to process the error is at least (FWT+ΔFWT) and at most [(FWT+ΔFWT) + t_{RETRANSMISSION}].

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ▲ '89 2E C6 66' + '07' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '89 2E C6 66' + '07'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ▲ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ▲ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ▲ I(0)₀ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00']	◀ LT
15	PUT ▶ I(1)₁ ['00 A4 04 00 3B' + '01 02 ... 18']	▶ LT Loop-back
16	PUT ▲ 'Noise' error in function of 'x' sent using a delay of (FDT _{A,PICC,MIN} + 128/f _c) between the end of the sequence sent by the PUT and the beginning of the error For x=0 to 1: R(ACK) ₁ with a transmission error in function of 'x' For x=2: R(ACK) ₁ with 3 bits to (101) _b following the CRC bytes For x=4: Block replaced by a continuous subcarrier modulation with a duration of 4736 x 1/f _c	◀ LT Error in function of 'x'
17	PUT ▶ R(NAK)₁ sent between (FWT+ΔFWT) and [(FWT+ΔFWT) + t _{RETRANSMISSION}] measured from the end of the last sequence from the PUT	▶ LT Request for Block repetition
18	PUT ▲ R(ACK)₁	◀ LT Error recovery
19	PUT ▶ I(1)₀ ['19 1A 1B ... 33 34 35']	▶ LT Loop-back

Step	Exchanges	Comments
20	<p>PUT ↪ 'Noise' error in function of 'x' sent using a delay of ($FDT_{A,PICC,MIN} + 128/f_c$) between the end of the sequence sent by the PUT and the beginning of the error.</p> <p>For $x=0$ to 1: $R(ACK)_0$ with transmission error in function of 'x'</p> <p>For $x=2$: $R(ACK)_0$ with 3 bits to $(101)_b$ following the CRC bytes</p> <p>For $x=4$: Block replaced by a continuous subcarrier modulation with a duration of $4736 \times 1/f_c$</p>	<p>◀ LT</p> <p>Error in function of 'x'</p>
21	PUT ↪ $R(NAK)_0$ sent between $(FWT+\Delta FWT)$ and $[(FWT+\Delta FWT) + t_{RETRANSMISSION}]$ measured from the end of the last sequence from the PUT	▶ LT Request for Block repetition
22	PUT ↪ R(ACK)₀	◀ LT Error recovery
23	PUT ↪ I(0)₁ ['36 37 38 39 3A 3B' + '00']	▶ LT Loop-back
24	PUT ↪ I(0)₁ ['EOT Command' + '90 00']	◀ LT End Of Test command
25	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
26	PUT ↪ '52' (short frame)	▶ LT WUPA to poll for the PICC
27	PUT ↪ '52' (short frame)	▶ LT WUPA to poll for the PICC
28	PUT ↪ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 71: Type A 'Noise' in response to an I-Block indicating chaining (x=0 to 2 and 4)

4.47.Type A ‘Noise’ in response to an R(ACK) Block [TA416.x]

Test codification:

TA416.x

Test objective:

To ensure that the PCD behaves correctly when it receives some ‘noise’ (i.e. a frame with a transmission error to be processed as noise by the PCD) in response to an R(ACK) Block sent to acknowledge a chained I-Block.

References Requirements:

4.7.1.3, 4.9.2.1, 5.2.1.1, 5.2.1.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT replies to an R(ACK)-Block sent by the PUT with a sequence inducing a ‘noise’ error sent using a delay of ($FDT_{A,PICC,MIN} + 128/f_c$) between the end of the sequence sent by the PUT and the beginning of the ‘noise’ error generated by the LT.

The LT measures the delay between the end of the sequence sent by the PUT after which a ‘noise’ error is generated and the beginning of the next sequence sent by the PUT to process the error.

The following ‘noise’ errors are generated successively by the LT:

- x=0: Erroneous block of less than 4 bytes (PCB inducing a protocol error) with CRC error (the CRC bytes are corrupted and the parity bits of the CRC bytes are adapted in order to have only a CRC error)
- x=1: Erroneous block of less than 4 bytes (PCB inducing a protocol error) with parity error (a single parity bit is corrupted on any byte)
- x=2: Erroneous block of less than 4 bytes (PCB inducing a protocol error) with some residual bits (i.e. the total number of bits is not a multiple of 8)
- x=4: Continuous modulation of the PUT carrier with a frequency equal to $f_s = f_c/16$, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of $4736 \times 1/f_c$ (i.e. duration of a 4-bytes frame in Type A)

In this test, the following ATS shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
‘05’	‘78’	‘80’	‘70’	‘02’	-	(FWT+ΔFWT) = 573440 × 1/f _c FSC = 256 bytes

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT ignores the ‘noise’ error, notifies a time-out error and continues the transaction upon receipt of a correct block).

The delay between the end of the sequence sent by the PUT after which a ‘noise’ error is generated and the beginning of the next sequence sent by the PUT to process the error is at least ($\text{FWT} + \Delta\text{FWT}$) and at most [$(\text{FWT} + \Delta\text{FWT}) + t_{\text{RETRANSMISSION}}$].

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ ‘52’ (short frame) ▶ LT	WUPA during polling
2	PUT ▲ ‘01 00’ (no CRC_A) ▲ LT	ATQA
3	PUT ▶ ‘50 00’ ▶ LT	HLTA
4	PUT ▶ ‘05 00 08’ (Type B frame) ▶ LT	WUPB
5	PUT ▶ ‘52’ (short frame) ▶ LT	WUPA
6	PUT ▲ ‘01 00’ (no CRC_A) ▲ LT	ATQA
7	PUT ▶ ‘93 20’ (no CRC_A) ▶ LT	ANTICOLLISION CL1
8	PUT ▲ ‘34 4C 1B E0’ + ‘83’ (no CRC_A) ▲ LT	UID
9	PUT ▶ ‘93 70’ + ‘34 4C 1B E0’ + ‘83’ ▶ LT	SEL1 + UID CL1 + BCC
10	PUT ▲ ‘20’ ▲ LT	SAK
11	PUT ▶ ‘E0 80’ ▶ LT	RATS
12	PUT ▲ ATS ▲ LT	ATS
13	PUT ▶ I(0)₀ [‘00 A4 04 00 0E’ + “2PAY.SYS.DDF01” + ‘00’] ▶ LT	Select PPSE
14	PUT ▲ I(1)₀ [‘00 A4 04 00 20’ + ‘01 02 03 ... 06 07 08’] ▲ LT	
15	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgement R-Block
16	PUT ▲ For x=0 to 1: ‘FF’ with a transmission error in function of ‘x’ For x=2: ‘FF’ with 3 bits to $(101)_b$ following the CRC bytes For x=4: Block replaced by a continuous subcarrier modulation with a duration of $4736 \times 1/f_c$	◀ LT Error in function of ‘x’
17	PUT ▶ R(ACK)₁ sent between $(\text{FWT} + \Delta\text{FWT})$ and $[(\text{FWT} + \Delta\text{FWT}) + t_{\text{RETRANSMISSION}}]$ measured from the end of the last sequence from the PUT ▶ LT	Error notification
18	PUT ▲ I(1)₁ [‘09 0A 0B ... 13 14 15’] ▲ LT	Error recovery

Step	Exchanges	Comments
19	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgement R-Block
20	'Noise' error in function of 'x' sent using a delay of (FDT _{A,PICC,MIN} + 128/f _c) between the end of the sequence sent by the PUT and the beginning of the error PUT ↲ For x=0 to 1: 'FF' with a transmission error in function of 'x' For x=2: 'FF' with 3 bits to (101) _b following the CRC bytes For x=4: Block replaced by a continuous subcarrier modulation with a duration of 4736 x 1/f _c	◀ LT Error in function of 'x'
21	PUT ▶ R(ACK)₀ sent between (FWT+ΔFWT) and [(FWT+ΔFWT) + t _{RETRANSMISSION}] measured from the end of the last sequence from the PUT ▶ LT	Error notification
22	PUT ↲ I(0)₀ ['16 17 18 ... 20' + '00' + '90 00'] ▶ LT	Error recovery
23	PUT ▶ I(0)₁ ['00 A4 04 00 20' + '01 02 03 ... 1E 1F 20' + '00'] ▶ LT	Loop-Back (41 bytes)
24	PUT ↲ I(0)₁ ["EOT Command" + '90 00'] ▶ LT	End Of Test command
25	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) □ LT	PICC Reset
26	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
27	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
28	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC

Scenario 72: Type A 'Noise' in response to an R(ACK) Block (x=0 to 2 and 4)

4.48.Type A Protocol error in response to an R(NAK)-Block sent to notify a transmission error [TA417.xy]

Test codification:

TA417.xy

Test objective:

To ensure that the PCD behaves correctly when it receives a sequence inducing a protocol error in response to an R(NAK)-Block sent to notify a transmission error.

References Requirements:

10.1.5.1, 10.2.1.1, 10.2.2.1, 10.3.4.5, 10.3.4.6, 10.3.5.4, 10.3.5.9

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

xy=07 is Not Applicable if the PCD implements a legacy behavior by accepting I-Blocks with b₆ of PCB set to '1' (see ICS).

Procedure:

Run the following scenario.

The LT measures the delay between the beginning of the sequence inducing a protocol error and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The following protocol errors are generated successively by the LT:

- xy=00: I-Block with bit b₂ of the PCB equal to '0'
- xy=01: I-Block with wrong Block number indicated in the PCB
- xy=02: R(NAK) Block
- xy=03: R(ACK) Block with a Block number different from the one of the last Block sent by the LT
- xy=04: S(DESELECT) response
- xy=05: S(WTX) Request with WTXM = 0
- xy=06: S(WTX) Request with WTXM = 62
- xy=07: I-Block with bit b₆ of the PCB equal to '1' (See "Conditions")
- xy=09: S(WTX) Request with b₆-b₅ of the PCB set to 01_b, with WTXM =1
- xy=10: S(WTX) Request with b₆-b₅ of the PCB set to 10_b, with WTXM =1
- xy=11: I-Block with b₈-b₇ of the PCB set to 01_b

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT initiates a PICC Reset when it detects a protocol error after an R(NAK)-Block sent to notify a transmission error).

The delay between the beginning of the sequence inducing a protocol error and the beginning of the PICC Reset initiated by the PUT is at most $t_{RESETDELAY}$ (i.e. the PUT stops sending the carrier within $t_{RESETDELAY}$).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ '21 4E C3 F6' + '5A' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '21 4E C3 F6' + '5A'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0)0 ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ◀ I(0)0 ['00 B2 05 04 00' + '90 00'] with CRC error	◀ LT Error
15	PUT ▶ R(NAK)0	▶ LT Request for Block repetition

Step	Exchanges	Comments	
16 PUT ↶	<p>Protocol error in function of 'x'</p> <p>For xy=00: I(0)₀ ['00 B2 05 04 00' + '90 00'] with b₂=0 in PCB</p> <p>For xy=01: I(0)₁ ['00 B2 05 04 00' + '90 00']</p> <p>For xy=02: R(NAK)₀</p> <p>For xy=03: R(ACK)₀</p> <p>For xy=04: S(DESELECT) response</p> <p>For xy=05: S(WTX Request) [WTXM='00']</p> <p>For xy=06: S(WTX Request) [WTXM='3E']</p> <p>For xy=07: I(0)₀ ['00 B2 05 04 00' + '90 00'] with b₆=1 in PCB (See "Conditions")</p> <p>For xy=09: S(WTX Request) with b₆-b₅ set to 01_b in PCB, with WTXM =1</p> <p>For xy=10: S(WTX Request) with b₆-b₅ set to 10_b in PCB, with WTXM =1</p> <p>For xy=11: I(0)₀ ['00 B2 05 04 00' + '90 00'] with b₈-b₇ set to 01_b in PCB</p>	◀ LT	Error in function of 'x'
17 PUT II	<p>The PUT performs a PICC Reset (i.e. stops sending the carrier)</p> <p>The PICC Reset is initiated within t_{RESETDELAY}</p>	II LT	PICC Reset

Scenario 73: Type A Protocol error in response to an R(NAK)-Block sent to notify a transmission error (xy=00 to 07 and 09 to 11)

4.49.Type A Removal with an error after WUPA [TA420]

Test codification:

TA420

Test objective:

To ensure that the PCD does not exit the Type A removal procedure on detection of a transmission or a protocol error.

References Requirements:

4.7.1.3, 9.5.1.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

During the removal procedure, the PUT successively generates some errors following the WUPA command (see scenario).

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (upon receipt of a sequence with error during the removal procedure, the PUT sends the HLTA command followed by a new WUPA command; on detection of a time-out during the removal procedure, the PUT repeats the WUPA command up to 2 times and continues to poll for a PICC when it receives an answer following the repetitions).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA

Step	Exchanges	Comments
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ 'BA DC 0F FE' + '97' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + 'BA DC 0F FE' + '97'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0)0 ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ◀ I(0)0 ["EOT Command" + '90 00']	◀ LT End Of Test command
15	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
16	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
17	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
18	PUT ▶ '50 00'	▶ LT HLTA
19	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
20	PUT ◀ '01 00' (no CRC_A) with a parity error (on any byte)	◀ LT ATQA with a parity error
21	PUT ▶ '50 00'	▶ LT HLTA
22	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
23	PUT ◀ 'C3 00' (no CRC_A)	◀ LT ATQA with protocol error
24	PUT ▶ '50 00'	▶ LT HLTA
25	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
26	PUT ◀ I(0)0 ['00 B2 04 04 00' + '90 00']	◀ LT I-Block
27	PUT ▶ '50 00'	▶ LT HLTA
28	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
29	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
30	PUT ◀ '02 0F' (no CRC_A)	◀ LT ATQA not consistent
31	PUT ▶ '50 00'	▶ LT HLTA
32	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
33	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Step	Exchanges	Comments
34	PUT ▶ '52' (<i>short frame</i>)	▶ LT WUPA to poll for the PICC
35	PUT ◀ '01 00' (<i>no CRC_A</i>)	◀ LT ATQA
36	PUT ▶ '50 00'	▶ LT HLTA
37	PUT ▶ '52' (<i>short frame</i>)	▶ LT WUPA to poll for the PICC
38	PUT ▶ '52' (<i>short frame</i>)	▶ LT WUPA to poll for the PICC
39	PUT ▶ '52' (<i>short frame</i>)	▶ LT WUPA to poll for the PICC

Scenario 74: Type A Removal with an error after WUPA

4.50.Type A Consecutive time-outs after S(WTX) Response Blocks [TA421]

Test codification:

TA421

Test objective:

To ensure that the PCD behaves correctly when it detects consecutive time-outs after S(WTX) Response Blocks.

References Requirements:

10.2.2.7, 10.3.5.5, 10.3.5.9

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

In this test, all the Frame Waiting Time Extension Requests are sent with WTXM = 1.

When a time-out error is generated by the LT following 2 consecutive S(WTX) Response Blocks, the LT measures the delay between the end of the second S(WTX) Response sequence and the beginning of the next R(NAK) Block sequence both sent by the PUT.

When three consecutive time-out errors are generated, the LT measures the delay between the end of the third S(WTX) Response sequence and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						(FWT+ΔFWT)
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	114688 x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends an R(NAK) Block when it does not receive any response to a first or a second consecutive S(WTX) Response Block within the extended Frame Waiting Time and initiates a PICC Reset when it does not receive any response to a third consecutive S(WTX) Response Block).

When a time-out error is generated by the LT following 2 consecutive S(WTX) Response Blocks, the delay between the end of the second S(WTX) Response sequence and the beginning of the next R(NAK) Block sequence both sent by the PUT is at most [(FWT+ΔFWT) + t_{RETRANSMISSION}].

When a time-out error is generated by the LT following 3 consecutive S(WTX) Response Blocks, the delay between the end of the third S(WTX) Response sequence and the beginning

of the PICC Reset initiated by the PUT is at most $[(FWT + \Delta FWT) + t_{RESETDELAY}]$ (i.e. the PUT stops sending the carrier within $[(FWT + \Delta FWT) + t_{RESETDELAY}]$).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ 'FA D0 FA D0' + '00' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + 'FA D0 FA D0' + '00'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ◀ I(0)₀ ['00 B2 01 04 00' + '90 00']	◀ LT
15	PUT ▶ I(0)₁ ['00 B2 01 04 00']	▶ LT Loop-back
16	PUT ◀ S(WTX Request) [WTXM = 1]	◀ LT WTX request
17	PUT ▶ S(WTX Response) [WTXM = 1]	▶ LT WTX acknowledgment
18	PUT ▶ R(NAK)₁	▶ LT Time-out error notification
19	PUT ◀ S(WTX Request) [WTXM = 1]	◀ LT WTX request
20	PUT ▶ S(WTX Response) [WTXM = 1]	▶ LT WTX acknowledgment
21	PUT ▶ R(NAK)₁ sent within $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$	▶ LT Time-out error notification
22	PUT ◀ I(0)₁ ['00 B2 02 04 00' + '90 00']	◀ LT Error recovery
23	PUT ▶ I(0)₀ ['00 B2 02 04 00']	▶ LT Loop-back
24	PUT ◀ S(WTX Request) [WTXM = 1]	◀ LT WTX request
25	PUT ▶ S(WTX Response) [WTXM = 1]	▶ LT WTX acknowledgment
26	PUT ▶ R(NAK)₀	▶ LT Time-out error notification
27	PUT ◀ S(WTX Request) [WTXM = 1]	◀ LT WTX request

Step	Exchanges	Comments
28	PUT ▶ S(WTX Response) [WTXM = 1] ▶ LT	WTX acknowledgment
29	PUT ▶ R(NAK)₀ sent within [(FWT+ΔFWT) + t _{RETRANSMISSION}] ▶ LT	Time-out error notification
30	PUT ◀ I(0)₀ ['00 B2 03 04 00' + '90 00'] ◀ LT	Error recovery
31	PUT ▶ I(0)₁ ['00 B2 03 04 00'] ▶ LT	Loop-back
32	PUT ◀ S(WTX Request) [WTXM = 1] ◀ LT	WTX request
33	PUT ▶ S(WTX Response) [WTXM = 1] ▶ LT	WTX acknowledgment
34	PUT ▶ R(NAK)₁ ▶ LT	Time-out error notification
35	PUT ◀ S(WTX Request) [WTXM = 1] ◀ LT	WTX request
36	PUT ▶ S(WTX Response) [WTXM = 1] ▶ LT	WTX acknowledgment
37	PUT ▶ R(NAK)₁ ▶ LT	Time-out error notification
38	PUT ◀ S(WTX Request) [WTXM = 1] ◀ LT	WTX request
39	PUT ▶ S(WTX Response) [WTXM = 1] ▶ LT	WTX acknowledgment
40	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) The PICC Reset is initiated within [(FWT+ΔFWT) + t _{RESETDELAY}]	II LT PICC Reset

Scenario 75: Type A Consecutive time-outs after S(WTX) Response Blocks

4.51.Type A Block protocol with respect of the EMD suppression behavior [TA430.xy]

Test codification:

TA430.xy

Test objective:

To ensure that during the block protocol the PCD correctly ignores all the transmission errors except the frames of at least 4 bytes with no residual bit and with a parity or/and a CRC error and is ready to process a correct sequence no later than $t_{RECOVERY}$ after reception of the last transmission error.

References Requirement:

4.9.2.1

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

Upon receipt of an I-Block sent by the PUT during the Block Protocol (performed at least for 2 blocks with different block numbers), the LT sends a transmission error (but not a frame of at least 4 bytes with no residual bit and with a parity or/and CRC error) using the following Frame Delay Time between the end of the sequence sent by the PUT and the beginning of the transmission error generated by the LT:

- $x=0: FDT_{A,PICC} = FDT_{A,PICC,MIN} - 256/f_c$
- $x=1: FDT_{A,PICC} = FDT_{A,PICC,MIN}$
- $x=2: FDT_{A,PICC} =$
 - $499968 \times 1/f_c + 20/f_c$ if the last bit transmitted by the PUT is $(0)_b$
 - $499968 \times 1/f_c + 84/f_c$ if the last bit transmitted by the PUT is $(1)_b$

Then, the LT sends a correct response sequence to the PUT using the following delay between the end of the transmission error and the beginning of the correct response sequence both sent by the LT:

- $t_{RECOVERY}$ if the transmission error sent by the LT is a continuous modulation with a duration $= n \times 128/f_c$ (i.e. $y=0$ to 2) or if the last bit of the transmission error sent by the LT is $(0)_b$
- $(t_{RECOVERY} + 64/f_c)$ if the last bit of the transmission error sent by the LT is $(1)_b$

Remarks:

- An additional delay of $64/f_c$ is added for the last bit value $(1)_b$ because no event can be observed during the second half of the last bit of the transmission error.
- If the test tool is not able to detect any event during the second half of the last subcarrier cycle of the transmission error, then an additional delay of $8/f_c$ shall be applied for both last bit values.

The following ‘noise’ errors are generated successively by the LT:

- y=0: Continuous modulation of the PUT carrier with a frequency equal to $f_s = f_c/16$, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of $512 \times 1/f_c$
- y=1: Continuous modulation of the PUT carrier with a frequency equal to $f_s = f_c/16$, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of $4736 \times 1/f_c$ (i.e. duration of a 4-bytes frame in Type A)
- y=2: Continuous modulation of the PUT carrier with a frequency equal to $f_s = f_c/16$, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of $64640 \times 1/f_c$ (i.e. duration of a 56-bytes frame in Type A)
- y=3: Erroneous block of less than 4 bytes (PCB inducing a protocol error) with parity error (a single parity bit is corrupted on any byte)
- y=4: Erroneous block of less than 4 bytes (PCB inducing a protocol error) with CRC error (the CRC bytes are corrupted and the parity bits of the CRC bytes are adapted in order to have only a CRC error)
- y=5: Erroneous block of less than 4 bytes (PCB inducing a protocol error) with some residual bits (i.e. the total number of bits is not a multiple of 8)

In this test, the following ATS shall be used:

ATS						FWT+ΔFWT
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
‘05’	‘72’	‘80’	‘70’	‘02’	-	573440x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (after sending a sequence during block protocol, the PUT ignores the transmission error and accepts the next correct sequence sent by the LT).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ 'A0 F9 73 11' + '3B' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + 'A0 F9 73 11' + '3B'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + '2PAY.SYS.DDF01' + '00']	▶ LT Select PPSE
14	<p>'Noise' error in function of 'y' sent using the Frame Delay Time in function of 'x'</p> <p>For y=0: 512 x 1/f_c of continuous subcarrier modulation</p> <p>For y=1: 4736 x 1/f_c of continuous subcarrier modulation</p> <p>For y=2: 64640 x 1/f_c of continuous subcarrier modulation</p> <p>For y=3: 'FF' (erroneous PCB byte) with parity error (on any byte)</p> <p>For y=4: 'FF' (erroneous PCB byte) with CRC error</p> <p>For y=5: 'FF' (erroneous PCB byte) with 3 bits to (101)_b following the CRC bytes</p>	◀ LT Error in function of 'y' sent with a Frame Delay Time in function of 'x'
15	PUT ◀ I(0)₀ ['00 A4 04 00 0C' + '01 02 ... 0C' + '00' + '90 00'] sent using a delay of t _{RECOVERY} or (t _{RECOVERY} + 64/f _c) from the end of the transmission error	◀ LT Correct response sequence sent with recovery delay
16	PUT ▶ I(0)₁ ['00 A4 04 00 0C' + '01 02 ... 0C' + '00']	▶ LT Loop-back
17	<p>'Noise' error in function of 'y' sent using the Frame Delay Time in function of 'x'</p> <p>For y=0: 512 x 1/f_c of continuous subcarrier modulation</p> <p>For y=1: 4736 x 1/f_c of continuous subcarrier modulation</p> <p>For y=2: 64640 x 1/f_c of continuous subcarrier modulation</p> <p>For y=3: 'FF' (erroneous PCB byte) with parity error (on any byte)</p> <p>For y=4: 'FF' (erroneous PCB byte) with CRC error</p> <p>For y=5: 'FF' (erroneous PCB byte) with 3 bits to (101)_b following the CRC bytes</p>	◀ LT Error in function of 'y' sent with a Frame Delay Time in function of 'x'

Step	Exchanges	Comments
18	PUT ↪ I(0)₁ ['00 A4 04 00 0C' + '91 92 ... 9C' + '00' + '90 00'] sent using a delay of tRECOVERY or (tRECOVERY + 64/f_c) from the end of the transmission error ↪ LT	Correct response sequence sent with recovery delay
19	PUT ↗ I(0)₀ ['00 A4 04 00 0C' + '91 92 ... 9C' + '00'] ↗ LT	Loop-back
20	PUT ↪ I(0)₀ ['EOT Command' + '90 00'] ↪ LT	End Of Test command
21	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
22	PUT ↗ '52' (short frame) ↗ LT	WUPA to poll for the PICC
23	PUT ↗ '52' (short frame) ↗ LT	WUPA to poll for the PICC
24	PUT ↗ '52' (short frame) ↗ LT	WUPA to poll for the PICC

**Scenario 76: Type A Block protocol with respect of the EMD suppression behavior
(xy=00 to 05, xy=10 to 15 and xy=20 to 25)**

4.52.Type A Block Protocol with respect of the ‘deaf time’ [TA435.x]

Test codification:

TA435.x

Test objective:

To ensure that after sending a block during the block protocol, the PCD is completely deaf (i.e. ignores any subcarrier generated by the PICC) until $FDT_{A,PICC,MIN} - 128/f_c$.

References Requirement:

4.8.1.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) on reception of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

On reception of an I-Block sent by the PUT during the Block Protocol (performed at least for 2 blocks with different block numbers), the LT sends a sequence with no transmission error (i.e. a correct sequence or a sequence with protocol error) using the Frame Delay Time $FDT_{A,PICC} = FDT_{A,PICC,MIN} - 256/f_c$ between the end of the sequence sent by the PUT and the beginning of the sequence replied by the LT.

The following sequences are successively sent by the LT in response to the relevant I-Blocks:

- x=0: Erroneous block of less than 4 bytes (PCB inducing a protocol error) with correct CRC
- x=1: Erroneous block of less than 4 bytes (PCB inducing a protocol error) with no CRC

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
‘05’	‘72’	‘80’	‘40’	‘02’	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (after sending a sequence during block protocol, the PUT ignores the sequence received during the ‘deaf time’ and processes it as a time-out error i.e. sends an error notification block).

Failure action:

Proceed with next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ '66 D8 E4 C6' + '9C' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '66 D8 E4 C6' + '9C'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + '2PAY.SYS.DDF01' + '00']	▶ LT Select PPSE
14	PUT ◀ Sequence in function of 'x' sent using the Frame Delay Time FDT _{A,PICC} = (FDT _{A,PICC,MIN} - 256/f _c) For x=0: 'FF' (erroneous PCB byte) with correct CRC For x=1: 'FF' (erroneous PCB byte) with no CRC	◀ LT Sequence in function of 'x' sent using the Frame Delay Time FDT _{A,PICC,MIN} - 256/f _c
15	PUT ▶ R(NAK)₀	▶ LT Time-out error notification
16	PUT ◀ I(0)₀ ['00 A4 04 00 0C' + '01 02 ... 0C' + '00' + '90 00']	◀ LT Error recovery
17	PUT ▶ I(0)₁ ['00 A4 04 00 0C' + '01 02 ... 0C' + '00']	▶ LT Loop-back
18	PUT ◀ Sequence in function of 'x' sent using the Frame Delay Time FDT _{A,PICC} = (FDT _{A,PICC,MIN} - 256/f _c) For x=0: 'FF' (erroneous PCB byte) with correct CRC For x=1: 'FF' (erroneous PCB byte) with no CRC	◀ LT Sequence in function of 'x' sent using the Frame Delay Time FDT _{A,PICC,MIN} - 256/f _c
19	PUT ▶ R(NAK)₁	▶ LT Time-out error notification
20	PUT ◀ I(0)₁ ['00 A4 04 00 0C' + '91 92 ... 9C' + '00' + '90 00']	◀ LT Error recovery
21	PUT ▶ I(0)₀ ['00 A4 04 00 0C' + '91 92 ... 9C' + '00']	▶ LT Loop-back
22	PUT ◀ I(0)₀ ['EOT Command' + '90 00']	◀ LT End Of Test command
23	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset

Step	Exchanges	Comments
24	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
25	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC
26	PUT ▶ '52' (short frame)	▶ LT WUPA to poll for the PICC

Scenario 77: Type A Block Protocol with respect of the 'deaf time' (x=0 and 1)

4.53. Type A Parity error in the first 4 bytes of a sequence in response to an I-Block not indicating chaining [TA440]

Test codification:

TA440

Test objective:

To ensure that the PCD behaves correctly when it receives a sequence with a parity error in the first 4 bytes in response to an I-Block not indicating chaining.

References Requirements:

4.7.1.3, 4.9.2.1, 10.3.5.3, 10.3.5.9

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

When a single parity error is generated, the LT measures the delay between the end of the last command sent by the PUT and the beginning of the next sequence sent by the PUT to process the parity error.

When a single parity error is generated, the LT measures the delay between the end of the sequence with parity error and the beginning of the sequence replied by the PUT to process the error.

When two consecutive parity errors are generated, the LT measures the delay between the end of the last command sent by the PUT and the beginning of the sequence replied by the PUT to process the error.

When two consecutive parity errors are generated, the LT measures the delay between the end of the sequence with parity error and the beginning of the sequence replied by the PUT to process the error.

When three consecutive parity errors are generated, the LT measures the delay between the end of the last command sent by the PUT and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

The following transmission errors are generated by the LT:

- I-Block (in a frame of at least 4 bytes) with parity error (corrupted parity bit) on the following bytes: the 2nd byte of the frame for the 1st, 3rd, 5th, 7th, 8th and 9th errors generated, 3rd byte of the frame for the 2nd, 4th and 6th errors generated

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends an R(NAK) Block when it detects a first or a second consecutive parity error or time-out after an I-Block not indicating chaining and initiates a PICC Reset when it detects a third consecutive parity or time-out error).

When a single parity error is generated, the delay between the end of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at least $FDT_{A,PCD,MIN}$.

When a single parity error is generated, the delay between the end of the last command sent by the PUT and the beginning of the sequence sent by the PUT to process the error is at most $(FWT+\Delta FWT) + t_{RETRANSMISSION}$.

When two consecutive parity errors are generated, the delay between the end of the second sequence with parity error and the beginning of the sequence replied by the PUT to process the error is at least $FDT_{A,PCD,MIN}$.

When two consecutive parity errors are generated, the delay between the end of the last command sent by the PUT and the beginning of the sequence sent by the PUT to process the parity error is at most $(FWT+\Delta FWT) + t_{RETRANSMISSION}$.

When three consecutive parity errors are generated, the delay between the end of the last command sent by the PUT and the beginning of the PICC Reset initiated by the PUT is at most $(FWT+\Delta FWT) + t_{RESETDELAY}$ (i.e. the PUT stops sending the carrier within $t_{RESETDELAY}$).

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ 'D7 EE 3B 98' + '9A' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + 'D7 EE 3B 98' + '9A'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE

Step	Exchanges	Comments
14	PUT \leftarrow I(0) ₀ ['00 B2 01 04 00' + '90 00'] \leftarrow LT	
15	PUT \rightarrow I(0) ₁ ['00 B2 01 04 00'] \rightarrow LT	Loop-back
16	PUT \leftarrow I(0) ₁ ['00 B2 02 04 00' + '90 00'] with a parity error on the 2 nd byte of the frame \leftarrow LT	Erroneous I-Block
17	PUT \rightarrow R(NAK) ₁ sent after FDT _{A,PCD,MIN} after the last LT response and before [(FWT+ΔFWT) + t _{RETRANSMISSION}] since the last PUT command \rightarrow LT	Request for Block repetition
18	PUT \leftarrow I(0) ₁ ['00 B2 02 04 00' + '90 00'] \leftarrow LT	Error recovery
19	PUT \rightarrow I(0) ₀ ['00 B2 02 04 00'] \rightarrow LT	Loop-back
20	PUT \leftarrow I(0) ₀ ['00 B2 03 04 00' + '90 00'] with a parity error on the 3 rd byte of the frame \leftarrow LT	Erroneous I-Block
21	PUT \rightarrow R(NAK) ₀ sent after FDT _{A,PCD,MIN} after the last LT response and before [(FWT+ΔFWT) + t _{RETRANSMISSION}] since the last PUT command \rightarrow LT	Request for Block repetition
22	PUT \leftarrow I(0) ₀ ['00 B2 03 04 00' + '90 00'] \leftarrow LT	Error recovery
23	PUT \rightarrow I(0) ₁ ['00 B2 03 04 00'] \rightarrow LT	Loop-back
24	PUT \leftarrow I(0) ₁ ['00 B2 04 04 00' + '90 00'] with a parity error on the 2 nd byte of the frame \leftarrow LT	Erroneous I-Block
25	PUT \rightarrow R(NAK) ₁ \rightarrow LT	Request for Block repetition
26	PUT \leftarrow I(0) ₁ ['00 B2 04 04 00' + '90 00'] with a parity error on the 3 rd byte of the frame \leftarrow LT	Erroneous I-Block
27	PUT \rightarrow R(NAK) ₁ sent after FDT _{A,PCD,MIN} after the last LT response and before [(FWT+ΔFWT) + t _{RETRANSMISSION}] since the last PUT command \rightarrow LT	Request for Block repetition
28	PUT \leftarrow I(0) ₁ ['00 B2 04 04 00' + '90 00'] \leftarrow LT	Error recovery
29	PUT \rightarrow I(0) ₀ ['00 B2 04 04 00'] \rightarrow LT	Loop-back
30	PUT \leftarrow I(0) ₀ ['00 B2 05 04 00' + '90 00'] with a parity error on the 2 nd byte of the frame \leftarrow LT	Erroneous I-Block
31	PUT \rightarrow R(NAK) ₀ \rightarrow LT	Request for Block repetition
32	PUT \leftarrow I(0) ₀ ['00 B2 05 04 00' + '90 00'] with a parity error on the 3 rd byte of the frame \leftarrow LT	Erroneous I-Block
33	PUT \rightarrow R(NAK) ₀ sent after FDT _{A,PCD,MIN} after the last LT response and before [(FWT+ΔFWT) + t _{RETRANSMISSION}] since the last PUT command \rightarrow LT	Request for Block repetition
34	PUT \leftarrow I(0) ₀ ['00 B2 05 04 00' + '90 00'] \leftarrow LT	Error recovery
35	PUT \rightarrow I(0) ₁ ['00 B2 05 04 00'] \rightarrow LT	Loop-back
36	PUT \leftarrow I(0) ₁ ['00 B2 06 04 00' + '90 00'] with a parity error on the 2 nd byte of the frame \leftarrow LT	Erroneous I-Block

Step	Exchanges	Comments
37	PUT ▶ R(NAK)₁ ▶ LT	Request for Block repetition
38	PUT ↵ I(0)₁ ['00 B2 06 04 00' + '90 00'] with a parity error on the 2 nd byte of the frame ↵ LT	Erroneous I-Block
39	PUT ▶ R(NAK)₁ ▶ LT	Request for Block repetition
40	PUT ↵ I(0)₁ ['00 B2 06 04 00' + '90 00'] with a parity error on the 2 nd byte of the frame ↵ LT	Erroneous I-Block
41	<p>The PUT performs a PICC Reset (i.e. stops sending the carrier)</p> <p>PUT II The PICC Reset is initiated within $(FWT + \Delta FWT) + t_{RESETDELAY}$ since the last PUT command</p> <p>The PUT keeps the carrier off during at least $t_{RESET,MIN}$</p>	PICC Reset

Scenario 78: Type A Parity error in the first 4 bytes of a sequence in response to an I-Block not indicating chaining)

4.54. Type A Parity error in the first 4 bytes of a sequence in response to an I-Block indicating chaining [TA441]

Test codification:

TA441

Test objective:

To ensure that the PCD behaves correctly when it receives a sequence with a parity error in the first 4 bytes in response to an I-Block indicating chaining.

References Requirements:

4.7.1.3, 4.9.2.1, 10.3.5.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

When a single parity error is generated, the LT measures the delay between the end of the last command sent by the PUT and the beginning of the sequence replied by the PUT to process the error.

When a single parity error is generated, the LT measures the delay between the end of the sequence with parity error and the beginning of the sequence replied by the PUT to process the error.

When three consecutive parity errors are generated, the LT measures the delay between the end of the last command sent by the PUT and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

The following transmission errors are generated successively by the LT:

- S(WTX Request) Block with parity error (corrupted parity bit) on the following bytes: the 2nd byte of the frame for the 1st, 3rd, 4th and 5th errors generated, 3rd byte of the frame for the 2nd error generated

In this test, the default ATS (with default values for all parameters) shall be used:

ATS						Comments
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends an R(NAK) Block when it detects a parity or time-out error after an I-Block indicating chaining and continues the transaction upon receipt of a correct block).

When a single parity error is generated, the delay between the end of the sequence with parity error and the beginning of the sequence replied by the PUT to process the error is at least $FDT_{A,PCD,MIN}$.

When a single parity error is generated, the delay between the end of the last command sent by the PUT and the beginning of the sequence sent by the PUT to process the error is at most $(FWT+\Delta FWT) + t_{RETRANSMISSION}$.

When three consecutive parity errors are generated, the delay between the end of the last command sent by the PUT and the beginning of the PICC Reset initiated by the PUT is at most $(FWT+\Delta FWT) + t_{RESETDELAY}$ (i.e. the PUT stops sending the carrier within $t_{RESETDELAY}$).

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ▲ 'EE 0A 3B D7' + '08' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + 'EE 0A 3B D7' + '08'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ▲ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ▲ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ▲ I(0)₀ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00']	◀ LT
15	PUT ▶ I(1)₁ ['00 A4 04 00 3B' + '01 02 ... 18']	▶ LT Loop-back
16	PUT ▲ S(WTX Request) [WTXM='01'] with a parity error on the 2nd byte of the frame	◀ LT Erroneous I-Block
17	PUT ▶ R(NAK)₁ sent after $FDT_{A,PCD,MIN}$ after the last LT response and before $[(FWT+\Delta FWT) + t_{RETRANSMISSION}]$ since the last PUT command	▶ LT Request for Block repetition
18	PUT ▲ R(ACK)₁	◀ LT Error recovery
19	PUT ▶ I(1)₀ ['19 1A 1B ... 33 34 35']	▶ LT Loop-back

Step	Exchanges	Comments
20	PUT ↪ S(WTX Request) [WTXM='01'] with a parity error on the 3rd byte of the frame ↪ LT	Erroneous I-Block
21	PUT ↪ R(NAK)₀ sent after FDT _{A,PCD,MIN} after the last LT response and before [(FWT+ΔFWT) + t _{RETRANSMISSION}] since the last PUT command ↪ LT	Request for Block repetition
22	PUT ↪ R(ACK)₀ ↪ LT	Error recovery
23	PUT ↪ I(0)₁ ['36 37 38 39 3A 3B' + '00'] ↪ LT	Last I-Block of the chain
24	PUT ↪ I(0)₁ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00'] ↪ LT	
25	PUT ↪ I(1)₀ ['00 A4 04 00 3B' + '01 02 ... 18'] ↪ LT	Loop-back
26	PUT ↪ S(WTX Request) [WTXM='01'] with a parity error on the 2nd byte of the frame ↪ LT	Erroneous I-Block
27	PUT ↪ R(NAK)₀ ↪ LT	Request for Block repetition
28	PUT ↪ S(WTX Request) [WTXM='01'] with a parity error on the 2nd byte of the frame ↪ LT	Erroneous I-Block
29	PUT ↪ R(NAK)₀ ↪ LT	Request for Block repetition
30	PUT ↪ S(WTX Request) [WTXM='01'] with a parity error on the 2nd byte of the frame ↪ LT	Erroneous I-Block
31	The PUT performs a PICC Reset (i.e. stops sending the carrier) PUT II The PICC Reset is initiated within (FWT+ΔFWT) + t _{RESETDELAY} since the last PUT command The PUT keeps the carrier off during at least t _{RESET,MIN}	II LT PICC Reset

Scenario 79: Type A Parity error in the first 4 bytes of a sequence in response to an I-Block indicating chaining

4.55.Type A Parity error in the first 4 bytes of a sequence in response to an R(ACK) Block [TA442]

Test codification:

TA442

Test objective:

To ensure that the PCD behaves correctly when it receives a sequence with parity error in the first 4 bytes in response to an R(ACK) Block sent to acknowledge a chained I-Block.

References Requirements:

4.7.1.3, 4.9.2.1, 10.3.5.6, 10.3.5.9

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

When a single parity error is generated, the LT measures the delay between the end of the last command sent by the PUT and the beginning of the sequence replied by the PUT to process the error.

When a single parity error is generated, the LT measures the delay between the end of the sequence with parity error and the beginning of the sequence replied by the PUT to process the error.

When two consecutive parity errors are generated, the LT measures the delay between the end of the last command sent by the PUT and the beginning of the sequence replied by the PUT to process the error.

When two consecutive parity errors are generated, the LT measures the delay between the end of the sequence with parity error and the beginning of the sequence replied by the PUT to process the error.

When three consecutive parity errors are generated, the LT measures the delay between the end of the last command sent by the PUT and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

The following transmission errors are generated by the LT:

- I-Block (in a frame of at least 4 bytes) with parity error (corrupted parity bit) on the following bytes: the 2nd byte of the frame for the 1st, 3rd, 5th, 7th, 8th and 9th errors generated, 3rd byte of the frame for the 2nd, 4th and 6th errors generated

In this test, the following ATS shall be used:

ATS						Maximum Frame Size for the PICC (FSC)
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'78'	'80'	'40'	'02'	-	256 bytes

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT retransmits the R(ACK) Block up to two times when it detects a parity or time-out error and initiates a PICC Reset when it detects a third consecutive parity or time-out error).

When a single parity error is generated, the delay between the end of the sequence with parity error and the beginning of the sequence replied by the PUT to process the error is at least $FDT_{A,PCD,MIN}$.

When a single parity error is generated, the delay between the end of the last command sent by the PUT and the beginning of the sequence sent by the PUT to process the error is at most $(FWT+\Delta FWT) + t_{RETRANSMISSION}$.

When two consecutive parity errors are generated, the delay between the end of the second sequence with parity error and the beginning of the sequence replied by the PUT to process the error is at least $FDT_{A,PCD,MIN}$.

When two consecutive parity errors are generated, the delay between the end of the last command sent by the PUT and the beginning of the sequence sent by the PUT to process the error is at most $(FWT+\Delta FWT) + t_{RETRANSMISSION}$.

When three consecutive parity errors are generated, the delay between the end of the last command sent by the PUT and the beginning of the PICC Reset initiated by the PUT is at most $(FWT+\Delta FWT) + t_{RESETDELAY}$ (i.e. the PUT stops sending the carrier within $t_{RESETDELAY}$).

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ▲ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ▲ '44 3B EC 10' + '83' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + '44 3B EC 10' + '83'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ▲ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ▲ ATS	◀ LT ATS
13	PUT ▶ I(0)0 ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE

Step	Exchanges	Comments
14	PUT \leftarrow I(1) ₀ ['00 A4 04 00 50' + '01 02 03 ... 06 07 08'] \leftarrow LT	
15	PUT \rightarrow R(ACK) ₁ \rightarrow LT	Acknowledgement R-Block
16	PUT \leftarrow I(1) ₁ ['09 0A 0B ... 13 14 15'] with a parity error on the 2 nd byte of the frame \leftarrow LT	Erroneous I-Block
17	PUT \rightarrow R(ACK) ₁ sent after FDT _{A,PCD,MIN} after the last LT response and before [(FWT+ΔFWT) + t _{RETRANSMISSION}] since the last PUT command \rightarrow LT	Error notification
18	PUT \leftarrow I(1) ₁ ['09 0A 0B ... 13 14 15'] \leftarrow LT	Error recovery
19	PUT \rightarrow R(ACK) ₀ \rightarrow LT	Acknowledgement R-Block
20	PUT \leftarrow I(1) ₀ ['16 17 18 ... 20 21 22'] with a parity error on the 3 rd byte of the frame \leftarrow LT	Erroneous I-Block
21	PUT \rightarrow R(ACK) ₀ sent after FDT _{A,PCD,MIN} after the last LT response and before [(FWT+ΔFWT) + t _{RETRANSMISSION}] since the last PUT command \rightarrow LT	Error notification
22	PUT \leftarrow I(1) ₀ ['16 17 18 ... 20 21 22'] \leftarrow LT	Error recovery
23	PUT \rightarrow R(ACK) ₁ \rightarrow LT	Acknowledgement R-Block
24	PUT \leftarrow I(1) ₁ ['23 24 25 ... 2D 2E 2F'] with a parity error on the 2 nd byte of the frame \leftarrow LT	Erroneous I-Block
25	PUT \rightarrow R(ACK) ₁ \rightarrow LT	Error notification
26	PUT \leftarrow I(1) ₁ ['23 24 25 ... 2D 2E 2F'] with a parity error on the 3 rd byte of the frame \leftarrow LT	Erroneous I-Block
27	PUT \rightarrow R(ACK) ₁ sent after FDT _{A,PCD,MIN} after the last LT response and before [(FWT+ΔFWT) + t _{RETRANSMISSION}] since the last PUT command \rightarrow LT	Error notification
28	PUT \leftarrow I(1) ₁ ['23 24 25 ... 2D 2E 2F'] \leftarrow LT	Error recovery
29	PUT \rightarrow R(ACK) ₀ \rightarrow LT	Acknowledgement R-Block
30	PUT \leftarrow I(1) ₀ ['30 31 32 ... 3A 3B 3C'] with a parity error on the 2 nd byte of the frame \leftarrow LT	Erroneous I-Block
31	PUT \rightarrow R(ACK) ₀ \rightarrow LT	Error notification
32	PUT \leftarrow I(1) ₀ ['30 31 32 ... 3A 3B 3C'] with a parity error on the 3 rd byte of the frame \leftarrow LT	Erroneous I-Block
33	PUT \rightarrow R(ACK) ₀ sent after FDT _{A,PCD,MIN} after the last LT response and before [(FWT+ΔFWT) + t _{RETRANSMISSION}] since the last PUT command \rightarrow LT	Error notification
34	PUT \leftarrow I(1) ₀ ['30 31 32 ... 3A 3B 3C'] \leftarrow LT	Error recovery
35	PUT \rightarrow R(ACK) ₁ \rightarrow LT	Acknowledgement R-Block

Step	Exchanges	Comments
36	PUT ↪ I(1)₁ ['3D 3E 3F ... 47 48 49'] with a parity error on the 2 nd byte of the frame ↪ LT	Erroneous I-Block
37	PUT ↶ R(ACK)₁ ↪ LT	Error notification
38	PUT ↪ I(1)₁ ['3D 3E 3F ... 47 48 49'] with a parity error on the 2 nd byte of the frame ↪ LT	Erroneous I-Block
39	PUT ↶ R(ACK)₁ ↪ LT	Error notification
40	PUT ↪ I(1)₁ ['3D 3E 3F ... 47 48 49'] with a parity error on the 2 nd byte of the frame ↪ LT	Erroneous I-Block
41	The PUT performs a PICC Reset (i.e. stops sending the carrier) PUT II The PICC Reset is initiated within $(FWT + \Delta FWT) + t_{RESETDELAY}$ since the last PUT command The PUT keeps the carrier off during at least $t_{RESET,MIN}$	PIICC Reset

Scenario 80: Type A Parity error in the first 4 bytes of a sequence in response to an R(ACK) Block

4.56.Type A Parity error in the first 4 bytes of a sequence in response to an S(WTX) Response Block [TA443]

Test codification:

TA443

Test objective:

To ensure that the PCD behaves correctly when it receives a sequence with parity error in the first 4 bytes following a S(WTX) Response Block.

References Requirements:

4.9.2.1, 10.2.2.7, 10.3.5.5

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

When a parity error is generated, the LT measures the delay between the end of the last command sent by the PUT and the beginning of the next sequence sent by the PUT to process the parity error.

When a parity error is generated, the LT measures the delay between the end of the sequence with parity error and the beginning of the sequence replied by the PUT to process the error.

The following transmission errors are generated by the LT:

- I-Block (in a frame of at least 4 bytes) with parity error (corrupted parity bit) on the following bytes: the 2nd byte of the frame for the 1st and 3rd errors generated, 3rd byte of the frame for the 2nd error generated

In this test, the following ATS shall be used:

ATS						(FWT+ΔFWT)
TL	T0	TA(1)	TB(1)	TC(1)	T1...TK	
'05'	'72'	'80'	'40'	'02'	-	114688x 1/f _c (default value)

The corresponding extended Frame Waiting Time is as follows:

- $FWT_{EXT} + \Delta FWT = (FWT \times WTXM) + \Delta FWT$ with $FWT \times WTXM \leq FWT_{MAX}$

And we define:

- $FWT_{EXT1} + \Delta FWT$ corresponding to $WTXM_1$
- $FWT_{EXT2} + \Delta FWT$ corresponding to $WTXM_2$
- $FWT_{EXT3} + \Delta FWT$ corresponding to $WTXM_3$

Which leads to:

WTXM ₁	FWT _{EXT1+ΔFWT}	WTXM ₂	FWT _{EXT2+ΔFWT}	WTXM ₃	FWT _{EXT3+ΔFWT}
47	3129344 x 1/f _c	45	2998272 x 1/f _c	42	2801664 x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends an R(NAK) Block to ask for retransmission when it detects a parity or time-out error after an S(WTX) Response).

At step 19 of the following scenario, the delay between the end of the sequence with parity error and the beginning of the sequence replied by the PUT to process the error is at least FDT_{A,PCD,MIN}. The delay between the end of the last command sent by the PUT and the beginning of the next sequence sent by the PUT to process the error is at most [FWT_{EXT1+ΔFWT} + t_{RETRANSMISSION}].

At step 25 of the following scenario, the delay between the end of the sequence with parity error and the beginning of the sequence replied by the PUT to process the error is at least FDT_{A,PCD,MIN}. The delay between the end of the last command sent by the PUT and the beginning of the next sequence sent by the PUT to process the error is at most [FWT_{EXT2+ΔFWT} + t_{RETRANSMISSION}].

At step 31 of the following scenario, the delay between the end of the sequence with parity error and the beginning of the sequence replied by the PUT to process the error is at least FDT_{A,PCD,MIN}. The delay between the end of the last command sent by the PUT and the beginning of the next sequence sent by the PUT to process the error is at most [FWT_{EXT3+ΔFWT} + t_{RETRANSMISSION}].

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '52' (short frame)	▶ LT WUPA during polling
2	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
3	PUT ▶ '50 00'	▶ LT HLTA
4	PUT ▶ '05 00 08' (Type B frame)	▶ LT WUPB
5	PUT ▶ '52' (short frame)	▶ LT WUPA
6	PUT ◀ '01 00' (no CRC_A)	◀ LT ATQA
7	PUT ▶ '93 20' (no CRC_A)	▶ LT ANTICOLLISION CL1
8	PUT ◀ 'FB 29 EF 53' + '6E' (no CRC_A)	◀ LT UID
9	PUT ▶ '93 70' + 'FB 29 EF 53' + '6E'	▶ LT SEL1 + UID CL1 + BCC
10	PUT ◀ '20'	◀ LT SAK
11	PUT ▶ 'E0 80'	▶ LT RATS
12	PUT ◀ ATS	◀ LT ATS
13	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
14	PUT ◀ I(0)₀ ['00 B2 01 04 00' + '90 00']	◀ LT
15	PUT ▶ I(0)₁ ['00 B2 01 04 00']	▶ LT Loop-back
16	PUT ◀ S(WTX Request) [WTXM₁] with WTXM₁	◀ LT WTXM ₁
17	PUT ▶ S(WTX Response) [WTXM₁]	▶ LT WTX acknowledgment
18	PUT ◀ I(0)₁ ['00 A4 04 00 05+ 'C1 C2 ... C5' + '00' + '90 00'] with a parity error on the 2nd byte of the frame	◀ LT Erroneous I-Block
19	PUT ▶ R(NAK)₁ sent after FDT_{A,PCD,MIN} after the last LT response and before [(FWT_{EXT1}+ΔFWT) + t_{RETRANSMISSION}] since the last PUT command	▶ LT Parity error notification
20	PUT ◀ I(0)₁ ['00 A4 04 00 05+ 'C1 C2 ... C5' + '00' + '90 00']	◀ LT Error recovery
21	PUT ▶ I(0)₀ ['00 A4 04 00 05+ 'C1 C2 ... C5' + '00']	▶ LT Loop-back
22	PUT ◀ S(WTX Request) [WTXM₂] with WTXM₂	◀ LT WTXM ₂
23	PUT ▶ S(WTX Response) [WTXM₂]	▶ LT WTX acknowledgment
24	PUT ◀ I(0)₀ ['00 A4 04 00 05+ 'C6 C7 ... CA' + '00' + '90 00'] with a parity error on the 3rd byte of the frame	◀ LT Erroneous I-Block
25	PUT ▶ R(NAK)₀ sent after FDT_{A,PCD,MIN} after the last LT response and before [(FWT_{EXT2}+ΔFWT) + t_{RETRANSMISSION}] since the last PUT command	▶ LT Parity error notification
26	PUT ◀ I(0)₀ ['00 A4 04 00 05+ 'C6 C7 ... CA' + '00' + '90 00']	◀ LT Error recovery
27	PUT ▶ I(0)₁ ['00 A4 04 00 05+ 'C6 C7 ... CA' + '00']	▶ LT Loop-back
28	PUT ◀ S(WTX Request) [WTXM₃] with WTXM₃	◀ LT WTXM ₃

Step	Exchanges	Comments
29	PUT ▶ S(WTX Response) [WTXM₃] ▶ LT	WTX acknowledgment
30	PUT ↲ I(0)₁ ['00 A4 04 00 05+ 'CB CC ... CF' + '00' + '90 00'] with a parity error on the 2 nd byte of the frame ↲ LT	Erroneous I-Block
31	PUT ▶ R(NAK)₁ sent after FDT _{A,PCD,MIN} after the last LT response and before [(FWTEXT ₃ +ΔFWT) + t _{RETRANSMISSION}] since the last PUT command ▶ LT	Parity error notification
32	PUT ↲ I(0)₁ ['00 A4 04 00 05+ 'CB CC ... CF' + '00' + '90 00'] ↲ LT	Error recovery
33	PUT ▶ I(0)₀ ['00 A4 04 00 05+ 'CB CC ... CF' + '00'] ▶ LT	Loop-back
34	PUT ↲ I(0)₀ ['EOT Command' + '90 00'] ↲ LT	End Of Test command
35	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
36	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
37	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC
38	PUT ▶ '52' (short frame) ▶ LT	WUPA to poll for the PICC

Scenario 81: Type A Parity error in the first 4 bytes of a sequence after an S(WTX) Response Block

5. Type B TEST CASES

5.1. Type B Pre-test to determine TR1_{PUTMIN} [TB000]

Test codification:

TB000

Test objective:

To determine TR1_{PUTMIN}, the minimum value of TR1 supported by the PCD (to initialize the tests TB340.x and TB435.x).

References Requirement:

4.3.2.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario 5 consecutive times to determine 5 times the value of TR1_{PUTMIN}.

(A): a correct I-Block preceded by the synchronization time $TR1 = TR1_{MIN} - 128/f_c$ (with subcarrier on but no modulation) is sent as an answer to the first I-Block sent by the PUT (using the delay $TR0 = 1920/f_c$ between the end of the sequence sent by the PUT and the beginning of the synchronization time preceding the sequence replied by the LT). And:

- If the PUT correctly replies to the I-Block with $TR1 = (TR1_{MIN} - 128/f_c)$ with a new I-Block, then the test continues with the procedure **(B)** described below using $i=2$
- Or else, if the PUT replies to the I-Block with $TR1 = (TR1_{MIN} - 128/f_c)$ with an R(NAK)-Block, then the tool parameter TR1_{PUTMIN} is set to the value $TR1_{PUTMIN} = TR1_{MIN}$ and the test is ended

(B): a correct I-Block preceded by the synchronization time $TR1 = TR1_{MIN} - i \times 128/f_c$ (with subcarrier on but no modulation) is sent as an answer to new I-Block sent by the PUT (using the delay $TR0 = 1920/f_c$ between the end of the sequence sent by the PUT and the beginning of the synchronization time preceding the sequence replied by the LT). And:

- If the PUT correctly replies to the I-Block with $TR1 = (TR1_{MIN} - i \times 128/f_c)$ with a new I-Block, then the test continues with the present procedure **(B)** using $i=i+1$
- Or else, if the PUT replies to the I-Block with $TR1 = (TR1_{MIN} - i \times 128/f_c)$ with an R(NAK)-Block, then the tool parameter TR1_{PUTMIN} is set to the value $TR1_{PUTMIN} = (TR1_{MIN} - i \times 128/f_c + 128/f_c)$ and the test is ended

The value of TR1_{PUTMIN} obtained at the end of the test is stored to initialize the tests TB340.x and TB435.x.

In this test, the default Protocol Information (PI) shall be used:

PI			Comments
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	Default value

Acceptance criteria:

The 5 value of TR1_{PUTMIN} are determined as defined in the following scenario and are equal.

Failure action:

Perform the remaining tests except TB340.x and TB435.x.

The verdicts for TB000, TB340 and TB435 are set to INCONCLUSIVE.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ▲ '50' + 'CB 23 8E 36' + '00 00 00 00' + PI ▲ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ▲ '50' + 'CB 23 8E 36' + '00 00 00 00' + PI ▲ LT	ATQB
6	PUT ▶ '1D' + 'CB 23 8E 36' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ▲ '00' ▲ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
(A.1)	PUT ▲ I(0)₀ ['00 B2 01 04 00' + '90 00'] preceded by TR1 = (TR1_{MIN} - 128/f_c) with subcarrier on but no modulation ▲ LT	
(A.2)	I(0)₁ ['00 B2 01 04 00'] Then, the test continues at step (B.1) using i=2 OR R(NAK)₀ Then TR1 _{PUTMIN} = TR1 _{MIN} and the test is ended ▶ LT	Loop-back or error notification
(B.1)	PUT ▲ I(0)_j ['00 B2 01 04 00' + '90 00'] with j=[(i+1) mod 2] and preceded by TR1 = (TR1_{MIN} - i x 128/f_c) with subcarrier on but no modulation ▲ LT	
(B.2)	I(0)_k ['00 B2 01 04 00'] with k=[i mod 2] Then the test continues at step (B.1) using i=i+1 OR R(NAK)_j with j=[(i+1) mod 2] Then TR1 _{PUTMIN} = (TR1 _{MIN} - i x 128/f _c + 128/f _c) and the test is ended ▶ LT	Loop-back or error notification

The parameter 'i' can take a value up to 9 (for TR1_{PUTMIN} = 128/f_c)

Scenario 82: Type B Pre-test to determine TR1_{PUTMIN}

5.2. Basic Type B Exchange and timings measurement [TB001]

Test codification:

TB001

Test objective:

To ensure that the PCD respects the frame format, the timings and the series of commands during a basic exchange (installation and block protocol) with a Type B PICC.

References Requirements:

4.2.1.1, 4.3.2.1, 4.5.1.1, 4.7.2.1, 4.7.3.3, 4.8.2.1, 6.2.1.1, 6.2.1.2, 6.3.1.1, 6.3.1.2, 6.3.1.3, 6.3.2.4, 6.3.2.8, 6.4.1.1, 6.4.1.3, 6.4.1.4, 6.4.1.5, 6.4.1.6, 6.4.1.9, 6.4.1.10, 6.4.1.12, 6.4.2.4, 9.1.2.1, 9.1.2.3, 9.2.1.2, 9.2.1.3, 9.2.1.4, 9.3.1.1, 9.3.1.2, 9.3.3.1, 9.4.2.1, 9.4.2.2, 10.3.1.1, 10.3.1.3, 10.3.3.1, 10.3.3.3, 10.3.4.1, 4.6.2.1

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

Until the End Of Test command, when a sequence sent by the LT is followed by a sequence sent by the PUT, the LT measures the delay between the end of the sequence sent by the LT and the beginning of the sequence replied by the PUT.

Remark: the end of an EMV Contactless PICC sequence is defined as the “start of the EoS transmitted by the PICC”.

Until the End Of Test command, when two consecutive sequences are sent by the PUT, the LT measures the delay between the end of the first sequence sent by the PUT and the beginning of the second sequence sent by the PUT.

Until the End Of Test command, the LT measures the delay between two consecutive characters sent within the sequences sent by the PUT.

Until the End Of Test command, the LT observes the format and coding of the sequences transmitted by the PUT (Start of Sequence and End of Sequence included).

In this test, the default Protocol Information (PI) shall be used:

PI			Comments
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to all the sequences sent by the LT).

The PUT uses the default bit rate of $f_c/128$ during installation (~ 106 kbit/s as $f_c = 13,56$ MHz).

The PUT continues the EMV Contactless session using the default bit rate.

The PUT uses the Type A short frame format to transmit the WUPA command and the Type B frame format to transmit all other commands and blocks.

The PUT sends commands (except WUPA) and blocks in sequences ending with two CRC_B bytes calculated as defined in ISO/IEC 13239 specification (initial register value = 'FFFF').

The PUT sends a WUPB command having the value '05 00 08'.

The PUT sends an ATTRIB command with the last four bytes (Param1 to Param4) having the value '00 08 01 00'.

The Type B frames sent by the PUT are composed of the data bits grouped in characters. A Type B character is composed of a start bit (= Logic "0"), a byte (= 8 data bits) and a stop bit (Logic "1").

The Type A short frames sent by the PUT are composed of a Start of Frame (SoF = Logic "0") followed by 7 data bits and followed by an End of Frame (EoF = Logic "0").

The bytes are transmitted most significant byte first and the bits are transmitted less significant bit first.

The Type B frames sent by the PUT are contained in sequences starting with a Start of Sequence (SoS) i.e. $t_{PCD,S,1,MIN}$ to $t_{PCD,S,1,MAX}$ with carrier low (modulation applied) followed by $t_{PCD,S,2,MIN}$ to $t_{PCD,S,2,MAX}$ with carrier high (no modulation applied), and ending with an End of Sequence (EoS) i.e. $t_{PCD,E,MIN}$ to $t_{PCD,E,MAX}$ with carrier low (modulation applied) followed by a logical state transition (= transition to carrier high). The EoS is immediately after the last data character (i.e. with no EGT).

The Type A frames sent by the PUT are contained in sequences ending with an End of Sequence (EoS) i.e. a full bit duration with no modulation applied.

The delay between two consecutive characters within the command sequences sent by the PUT is at most $EGT_{PCD,MAX}$.

The delay between the end of a sequence sent by the LT and the beginning of the sequence replied by the PUT is at least $FDT_{B,PCD,MIN}$ during installation and block protocol.

The delay between the end of the first ATQB response sequence and the beginning of the next WUPA command sequence is at least $t_{P,MIN}$ and at most $t_{P,MAX}$ with carrier on.

The delay between the end of the WUPA command sequence and the beginning of the WUPB command sequence is at least $t_{P,MIN}$ and at most $t_{P,MAX}$ with carrier on.

The Block number of the first I-Block sent by the PCD is equal to 0.

The Blocks sent by the PCD contain no NAD or CID.

Failure action:

Stop further testing.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + '5A 36 B9 F4' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) sent between t_{P,MIN} and t_{P,MAX} ▶ LT	WUPA
4	PUT ▶ '05 00 08' sent between t_{P,MIN} and t_{P,MAX} ▶ LT	WUPB
5	PUT ◀ '50' + '5A 36 B9 F4' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + '5A 36 B9 F4' + '00 08 01 00' sent after FDT_{B,PCD,MIN} ▶ LT	ATTRIB
7	PUT ◀ '00' ◀ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] sent after FDT_{B,PCD,MIN} ▶ LT	Select PPSE
9	PUT ◀ I(0)₀ ['00 B2 01 04 00' + '90 00'] ◀ LT	
10	PUT ▶ I(0)₁ ['00 B2 01 04 00'] sent after FDT_{B,PCD,MIN} ▶ LT	Loop-back
11	PUT ◀ I(0)₁ ['00 B2 02 04 00' + '90 00'] ◀ LT	
12	PUT ▶ I(0)₀ ['00 B2 02 04 00'] sent after FDT_{B,PCD,MIN} ▶ LT	Loop-back
13	PUT ◀ I(0)₀ ['00 A4 04 00 17' + '01 02 ... 17' + '00' + '90 00'] ◀ LT	
14	PUT ▶ I(0)₁ ['00 A4 04 00 17' + '01 02 ... 17' + '00'] sent after FDT_{B,PCD,MIN} ▶ LT	Loop-back (32 bytes frame)
15	PUT ◀ I(0)₁ ['00 B2 03 04 00' + '90 00'] ◀ LT	
16	PUT ▶ I(0)₀ ['00 B2 03 04 00'] sent after FDT_{B,PCD,MIN} ▶ LT	Loop-back
17	PUT ◀ I(0)₀ ['00 B2 04 04 00' + '90 00'] ◀ LT	
18	PUT ▶ I(0)₁ ['00 B2 04 04 00'] sent after FDT_{B,PCD,MIN} ▶ LT	Loop-back
19	PUT ◀ I(0)₁ ['00 A4 04 00 17' + '18 19 ... 2E' + '00' + '90 00'] ◀ LT	
20	PUT ▶ I(0)₀ ['00 A4 04 00 17' + '18 19 ... 2E' + '00'] sent after FDT_{B,PCD,MIN} ▶ LT	Loop-back (32 bytes frame)
21	PUT ◀ I(0)₀ ["EOT Command" + '90 00'] ◀ LT	End Of Test command
22	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
24	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
25	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 83: Basic Type B Exchange and timings measurement

5.3. Basic Type B Exchange with supported SoS and EoS [TB002.x]

Test codification:

TB002.x

Test objective:

To ensure that the PCD correctly supports all possible timings for the Start of Sequence (SoS) and the End of Sequence (EoS).

References Requirements:

4.3.2.5, 4.6.2.3, 4.6.2.5

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

Until the End Of Test command, the LT sends sequences using the following the Start of Sequence (SoS) and the End of Sequence (EoS) in function of x.

For x=0:

- SoS = $t_{\text{PICC,S},1,\text{MIN}}$ of logical state low (i.e. a subcarrier phase transition followed by the subcarrier with phase φ_0+180°) followed by $t_{\text{PICC,S},2,\text{MIN}}$ of logical state high (i.e. a subcarrier phase transition followed by the subcarrier with phase φ_0)
- EoS = $t_{\text{PICC,E},\text{MIN}}$ of logical state low (i.e. a subcarrier phase transition followed by the subcarrier with phase φ_0+180°) before the LT turns the subcarrier off (directly after the $t_{\text{PICC,E},\text{MIN}}$ of logical state low)

For x=1:

- SoS = $t_{\text{PICC,S},1,\text{MAX}}$ of logical state low (i.e. a subcarrier phase transition followed by the subcarrier with phase φ_0+180°) followed by $t_{\text{PICC,S},2,\text{MAX}}$ of logical state high (i.e. a subcarrier phase transition followed by the subcarrier with phase φ_0)
- EoS = $t_{\text{PICC,E},\text{MAX}}$ of logical state low (i.e. a subcarrier phase transition followed by the subcarrier with phase φ_0+180°) followed by a logical state transition (i.e. a subcarrier phase transition to phase φ_0) and $t_{\text{FSOFF},\text{MAX}}$ with subcarrier on (then the LT turns the subcarrier off)

In this test, the default Protocol Information (PI) shall be used:

PI			Comments
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	Default value

Acceptance criteria:

The PUT accepts the sequences sent by the LT and sends commands and blocks as described in the following scenario (the PUT accepts all possible SoS and EoS).

Failure action:

Stop further testing.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + '50 81 A5 C3' + '00 00 00 00' + PI with SoS and EoS in function of 'x' ▲ LT	ATQB
3	PUT ▶ '52' (<i>Type A short frame</i>) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + '50 81 A5 C3' + '00 00 00 00' + PI with SoS and EoS in function of 'x' ▲ LT	ATQB
6	PUT ▶ '1D' + '50 81 A5 C3' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' with SoS and EoS in function of 'x' ▲ LT	ATTRIB Response
8	PUT ▶ I(0) ₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(0) ₀ ['00 B2 01 04 00' + '90 00'] with SoS and EoS in function of 'x' ▲ LT	
10	PUT ▶ I(0) ₁ ['00 B2 01 04 00'] ▶ LT	Loop-back
11	PUT ◀ I(0) ₁ ['00 B2 02 04 00' + '90 00'] with SoS and EoS in function of 'x' ▲ LT	
12	PUT ▶ I(0) ₀ ['00 B2 02 04 00'] ▶ LT	Loop-back
13	PUT ◀ I(0) ₀ ['00 A4 04 00 17' + '01 02 ... 17' + '00' + '90 00'] with SoS and EoS in function of 'x' ▲ LT	
14	PUT ▶ I(0) ₁ ['00 A4 04 00 17' + '01 02 ... 17' + '00'] ▶ LT	Loop-back (32 bytes frame)
15	PUT ◀ I(0) ₁ ['00 B2 03 04 00' + '90 00'] with SoS and EoS in function of 'x' ▲ LT	
16	PUT ▶ I(0) ₀ ['00 B2 03 04 00'] ▶ LT	Loop-back
17	PUT ◀ I(0) ₀ ['00 B2 04 04 00' + '90 00'] with SoS and EoS in function of 'x' ▲ LT	
18	PUT ▶ I(0) ₁ ['00 B2 04 04 00'] ▶ LT	Loop-back
19	PUT ◀ I(0) ₁ ['00 A4 04 00 17' + '18 19 ... 2E' + '00' + '90 00'] with SoS and EoS in function of 'x' ▲ LT	
20	PUT ▶ I(0) ₀ ['00 A4 04 00 17' + '18 19 ... 2E' + '00'] ▶ LT	Loop-back (32 bytes frame)
21	PUT ◀ I(0) ₀ ["EOT Command" + '90 00'] with SoS and EoS in function of 'x' ▲ LT	End Of Test command

Step	Exchanges	Comments
22	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
23	PUT ▶ '05 00 08'	▶ LT WUPB to poll for the PICC
24	PUT ▶ '05 00 08'	▶ LT WUPB to poll for the PICC
25	PUT ▶ '05 00 08'	▶ LT WUPB to poll for the PICC

Scenario 84: Basic Type B Exchange with supported SoS and EoS (x=0 to 1)

5.4. Type B Correct Removal [TB003]

Test codification:

TB003

Test objective:

To ensure that the PCD respects the timings and the series of commands during the removal of a Type B PICC.

References Requirements:

9.5.1.5, 9.5.1.6, 9.5.1.7, 9.5.1.8

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenarios.

After the end of the ‘End Of Test command’ sequence, The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

The LT measures the delay during which the PUT sends the unmodulated carrier between the end of the PICC Reset and the beginning of the first WUPB command sequence of the removal procedure.

After the PICC Reset, when a sequence sent by the LT is followed by a sequence sent by the PUT, the LT measures the delay between the end of the sequence sent by the LT and the beginning of the sequence replied by the PUT.

Remark: the end of an EMV Contactless PICC sequence is defined as the “start of the EoS transmitted by the PICC”.

After the PICC Reset, when two consecutive sequences are sent by the PUT, the LT measures the delay between the end of the first sequence sent by the PUT and the beginning of the second sequence sent by the PUT.

In this test, the default Protocol Information (PI) shall be used:

PI			Comments
Byte 1	Byte 2	Byte 3	
‘80’	‘21’	‘41’	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (upon receipt of the ‘End Of Test command’, the PUT performs a PICC Reset and ensures that the PICC is removed from the field).

The time during which the PUT stops the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$.

After the PICC Reset, the delay between the end of an ATQB sequence sent by the LT and the beginning of the next WUPB command sequence sent by the PUT is at least $t_{P,MIN}$ and at most $t_{P,MAX}$ with carrier on.

After the PICC Reset, when two consecutive WUPB commands are sent by the PUT, the delay between the end of the first WUPB command sequence and the beginning of the second WUPB command sequence is at most $[FWT_{ATQB} + t_{RETRANSMISSION}]$.

Failure action:

Stop further testing.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ▲ '50' + '50 81 A5 C3' + '00 00 00 00' + PI ▲ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ▲ '50' + '50 81 A5 C3' + '00 00 00 00' + PI ▲ LT	ATQB
6	PUT ▶ '1D' + '50 81 A5 C3' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ▲ '00' ▲ LT	ATTRIB Response
8	PUT ▶ I(0)0 [00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ▲ I(0)0 ["EOT Command" + '90 00'] ▲ LT	End Of Test command
10	PUT II The PUT keeps the carrier off during at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$. □ LT	PICC Reset
11	PUT ▶ '05 00 08' sent between $t_{P,MIN}$ and $t_{P,MAX}$ ▶ LT	WUPB to poll for the PICC
12	PUT ▲ '50' + '50 81 A5 C3' + '00 00 00 00' + PI ▲ LT	ATQB
13	PUT ▶ '05 00 08' sent between $t_{P,MIN}$ and $t_{P,MAX}$ ▶ LT	WUPB to poll for the PICC
14	PUT ▲ '50' + '50 81 A5 C3' + '00 00 00 00' + PI ▲ LT	ATQB
15	PUT ▶ '05 00 08' sent between $t_{P,MIN}$ and $t_{P,MAX}$ ▶ LT	WUPB to poll for the PICC
16	PUT ▲ '50' + '50 81 A5 C3' + '00 00 00 00' + PI ▲ LT	ATQB
17	PUT ▶ '05 00 08' sent between $t_{P,MIN}$ and $t_{P,MAX}$ ▶ LT	WUPB to poll for the PICC
18	PUT ▶ '05 00 08' sent within $[FWT_{ATQB} + t_{RETRANSMISSION}]$ ▶ LT	WUPB to poll for the PICC
19	PUT ▶ '05 00 08' sent within $[FWT_{ATQB} + t_{RETRANSMISSION}]$ ▶ LT	WUPB to poll for the PICC

Scenario 85: Type B Correct Removal

5.5. Basic Type B Exchange with the minimum and the default maximum Frame Delay Time PCD→PICC [TB004.x]

Test codification:

TB004.x

Test objective:

To ensure that the PCD accepts sequences received with the minimum or the maximum Frame Delay Time $FDT_{B,PICC}$ (i.e. the minimum timings $TR0_{MIN}$ and $TR1_{MIN}$, and the maximum timings $TR0_{MAX}$ and FWT) during a basic exchange (installation and block protocol).

References Requirements:

4.3.2.3, 4.8.1.6, 4.8.1.8, 4.8.1.10, 4.8.1.14

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

For $x=0$:

Until the End Of Test command (included), the LT sends sequences (commands and blocks) using the minimum Frame Delay Time $FDT_{B,PICC,MIN} = TR0_{MIN} + TR1_{MIN}$ (i.e. no subcarrier during $TR0_{MIN}$ and subcarrier with no phase transition during $TR1_{MIN}$) between the end of the sequence sent by the PUT and the beginning of the sequence replied by the LT.

For $x=1$:

During installation, the LT replies to the first WUPB command using the maximum Frame Delay Time $FWT_{ATQB} = TR0 + TR1_{MAX}$ (i.e. no subcarrier during $FWT_{ATQB} - TR1_{MAX}$ and subcarrier with no phase transition during $TR1_{MAX}$) between the end of the sequence sent by the PUT and the beginning of the sequence replied by the LT.

During installation, the LT replies to the second WUPB command using the maximum Frame Delay Time $FWT_{ATQB} = TR0_{MAX,ATQB} + TR1$ (i.e. no subcarrier during $TR0_{MAX,ATQB}$ and subcarrier with no phase transition during $FWT_{ATQB} - TR0_{MAX,ATQB}$) between the end of the sequence sent by the PUT and the beginning of the sequence replied by the LT.

Until the End Of Test command (included), the LT replies to all other commands and blocks using the default maximum Frame Delay Time $FDT_{B,PICC,MAX} = TR0 + TR1_{MAX}$ (i.e. no subcarrier during $FDT_{B,PICC,MAX} - TR1_{MAX}$ and subcarrier with no phase transition during $TR1_{MAX}$) between the end of the sequence sent by the PUT and the beginning of the sequence replied by the LT - with:

- $FDT_{B,PICC,MAX} = (FWT + \Delta FWT) = 114688 \times 1/f_c$ as the default value of FWT is used in this test

In this test, the default Protocol Information (PI) shall be used:

PI			FWT+ΔFWT
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	114688x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to the sequences sent by the LT with the minimum or the maximum Frame Delay Time).

Failure action:

Stop further testing.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + '6B 47 CA 15' + '00 00 00 00' + PI ↴ LT sent using the Frame Delay Time in function of 'x'	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + '6B 47 CA 15' + '00 00 00 00' + PI ↴ LT sent using the Frame Delay Time in function of 'x'	ATQB
6	PUT ▶ '1D' + '6B 47 CA 15' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' sent using the Frame Delay Time in function of 'x' ↴ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 B2 01 04 00' + '90 00'] ↴ LT sent using the Frame Delay Time in function of 'x'	
10	PUT ▶ I(0)₁ ['00 B2 01 04 00'] ▶ LT	Loop-back
11	PUT ↴ I(0)₁ ['00 B2 02 04 00' + '90 00'] ↴ LT sent using the Frame Delay Time in function of 'x'	
12	PUT ▶ I(0)₀ ['00 B2 02 04 00'] ▶ LT	Loop-back
13	PUT ↴ I(0)₀ ['00 A4 04 00 17' + '01 02 ... 17' + '00' + '90 00'] ↴ LT sent using the Frame Delay Time in function of 'x'	
14	PUT ▶ I(0)₁ ['00 A4 04 00 17' + '01 02 ... 17' + '00'] ▶ LT	Loop-back (32 bytes frame)
15	PUT ↴ I(0)₁ ['00 B2 03 04 00' + '90 00'] ↴ LT sent using the Frame Delay Time in function of 'x'	
16	PUT ▶ I(0)₀ ['00 B2 03 04 00'] ▶ LT	Loop-back
17	PUT ↴ I(0)₀ ['00 B2 04 04 00' + '90 00'] ↴ LT sent using the Frame Delay Time in function of 'x'	
18	PUT ▶ I(0)₁ ['00 B2 04 04 00'] ▶ LT	Loop-back
19	PUT ↴ I(0)₁ ['00 A4 04 00 17' + '18 19 ... 2E' + '00' + '90 00'] ↴ LT sent using the Frame Delay Time in function of 'x'	

Step	Exchanges	Comments
20	PUT ▶ I(0)₀ ['00 A4 04 00 17' + '18 19 ... 2E' + '00'] ▶ LT	Loop-back (32 bytes frame)
21	PUT ↵ I(0)₀ ['EOT Command' + '90 00'] ↵ LT sent using the Frame Delay Time in function of 'x'	End Of Test command
22	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
24	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
25	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 86: Basic Type B Exchange with the minimum and the default maximum Frame Delay Time PCD→PICC (x=0 and 1)

5.6. Basic Type B Exchange with the minimum and the maximum character-to-character delay [TB006.x]

Test codification:

TB006.x

Test objective:

To ensure that the PCD accepts sequences received with the minimum or the maximum character-to-character delay EGT_{PICC} during a basic exchange (installation and block protocol).

References Requirement:

4.5.1.2, 4.6.2.3a

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenarios.

For $x=0$:

Until the End Of Test command, the LT sends commands and blocks using the minimum character-to-character delay $EGT_{PICC,MIN}$ between two consecutive characters within a sequence sent to the PUT.

For $x=1$:

Until the End Of Test command, the LT sends commands and blocks using the maximum character-to-character delay $EGT_{PICC,MAX}$ between two consecutive characters within a sequence sent to the PUT.

The LT sends commands and blocks using the delay $EGT_{PICC,MAX}$ between the last character and the EoS within a sequence sent to the PUT.

In this test, the default Protocol Information (PI) shall be used:

PI			Comments
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to the sequences sent by the LT with the minimum or the maximum character-to-character delay).

Failure action:

Stop further testing

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + '50 81 A5 C3' + '00 00 00 00' + PI sent with EGT _{PICC} in function of 'x' ▲ LT	ATQB
3	PUT ▶ '52' (<i>Type A short frame</i>) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + '50 81 A5 C3' + '00 00 00 00' + PI sent with EGT _{PICC} in function of 'x' ▲ LT	ATQB
6	PUT ▶ '1D' + '50 81 A5 C3' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' sent with EGT _{PICC} in function of 'x' ▲ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 B2 01 04 00' + '90 00'] sent with EGT _{PICC} in function of 'x' ▲ LT	
10	PUT ▶ I(0)₁ ['00 B2 01 04 00'] ▶ LT	Loop-back
11	PUT ↴ I(0)₁ ['00 B2 02 04 00' + '90 00'] sent with EGT _{PICC} in function of 'x' ▲ LT	
12	PUT ▶ I(0)₀ ['00 B2 02 04 00'] ▶ LT	Loop-back
13	PUT ↴ I(0)₀ ['00 A4 04 00 17' + '01 02 ... 17' + '00' + '90 00'] sent with EGT _{PICC} in function of 'x' ▲ LT	
14	PUT ▶ I(0)₁ ['00 A4 04 00 17' + '01 02 ... 17' + '00'] ▶ LT	Loop-back (32 bytes frame)
15	PUT ↴ I(0)₁ ['00 B2 03 04 00' + '90 00'] sent with EGT _{PICC} in function of 'x' ▲ LT	
16	PUT ▶ I(0)₀ ['00 B2 03 04 00'] ▶ LT	Loop-back
17	PUT ↴ I(0)₀ ['00 B2 04 04 00' + '90 00'] sent with EGT _{PICC} in function of 'x' ▲ LT	
18	PUT ▶ I(0)₁ ['00 B2 04 04 00'] ▶ LT	Loop-back
19	PUT ↴ I(0)₁ ['00 A4 04 00 17' + '18 19 ... 2E' + '00' + '90 00'] sent with EGT _{PICC} in function of 'x' ▲ LT	
20	PUT ▶ I(0)₀ ['00 A4 04 00 17' + '18 19 ... 2E' + '00'] ▶ LT	Loop-back (32 bytes frame)
21	PUT ↴ I(0)₀ [“EOT Command” + '90 00'] sent with EGT _{PICC} in function of 'x' ▲ LT	End Of Test command
22	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) □ LT	PICC Reset

Step	Exchanges	Comments
23	PUT ▶ '05 00 08'	▶ LT WUPB to poll for the PICC
24	PUT ▶ '05 00 08'	▶ LT WUPB to poll for the PICC
25	PUT ▶ '05 00 08'	▶ LT WUPB to poll for the PICC

Scenario 87: Basic Type B Exchange with the minimum and the maximum character-to-character delay (x=0 and 1)

5.7. Type B Installation with supported values of ADC [TB101.x]

Test codification:

TB101.x

Test objective:

To ensure that the PCD accepts all the possible values of ADC in the Byte 3 of the Protocol Info field of ATQB.

References Requirement:

6.3.2.13

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

In this test, the following Protocol Information (PI) shall be used:

PI				ADC value
	Byte 1	Byte 2	Byte 3	
-	'80'	'21'	'41'	$(00)_b$ already tested in TB001
x=0	'80'	'21'	'45'	$(01)_b$
x=1	'80'	'21'	'49'	$(10)_b$
x=2	'80'	'21'	'4D'	$(11)_b$

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to ATQB).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + '50 81 A5 C3' + '00 00 00 00' + PI with ADC in function of 'x' ▶ LT	ATQB in function of 'x'
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + '50 81 A5 C3' + '00 00 00 00' + PI with ADC in function of 'x' ▶ LT	ATQB in function of 'x'
6	PUT ▶ '1D' + '50 81 A5 C3' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' ▶ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(0)₀ ["EOT Command" + '90 00'] ▶ LT	End Of Test command
10	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
11	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
12	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
13	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 88: Type B Installation with supported values of ADC (x=0 to 2)

5.8. Type B Installation with supported values of FO [TB102.x]

Test codification:

TB102.x

Test objective:

To ensure that the PCD accepts all the possible values of FO in the Byte 3 of the Protocol Info field of ATQB.

References Requirement:

6.3.2.14

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

In this test, the following Protocol Information (PI) shall be used:

PI				FO value
	Byte 1	Byte 2	Byte 3	
x=0	'80'	'21'	'40'	(00) _b
-	'80'	'21'	'41'	(01) _b already tested in TB001
x=1	'80'	'21'	'42'	(10) _b
x=2	'80'	'21'	'43'	(11) _b

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to ATQB and sends all its Blocks with no CID/NAD bytes in the prologue field).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + '50 81 A5 C3' + '00 00 00 00' + PI with FO in function of 'x' ▶ LT	ATQB in function of 'x'
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + '50 81 A5 C3' + '00 00 00 00' + PI with FO in function of 'x' ▶ LT	ATQB in function of 'x'
6	PUT ▶ '1D' + '50 81 A5 C3' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ▶ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ["EOT Command" + '90 00'] ▶ LT	End Of Test command
10	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
11	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
12	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
13	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 89: Type B Installation with supported values of FO (x=0 to 2)

5.9. Type B Installation with supported values of Bit_Rate_Capability [TB104.x]

Test codification:

TB104.x

Test objective:

To ensure that the PCD accepts all the possible values of Bit_Rate_Capability in the Byte 1 of the Protocol Info field of ATQB.

References Requirement:

6.3.2.4, 6.3.2.5a

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

In this test, the following Protocol Information (PI) shall be used:

PI				Comments
	Byte 1	Byte 2	Byte 3	
x=0	'08'	'21'	'41'	Different correct values of Bit_Rate_Capability
x=1	'00'	'21'	'41'	
x=2	'88'	'21'	'41'	
x=3	'FF'	'21'	'41'	

Remark: The Bit_Rate_Capability value '80' is implicitly tested in most of the other tests.

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to ATQB).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↵ '50' + '50 81 A5 C3' + '00 00 00 00' + PI with Bit_Rate_Capability in function of 'x' ▶ LT	ATQB in function of 'x'
3	PUT ▶ '52' (<i>Type A short frame</i>) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↵ '50' + '50 81 A5 C3' + '00 00 00 00' + PI with Bit_Rate_Capability in function of 'x' ▶ LT	ATQB in function of 'x'
6	PUT ▶ '1D' + '50 81 A5 C3' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↵ '00' ▶ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↵ I(0)₀ ["EOT Command" + '90 00'] ▶ LT	End Of Test command
10	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
11	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
12	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
13	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 90: Type B Installation with supported values of Bit_Rate_Capability (x=0 to 3)

5.10.Type B Installation with supported values of ADF [TB106.x]

Test codification:

TB106.x

Test objective:

To ensure that the PCD disregards the value of ADF in the Bytes 6 to 9 of the ATQB.

References Requirement:

6.3.2.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The following ATQB responses are successively sent by the LT:

- x=0: ATQB = '50' + '89 00 00 AF' + 'FF FF FF FF' + PI
- x=1: ATQB = '50' + '89 00 00 AF' + 'A5 A5 A5 A5' + PI
- x=2: ATQB = '50' + '89 00 00 AF' + '3C 3C 3C 3C' + PI
- x=3: ATQB = '50' + '89 00 00 AF' + 'E1 5E F3 11' + PI

In this test, the following Protocol Information (PI) shall be used:

	PI			ADC value
	Byte 1	Byte 2	Byte 3	
x=0-2	'80'	'21'	'41'	(00) _b i.e. ADF is proprietary
x=3	'80'	'21'	'45'	(01) _b i.e. ADF is ISO 14443 compliant

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to ATQB).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↲ ATQB in function of 'x' For x=0: ATQB = '50' + '89 00 00 AF' + 'FF FF FF FF' + PI For x=1: ATQB = '50' + '89 00 00 AF' + 'A5 A5 A5 A5' + PI For x=2: ATQB = '50' + '89 00 00 AF' + '3C 3C 3C 3C' + PI For x=3: ATQB = '50' + '89 00 00 AF' + 'E1 5E F3 11' + PI ▲ LT	ATQB in function of 'x'
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↲ ATQB in function of 'x' For x=0: ATQB = '50' + '89 00 00 AF' + 'FF FF FF FF' + PI For x=1: ATQB = '50' + '89 00 00 AF' + 'A5 A5 A5 A5' + PI For x=2: ATQB = '50' + '89 00 00 AF' + '3C 3C 3C 3C' + PI For x=3: ATQB = '50' + '89 00 00 AF' + 'E1 5E F3 11' + PI ▲ LT	ATQB in function of 'x'
6	PUT ▶ '1D' + '89 00 00 AF' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↲ '00' ▲ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↲ I(0)₀ ["EOT Command" + '90 00'] ▲ LT	End Of Test command
10	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) □ LT	PICC Reset
11	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
12	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
13	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 91: Type B Installation with supported values of ADF (x=0 to 3)

5.11.Type B Installation with supported values of b4-b2 of Protocol_Type [TB107.x]

Test codification:

TB107.x

Test objective:

To ensure that the PCD disregards the value of bits b4-b2 of Protocol_Type in the Protocol Info field Byte 2 of the ATQB and always uses FDT_{B,PCD,MIN} as minimum TR2.

References Requirements:

4.8.2.1, 6.3.2.10

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

Until the End Of Test command, when a Type B sequence sent by the LT is followed by a Type B sequence sent by the PUT, the LT measures the delay between the end of the sequence sent by the LT and the beginning of the sequence replied by the PUT.

Remark: the end of an EMV Contactless PICC sequence is defined as the “start of the EoS transmitted by the PICC”.

In this test, the following Protocol Information (PI) shall be used:

PI				Comments
	Byte 1	Byte 2	Byte 3	
x=0	'80'	'21'	'41'	Different correct values of b4-b2 of Protocol_Type
x=1	'80'	'23'	'41'	
x=2	'80'	'25'	'41'	
x=3	'80'	'27'	'41'	

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to ATQB and continues the transaction using the correct Frame Delay Time).

The delay between the end of a Type B sequence sent by the LT and the beginning of the Type B sequence replied by the PUT is at least FDT_{B,PCD,MIN} during installation and block protocol.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + 'B1 83 C8 88' + '00 00 00 00' + PI with an error in PI in function of 'x' ▲ LT	ATQB in function of 'x'
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + 'B1 83 C8 88' + '00 00 00 00' + PI with an error in PI in function of 'x' ▲ LT	ATQB in function of 'x'
6	PUT ▶ '1D' + 'B1 83 C8 88' + '00 08 01 00' sent after FDT_{B,PCD,MIN} ▶ LT	ATTRIB
7	PUT ↴ '00' ▲ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] sent after FDT_{B,PCD,MIN} ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 B2 01 04 00' + '90 00'] ▲ LT	
10	PUT ▶ I(0)₁ ['00 B2 01 04 00'] sent after FDT_{B,PCD,MIN} ▶ LT	Loop-back
11	PUT ↴ I(0)₁ ['00 B2 02 04 00' + '90 00'] ▲ LT	
12	PUT ▶ I(0)₀ ['00 B2 02 04 00'] sent after FDT_{B,PCD,MIN} ▶ LT	Loop-back
13	PUT ↴ I(0)₀ ['00 A4 04 00 17' + '01 02 ... 17' + '00' + '90 00'] ▲ LT	
14	PUT ▶ I(0)₁ ['00 A4 04 00 17' + '01 02 ... 17' + '00'] sent after FDT_{B,PCD,MIN} ▶ LT	Loop-back (32 bytes frame)
15	PUT ↴ I(0)₁ ['00 B2 03 04 00' + '90 00'] ▲ LT	
16	PUT ▶ I(0)₀ ['00 B2 03 04 00'] sent after FDT_{B,PCD,MIN} ▶ LT	Loop-back
17	PUT ↴ I(0)₀ ["EOT Command" + '90 00'] ▲ LT	End Of Test command
18	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) □ LT	PICC Reset
19	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
20	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
21	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 92: Type B Installation with supported values of b4-b2 of Protocol_Type (x=0 to 3)

5.12.Type B Installation with supported values of MBLI [TB108.x]

Test codification:

TB108.x

Test objective:

To ensure that the PCD disregards the value of MBLI in the most significant nibble of the first byte of the ATTRIB Response.

References Requirement:

6.4.2.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The following ATTRIB Responses are successively sent by the LT:

- x=0: ATTRIB Response = 'F0'
- x=1: ATTRIB Response = 'C0'
- x=2: ATTRIB Response = '10'
- x=3: ATTRIB Response = '20'
- x=4: ATTRIB Response = '30'

In this test, the default Protocol Information (PI) shall be used:

PI			Comments
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to ATTRIB Response).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + 'D5 1E 70 8E' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + 'D5 1E 70 8E' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + 'D5 1E 70 8E' + '00 08 01 00' ▶ LT	ATTRIB
7	ATTRIB Response in function of 'x' For x=0: ATTRIB Response = 'F0' For x=1: ATTRIB Response = 'C0' For x=2: ATTRIB Response = '10' For x=3: ATTRIB Response = '20' For x=4: ATTRIB Response = '30' PUT ◀ ▲ LT	ATTRIB Response in function of 'x'
8	PUT ▶ I(0)0 ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(0)0 ["EOT Command" + '90 00'] ◀ LT	End Of Test command
10	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) □ LT	PICC Reset
11	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
12	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
13	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 93: Type B Installation with supported values of MBLI (x=0 to 4)

5.13.Type B Installation with different values of ATQB [TB110.x]

Test codification:

TB110.x

Test objective:

To ensure that the PCD does not compare the different ATQB received during polling and collision detection and only takes the value of the second ATQB into account.

References Requirements:

6.4.1.1, 9.2.1.4

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

During the polling procedure and during the collision detection procedure, the LT sends ATQB responses having different values (ATQB with different values of the fields PUPI, ADF or Protocol Info).

The following ATQB responses are successively sent by the LT during the polling procedure (following the first WUPB command received from the PUT):

- x=0: ATQB = '50' + 'C3 5A 10 7E' + '00 00 00 00' + PI
- x=1: ATQB = '50' + '3C A5 EF 81' + 'FF A5 5A FF' + PI
- x=2: ATQB = '50' + '3C A5 EF 81' + '00 00 00 00' + '88 21 41'
- x=3: ATQB = '50' + '3C A5 EF 81' + '00 00 00 00' + '00 81 41'
- x=4: ATQB = '50' + '3C A5 EF 81' + '00 00 00 00' + '00 21 01'
- x=5: ATQB = '50' + '3C A5 EF 81' + '00 00 00 00' + '00 21 41 88' (extended ATQB)

And for x=0 to 5, the LT sends the standard ATQB response during the collision detection procedure (following the second WUPB command received from the PUT): ATQB = '50' + '3C A5 EF 81' + '00 00 00 00' + PI.

For x=4 only, the LT replies to the first block of the Block Protocol sent by the PUT using the maximum Frame Delay Time $FDT_{B,PICC,MAX} = 71680 \times 1/f_c$ (corresponding to the default value of FWI = 4) between the end of the sequence sent by the PUT and the beginning of the sequence replied by the LT.

In this test, the default Protocol Information (PI) shall be used (except when the scenario defines a specific value for the ATQB sent during the polling procedure):

PI	Comments	
Byte 1	Byte 2	Byte 3
'80'	'21'	'41'

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to ATQB and takes only the value of the second ATQB into account).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↵ ATQB in function of 'x' For x=0: ATQB = '50' + 'C3 5A 10 7E' + '00 00 00 00' + PI For x=1: ATQB = '50' + '3C A5 EF 81' + 'FF A5 5A FF' + PI For x=2: ATQB = '50' + '3C A5 EF 81' + '00 00 00 00' + '88 21 41' PUT ↵ For x=3: ATQB = '50' + '3C A5 EF 81' + '00 00 00 00' + '00 81 41' For x=4: ATQB = '50' + '3C A5 EF 81' + '00 00 00 00' + '00 21 01' For x=5: ATQB = '50' + '3C A5 EF 81' + '00 00 00 00' + '00 21 41 88' (extended ATQB)	ATQB in function of 'x'
3	PUT ▶ '52' (<i>Type A short frame</i>) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↵ '50' + '3C A5 EF 81' + '00 00 00 00' + PI ▶ LT	ATQB
6	PUT ▶ '1D' + '3C A5 EF 81' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↵ '00' ▶ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↵ I(0)₀ ['00 A4 04 00 24' + '01 02 ... 24' + '00' + '90 00'] sent using FDT _{B,PICC,MAX} for x=4 only ▶ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 24' + '01 02 ... 18'] ▶ LT	32 bytes frame
11	PUT ↵ R(ACK)₁ ▶ LT	Acknowledgment R-Block
12	PUT ▶ I(0)₀ ['19 1A 1B ... 22 23 24' + '00'] ▶ LT	16 bytes frame
13	PUT ↵ I(0)₀ ["EOT Command" + '90 00'] ▶ LT	End Of Test command
14	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
15	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
16	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
17	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 94: Type B Installation with different values of ATQB (x=0 to 5)

5.14.Type B Error free non-chained I-Blocks exchanges for all possible values of FWT [TB201.xy]

Test codification:

TB201.xy

Test objective:

To ensure that the PCD accepts all the possible values of FWI in the Byte 3 of the Protocol Info field of the ATQB and accepts sequences received with the corresponding maximum Frame Delay Time $FDT_{B,PICC}$ (i.e. the maximum timings $TR0_{MAX}$ and FWT) during the EMV Contactless transaction.

References Requirements:

4.8.1.8, 4.8.1.10, 6.3.2.12a, 6.3.2.12b

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

Until the End Of Test command, the LT replies to the WUPB command using the maximum Frame Delay Time $FWT_{ATQB} = TR0 + TR1_{MAX}$ (i.e. no subcarrier during $FWT_{ATQB} - TR1_{MAX}$ and subcarrier with no phase transition during $TR1_{MAX}$) between the end of the sequence sent by the PUT and the beginning of the sequence replied by the LT.

Until the End Of Test command (included), the LT replies to all other commands and blocks using the maximum Frame Delay Time $FDT_{B,PICC,MAX} = TR0 + TR1_{MAX}$ (i.e. no subcarrier during $FDT_{B,PICC, MAX} - TR1_{MAX}$ and subcarrier with no phase transition during $TR1_{MAX}$) between the end of the sequence sent by the PUT and the beginning of the sequence replied by the LT - with:

- $FDT_{B,PICC,MAX} = (FWT + \Delta FWT)$

In this test, the following Protocol Information (PI) and Frame Waiting Time shall be used:

PI				$FWT + \Delta FWT$
	Byte 1	Byte 2	Byte 3	
xy=00	'80'	'21'	'01'	$53248 \times 1/f_c$
xy=01	'80'	'21'	'11'	$57344 \times 1/f_c$
xy=02	'80'	'21'	'21'	$65536 \times 1/f_c$
xy=03	'80'	'21'	'31'	$81920 \times 1/f_c$
-	'80'	'21'	'41'	Already tested in TB004.1 (default value)
xy=04	'80'	'21'	'51'	$180224 \times 1/f_c$
xy=05	'80'	'21'	'61'	$311296 \times 1/f_c$
xy=06	'80'	'21'	'71'	$573440 \times 1/f_c$

PI				FWT+ΔFWT
	Byte 1	Byte 2	Byte 3	
xy=07	'80'	'21'	'81'	1097728 x 1/f _c
xy=08	'80'	'21'	'91'	2146304 x 1/f _c
xy=09	'80'	'21'	'A1'	4243456 x 1/f _c
xy=10	'80'	'21'	'B1'	8437760 x 1/f _c
xy=11	'80'	'21'	'C1'	16826368 x 1/f _c
xy=12	'80'	'21'	'D1'	33603584 x 1/f _c
xy=13	'80'	'21'	'E1'	67158016 x 1/f _c
xy=14	'80'	'21'	'F1'	114688 x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts all the sequences sent by the LT with the maximum Frame Delay Time).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + '7C 58 DB 26' + '00 00 00 00' + PI ↴ LT sent using FWT _{ATQB}	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + '7C 58 DB 26' + '00 00 00 00' + PI ↴ LT sent using FWT _{ATQB}	ATQB
6	PUT ▶ '1D' + '7C 58 DB 26' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' sent using FDT_{B,PICC,MAX} in function of 'xy' ↴ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 B2 01 04 00' + '90 00'] ↴ LT sent using FDT _{B,PICC,MAX} in function of 'xy'	
10	PUT ▶ I(0)₁ ['00 B2 01 04 00'] ▶ LT	Loop-back
11	PUT ↴ I(0)₁ ['00 B2 02 04 00' + '90 00'] ↴ LT sent using FDT _{B,PICC,MAX} in function of 'xy'	
12	PUT ▶ I(0)₀ ['00 B2 02 04 00'] ▶ LT	Loop-back
13	PUT ↴ I(0)₀ ['00 A4 04 00 17' + '01 02 ... 17' + '00' + '90 00'] ↴ LT sent using FDT _{B,PICC,MAX} in function of 'xy'	

Step	Exchanges	Comments
14	PUT ▶ I(0)₁ ['00 A4 04 00 17' + '01 02 ... 17' + '00'] ▶ LT	Loop-back
15	PUT ◀ I(0)₁ ['00 B2 03 04 00' + '90 00'] ◀ LT sent using FDT _{B,PICC,MAX} in function of 'xy'	
16	PUT ▶ I(0)₀ ['00 B2 03 04 00'] ▶ LT	Loop-back
17	PUT ◀ I(0)₀ ['00 B2 04 04 00' + '90 00'] ◀ LT sent using FDT _{B,PICC,MAX} in function of 'xy'	
18	PUT ▶ I(0)₁ ['00 B2 04 04 00'] ▶ LT	Loop-back
19	PUT ◀ I(0)₁ ['00 A4 04 00 17' + '18 19 ... 2E' + '00' + '90 00'] ◀ LT sent using FDT _{B,PICC,MAX} in function of 'xy'	
20	PUT ▶ I(0)₀ ['00 A4 04 00 17' + '18 19 ... 2E' + '00'] ▶ LT	Loop-back
21	PUT ◀ I(0)₀ [“EOT Command” + '90 00'] ◀ LT sent using FDT _{B,PICC,MAX} in function of 'xy'	End Of Test command
22	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) □ LT	PICC Reset
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
24	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
25	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 95: Type B Error free non-chained I-Blocks exchanges for all possible values of FWT (xy=00 to 14)

5.15.Type B Error free chained I-Blocks in both directions for FSC = 256 bytes [TB202.xy]

Test codification:

TB202.xy

Test objective:

To ensure that the PCD accepts the values FSCI = '8' to 'F' in the Byte 2 of the Protocol Info field of the ATQB and is able to correctly send and receive chained I-Blocks of size up to 256 bytes.

References Requirements:

4.7.3.1, 4.7.4.1, 4.7.4.3, 6.3.2.7, 10.1.1.1, 10.1.1.3, 10.3.2.1, 10.3.2.2, 10.3.3.3, 10.3.4.5

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Run y=0, if the PCD does not send empty I-Block after chained blocks (see ICS).

Run y=1, if the PCD may send empty I-blocks after a chain of I-Blocks (see ICS).

Procedure:

Run the following scenarios.

When the sequences sent by the LT are followed by a sequence sent by the PUT containing R(ACK)-Blocks, the LT measures the delay between the end of the sequence sent by the LT and the beginning of the sequence replied by the PUT.

During the Half-Duplex Block Protocol and until the End Of Test command, the LT replies to all the blocks sent by the PUT using a Frame Delay Time as follows between the end of a sequence sent by the PUT and the beginning of the next sequence replied by the LT:

- For x=0 to 7, $FDT_{B,PICC} = 3840 \times 1/f_c$ (with $TR0 = 1920 \times 1/f_c$ and $TR1 = 1920 \times 1/f_c$)
- For x=8, $FDT_{B,PICC} = FDT_{B,PICC,MIN}$

In this test, the following Protocol Information (PI) shall be used:

	PI			Maximum Frame Size for the PICC (FSC)
	Byte 1	Byte 2	Byte 3	
x=0	'80'	'81'	'41'	256 bytes
x=1	'80'	'91'	'41'	
x=2	'80'	'A1'	'41'	
x=3	'80'	'B1'	'41'	
x=4	'80'	'C1'	'41'	
x=5	'80'	'D1'	'41'	
x=6	'80'	'E1'	'41'	
x=7	'80'	'F1'	'41'	
x=8	'80'	'81'	'41'	

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends sequences containing up to 256 bytes and uses chaining when necessary).

The delay between the end of a sequence sent by the LT and the beginning of the sequence replied by the PUT containing a R(ACK)-Block is at least FDT_{B,PCD,MIN}.

The delay between the end of a sequence sent by the LT and the beginning of the sequence replied by the PUT is at least FDT_{B,PCD,MIN} during installation and block protocol.

Failure action:

Proceed with the next test.

Scenarios:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ▲ '50' + '8D 69 EC 37' + '00 00 00 00' + PI ▲ LT with Byte 2 of PI in function of 'x'	ATQB in function of 'x'
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ▲ '50' + '8D 69 EC 37' + '00 00 00 00' + PI ▲ LT with Byte 2 of PI in function of 'x'	ATQB in function of 'x'
6	PUT ▶ '1D' + '8D 69 EC 37' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ▲ '00' ▲ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ▲ I(1)₀ ['00 A4 04 00 18' + '01 02 03 ... 06 07 08'] ▲ LT	16 bytes frame
10	PUT ▶ R(ACK) ₁ sent after FDT _{B,PCD,MIN} ▶ LT	Acknowledgment R-Block

Step	Exchanges	Comments
11	PUT \leftarrow I(1) ₁ ['09 0A 0B ... 13 14 15']	\leftarrow LT 16 bytes frame
12	PUT \rightarrow R(ACK) ₀ sent after FDT _{B,PCD,MIN}	\rightarrow LT Acknowledgment R-Block
13	PUT \leftarrow I(0) ₀ ['16 17 18' + '00' + '90 00']	\leftarrow LT 9 bytes last Block of chain
14	PUT \rightarrow I(0) ₁ ['00 A4 04 00 18' + '01 02 03 ... 16 17 18' + '00']	\rightarrow LT Loop-back
15	PUT \leftarrow I(1) ₁ ['00 A4 04 00 47' + '01 02 03 ... 16 17 18']	\leftarrow LT 32 bytes frame
16	PUT \rightarrow R(ACK) ₀ sent after FDT _{B,PCD,MIN}	\rightarrow LT Acknowledgment R-Block
17	PUT \leftarrow I(1) ₀ ['19 1A 1B ... 33 34 35']	\leftarrow LT 32 bytes frame
18	PUT \rightarrow R(ACK) ₁ sent after FDT _{B,PCD,MIN}	\rightarrow LT Acknowledgment R-Block
19	PUT \leftarrow I(0) ₁ ['36 37 ... 46 47' + '00' + '90 00']	\leftarrow LT 24 bytes last Block of chain
20	PUT \rightarrow I(0) ₀ ['00 A4 04 00 47' + '01 02 03 ... 45 46 47' + '00']	\rightarrow LT Loop-back
21	PUT \leftarrow I(1) ₀ ['00 A4 04 00 87' + '01 02 03 ... 36 37 38']	\leftarrow LT 64 bytes frame
22	PUT \rightarrow R(ACK) ₁ sent after FDT _{B,PCD,MIN}	\rightarrow LT Acknowledgment R-Block
23	PUT \leftarrow I(1) ₁ ['39 3A 3B ... 73 74 75']	\leftarrow LT 64 bytes frame
24	PUT \rightarrow R(ACK) ₀ sent after FDT _{B,PCD,MIN}	\rightarrow LT Acknowledgment R-Block
25	PUT \leftarrow I(0) ₀ ['76 77 78 ... 85 86 87' + '00' + '90 00']	\leftarrow LT 24 bytes last Block of chain
26	PUT \rightarrow I(0) ₁ ['00 A4 04 00 87' + '01 02 03 ... 85 86 87' + '00']	\rightarrow LT Loop-back
27	PUT \leftarrow I(1) ₁ ['00 A4 04 00 F7' + '01 02 03 ... 76 77 78']	\leftarrow LT 128 bytes frame
28	PUT \rightarrow R(ACK) ₀ sent after FDT _{B,PCD,MIN}	\rightarrow LT Acknowledgment R-Block
29	PUT \leftarrow I(1) ₀ ['79 7A 7B ... F3 F4 F5']	\leftarrow LT 128 bytes frame
30	PUT \rightarrow R(ACK) ₁ sent after FDT _{B,PCD,MIN}	\rightarrow LT Acknowledgment R-Block
31	PUT \leftarrow I(1) ₁ []	\leftarrow LT Empty I-Block indicating chaining
32	PUT \rightarrow R(ACK) ₀ sent after FDT _{B,PCD,MIN}	\rightarrow LT Acknowledgment R-Block
33	PUT \leftarrow I(0) ₀ ['F6 F7' + '00' + '90 00']	\leftarrow LT 8 bytes frame
34	PUT \rightarrow I(0) ₁ ['00 A4 04 00 F7' + '01 02 ... 46 F7' + '00']	\rightarrow LT Loop-back (256 bytes non chained block)
35	PUT \leftarrow I(1) ₁ ['00 A4 04 00 F8' + '01 02 03 ... F6 F7 F8']	\leftarrow LT 256 bytes chained block

Step	Exchanges		Comments
36	PUT ▶ R(ACK)₀ sent after FDT_{B,PCD,MIN}	▶ LT	Acknowledgment R-Block
37	PUT ◀ I(0)₀ ['00' + '90 00']	◀ LT	6 bytes frame
38	PUT ▶ I(1)₁ ['00 A4 04 00 F8' + '01 02 03 ... F6 F7 F8']	▶ LT	Loop-back (256 bytes chained block)
39	PUT ◀ R(ACK)₁	◀ LT	Acknowledgment R-Block
40	PUT ▶ I(0)₀ ['00']	▶ LT	Loop-back (4 bytes frame)
41	PUT ◀ I(0)₀ ['EOT Command' + '90 00']	◀ LT	End Of Test command
42	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT	PICC Reset
43	PUT ▶ '05 00 08'	▶ LT	WUPB to poll for the PICC
44	PUT ▶ '05 00 08'	▶ LT	WUPB to poll for the PICC
45	PUT ▶ '05 00 08'	▶ LT	WUPB to poll for the PICC

**Scenario 96: Type B Error free chained I-Blocks in both directions for FSC = 256 bytes
(x=0 to 8, y=0)**

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + '8D 69 EC 37' + '00 00 00 00' + PI with Byte 2 of PI in function of 'x' ▶ LT	ATQB in function of 'x'
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + '8D 69 EC 37' + '00 00 00 00' + PI with Byte 2 of PI in function of 'x' ▶ LT	ATQB in function of 'x'
6	PUT ▶ '1D' + '8D 69 EC 37' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ▶ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(1)₀ ['00 A4 04 00 18' + '01 02 03 ... 06 07 08'] ▶ LT	16 bytes frame
10	PUT ▶ R(ACK)₁ sent after FDT_{B,PCD,MIN} ▶ LT	Acknowledgment R-Block
11	PUT ↴ I(1)₁ ['09 0A 0B ... 13 14 15'] ▶ LT	16 bytes frame
12	PUT ▶ R(ACK)₀ sent after FDT_{B,PCD,MIN} ▶ LT	Acknowledgment R-Block
13	PUT ↴ I(0)₀ ['16 17 18' + '00' + '90 00'] ▶ LT	9 bytes last Block of chain
14	PUT ▶ I(0)₁ ['00 A4 04 00 18' + '01 02 03 ... 16 17 18' + '00'] ▶ LT	Loop-back
15	PUT ↴ I(1)₁ ['00 A4 04 00 47' + '01 02 03 ... 16 17 18'] ▶ LT	32 bytes frame
16	PUT ▶ R(ACK)₀ sent after FDT_{B,PCD,MIN} ▶ LT	Acknowledgment R-Block
17	PUT ↴ I(1)₀ ['19 1A 1B ... 33 34 35'] ▶ LT	32 bytes frame
18	PUT ▶ R(ACK)₁ sent after FDT_{B,PCD,MIN} ▶ LT	Acknowledgment R-Block
19	PUT ↴ I(0)₁ ['36 37 ... 46 47' + '00' + '90 00'] ▶ LT	24 bytes last Block of chain
20	PUT ▶ I(0)₀ ['00 A4 04 00 47' + '01 02 03 ... 45 46 47' + '00'] ▶ LT	Loop-back
21	PUT ↴ I(1)₀ ['00 A4 04 00 87' + '01 02 03 ... 36 37 38'] ▶ LT	64 bytes frame
22	PUT ▶ R(ACK)₁ sent after FDT_{B,PCD,MIN} ▶ LT	Acknowledgment R-Block
23	PUT ↴ I(1)₁ ['39 3A 3B ... 73 74 75'] ▶ LT	64 bytes frame
24	PUT ▶ R(ACK)₀ sent after FDT_{B,PCD,MIN} ▶ LT	Acknowledgment R-Block
25	PUT ↴ I(0)₀ ['76 77 78 ... 85 86 87' + '00' + '90 00'] ▶ LT	24 bytes last Block of chain
26	PUT ▶ I(0)₁ ['00 A4 04 00 87' + '01 02 03 ... 85 86 87' + '00'] ▶ LT	Loop-back

Step	Exchanges	Comments
27	PUT \leftarrow I(1) ₁ ['00 A4 04 00 F7' + '01 02 03 ... 76 77 78']	\leftarrow LT 128 bytes frame
28	PUT \rightarrow R(ACK) ₀ sent after FDT _{B,PCD,MIN}	\rightarrow LT Acknowledgment R-Block
29	PUT \leftarrow I(1) ₀ ['79 7A 7B ... F3 F4 F5']	\leftarrow LT 128 bytes frame
30	PUT \rightarrow R(ACK) ₁ sent after FDT _{B,PCD,MIN}	\rightarrow LT Acknowledgment R-Block
31	PUT \leftarrow I(1) ₁ []	\leftarrow LT Empty I-Block indicating chaining
32	PUT \rightarrow R(ACK) ₀ sent after FDT _{B,PCD,MIN}	\rightarrow LT Acknowledgment R-Block
33	PUT \leftarrow I(0) ₀ ['F6 F7' + '00' + '90 00']	\leftarrow LT 8 bytes frame
34	PUT \rightarrow I(1) ₁ ['00 A4 04 00 F7' + '01 02 ... 46 F7' + '00']	\rightarrow LT Loop-back (256 bytes indicating chaining block)
35	PUT \leftarrow R(ACK) ₁	\leftarrow LT Acknowledgment R-Block
36	PUT \rightarrow I(0) ₀ []	\rightarrow LT Empty I-Block
37	PUT \leftarrow I(1) ₀ ['00 A4 04 00 F8' + '01 02 03 ... F6 F7 F8']	\leftarrow LT 256 bytes chained block
38	PUT \rightarrow R(ACK) ₁ sent after FDT _{B,PCD,MIN}	\rightarrow LT Acknowledgment R-Block
39	PUT \leftarrow I(0) ₁ ['00' + '90 00']	\leftarrow LT 6 bytes frame
40	PUT \rightarrow I(1) ₀ ['00 A4 04 00 F8' + '01 02 03 ... F6 F7 F8']	\rightarrow LT Loop-back (256 bytes chained block)
41	PUT \leftarrow R(ACK) ₀	\leftarrow LT Acknowledgment R-Block
42	PUT \rightarrow I(0) ₁ ['00']	\rightarrow LT Loop-back (4 bytes frame)
43	PUT \leftarrow I(0) ₁ ['EOT Command' + '90 00']	\leftarrow LT End Of Test command
44	PUT \leftarrow The PUT performs a PICC Reset (i.e. stops sending the carrier)	\leftarrow LT PICC Reset
45	PUT \rightarrow '05 00 08'	\rightarrow LT WUPB to poll for the PICC
46	PUT \rightarrow '05 00 08'	\rightarrow LT WUPB to poll for the PICC
47	PUT \rightarrow '05 00 08'	\rightarrow LT WUPB to poll for the PICC

**Scenario 97: Type B Error free chained I-Blocks in both directions for FSC = 256 bytes
(x=0 to 8, y=1)**

5.16.Type B Error free chained I-Blocks transmission for FSC = 16 to 128 bytes [TB203.xy]

Test codification:

TB203.xy

Test objective:

To ensure that the PCD accepts the values FSCI = '0' to '7' in the Byte 2 of the Protocol Info field of the ATQB and is able to send chained I-Blocks respecting the corresponding values of FSC.

References Requirements:

4.7.4.1, 4.7.4.3, 10.1.1.1, 10.1.1.3, 10.3.2.2, 10.3.4.5

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Run y=0, if the PCD does not send empty I-Block after chained blocks (See ICS).

Run y=1, if the PCD may send empty I-blocks after a chain of I-Blocks (See ICS).

Procedure:

Run the following scenarios.

In this test, the following Protocol Information (PI) shall be used:

	PI			Maximum Frame size for the PICC (FSC)
	Byte 1	Byte 2	Byte 3	
x=0	'80'	'21'	'41'	32 bytes
x=1	'80'	'31'	'41'	40 bytes
x=2	'80'	'41'	'41'	48 bytes
x=3	'80'	'51'	'41'	64 bytes
x=4	'80'	'61'	'41'	96 bytes
x=5	'80'	'71'	'41'	128 bytes
x=6	'80'	'01'	'41'	16 bytes
x=7	'80'	'11'	'41'	24 bytes

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenarios (the PUT uses chaining when sending an APDU too long to be transmitted within a frame of size FSC).

Failure action:

Proceed with the next test.

Scenarios:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + 'B1 9C 2F 6A' + '00 00 00 00' + PI with Byte 2 of PI = '21' ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + 'B1 9C 2F 6A' + '00 00 00 00' + PI with Byte 2 of PI = '21' ◀ LT	ATQB
6	PUT ▶ '1D' + 'B1 9C 2F 6A' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' ◀ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(0)₀ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00'] ◀ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 3B' + '01 02 ... 18'] ▶ LT	32 bytes frame
11	PUT ◀ R(ACK)₁ ◀ LT	Acknowledgment R-Block
12	PUT ▶ I(1)₀ ['19 1A 1B ... 33 34 35'] ▶ LT	32 bytes frame
13	PUT ◀ R(ACK)₀ ◀ LT	Acknowledgment R-Block
14	PUT ▶ I(0)₁ ['36 37 38 39 3A 3B' + '00'] ▶ LT	10 bytes frame
15	PUT ◀ I(0)₁ ['00 A4 04 00 34' + '01 02 ... 34' + '00' + '90 00'] ◀ LT	
16	PUT ▶ I(1)₀ ['00 A4 04 00 34' + '01 02 ... 18'] ▶ LT	32 bytes frame
17	PUT ◀ R(ACK)₀ ◀ LT	Acknowledgment R-Block
18	PUT ▶ I(0)₁ ['19 1A 1B ... 33 34' + '00'] ▶ LT	32 bytes frame
19	PUT ◀ I(0)₁ ["EOT Command" + '90 00'] ◀ LT	End Of Test command
20	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
21	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
22	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 98: Type B Error free chained I-Blocks transmission (FSC = 32 bytes; x=0, y=0)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + 'B1 9C 2F 6A' + '00 00 00 00' + PI with Byte 2 of PI = '21' ↴ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + 'B1 9C 2F 6A' + '00 00 00 00' + PI with Byte 2 of PI = '21' ↴ LT	ATQB
6	PUT ▶ '1D' + 'B1 9C 2F 6A' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ↴ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00'] ↴ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 3B' + '01 02 ... 18'] ▶ LT	32 bytes frame
11	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
12	PUT ▶ I(1)₀ ['19 1A 1B ... 33 34 35'] ▶ LT	32 bytes frame
13	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
14	PUT ▶ I(0)₁ ['36 37 38 39 3A 3B' + '00'] ▶ LT	10 bytes frame
15	PUT ↴ I(0)₁ ['00 A4 04 00 34' + '01 02 ... 34' + '00' + '90 00'] ↴ LT	
16	PUT ▶ I(1)₀ ['00 A4 04 00 34' + '01 02 ... 18'] ▶ LT	32 bytes frame
17	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
18	PUT ▶ I(1)₁ ['19 1A 1B ... 33 34' + '00'] ▶ LT	32 bytes frame
19	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
20	PUT ▶ I(0)₀ [] ▶ LT	Empty I-Block
21	PUT ↴ I(0)₀ ["EOT Command" + '90 00'] ↴ LT	End Of Test command
22	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
24	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
25	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 99: Type B Error free chained I-Blocks transmission (FSC = 32 bytes; x=0, y=1)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + 'C2 AD 31 7B' + '00 00 00 00' + PI with Byte 2 of PI = '31' ↴ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + 'C2 AD 31 7B' + '00 00 00 00' + PI with Byte 2 of PI = '31' ↴ LT	ATQB
6	PUT ▶ '1D' + 'C2 AD 31 7B' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ↴ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 A4 04 00 50' + '01 02 ... 50' + '00' + '90 00'] ↴ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 50' + '01 02 ... 19 20'] ▶ LT	40 bytes frame
11	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
12	PUT ▶ I(1)₀ ['21 22 23 ... 43 44 45'] ▶ LT	40 bytes frame
13	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
14	PUT ▶ I(0)₁ ['46 47 ... 4F 50' + '00'] ▶ LT	15 bytes frame
15	PUT ↴ I(0)₁ ['00 A4 04 00 44' + '01 02 ... 44' + '00' + '90 00'] ↴ LT	
16	PUT ▶ I(1)₀ ['00 A4 04 00 44' + '01 02 ... 19 20'] ▶ LT	40 bytes frame
17	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
18	PUT ▶ I(0)₁ ['21 22 23 ... 43 44' + '00'] ▶ LT	40 bytes frame
19	PUT ↴ I(0)₁ ["EOT Command" + '90 00'] ↴ LT	End Of Test command
20	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
21	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
22	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 100: Type B Error free chained I-Blocks transmission (FSC = 40 bytes, x=1, y=0)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + 'C2 AD 31 7B' + '00 00 00 00' + PI with Byte 2 of PI = '31' ▶ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + 'C2 AD 31 7B' + '00 00 00 00' + PI with Byte 2 of PI = '31' ▶ LT	ATQB
6	PUT ▶ '1D' + 'C2 AD 31 7B' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ▶ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 A4 04 00 50' + '01 02 ... 50' + '00' + '90 00'] ▶ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 50' + '01 02 ... 19 20'] ▶ LT	40 bytes frame
11	PUT ↴ R(ACK)₁ ▶ LT	Acknowledgment R-Block
12	PUT ▶ I(1)₀ ['21 22 23 ... 43 44 45'] ▶ LT	40 bytes frame
13	PUT ↴ R(ACK)₀ ▶ LT	Acknowledgment R-Block
14	PUT ▶ I(0)₁ ['46 47 ... 4F 50' + '00'] ▶ LT	15 bytes frame
15	PUT ↴ I(0)₁ ['00 A4 04 00 44' + '01 02 ... 44' + '00' + '90 00'] ▶ LT	
16	PUT ▶ I(1)₀ ['00 A4 04 00 44' + '01 02 ... 19 20'] ▶ LT	40 bytes frame
17	PUT ↴ R(ACK)₀ ▶ LT	Acknowledgment R-Block
18	PUT ▶ I(1)₁ ['21 22 23 ... 43 44' + '00'] ▶ LT	40 bytes frame
19	PUT ↴ R(ACK)₁ ▶ LT	Acknowledgment R-Block
20	PUT ▶ I(0)₀ [] ▶ LT	Empty I-Block
21	PUT ↴ I(0)₀ ["EOT Command" + '90 00'] ▶ LT	End Of Test command
22	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) ▶ LT	PICC Reset
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
24	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
25	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 101: Type B Error free chained I-Blocks transmission (FSC = 40 bytes, x=1, y=1)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + 'D3 BE 42 8C' + '00 00 00 00' + PI with Byte 2 of PI = '41' ↴ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + 'D3 BE 42 8C' + '00 00 00 00' + PI with Byte 2 of PI = '41' ↴ LT	ATQB
6	PUT ▶ '1D' + 'D3 BE 42 8C' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ↴ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 A4 04 00 60' + '01 02 ... 60' + '00' + '90 00'] ↴ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 60' + '01 02 ... 27 28'] ▶ LT	48 bytes frame
11	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
12	PUT ▶ I(1)₀ ['29 2A 2B ... 53 54 55'] ▶ LT	48 bytes frame
13	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
14	PUT ▶ I(0)₁ ['56 57 ... 5F 60' + '00'] ▶ LT	15 bytes frame
15	PUT ↴ I(0)₁ ['00 A4 04 00 54' + '01 02 ... 54' + '00' + '90 00'] ↴ LT	
16	PUT ▶ I(1)₀ ['00 A4 04 00 54' + '01 02 ... 27 28'] ▶ LT	48 bytes frame
17	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
18	PUT ▶ I(0)₁ ['29 2A 2B ... 53 54' + '00'] ▶ LT	48 bytes frame
19	PUT ↴ I(0)₁ ["EOT Command" + '90 00'] ↴ LT	End Of Test command
20	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
21	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
22	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 102: Type B Error free chained I-Blocks transmission (FSC = 48 bytes, x=2, y=0)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + 'D3 BE 42 8C' + '00 00 00 00' + PI with Byte 2 of PI = '41' ↴ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + 'D3 BE 42 8C' + '00 00 00 00' + PI with Byte 2 of PI = '41' ↴ LT	ATQB
6	PUT ▶ '1D' + 'D3 BE 42 8C' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ↴ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 A4 04 00 60' + '01 02 ... 60' + '00' + '90 00'] ↴ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 60' + '01 02 ... 27 28'] ▶ LT	48 bytes frame
11	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
12	PUT ▶ I(1)₀ ['29 2A 2B ... 53 54 55'] ▶ LT	48 bytes frame
13	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
14	PUT ▶ I(0)₁ ['56 57 ... 5F 60' + '00'] ▶ LT	15 bytes frame
15	PUT ↴ I(0)₁ ['00 A4 04 00 54' + '01 02 ... 54' + '00' + '90 00'] ↴ LT	
16	PUT ▶ I(1)₀ ['00 A4 04 00 54' + '01 02 ... 27 28'] ▶ LT	48 bytes frame
17	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
18	PUT ▶ I(1)₁ ['29 2A 2B ... 53 54' + '00'] ▶ LT	48 bytes frame
19	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
20	PUT ▶ I(0)₀ [] ▶ LT	Empty I-Block
21	PUT ↴ I(0)₀ ["EOT Command" + '90 00'] ↴ LT	End Of Test command
22	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
24	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
25	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 103: Type B Error free chained I-Blocks transmission (FSC = 48 bytes, x=2, y=1)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + 'E4 CF 53 9D' + '00 00 00 00' + PI with Byte 2 of PI = '51' ↴ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + 'E4 CF 53 9D' + '00 00 00 00' + PI with Byte 2 of PI = '51' ↴ LT	ATQB
6	PUT ▶ '1D' + 'E4 CF 53 9D' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ↴ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 A4 04 00 7F' + '01 02 ... 7F' + '00' + '90 00'] ↴ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 7F' + '01 02 ... 37 38'] ▶ LT	64 bytes frame
11	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
12	PUT ▶ I(1)₀ ['39 3A 3B ... 73 74 75'] ▶ LT	64 bytes frame
13	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
14	PUT ▶ I(0)₁ ['76 77 ... 7E 7F' + '00'] ▶ LT	14 bytes frame
15	PUT ↴ I(0)₁ ['00 A4 04 00 74' + '01 02 ... 74' + '00' + '90 00'] ↴ LT	
16	PUT ▶ I(1)₀ ['00 A4 04 00 74' + '01 02 ... 37 38'] ▶ LT	64 bytes frame
17	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
18	PUT ▶ I(0)₁ ['39 3A 3B ... 73 74' + '00'] ▶ LT	64 bytes frame
19	PUT ↴ I(0)₁ ["EOT Command" + '90 00'] ↴ LT	End Of Test command
20	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
21	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
22	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 104: Type B Error free chained I-Blocks transmission (FSC = 64 bytes, x=3, y=0)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + 'E4 CF 53 9D' + '00 00 00 00' + PI with Byte 2 of PI = '51' ↴ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + 'E4 CF 53 9D' + '00 00 00 00' + PI with Byte 2 of PI = '51' ↴ LT	ATQB
6	PUT ▶ '1D' + 'E4 CF 53 9D' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ↴ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 A4 04 00 7F' + '01 02 ... 7F' + '00' + '90 00'] ↴ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 7F' + '01 02 ... 37 38'] ▶ LT	64 bytes frame
11	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
12	PUT ▶ I(1)₀ ['39 3A 3B ... 73 74 75'] ▶ LT	64 bytes frame
13	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
14	PUT ▶ I(0)₁ ['76 77 ... 7E 7F' + '00'] ▶ LT	14 bytes frame
15	PUT ↴ I(0)₁ ['00 A4 04 00 74' + '01 02 ... 74' + '00' + '90 00'] ↴ LT	
16	PUT ▶ I(1)₀ ['00 A4 04 00 74' + '01 02 ... 37 38'] ▶ LT	64 bytes frame
17	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
18	PUT ▶ I(1)₁ ['39 3A 3B ... 73 74' + '00'] ▶ LT	64 bytes frame
19	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
20	PUT ▶ I(0)₀ [] ▶ LT	Empty I-Block
21	PUT ↴ I(0)₀ ["EOT Command" + '90 00'] ↴ LT	End Of Test command
22	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
24	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
25	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 105: Type B Error free chained I-Blocks transmission (FSC = 64 bytes, x=3, y=1)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + 'F5 D1 64 AE' + '00 00 00 00' + PI with Byte 2 of PI = '61' ↴ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + 'F5 D1 64 AE' + '00 00 00 00' + PI with Byte 2 of PI = '61' ↴ LT	ATQB
6	PUT ▶ '1D' + 'F5 D1 64 AE' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ↴ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 A4 04 00 BF' + '01 02 ... BF' + '00' + '90 00'] ↴ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 BF' + '01 02 ... 57 58'] ▶ LT	96 bytes frame
11	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
12	PUT ▶ I(1)₀ ['59 5A 5B ... B3 B4 B5'] ▶ LT	96 bytes frame
13	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
14	PUT ▶ I(0)₁ ['B6 B7 ... BE BF' + '00'] ▶ LT	14 bytes frame
15	PUT ↴ I(0)₁ ['00 A4 04 00 B4' + '01 02 ... B4' + '00' + '90 00'] ↴ LT	
16	PUT ▶ I(1)₀ ['00 A4 04 00 B4' + '01 02 ... 57 58'] ▶ LT	96 bytes frame
17	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
18	PUT ▶ I(0)₁ ['59 5A 5B ... B3 B4' + '00'] ▶ LT	96 bytes frame
19	PUT ↴ I(0)₁ ["EOT Command" + '90 00'] ↴ LT	End Of Test command
20	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
21	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
22	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 106: Type B Error free chained I-Blocks transmission (FSC = 96 bytes, x=4, y=0)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + 'F5 D1 64 AE' + '00 00 00 00' + PI with Byte 2 of PI = '61' ↴ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + 'F5 D1 64 AE' + '00 00 00 00' + PI with Byte 2 of PI = '61' ↴ LT	ATQB
6	PUT ▶ '1D' + 'F5 D1 64 AE' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ↴ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 A4 04 00 BF' + '01 02 ... BF' + '00' + '90 00'] ↴ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 BF' + '01 02 ... 57 58'] ▶ LT	96 bytes frame
11	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
12	PUT ▶ I(1)₀ ['59 5A 5B ... B3 B4 B5'] ▶ LT	96 bytes frame
13	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
14	PUT ▶ I(0)₁ ['B6 B7 ... BE BF' + '00'] ▶ LT	14 bytes frame
15	PUT ↴ I(0)₁ ['00 A4 04 00 B4' + '01 02 ... B4' + '00' + '90 00'] ↴ LT	
16	PUT ▶ I(1)₀ ['00 A4 04 00 B4' + '01 02 ... 57 58'] ▶ LT	96 bytes frame
17	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
18	PUT ▶ I(1)₁ ['59 5A 5B ... B3 B4' + '00'] ▶ LT	96 bytes frame
19	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
20	PUT ▶ I(0)₀ [] ▶ LT	Empty I-Block
21	PUT ↴ I(0)₀ ["EOT Command" + '90 00'] ↴ LT	End Of Test command
22	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
24	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
25	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 107: Type B Error free chained I-Blocks transmission (FSC = 96 bytes, x=4, y=1)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + '16 E2 75 BF' + '00 00 00 00' + PI with Byte 2 of PI = '71' ↴ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + '16 E2 75 BF' + '00 00 00 00' + PI with Byte 2 of PI = '71' ↴ LT	ATQB
6	PUT ▶ '1D' + '16 E2 75 BF' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ↴ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 A4 04 00 F5' + '01 02 ... F5' + '00' + '90 00'] ↴ LT	256 bytes non-chained block
10	PUT ▶ I(1)₁ ['00 A4 04 00 F5' + '01 02 ... 77 78'] ▶ LT	128 bytes frame
11	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
12	PUT ▶ I(1)₀ ['79 7A 7B ... F3 F4 F5'] ▶ LT	128 bytes frame
13	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
14	PUT ▶ I(0)₁ ['00'] ▶ LT	4 bytes frame
15	PUT ↴ I(0)₁ ['00 A4 04 00 F4' + '01 02 ... F4' + '00' + '90 00'] ↴ LT	
16	PUT ▶ I(1)₀ ['00 A4 04 00 F4' + '01 02 ... 77 78'] ▶ LT	128 bytes frame
17	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
18	PUT ▶ I(0)₁ ['79 7A 7B ... F3 F4' + '00'] ▶ LT	128 bytes frame
19	PUT ↴ I(0)₁ ["EOT Command" + '90 00'] ↴ LT	End Of Test command
20	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
21	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
22	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 108: Type B Error free chained I-Blocks transmission (FSC = 128; x=5, y=0)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + '16 E2 75 BF' + '00 00 00 00' + PI with Byte 2 of PI = '71' ↴ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + '16 E2 75 BF' + '00 00 00 00' + PI with Byte 2 of PI = '71' ↴ LT	ATQB
6	PUT ▶ '1D' + '16 E2 75 BF' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ↴ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 A4 04 00 F5' + '01 02 ... F5' + '00' + '90 00'] ↴ LT	256 bytes non-chained block
10	PUT ▶ I(1)₁ ['00 A4 04 00 F5' + '01 02 ... 77 78'] ▶ LT	128 bytes frame
11	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
12	PUT ▶ I(1)₀ ['79 7A 7B ... F3 F4 F5'] ▶ LT	128 bytes frame
13	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
14	PUT ▶ I(0)₁ ['00'] ▶ LT	4 bytes frame
15	PUT ↴ I(0)₁ ['00 A4 04 00 F4' + '01 02 ... F4' + '00' + '90 00'] ↴ LT	
16	PUT ▶ I(1)₀ ['00 A4 04 00 F4' + '01 02 ... 77 78'] ▶ LT	128 bytes frame
17	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
18	PUT ▶ I(1)₁ ['79 7A 7B ... F3 F4' + '00'] ▶ LT	128 bytes frame
19	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
20	PUT ▶ I(0)₀ [] ▶ LT	Empty I-Block
21	PUT ↴ I(0)₀ ["EOT Command" + '90 00'] ↴ LT	End Of Test command
22	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
24	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
25	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 109: Type B Error free chained I-Blocks transmission (FSC = 128; x=5, y=1)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + '7A 53 66 EE' + '00 00 00 00' + PI with Byte 2 of PI = '01' ↴ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + '7A 53 66 EE' + '00 00 00 00' + PI with Byte 2 of PI = '01' ↴ LT	ATQB
6	PUT ▶ '1D' + '7A 53 66 EE' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ↴ LT	ATTRIB Response
8	PUT ▶ I(1)₀ ['00 A4 04 00 0E' + "2PAY.SYS"] ▶ LT	Select PPSE (16 bytes frames)
9	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
10	PUT ▶ I(0)₁ [".DDF01" + '00'] ▶ LT	Select PPSE (10 bytes frames)
11	PUT ↴ I(0)₁ ['00 A4 04 00 1C' + '01 02 ... 1C' + '00' + '90 00'] ↴ LT	
12	PUT ▶ I(1)₀ ['00 A4 04 00 1C' + '01 02 ... 08'] ▶ LT	16 bytes frame
13	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
14	PUT ▶ I(1)₁ ['09 0A 0B ... 13 14 15'] ▶ LT	16 bytes frame
15	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
16	PUT ▶ I(0)₀ ['16 17 18 19 1A 1B 1C' + '00'] ▶ LT	11 bytes frame
17	PUT ↴ I(0)₀ ['00 A4 04 00 14' + '01 02 ... 14' + '00' + '90 00'] ↴ LT	
18	PUT ▶ I(1)₁ ['00 A4 04 00 14' + '01 02 ... 08'] ▶ LT	16 bytes frame
19	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
20	PUT ▶ I(0)₀ ['09 0A 0B ... 13 14' + '00'] ▶ LT	16 bytes frame
21	PUT ↴ I(0)₀ ["EOT Command" + '90 00'] ↴ LT	End Of Test command
22	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
24	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
25	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 110: Type B Error free chained I-Blocks transmission (FSC = 16; x=6, y=0)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + '7A 53 66 EE' + '00 00 00 00' + PI with Byte 2 of PI = '01' ▲ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + '7A 53 66 EE' + '00 00 00 00' + PI with Byte 2 of PI = '01' ▲ LT	ATQB
6	PUT ▶ '1D' + '7A 53 66 EE' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ▲ LT	ATTRIB Response
8	PUT ▶ I(1)₀ ['00 A4 04 00 0E' + "2PAY.SYS"] ▶ LT	Select PPSE (16 bytes frames)
9	PUT ↴ R(ACK)₀ ▲ LT	Acknowledgment R-Block
10	PUT ▶ I(0)₁ [".DDF01" + '00'] ▶ LT	Select PPSE (10 bytes frames)
11	PUT ↴ I(0)₁ ['00 A4 04 00 1C' + '01 02 ... 1C' + '00' + '90 00'] ▲ LT	
12	PUT ▶ I(1)₀ ['00 A4 04 00 1C' + '01 02 ... 08'] ▶ LT	16 bytes frame
13	PUT ↴ R(ACK)₀ ▲ LT	Acknowledgment R-Block
14	PUT ▶ I(1)₁ ['09 0A 0B ... 13 14 15'] ▶ LT	16 bytes frame
15	PUT ↴ R(ACK)₁ ▲ LT	Acknowledgment R-Block
16	PUT ▶ I(0)₀ ['16 17 18 19 1A 1B 1C' + '00'] ▶ LT	11 bytes frame
17	PUT ↴ I(0)₀ ['00 A4 04 00 14' + '01 02 ... 14' + '00' + '90 00'] ▲ LT	
18	PUT ▶ I(1)₁ ['00 A4 04 00 14' + '01 02 ... 08'] ▶ LT	16 bytes frame
19	PUT ↴ R(ACK)₁ ▲ LT	Acknowledgment R-Block
20	PUT ▶ I(1)₀ ['09 0A 0B ... 13 14' + '00'] ▶ LT	16 bytes frame
21	PUT ↴ R(ACK)₀ ▲ LT	Acknowledgment R-Block
22	PUT ▶ I(0)₁ [] ▶ LT	Empty I-Block
23	PUT ↴ I(0)₁ ["EOT Command" + '90 00'] ▲ LT	End Of Test command
24	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) □ LT	PICC Reset
25	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Step	Exchanges	Comments
26	PUT ▶ '05 00 08'	▶ LT WUPB to poll for the PICC
27	PUT ▶ '05 00 08'	▶ LT WUPB to poll for the PICC

Scenario 111: Type B Error free chained I-Blocks transmission (FSC = 16; x=6, y=1)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + 'EE 19 A4 4A' + '00 00 00 00' + PI with Byte 2 of PI = '11' ↴ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + 'EE 19 A4 4A' + '00 00 00 00' + PI with Byte 2 of PI = '11' ↴ LT	ATQB
6	PUT ▶ '1D' + 'EE 19 A4 4A' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ↴ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 A4 04 00 2B' + '01 02 ... 2B' + '00' + '90 00'] ↴ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 2B' + '01 02 ... 0F 10'] ▶ LT	24 bytes frame
11	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
12	PUT ▶ I(1)₀ ['11 12 13 ... 23 24 25'] ▶ LT	24 bytes frame
13	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
14	PUT ▶ I(0)₁ ['26 27 28 29 2A 2B' + '00'] ▶ LT	10 bytes frame
15	PUT ↴ I(0)₁ ['00 A4 04 00 24' + '01 02 ... 24' + '00' + '90 00'] ↴ LT	
16	PUT ▶ I(1)₀ ['00 A4 04 00 24' + '01 02 ... 0F 10'] ▶ LT	24 bytes frame
17	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
18	PUT ▶ I(0)₁ ['11 12 13 ... 23 24' + '00'] ▶ LT	24 bytes frame
19	PUT ↴ I(0)₁ ["EOT Command" + '90 00'] ↴ LT	End Of Test command
20	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
21	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
22	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 112: Type B Error free chained I-Blocks transmission (FSC = 24; x=7, y=0)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + 'EE 19 A4 4A' + '00 00 00 00' + PI with Byte 2 of PI = '11' ↴ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + 'EE 19 A4 4A' + '00 00 00 00' + PI with Byte 2 of PI = '11' ↴ LT	ATQB
6	PUT ▶ '1D' + 'EE 19 A4 4A' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ↴ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 A4 04 00 2B' + '01 02 ... 2B' + '00' + '90 00'] ↴ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 2B' + '01 02 ... 0F 10'] ▶ LT	24 bytes frame
11	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
12	PUT ▶ I(1)₀ ['11 12 13 ... 23 24 25'] ▶ LT	24 bytes frame
13	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
14	PUT ▶ I(0)₁ ['26 27 28 29 2A 2B' + '00'] ▶ LT	10 bytes frame
15	PUT ↴ I(0)₁ ['00 A4 04 00 24' + '01 02 ... 24' + '00' + '90 00'] ↴ LT	
16	PUT ▶ I(1)₀ ['00 A4 04 00 24' + '01 02 ... 0F 10'] ▶ LT	24 bytes frame
17	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
18	PUT ▶ I(1)₁ ['11 12 13 ... 23 24' + '00'] ▶ LT	24 bytes frame
19	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
20	PUT ▶ I(0)₀ [] ▶ LT	Empty I-Block
21	PUT ↴ I(0)₀ ["EOT Command" + '90 00'] ↴ LT	End Of Test command
22	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
24	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
25	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 113: Type B Error free chained I-Blocks transmission (FSC = 24; x=7, y=1)

5.17.Type B Error free request for Frame Waiting Time Extension on non-chained I-Blocks [TB204]

Test codification:

TB204

Test objective:

To ensure that the PCD correctly manages a request for Frame Waiting Time Extension received in response to an I-Block not indicating chaining.

References Requirements:

10.2.2.1, 10.2.2.3, 10.2.2.5, 10.2.2.7, 10.3.4.2, 10.1.2.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

After each S(WTX) Response block, the LT replies using the Frame Delay Time $FDT_{B,PICC,EXT}$ between the end of the S(WTX) Response sequence sent by the PUT and the beginning of the sequence containing the next block sent by the LT, with:

- $FDT_{B,PICC,EXT} = FWT_{TEMP} + \Delta FWT = [(FWT \times WTXM) + \Delta FWT] = [(4096 \times WTXM) + 49152] \times 1/f_c$ if $WTXM \leq 59$, as $FWT = 4096 \times 1/f_c$ and $\Delta FWT = 49152 \times 1/f_c$

When the sequences sent by the LT are followed by a sequence sent by the PUT containing S(WTX) Responses, the LT measures the delay between the end of the sequence sent by the LT and the beginning of the sequence replied by the PUT.

In this test, the default Protocol Information (PI) shall be used:

PI			FWT+ΔFWT
Byte 1	Byte 2	Byte 3	
'80'	'21'	'01'	53248x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (each time the LT sends a S(WTX) Request, the PUT correctly grants the Frame Waiting Time Extension).

On reception of an S(WTX) Block, the PUT replies with an S(WTX) Block having a PCB field (i.e. first byte of the Block) equal to ('F2')_h (i.e. b₂ of S-Block PCB is set to (1)_b).

The delay between the end of a sequence sent by the LT and the beginning of the sequence replied by the PUT containing a S(WTX) Response is at least FDT_{B,PCD,MIN}.

The delay between the end of a sequence sent by the LT and the beginning of the sequence replied by the PUT is at least FDT_{B,PCD,MIN} during installation and block protocol.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + 'F5 D1 64 AE' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + 'F5 D1 64 AE' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + 'F5 D1 64 AE' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' ◀ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(0)₀ ['00 B2 01 04 00' + '90 00'] ◀ LT	
10	PUT ▶ I(0)₁ ['00 B2 01 04 00'] ▶ LT	Loop-back
11	PUT ◀ S(WTX Request) [WTXM='03'] ◀ LT	WTXM = 3
12	PUT ▶ S(WTX Response) [WTXM='03'] sent after FDT_{B,PCD,MIN} ▶ LT	WTX acknowledgment
13	PUT ◀ I(0)₁ ['00 A4 04 00 05+ '01 02 ... 05' + '00' + '90 00'] sent using FDT _{B,PICC,EXT} with WTXM = 3 ◀ LT	
14	PUT ▶ I(0)₀ ['00 A4 04 00 05' + '01 02 ... 05' + '00'] ▶ LT	Loop-back (14 bytes frame)
15	PUT ◀ I(0)₀ ['00 A4 04 00 05' + '06 07 ... 0A' + '00' + '90 00'] ◀ LT	
16	PUT ▶ I(0)₁ ['00 A4 04 00 05' + '06 07 ... 0A' + '00'] ▶ LT	Loop-back (14 bytes frame)
17	PUT ◀ S(WTX Request) [WTXM='23'] ◀ LT	WTXM = 35
18	PUT ▶ S(WTX Response) [WTXM='23'] sent after FDT_{A,PCD,MIN} ▶ LT	WTX acknowledgment
19	PUT ◀ S(WTX Request) [WTXM='23'] ◀ LT	WTXM = 35

Step	Exchanges	Comments
20	PUT ▶ S(WTX Response) [WTXM='23'] sent after FDT_{A,PCD,MIN} ▶ LT	WTX acknowledgment
21	PUT ◀ S(WTX Request) [WTXM='23'] ◀ LT	WTXM = 35
22	PUT ▶ S(WTX Response) [WTXM='23'] sent after FDT_{A,PCD,MIN} ▶ LT	WTX acknowledgment
23	PUT ◀ S(WTX Request) [WTXM='23'] ◀ LT	WTXM = 35
24	PUT ▶ S(WTX Response) [WTXM='23'] sent after FDT_{A,PCD,MIN} ▶ LT	WTX acknowledgment
25	PUT ◀ S(WTX Request) [WTXM='23'] ◀ LT	WTXM = 35
26	PUT ▶ S(WTX Response) [WTXM='23'] sent after FDT_{A,PCD,MIN} ▶ LT	WTX acknowledgment
27	PUT ◀ S(WTX Request) [WTXM='23'] ◀ LT	WTXM = 35
28	PUT ▶ S(WTX Response) [WTXM='23'] sent after FDT_{A,PCD,MIN} ▶ LT	WTX acknowledgment
29	PUT ◀ S(WTX Request) [WTXM='23'] ◀ LT	WTXM = 35
30	PUT ▶ S(WTX Response) [WTXM='23'] sent after FDT_{B,PCD,MIN} ▶ LT	WTX acknowledgment
31	PUT ◀ I(0)₁ ['00 A4 04 00 05+ '0B 0C ... 0F' + '00' + '90 00'] sent using FDT _{B,PICC,EXT} with WTXM = 35 ◀ LT	
32	PUT ▶ I(0)₀ ['00 A4 04 00 05+ '0B 0C ... 0F' + '00'] ▶ LT	Loop-back (14 bytes frame)
33	PUT ◀ I(0)₀ ['00 A4 04 00 05' + '11 12 ... 15' + '00' + '90 00'] ◀ LT	
34	PUT ▶ I(0)₁ ['00 A4 04 00 05' + '11 12 ... 15' + '00'] ▶ LT	Loop-back (14 bytes frame)
35	PUT ◀ S(WTX Request) [WTXM='38'] ◀ LT	WTXM = 56
36	PUT ▶ S(WTX Response) [WTXM='38'] sent after FDT_{B,PCD,MIN} ▶ LT	WTX acknowledgment
37	PUT ◀ I(0)₁ ['00 A4 04 00 05+ '16 17 ... 1A' + '00' + '90 00'] sent using FDT _{B,PICC,EXT} with WTXM = 56 ◀ LT	
38	PUT ▶ I(0)₀ ['00 A4 04 00 05+ '16 17 ... 1A' + '00'] ▶ LT	Loop-back (14 bytes frame)
39	PUT ◀ I(0)₀ ['00 A4 04 00 05' + '1B 1C ... 1F' + '00' + '90 00'] ◀ LT	
40	PUT ▶ I(0)₁ ['00 A4 04 00 05' + '1B 1C ... 1F' + '00'] ▶ LT	Loop-back (14 bytes frame)
41	PUT ◀ S(WTX Request) [WTXM='12'] ◀ LT	WTXM = 18
42	PUT ▶ S(WTX Response) [WTXM='12'] sent after FDT_{B,PCD,MIN} ▶ LT	WTX acknowledgment
43	PUT ◀ I(0)₁ ['00 A4 04 00 05+ '20 21 ... 24' + '00' + '90 00'] sent using FDT _{B,PICC,EXT} with WTXM = 18 ◀ LT	

Step	Exchanges	Comments
44	PUT ▶ I(0)₀ [‘00 A4 04 00 05+ ‘20 21 ... 24’ + ‘00’] ▶ LT	Loop-back (14 bytes frame)
45	PUT ◀ I(0)₀ [‘00 A4 04 00 05’ + ‘25 26 ... 29’ + ‘00’ + ‘90 00’] ◀ LT	
46	PUT ▶ I(0)₁ [‘00 A4 04 00 05’ + ‘25 26 ... 29’ + ‘00’] ▶ LT	Loop-back (14 bytes frame)
47	PUT ◀ I(0)₁ [“EOT Command” + ‘90 00’] ◀ LT	End Of Test command
48	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
49	PUT ▶ ‘05 00 08’ ▶ LT	WUPB to poll for the PICC
50	PUT ▶ ‘05 00 08’ ▶ LT	WUPB to poll for the PICC
51	PUT ▶ ‘05 00 08’ ▶ LT	WUPB to poll for the PICC

Scenario 114: Type B Error free request for Frame Waiting Time Extension on non-chained I-Blocks

5.18.Type B Error free request for Frame Waiting Time Extension during chaining in both directions [TB205]

Test codification:

TB205

Test objective:

To ensure that the PCD correctly manages a request for Frame Waiting Time Extension received in response to an R(ACK) Block or to an I-Block indicating chaining.

References Requirements:

10.2.2.1, 10.2.2.3, 10.2.2.5, 10.2.2.7, 10.3.4.2, 10.1.2.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

After each S(WTX) Response block, the LT replies using the Frame Delay Time $FDT_{B,PICC,EXT}$ between the end of the S(WTX) Response sequence sent by the PUT and the beginning of the sequence containing the next block sent by the LT, with:

- $FDT_{B,PICC,EXT} = [(4096 \times WTXM) + 49152] \times 1/f_c$
 - as FWT = $4096 \times 1/f_c$ and $\Delta FWT = 49152 \times 1/f_c$

In this test, the default Protocol Information (PI) shall be used:

PI			FWT+ΔFWT
Byte 1	Byte 2	Byte 3	
'80'	'21'	'01'	$53248 \times 1/f_c$

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (each time the LT sends a S(WTX) Request, the PUT correctly grants the Frame Waiting Time Extension).

On reception of an S(WTX) Block, the PUT replies with an S(WTX) Block having a PCB field (i.e. first byte of the Block) equal to ('F2')_h (i.e. b₂ of S-Block PCB is set to (1)_b).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + '1C 8F 5F 3D' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + '1C 8F 5F 3D' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + '1C 8F 5F 3D' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' ◀ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(1)₀ ['00 A4 04 00 39' + '91 92 93 ... 96 97 98'] ◀ LT	
10	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgment R-Block
11	PUT ◀ S(WTX Request) [WTXM='04'] ◀ LT	WTXM = 4
12	PUT ▶ S(WTX Response) [WTXM='04'] ▶ LT	WTX acknowledgment
13	PUT ◀ I(1)₁ ['99 9A 9B ... A3 A4 A5'] sent using FDT_{B,PICC,EXT} with WTXM = 4 ◀ LT	
14	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgment R-Block
15	PUT ◀ S(WTX Request) [WTXM='10'] ◀ LT	WTXM = 16
16	PUT ▶ S(WTX Response) [WTXM='10'] ▶ LT	WTX acknowledgment
17	PUT ◀ I(1)₀ ['A6 A7 A8 ... B0 B1 B2'] sent using FDT_{B,PICC,EXT} with WTXM = 16 ◀ LT	
18	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgment R-Block
19	PUT ◀ S(WTX Request) [WTXM='20'] ◀ LT	WTXM = 32
20	PUT ▶ S(WTX Response) [WTXM='20'] ▶ LT	WTX acknowledgment
21	PUT ◀ I(1)₁ ['B3 B4 B5 ... BD BE BF'] sent using FDT_{B,PICC,EXT} with WTXM = 32 ◀ LT	
22	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgment R-Block
23	PUT ◀ S(WTX Request) [WTXM='2E'] ◀ LT	WTXM = 46
24	PUT ▶ S(WTX Response) [WTXM='2E'] ▶ LT	WTX acknowledgment t
25	PUT ◀ I(0)₀ ['C0 C1 C2 ... C7 C8 C9' + '00' + '90 00'] sent using FDT_{B,PICC,EXT} with WTXM = 46 ◀ LT	
26	PUT ▶ I(1)₁ ['00 A4 04 00 39' + '91 92 ... A7 A8'] ▶ LT	Loop-back (32 bytes frame)
27	PUT ◀ S(WTX Request) [WTXM='06'] ◀ LT	WTXM = 6

Step	Exchanges	Comments
28	PUT ▶ S(WTX Response) [WTXM='06'] ▶ LT	WTX acknowledgment
29	PUT ◀ R(ACK)₁ sent using FDT _{B,PICC,EXT} with WTXM = 6 ▶ LT	
30	PUT ▶ I(1)₀ ['A9 AA AB ... C3 C4 C5'] ▶ LT	Loop-back (32 bytes frame)
31	PUT ◀ S(WTX Request) [WTXM='31'] ▶ LT	WTXM = 49
32	PUT ▶ S(WTX Response) [WTXM='31'] ▶ LT	WTX acknowledgment
33	PUT ◀ R(ACK)₀ sent using FDT _{B,PICC,EXT} with WTXM = 49 ▶ LT	
34	PUT ▶ I(0)₁ ['C6 C7 C8 C9' + '00'] ▶ LT	Loop-back (8 bytes frame)
35	PUT ◀ I(0)₁ ['EOT Command' + '90 00'] ▶ LT	End Of Test command
36	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) □ LT	PICC Reset
37	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
38	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
39	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 115: Type B Error free request for Frame Waiting Time Extension during chaining in both directions

5.19.Type B Error free chained I-Blocks reception with rare frame sizes [TB210]

Test codification:

TB210

Test objective:

To ensure that the PCD is able to correctly receive chained I-Blocks of rare sizes (i.e. block sizes different from the ISO 14443 values of FSD and not constant within a single chain).

References Requirements:

10.1.1.3, 10.3.2.1

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

In this test, the default Protocol Information (PI) shall be used:

PI			Maximum Frame Size for the PICC (FSC)
Byte 1	Byte 2	Byte 3	
'80'	'81'	'41'	256 bytes

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to all the received chained I-Blocks).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + 'E6 5C 87 F0' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + 'E6 5C 87 F0' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + 'E6 5C 87 F0' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' ◀ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(1)₀ ['00 A4 04 00 40' + '01 02 03'] ◀ LT	11 bytes frame
10	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgment R-Block
11	PUT ◀ I(1)₁ ['04 05 06 ... 1F 20 21'] ◀ LT	33 bytes frame
12	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgment R-Block
13	PUT ◀ I(1)₀ ['22'] ◀ LT	4 bytes frame
14	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgment R-Block
15	PUT ◀ I(1)₁ ['23 24 25 ... 38 39 3A'] ◀ LT	27 bytes frame
16	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgment R-Block
17	PUT ◀ I(1)₀ ['3B 3C 3D 3E 3F'] ◀ LT	8 bytes frame
18	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgment R-Block
19	PUT ◀ I(1)₁ ['40' + '00' + '90'] ◀ LT	6 bytes frame
20	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgment R-Block
21	PUT ◀ I(0)₀ ['00'] ◀ LT	4 bytes last Block of chain
22	PUT ▶ I(0)₁ ['00 A4 04 00 40' + '01 02 03 ... 3E 3F 40' + '00'] ▶ LT	Loop-back (73 bytes)
23	PUT ◀ I(1)₁ ['00 A4 04 00 87' + '01 02 03 ... 40 41 42'] ◀ LT	74 bytes frame
24	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgment R-Block
25	PUT ◀ I(1)₀ ['43 44'] ◀ LT	5 bytes frame
26	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgment R-Block
27	PUT ◀ I(1)₁ ['45 46 47 ... 6A 6B 6C'] ◀ LT	43 bytes frame

Step	Exchanges	Comments
28	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgment R-Block
29	PUT ◀ I(1)₀ ['6D 6E 6F ... 72 73 74'] ◀ LT	11 bytes frame
30	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgment R-Block
31	PUT ◀ I(1)₁ ['75 76 77 ... 85 86 87'] ◀ LT	22 bytes frame
32	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgment R-Block
33	PUT ◀ I(0)₀ ['00' + '90 00'] ◀ LT	6 bytes last Block of chain
34	PUT ▶ I(0)₁ ['00 A4 04 00 87' + '01 02 03 ... 85 86 87' + '00'] ▶ LT	Loop-back (144 bytes)
35	PUT ◀ I(0)₁ ['“EOT Command”' + '90 00'] ◀ LT	End Of Test command
36	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
37	PUT ▶ ‘05 00 08’ ▶ LT	WUPB to poll for the PICC
38	PUT ▶ ‘05 00 08’ ▶ LT	WUPB to poll for the PICC
39	PUT ▶ ‘05 00 08’ ▶ LT	WUPB to poll for the PICC

Scenario 116: Type B Error free chained I-Blocks reception with rare frame sizes

5.20.Type B Error free exchange with the minimum Frame Delay Time PCD→PICC for different values of the Frame Waiting Time [TB215.x]

Test codification:

TB215.x

Test objective:

To ensure that the PCD accepts sequences received with the minimum Frame Delay Time $FDT_{B,PICC,MIN} = TR0_{MIN} + TR1_{MIN}$ for all possible values of the Frame Waiting Time (FWT).

References Requirement:

4.8.1.6

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

Until the End Of Test command (included), the LT sends sequences (commands and blocks) using the minimum Frame Delay Time $FDT_{B,PICC,MIN} = TR0_{MIN} + TR1_{MIN}$ (i.e. no subcarrier during $TR0_{MIN}$ and subcarrier with no phase transition during $TR1_{MIN}$) between the end of the sequence sent by the PUT and the beginning of the sequence replied by the LT.

In this test, the following Protocol Information (PI) and Frame Waiting Time shall be used:

	PI			(FWT+ΔFWT)
	Byte 1	Byte 2	Byte 3	
x=0	'80'	'21'	'01'	53248x 1/f _c
x=1	'80'	'21'	'81'	1097728x 1/f _c
x=2	'80'	'21'	'E1'	67158016x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT accepts and replies to the sequences sent by the LT with the minimum Frame Delay Time).

Failure action:

Stop further testing.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + '56 F1 23 DD' + '00 00 00 00' + PI sent using FDT _{B,PICC,MIN} ▲ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + '56 F1 23 DD' + '00 00 00 00' + PI sent using FDT _{B,PICC,MIN} ▲ LT	ATQB
6	PUT ▶ '1D' + '56 F1 23 DD' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' sent using FDT _{B,PICC,MIN} ▲ LT	ATTRIB Response
8	PUT ▶ I(0) ₀ ['00 A4 04 00 0E' + '2PAY.SYS.DDF01' + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(0) ₀ ['00 B2 01 04 00' + '90 00'] sent using FDT _{B,PICC,MIN} ▲ LT	
10	PUT ▶ I(0) ₁ ['00 B2 01 04 00'] ▶ LT	Loop-back
11	PUT ◀ I(0) ₁ ['00 B2 02 04 00' + '90 00'] sent using FDT _{B,PICC,MIN} ▲ LT	
12	PUT ▶ I(0) ₀ ['00 B2 02 04 00'] ▶ LT	Loop-back
13	PUT ◀ I(0) ₀ ['00 A4 04 00 17' + '01 02 ... 17' + '00' + '90 00'] sent using FDT _{B,PICC,MIN} ▲ LT	
14	PUT ▶ I(0) ₁ ['00 A4 04 00 17' + '01 02 ... 17' + '00'] ▶ LT	Loop-back (32 bytes frame)
15	PUT ◀ I(0) ₁ ['00 B2 03 04 00' + '90 00'] sent using FDT _{B,PICC,MIN} ▲ LT	
16	PUT ▶ I(0) ₀ ['00 B2 03 04 00'] ▶ LT	Loop-back
17	PUT ◀ I(0) ₀ ['00 B2 04 04 00' + '90 00'] sent using FDT _{B,PICC,MIN} ▲ LT	
18	PUT ▶ I(0) ₁ ['00 B2 04 04 00'] ▶ LT	Loop-back
19	PUT ◀ I(0) ₁ ['00 A4 04 00 17' + '18 19 ... 2E' + '00' + '90 00'] sent using FDT _{B,PICC,MIN} ▲ LT	
20	PUT ▶ I(0) ₀ ['00 A4 04 00 17' + '18 19 ... 2E' + '00'] ▶ LT	Loop-back (32 bytes frame)

Step	Exchanges	Comments
21	PUT ↪ I(0)₀ [“EOT Command” + ‘90 00’] sent using FDT _{B,PICC,MIN}	◀ LT End Of Test command
22	PUT ↤ II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
23	PUT ↪ ‘05 00 08’	▶ LT WUPB to poll for the PICC
24	PUT ↪ ‘05 00 08’	▶ LT WUPB to poll for the PICC
25	PUT ↪ ‘05 00 08’	▶ LT WUPB to poll for the PICC

**Scenario 117: Type B Error free exchange with the minimum Frame Delay Time
PCD→PICC for different values of the Frame Waiting Time (x=0 to 2)**

5.21. Type B Polling with an error after WUPB [TB301.xy]

Test codification:

TB301.xy

Test objective:

To ensure that the PCD detects a Type B PICC and initiates a Type B transaction when it receives an error in response to the WUPB command sent during polling.

References Requirements:

6.2.1.1, 6.2.1.2, 9.2.1.4, 9.6.1.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

During the polling procedure, the LT replies to the WUPB command sent by the PUT with an ATQB with error.

The following transmission errors on ATQB are generated successively by the LT:

- xy=01: ATQB with CRC error: the less significant bit of the 1st CRC byte is corrupted and the parity bit of this CRC byte is adapted in order to have only a CRC error
- xy=02: ATQB with CRC with residual bits: the 2nd CRC byte contains only 5 bits followed by no modulation (no EoS)

The following protocol errors are generated successively by the LT:

- xy=10: ATQB with the first byte (Byte1) equal to 'FA' (different from '50')
- xy=11: ATQB with no CRC_B bytes
- xy=13: 13 bytes long ATQB (too short ATQB)
- xy=14: b₁-b₄ of B2 of PI set to 9_h
- xy=15: HLTB Response = '00'

In this test, the following Protocol Information (PI) shall be used:

PI				Comments
	Byte 1	Byte 2	Byte 3	
xy=01-02 and 10-11	'80'	'21'	'41'	Default Protocol Information with an error in function of 'xy'
xy=13	'80'	'21'	-	Too short ATQB
xy=14	'80'	'29'	'41'	b ₁ -b ₄ of B2 of PIC set to 9 _h
xy=15	NA	NA	NA	Not Applicable

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT continues polling upon receipt of an ATQB with error and then starts the Type B collision detection procedure).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	Error in function of 'xy' For xy=01, 02, 13 and 14: ATQB = '50'+'10 FE C6 B5'+'00 00 00'+PI - with an error in function of 'xy' PUT ↵ For xy=10: ATQB = 'FA'+'10 FE C6 B5'+'00 00 00 00'+PI ↵ LT For xy=11: ATQB = '50'+'10 FE C6 B5'+'00 00 00 00'+PI (no CRC_B) For xy=15: HLTB Response = '00'	Error in function of 'xy'
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↵ '50' + '10 FE C6 B5' + '00 00 00 00' + PI ↵ LT	ATQB
6	PUT ▶ '1D' + '10 FE C6 B5' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↵ '00' ↵ LT	ATTRIB Response
8	PUT ▶ I(0)o ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↵ I(0)o ["EOT Command" + '90 00'] ↵ LT	End Of Test command
10	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
11	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
12	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
13	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 118: Type B Polling with an error after WUPB (x=01, 02, 10, 11, 13, 14 and 15)

5.22. Type B Polling with detection of a Type B then a Type A PICC [TB303]

Test codification:

TB303

Test objective:

To ensure that the PCD behaves correctly when it detects a Type A PICC after having detected a Type B PICC during polling.

References Requirement:

9.3.1.1

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

After having replied to a WUPB command during polling (first step of this Type B test), the LT responds to the next WUPA command sent by the PUT during polling with a valid ATQA sequence.

Remark: the LT uses the default Frame Delay Time $FDT_{A,PICC,ANTICOLLISION}$ to send the ATQA sequence.

The LT measures the delay between the beginning of the ATQA sequence and the beginning of the PICC Reset.

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

In this test, the default Protocol Information (PI) shall be used:

PI			Comments
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT performs a PICC Reset when it receives an ATQA after having received an ATQB during polling).

The delay between the beginning of the ATQA sequence and the beginning of the PICC Reset is at most $t_{RESETDELAY}$.

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$.

Following the PICC Reset, the PUT restarts the initial polling procedure by sending a WUPA command followed by a WUPB command both preceded by a delay of at least $t_{P,MIN}$ and at most $t_{P,MAX}$ with carrier on (i.e. returns to step 1 of the Scenario of the Test Case TC001).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + '19 94 67 31' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (<i>Type A short frame</i>) ▶ LT	WUPA
4	PUT ◀ '01 00' (<i>no CRC_A</i>) ◀ LT	Default ATQA
5	PUT ▶ '50 00' ▶ LT	HLTA
6	PUT II The PUT stops sending the carrier within tRESETDELAY The PUT keeps the carrier off during at least tRESET,MIN and at most tRESET,MAX	II LT PICC Reset

The PUT restarts the initial polling procedure i.e. returns to step 1 of the Scenario of the Test Case TC001

Scenario 119: Type B Polling with detection of a Type B then a Type A PICC

5.23.Type B Collision detection with an error after WUPB [TB304.xy]

Test codification:

TB304.xy

Test objective:

To ensure that the PCD behaves correctly when it receives an error in response to the WUPB command sent during collision detection.

References Requirements:

6.2.1.1, 6.2.1.2, 9.3.3.1, 9.6.1.2, 6.3.2.8a

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT responds to the WUPB command sent by the PUT during polling with the default ATQB (i.e. '50' + PUPI + '00 00 00 00 00 21 41').

The LT responds to the WUPB command sent by the PUT during collision detection (i.e. 2nd WUPB of the Scenario) with an erroneous ATQB.

The LT measures the delay between the beginning of the sequence with error and the beginning of the PICC Reset.

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

The following transmission errors on ATQB are generated successively by the LT:

- xy=01: ATQB with CRC error: the most significant bit of the 2nd CRC byte is corrupted and the parity bit of this CRC byte is adapted in order to have only a CRC error
- xy=02: ATQB with CRC with residual bits: the 2nd CRC byte contains only 5 bits followed by no modulation (no EoS)

The following protocol errors are generated successively by the LT:

- xy=10: ATQB with the first byte (Byte1) equal to 'FA' (different from '50')
- xy=11: ATQB with no CRC_B bytes
- xy=13: 13 bytes long ATQB (too short ATQB)
- xy=14: ATQB with b₄ of Protocol Type set to (1)_b
- xy=15: HLTB Response = '00'

In this test, the following Protocol Information (PI) shall be used (during activation only):

	PI			Comments
	Byte 1	Byte 2	Byte 3	
xy=01-02 and 10-11	'80'	'21'	'41'	Default Protocol Information with an error in function of 'xy'

	PI			Comments
	Byte 1	Byte 2	Byte 3	
xy=13	'80'	'21'	-	Too short ATQB
xy=14	'80'	'29'	'41'	b ₄ of Protocol Type set to (1) _b
xy=15	NA	NA	NA	Not Applicable

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT performs a PICC Reset when it detects an error after WUPB).

The delay between the beginning of the sequence with error and the beginning of the PICC Reset is at most t_{RESETDELAY}.

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least t_{RESET,MIN} and at most t_{RESET,MAX}.

Following the PICC Reset, the PUT restarts the initial polling procedure by sending a WUPA command followed by a WUPB command both preceded by a delay of at least t_{P,MIN} and at most t_{P,MAX} with carrier on (i.e. returns to step 1 of the Scenario of the Test Case TC001).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ▲ '50' + '76 75 57 40' + '00 00 00 00 00 21 41' ▲ LT	Valid ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ▲ Error in function of 'xy' For xy=01, 02, 13 and 14: ATQB = '50'+'10 FE C6 B5'+'00 00 00'+P/ with an error in function of 'xy' For xy=10: ATQB = 'FA'+'10 FE C6 B5'+'00 00 00 00'+P/ For xy=11: ATQB = '50'+'10 FE C6 B5'+'00 00 00 00'+P/ (no CRC_B) For xy=15: HLTB = '00' ▲ LT	Error in function of 'xy'
6	PUT II The PUT stops sending the carrier within t _{RESETDELAY} The PUT keeps the carrier off during at least t _{RESET,MIN} and at most t _{RESET,MAX} II LT	PICC Reset

The PUT restarts the initial polling procedure i.e. returns to step 1 of the Scenario of the Test Case TC001

Scenario 120: Type B Collision detection with an error after WUPB (xy=01, 02, 10, 11, 13, 14 and 15)

5.24. Type B Activation with ‘noise’ after ATTRIB [TB305.x]

Test codification:

TB305.x

Test objective:

To ensure that the PCD behaves correctly when it receives some ‘noise’ (i.e. a frame with a transmission error to be processed as noise by the PCD) in response to the ATTRIB command sent during activation.

References Requirements:

4.9.2.1, 6.2.1.1, 6.2.1.2, 9.6.1.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT replies to the ATTRIB command sent by the PUT with a sequence inducing a ‘noise’ error using a delay of $[TR0_{MIN} + 128/f_c]$ (with no subcarrier generated by the LT) between the end of the ATTRIB sequence sent by the PUT and the beginning of the ‘noise’ error generated by the LT (in this test, we consider that the synchronization time TR1 with subcarrier on but no modulation is part of the defined ‘noise’ errors).

The LT measures the delay between the end of the sequence sent by the PUT after which a transmission error is generated and the beginning of the next sequence sent by the PUT to process the error.

The following ‘noise’ errors are generated successively by the LT:

- x=0: ATTRIB Response preceded by the minimum synchronization time $TR1_{MIN}$ (with subcarrier on but no modulation) and with CRC error (the CRC bytes are corrupted)
- x=1: ATTRIB Response preceded by the minimum synchronization time $TR1_{MIN}$ (with subcarrier on but no modulation) and with some residual bits (i.e. the total number of bits is not a multiple of 8) followed by no modulation (no EoS)
- x=2: ATTRIB Response preceded by the minimum synchronization time $TR1_{MIN}$ (with subcarrier on but no modulation) and with no End of Sequence (EoS)
- x=4: Continuous modulation of the PUT carrier with a frequency equal to $f_s = f_c/16$, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of $21712 \times 1/f_c$ (i.e. duration of the maximum synchronization time $TR1_{MAX}$) followed by a 10 bytes frame with the maximum Start of Sequence and End of Sequence and with $EGT_{PICC,MAX}$ between 2 consecutive characters in Type B)
- x=5: Too short ATTRIB Response (equivalent to “ATTRIB Response with no CRC byte”)

In this test, the default Protocol Information (PI) shall be used:

PI			FWT+ΔFWT
Byte 1	Byte 2	Byte 3	
'80'	'21'	'71'	573440 x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT ignores the ‘noise’ error, retransmits the ATTRIB command and continues the transaction upon receipt of a correct ATTRIB Response).

The delay between the end of the sequence sent by the PUT after which a ‘noise’ error is generated and the beginning of the next sequence sent by the PUT to process the error is at least [(FWT+ ΔFWT) + t_{MIN,RETRANSMISSION}] and at most [(FWT+ ΔFWT) + t_{RETRANSMISSION}].

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + 'A5 63 9B 4F' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + 'A5 63 9B 4F' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + 'A5 63 9B 4F' + '00 08 01 00' ▶ LT	ATTRIB
7	'Noise' error in function of 'x' For x=0 and 2: '00' with a transmission error in function of 'x' PUT ◀ For x=1: '00' with 3 bits to (101) _b following the CRC bytes For x=4: ATTRIB Response replaced by a continuous modulation with a duration of 21712 x 1/f _c For x=5: '00' (no CRC_B)	◀ LT Error in function of 'x'
8	'1D' + 'A5 63 9B 4F + '00 08 01 00' PUT ▶ sent between [(FWT+ ΔFWT) + t _{MIN,RETRANSMISSION}] and [(FWT+ ΔFWT) + t _{RETRANSMISSION}] measured from the end of the last sequence from the PUT	▶ LT ATTRIB
9	PUT ◀ '00' ◀ LT	ATTRIB Response (error recovery)
10	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
11	PUT ◀ I(0)₀ ["EOT Command" + '90 00'] ◀ LT	End Of Test command
12	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
13	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
14	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
15	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 121: Type B Activation with 'noise' after ATTRIB (x=0 to 2 and 4 to 5)

5.25. Type B Activation with an error after ATTRIB [TB306.xy]

Test codification:

TB306.xy

Test objective:

To ensure that the PCD behaves correctly when it receives a frame with error in response to the ATTRIB command sent during activation.

References Requirements:

6.2.1.1, 6.2.1.2, 9.6.1.1, 9.6.1.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT measures the delay between the beginning of the sequence with error and the beginning of the PICC Reset.

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

The following transmission errors are generated successively by the LT:

- xy=01: I-Block with CRC error: the most significant bit of the 2nd CRC byte is corrupted
- xy=02: I-Block preceded by the minimum synchronization time TR1_{MIN} (with subcarrier on but no modulation) and with some residual bits (i.e. the total number of bits is not a multiple of 8) followed by no modulation (no EoS)

The following protocol errors are generated successively by the LT:

- xy=10: ATTRIB Response with CID different from '0'
- xy=11: I-Block

In this test, the default Protocol Information (PI) shall be used:

PI			Comments
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT performs a PICC Reset when it detects an error after ATTRIB).

The delay between the beginning of the sequence with error and the beginning of the PICC Reset is at most t_{RESETDELAY}.

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least t_{RESET,MIN} and at most t_{RESET,MAX}.

Following the PICC Reset, the PUT restarts the initial polling procedure by sending a WUPA command followed by a WUPB command both preceded by a delay of at least $t_{P,MIN}$ and at most $t_{P,MAX}$ with carrier on (i.e. returns to step 1 of the Scenario of the Test Case TC001).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ▲ '50' + 'AA 65 3F 4B' + '00 00 00 00' + PI ▲ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ▲ '50' + 'AA 65 3F 4B' + '00 00 00 00' + PI ▲ LT	ATQB
6	PUT ▶ '1D' + 'AA 65 3F 4B' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ▲ Error in function of 'xy' For xy=01: I(0) ₀ ['00 B2 01 04 00' + '90 00'] with CRC error For xy=02: I(0) ₀ ['00 B2 01 04 00' + '90 00'] with 3 bits to (101) _b following the CRC bytes For xy=10: '0F' For xy=11: I(0) ₀ ['00 B2 01 04 00' + '90 00']	◀ LT Error in function of 'xy'
8	PUT II The PUT stops sending the carrier within $t_{RESETDELAY}$ The PUT keeps the carrier off during at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$	II LT PICC Reset
The PUT restarts the initial polling procedure i.e. returns to step 1 of the Scenario of the Test Case TC001		

Scenario 122: Type B Activation with an error after ATTRIB (xy=01, 02, 10 and 11)

5.26.Type B Collision detection with a time-out after WUPB [TB311.x]

Test codification:

TB311.x

Test objective:

To ensure that the PCD behaves correctly when it does not receive any response to the WUPB command sent during collision detection.

References Requirements:

4.8.1.14, 9.6.1.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenarios.

For $x=0$, the LT measures the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

For $x=1$, the LT measures the delay between the end of the second sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

For $x=2$, the LT measures the delay between the end of the third sequence to which the LT does not respond and the beginning of the PICC Reset and the time during which the PUT stops sending the carrier to perform a PICC Reset.

In this test, the default Protocol Information (PI) shall be used:

PI			Comments
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenarios (the PUT retransmits the WUPB commands up to two times when it detects a time-out error and performs a PICC Reset when it detects a third consecutive time-out error).

For $x=0$, the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at least $[(FWT_{ATQB}) + t_{MIN,RETRANSMISSION}]$ and at most $[(FWT_{ATQB}) + t_{RETRANSMISSION}]$.

For $x=1$, the delay between the end of the second sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at least $[(FWT_{ATQB}) + t_{MIN,RETRANSMISSION}]$ and at most $[(FWT_{ATQB}) + t_{RETRANSMISSION}]$.

For $x=2$, the delay between the end of the third sequence to which the LT does not respond and the beginning of the PICC Reset is at most $[FWT_{ATQB} + t_{RESETDELAY}]$.

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$.

For $x=2$ (only), following the PICC Reset, the PUT restarts the initial polling procedure by sending a WUPA command followed by a WUPB command both preceded by a delay of at least $t_{P,MIN}$ and at most $t_{P,MAX}$ with carrier on (i.e. returns to step 1 of the Scenario of the Test Case TC001).

Failure action:

Proceed with the next test.

Scenarios:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ▲ '50' + '90 FE 01 5A' + '00 00 00 00' + PI ▲ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ▶ '05 00 08' sent between $[(FWT_{ATQB}) + t_{MIN,RETRANSMISSION}]$ and $[(FWT_{ATQB}) + t_{RETRANSMISSION}]$ ▶ LT	WUPB
6	PUT ▲ '50' + '90 FE 01 5A' + '00 00 00 00' + PI ▲ LT	ATQB
7	PUT ▶ '1D' + '90 FE 01 5A' + '00 08 01 00' ▶ LT	ATTRIB
8	PUT ▲ '00' ▲ LT	ATTRIB Response
9	PUT ▶ I(0)0 ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
10	PUT ▲ I(0)0 ["EOT Command" + '90 00'] ▲ LT	End Of Test command
11	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) □ LT	PICC Reset
12	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
13	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
14	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 123: Type B Collision detection with a time-out after WUPB ($x=0$)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + '11 22 44 88' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ▶ '05 00 08' ▶ LT	WUPB
6	PUT ▶ '05 00 08' sent between $[(FWT_{ATQB}) + t_{MIN,RETRANSMISSION}]$ and $[(FWT_{ATQB}) + t_{RETRANSMISSION}]$ ▶ LT	WUPB
7	PUT ◀ '50' + '11 22 44 88' + '00 00 00 00' + PI ◀ LT	ATQB
8	PUT ▶ '1D' + '11 22 44 88' + '00 08 01 00' ▶ LT	ATTRIB
9	PUT ◀ '00' ◀ LT	ATTRIB Response
10	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
11	PUT ◀ I(0)₀ ["EOT Command" + '90 00'] ◀ LT	End Of Test command
12	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
13	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
14	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
15	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 124: Type B Collision detection with a time-out after WUPB (x=1)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + '31 10 C2 14' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ▶ '05 00 08' ▶ LT	WUPB
6	PUT ▶ '05 00 08' ▶ LT	WUPB
7	PUT II The PUT stops sending the carrier within $[FWT_{ATQB} + t_{RESETDELAY}]$ The PUT keeps the carrier off during at least $t_{RESET,MIN}$ and at most $t_{RESET,MAX}$ II LT	PICC Reset

The PUT restarts the initial polling procedure i.e. returns to step 1 of the Scenario of the Test Case TC001

Scenario 125: Type B Collision detection with a time-out after WUPB (x=2)

5.27.Type B Activation with a time-out after ATTRIB [TB312.x]

Test codification:

TB312.x

Test objective:

To ensure that the PCD behaves correctly when it does not receive any response to the ATTRIB command sent during activation.

References Requirements:

4.8.1.8, 9.6.1.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT measures the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

In this test, the following Protocol Information (PI) shall be used:

PI				(FWT+ΔFWT)
	Byte 1	Byte 2	Byte 3	
x=0	'80'	'21'	'01'	53248 x 1/f _c
x=1	'80'	'21'	'11'	57344 x 1/f _c
x=2	'80'	'21'	'21'	65536 x 1/f _c
x=3	'80'	'21'	'31'	81920 x 1/f _c
x=4	'80'	'21'	'41'	114688 x 1/f _c (default value)
x=5	'80'	'21'	'51'	180224 x 1/f _c
x=6	'80'	'21'	'61'	311296 x 1/f _c
x=7	'80'	'21'	'71'	573440 x 1/f _c
x=8	'80'	'21'	'81'	1097728 x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT retransmits the ATTRIB command when it detects a time-out error).

The delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at least [(FWT+ ΔFWT) + t_{MIN,RETRANSMISSION}] and at most [(FWT+ ΔFWT) + t_{RETRANSMISSION}].

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + 'D3 5E 33 AF' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + 'D3 5E 33 AF' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + 'D3 5E 33 AF' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ▶ '1D' + 'D3 5E 33 AF' + '00 08 01 00' sent between [(FWT+ ΔFWT) + t _{MIN,RETRANSMISSION}] and [(FWT+ ΔFWT) + t _{RETRANSMISSION}] in function of 'x' ▶ LT	ATTRIB
8	PUT ◀ '00' ◀ LT	ATTRIB Response
9	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
10	PUT ◀ I(0)₀ ["EOT Command" + '90 00'] ◀ LT	End Of Test command
11	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
12	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
13	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
14	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 126: Type B Activation with a time-out after ATTRIB (x=0 to 8)

5.28.Type B Activation with respect of the EMD Suppression behavior after ATTRIB [TB335.xy]

Test codification:

TB335.xy

Test objective:

To ensure that, following the ATTRIB command sent during activation, the PCD correctly ignores all the transmission errors except the frames of at least 4 bytes with no residual bit and with CRC error and is ready to process a correct sequence no later than $t_{RECOVERY}$ after reception of the last transmission error.

References Requirement:

4.9.2.1

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT responds to an ATTRIB command sent by the PUT during activation with a transmission error (but not a frame of at least 4 bytes with no residual bit and with CRC error) using the following delay TR0 (with no subcarrier generated by the LT) between the end of the sequence sent by the PUT and the beginning of the transmission error generated by the LT (in this test, we consider that the synchronization time TR1 with subcarrier on but no modulation is part of the defined errors):

- $x=0: TR0 = TR0_{MIN} - 128/f_c$
- $x=1: TR0 = TR0_{MIN} + 128/f_c$
- $x=2: TR0 = 524288 \times 1/f_c$

Then, the LT sends a correct ATTRIB Response sequence to the PUT using a delay equal to $t_{RECOVERY}$ between the end of the transmission error and the beginning of the synchronization time TR1 (with subcarrier on but no modulation) of the correct response sequence both sent by the LT.

Remark: this sequence is sent using the default value of TR1 defined in the section Generic Information about the Tests.

The following 'noise' errors are generated successively by the LT:

- $y=0: Continuous modulation of the PUT carrier with a frequency equal to f_s = f_c/16, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of 512 \times 1/f_c$
- $y=1: Continuous modulation of the PUT carrier with a frequency equal to f_s = f_c/16, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of 5312 \times 1/f_c (i.e. duration of the minimum synchronization time TR1_{MIN} followed by a 1 byte frame with the minimum Start of Sequence and End of Sequence and with EGT_{PICC,MIN} between 2 consecutive characters in Type B)$
- $y=2: Continuous modulation of the PUT carrier with a frequency equal to f_s = f_c/16, with the same amplitude as the other responses sent by the LT during the test$

transaction and with a duration of $21712 \times 1/f_c$ (i.e. duration of the maximum synchronization time $TR1_{MAX}$ followed by a 10 bytes frame with the maximum Start of Sequence and End of Sequence and with $EGT_{PICC,MAX}$ between 2 consecutive characters in Type B)

- $y=3$: ATTRIB Response preceded by the minimum synchronization time $TR1_{MIN}$ (with subcarrier on but no modulation) and with the minimum Start of Sequence and End of Sequence ($SoS = t_{PICC,S,1,MIN}$ of logical state low followed by $t_{PICC,S,2,MIN}$ of logical state high with $EGT_{PICC,MIN}$ between 2 consecutive characters and with some residual bits (i.e. the total number of bits is not a multiple of 8) followed by no modulation (no EoS)
- $y=4$: ATTRIB Response preceded by the minimum synchronization time $TR1_{MIN}$ (with subcarrier on but no modulation) and with the minimum Start of Sequence ($SoS = t_{PICC,S,1,MIN}$ of logical state low followed by $t_{PICC,S,2,MIN}$ of logical state high), with $EGT_{PICC,MIN}$ between 2 consecutive characters and with no End of Sequence (EoS)
- $y=5$: ATTRIB Response preceded by the minimum synchronization time $TR1_{MIN}$ (with subcarrier on but no modulation) and with the minimum Start of Sequence and End of Sequence ($SoS = t_{PICC,S,1,MIN}$ of logical state low followed by $t_{PICC,S,2,MIN}$ of logical state high and $EoS = t_{PICC,E,MIN}$ of logical state low before the LT turns the subcarrier off), with $EGT_{PICC,MIN}$ between 2 consecutive characters and with CRC error (the CRC bytes are corrupted)

In this test, the default Protocol Information (PI) shall be used:

PI			FWT+ΔFWT
Byte 1	Byte 2	Byte 3	
'80'	'21'	'71'	$573440 \times 1/f_c$

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (after sending each frame, the PUT ignores the transmission error and accepts the next correct sequence sent by the LT).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + '3E 28 49 FF' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + '3E 28 49 FF' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + '3E 28 49 FF' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ 'Noise' error in function of 'y' sent using the delay TR0 (delay with no subcarrier generated by the LT preceding the synchronization time TR1) in function of 'x' For y=0: 512 x 1/f _c of continuous subcarrier modulation For y=1: 5312 x 1/f _c of continuous subcarrier modulation For y=2: 21712 x 1/f _c of continuous subcarrier modulation For y=3: ATTRIB Response = '00' preceded by TR1 _{MIN} , with the minimum SoS and EoS, with EGT _{PICC,MIN} and with 3 bits to (101) _b following the CRC bytes For y=4: ATTRIB Response = '00' preceded by TR1 _{MIN} , with the minimum SoS, with EGT _{PICC,MIN} and with no EoS For y=5: ATTRIB Response = '00' preceded by TR1 _{MIN} , with the minimum SoS and EoS, with EGT _{PICC,MIN} and with CRC error	◀ LT Error in function of 'y' sent with a delay TR0 (delay with no subcarrier generated by the LT preceding the synchronization time TR1) in function of 'x'
8	PUT ◀ '00' (correct ATTRIB Response) sent using a delay of t _{RECOVERY} between the end of the transmission error and the beginning of the synchronization time TR1 (with subcarrier on but no modulation) preceding the correct sequence	◀ LT Correct ATTRIB Response sequence sent at t _{RECOVERY} after the transmission error (applied before the synchronization time TR1)
9	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
10	PUT ◀ I(0)₀ ["EOT Command" + '90 00'] ◀ LT	End Of Test command
11	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
12	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
13	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
14	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 127: Type B Activation with respect of the EMD Suppression behavior after ATTRIB (xy=00 to 05, xy=10 to 15 and xy=20 to 25)

5.29.Type B Activation with respect of the ‘deaf time’ after ATTRIB [TB340.x]

Test codification:

TB340.x

Test objective:

To ensure that, following the ATTRIB command sent during activation, the PCD is completely deaf (i.e. ignores any subcarrier generated by the PICC) until TR0_{MIN}.

References Requirement:

4.3.2.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) on reception of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

The tests TB340.x is performed after a new run of TB000, with no reset of the test tool between the pre-test TB000 and the tests TB340.x to ensure that the value of TR1_{PUTMIN} used is during TB340 is correct.

Procedure:

Run the following scenario.

The LT responds to an ATTRIB command sent by the PUT during activation with a sequence with no transmission error (i.e. a correct sequence or a sequence with protocol error) using the delay TR0 = TR0_{MIN} – 128/f_c (with no subcarrier generated by the LT) between the end of the sequence sent by the PUT and the beginning of the synchronization time TR1 (with subcarrier on but no modulation) preceding the sequence replied by the LT.

The following sequences are successively sent by the LT in response to the ATTRIB command:

- x=0: ATTRIB Response preceded by TR1 = TR1_{PUTMIN}, the minimum synchronization time supported by the PUT (with subcarrier on but no modulation), and with the minimum Start of Sequence and End of Sequence (SoS = t_{PICC,S,1,MIN} of logical state low followed by t_{PICC,S,2,MIN} of logical state high and EoS = t_{PICC,E,MIN} of logical state low before the LT turns the subcarrier off), with EGT_{PICC,MIN} between 2 consecutive characters and with correct CRC
 - *Remark: the value of the parameter TR1_{PUTMIN} has been determined during the test TB000*
- x=1: ATTRIB Response preceded by TR1 = TR1_{PUTMIN}, the minimum synchronization time supported by the PUT (with subcarrier on but no modulation), and with the minimum Start of Sequence and End of Sequence (SoS = t_{PICC,S,1,MIN} of logical state low followed by t_{PICC,S,2,MIN} of logical state high and EoS = t_{PICC,E,MIN} of logical state low before the LT turns the subcarrier off), with EGT_{PICC,MIN} between 2 consecutive characters and with no CRC
 - *Remark: the value of the parameter TR1_{PUTMIN} has been determined during the test TB000*

In this test, the default Protocol Information (PI) shall be used:

PI			Comments
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (after sending the ATTRIB command, the PUT ignores the sequence received during the 'deaf time' and processes it as a time-out error i.e. resends the ATTRIB command).

Failure action:

Proceed with next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + '98 3A E5 00' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + '98 3A E5 00' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + '98 3A E5 00' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ Sequence in function of 'x' sent using the delay TR0 = TR0 _{MIN} – 128/f _c (delay with no subcarrier generated by the LT preceding the synchronization time TR1) For x=0: ATTRIB Response = '00' preceded by TR1 _{PUTMIN} , with the minimum SoS and EoS, with EGT _{PICC,MIN} and with correct CRC For x=1: ATTRIB Response = '00' preceded by TR1 _{PUTMIN} , with the minimum SoS and EoS, with EGT _{PICC,MIN} and with no CRC	◀ LT Sequence in function of 'x' sent with the delay TR0 _{MIN} – 128/f _c
8	PUT ▶ '1D' + '98 3A E5 00' + '00 08 01 00' ▶ LT	ATTRIB
9	PUT ◀ '00' ◀ LT	ATTRIB Response
10	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
11	PUT ◀ I(0)₀ [“EOT Command” + '90 00'] ◀ LT	End Of Test command
12	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
13	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
14	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
15	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 128: Type B Activation with respect of the ‘deaf time’ after ATTRIB (x=0 and 1)

5.30.Type B Error notification on an I-Block not indicating chaining [TB401.xy]

Test codification:

TB401.xy

Test objective:

To ensure that the PCD behaves correctly when it receives one to three consecutive error notification(s) on an I-Block not indicating chaining.

References Requirements:

4.8.1.8, 10.1.5.1, 10.3.4.3, 10.3.4.4, 10.3.5.5, 10.3.5.9

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenarios.

For $xy=00$ to 14 and for each error notification during block protocol, the LT measures the delay between the end of the sequence on which the LT signals an error and the beginning of the sequence sent by the PUT to process the time-out error.

For $xy=15$, the LT measures the delay between the beginning of the sequence containing the last R(ACK) Block sent by the LT and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier). And the LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

In this test, the following Protocol Information (PI) shall be used:

PI				(FWT+ΔFWT)
	Byte 1	Byte 2	Byte 3	
x=00	'80'	'21'	'01'	53248 x 1/f _c
x=01	'80'	'21'	'11'	57344 x 1/f _c
x=02	'80'	'21'	'21'	65536 x 1/f _c
x=03	'80'	'21'	'31'	81920 x 1/f _c
x=04 or 15	'80'	'21'	'41'	114688 x 1/f _c (default value)
x=05	'80'	'21'	'51'	180224 x 1/f _c
x=06	'80'	'21'	'61'	311296 x 1/f _c
x=07	'80'	'21'	'71'	573440 x 1/f _c
x=08	'80'	'21'	'81'	1097728 x 1/f _c
x=09	'80'	'21'	'91'	2146304 x 1/f _c
x=10	'80'	'21'	'A1'	4243456 x 1/f _c
x=11	'80'	'21'	'B1'	8437760 x 1/f _c

PI				(FWT+ΔFWT)
	Byte 1	Byte 2	Byte 3	
x=12	'80'	'21'	'C1'	16826368 x 1/f _c
x=13	'80'	'21'	'D1'	33603584 x 1/f _c
x=14	'80'	'21'	'E1'	67158016 x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenarios (the PUT retransmits the I-Block on which it is notified an error up to two times and initiates a PICC Reset upon receipt of a third error notification).

For xy=00 to 14 and for each error notification, the delay between the end of the sequence sent by the PUT to which the LT does not respond and the beginning of the sequence sent by the PUT to process the time-out error is at most [(FWT+ΔFWT) + t_{RETRANSMISSION}].

For xy=15, the delay between the beginning of the sequence containing the last R(ACK) Block sent by the LT (protocol error) and the beginning of the PICC Reset initiated by the PUT is at most t_{RESETDELAY} (i.e. the PUT stops sending the carrier within t_{RESETDELAY}). And the time during which the PUT stops sending the carrier to perform a PICC Reset is at least t_{RESET,MIN}.

Failure action:

Proceed with the next test.

Scenarios:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ▲ '50' + '8F 72 B3 3A' + '00 00 00 00' + PI ▲ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ▲ '50' + '8F 72 B3 3A' + '00 00 00 00' + PI ▲ LT	ATQB
6	PUT ▶ '1D' + '8F 72 B3 3A' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ▲ '00' ▲ LT	ATTRIB Response
8	PUT ▶ I(0) ₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ▲ I(0) ₀ ['00 B2 01 04 00' + '90 00'] ▲ LT	
10	PUT ▶ I(0) ₁ ['00 B2 01 04 00'] ▶ LT	Loop-back
11	PUT ▶ R(NAK) ₁ sent within [(FWT+ ΔFWT) + t _{RETRANSMISSION}] in function of 'xy' ▶ LT	Time-out error notification
12	PUT ▲ R(ACK) ₀ ▲ LT	Request for Block repetition
13	PUT ▶ I(0) ₁ ['00 B2 01 04 00'] ▶ LT	Error recovery
14	PUT ▲ I(0) ₁ ['00 B2 02 04 00' + '90 00'] ▲ LT	
15	PUT ▶ I(0) ₀ ['00 B2 02 04 00'] ▶ LT	Loop-back

Step	Exchanges	Comments
16	PUT ▶ R(NAK)₀ sent within [(FWT+ ΔFWT) + t _{RETRANSMISSION}] in function of 'xy' ▶ LT	Time-out error notification
17	PUT ◀ R(ACK)₁ ◀ LT	Request for Block repetition
18	PUT ▶ I(0)₀ ['00 B2 02 04 00'] ▶ LT	Error recovery
19	PUT ◀ I(0)₀ ['EOT Command' + '90 00'] ◀ LT	End Of Test command
20	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
21	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
22	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 129: Type B Error notification on an I-Block not indicating chaining (xy=00 to 14)

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + 'F8 27 3B A3' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + 'F8 27 3B A3' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + 'F8 27 3B A3' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' ◀ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + '2PAY.SYS.DDF01' + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(0)₀ ['00 B2 5A 04 00' + '90 00'] ◀ LT	
10	PUT ▶ I(0)₁ ['00 B2 5A 04 00'] ▶ LT	Loop-back
11	PUT ▶ R(NAK)₁ ▶ LT	Time-out error notification
12	PUT ◀ R(ACK)₀ ◀ LT	Request for Block repetition
13	PUT ▶ I(0)₁ ['00 B2 5A 04 00'] ▶ LT	Error recovery
14	PUT ▶ R(NAK)₁ ▶ LT	Time-out error notification
15	PUT ◀ R(ACK)₀ ◀ LT	Request for Block repetition
16	PUT ▶ I(0)₁ ['00 B2 5A 04 00'] ▶ LT	Error recovery

Step	Exchanges	Comments
17	PUT \leftarrow I(0) ₁ ['00 B2 C3 04 00' + '90 00'] \leftarrow LT	
18	PUT \rightarrow I(0) ₀ ['00 B2 C3 04 00'] \rightarrow LT	Loop-back
19	PUT \rightarrow R(NAK) ₀ \rightarrow LT	Time-out error notification
20	PUT \leftarrow R(ACK) ₁ \leftarrow LT	Request for Block repetition
21	PUT \rightarrow I(0) ₀ ['00 B2 C3 04 00'] \rightarrow LT	Error recovery
22	PUT \rightarrow R(NAK) ₀ \rightarrow LT	Time-out error notification
23	PUT \leftarrow R(ACK) ₁ \leftarrow LT	Request for Block repetition
24	PUT \rightarrow I(0) ₀ ['00 B2 C3 04 00'] \rightarrow LT	Error recovery
25	PUT \rightarrow R(NAK) ₀ \rightarrow LT	Time-out error notification
26	PUT \leftarrow R(ACK) ₁ (protocol error) \leftarrow LT	Request for Block repetition
27	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) The PICC Reset is initiated within tRESETDELAY The PUT keeps the carrier off during at least tRESET,MIN	II LT PICC Reset

Scenario 130: Type B Error notification on an I-Block not indicating chaining (xy=15)

5.31.Type B Time-out after an I-Block not indicating chaining [TB402]

Test codification:

TB402

Test objective:

To ensure that the PCD behaves correctly when it does not receive any response to an I-Block not indicating chaining.

References Requirements:

4.8.1.8, 10.3.5.5, 10.3.5.9

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

When two consecutive time-out errors are generated successively by the LT, the LT measures the delay between the end of the second sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

When three consecutive time-out errors are generated successively by the LT, the LT measures the delay between the end of the third sequence to which the LT does not respond and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

In this test, the default Protocol Information (PI) shall be used:

PI			FWT+ΔFWT
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	$114688 \times 1/f_c$

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends an R(NAK) Block to ask for retransmission when it detects a first or a second consecutive time-out error after an I-Block not indicating chaining and initiates a PICC Reset when it detects a third consecutive time-out error).

When two consecutive time-out errors are generated successively by the LT, the delay between the end of the second sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at most $[(FWT+\Delta FWT) + t_{RETRANSMISSION}]$.

When three consecutive time-out errors are generated successively by the LT, the delay between the end of the third sequence to which the LT does not respond and the beginning

of the PICC Reset initiated by the PUT is at most $[(FWT + \Delta FWT) + t_{RESETDELAY}]$ (i.e. the PUT stops sending the carrier within $[(FWT + \Delta FWT) + t_{RESETDELAY}]$).

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08'	▶ LT WUPB during polling
2	PUT ▲ '50' + '14 00 0B AC' + '00 00 00 00' + PI	◀ LT ATQB
3	PUT ▶ '52' (Type A short frame)	▶ LT WUPA
4	PUT ▶ '05 00 08'	▶ LT WUPB
5	PUT ▲ '50' + '14 00 0B AC' + '00 00 00 00' + PI	◀ LT ATQB
6	PUT ▶ '1D' + '14 00 0B AC' + '00 08 01 00'	▶ LT ATTRIB
7	PUT ▲ '00'	◀ LT ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
9	PUT ▲ I(0)₀ ['00 B2 01 04 00' + '90 00']	◀ LT
10	PUT ▶ I(0)₁ ['00 B2 01 04 00']	▶ LT Loop-back
11	PUT ▶ R(NAK)₁	▶ LT Time-out error notification
12	PUT ▲ I(0)₁ ['00 B2 02 04 00' + '90 00']	◀ LT Error recovery
13	PUT ▶ I(0)₀ ['00 B2 02 04 00']	▶ LT Loop-back
14	PUT ▶ R(NAK)₀	▶ LT Time-out error notification
15	PUT ▲ I(0)₀ ['00 B2 03 04 00' + '90 00']	◀ LT Error recovery
16	PUT ▶ I(0)₁ ['00 B2 03 04 00']	▶ LT Loop-back
17	PUT ▶ R(NAK)₁	▶ LT Time-out error notification
18	PUT ▶ R(NAK)₁ sent within $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$	▶ LT Time-out error notification
19	PUT ▲ I(0)₁ ['00 B2 04 04 00' + '90 00']	◀ LT Error recovery
20	PUT ▶ I(0)₀ ['00 B2 04 04 00']	▶ LT Loop-back
21	PUT ▶ R(NAK)₀	▶ LT Time-out error notification
22	PUT ▶ R(NAK)₀ sent within $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$	▶ LT Time-out error notification
23	PUT ▲ I(0)₀ ['00 B2 05 04 00' + '90 00']	◀ LT Error recovery

Step	Exchanges		Comments
24	PUT ▶ I(0)₁ ['00 B2 05 04 00']	▶ LT	Loop-back
25	PUT ▶ R(NAK)₁	▶ LT	Time-out error notification
26	PUT ▶ R(NAK)₁	▶ LT	Time-out error notification
27	<p>The PUT performs a PICC Reset (i.e. stops sending the carrier)</p> <p>PUT II The PICC Reset is initiated within $[(FWT + \Delta FWT) + t_{RESETDELAY}]$</p> <p>The PUT keeps the carrier off during at least $t_{RESET,MIN}$</p>	II LT	PICC Reset

Scenario 131: Type B Time-out after an I-Block not indicating chaining

5.32.Type B Transmission error in response to an I-Block not indicating chaining [TB403.x]

Test codification:

TB403.x

Test objective:

To ensure that the PCD behaves correctly when it receives a transmission error in response to an I-Block not indicating chaining.

References Requirements:

6.2.1.1, 6.2.1.2, 10.3.5.3, 10.3.5.9

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPA command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type A frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

When a single transmission error is generated, the LT measures the delay between the beginning of the sequence with transmission error and the beginning of the next sequence replied by the PUT to process the error.

When a single transmission error is generated, the LT measures the delay between the end of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When two consecutive transmission errors are generated, the LT measures the delay between the beginning of the second sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When two consecutive transmission errors are generated, the LT measures the delay between the end of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When three consecutive transmission errors are generated, the LT measures the delay between the beginning of the third sequence with transmission error and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

The following transmission error is generated by the LT:

- x=0: I-Block (in a frame of at least 4 bytes) with CRC error: the less significant bit of the 1st CRC byte is corrupted for the 1st, 4th and 7th error generated, the less significant bit of the 2nd CRC byte is corrupted for the 2nd, 5th and 8th error generated and the most significant bit of the 2nd CRC byte is corrupted for the 3rd, 6th and 9th error generated
- x=2: I-Block of at least 4 bytes preceded by the minimum synchronization time TR1_{MIN} (with subcarrier on but no modulation) and with some residual bits (i.e. the total number of bits is not a multiple of 8) followed by no modulation (no EoS)

- x=3: I-Block of at least 4 bytes preceded by the maximum synchronization time $TR1_{MAX}$ (with subcarrier on but no modulation) and with the maximum Start of Sequence and End of Sequence ($SoS = t_{PICC,S,1,MAX}$ of logical state low followed by $t_{PICC,S,2,MAX}$ of logical state high with $EGT_{PICC,MAX}$ between 2 consecutive characters and with some residual bits (i.e. the total number of bits is not a multiple of 8) followed by no modulation (no EoS)
- x=4: I-Block of at least 4 bytes preceded by the maximum synchronization time $TR1_{MAX}$ (with subcarrier on but no modulation) and with the maximum Start of Sequence ($SoS = t_{PICC,S,1,MAX}$ of logical state low followed by $t_{PICC,S,2,MAX}$ of logical state high), with $EGT_{PICC,MAX}$ between 2 consecutive characters and with no End of Sequence (EoS) field

In this test, the default Protocol Information (PI) shall be used:

PI			Comments
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends an R(NAK) Block when it detects a first or a second consecutive transmission error after an I-Block not indicating chaining and initiates a PICC Reset when it detects a third consecutive transmission error).

When a single transmission error is generated, the delay between the end of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at least $FDT_{B,PCD,MIN}$.

When a single transmission error is generated, the delay between the beginning of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at most $t_{RETRANSMISSION}$.

When two consecutive transmission errors are generated, the delay between the end of the second sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at least $FDT_{B,PCD,MIN}$.

When two consecutive transmission errors are generated, the delay between the beginning of the second sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at most $t_{RETRANSMISSION}$.

When three consecutive transmission errors are generated, the LT measures the delay between the beginning of the third sequence with transmission error and the beginning of the PICC Reset initiated by the PUT is at most $t_{RESETDELAY}$ (i.e. the PUT stops sending the carrier within $t_{RESETDELAY}$).

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + 'ED 74 6F EF' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + 'ED 74 6F EF' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + 'ED 74 6F EF' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' ◀ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(0)₀ ['00 B2 01 04 00' + '90 00'] ◀ LT	
10	PUT ▶ I(0)₁ ['00 B2 01 04 00'] ▶ LT	Loop-back
11	PUT ◀ I(0)₁ ['00 B2 02 04 00' + '90 00'] with a transmission error (i.e. CRC error) in function of x ◀ LT	Error
12	PUT ▶ R(NAK)₁ sent after FDT_{B,PCD,MIN} and within t_{RETRANSMISSION} ▶ LT	Request for Block repetition
13	PUT ◀ I(0)₁ ['00 B2 02 04 00' + '90 00'] ◀ LT	Error recovery
14	PUT ▶ I(0)₀ ['00 B2 02 04 00'] ▶ LT	Loop-back
15	PUT ◀ I(0)₀ ['00 B2 03 04 00' + '90 00'] with a transmission error (i.e. CRC error) in function of x ◀ LT	Error
16	PUT ▶ R(NAK)₀ sent after FDT_{B,PCD,MIN} and within t_{RETRANSMISSION} ▶ LT	Request for Block repetition
17	PUT ◀ I(0)₀ ['00 B2 03 04 00' + '90 00'] ◀ LT	Error recovery
18	PUT ▶ I(0)₁ ['00 B2 03 04 00'] ▶ LT	Loop-back
19	PUT ◀ I(0)₁ ['00 B2 04 04 00' + '90 00'] with a transmission error (i.e. CRC error) in function of x ◀ LT	Error
20	PUT ▶ R(NAK)₁ ▶ LT	Request for Block repetition
21	PUT ◀ I(0)₁ ['00 B2 04 04 00' + '90 00'] with a transmission error (i.e. CRC error) in function of x ◀ LT	Error
22	PUT ▶ R(NAK)₁ sent after FDT_{B,PCD,MIN} and within t_{RETRANSMISSION} ▶ LT	Request for Block repetition
23	PUT ◀ I(0)₁ ['00 B2 04 04 00' + '90 00'] ◀ LT	Error recovery
24	PUT ▶ I(0)₀ ['00 B2 04 04 00'] ▶ LT	Loop-back
25	PUT ◀ I(0)₀ ['00 B2 05 04 00' + '90 00'] with a transmission error (i.e. CRC error) in function of x ◀ LT	Error
26	PUT ▶ R(NAK)₀ ▶ LT	Request for Block repetition

Step	Exchanges	Comments
27	PUT ↪ I(0)₀ ['00 B2 05 04 00' + '90 00'] with a transmission error (i.e. CRC error) in function of x ↪ LT	Error
28	PUT ↪ R(NAK)₀ sent after FDT_{B,PCD,MIN} and within t_{RETRANSMISSION} ↪ LT	Request for Block repetition
29	PUT ↪ I(0)₀ ['00 B2 05 04 00' + '90 00'] ↪ LT	Error recovery
30	PUT ↪ I(0)₁ ['00 B2 05 04 00'] ↪ LT	Loop-back
31	PUT ↪ I(0)₁ ['00 B2 06 04 00' + '90 00'] with a transmission error (i.e. CRC error) in function of x ↪ LT	Error
32	PUT ↪ R(NAK)₁ ↪ LT	Request for Block repetition
33	PUT ↪ I(0)₁ ['00 B2 06 04 00' + '90 00'] with a transmission error (i.e. CRC error) in function of x ↪ LT	Error
34	PUT ↪ R(NAK)₁ ↪ LT	Request for Block repetition
35	PUT ↪ I(0)₁ ['00 B2 06 04 00' + '90 00'] with a transmission error (i.e. CRC error) in function of x ↪ LT	Error
36	The PUT performs a PICC Reset (i.e. stops sending the carrier) PUT II The PICC Reset is initiated within t_{RESETDELAY} The PUT keeps the carrier off during at least t_{RESET,MIN} ↪ LT	PICC Reset

Scenario 132: Type B Transmission error in response to an I-Block not indicating chaining (x=0 and 2 to 4)

5.33.Type B Protocol error in response to an I-Block not indicating chaining [TB404.xy]

Test codification:

TB404.xy

Test objective:

To ensure that the PCD behaves correctly when it receives a protocol error in response to an I-Block not indicating chaining.

References Requirements:

4.7.3.1, 10.1.1.3, 10.2.1.1, 10.2.2.1, 10.3.4.5, 10.3.4.6, 10.3.5.4, 10.3.5.9, 10.1.2.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

xy=11 is Not Applicable if the PCD implements a legacy behavior by accepting I-Blocks with b₆ of PCB set to '1' (see ICS).

Procedure:

Run the following scenario.

The LT measures the delay between the beginning of the sequence inducing a protocol error and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

The following protocol errors are generated successively by the LT:

- xy=00: I-Block with bit b₂ of the PCB equal to '0'
- xy=01: I-Block with bit b₄ of the PCB equal to '1' (i.e. CID following)
- xy=02: I-Block with bit b₃ of the PCB equal to '1' (i.e. NAD following)
- xy=03: I-Block with wrong Block number indicated in the PCB
- xy=04: I-Block of length > FSD
- xy=05: R(NAK) Block
- xy=06: R(ACK) Block with a Block number different from the one of the last Block sent by the LT
- xy=07: S(DESELECT) response
- xy=08: S(WTX) Request with WTXM = 0
- xy=09: S(WTX) Request with WTXM = 1 and with bit b₂ of PCB equal to (0)_b
- xy=10: S(WTX) Request with WTXM = 60
- xy=11: I-Block with bit b₆ of the PCB equal to '1' (See "Conditions")
- xy=13: S(WTX) Request with b₆-b₅ of the PCB set to 01_b, with WTXM =1
- xy=14: S(WTX) Request with b₆-b₅ of the PCB set to 10_b, with WTXM =1
- xy=15: I-Block with b₈-b₇ of the PCB set to 01_b

In this test, the default Protocol Information (PI) shall be used:

PI			Comments
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT initiates a PICC Reset when it detects a protocol error after an I-Block not indicating chaining).

The delay between the beginning of the sequence inducing a protocol error and the beginning of the PICC Reset initiated by the PUT is at most $t_{RESETDELAY}$ (i.e. the PUT stops sending the carrier within $t_{RESETDELAY}$).

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + 'B5 86 4D 12' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + 'B5 86 4D 12' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + 'B5 86 4D 12' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' ◀ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(0)₀ ['00 B2 01 04 00' + '90 00'] ◀ LT	
10	PUT ▶ I(0)₁ ['00 B2 01 04 00'] ▶ LT	Loop-back
11	Protocol error in function of 'xy' For xy=00: I(0) ₁ ['00 B2 02 04 00' + '90 00'] with b ₂ =0 in PCB For xy=01: I(0) ₁ ['00 B2 02 04 00' + '90 00'] with b ₄ =1 in PCB For xy=02: I(0) ₁ ['00 B2 02 04 00' + '90 00'] with b ₃ =1 in PCB For xy=03: I(0) ₀ ['00 B2 02 04 00' + '90 00'] For xy=04: I(0) ₁ ['00 A4 04 00 F7' + '00 ... F6' + '00' + '90 00'] For xy=05: R(NAK)1 For xy=06: R(ACK)1 For xy=07: S(DESELECT) response PUT ◀ For xy=08: S(WTX Request) [WTXM='00'] ◀ LT For xy=09: S(WTX Request) [WTXM='01'] and bit b ₂ of PCB equal to (0) _b For xy=10: S(WTX Request) [WTXM='3C'] For xy=11 - (See "Conditions"): I(0) ₁ ['00 B2 02 04 00' + '90 00'] with b ₆ =1 in PCB For xy=13: S(WTX Request) with b ₆ -b ₅ set to 01 _b in PCB, with WTXM =1 For xy=14: S(WTX Request) with b ₆ -b ₅ set to 10 _b in PCB, with WTXM =1 For xy=15: I(0) ₁ ['00 B2 02 04 00' + '90 00'] with b ₈ -b ₇ set to 01 _b in PCB	Error in function of 'xy'
12	The PUT performs a PICC Reset (i.e. stops sending the carrier) PUT II The PICC Reset is initiated within t _{RESETDELAY} The PUT keeps the carrier off during at least t _{RESET,MIN}	PICC Reset

Scenario 133: Type B Protocol error in response to an I-Block not indicating chaining (xy=00 to 11, 13 to 15)

5.34.Type B Error notification on an I-Block indicating chaining [TB405.xy]

Test codification:

TB405.xy

Test objective:

To ensure that the PCD behaves correctly when it receives an error notification on an I-Block indicating chaining.

References Requirements:

4.8.1.8, 10.3.4.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

For each error notification during block protocol, the LT measures the delay between the end of the sequence on which the LT signals an error and the beginning of the next sequence sent by the PUT to process the time-out error.

In this test, the following Protocol Information (PI) shall be used:

PI				(FWT+ΔFWT)
	Byte 1	Byte 2	Byte 3	
x=00	'80'	'21'	'01'	53248 x 1/f _c
x=01	'80'	'21'	'11'	57344 x 1/f _c
x=02	'80'	'21'	'21'	65536 x 1/f _c
x=03	'80'	'21'	'31'	81920 x 1/f _c
x=04	'80'	'21'	'41'	114688 x 1/f _c (default value)
x=05	'80'	'21'	'51'	180224 x 1/f _c
x=06	'80'	'21'	'61'	311296 x 1/f _c
x=07	'80'	'21'	'71'	573440 x 1/f _c
x=08	'80'	'21'	'81'	1097728 x 1/f _c
x=09	'80'	'21'	'91'	2146304 x 1/f _c
x=10	'80'	'21'	'A1'	4243456 x 1/f _c
x=11	'80'	'21'	'B1'	8437760 x 1/f _c
x=12	'80'	'21'	'C1'	16826368 x 1/f _c
x=13	'80'	'21'	'D1'	33603584 x 1/f _c
x=14	'80'	'21'	'E1'	67158016 x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT retransmits the I-Block on which is notified an error).

For each error notification, the delay between the end of the sequence sent by the PUT to which the LT does not respond and the beginning of the sequence sent by the PUT to process the time-out error is at most [(FWT+ΔFWT) + t_{RETRANSMISSION}].

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ↴ '50' + '6E B4 5A 89' + '00 00 00 00' + PI ↴ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ↴ '50' + '6E B4 5A 89' + '00 00 00 00' + PI ↴ LT	ATQB
6	PUT ▶ '1D' + '6E B4 5A 89' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ↴ '00' ↴ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ↴ I(0)₀ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00'] ↴ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 3B' + '01 02 ... 18'] ▶ LT	Loop-back
11	PUT ▶ R(NAK)₁ sent within [(FWT+ ΔFWT) + t_{RETRANSMISSION}] in function of 'xy' ▶ LT	Time-out error notification
12	PUT ↴ R(ACK)₀ ↴ LT	Request for Block repetition
13	PUT ▶ I(1)₁ ['00 A4 04 00 3B' + '01 02 ... 18'] ▶ LT	Error recovery
14	PUT ↴ R(ACK)₁ ↴ LT	Acknowledgment R-Block
15	PUT ▶ I(1)₀ ['19 1A 1B ... 33 34 35'] ▶ LT	Loop-back
16	PUT ▶ R(NAK)₀ sent within [(FWT+ ΔFWT) + t_{RETRANSMISSION}] in function of 'xy' ▶ LT	Time-out error notification
17	PUT ↴ R(ACK)₁ ↴ LT	Request for Block repetition
18	PUT ▶ I(1)₀ ['19 1A 1B ... 33 34 35'] ▶ LT	Error recovery
19	PUT ↴ R(ACK)₀ ↴ LT	Acknowledgment R-Block
20	PUT ▶ I(0)₁ ['36 37 38 39 3A 3B' + '00'] ▶ LT	Last I-Block of the chain
21	PUT ↴ I(0)₁ ["EOT Command" + '90 00'] ↴ LT	End Of Test command

Step	Exchanges	Comments
22	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
23	PUT ▶ '05 00 08'	▶ LT WUPB to poll for the PICC
24	PUT ▶ '05 00 08'	▶ LT WUPB to poll for the PICC
25	PUT ▶ '05 00 08'	▶ LT WUPB to poll for the PICC

Scenario 134: Type B Error notification on an I-Block indicating chaining (xy=00 to 14)

5.35.Type B Time-out after an I-Block indicating chaining [TB406]

Test codification:

TB406

Test objective:

To ensure that the PCD behaves correctly when it does not receive any response to an I-Block indicating chaining.

References Requirements:

4.8.1.8, 10.3.4.3, 10.3.5.8

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

When a single time-out error is generated, the LT measures the delay between the end of the sequence with sent by the PUT before the time-out error and the beginning of the next sequence sent by the PUT to process the error.

When three consecutive time-out errors are generated, the LT measures the delay between the end of the sequence preceding the third time-out and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

In this test, the default Protocol Information (PI) shall be used:

PI			FWT+ΔFWT
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	114688 x 1/f _c (default value)

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends an R(NAK) Block to ask for retransmission when it detects a time-out error after an I-Block indicating chaining).

When a single time-out error is generated, the delay between the end of the sequence with sent by the PUT before the time-out error and the beginning of the next sequence sent by the PUT to process the error is at least FWT+ ΔFWT and at most t_{TIMEOUT} + t_{RETRANSMISSION} = FWT+ ΔFWT + t_{RETRANSMISSION}.

When three consecutive transmission errors are generated, the delay between the end of the sequence preceding the third time-out and the beginning of the PICC Reset initiated by the PUT is at least FWT+ ΔFWT at most t_{TIMEOUT} + t_{RESETDELAY} = FWT+ ΔFWT + t_{RESETDELAY}.

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + '50 50 50 50' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + '50 50 50 50' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + '50 50 50 50' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' ◀ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(0)₀ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00'] ◀ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 3B' + '01 02 ... 18'] ▶ LT	Loop-back
11	PUT ▶ R(NAK)₁ sent after FWT+ ΔFWT and before [(FWT+ ΔFWT) + t _{RETRANSMISSION}] ▶ LT	Time-out error notification
12	PUT ◀ R(ACK)₁ ◀ LT	Error recovery
13	PUT ▶ I(1)₀ ['19 1A 1B ... 33 34 35'] ▶ LT	Loop-back
14	PUT ▶ R(NAK)₀ sent after FWT+ ΔFWT and before [(FWT+ ΔFWT) + t _{RETRANSMISSION}] ▶ LT	Time-out error notification
15	PUT ◀ R(ACK)₀ ◀ LT	Error recovery
16	PUT ▶ I(0)₁ ['36 37 38 39 3A 3B' + '00'] ▶ LT	Last I-Block of the chain
17	PUT ◀ I(0)₁ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00'] ◀ LT	
18	PUT ▶ I(1)₀ ['00 A4 04 00 3B' + '01 02 ... 18'] ▶ LT	Loop-back
19	PUT ▶ R(NAK)₀ ▶ LT	Request for Block repetition
20	PUT ▶ R(NAK)₀ ▶ LT	Request for Block repetition
21	<p>The PUT performs a PICC Reset (i.e. stops sending the carrier)</p> <p>PUT II The PICC Reset is initiated after FWT+ ΔFWT and before FWT+ ΔFWT + t_{RESETDELAY}</p> <p>The PUT keeps the carrier off during at least $t_{RESET,MIN}$</p>	II LT PICC Reset

Scenario 135: Type B Time-out after an I-Block indicating chaining

5.36.Type B Transmission error in response to an I-Block indicating chaining [TB407]

Test codification:

TB407

Test objective:

To ensure that the PCD behaves correctly when it receives a sequence with transmission error in response to an I-Block indicating chaining.

References Requirements:

6.2.1.1, 6.2.1.2, 10.3.5.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

When a single transmission error is generated, the LT measures the delay between the beginning of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When a single transmission error is generated, the LT measures the delay between the end of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When three consecutive transmission errors are generated, the LT measures the delay between the beginning of the third sequence with transmission error and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The LT measures the time during which the PUT stops sending the carrier to perform a PICC Reset.

The following transmission error is generated by the LT: I-Block of at least 4 bytes preceded by the minimum synchronization time TR1_{MIN} (with subcarrier on but no modulation) and with some residual bits (i.e. the total number of bits is not a multiple of 8) followed by no modulation (no EoS).

In this test, the default Protocol Information (PI) shall be used:

PI			Comments
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends an R(NAK) Block when it detects a transmission error after an I-Block indicating chaining and continues the transaction upon receipt of a correct block).

When a single transmission error is generated, the delay between the end of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at least $FDT_{B,PCD,MIN}$.

When a single transmission error is generated, the delay between the beginning of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at most $t_{RETRANSMISSION}$.

When three consecutive transmission errors are generated, the delay between the beginning of the third sequence with transmission error and the beginning of the PICC Reset initiated by the PUT is at most $t_{RESETDELAY}$ (i.e. the PUT stops sending the carrier within $t_{RESETDELAY}$).

The time during which the PUT stops sending the carrier to perform a PICC Reset is at least $t_{RESET,MIN}$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ▲ '50' + '48 0E BA 83' + '00 00 00 00' + PI ▲ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ▲ '50' + '48 0E BA 83' + '00 00 00 00' + PI ▲ LT	ATQB
6	PUT ▶ '1D' + '48 0E BA 83' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ▲ '00' ▲ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ▲ I(0)₀ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00'] ▲ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 3B' + '01 02 ... 18'] ▶ LT	Loop-back
11	PUT ▲ I(0)₁ ['00 B2 01 04 00' + '90 00'] with 3 bits to (101)_b following the CRC bytes ▲ LT	Error
12	PUT ▶ R(NAK)₁ sent after FDT_{B,PCD,MIN} and within t_{RETRANSMISSION} ▶ LT	Request for Block repetition
13	PUT ▲ R(ACK)₁ ▲ LT	Error recovery
14	PUT ▶ I(1)₀ ['19 1A 1B ... 33 34 35'] ▶ LT	Loop-back
15	PUT ▲ I(0)₁ ['00 B2 01 04 00' + '90 00'] with 3 bits to (101)_b following the CRC bytes ▲ LT	Error
16	PUT ▶ R(NAK)₀ sent after FDT_{B,PCD,MIN} and within t_{RETRANSMISSION} ▶ LT	Request for Block repetition
17	PUT ▲ R(ACK)₀ ▲ LT	Error recovery
18	PUT ▶ I(0)₁ ['36 37 38 39 3A 3B' + '00'] ▶ LT	Last I-Block of the chain
19	PUT ▲ I(0)₁ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00'] ▲ LT	
20	PUT ▶ I(1)₀ ['00 A4 04 00 3B' + '01 02 ... 18'] ▶ LT	Loop-back

Step	Exchanges	Comments
21	PUT ↪ I(0)1 ['00 B2 01 04 00' + '90 00'] with 3 bits to (101)_b following the CRC bytes ↮ LT	Error
22	PUT ↪ R(NAK)₀ ↮ LT	Request for Block repetition
23	PUT ↪ I(0)1 ['00 B2 01 04 00' + '90 00'] with 3 bits to (101)_b following the CRC bytes ↮ LT	Error
24	PUT ↪ R(NAK)₀ ↮ LT	Request for Block repetition
25	PUT ↪ I(0)1 ['00 B2 01 04 00' + '90 00'] with 3 bits to (101)_b following the CRC bytes ↮ LT	Error
26	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) The PICC Reset is initiated within tRESETDELAY The PUT keeps the carrier off during at least tRESET,MIN	PICC Reset

Scenario 136: Type B Transmission error in response to an I-Block indicating chaining

5.37.Type B Protocol error in response to an I-Block indicating chaining [TB408.xy]

Test codification:

TB408.xy

Test objective:

To ensure that the PCD behaves correctly when it receives a protocol error in response to an I-Block indicating chaining.

References Requirements:

10.1.5.1, 10.2.1.1, 10.2.2.1, 10.3.4.6, 10.3.5.7, 10.3.5.9, 10.1.2.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

xy=09 is Not Applicable if the PCD implements a legacy behavior by accepting R-Blocks with b₂ of PCB set to '0' (see ICS).

Procedure:

Run the following scenario.

The LT measures the delay between the beginning of the sequence inducing a protocol error and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The following protocol errors are generated successively by the LT:

- xy=00: R(ACK) Block with bit b₆ of the PCB equal to '0'
- xy=01: R(NAK) Block (b₅=1 in PCB)
- xy=02: R(ACK) Block with bit b₄ of the PCB equal to '1' (i.e. CID following)
- xy=03: R(ACK) Block with bit b₃ of the PCB equal to '1' (i.e. NAD following)
- xy=04: I-Block
- xy=05: S(DESELECT) response
- xy=06: S(WTX) Request with WTXM = 0
- xy=07: S(WTX) Request with WTXM = 1 and with bit b₂ of PCB equal to (0)_b
- xy=08: S(WTX) Request with WTXM = 63
- xy=09: R(ACK) Block with bit b₂ of the PCB equal to '0' (See "Conditions")
- xy=11: S(WTX) Request with b₆-b₅ of the PCB set to 01_b, with WTXM =1
- xy=12: S(WTX) Request with b₆-b₅ of the PCB set to 10_b, with WTXM =1

In this test, the default Protocol Information (PI) shall be used:

PI			Comments
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT initiates a PICC Reset when it detects a protocol error after an I-Block indicating chaining).

The delay between the beginning of the sequence inducing a protocol error and the beginning of the PICC Reset initiated by the PUT is at most $t_{RESETDELAY}$ (i.e. the PUT stops sending the carrier within $t_{RESETDELAY}$).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + '9D C1 AC 10' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + '9D C1 AC 10' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + '9D C1 AC 10' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' ◀ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(0)₀ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00'] ◀ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 3B' + '01 02 ... 18'] ▶ LT	Loop-back
11	Protocol error in function of 'x' For xy=00: R(ACK) ₁ with b ₆ =0 in PCB For xy=01: R(NAK) ₁ For xy=02: R(ACK) ₁ with b ₄ =1 in PCB For xy=03: R(ACK) ₁ with b ₃ =1 in PCB For xy=04: I(0) ₀ ['00 B2 01 04 00' + '90 00'] For xy=05: S(DESELECT) response PUT ◀ For xy=06: S(WTX Request) [WTXM='00'] ◀ LT For xy=07: S(WTX Request) [WTXM='01'] and bit b ₂ of PCB equal to (0) _b For xy=08: S(WTX Request) [WTXM='3F'] For xy=09: R(ACK) ₁ with b ₂ =0 in PCB (See "Conditions") For xy=11: S(WTX Request) with b ₆ -b ₅ set to 01b in PCB, with WTXM =1 For xy=12: S(WTX Request) with b ₆ -b ₅ set to 10b in PCB, with WTXM =1	Error in function of 'xy'
12	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) The PICC Reset is initiated within t _{RESETDELAY}	II LT PICC Reset

Scenario 137: Type B Protocol error in response to an I-Block indicating chaining (xy=00 to 09, 11 to 12)

5.38.Type B Time-out after an R(ACK) Block (i.e. error notification) [TB409.xy]

Test codification:

TB409.xy

Test objective:

To ensure that the PCD behaves correctly when it does not receive any response to an R(ACK) Block sent to acknowledge a chained I-Block.

References Requirements:

4.8.1.8, 10.3.5.9

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

When a single time-out error is generated, the LT measures the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

When two consecutive time-out errors are generated, the LT measures the delay between the end of the second sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

When three consecutive time-out errors are generated, the LT measures the delay between the end of the third sequence to which the LT does not respond and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

In this test, the following Protocol Information (PI) shall be used:

PI				(FWT+ΔFWT)
	Byte 1	Byte 2	Byte 3	
x=00	'80'	'21'	'01'	53248 x 1/f _c
x=01	'80'	'21'	'11'	57344 x 1/f _c
x=02	'80'	'21'	'21'	65536 x 1/f _c
x=03	'80'	'21'	'31'	81920 x 1/f _c
x=04	'80'	'21'	'41'	114688 x 1/f _c (default value)
x=05	'80'	'21'	'51'	180224 x 1/f _c
x=06	'80'	'21'	'61'	311296 x 1/f _c
x=07	'80'	'21'	'71'	573440 x 1/f _c
x=08	'80'	'21'	'81'	1097728 x 1/f _c
x=09	'80'	'21'	'91'	2146304 x 1/f _c

	PI			$(FWT + \Delta FWT)$
	Byte 1	Byte 2	Byte 3	
x=10	'80'	'21'	'A1'	$4243456 \times 1/f_c$
x=11	'80'	'21'	'B1'	$8437760 \times 1/f_c$
x=12	'80'	'21'	'C1'	$16826368 \times 1/f_c$
x=13	'80'	'21'	'D1'	$33603584 \times 1/f_c$
x=14	'80'	'21'	'E1'	$67158016 \times 1/f_c$
x=15	'80'	'21'	'F1'	$114688 \times 1/f_c$

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT retransmits the R(ACK) Block up to two times when it detects a time-out error after an R(ACK) Block and initiates a PICC Reset when it detects a third consecutive time-out error).

When a single time-out error is generated, the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at most $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$.

When two consecutive time-out errors are generated, the delay between the end of the second sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at most $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$.

When three consecutive time-out errors are generated, the delay between the end of the third sequence to which the LT does not respond and the beginning of the PICC Reset initiated by the PUT is at most $[(FWT + \Delta FWT) + t_{RESETDELAY}]$ (i.e. the PUT stops sending the carrier within $[(FWT + \Delta FWT) + t_{RESETDELAY}]$).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ▲ '50' + '34 DA 39 B7' + '00 00 00 00' + PI ▲ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ▲ '50' + '34 DA 39 B7' + '00 00 00 00' + PI ▲ LT	ATQB
6	PUT ▶ '1D' + '34 DA 39 B7' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ▲ '00' ▲ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ▲ I(1)₀ ['00 A4 04 00 50' + '01 02 03 ... 06 07 08'] ▲ LT	
10	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgment R-Block

Step	Exchanges	Comments
11	PUT ▶ R(ACK)₁ sent within $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$ in function of 'xy' ▶ LT	Time-out error notification
12	PUT ◀ I(1)₁ ['09 0A 0B ... 13 14 15'] ◀ LT	Error recovery
13	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgment R-Block
14	PUT ▶ R(ACK)₀ sent within $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$ in function of 'xy' ▶ LT	Time-out error notification
15	PUT ◀ I(1)₀ ['16 17 18 ... 20 21 22'] ◀ LT	Error recovery
16	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgment R-Block
17	PUT ▶ R(ACK)₁ ▶ LT	Time-out error notification
18	PUT ▶ R(ACK)₁ sent within $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$ in function of 'xy' ▶ LT	Time-out error notification
19	PUT ◀ I(1)₁ ['23 24 25 ... 2D 2E 2F'] ◀ LT	Error recovery
20	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgment R-Block
21	PUT ▶ R(ACK)₀ ▶ LT	Time-out error notification
22	PUT ▶ R(ACK)₀ sent within $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$ in function of 'xy' ▶ LT	Time-out error notification
23	PUT ◀ I(1)₀ ['30 31 32 ... 3A 3B 3C'] ◀ LT	Error recovery
24	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgment R-Block
25	PUT ▶ R(ACK)₁ ▶ LT	Time-out error notification
26	PUT ▶ R(ACK)₁ ▶ LT	Time-out error notification
27	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) The PICC Reset is initiated within $[(FWT + \Delta FWT) + t_{RESETDELAY}]$ in function of 'xy'	II LT PICC Reset

Scenario 138: Type B Time-out after an R(ACK) Block (i.e. error notification) (xy=00 to 15)

5.39.Type B Transmission error in response to an R(ACK) Block [TB410.x]

Test codification:

TB410.x

Test objective:

To ensure that the PCD behaves correctly when it receives a transmission error in response to an R(ACK) Block sent to acknowledge a chained I-Block.

References Requirements:

6.2.1.1, 6.2.1.2, 10.3.5.6, 10.3.5.9

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

When a single transmission error is generated, the LT measures the delay between the beginning of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When a single transmission error is generated, the LT measures the delay between the end of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When two consecutive transmission errors are generated, the LT measures the delay between the beginning of the second sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When two consecutive transmission errors are generated, the LT measures the delay between the end of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error.

When three consecutive transmission errors are generated, the LT measures the delay between the beginning of the third sequence with transmission error and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The following transmission error is generated by the LT:

- x=0: I-Block (in a frame of at least 4 bytes) with CRC error: the less significant bit of the 1st CRC byte is corrupted for the 1st, 4th and 7th error generated, the less significant bit of the 2nd CRC byte is corrupted for the 2nd, 5th and 8th error generated and the most significant bit of the 2nd CRC byte is corrupted for the 3rd, 6th and 9th error generated
- x=1: I-Block of at least 4 bytes preceded by the minimum synchronization time TR1_{MIN} (with subcarrier on but no modulation) and with some residual bits (i.e. the total number of bits is not a multiple of 8) followed by no modulation (no EoS)

In this test, the default Protocol Information (PI) shall be used:

PI			Maximum Frame Size for the PICC (FSC)
Byte 1	Byte 2	Byte 3	
'80'	'81'	'41'	256 bytes

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT retransmits the R(ACK) Block up to two times when it detects a transmission error and initiates a PICC Reset when it detects a third consecutive transmission error).

When a single transmission error is generated, the delay between the end of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at least $FDT_{B,PCD,MIN}$.

When a single transmission error is generated, the delay between the beginning of the sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at most $t_{RETRANSMISSION}$.

When two consecutive transmission errors are generated, the delay between the end of the second sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at least $FDT_{B,PCD,MIN}$.

When two consecutive transmission errors are generated, the delay between the beginning of the second sequence with transmission error and the beginning of the sequence replied by the PUT to process the error is at most $t_{RETRANSMISSION}$.

When three consecutive transmission errors are generated, the delay between the beginning of the third sequence with transmission error and the beginning of the PICC Reset initiated by the PUT is at most $t_{RESETDELAY}$ (i.e. the PUT stops sending the carrier within $t_{RESETDELAY}$).

The delay between the end of a sequence sent by the LT and the beginning of the sequence replied by the PUT is at least $FDT_{B,PCD,MIN}$ during installation and block protocol.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + '53 26 C9 E4' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + '53 26 C9 E4' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + '53 26 C9 E4' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' ◀ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(1)₀ ['00 A4 04 00 50' + '01 02 03 ... 06 07 08'] ◀ LT	
10	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgement R-Block
11	PUT ◀ I(1)₁ ['09 0A 0B ... 13 14 15'] ◀ LT with a transmission error in function of x	Error
12	PUT ▶ R(ACK)₁ sent after FDT_{B,PCD,MIN} and within t_{RETRANSMISSION} ▶ LT	Error notification
13	PUT ◀ I(1)₁ ['09 0A 0B ... 13 14 15'] ◀ LT	Error recovery
14	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgement R-Block
15	PUT ◀ I(1)₀ ['16 17 18 ... 20 21 22'] ◀ LT with a transmission error in function of x	Error
16	PUT ▶ R(ACK)₀ sent after FDT_{B,PCD,MIN} and within t_{RETRANSMISSION} ▶ LT	Error notification
17	PUT ◀ I(1)₀ ['16 17 18 ... 20 21 22'] ◀ LT	Error recovery
18	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgement R-Block
19	PUT ◀ I(1)₁ ['23 24 25 ... 2D 2E 2F'] ◀ LT with a transmission error in function of x	Error
20	PUT ▶ R(ACK)₁ ▶ LT	Error notification
21	PUT ◀ I(1)₁ ['23 24 25 ... 2D 2E 2F'] ◀ LT with a transmission error in function of x	Error
22	PUT ▶ R(ACK)₁ sent after FDT_{B,PCD,MIN} and within t_{RETRANSMISSION} ▶ LT	Error notification
23	PUT ◀ I(1)₁ ['23 24 25 ... 2D 2E 2F'] ◀ LT	Error recovery
24	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgement R-Block
25	PUT ◀ I(1)₀ ['30 31 32 ... 3A 3B 3C'] ◀ LT with a transmission error in function of x	Error

Step	Exchanges	Comments
26	PUT ▶ R(ACK)₀ ▶ LT	Error notification
27	PUT ↵ I(1)₀ ['30 31 32 ... 3A 3B 3C'] with a transmission error in function of x ↶ LT	Error
28	PUT ▶ R(ACK)₀ sent after FDT _{B,PCD,MIN} and within t _{RETRANSMISSION} ▶ LT	Error notification
29	PUT ↵ I(1)₀ ['30 31 32 ... 3A 3B 3C'] ↶ LT	Error recovery
30	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgement R-Block
31	PUT ↵ I(1)₁ ['3D 3E 3F ... 47 48 49'] with a transmission error in function of x ↶ LT	Error
32	PUT ▶ R(ACK)₁ ▶ LT	Error notification
33	PUT ↵ I(1)₁ ['3D 3E 3F ... 47 48 49'] with a transmission error in function of x ↶ LT	Error
34	PUT ▶ R(ACK)₁ ▶ LT	Error notification
35	PUT ↵ I(1)₁ ['3D 3E 3F ... 47 48 49'] with a transmission error in function of x ↶ LT	Error
36	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) The PICC Reset is initiated within t _{RESETDELAY} II LT	PICC Reset

Scenario 139: Type B Transmission error in response to an R(ACK) Block (x=0 to 1)

5.40.Type B Protocol error in response to an R(ACK) Block [TB411.xy]

Test codification:

TB411.xy

Test objective:

To ensure that the PCD behaves correctly when it receives a protocol error in response to an R(ACK) Block sent to acknowledge a chained I-Block.

References Requirements:

4.7.3.1, 10.1.1.3, 10.1.5.1, 10.2.1.1, 10.2.2.1, 10.3.4.5, 10.3.4.6, 10.3.5.4, 10.3.5.9, 10.1.2.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

xy=11 is Not Applicable if the PCD implements a legacy behavior by accepting I-Blocks with b₆ of PCB set to '1' (see ICS).

Procedure:

Run the following scenario.

The LT measures the delay between the beginning of the sequence inducing a protocol error and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The following protocol errors are generated successively by the LT:

- xy=00: I-Block with bit b₂ of the PCB equal to '0'
- xy=01: I-Block with bit b₄ of the PCB equal to '1' (i.e. CID following)
- xy=02: I-Block with bit b₃ of the PCB equal to '1' (i.e. NAD following)
- xy=03: I-Block with wrong Block number indicated in the PCB
- xy=04: I-Block of length > FSD
- xy=05: R(NAK) Block
- xy=06: R(ACK) Block with a Block number different from the one of the last Block from the LT
- xy=07: S(DESELECT) response
- xy=08: S(WTX) Request with WTXM = 0
- xy=09: S(WTX) Request with WTXM = 1 and with bit b₂ of PCB equal to (0)_b
- xy=10: S(WTX) Request with WTXM = 61
- xy=11: I-Block with bit b₆ of the PCB equal to '1' (See "Conditions")
- xy=13: S(WTX) Request with b₆-b₅ of the PCB set to 01_b, with WTXM =1
- xy=14: S(WTX) Request with b₆-b₅ of the PCB set to 10_b, with WTXM =1
- xy=15: I-Block with b₈-b₇ of the PCB set to 01_b

In this test, the default Protocol Information (PI) shall be used:

PI			Maximum Frame Size for the PICC (FSC)
Byte 1	Byte 2	Byte 3	
'80'	'81'	'41'	256 bytes

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT initiates a PICC Reset when it detects a protocol error after an R(ACK) Block).

The delay between the beginning of the sequence inducing a protocol error and the beginning of the PICC Reset initiated by the PUT is at most $t_{RESETDELAY}$ (i.e. the PUT stops sending the carrier within $t_{RESETDELAY}$).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + '22 29 75 92' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + '22 29 75 92' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + '22 29 75 92' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' ◀ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(1)₀ ['00 A4 04 00 14' + '01 02 03 ... 06 07 08'] ◀ LT	
10	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgement R-Block
11	Protocol error in function of 'x' For xy=00: I(0) ₁ ['00 B2 02 04 00' + '90 00'] with b ₂ =0 in PCB For xy=01: I(0) ₁ ['00 B2 02 04 00' + '90 00'] with b ₄ =1 in PCB For xy=02: I(0) ₁ ['00 B2 02 04 00' + '90 00'] with b ₃ =1 in PCB For xy=03: I(0) ₀ ['00 B2 02 04 00' + '90 00'] For xy=04: I(0) ₁ ['00 A4 04 00 F7' + '00 ... F6' + '00' + '90 00'] For xy=05: R(NAK) ₁ For xy=06: R(ACK) ₁ For xy=07: S(DESELECT) response PUT ◀ For xy=08: S(WTX Request) [WTXM='00'] ◀ LT Error in function of 'xy' For xy=09: S(WTX Request) [WTXM='01'] and bit b ₂ of PCB equal to (0) _b For xy=10: S(WTX Request) [WTXM='3D'] For xy=11 - (See "Conditions"): I(0) ₁ ['00 B2 02 04 00' + '90 00'] with b ₆ =1 in PCB For xy=13: Block with with b ₈ -b ₇ set to 01 _b in PCB, with WTXM =1 For xy=14: Block with with b ₆ -b ₅ set to 10 _b in PCB, with WTXM =1 For xy=15: I(0) ₁ ['00 B2 02 04 00' + '90 00'] with b ₈ -b ₇ set to 01 _b	
12	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) The PICC Reset is initiated within t _{RESETDELAY} II LT	PICC Reset

Scenario 140: Type B Protocol error in response to an R(ACK) Block (xy=00 to 11, 13 to 15)

5.41.Type B Single time-out after an S(WTX) Response Block (several values of WTXM) [TB412.xy]

Test codification:

TB412.xy

Test objective:

To ensure that the PCD behaves correctly when it does not receive any response to a S(WTX) Response Block.

References Requirements:

10.2.2.7, 10.3.5.5

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

For each time-out error generated, the LT measures the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

In this test, the following Protocol Information (PI) shall be used:

	PI			(FWT+ΔFWT)
	Byte 1	Byte 2	Byte 3	
x=00	'80'	'21'	'01'	53248 x 1/f _c
x=01	'80'	'21'	'11'	57344 x 1/f _c
x=02	'80'	'21'	'21'	65536 x 1/f _c
x=03	'80'	'21'	'31'	81920 x 1/f _c
x=04	'80'	'21'	'41'	114688 x 1/f _c (default value)
x=05	'80'	'21'	'51'	180224 x 1/f _c
x=06	'80'	'21'	'61'	311296 x 1/f _c
x=07	'80'	'21'	'71'	573440 x 1/f _c
x=08	'80'	'21'	'81'	1097728 x 1/f _c
x=09	'80'	'21'	'91'	2146304 x 1/f _c
x=10	'80'	'21'	'A1'	4243456 x 1/f _c
x=11	'80'	'21'	'B1'	8437760 x 1/f _c
x=12	'80'	'21'	'C1'	16826368 x 1/f _c
x=13	'80'	'21'	'D1'	33603584 x 1/f _c
x=14	'80'	'21'	'E1'	67158016 x 1/f _c

The corresponding extended Frame Waiting Time is as follows:

- $FWT_{EXT} + \Delta FWT = (FWT_{EXT} \times WTXM) + \Delta FWT$ with $FWT \times WTXM \leq FWT_{MAX}$

And we define:

- $FWT_{EXT1} + \Delta FWT$ corresponding to $WTXM_1$
- $FWT_{EXT2} + \Delta FWT$ corresponding to $WTXM_2$
- $FWT_{EXT3} + \Delta FWT$ corresponding to $WTXM_3$

Which leads to:

xy	WTXM₁	FWT_{EXT1+ΔFWT}	WTXM₂	FWT_{EXT2+ΔFWT}	WTXM₃	FWT_{EXT3+ΔFWT}
00	59	$290816 \times 1/f_c$	57	$282624 \times 1/f_c$	56	$278528 \times 1/f_c$
01	59	$532480 \times 1/f_c$	54	$491520 \times 1/f_c$	51	$466944 \times 1/f_c$
02	58	$999424 \times 1/f_c$	55	$950272 \times 1/f_c$	53	$917504 \times 1/f_c$
03	52	$1753088 \times 1/f_c$	50	$1687552 \times 1/f_c$	48	$1622016 \times 1/f_c$
04	47	$3129344 \times 1/f_c$	45	$2998272 \times 1/f_c$	42	$2801664 \times 1/f_c$
05	40	$5292032 \times 1/f_c$	38	$5029888 \times 1/f_c$	36	$4767744 \times 1/f_c$
06	35	$9224192 \times 1/f_c$	33	$8699904 \times 1/f_c$	30	$7913472 \times 1/f_c$
07	29	$15253504 \times 1/f_c$	27	$14204928 \times 1/f_c$	26	$13680640 \times 1/f_c$
08	25	$26263552 \times 1/f_c$	22	$23117824 \times 1/f_c$	20	$21020672 \times 1/f_c$
09	18	$37797888 \times 1/f_c$	15	$31506432 \times 1/f_c$	12	$25214976 \times 1/f_c$
10	10	$41992192 \times 1/f_c$	9	$37797888 \times 1/f_c$	8	$33603584 \times 1/f_c$
11	7	$58769408 \times 1/f_c$	6	$50380800 \times 1/f_c$	5	$41992192 \times 1/f_c$
12	4	$67158016 \times 1/f_c$	3	$50380800 \times 1/f_c$	2	$33603584 \times 1/f_c$
13	2	$67158016 \times 1/f_c$	2	$67158016 \times 1/f_c$	1	$33603584 \times 1/f_c$
14	1	$67158016 \times 1/f_c$	1	$67158016 \times 1/f_c$	1	$67158016 \times 1/f_c$

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends an R(NAK) Block to ask for retransmission when it detects a time-out error after an S(WTX) Response).

At step 13 of the following scenario, the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at most $[FWT_{EXT1} + \Delta FWT + t_{RETRANSMISSION}]$.

At step 18 of the following scenario, the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at most $[FWT_{EXT2} + \Delta FWT + t_{RETRANSMISSION}]$.

At step 23 of the following scenario, the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error is at most $[FWT_{EXT3} + \Delta FWT + t_{RETRANSMISSION}]$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + 'E3 20 03 DD' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + 'E3 20 03 DD' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + 'E3 20 03 DD' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' ◀ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(0)₀ ['00 B2 01 04 00' + '90 00'] ◀ LT	
10	PUT ▶ I(0)₁ ['00 B2 01 04 00'] ▶ LT	Loop-back
11	PUT ◀ S(WTX Request) [WTXM₁] WTXM₁ in function of 'xy' ◀ LT	WTXM ₁ in function of 'xy'
12	PUT ▶ S(WTX Response) [WTXM₁] ▶ LT	WTX acknowledgment
13	PUT ▶ R(NAK)₁ sent within [FWT_{EXT1}+ΔFWT+ t_{RETRANSMISSION}] in function of 'xy' ▶ LT	Time-out error notification
14	PUT ◀ I(0)₁ ['00 A4 04 00 05+ 'A1 A2 ... A5' + '00' + '90 00'] ◀ LT	Error recovery
15	PUT ▶ I(0)₀ ['00 A4 04 00 05+ 'A1 A2 ... A5' + '00'] ▶ LT	Loop-back
16	PUT ◀ S(WTX Request) [WTXM₂] WTXM₂ in function of 'xy' ◀ LT	WTXM ₂ in function of 'xy'
17	PUT ▶ S(WTX Response) [WTXM₂] ▶ LT	WTX acknowledgment
18	PUT ▶ R(NAK)₀ sent within [FWT_{EXT2}+ΔFWT+ t_{RETRANSMISSION}] in function of 'xy' ▶ LT	Time-out error notification
19	PUT ◀ I(0)₀ ['00 A4 04 00 05+ 'A6 A7 ... AA' + '00' + '90 00'] ◀ LT	Error recovery
20	PUT ▶ I(0)₁ ['00 A4 04 00 05+ 'A6 B7 ... AA' + '00'] ▶ LT	Loop-back
21	PUT ◀ S(WTX Request) [WTXM₃] WTXM₃ in function of 'xy' ◀ LT	WTXM ₃ in function of 'xy'
22	PUT ▶ S(WTX Response) [WTXM₃] ▶ LT	WTX acknowledgment
23	PUT ▶ R(NAK)₁ sent within [FWT_{EXT3}+ΔFWT+ t_{RETRANSMISSION}] in function of 'xy' ▶ LT	Time-out error notification
24	PUT ◀ I(0)₁ ['00 A4 04 00 05+ 'AB AC ... AF' + '00' + '90 00'] ◀ LT	Error recovery
25	PUT ▶ I(0)₀ ['00 A4 04 00 05+ 'AB AC ... AF' + '00'] ▶ LT	Loop-back
26	PUT ◀ I(0)₀ ["EOT Command" + '90 00'] ◀ LT	End Of Test command

Step	Exchanges	Comments
27	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
28	PUT ▶ '05 00 08'	▶ LT WUPB to poll for the PICC
29	PUT ▶ '05 00 08'	▶ LT WUPB to poll for the PICC
30	PUT ▶ '05 00 08'	▶ LT WUPB to poll for the PICC

Scenario 141: Type B Single time-out after an S(WTX) Response Block (i.e. several values of WTXM) (xy=00 to 14)

5.42. Type B Repeated use of a FWT extension after a single S(WTX) Request [TB413]

Test codification:

TB413

Test objective:

To ensure that the PCD applies the Frame Waiting Time Extension only until the next Block has been received.

References Requirements:

10.2.2.9, 10.3.5.5

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

After reception of a S(WTX) Response, the LT sends the next block within the extended Frame Waiting Time $FWT_{EXT} + \Delta FWT = [(4096 \times WTXM) + 49152] \times 1/f_c$ as $FWT = 4096 \times 1/f_c$ and $\Delta FWT = 49152 \times 1/f_c$.

Upon receipt of the next block sent by the PUT, the LT stays mute and exceeds the Frame Waiting Time ($FWT + \Delta FWT$) (as if the LT uses the FWT extension a 2nd time).

For each time-out error generated, the LT measures the delay between the end of the sequence to which the LT does not respond and the beginning of the next sequence sent by the PUT to process the time-out error.

In this test, the following Protocol Information (PI) and Frame Waiting Time shall be used:

PI			(FWT+ΔFWT)
Byte 1	Byte 2	Byte 3	
'80'	'21'	'01'	$53248 \times 1/f_c$

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends an R(NAK) Block to signal an error when the LT uses the Frame Waiting Time Extension a second consecutive time).

When a time-out error is generated, the delay between the end of the sequence to which the LT does not respond and the beginning of the sequence sent by the PUT to process the time-out is at most $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08'	▶ LT WUPB during polling
2	PUT ◀ '50' + '14 18 AC BC' + '00 00 00 00' + PI	◀ LT ATQB
3	PUT ▶ '52' (Type A short frame)	▶ LT WUPA
4	PUT ▶ '05 00 08'	▶ LT WUPB
5	PUT ◀ '50' + '14 18 AC BC' + '00 00 00 00' + PI	◀ LT ATQB
6	PUT ▶ '1D' + '14 18 AC BC' + '00 08 01 00'	▶ LT ATTRIB
7	PUT ◀ '00'	◀ LT ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00']	▶ LT Select PPSE
9	PUT ◀ I(0)₀ ['00 B2 01 04 00' + '90 00']	◀ LT
10	PUT ▶ I(0)₁ ['00 B2 01 04 00']	▶ LT Loop-back
11	PUT ◀ S(WTX Request) [WTXM='18']	◀ LT WTXM = 24
12	PUT ▶ S(WTX Response) [WTXM='18']	▶ LT WTX acknowledgment
13	PUT ◀ I(0)₁ ['00 A4 04 00 05+ 'B1 B2 ... B5' + '00' + '90 00']	◀ LT Sent with the default FDT
14	PUT ▶ I(0)₀ ['00 A4 04 00 05+ 'B1 B2 ... B5' + '00']	▶ LT Loop-back
15	PUT ▶ R(NAK)₀ sent within [(FWT+ΔFWT) + t_{RETRANSMISSION}]	▶ LT Time-out error notification
16	PUT ◀ I(0)₀ ['00 A4 04 00 05' + 'B6 B7 ... BA' + '00' + '90 00']	◀ LT Error recovery
17	PUT ▶ I(0)₁ ['00 A4 04 00 05' + 'B6 B7 ... BA' + '00']	▶ LT Loop-back
18	PUT ◀ S(WTX Request) [WTXM='2E']	◀ LT WTXM = 46
19	PUT ▶ S(WTX Response) [WTXM='2E']	▶ LT WTX acknowledgment
20	PUT ◀ I(0)₁ ['00 A4 04 00 05+ 'BB BC ... BF' + '00' + '90 00']	◀ LT Sent with the default FDT
21	PUT ▶ I(0)₀ ['00 A4 04 00 05+ 'BB BC ... BF' + '00']	▶ LT Loop-back
22	PUT ▶ R(NAK)₀ sent within [(FWT+ΔFWT) + t_{RETRANSMISSION}]	▶ LT Time-out error notification
23	PUT ◀ I(0)₀ ['00 A4 04 00 05' + 'D1 D2 ... D5' + '00' + '90 00']	◀ LT Error recovery
24	PUT ▶ I(0)₁ ['00 A4 04 00 05' + 'D1 D2 ... D5' + '00']	▶ LT Loop-back
25	PUT ◀ S(WTX Request) [WTXM='3A']	◀ LT WTXM = 58
26	PUT ▶ S(WTX Response) [WTXM='3A']	▶ LT WTX acknowledgment
27	PUT ◀ I(0)₁ ['00 A4 04 00 05+ 'D6 D7 ... DA' + '00' + '90 00']	◀ LT Sent with the default FDT
28	PUT ▶ I(0)₀ ['00 A4 04 00 05+ 'D6 D7 ... DA' + '00']	▶ LT Loop-back

Step	Exchanges		Comments
29	PUT ▶ R(NAK)₀ sent within $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$	▶ LT	Time-out error notification
30	PUT ◀ I(0)₀ ['00 A4 04 00 05' + 'DB DC ... DF' + '00' + '90 00']	◀ LT	Error recovery
31	PUT ▶ I(0)₁ ['00 A4 04 00 05' + 'DB DC ... DF' + '00']	▶ LT	Loop-back
32	PUT ◀ I(0)₁ ['EOT Command' + '90 00']	◀ LT	End Of Test command
33	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT	PICC Reset
34	PUT ▶ '05 00 08'	▶ LT	WUPB to poll for the PICC
35	PUT ▶ '05 00 08'	▶ LT	WUPB to poll for the PICC
36	PUT ▶ '05 00 08'	▶ LT	WUPB to poll for the PICC

Scenario 142: Type B Repeated use of a FWT extension after a single S(WTX) Request

5.43.Type B ‘Noise’ in response to an I-Block not indicating chaining [TB414.x]

Test codification:

TB414.x

Test objective:

To ensure that the PCD behaves correctly when it receives some ‘noise’ (i.e. a frame with a transmission error to be processed as noise by the PCD) in response to an I-Block not indicating chaining.

References Requirements:

4.9.2.1, 6.2.1.1, 6.2.1.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT replies to an I-Block not indicating chaining sent by the PUT with a sequence inducing a ‘noise’ error sent using a delay of $[TR0_{MIN} + 128/f_c]$ (with no subcarrier generated by the LT) between the end of the sequence sent by the PUT and the beginning of the ‘noise’ error generated by the LT (in this test, we consider that the synchronization time TR1 with subcarrier on but no modulation is part of the defined ‘noise’ errors).

The LT measures the delay between the end of the sequence sent by the PUT after which a ‘noise’ error is generated and the beginning of the next sequence sent by the PUT to process the error.

The following ‘noise’ errors are generated successively by the LT:

- x=0: Erroneous block of less than 4 bytes (PCB inducing a protocol error) preceded by the minimum synchronization time $TR1_{MIN}$ (with subcarrier on but no modulation) and with CRC error (the CRC bytes are corrupted)
- x=1: Erroneous block of less than 4 bytes (PCB inducing a protocol error) preceded by the minimum synchronization time $TR1_{MIN}$ (with subcarrier on but no modulation) and with some residual bits (i.e. the total number of bits is not a multiple of 8) followed by no modulation (no EoS)
- x=3: Continuous modulation of the PUT carrier with a frequency equal to $f_s = f_c/16$, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of $9152 \times 1/f_c$ (i.e. duration of the minimum synchronization time $TR1_{MIN}$ followed by a 4 bytes frame with the minimum Start of Sequence and End of Sequence and with $EGT_{PICC,MIN}$ between 2 consecutive characters in Type B)

In this test, the default Protocol Information (PI) shall be used:

PI			FWT+ΔFWT
Byte 1	Byte 2	Byte 3	
‘80’	‘21’	‘71’	$573440 \times 1/f_c$

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT ignores the ‘noise’ error, notifies a time-out error and continues the transaction upon receipt of a correct block).

The delay between the end of the sequence sent by the PUT after which a ‘noise’ error is generated and the beginning of the next sequence sent by the PUT to process the error is at least ($\text{FWT} + \Delta\text{FWT}$) and at most [$(\text{FWT} + \Delta\text{FWT}) + t_{\text{RETRANSMISSION}}$].

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ▲ '50' + '55 E6 B9 3C' + '00 00 00 00' + PI ▲ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ▲ '50' + '55 E6 B9 3C' + '00 00 00 00' + PI ▲ LT	ATQB
6	PUT ▶ '1D' + '55 E6 B9 3C' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ▲ '00' ▲ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ▲ I(0)₀ ['00 B2 01 04 00' + '90 00'] ▲ LT	
10	PUT ▶ I(0)₁ ['00 B2 01 04 00'] ▶ LT	Loop-back
11	PUT ▲ For x=0: 'FF' with a CRC error For x=1: 'FF' with 3 bits to (101) _b following the CRC bytes For x=3: Block replaced by a continuous modulation with a duration of $9152 \times 1/f_c$	‘Noise’ error in function of ‘x’ sent using the delay [$\text{TR0}_{\text{MIN}} + 128/f_c$] (delay with no subcarrier generated by the LT) between the end the sequence sent by the PUT and the error (which contains the synchronization time TR1) ▲ LT Error in function of ‘x’
12	PUT ▶ R(NAK)₁ sent between ($\text{FWT} + \Delta\text{FWT}$) and [$(\text{FWT} + \Delta\text{FWT}) + t_{\text{RETRANSMISSION}}$] measured from the end of the last sequence from the PUT ▶ LT	Request for Block repetition
13	PUT ▲ I(0)₁ ['00 B2 02 04 00' + '90 00'] ▲ LT	Error recovery
14	PUT ▶ I(0)₀ ['00 B2 02 04 00'] ▶ LT	Loop-back

Step	Exchanges	Comments
15	<p>'Noise' error in function of 'x' sent using the delay [$TR0_{MIN} + 128/f_c$] (delay with no subcarrier generated by the LT) between the end the sequence sent by the PUT and the error (which contains the synchronization time TR1)</p> <p>PUT ↪ For $x=0$: 'FF' with a CRC error For $x=1$: 'FF' with 3 bits to $(101)_b$ following the CRC bytes For $x=3$: Block replaced by a continuous modulation with a duration of $9152 \times 1/f_c$</p>	◀ LT Error in function of 'x'
16	PUT ↪ $R(NAK)_0$ sent between $(FWT+\Delta FWT)$ and $[(FWT+\Delta FWT) + t_{RETRANSMISSION}]$ measured from the end of the last sequence from the PUT	▶ LT Request for Block repetition
17	PUT ↪ $I(0)_0$ ['00 B2 03 04 00' + '90 00']	◀ LT Error recovery
18	PUT ↪ $I(0)_1$ ['00 B2 03 04 00']	▶ LT Loop-back
19	PUT ↪ $I(0)_1$ ["EOT Command" + '90 00']	◀ LT End Of Test command
20	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
21	PUT ↪ '05 00 08'	▶ LT WUPB to poll for the PICC
22	PUT ↪ '05 00 08'	▶ LT WUPB to poll for the PICC
23	PUT ↪ '05 00 08'	▶ LT WUPB to poll for the PICC

Scenario 143: Type B 'Noise' in response to an I-Block not indicating chaining (x=0, 1 and 3)

5.44. Type B ‘Noise’ in response to an I-Block indicating chaining [TB415.x]

Test codification:

TB415.x

Test objective:

To ensure that the PCD behaves correctly when it receives some ‘noise’ (i.e. a frame with a transmission error to be processed as noise by the PCD) in response to an I-Block indicating chaining.

References Requirements:

4.9.2.1, 6.2.1.1, 6.2.1.2, 10.3.5.6

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT replies to an I-Block indicating chaining sent by the PUT with a sequence inducing a ‘noise’ error sent using a delay of $[TR0_{MIN} + 128/f_c]$ (with no subcarrier generated by the LT) between the end of the sequence sent by the PUT and the beginning of the ‘noise’ error generated by the LT (in this test, we consider that the synchronization time TR1 with subcarrier on but no modulation is part of the defined ‘noise’ errors).

For each transmission error generated during block protocol, the LT measures the delay between the end of the sequence sent by the PUT after which a transmission error is generated and the beginning of the next sequence sent by the PUT to process the error.

The following ‘noise’ errors are generated successively by the LT:

- x=0: R(ACK) Block preceded by the minimum synchronization time $TR1_{MIN}$ (with subcarrier on but no modulation) and with CRC error (the CRC bytes are corrupted)
- x=1: R(ACK) Block preceded by the minimum synchronization time $TR1_{MIN}$ (with subcarrier on but no modulation) and with some residual bits (i.e. the total number of bits is not a multiple of 8) followed by no modulation (no EoS)
- x=3: Continuous modulation of the PUT carrier with a frequency equal to $f_s = f_c/16$, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of $9152 \times 1/f_c$ (i.e. duration of the minimum synchronization time $TR1_{MIN}$ followed by a 4 bytes frame with the minimum Start of Sequence and End of Sequence and with $EGT_{PICC,MIN}$ between 2 consecutive characters in Type B)

In this test, the default Protocol Information (PI) shall be used:

PI			FWT+ΔFWT
Byte 1	Byte 2	Byte 3	
‘80’	‘21’	‘71’	$573440 \times 1/f_c$

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT ignores the ‘noise’ error, notifies a time-out error and continues the transaction upon receipt of a correct block).

For each transmission error generated, the delay between the end of the sequence sent by the PUT after which a ‘noise’ error is generated and the beginning of the next sequence sent by the PUT to process the error is at least $(FWT + \Delta FWT)$ and at most $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$.

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ▲ '50' + '1D F0 0E 33' + '00 00 00 00' + PI ▲ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ▲ '50' + '1D F0 0E 33' + '00 00 00 00' + PI ▲ LT	ATQB
6	PUT ▶ '1D' + '1D F0 0E 33' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ▲ '00' ▲ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ▲ I(0)₀ ['00 A4 04 00 3B' + '01 02 ... 3B' + '00' + '90 00'] ▲ LT	
10	PUT ▶ I(1)₁ ['00 A4 04 00 3B' + '01 02 ... 18'] ▶ LT	Loop-back
11	'Noise' error in function of 'x' sent using the delay $[TR0_{MIN} + 128/f_c]$ (delay with no subcarrier generated by the LT) between the end the sequence sent by the PUT and the error (which contains the synchronization time TR1) PUT ▲ For x=0: R(ACK) ₁ with a CRC error For x=1: R(ACK) ₁ with 3 bits to $(101)_b$ following the CRC bytes For x=3: Block replaced by a continuous modulation with a duration of $9152 \times 1/f_c$	Error in function of 'x'
12	PUT ▶ R(NAK)₁ sent between $(FWT + \Delta FWT)$ and $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$ measured from the end of the last sequence from the PUT ▶ LT	Request for Block repetition
13	PUT ▲ R(ACK)₁ ▲ LT	Error recovery
14	PUT ▶ I(1)₀ ['19 1A 1B ... 33 34 35'] ▶ LT	Loop-back

Step	Exchanges	Comments
15	<p>'Noise' error in function of 'x' sent using the delay [$TR0_{MIN} + 128/f_c$] (delay with no subcarrier generated by the LT) between the end the sequence sent by the PUT and the error (which contains the synchronization time TR1)</p> <p>PUT ↶ For $x=0$: $R(ACK)_0$ with a CRC error For $x=1$: $R(ACK)_0$ with 3 bits to $(101)_b$ following the CRC bytes For $x=3$: Block replaced by a continuous modulation with a duration of $9152 \times 1/f_c$</p>	<p>◀ LT</p> <p>Error in function of 'x'</p>
16	PUT ↶ $R(NAK)_0$ sent between $(FWT+\Delta FWT)$ and $[(FWT+\Delta FWT) + t_{RETRANSMISSION}]$ measured from the end of the last sequence from the PUT	▶ LT Request for Block repetition
17	PUT ↶ $R(ACK)_0$	◀ LT Error recovery
18	PUT ↶ $I(0)_1 [36\ 37\ 38\ 39\ 3A\ 3B' + '00']$	▶ LT Loop-back
19	PUT ↶ $I(0)_1 ["EOT Command" + '90\ 00']$	◀ LT End Of Test command
20	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
21	PUT ↶ '05 00 08'	▶ LT WUPB to poll for the PICC
22	PUT ↶ '05 00 08'	▶ LT WUPB to poll for the PICC
23	PUT ↶ '05 00 08'	▶ LT WUPB to poll for the PICC

Scenario 144: Type B 'Noise' in response to an I-Block indicating chaining (x=0 to 1 and 3)

5.45.Type B ‘Noise’ in response to an R(ACK) Block [TB416.x]

Test codification:

TB416.x

Test objective:

To ensure that the PCD behaves correctly when it receives some ‘noise’ (i.e. a frame with a transmission error to be processed as noise by the PCD) in response to an R(ACK) Block sent to acknowledge a chained I-Block.

References Requirements:

4.9.2.1, 6.2.1.1, 6.2.1.2

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

The LT replies to an R(ACK)-Block sent by the PUT with a sequence inducing a ‘noise’ error sent using a delay of $[TR0_{MIN} + 128/f_c]$ (with no subcarrier generated by the LT) between the end of the sequence sent by the PUT and the beginning of the ‘noise’ error generated by the LT (in this test, we consider that the synchronization time TR1 with subcarrier on but no modulation is part of the defined ‘noise’ errors).

The LT measures the delay between the end of the sequence sent by the PUT after which a ‘noise’ error is generated and the beginning of the next sequence sent by the PUT to process the error.

The following ‘noise’ errors are generated successively by the LT:

- $x=0$: Erroneous block of less than 4 bytes (PCB inducing a protocol error) preceded by the minimum synchronization time $TR1_{MIN}$ (with subcarrier on but no modulation) and with CRC error (the CRC bytes are corrupted)
- $x=1$: Erroneous block of less than 4 bytes (PCB inducing a protocol error) preceded by the minimum synchronization time $TR1_{MIN}$ (with subcarrier on but no modulation) and with some residual bits (i.e. the total number of bits is not a multiple of 8) followed by no modulation (no EoS)
- $x=3$: Continuous modulation of the PUT carrier with a frequency equal to $f_s = f_c/16$, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of $9152 \times 1/f_c$ (i.e. duration of the minimum synchronization time $TR1_{MIN}$ followed by a 4 bytes frame with the minimum Start of Sequence and End of Sequence and with $EGT_{PICC,MIN}$ between 2 consecutive characters in Type B)

In this test, the default Protocol Information (PI) shall be used:

PI			FWT+ΔFWT
Byte 1	Byte 2	Byte 3	
‘80’	‘81’	‘71’	573440 x 1/f _c and FSC = 256 bytes

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT ignores the ‘noise’ error, notifies a time-out error and continues the transaction upon receipt of a correct block).

The delay between the end of the sequence sent by the PUT after which a ‘noise’ error is generated and the beginning of the next sequence sent by the PUT to process the error is at least ($\text{FWT} + \Delta\text{FWT}$) and at most [$(\text{FWT} + \Delta\text{FWT}) + t_{\text{RETRANSMISSION}}$].

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ▲ '50' + '20 9D CF 10' + '00 00 00 00' + PI ▲ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ▲ '50' + '20 9D CF 10' + '00 00 00 00' + PI ▲ LT	ATQB
6	PUT ▶ '1D' + '20 9D CF 10' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ▲ '00' ▲ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ▲ I(1)₀ ['00 A4 04 00 20' + '01 02 03 ... 06 07 08'] ▲ LT	
10	PUT ▶ R(ACK)₁ ▶ LT	Acknowledgement R-Block
11	PUT ▲ For x=0: 'FF' with a CRC error For x=1: 'FF' with 3 bits to (101) _b following the CRC bytes For x=3: Block replaced by a continuous modulation with a duration of $9152 \times 1/f_c$	‘Noise’ error in function of ‘x’ sent using the delay [$\text{TR0}_{\text{MIN}} + 128/f_c$] (delay with no subcarrier generated by the LT) between the end the sequence sent by the PUT and the error (which contains the synchronization time TR1) ▲ LT Error in function of ‘x’
12	PUT ▶ R(ACK)₁ sent within [$(\text{FWT} + \Delta\text{FWT}) + t_{\text{RETRANSMISSION}}$] measured from the end of the last sequence from the PUT ▶ LT	Error notification
13	PUT ▲ I(1)₁ ['09 0A 0B ... 13 14 15'] ▲ LT	Error recovery
14	PUT ▶ R(ACK)₀ ▶ LT	Acknowledgement R-Block

Step	Exchanges	Comments
15	<p>'Noise' error in function of 'x' sent using the delay [$TR0_{MIN} + 128/f_c$] (delay with no subcarrier generated by the LT) between the end the sequence sent by the PUT and the error (which contains the synchronization time TR1)</p> <p>PUT ↳ For $x=0$: 'FF' with a CRC error For $x=1$: 'FF' with 3 bits to $(101)_b$ following the CRC bytes For $x=3$: Block replaced by a continuous modulation with a duration of $9152 \times 1/f_c$</p>	◀ LT Error in function of 'x'
16	PUT ↲ $R(ACK)_0$ sent within $[(FWT+\Delta FWT) + t_{RETRANSMISSION}]$ measured from the end of the last sequence from the PUT	▶ LT Error notification
17	PUT ↳ $I(0)_0$ ['16 17 18 ... 20' + '00' + '90 00']	◀ LT Error recovery
18	PUT ↲ $I(0)_1$ ['00 A4 04 00 20' + '01 02 03 ... 1E 1F 20' + '00']	▶ LT Loop-Back (41 bytes)
19	PUT ↳ $I(0)_1$ ["EOT Command" + '90 00']	◀ LT End Of Test command
20	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
21	PUT ↲ '05 00 08'	▶ LT WUPB to poll for the PICC
22	PUT ↲ '05 00 08'	▶ LT WUPB to poll for the PICC
23	PUT ↲ '05 00 08'	▶ LT WUPB to poll for the PICC

Scenario 145: Type B 'Noise' in response to an R(ACK) Block (x=0 to 1 and 3)

5.46.Type B Protocol error in response to an R(NAK)-Block sent to notify a transmission error [TB417.xy]

Test codification:

TB417.xy

Test objective:

To ensure that the PCD behaves correctly when it receives a sequence inducing a protocol error in response to an R(NAK)-Block sent to notify a transmission error.

References Requirements:

10.1.5.1, 10.2.1.1, 10.2.2.1, 10.3.4.5, 10.3.4.6, 10.3.5.4, 10.3.5.9

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

xy=07 is Not Applicable if the PCD implements a legacy behavior by accepting I-Blocks with b₆ of PCB set to '1' (see ICS).

Procedure:

Run the following scenario.

The LT measures the delay between the beginning of the sequence inducing a protocol error and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

The following protocol errors are generated successively by the LT:

- xy=00: I-Block with bit b₂ of the PCB equal to '0'
- xy=01: I-Block with wrong Block number indicated in the PCB
- xy=02: R(NAK) Block
- xy=03: R(ACK) Block with a Block number different from the one of the last Block sent by the LT
- xy=04: S(DESELECT) response
- xy=05: S(WTX) Request with WTXM = 0
- xy=06: S(WTX) Request with WTXM = 62
- xy=07: I-Block with bit b₆ of the PCB equal to '1' (See "Conditions")
- xy=09: S(WTX) Request with b₆-b₅ of the PCB set to 01_b, with WTXM =1
- xy=10: S(WTX) Request with b₆-b₅ of the PCB set to 10_b, with WTXM =1
- xy=11: I-Block with b₈-b₇ of the PCB set to 01_b

In this test, the default Protocol Information (PI) shall be used:

PI			Comments
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT initiates a PICC Reset when it detects a protocol error after an R(NAK)-Block sent to notify a transmission error).

The delay between the beginning of the sequence inducing a protocol error and the beginning of the PICC Reset initiated by the PUT is at most $t_{RESETDELAY}$ (i.e. the PUT stops sending the carrier within $t_{RESETDELAY}$).

Failure action:

Proceed with the next test

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + 'ED 23 3C 06' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + 'ED 23 3C 06' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + 'ED 23 3C 06' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' ◀ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(0)₀ ['00 B2 05 04 00' + '90 00'] with a transmission error (i.e. CRC error) ◀ LT	Error
10	PUT ▶ R(NAK)₀ ▶ LT	Request for Block repetition
11	Protocol error in function of 'x' For xy=00: I(0) ₀ ['00 B2 05 04 00' + '90 00'] with b ₂ =0 in PCB For xy=01: I(0) ₁ ['00 B2 05 04 00' + '90 00'] For xy=02: R(NAK) ₀ For xy=03: R(ACK) ₀ For xy=04: S(DESELECT) response For xy=05: S(WTX Request) [WTXM='00'] PUT ◀ For xy=06: S(WTX Request) [WTXM='3E'] ◀ LT For xy=07: I(0) ₀ ['00 B2 05 04 00' + '90 00'] with b ₆ =1 in PCB (See "Conditions") For xy=09: S(WTX Request) with b ₆ -b ₅ set to 01 _b in PCB with WTXM =1 For xy=10: S(WTX Request) with b ₆ -b ₅ set to 10 _b in PCB with WTXM =1 For xy=11: I(0) ₀ ['00 B2 05 04 00' + '90 00'] with b ₈ -b ₇ set to 01 _b	Error in function of 'xy'
12	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) The PICC Reset is initiated within t _{RESETDELAY} □ LT	PICC Reset

Scenario 146: Type B Protocol error in response to an R(NAK)-Block sent to notify a transmission error (xy=00 to 07, 09 to 11)

5.47.Type B Removal with an error after WUPB [TB420]

Test codification:

TB420

Test objective:

To ensure that the PCD does not exit the Type B removal procedure on detection of a transmission or a protocol error.

References Requirements:

6.2.1.1, 6.2.1.2, 9.5.1.6

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

During the removal procedure, the PUT successively generates some errors following the WUPB command (see scenario).

In this test, the default Protocol Information (PI) shall be used:

PI			Comments
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (upon receipt of a sequence with error during the removal procedure, the PUT sends a new WUPB command; on detection of a time-out during the removal procedure, the PUT repeats the WUPB command up to 2 times and continues to poll for a PICC when it receives an answer following the repetitions)

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + 'BA DC 0F FE' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + 'BA DC 0F FE' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + 'BA DC 0F FE' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' ◀ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ◀ I(0)₀ ["EOT Command" + '90 00'] ◀ LT	End Of Test command
10	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
11	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
12	PUT ◀ '50' + '50 81 A5 C3' + '00 00 00 00' + PI ◀ LT	ATQB
13	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
14	PUT ◀ '50' + '50 81 A5 C3' + '00 00 00 00' + PI with a transmission error (i.e. CRC error) ◀ LT	Error
15	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
16	PUT ◀ 'C3' + '50 81 A5 C3' + '00 00 00 00' + PI ◀ LT	ATQB with protocol error
17	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
18	PUT ◀ I(0)₀ ['00 B2 04 04 00' + '90 00'] ◀ LT	I-Block
19	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
20	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
21	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
22	PUT ◀ '50' + '70 A5 CC 00' + '00 00 00 00' + PI ◀ LT	ATQB not consistent
23	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
24	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
25	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Step	Exchanges	Comments
26	PUT ↪ '50' + '50 81 A5 C3' + '00 00 00 00' + <i>PI</i>	◀ LT ATQB
27	PUT ↪ '05 00 08'	▶ LT WUPB to poll for the PICC
28	PUT ↪ '05 00 08'	▶ LT WUPB to poll for the PICC
29	PUT ↪ '05 00 08'	▶ LT WUPB to poll for the PICC

Scenario 147: Type B Removal with an error after WUPB

5.48.Type B Consecutive time-outs after S(WTX) Response Blocks [TB421]

Test codification:

TB421

Test objective:

To ensure that the PCD behaves correctly when it detects consecutive time-outs after S(WTX) Response Blocks.

References Requirements:

10.2.2.7, 10.3.5.5, 10.3.5.9

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

In this test, all the Frame Waiting Time Extension Requests are sent with WTXM = 1.

When a time-out error is generated by the LT following 2 consecutive S(WTX) Response Blocks, the LT measures the delay between the end of the second S(WTX) Response sequence and the beginning of the next R(NAK) Block sequence both sent by the PUT.

When three consecutive time-out errors are generated, the LT measures the delay between the end of the third S(WTX) Response sequence and the beginning of the PICC Reset initiated by the PUT (i.e. when the PUT stops sending the carrier).

In this test, the default Protocol Information (PI) shall be used:

PI			FWT+ΔFWT
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	114688 x 1/f _c (default value)

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (the PUT sends an R(NAK) Block when it does not receive any response to a first or a second consecutive S(WTX) Response Block within the extended Frame Waiting Time and initiates a PICC Reset when it does not receive any response to a third consecutive S(WTX) Response Block).

When a time-out error is generated by the LT following 2 consecutive S(WTX) Response Blocks, the delay between the end of the second S(WTX) Response sequence and the beginning of the next R(NAK) Block sequence both sent by the PUT is at most [(FWT+ΔFWT) + t_{RETRANSMISSION}].

When a time-out error is generated by the LT following 3 consecutive S(WTX) Response Blocks, the delay between the end of the third S(WTX) Response sequence and the beginning

of the PICC Reset initiated by the PUT is at most $[(FWT + \Delta FWT) + t_{RESETDELAY}]$ (i.e. the PUT stops sending the carrier within $[(FWT + \Delta FWT) + t_{RESETDELAY}]$).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ▲ '50' + 'FA D0 FA D0' + '00 00 00 00' + PI ▲ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ▲ '50' + 'FA D0 FA D0' + '00 00 00 00' + PI ▲ LT	ATQB
6	PUT ▶ '1D' + 'FA D0 FA D0' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ▲ '00' ▲ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ▲ I(0)₀ ['00 B2 01 04 00' + '90 00'] ▲ LT	
10	PUT ▶ I(0)₁ ['00 B2 01 04 00'] ▶ LT	Loop-back
11	PUT ▲ S(WTX Request) [WTXM = 1] ▲ LT	WTX request
12	PUT ▶ S(WTX Response) [WTXM = 1] ▶ LT	WTX acknowledgment
13	PUT ▶ R(NAK)₁ ▶ LT	Time-out error notification
14	PUT ▲ S(WTX Request) [WTXM = 1] ▲ LT	WTX request
15	PUT ▶ S(WTX Response) [WTXM = 1] ▶ LT	WTX acknowledgment
16	PUT ▶ R(NAK)₁ sent within $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$ ▶ LT	Time-out error notification
17	PUT ▲ I(0)₁ ['00 B2 02 04 00' + '90 00'] ▲ LT	Error recovery
18	PUT ▶ I(0)₀ ['00 B2 02 04 00'] ▶ LT	Loop-back
19	PUT ▲ S(WTX Request) [WTXM = 1] ▲ LT	WTX request
20	PUT ▶ S(WTX Response) [WTXM = 1] ▶ LT	WTX acknowledgment
21	PUT ▶ R(NAK)₀ ▶ LT	Time-out error notification
22	PUT ▲ S(WTX Request) [WTXM = 1] ▲ LT	WTX request
23	PUT ▶ S(WTX Response) [WTXM = 1] ▶ LT	WTX acknowledgment
24	PUT ▶ R(NAK)₀ sent within $[(FWT + \Delta FWT) + t_{RETRANSMISSION}]$ ▶ LT	Time-out error notification
25	PUT ▲ I(0)₀ ['00 B2 03 04 00' + '90 00'] ▲ LT	Error recovery
26	PUT ▶ I(0)₁ ['00 B2 03 04 00'] ▶ LT	Loop-back

Step	Exchanges	Comments
27	PUT ↘ S(WTX Request) [WTXM = 1] ↘ LT	WTX request
28	PUT ↗ S(WTX Response) [WTXM = 1] ↗ LT	WTX acknowledgment
29	PUT ↗ R(NAK)₁ ↗ LT	Time-out error notification
30	PUT ↘ S(WTX Request) [WTXM = 1] ↘ LT	WTX request
31	PUT ↗ S(WTX Response) [WTXM = 1] ↗ LT	WTX acknowledgment
32	PUT ↗ R(NAK)₁ ↗ LT	Time-out error notification
33	PUT ↘ S(WTX Request) [WTXM = 1] ↘ LT	WTX request
34	PUT ↗ S(WTX Response) [WTXM = 1] ↗ LT	WTX acknowledgment
35	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) The PICC Reset is initiated within $[(FWT + \Delta FWT) + t_{RESETDELAY}]$	II LT PICC Reset

Scenario 148: Type B consecutive time-outs after S(WTX) Response Blocks

5.49.Type B Block protocol with respect of the EMD suppression behavior [TB430.xy]

Test codification:

TB430.xy

Test objective:

To ensure that during the block protocol the PCD correctly ignores all the transmission errors except the frames of at least 4 bytes with no residual bit and with CRC error and is ready to process a correct frame no later than $t_{RECOVERY}$ after reception of the last transmission error.

References Requirement:

4.9.2.1

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) upon receipt of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

Procedure:

Run the following scenario.

Upon receipt of an I-Block sent by the PUT during the Block Protocol (performed for at least 2 blocks with different block numbers), the LT sends a transmission error (but not a frame at least 4 bytes with no residual bit and with CRC error) using the following delay TR0 (with no subcarrier generated by the LT) between the end of the sequence sent by the PUT and the beginning of the transmission error generated by the LT (in this test, we consider that the synchronization time TR1 with subcarrier on but no modulation is part of the defined errors):

- $x=0: TR0 = TR0_{MIN} - 128/f_c$
- $x=1: TR0 = TR0_{MIN} + 128/f_c$
- $x=2: TR0 = 499968 \times 1/f_c$

Then, the LT sends a correct response sequence to the PUT using a delay equal to $t_{RECOVERY}$ between the end of the transmission error and the beginning of the synchronization time TR1 (with subcarrier on but no modulation) of the correct response sequence both sent by the LT.
Remark: this sequence is sent using the default value of TR1 defined in the section Generic Information about the Tests.

The following 'noise' errors are generated successively by the LT:

- $y=0:$ Continuous modulation of the PUT carrier with a frequency equal to $f_s = f_c/16$, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of $512 \times 1/f_c$
- $y=1:$ Continuous modulation of the PUT carrier with a frequency equal to $f_s = f_c/16$, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of $9152 \times 1/f_c$ (i.e. duration of the minimum synchronization time $TR1_{MIN}$ followed by a 4 bytes frame with the minimum Start of Sequence and End of Sequence and with $EGT_{PICC,MIN}$ between 2 consecutive characters in Type B)
- $y=2:$ Continuous modulation of the PUT carrier with a frequency equal to $f_s = f_c/16$, with the same amplitude as the other responses sent by the LT during the test transaction and with a duration of $68272 \times 1/f_c$ (i.e. duration of the maximum synchronization time $TR1_{MAX}$ followed by a 40 bytes frame with the maximum Start of Sequence and End of Sequence and with $EGT_{PICC,MAX}$ between 2 consecutive characters in Type B)

of Sequence and End of Sequence and with EGT_{PICC,MAX} between 2 consecutive characters in Type B)

- y=3: Erroneous block of less than 4 bytes (PCB inducing a protocol error) preceded by the minimum synchronization time TR1_{MIN} (with subcarrier on but no modulation) and with the minimum Start of Sequence and End of Sequence (SoS = t_{PICC,S,1,MIN} of logical state low followed by t_{PICC,S,2,MIN} of logical state high with EGT_{PICC,MIN} between 2 consecutive characters and with some residual bits (i.e. the total number of bits is not a multiple of 8) followed by no modulation (no EoS)
- y=4: Erroneous block of less than 4 bytes (PCB inducing a protocol error) preceded by the minimum synchronization time TR1_{MIN} (with subcarrier on but no modulation) and with the minimum Start of Sequence (SoS = t_{PICC,S,1,MIN} of logical state low followed by t_{PICC,S,2,MIN} of logical state high), with EGT_{PICC,MIN} between 2 consecutive characters and with no End of Sequence (EoS) field
- y=5: Erroneous block of less than 4 bytes (PCB inducing a protocol error) preceded by the minimum synchronization time TR1_{MIN} (with subcarrier on but no modulation) and with the minimum Start of Sequence and End of Sequence (SoS = t_{PICC,S,1,MIN} of logical state low followed by t_{PICC,S,2,MIN} of logical state high and EoS = t_{PICC,E,MIN} of logical state low before the LT turns the subcarrier off), with EGT_{PICC,MIN} between 2 consecutive characters and with CRC error (the CRC bytes are corrupted)

In this test, the default Protocol Information (PI) shall be used:

PI			FWT+ΔFWT
Byte 1	Byte 2	Byte 3	
'80'	'81'	'71'	573440 x 1/f _c

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (after sending a sequence during block protocol, the PUT ignores the transmission error and accepts the next correct sequence sent by the LT).

Failure action:

Proceed with the next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ◀ '50' + '46 B5 C7 A0' + '00 00 00 00' + PI ◀ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ◀ '50' + '46 B5 C7 A0' + '00 00 00 00' + PI ◀ LT	ATQB
6	PUT ▶ '1D' + '46 B5 C7 A0' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ◀ '00' ◀ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ◀ 'Noise' error in function of 'y' sent using the delay TR0 (delay with no subcarrier generated by the LT preceding the synchronization time TR1) in function of 'x' For y=0: 512 x 1/f _c of continuous subcarrier modulation For y=1: 9152 x 1/f _c of continuous subcarrier modulation For y=2: 68272 x 1/f _c of continuous subcarrier modulation For y=3: 'FF' (erroneous PCB byte) preceded by TR _{1MIN} , with the minimum SoS and EoS, with EGT _{PICC,MIN} and with 3 bits to (101) _b following the CRC bytes For y=4: 'FF' (erroneous PCB byte) preceded by TR _{1MIN} , with the minimum SoS, with EGT _{PICC,MIN} and with no EoS For y=5: 'FF' (erroneous PCB byte) preceded by TR _{1MIN} , with the minimum SoS and EoS, with EGT _{PICC,MIN} and with CRC error	◀ LT Error in function of 'y' sent with a delay TR0 (delay with no subcarrier generated by the LT preceding the synchronization time TR1) in function of 'x'
10	PUT ◀ I(0) ₀ ['00 A4 04 00 0C' + '01 02 ... 0C' + '00' + '90 00'] sent using a delay of t _{RECOVERY} between the end of the transmission error and the beginning of the synchronization time TR1 (with subcarrier on but no modulation) preceding the correct sequence	◀ LT Correct response sequence sent at t _{RECOVERY} after the transmission error (applied before the synchronization time TR1)
11	PUT ▶ I(0)₁ ['00 A4 04 00 0C' + '01 02 ... 0C' + '00'] ▶ LT	Loop-back (32 bytes frame)
12	PUT ◀ 'Noise' error in function of 'y' sent using the delay TR0 (delay with no subcarrier generated by the LT preceding the synchronization time TR1) in function of 'x' For y=0: 512 x 1/f _c of continuous subcarrier modulation For y=1: 9152 x 1/f _c of continuous subcarrier modulation For y=2: 68272 x 1/f _c of continuous subcarrier modulation For y=3: 'FF' (erroneous PCB byte) with TR _{1MIN} , with the minimum SoS and EoS, with EGT _{PICC,MIN} and with 3 bits to (101) _b following the CRC bytes For y=4: 'FF' (erroneous PCB byte) with TR _{1MIN} , with the minimum SoS, with EGT _{PICC,MIN} and with no EoS For y=5: 'FF' (erroneous PCB byte) with TR _{1MIN} , with the minimum SoS and EoS, with EGT _{PICC,MIN} and with CRC error	◀ LT Error in function of 'y' sent with a delay TR0 (delay with no subcarrier generated by the LT preceding the synchronization time TR1) in function of 'x'

Step	Exchanges	Comments
13	PUT ↪ I(0)₁ ['00 A4 04 00 0C' + '91 92 ... 9C' + '00' + '90 00'] sent using a delay of tRECOVERY between the end of the transmission error and the beginning of the synchronization time TR1 (with subcarrier on but no modulation) preceding the correct sequence PUT ↪ I(0)₀ ['00 A4 04 00 0C' + '91 92 ... 9C' + '00']	◀ LT Correct response sequence sent at tRECOVERY after the transmission error (applied before the synchronization time TR1)
14	PUT ↪ I(0)₀ ['00 A4 04 00 0C' + '91 92 ... 9C' + '00']	▶ LT Loop-back
15	PUT ↪ I(0)₀ ['EOT Command' + '90 00']	◀ LT End Of Test command
16	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier)	II LT PICC Reset
17	PUT ↪ '05 00 08'	▶ LT WUPB to poll for the PICC
18	PUT ↪ '05 00 08'	▶ LT WUPB to poll for the PICC
19	PUT ↪ '05 00 08'	▶ LT WUPB to poll for the PICC

**Scenario 149: Type B Block protocol with respect of the EMD suppression behavior
(xy=00 to 05, xy=10 to 15 and xy=20 to 25)**

5.50.Type B Block Protocol with respect of the ‘deaf time’ [TB435.x]

Test codification:

TB435.x

Test objective:

To ensure that after sending a block during the block protocol, the PCD is completely deaf (i.e. ignores any subcarrier generated by the PICC) until TR0_{MIN}.

References Requirement:

4.3.2.3

Conditions:

Respect of the Generic Information about the Tests (see section 2).

The test starts (step 1 of the scenario) on reception of a WUPB command sent by the PUT during the polling procedure described in TC001.

The LT uses the Type B frame format and a bit rate of 106 kb/s.

The tests TB435.x is performed after a new run of TB000, with no reset of the test tool between the pre-test TB000 and the tests TB435.x to ensure that the value of TR1_{PUTMIN} used is during TB435 is correct.

Procedure:

Run the following scenario.

On reception of an I-Block sent by the PUT during the Block Protocol (performed for at least 2 blocks with different block numbers), the LT sends a sequence with no transmission error (i.e. a correct sequence or a sequence with protocol error) using the delay TR0 = TR0_{MIN} – 128/f_c (with no subcarrier generated by the LT) between the end of the sequence sent by the PUT and the beginning of the synchronization time TR1 (with subcarrier on but no modulation) preceding the sequence replied by the LT.

The following sequences are successively sent by the LT in response to the relevant I-Blocks:

- x=0: Erroneous block of less than 4 bytes (PCB inducing a protocol error) preceded by TR1_{PUTMIN}, the minimum synchronization time supported by the PUT (with subcarrier on but no modulation), and with the minimum Start of Sequence and End of Sequence (SoS = t_{PICC,S,1,MIN} of logical state low followed by t_{PICC,S,2,MIN} of logical state high and EoS = t_{PICC,E,MIN} of logical state low before the LT turns the subcarrier off), with EGT_{PICC,MIN} between 2 consecutive characters and with correct CRC
 - Note: the value of the parameter TR1_{PUTMIN} has been determined during the test TB000
- x=1: Erroneous block of less than 4 bytes (PCB inducing a protocol error) preceded by TR1_{PUTMIN}, the minimum synchronization time supported by the PUT (with subcarrier on but no modulation), and with the minimum Start of Sequence and End of Sequence (SoS = t_{PICC,S,1,MIN} of logical state low followed by t_{PICC,S,2,MIN} of logical state high and EoS = t_{PICC,E,MIN} of logical state low before the LT turns the subcarrier off), with EGT_{PICC,MIN} between 2 consecutive characters and with no CRC
 - Note: the value of the parameter TR1_{PUTMIN} has been determined during the test TB000

In this test, the default Protocol Information (PI) shall be used:

PI			Comments
Byte 1	Byte 2	Byte 3	
'80'	'21'	'41'	Default value

Acceptance criteria:

The PUT sends commands and blocks and behaves as described in the following scenario (after sending a sequence during block protocol, the PUT ignores the sequence received during the 'deaf time' and processes it as a time-out error i.e. sends an error notification block).

Failure action:

Proceed with next test.

Scenario:

Step	Exchanges	Comments
1	PUT ▶ '05 00 08' ▶ LT	WUPB during polling
2	PUT ▲ '50' + '66 D8 E4 C6' + '00 00 00 00' + PI ▲ LT	ATQB
3	PUT ▶ '52' (Type A short frame) ▶ LT	WUPA
4	PUT ▶ '05 00 08' ▶ LT	WUPB
5	PUT ▲ '50' + '66 D8 E4 C6' + '00 00 00 00' + PI ▲ LT	ATQB
6	PUT ▶ '1D' + '66 D8 E4 C6' + '00 08 01 00' ▶ LT	ATTRIB
7	PUT ▲ '00' ▲ LT	ATTRIB Response
8	PUT ▶ I(0)₀ ['00 A4 04 00 0E' + "2PAY.SYS.DDF01" + '00'] ▶ LT	Select PPSE
9	PUT ▲ Sequence in function of 'x' sent using the delay TR0 = TR0 _{MIN} – 128/f _c (delay with no subcarrier generated by the LT preceding the synchronization time TR1) For x=0: 'FF' (erroneous PCB byte) preceded by TR1 _{PUTMIN} , with the minimum SoS and EoS, with EGT _{PICC,MIN} and with correct CRC For x=1: 'FF' (erroneous PCB byte) preceded by TR1 _{PUTMIN} , with the minimum SoS and EoS, with EGT _{PICC,MIN} and with no CRC ▲ LT	Sequence in function of 'x' sent with the delay TR0 _{MIN} – 128/f _c
10	PUT ▶ R(NAK)₀ ▶ LT	Time-out error notification
11	PUT ▲ I(0)₀ ['00 A4 04 00 0C' + '01 02 ... 0C' + '00' + '90 00'] ▲ LT	Error recovery
12	PUT ▶ I(0)₁ ['00 A4 04 00 0C' + '01 02 ... 0C' + '00'] ▶ LT	Loop-back (32 bytes frame)
13	PUT ▲ Sequence in function of 'x' sent using the delay TR0 = TR0 _{MIN} – 128/f _c (delay with no subcarrier generated by the LT preceding the synchronization time TR1) For x=0: 'FF' (erroneous PCB byte) preceded by TR1 _{PUTMIN} , with the minimum SoS and EoS, with EGT _{PICC,MIN} and with correct CRC For x=1: 'FF' (erroneous PCB byte) preceded by TR1 _{PUTMIN} , with the minimum SoS and EoS, with EGT _{PICC,MIN} and with no CRC ▲ LT	Sequence in function of 'x' sent with the delay TR0 _{MIN} – 128/f _c

Step	Exchanges	Comments
14	PUT ▶ R(NAK)₁ ▶ LT	Time-out error notification
15	PUT ◀ I(0)₁ ['00 A4 04 00 0C' + '91 92 ... 9C' + '00' + '90 00'] ◀ LT	Error recovery
16	PUT ▶ I(0)₀ ['00 A4 04 00 0C' + '91 92 ... 9C' + '00'] ▶ LT	Loop-back
17	PUT ◀ I(0)₀ ["EOT Command" + '90 00'] ◀ LT	End Of Test command
18	PUT II The PUT performs a PICC Reset (i.e. stops sending the carrier) II LT	PICC Reset
19	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
20	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC
21	PUT ▶ '05 00 08' ▶ LT	WUPB to poll for the PICC

Scenario 150: Type B Block Protocol with respect of the 'deaf time' (x=0 and 1)

***** END OF DOCUMENT *****

EMV® Type Approval

Contactless Terminal Level 1

PCD Pre-Validation Test

Version 2.6b
December 2016

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Revision Log – Version 2.6b

The following changes have been made to the document since the publication of Version 2.5a. Some of the numbering and cross references in this version have been updated to reflect changes introduced by the published bulletins. The numbering of existing requirements did not change, unless explicitly stated otherwise.

Incorporated changes described in the following Specification Updates:

See section 1.3.2

Other editorial changes:

Minor typographical corrections

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1 Using this Manual

1.1 Purpose

The present document “ EMVCo Type Approval- Contactless Terminal Level 1- PCD Pre-Validation Test” describes a set of test cases which are designed to determine whether the tested Proximity Coupling Device (PCD) is able to establish a minimum level of communication with PICCs. Those test cases have to be applied before starting the Analogue Test of the PCD.

1.2 Audience

The target audience of this document includes:

- PCD vendors
- Testing laboratories accredited to perform the type approval tests

1.3 Reference Documents

EMV documents are available on the EMVCo web site:

<http://www.emvco.com/approvals.aspx> and
<http://www.emvco.com/specifications.aspx>

1.3.1 Standards Documents

Document	Version Issue date
ISO/IEC 17025:2005 : General Requirements for the Competence of Calibration and Testing Laboratories	2005
ISO/IEC Guide 98-3:2008 : Uncertainty of measurement – Part 3 – Guide to the expression of uncertainty in measurement, ISO/IEC, corrected version 2010.	2008

1.3.2 Specification Documents

Document	Version Issue date
EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification	Version 2.6 March 2016
EMV Contactless Symbol Reproduction Requirements	Version 2.0, 7 November 2016
Type B Modulation Index, EMV Specification Bulletin No.183	First edition, December 2015
Type B Bit Boundaries Tolerance, EMV Specification Bulletin No. 188	First edition, December 2016
<i>EMVCo Type Approval Accreditation Requirements for EMVCo Terminal Type Approval Laboratories.</i>	

1.3.3 Laboratory Test Documents

The test documents to be applied by EMVCo accredited laboratories when performing an EMV Contactless Terminal Type Approval Level 1 session are listed in the following document:

**EMVCo Type Approval
Contactless Terminal Level 1
Laboratories Documentation**

Check the last version of this document for any update of the test documents.

1.4 Definitions

In addition of terms already defined in the reference documentation, the following terms are used in this document:

Term	Definition
Analogue Test	Set of tests that check the Radio Frequency of the hardware and software/firmware of the PCD against the EMV Specifications.
Device Test Environment	Part of the Test Environment needed to perform the PCD Type Approval Test, which the Vendor needs to develop and submit to the Test Laboratory at the same time as the Samples.
EMV – TEST CMR	A hardware device qualified as reference equipment which is used with other EMV Test Equipment. Its purpose is to condition and switch signals between its inputs and outputs.

Term	Definition
EMV – TEST PCD	A hardware device qualified as reference equipment which is used with other EMV Test Equipment. Its purpose is to simulate a PCD.
EMV – TEST PICC	A hardware device qualified as reference equipment which is used with other EMV Test Equipment. Its purpose is to simulate a PICC.
Envelope	Waveform connecting positive or negative peaks of oscillating signal.
Implementation Conformance Statement (ICS)	Form completed by the Vendor identifying the PCD implementation and to be submitted to the Test Laboratory along with the Samples.
Landing Plane	The designated surface area of a PCD where a user should place a PICC to obtain a successful transaction.
Loopback Application	Test application that the vendor needs to develop and implement in the Device Test Environment.
Loopback mode	Loopback involves cycling back information in a channel. Any data transmitted through such a channel is immediately received by the same channel. A device is in loopback mode after such a mode has been activated.
Modulation Index	The modulation Index of an amplitude modulated signal is defined as $mi = ([A(t)]MAX - [A(t)]MIN)/([A(t)]MAX + [A(t)]MIN)$ where $A(t)$ is the envelope of the modulated carrier.
Operating Volume	The 3-dimensional space in which the PCD shall reliably communicate with an PICC by means of a magnetic field.
PCD Type Approval	Acknowledgment by EMVCo that a specified PCD within a specified Contactless Product has demonstrated sufficient conformance to the EMV Specification.
PCD Under Test	PCD embedded in the Sample that is actually tested during Type Approval Test.
PCD Vendor	Entity that submits the PCD for PCD Type Approval.
Pre-validation Test	Defined set of tests that checks whether a transaction takes place when a series of PICCs are presented in a series of parameterized positions at the PCD Under Test.
Pre-validation Test Application	Test application that the vendor needs to develop and to implement in the Device Test Environment.
Polling	Sequence during which the PCD sends alternatively WUPA and WUPB commands until a response is received.
Presentation Plane	The plane on the EMV – TEST PICC that faces the EMV – TEST PCD.
Proximity Coupling Device (PCD)	A hardware device that uses inductive coupling to provide power to the PICC and exchange data with the PICC.

Term	Definition
Proximity Integrated Circuit Card (PICC)	A hardware device containing an integrated circuit and capable of inductive coupling in the proximity of a coupling device.
Sample	A physical implementation of a PICC or a PCD delivered to the Testing Laboratory for testing.
Set-up	Procedure to follow to prepare EMV Test Equipment before starting a test.
Terminal	Any device used to interact with a PICC and which operates to the requirements of the EMV Contactless Specifications for Payment Systems — Book D — EMV Contactless Communication Protocol Specification. This includes the PCD and may also include other components and interfaces.
Test Bench	A specific test bench as described in the in the EMVCo Contactless Type Approval: PCD Analogue Test Bench and Test Case Requirements manual.
Test Environment	Environment needed to perform the Test. It is constituted of a Test Bench in combination with a Device Test Environment for PCD Type Approval Test.
Test Case	Test to verify a requirement at a specific position in the Operating Volume.
Test Code	Code to identify a Test Case.
Testing Laboratory	A facility accredited by EMVCo for performing EMV Contactless testing of the analogue interface for PICCs and PCDs.
Test Report	Document provided by the Test Laboratory containing the Test results.
Transaction	A sequence of logic interactions that the PICC and the Terminal shall execute as foreseen by the EMV Contactless application. The transaction starts with the first logic message from the PCD to the PICC.

1.5 Abbreviations and Notations

The following abbreviations and notations are used in this document:

PCD Proximity Coupling Device

PICC Proximity Integrated Circuit Cards

1.6 Terminology and Conventions

The following words are used often in this specification and have a specific meaning:

Shall

Defines a product or system capability which is mandatory.

May

Defines a product or system capability which is optional or a statement which is informative only and is out of scope for this specification.

Should

Defines a product or system capability which is recommended.

1.7 Support

For support regarding EMV Contactless analogue testing, refer to www.emvco.com.

2 General Requirements and Conventions

2.1 The Pre-validation Purpose

The purpose of pre-validation prior to PCD Analogue Test is to ensure that a minimum communication at protocol level can be established between the PCD Under Test and a set of actual and EMV compliant PICCs, at set distances from 0 cm to 4 cm.

If the PCD Under Test fails the Pre-validation Test, then there may be a risk of failure with the rest of the PCD Type Approval testing. The Test Laboratory shall warn the Vendor. The vendor then takes the responsibility to either stop the PCD Type Approval Test session or to continue with the Analogue Test session.

The Pre-Validation Test is optional.

2.2 Requirements for Test Laboratory

The requirements specified in section 1 of *EMVCo PCD Analogue Test Bench and Test Case Requirements* apply for the Pre-validation Test.

Some additional requirements are mentioned below.

2.2.1 Accreditation requirements

The Test Laboratory shall create its own test tool to allow correct positioning of the PICCs during Pre-validation Test.

The Test Laboratory shall have an internal management process in order to ensure that only the valid version of EMVCo Pre-validation PICCs Set at the time of testing will be used.

This equipment shall be considered as part of the Test Bench defined in the *EMVCo PCD Analogue Test Bench and Test Case Requirements*. All Test Bench accreditation requirements described in *EMVCo PCD Analogue Test Bench and Test Case Requirements* also apply to this equipment.

2.2.2 Controlled Test Conditions

The Controlled Test Conditions requirements described in *EMVCo PCD Analogue Test Bench and Test Case Requirements* also apply for the Pre-validation Test.

2.3 Positioning Conventions and Requirements

The Positioning Conventions and Requirements specified in section 2 of *EMVCo PCD Analogue Test Bench and Test Case Requirements* apply for Pre-validation Test.

Remark: In this section 2, when talking about Pre-validation Test, the term EMV- TEST PCD shall be understood as PCD Under Test, and the term EMV-TEST PICC as one PICC of the EMVCo Pre-validation PICCs Set.

2.4 Test Environment

2.4.1 Pre-validation Test tool

Test Laboratory shall develop a test tool (jig...) able to help the Test Laboratory operator to place the PICC of the EMVCo Pre-validation PICCs Set in the positions specified in section 6.4 below.

A non-metallic positioning tool shall be used to avoid influencing electromagnetic fields.

2.4.2 EMVCo Pre-validation PICCs Set

Test Laboratory shall use the EMVCo Pre-validation PICCs Set defined by EMVCo and provided by the Payment Systems. Additional rules governing the use of the cards may be defined by the Payment Systems.

3 Executing an EMV Pre-validation Test

3.1 Prerequisites

Before starting any test campaign, several important requirements shall be verified:

- The Test Laboratory shall develop a test tool for PICC positioning as specified in section 4.4.1,
- The Test Laboratory shall write a procedure for the management of the EMVCo Pre-validation PICCs Set,
- The staff performing the test shall be appropriately trained and qualified,
- The Test Laboratory shall write standard operating procedures providing detailed methods on Pre-validation Test and how results are recorded.

3.2 Sample testing

Test results

The test results shall be recorded as an ordered collection of pass/ fail values, related to the PCD Under Test and the test conditions. This is called detailed report data.

Failed procedures

If one or more of the following situations appear:

- A specified test condition cannot be attained during test execution,
- A test procedure cannot be executed exactly as indicated,
- A test procedure cannot be completed.
- The operator shall report a fail procedure situation.

3.3 Generating a report

The detailed report data has to be included in the full PCD Type Approval Test Report.

If it was not possible for any reason to carry out all the Pre-validation Test, then this shall be clearly documented.

3.4 Tasks after Completing Pre-validation Test

Two cases are possible depending on the test results:

- The results are pass, then the operator continues the Analogue Test of the PCD Type Approval process as described in section 5.5 of EMVCo PCD Analogue Test Bench and Test Case Requirements,

- Some results are failed, then the operator informs the Vendor and waits the decision of the Vendor to either continue the PCD Type Approval Test or stop the process. In the situation where the Vendor decides to stop, the test report shall be sent to the Vendor.

In either situation, the Payment System will be notified for any appropriate failed cards through EMVCo.

4 PCD Pre-validation Test Plan

4.1 Prerequisites

Before performing Pre-validation Test, make sure that Test Laboratory operator:

- Is familiar with the positioning conventions and requirements,
- Has verified the test tool, and the EMVCo Pre-validation PICCs Set,
- Has acquainted himself with the Device Test Environment documentation provided by the Vendor, knows how to operate the Device Test Environment, and how it will indicate that a minimum communication at protocol level has been established between a PICC of the EMVCo Pre-validation PICCs Set and the PCD Under Test.
- Has already performed sections 5.1, 5.2, 5.3 and 5.4 of EMVCo PCD Analogue Test Bench *and Test Case Requirements*

4.2 Preliminary set ups

Before Pre-validation Test, the Device Test Environment shall be installed as specified in the documentation provided by the Vendor.

4.3 Positioning Accuracy

The accuracy of the positioning during the test session shall be as follows:

- Accuracy on z and $r = \pm 1$ mm
- Accuracy on $\phi = \pm 0.1$ rad.

4.4 Test positions

Use the table below for the test positions of the PICCs during the Pre-validation Test.

z	r	ϕ
0 cm	0 cm	0 rad
1 cm	0 cm	0 rad
2 cm	0 cm	0 rad
3 cm	0 cm	0 rad
4 cm	0 cm	0 rad

Table 1: Positions

4.5 Procedure

Follow this procedure to verify that the PCD is able to establish a minimum communication at protocol level with actual and EMV compliant PICCs:

1. Display the TTA L1- Pre-validation Menu, using the Device Test Environment.
2. Place the first PICC of the set in the first position of Table 1.
3. Determine and record the result status.
4. Repeat steps 2 and 3 with the same PICC for all other positions.
5. Repeat steps 2 to 4 for all PICCs of the EMVCo Pre-validation PICCs Set.

5 Acceptance criteria

The Device Test Environment indicates “successful communication exchange” using a sound, a visual warning as indicated in the vendor’s documentation.

5.1 Expected results

Records are recorded by PICC and by position with one of the three statements:

- Pass message
- Fail message.
- Failed procedure – not tested.

*** End of Document ***