Diglient Nexys4 FPGA Board & Xilinx Vivado Development Suite

DD Lab3

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Outline

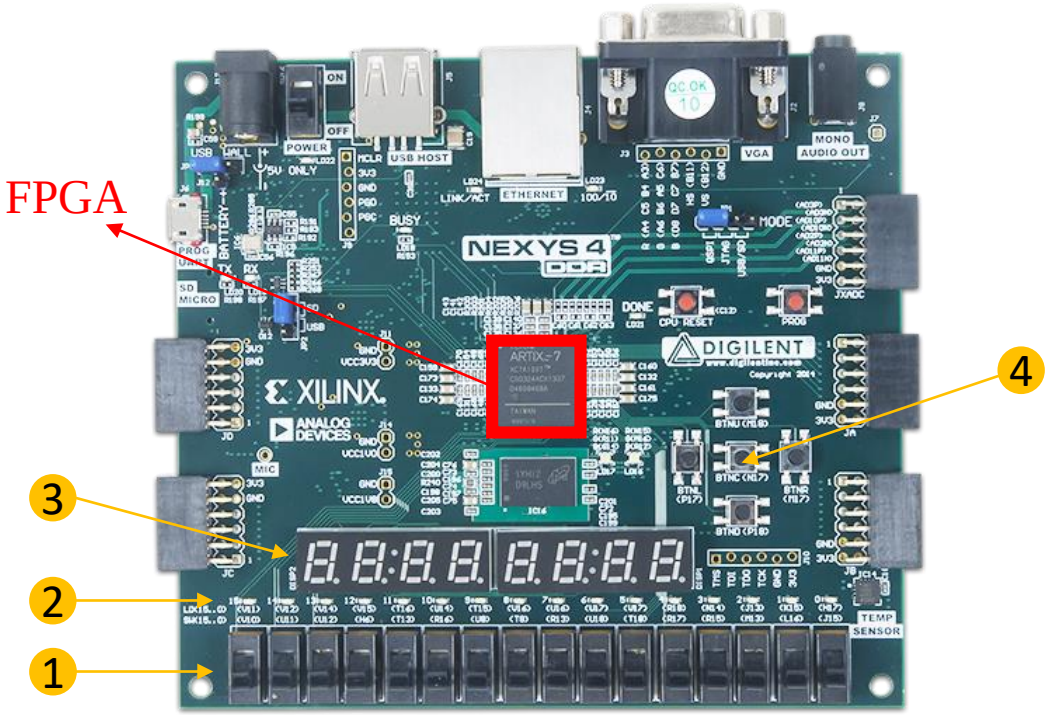
- 課程目的
- 課程工具介紹
- 課程實驗內容
- Lab作業
- 課程評分方式
- 附錄

課程目的

在本次Lab中，同學們將會學到如何利用Vivado開發工具將前一堂課的四個4-bit adder燒錄到Nexys4 FPGA開發板上，並透過Nexys4上的switch、LED等周邊驗證RTL電路設計的正確性

課程工具

- Nexys4上的FPGA可以用RTL來描述其電路行為
- Nexys4上有現成的電路像是LED、switch、七段顯示器等開發板周邊，可用作FPGA的輸入以及輸出



Callout	Component Description
1	switch(16)
2	LED(16)
3	7-segment display(8)
4	push button(5)

datasheet: https://reference.digilentinc.com/_media/nexys:nexys4:nexys4_rm.pdf

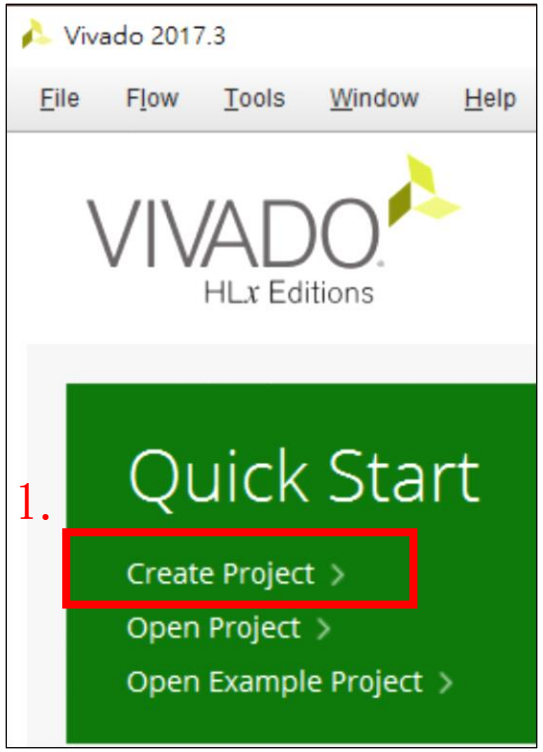
課程實驗

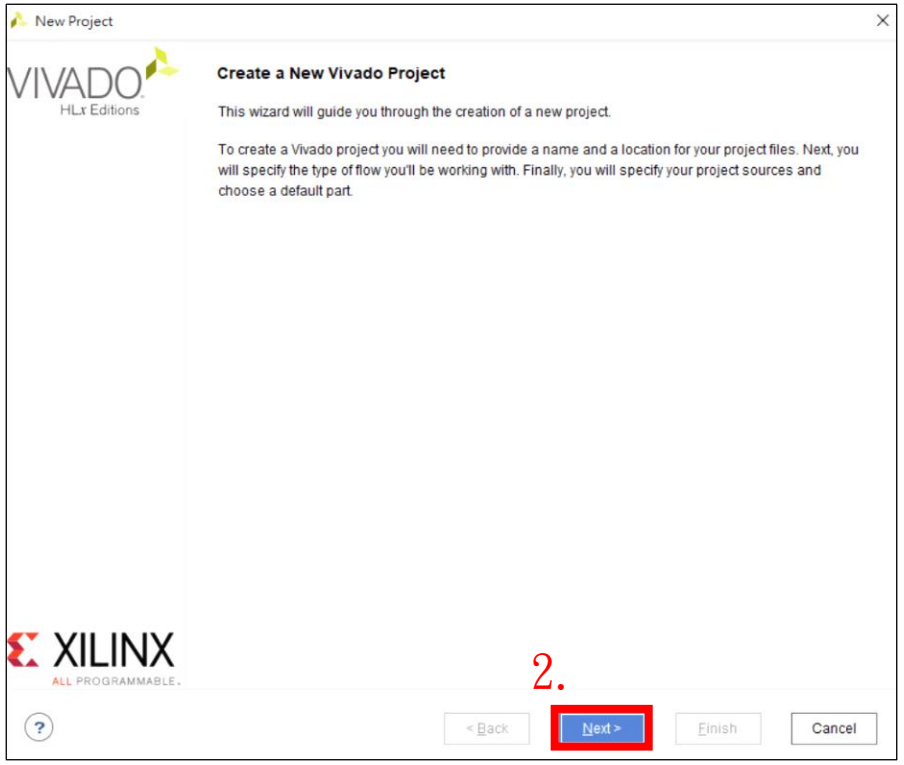
- 課程實驗項目
  - 用16顆switches (sw0~sw15)分別控制16顆LED (led0~led15)的明滅

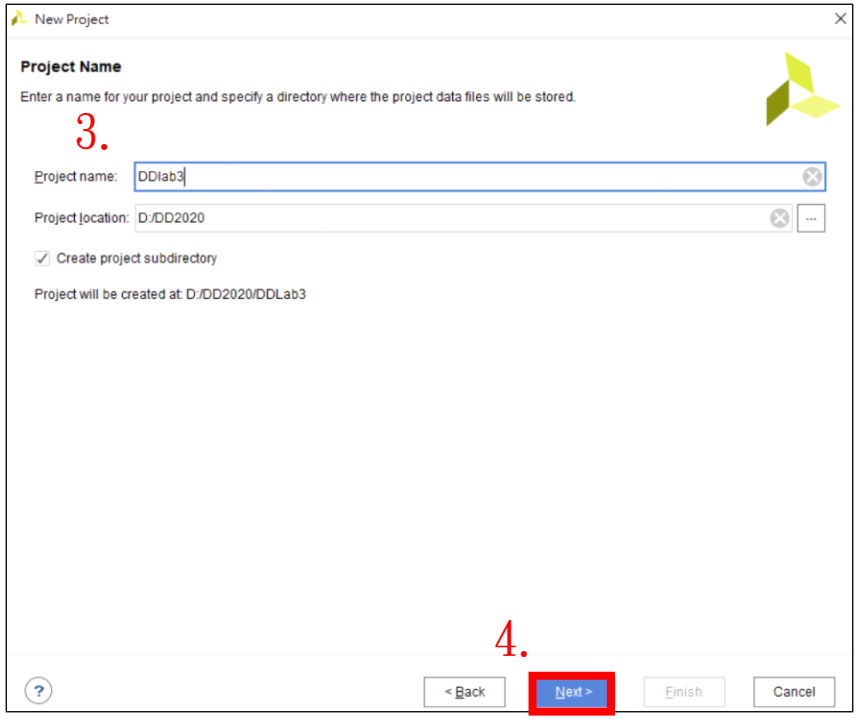
- 實驗教學內容
  - Vivado建立專案
  - Vivado創建專案原始檔
  - .xdc檔設定
  - 產生bit檔並燒入至Nexys4

Vivado建立專案(1/4)

- 建立課堂練習專案
- 開啟Vivado > Create Project > Next > 輸入專案名稱 > Next

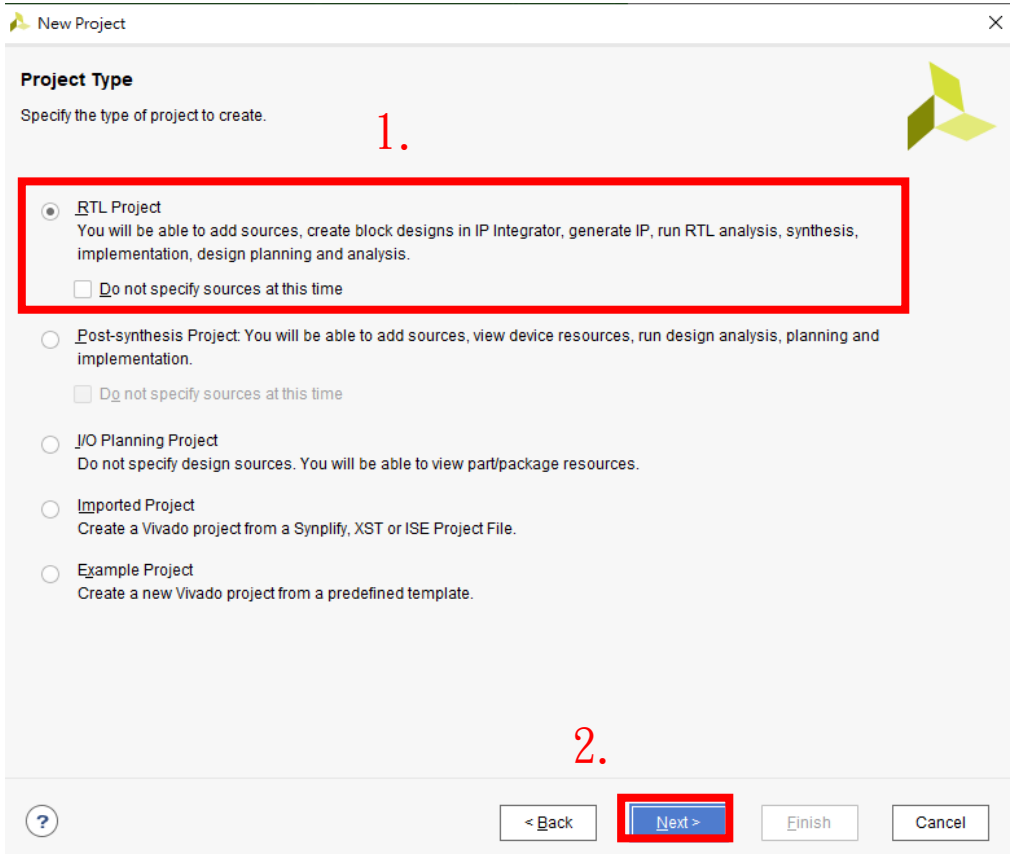


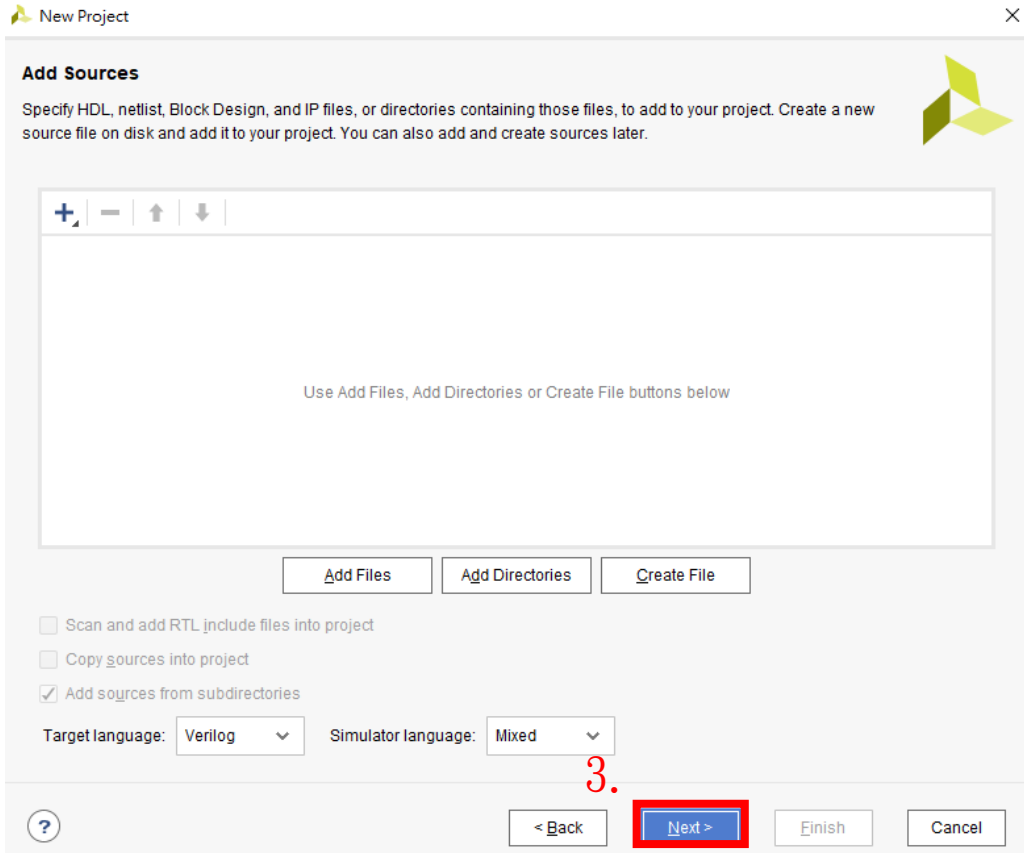




Vivado建立專案(2/4)

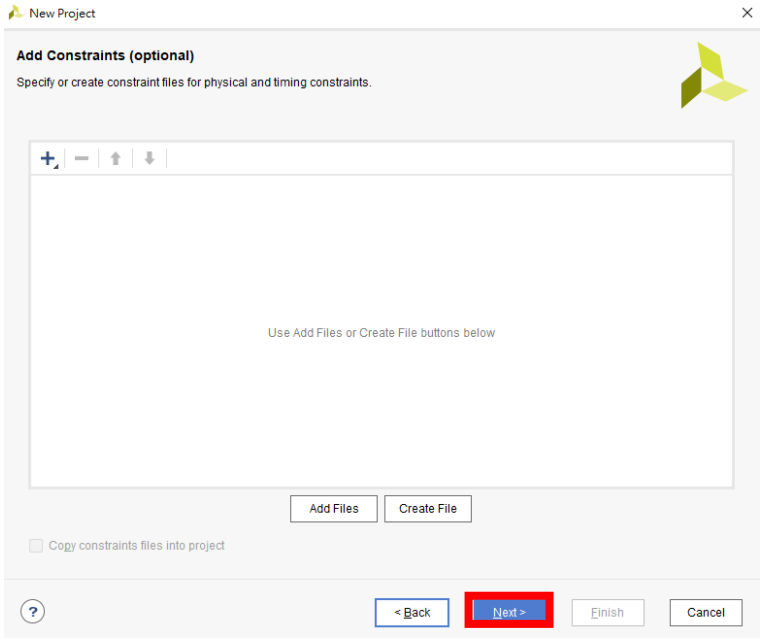
- 選擇RTL Project > Next > Next

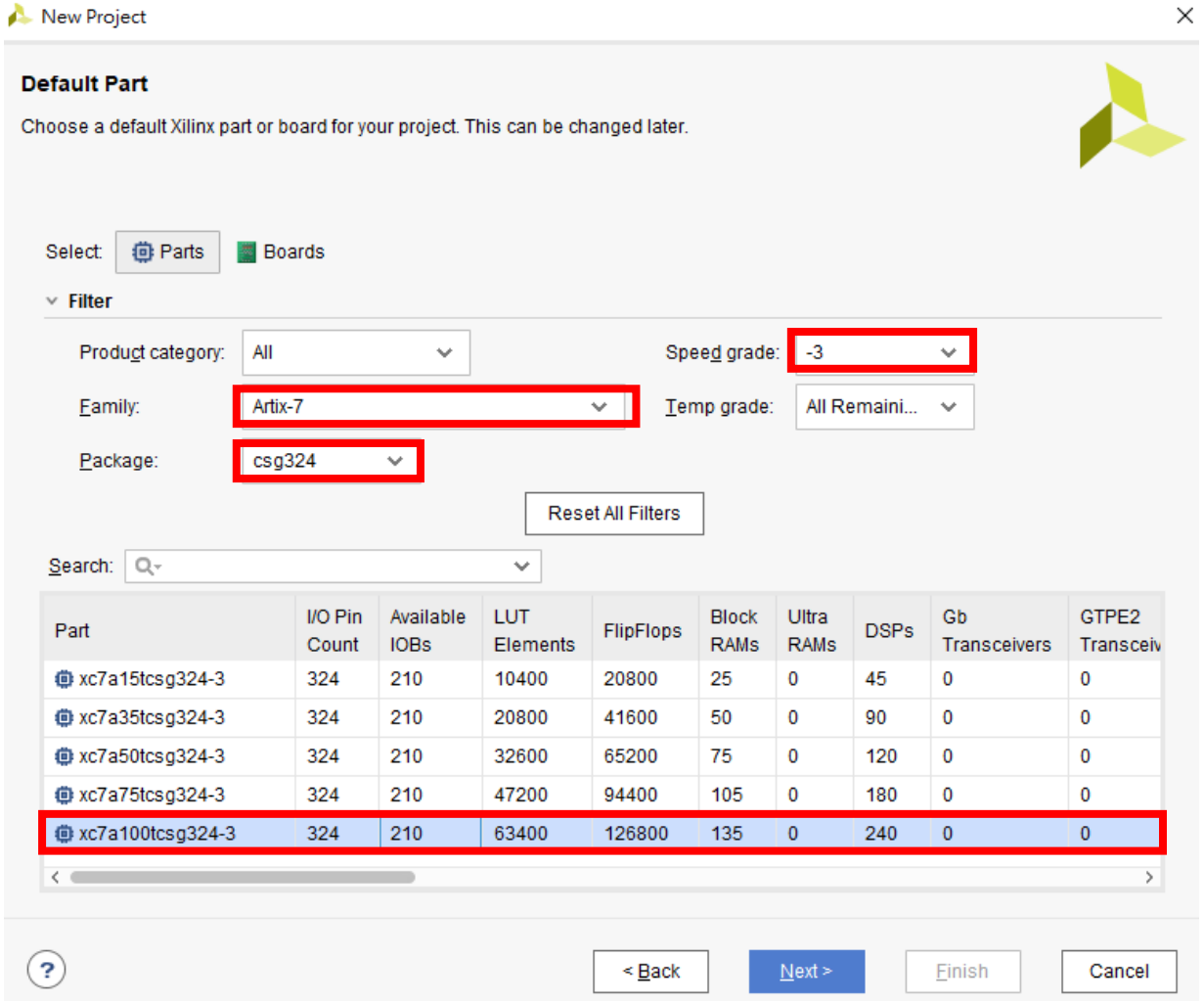




Vivado建立專案(3/4)

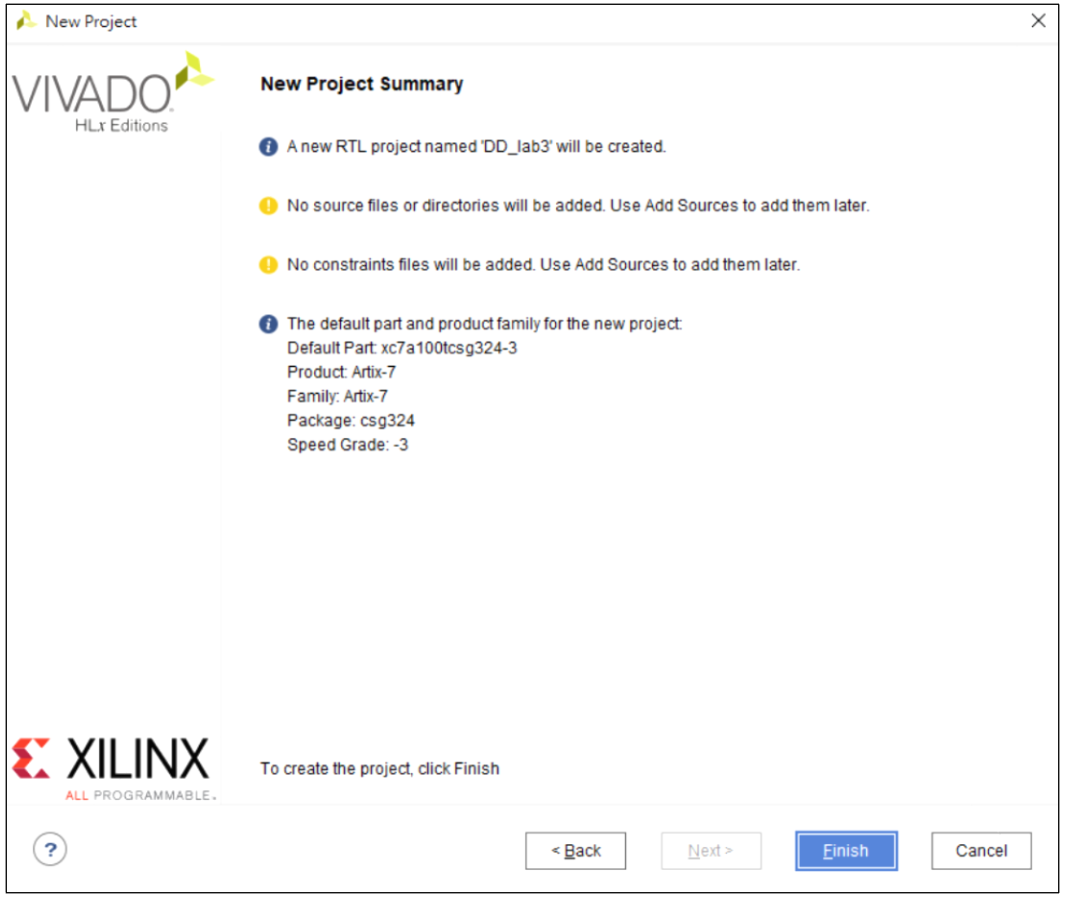
- Next > Family:Artix-7 > Package:csg324 > Speed grade:-3 > xc7a100tcsg324-3





Vivado建立專案(4/4)

- Finish

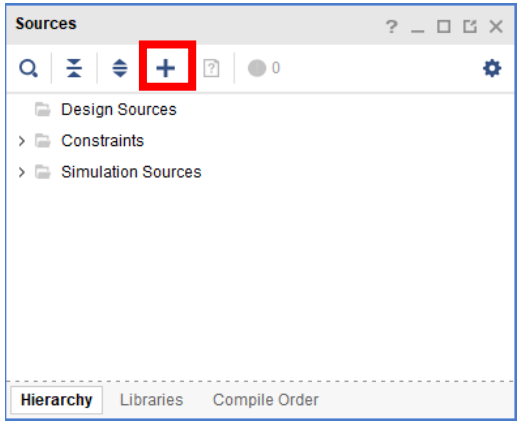


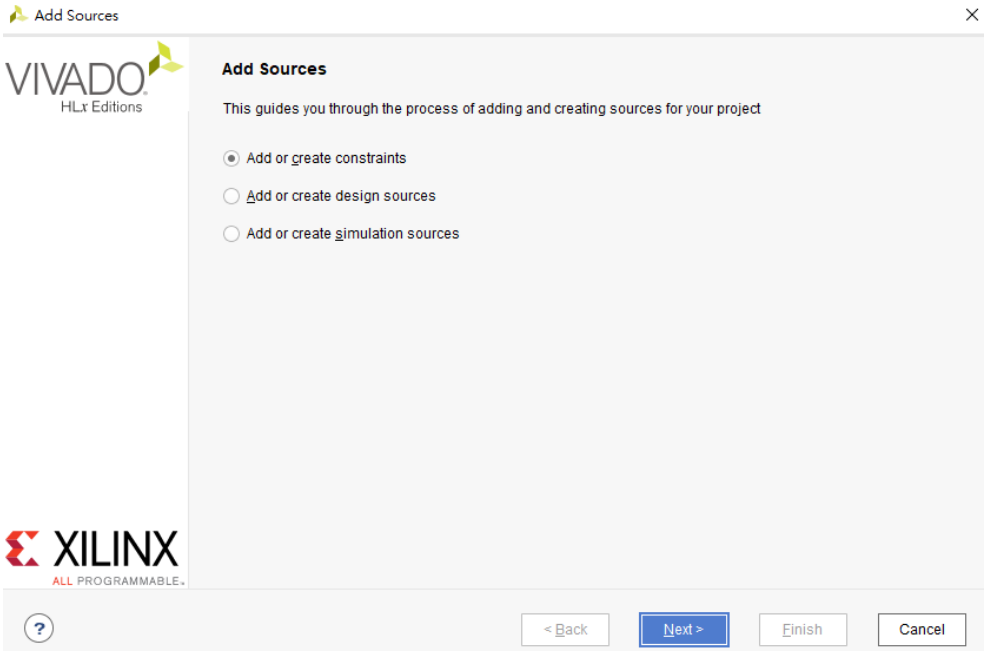
Vivado創建專案原始檔(1/3)

- 按加號新增檔案
- 選擇檔案類型 > Add or create constraints
  - constraints :新增.xdc檔

    .xdc用來描述.v與實體線路的連接關係
  - design sources :新增.v檔

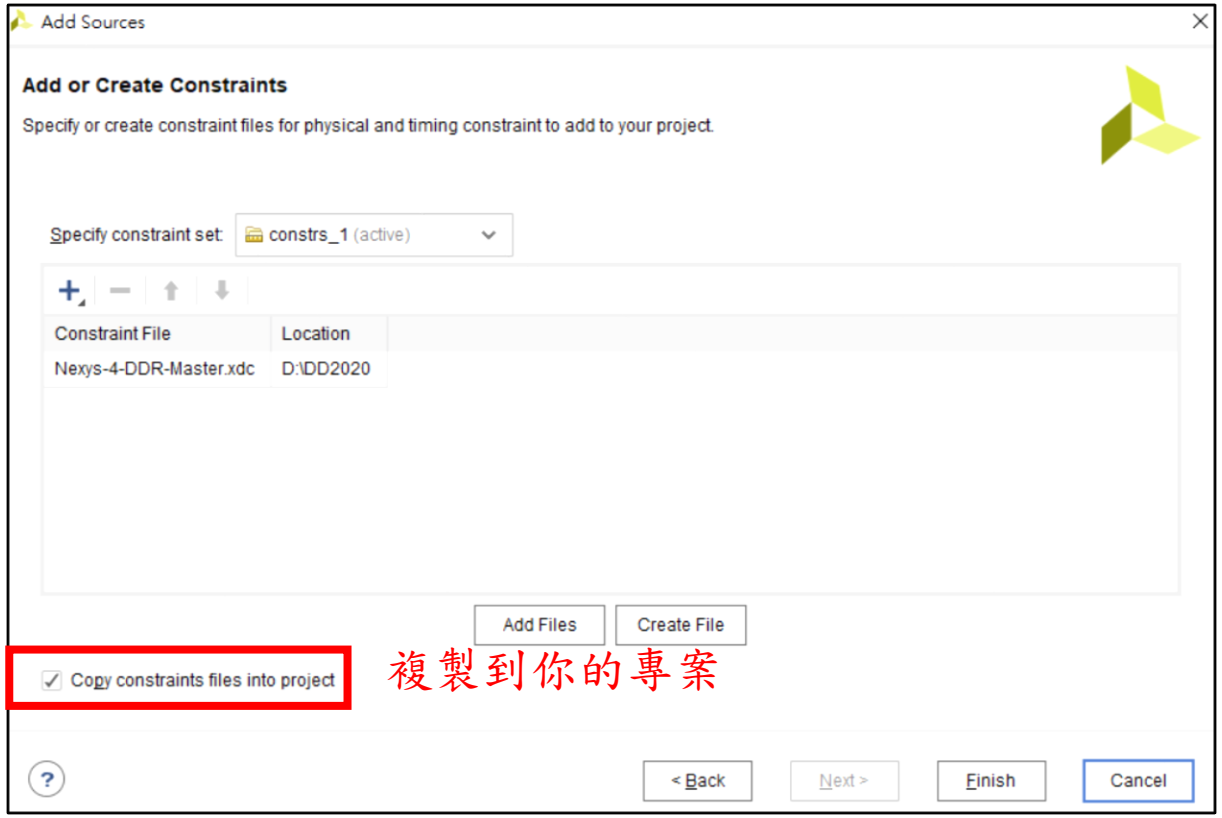
    .v用來描述硬體行為





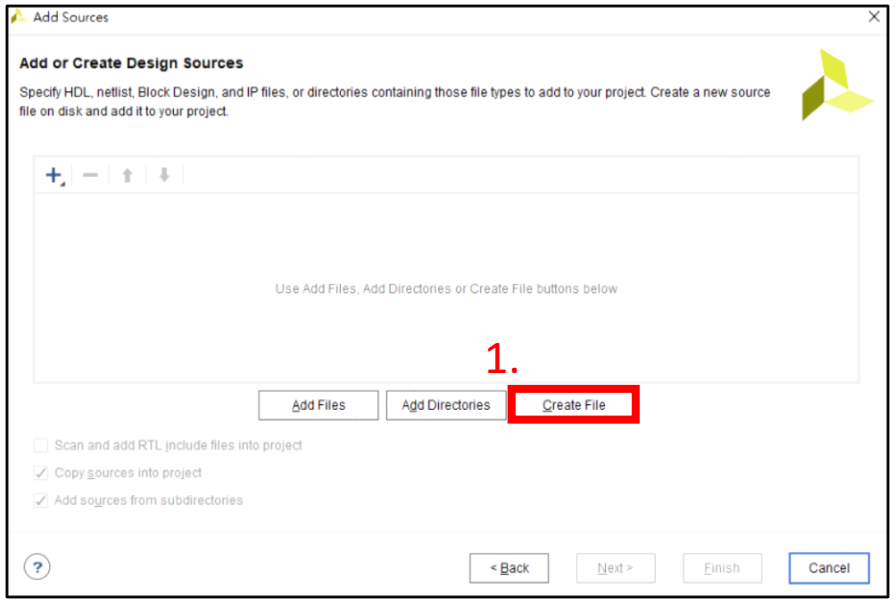
Vivado創建專案原始檔(2/3)

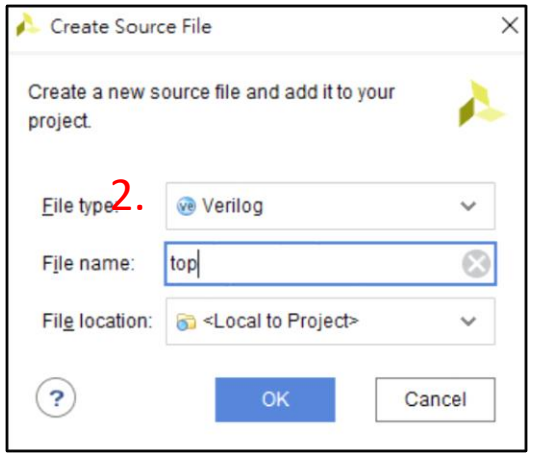
- 匯入.xdc檔
  - Add or create constraints > Next > Add files > 選擇下載的.xdc檔 > Finish

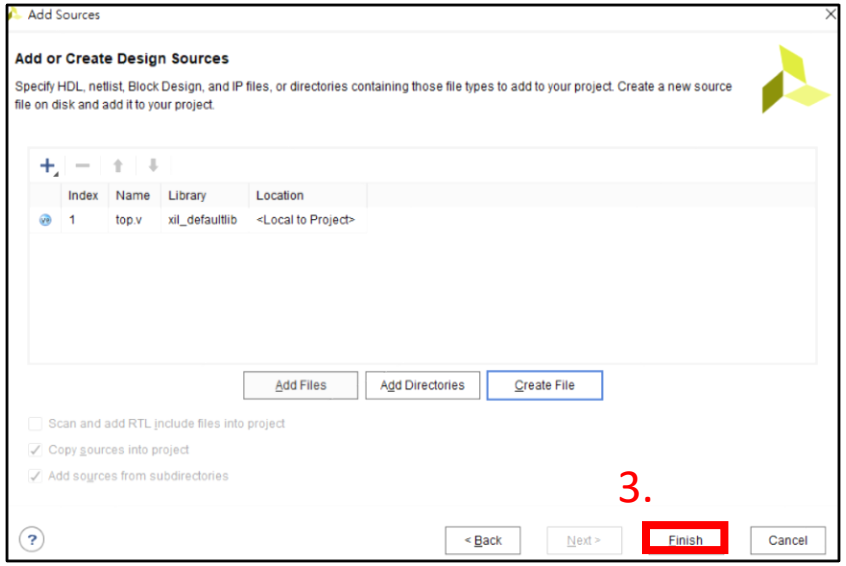


Vivado創建專案原始檔(3/3)

- 建立top.v檔
  - Add or create design sources > Next > Create file > 輸入檔名 > Finish







xdc檔設定

- Xilinx Design Constraints file(xdc file)
  - Nexys4上的周邊元件設定檔
  - 依據開發板上要用的元件PIN腳名稱去設定

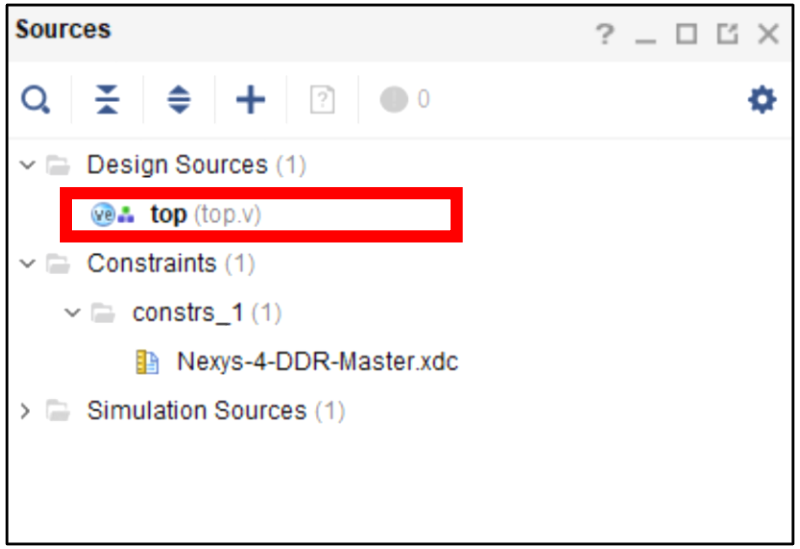

```
22  #set_property -dict { PACKAGE_PIN U8    IOSTANDARD LVCMOS18 } [get_ports { SW[9] }];
23  #set_property -dict { PACKAGE_PIN R16   IOSTANDARD LVCMOS33 } [get_ports { SW[10] }];
24  set_property -dict { PACKAGE_PIN T13    IOSTANDARD LVCMOS33 } [get_ports { SW[11] }];
25  set_property -dict { PACKAGE_PIN H6     IOSTANDARD LVCMOS33 } [get_ports { SW[12] }];
26  set_property -dict { PACKAGE_PIN U12    IOSTANDARD LVCMOS33 } [get_ports { SW[13] }];
27  set_property -dict { PACKAGE_PIN U11    IOSTANDARD LVCMOS33 } [get_ports { SW[14] }];
28  set_property -dict { PACKAGE_PIN V10    IOSTANDARD LVCMOS33 } [get_ports { SW[15] }];
```

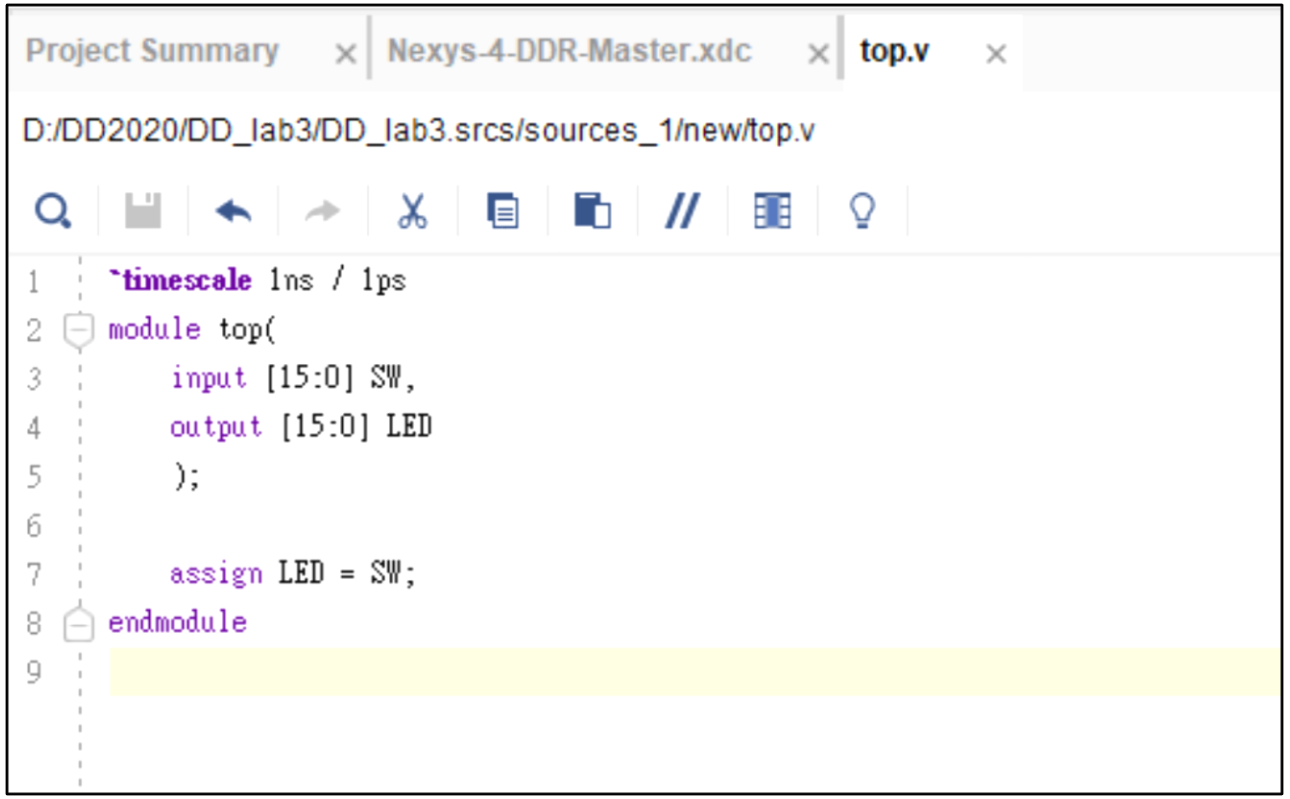
.xdc檔中對應PIN腳名稱

I/O名稱可自訂義

課堂實驗程式碼範例

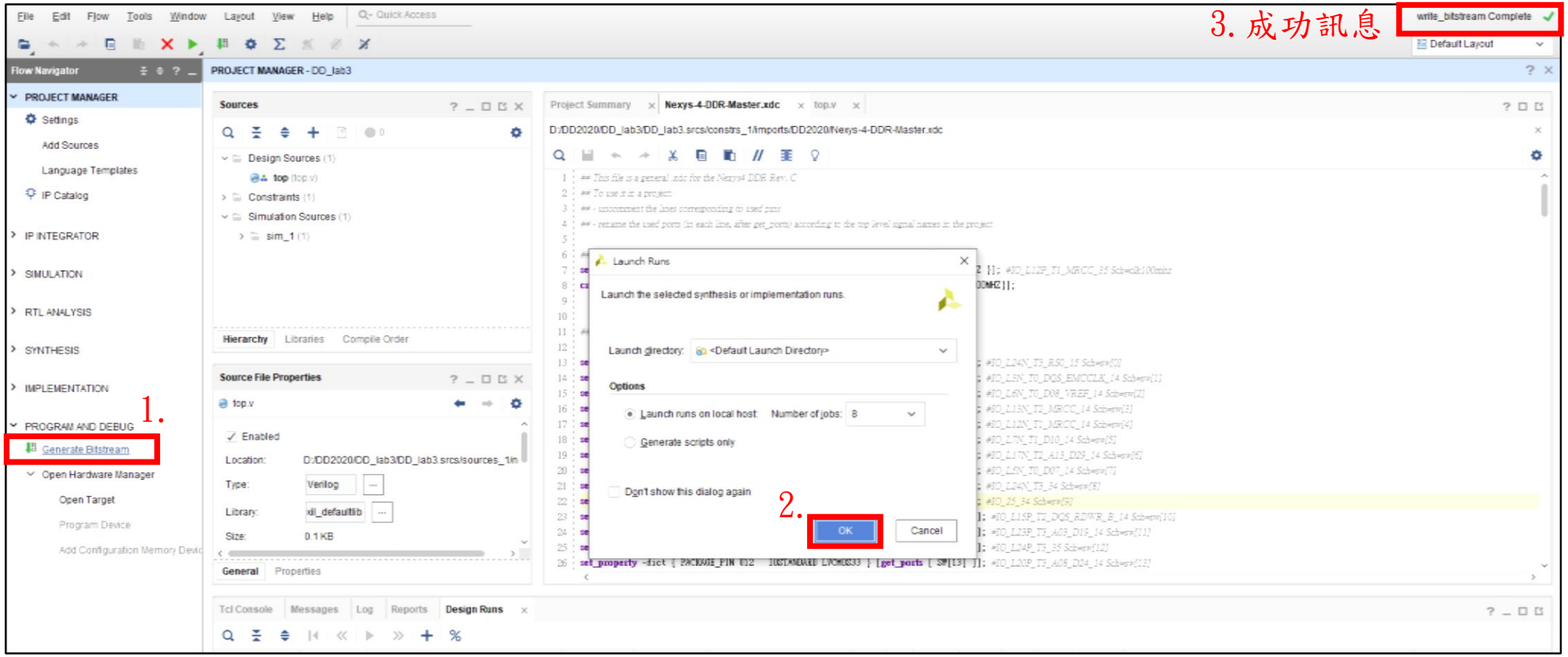
- 在左方欄位找到top.v並打開 > 輸入程式碼範例





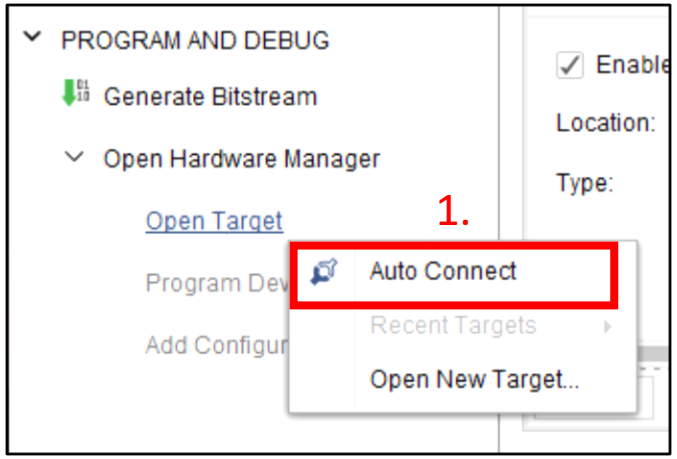
燒錄至FPGA(1/2)

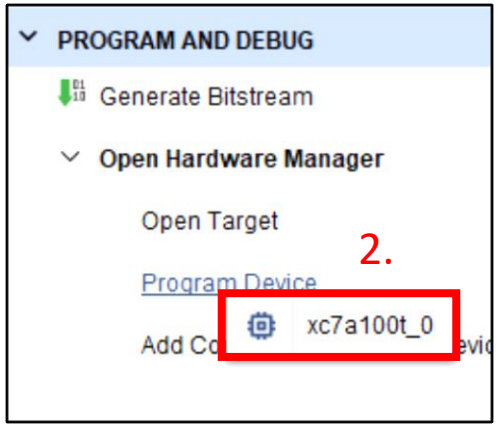
- 專案完成後要將電路燒錄至FPGA上
  - 左方欄位選擇Generate Bitstream > OK > 等待右上角跳出成功訊息

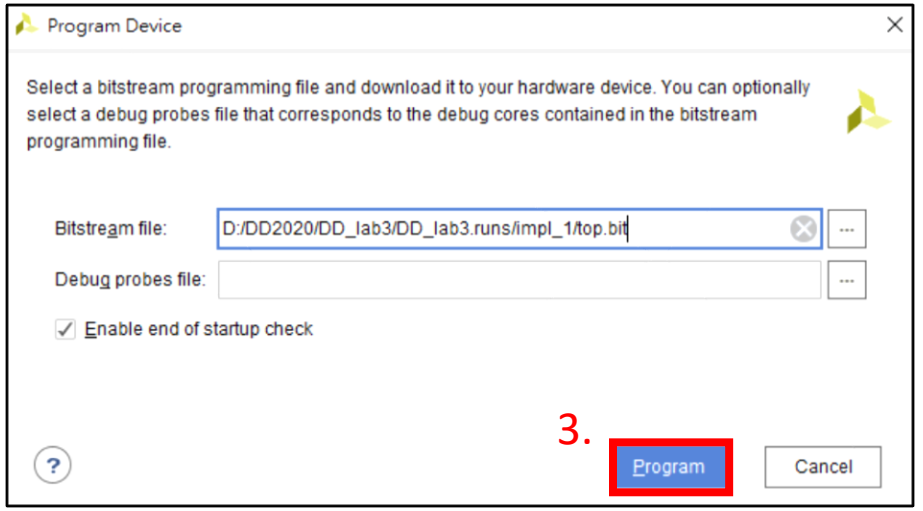


燒錄至FPGA(2/2)

- Open Target > Auto Connect > Program Device > Program
  (燒錄完後同學們可以確認switches是否能控制LED明滅)



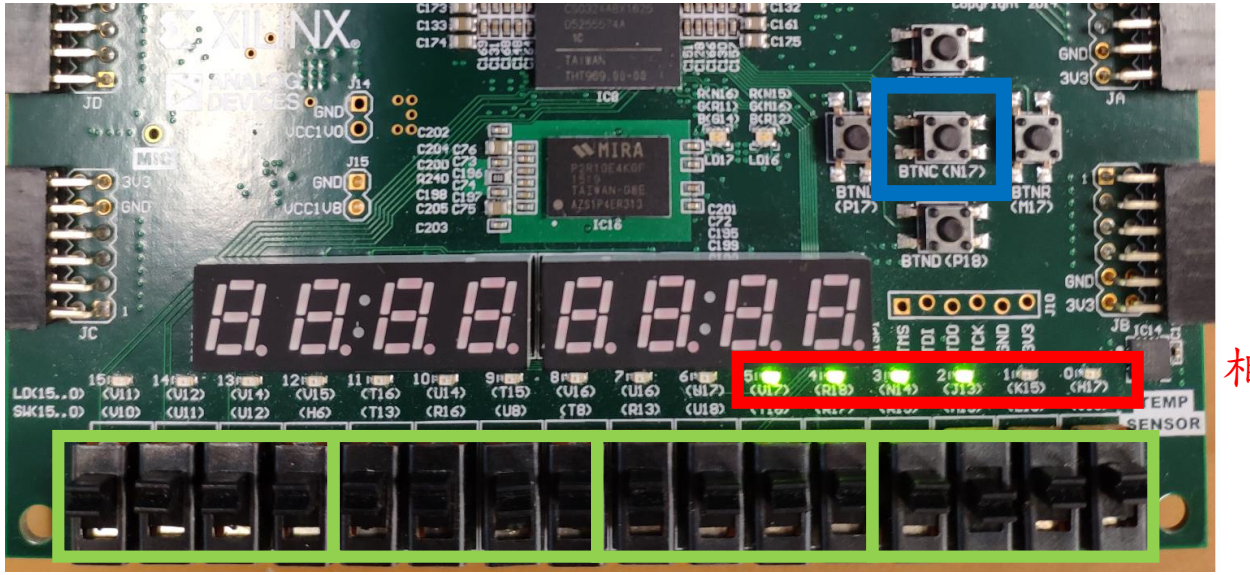




Lab作業

- 將Lab1作業四個4-bits的加法器在FPGA上實作，使用Nexys4開發板上從右到左每四個switches當作一個input，當按下button(N17)，就會將加法器相加結果以binary形式更新到LED上，相加結果以6-bits來表示。

按下button相加結果就更新



課程評分

- Demo時間:依E-Course公布為準
- Demo梯次:依E-Course公布為準
- Demo地點:501A
- 課程評分方式
  - Lab作業加法器相加結果呈現在LED(60%)
  - 有用button更新相加值(40%)

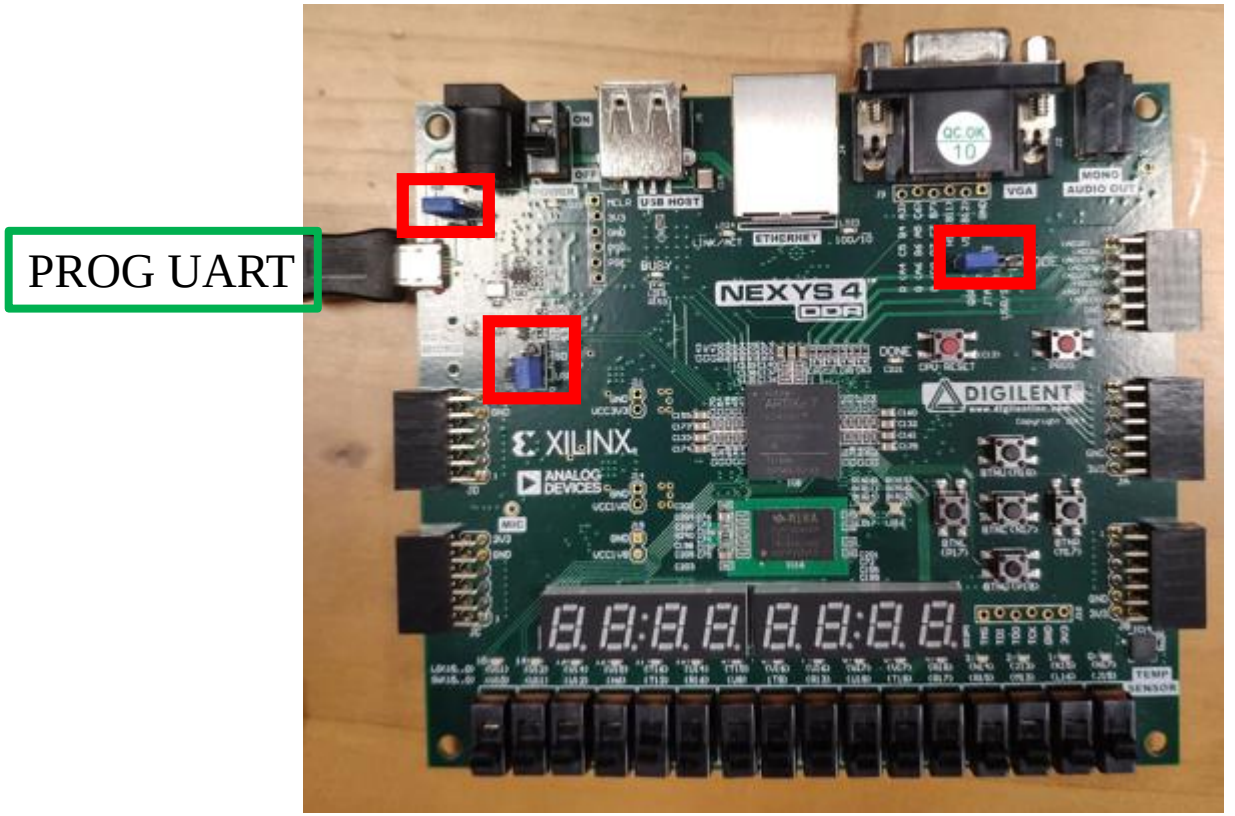
記得填寫意見回饋表，否則不予以計分

附錄

- 實驗環境架設
- Vivado安裝

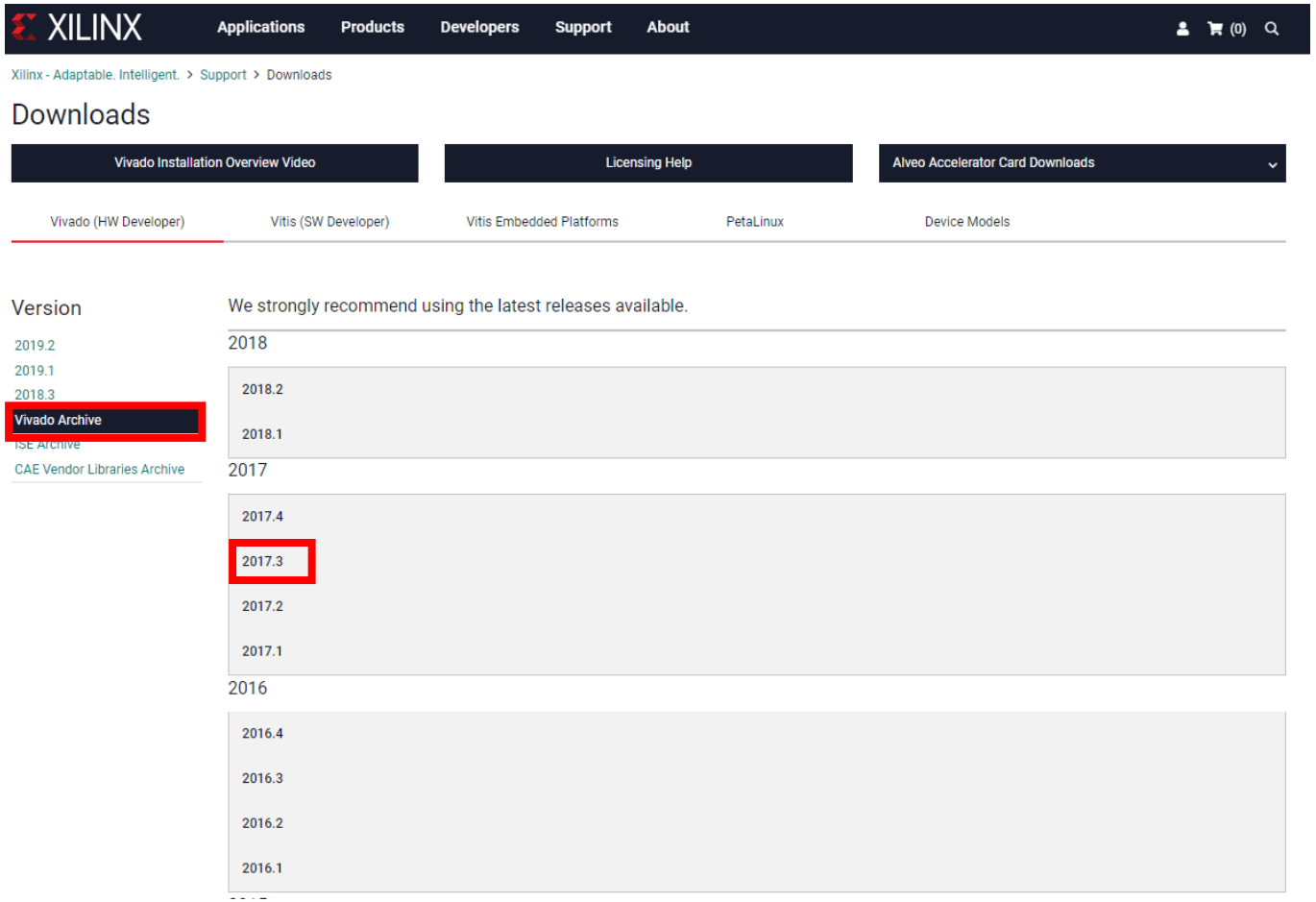
實驗環境架設

■ 同學們請確認Jumper和下圖一致，若有不同可能會造成Nexys4開發板沒辦法正常運作。



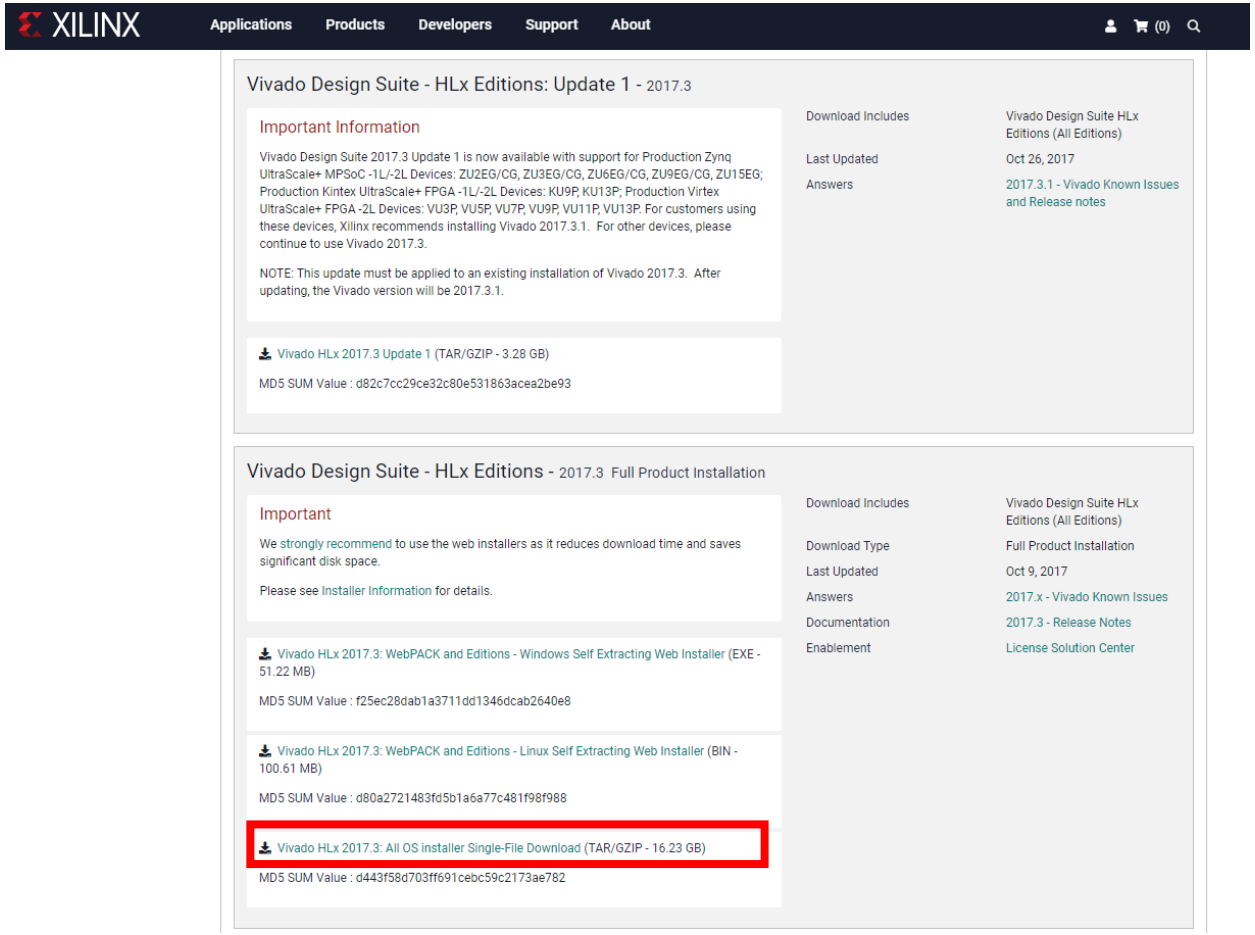
Vivado安裝(1/9)

- 前往下載網址>https://www.xilinx.com/support/download.html
- Vivado Archive > 2017.3



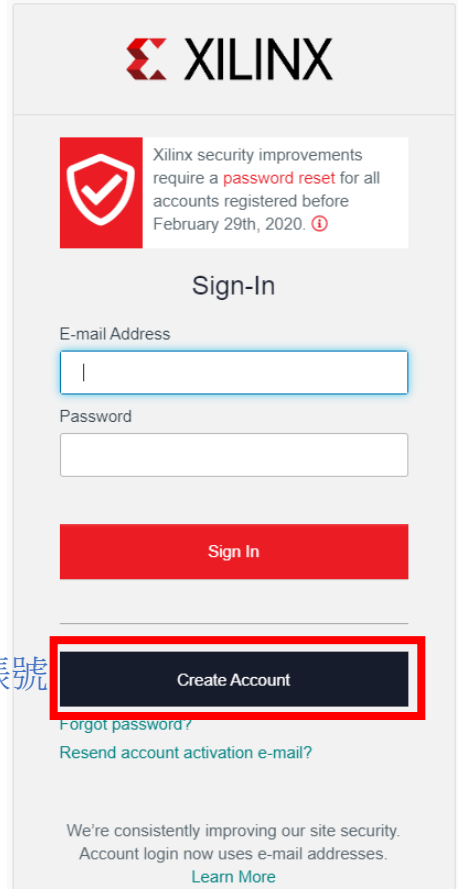
Vivado安裝(2/9)

- 選擇All OS版本

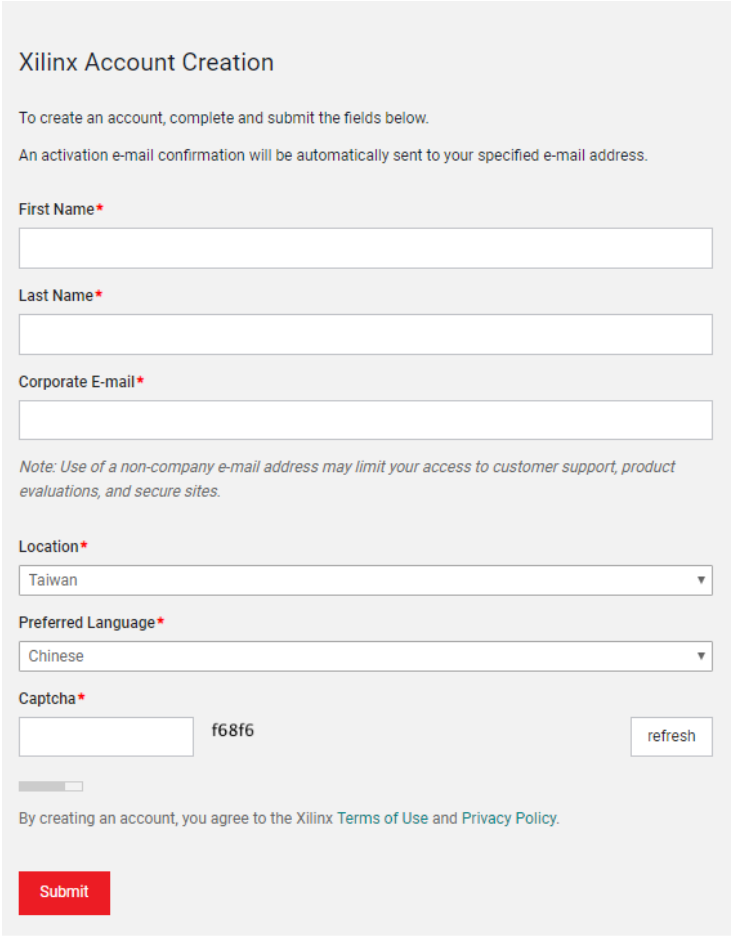


Vivado安裝(3/9)

- 註冊XILINX帳號 > 填寫表單 > email認證

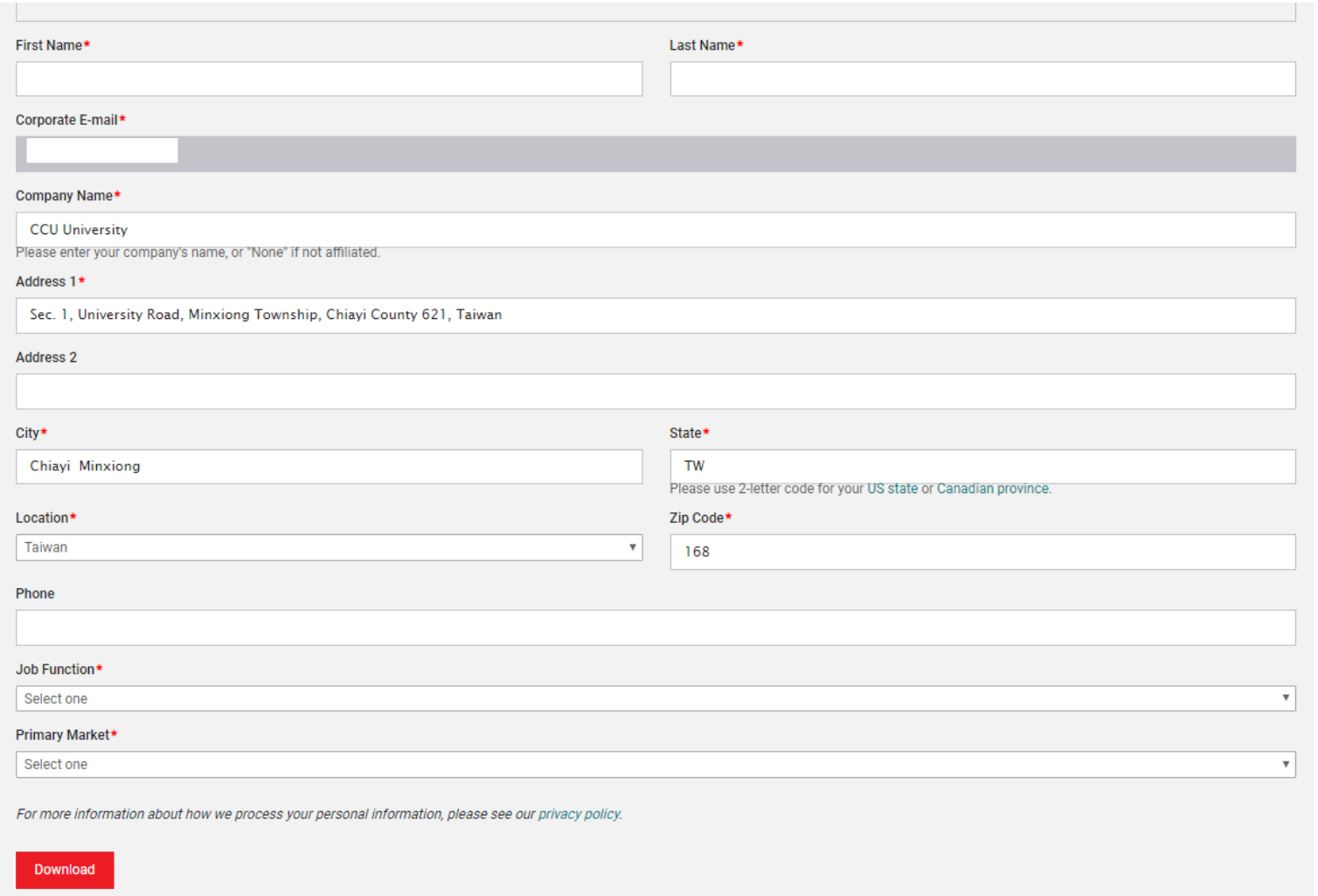


註冊帳號



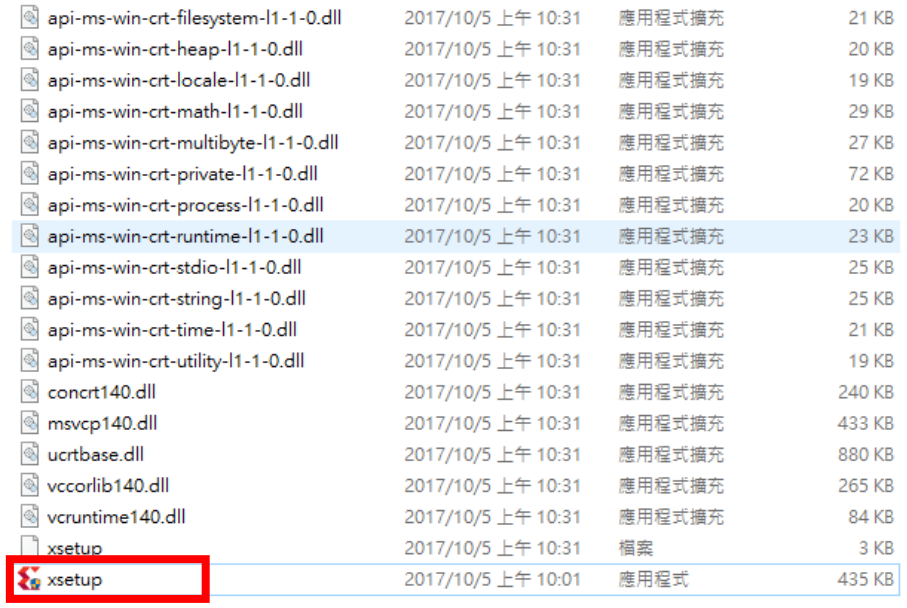
Vivado安裝(4/9)

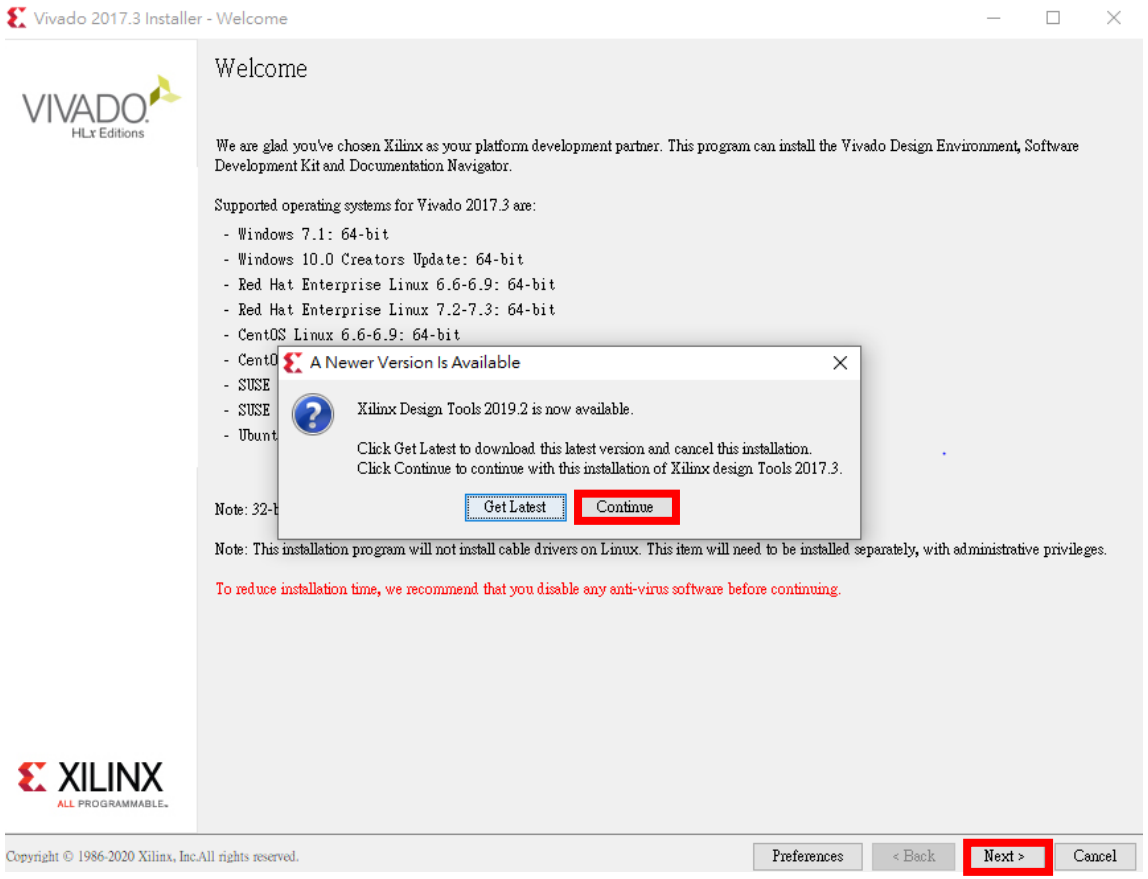
■ 登入完後填寫表單開始下載



Vivado安裝(5/9)

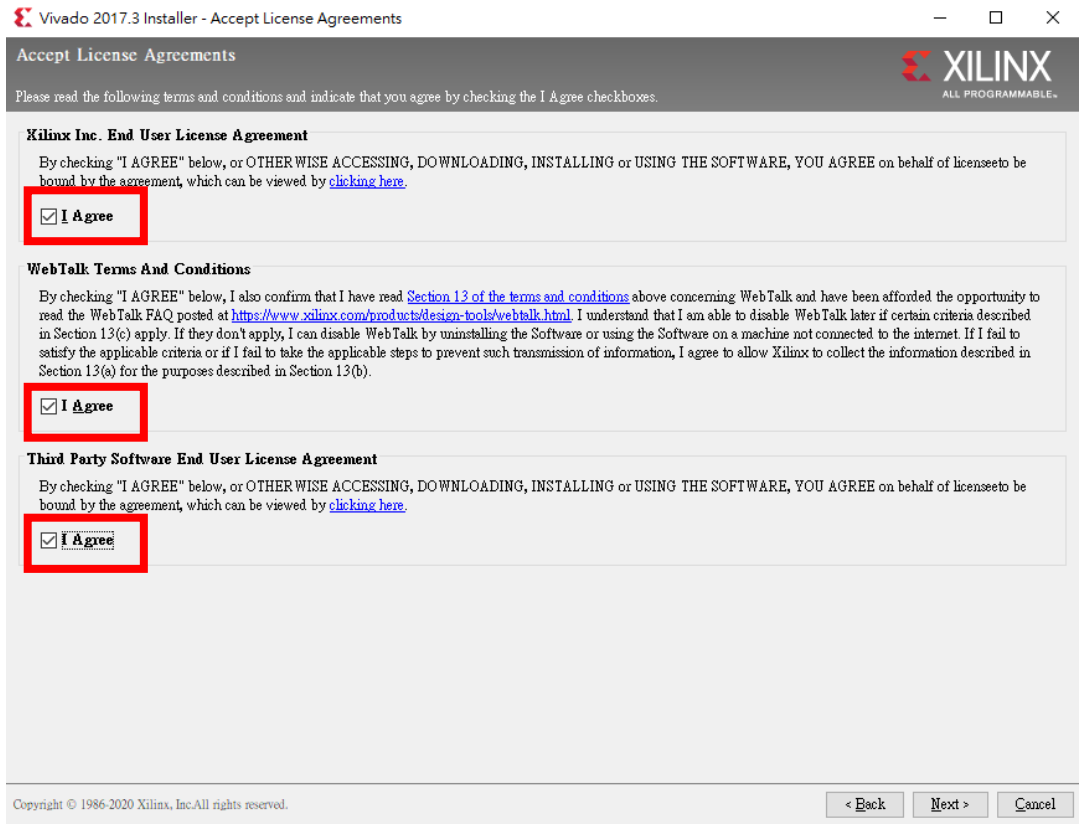
■ 下載完後解壓縮

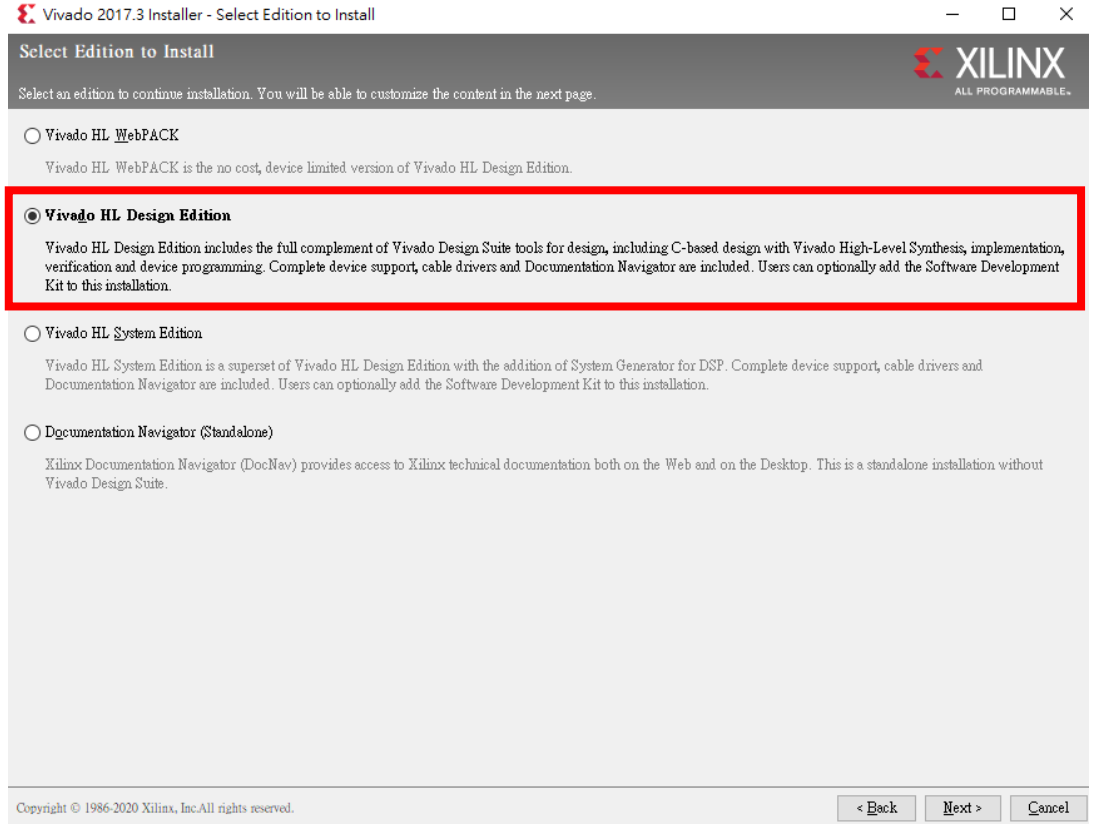




Vivado安裝(6/9)

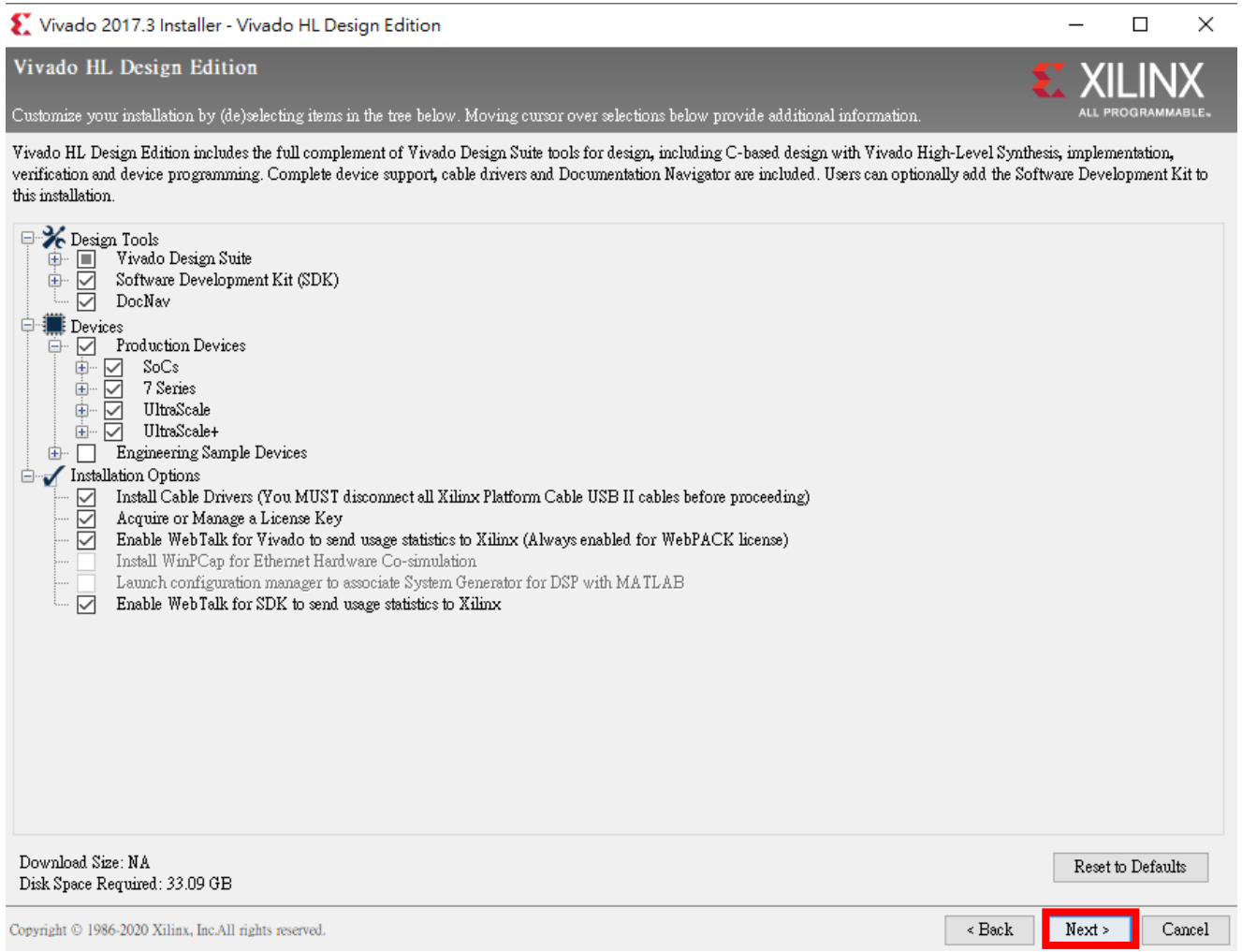
- 按照下圖勾選





Vivado安裝(7/9)

- 按照下圖勾選



Vivado安裝(8/9)

- 等待安裝

Vivado安裝(9/9)

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- 啟動Vivado > Help > Manage License
- Load License > Copy License > 選擇剛剛下載的License