

A decorative graphic featuring a thin brown circle on the left side. A thick brown horizontal bar extends from the circle towards the right. On the left end of this bar, there is a large, bold, black left square bracket '['. On the right end of the bar, there is a large, thin, brown right square bracket ']' that also encloses the text 'Digital Design Lab'.

Digital Design Lab

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Digital Design Lab

- 離線教學、課堂展示
- Office Hour：每週四下午2點至6點
- 12 Labs：60% 期末上機考試：40%
- 安排時段無法展示請即刻離場，違者一次扣總成績5分
- 可提前一時段到場準備，其餘時間違規進入，一次扣總成績3分
- 沒有任何保證的調分機制，如：「全勤分數」

Lab Modules

No.	Lab	Sim.	FPGA
1	Overview 1/2 (3-/4-op unsigned 4b adds)	<input type="checkbox"/>	
2	Overview 2/2 (signed adds)	<input type="checkbox"/>	
3	Nexys4 & Vivado (4-op unsigned adds)		<input type="checkbox"/>
4	7-seg display (binary to decimal)		<input type="checkbox"/>
5	Counter & birthdate display		<input type="checkbox"/>
6	CLA	<input type="checkbox"/>	
7	8b unsigned/signed MPY	<input type="checkbox"/>	
8	8b unsigned MPY		<input type="checkbox"/>
9	8b signed MPY		<input type="checkbox"/>
10	8b serial MPY		<input type="checkbox"/>
11	BF16 to decimal display		<input type="checkbox"/>
12	BF16 +1, +100, x2x, x3x, x10 display		<input type="checkbox"/>

Evaluation Form

- 學習目標 (教師填寫)
- 教學影片 (沒意見, 優點, 改善建議)
- 實驗講義 (沒意見, 優點, 改善建議)
- Office Hour (沒使用, 優點, 改善建議)
- 成果驗收 (沒意見, 優點, 改善建議)
- 學習成效概述及心得

務必繳交每次的Evaluation Form, 此為期末調分的主要依據