

Diglient Nexys4 FPGA Board & Xilinx Vivado Development Suite

DD Lab3

助教:徐瑋程、張宇秀



Department of Electrical Engineering and SoC Research Center National Chung Cheng University

Outline

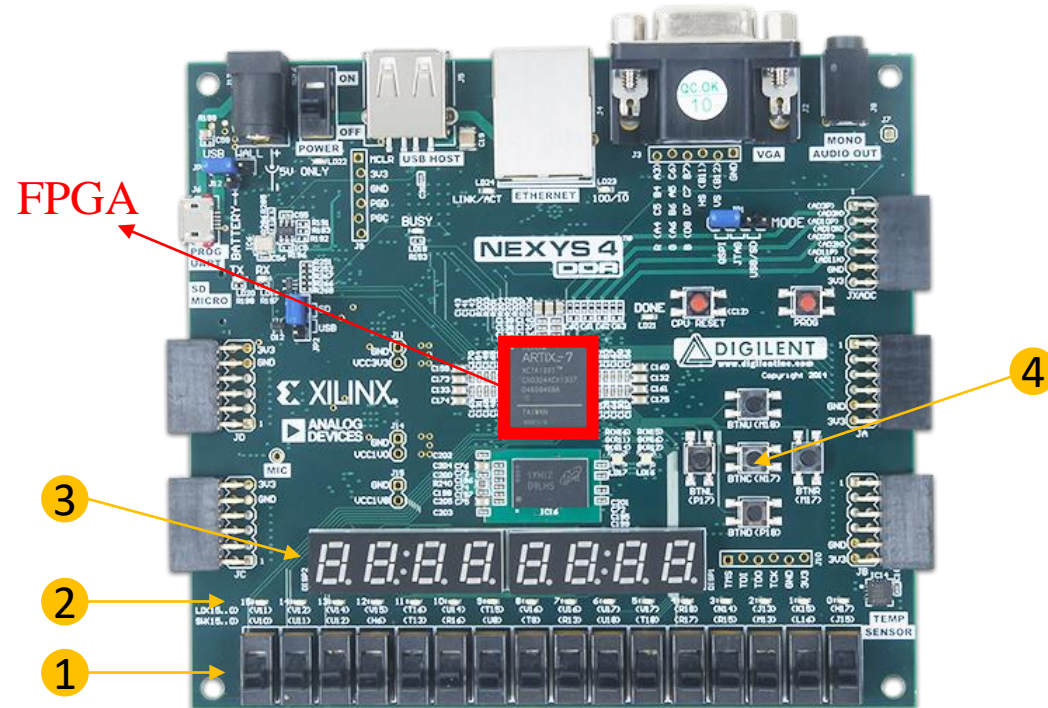
- 課程目的
- 課程工具介紹
- 課程實驗內容
- Lab作業
- 課程評分方式
- 附錄

課程目的

在本次Lab中，同學們將會學到如何利用Vivado開發工具將前一堂課的四個4-bit adder燒錄到Nexys4 FPGA開發板上，並透過Nexys4上的switch、LED等周邊驗證RTL電路設計的正確性

課程工具

- Nexys4上的FPGA可以用RTL來描述其電路行為
- Nexys4上有現成的電路像是LED、switch、七段顯示器等開發板周邊，可用作FPGA的輸入以及輸出



Callout	Component Description
1	switch(16)
2	LED(16)
3	7-segment display(8)
4	push button(5)

課程實驗

■ 課程實驗項目

- 用16顆switches (sw0~sw15)分別控制16顆LED (led0~led15)的明滅

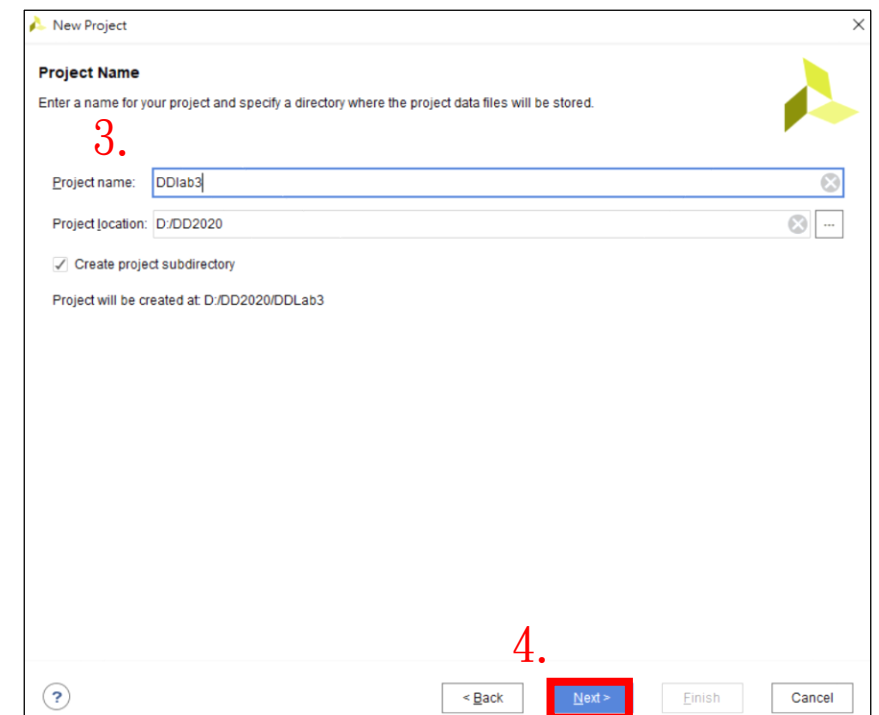
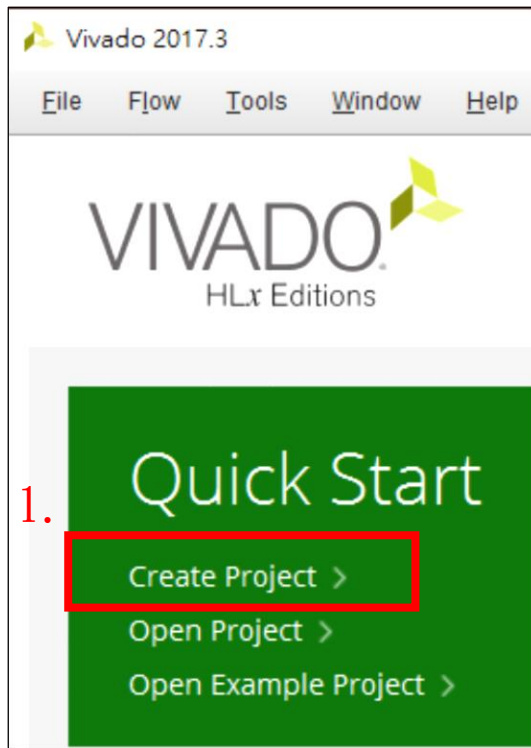


■ 實驗教學內容

- Vivado建立專案
- Vivado創建專案原始檔
- .xdc檔設定
- 產生bit檔並燒入至Nexys4

Vivado建立專案(1/4)

- 建立課堂練習專案
- 開啟 Vivado > Create Project > Next > 輸入專案名稱 > Next



Vivado建立專案(2/4)

■ 選擇RTL Project > Next > Next

New Project

Project Type
Specify the type of project to create.

1.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
☐ Do not specify sources at this time

☐ **Post-synthesis Project**: You will be able to add sources, view device resources, run design analysis, planning and implementation.
☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.

2.

New Project

Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Use Add Files, Add Directories or Create File buttons below

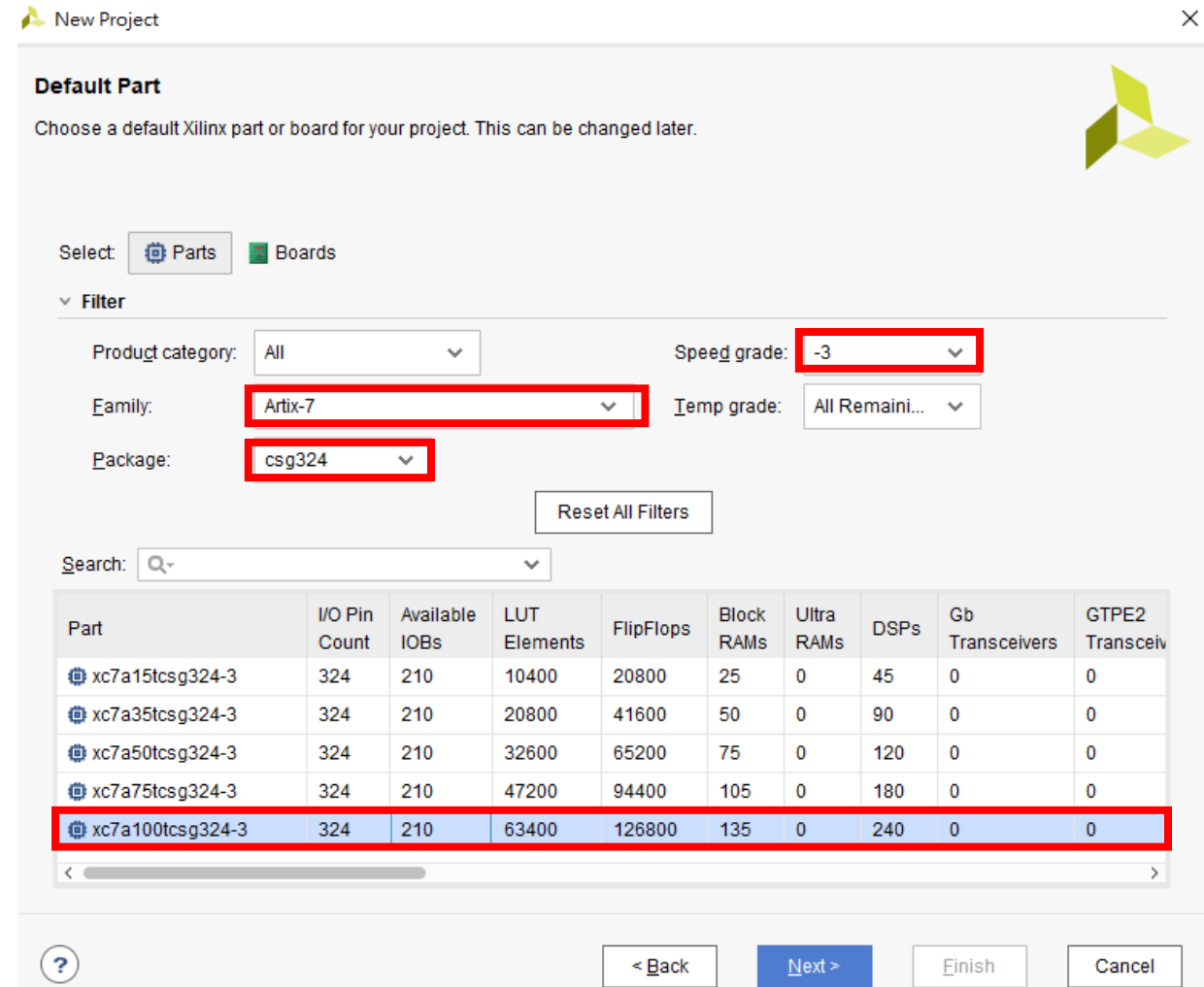
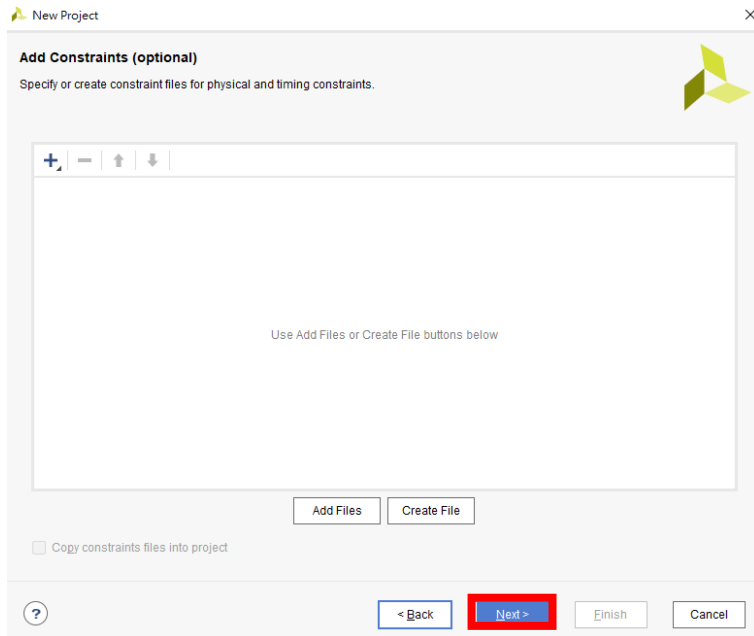
☐ Scan and add RTL include files into project
☐ Copy sources into project
☒ Add sources from subdirectories

Target language: Verilog Simulator language: Mixed

3.

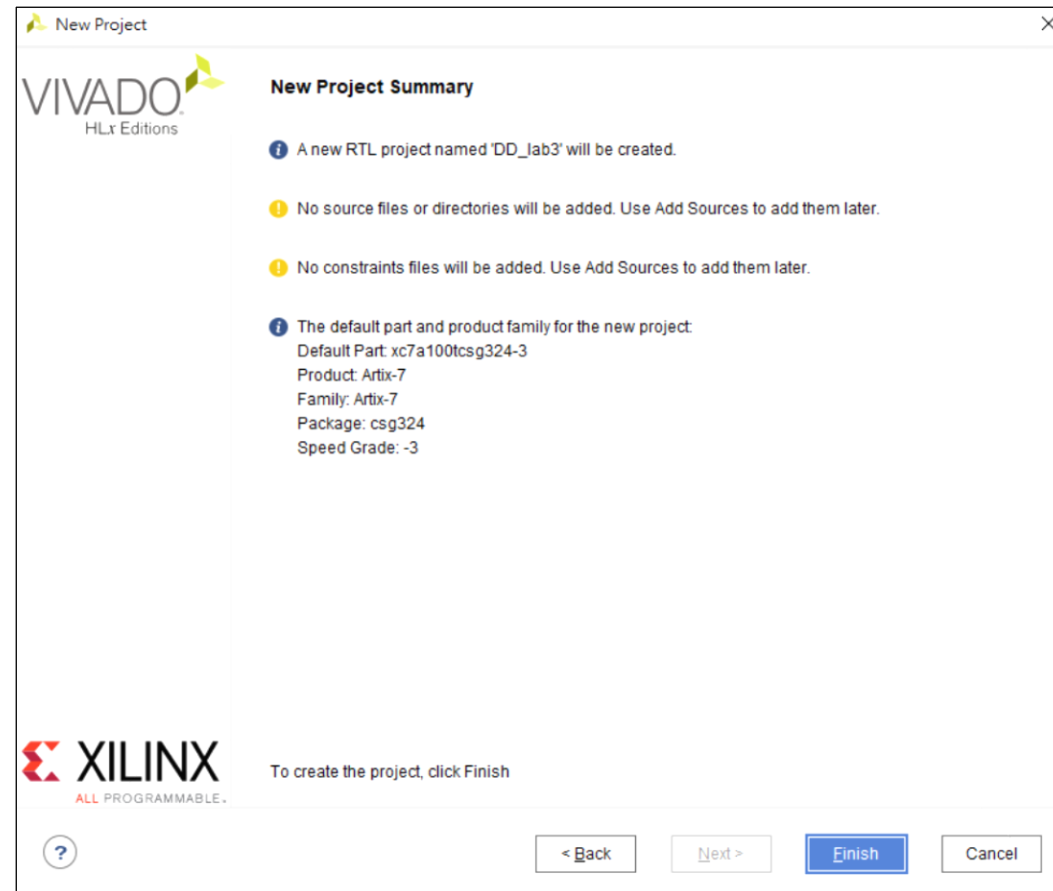
Vivado建立專案(3/4)

■ Next > Family:Artix-7 > Package:csg324 > Speed grade:-3 > xc7a100tcsg324-3



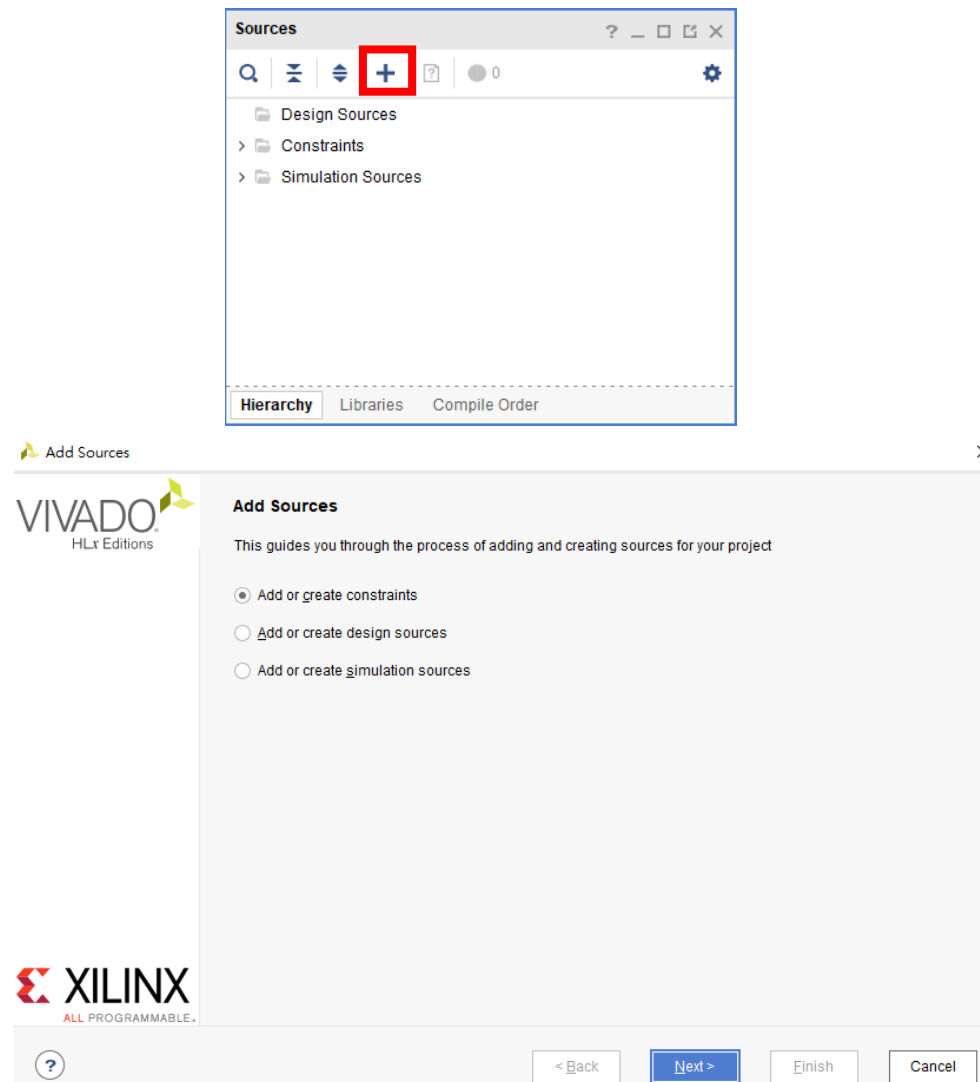
Vivado建立專案(4/4)

■ Finish



Vivado創建專案原始檔(1/3)

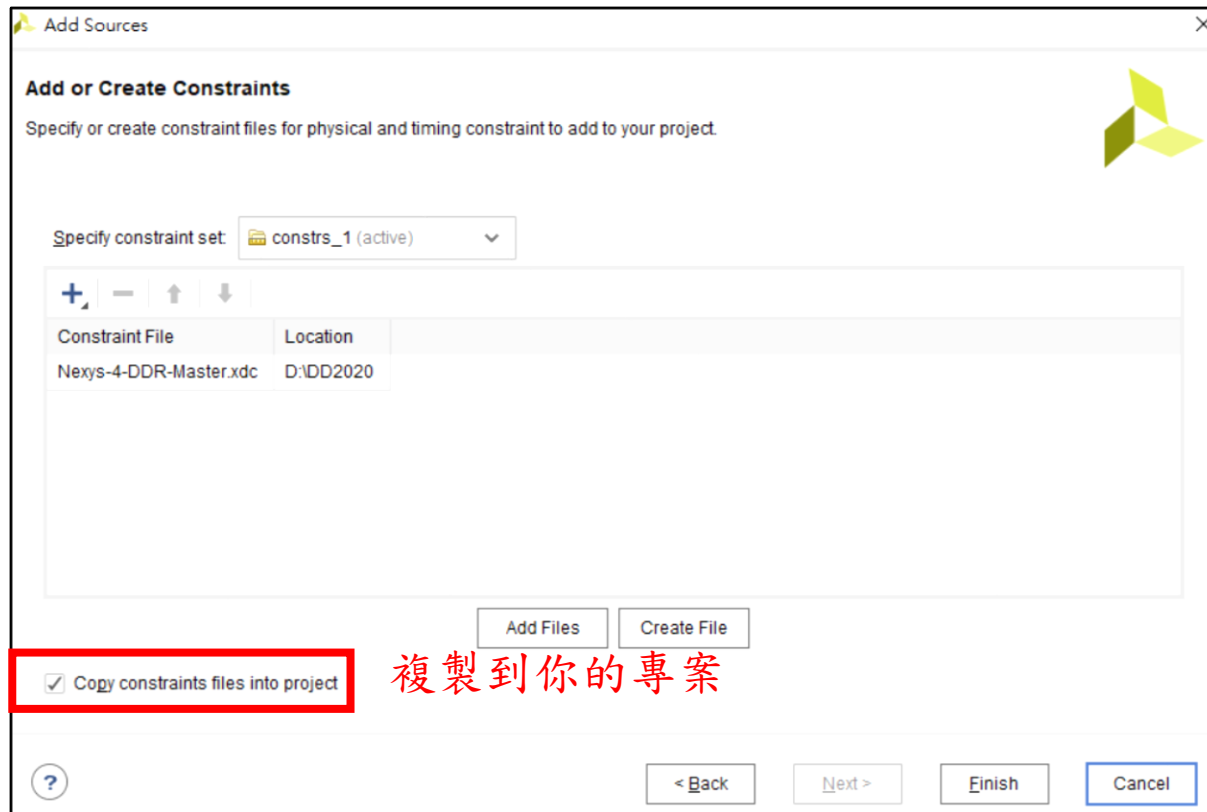
- 按加號新增檔案
- 選擇檔案類型 > Add or create constraints
 - constraints :新增.xdc檔
.xdc用來描述.v與實體線路的連接關係
 - design sources :新增.v檔
.v用來描述硬體行為



Vivado創建專案原始檔(2/3)

■ 匯入.xdc檔

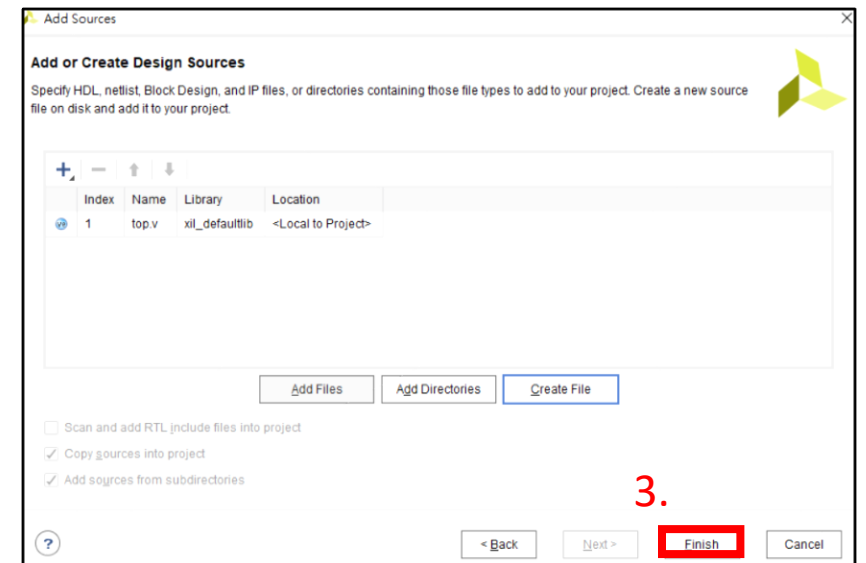
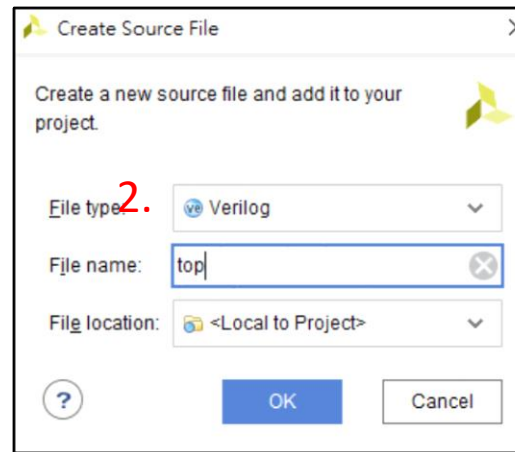
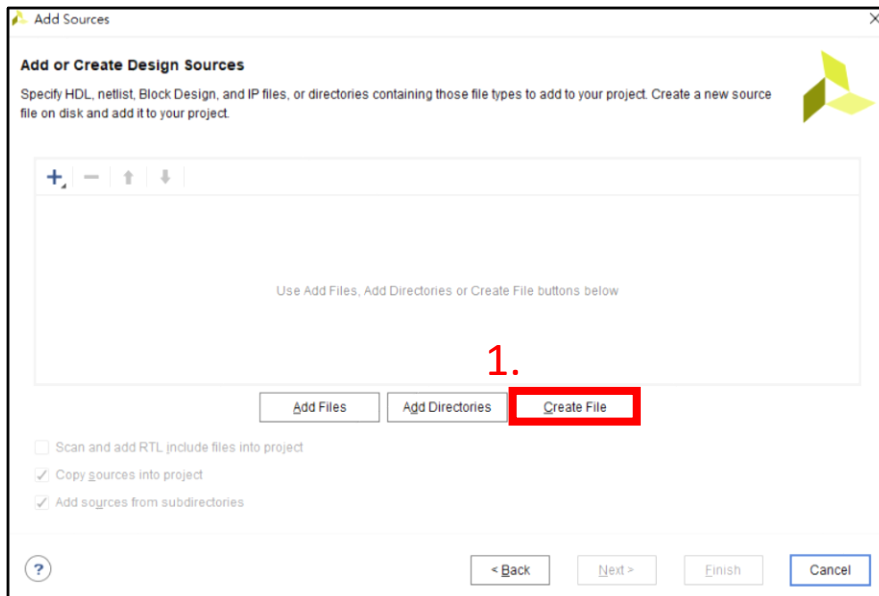
□ Add or create constraints > Next > Add files > 選擇下載的.xdc檔 > Finish



Vivado創建專案原始檔(3/3)

■ 建立top.v檔

□ Add or create design sources > Next > Create file > 輸入檔名 > Finish



xdc檔設定

- Xilinx Design Constraints file(xdc file)
 - Nexys4上的周邊元件設定檔
 - 依據開發板上要用的元件PIN腳名稱去設定



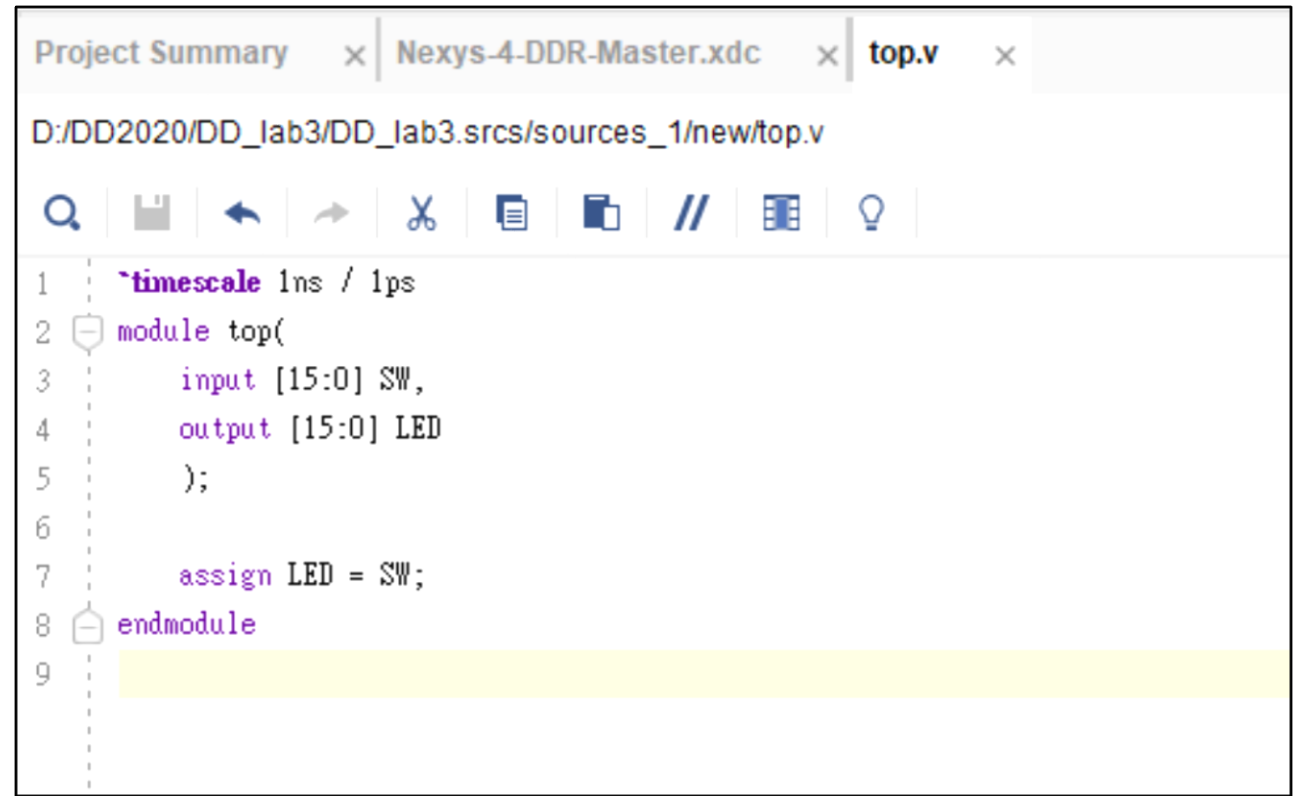
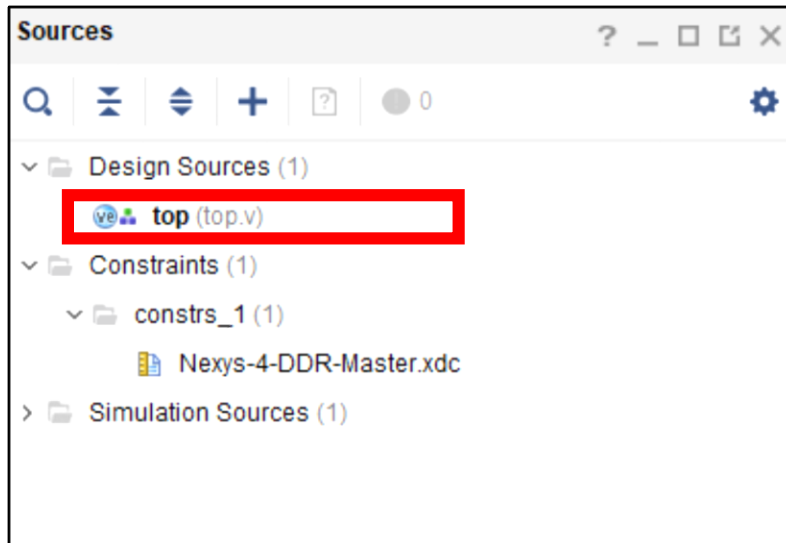
```
22 #set_property -dict { PACKAGE_PIN U8  IOSTANDARD LVCMOS18 } [get_ports { SW[9] }];
23 #set_property -dict { PACKAGE_PIN R16  IOSTANDARD LVCMOS33 } [get_ports { SW[10] }];
24 set_property -dict { PACKAGE_PIN T13  IOSTANDARD LVCMOS33 } [get_ports { SW[11] }];
25 set_property -dict { PACKAGE_PIN H6   IOSTANDARD LVCMOS33 } [get_ports { SW[12] }];
26 set_property -dict { PACKAGE_PIN U12  IOSTANDARD LVCMOS33 } [get_ports { SW[13] }];
27 set_property -dict { PACKAGE_PIN U11  IOSTANDARD LVCMOS33 } [get_ports { SW[14] }];
28 set_property -dict { PACKAGE_PIN V10  IOSTANDARD LVCMOS33 } [get_ports { SW[15] }];
```

.xdc檔中對應PIN腳名稱

I/O名稱可自訂義

課堂實驗程式碼範例

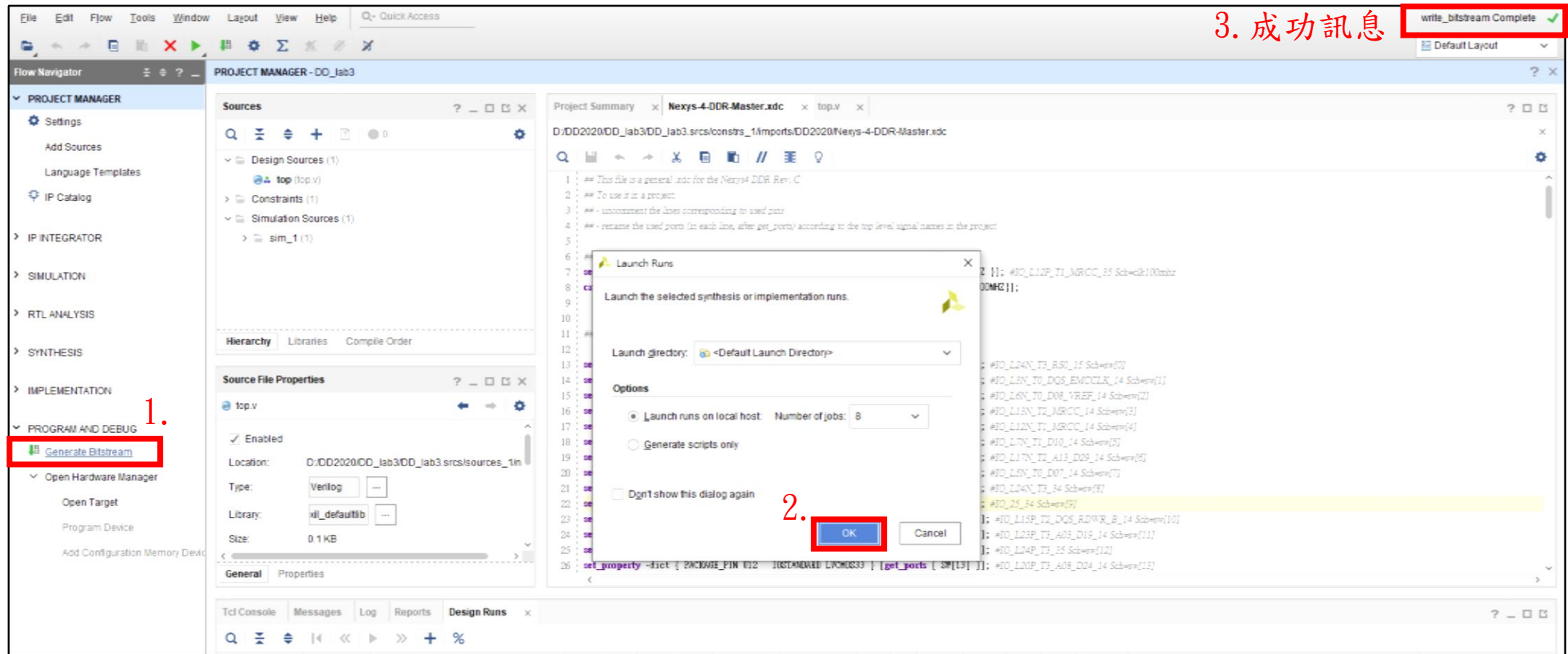
- 在左方欄位找到top.v並打開 > 輸入程式碼範例



燒錄至FPGA(1/2)

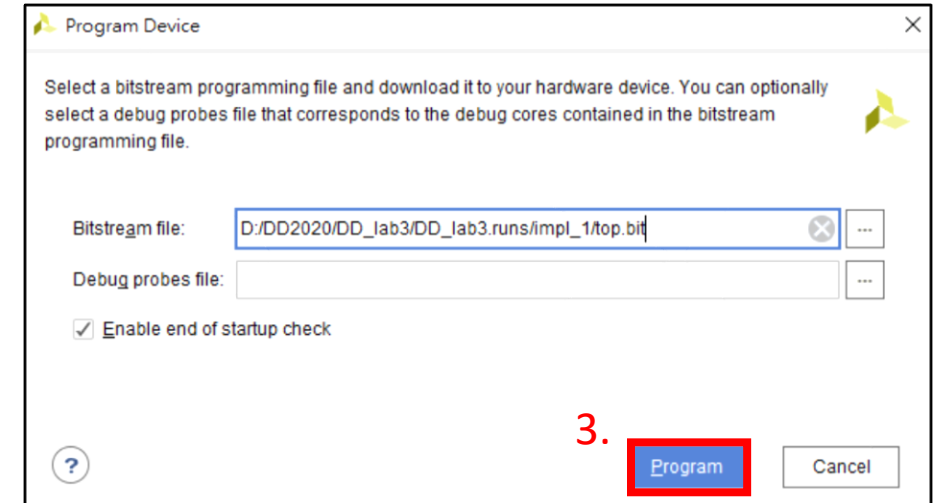
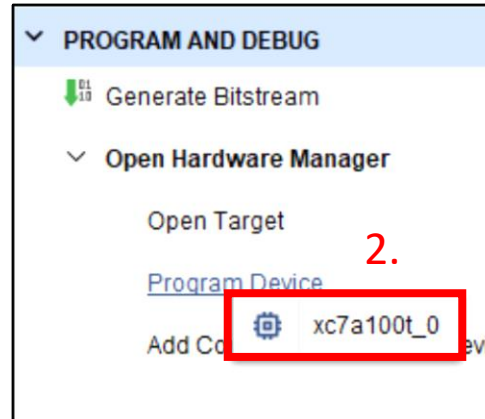
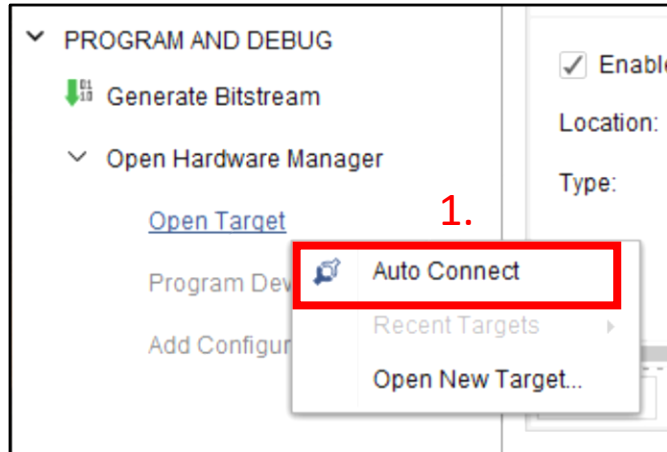
■ 專案完成後要將電路燒錄至FPGA上

□ 左方欄位選擇Generate Bitstream > OK > 等待右上角跳出成功訊息



燒錄至FPGA(2/2)

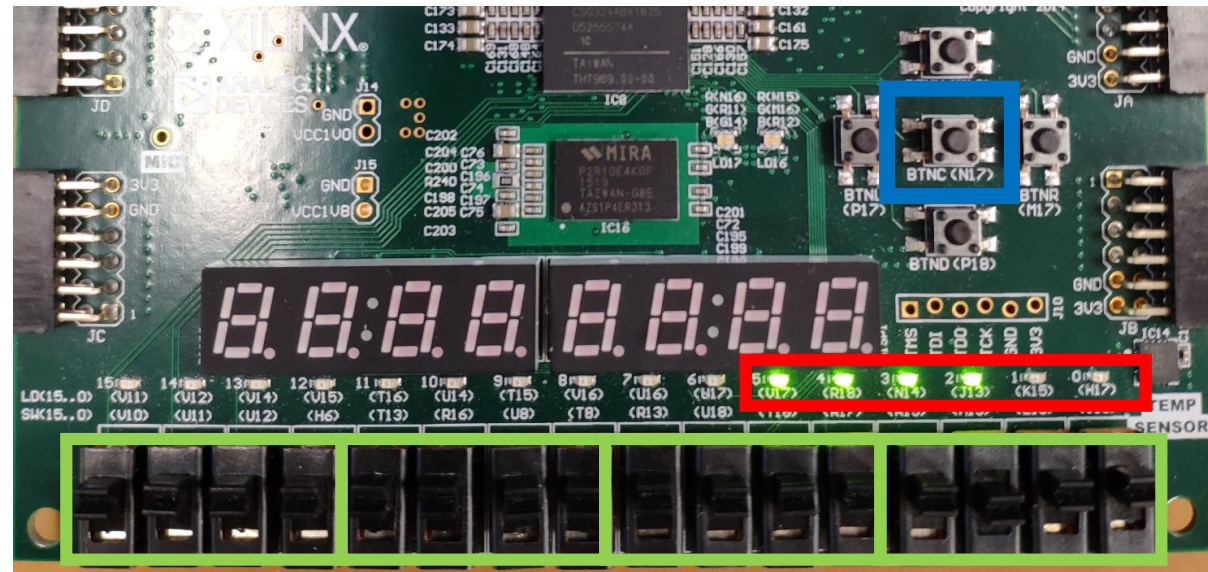
- Open Target > Auto Connect > Program Device > Program
(燒錄完後同學們可以確認switches是否能控制LED明滅)



Lab作業

- 將Lab1作業四個4-bits的加法器在FPGA上實作，使用Nexys4開發板上從右到左每四個switches當作一個input，當按下button(N17)，就會將加法器相加結果以binary形式更新到LED上，相加結果以6-bits來表示。

按下button相加結果就更新



相加結果

input d[3:0] input c[3:0] input b[3:0] input a[3:0]

課程評分

- Demo時間:依E-Course公布為準
- Demo梯次:依E-Course公布為準
- Demo地點:501A
- 課程評分方式
 - Lab作業加法器相加結果呈現在LED(60%)
 - 有用button更新相加值(40%)

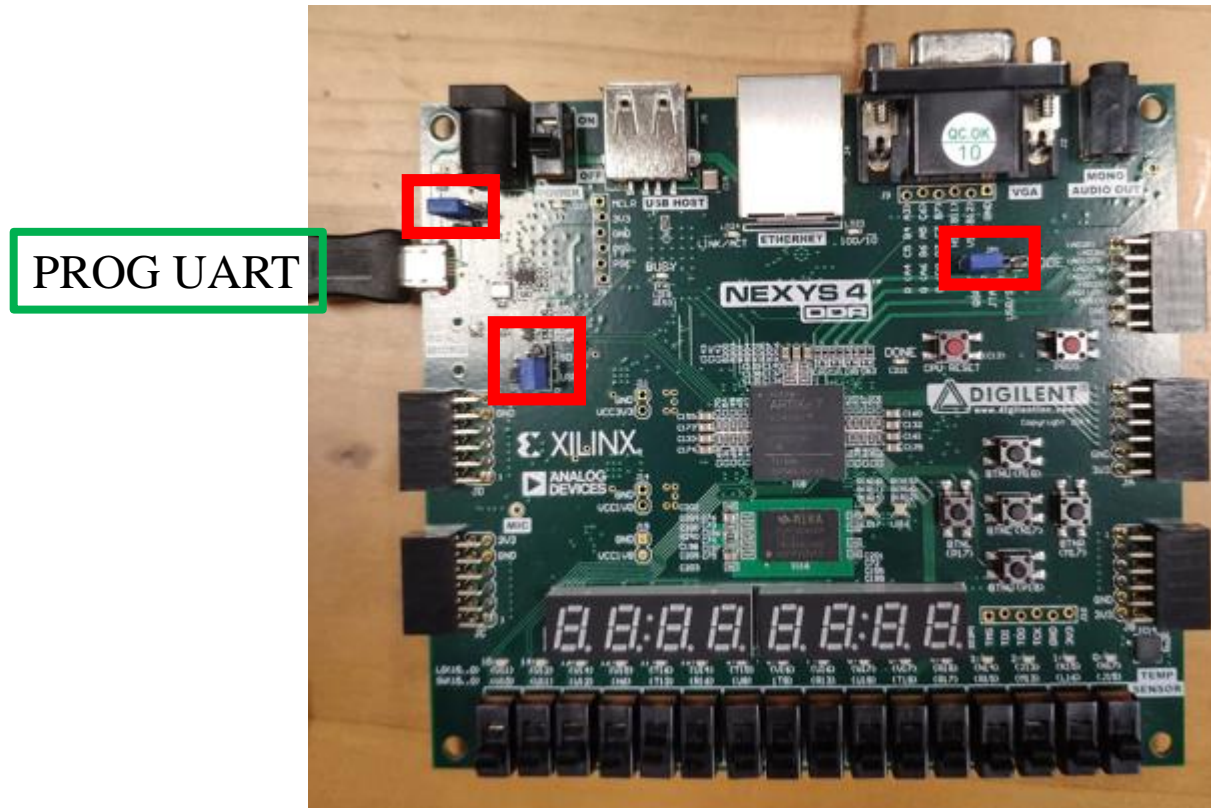
記得填寫意見回饋表，否則不予以計分

附錄

- 實驗環境架設
- Vivado安裝

實驗環境架設

- 同學們請確認**Jumper**和下圖一致，若有不同可能會造成Nexys4開發板沒辦法正常運作。



Vivado安裝(1/9)

- 前往下載網址><https://www.xilinx.com/support/download.html>
- Vivado Archive > 2017.3

The screenshot shows the Xilinx website's Downloads page. The navigation bar at the top includes the XILINX logo and links for Applications, Products, Developers, Support, and About. Below the navigation bar, the page title is "Downloads". There are three main sections: "Vivado Installation Overview Video", "Licensing Help", and "Alveo Accelerator Card Downloads". Under the "Vivado Installation Overview Video" section, there are five sub-sections: "Vivado (HW Developer)", "Vitis (SW Developer)", "Vitis Embedded Platforms", "PetaLinux", and "Device Models". The "Vivado (HW Developer)" section is selected. On the left side, there is a "Version" list with links for 2019.2, 2019.1, 2018.3, Vivado Archive (highlighted with a red box), ISE Archive, and CAE Vendor Libraries Archive. The main content area displays a message: "We strongly recommend using the latest releases available." Below this, there are three large boxes representing the years 2018, 2017, and 2016. The 2017 box is expanded, showing a list of versions: 2017.4, 2017.3 (highlighted with a red box), 2017.2, and 2017.1. The 2016 box is also expanded, showing versions 2016.4, 2016.3, 2016.2, and 2016.1.

XILINX Applications Products Developers Support About

Xilinx - Adaptable. Intelligent. > Support > Downloads

Downloads

Vivado Installation Overview Video Licensing Help Alveo Accelerator Card Downloads

Vivado (HW Developer) Vitis (SW Developer) Vitis Embedded Platforms PetaLinux Device Models

Version

2019.2
2019.1
2018.3
Vivado Archive
ISE Archive
CAE Vendor Libraries Archive

We strongly recommend using the latest releases available.

2018

2018.2
2018.1

2017


2017.4
2017.3
2017.2
2017.1

2016

2016.4
2016.3
2016.2
2016.1

Vivado安裝(2/9)

■ 選擇All OS版本

 Applications Products Developers Support About 👤 🛒 (0) 🔍

Vivado Design Suite - HLx Editions: Update 1 - 2017.3

Important Information

Vivado Design Suite 2017.3 Update 1 is now available with support for Production Zynq UltraScale+ MPSoC -1L/-2L Devices: ZU2EG/CG, ZU3EG/CG, ZU6EG/CG, ZU9EG/CG, ZU15EG; Production Kintex UltraScale+ FPGA -1L/-2L Devices: KU9P, KU13P; Production Virtex UltraScale+ FPGA -2L Devices: VU3P, VU5P, VU7P, VU9P, VU11P, VU13P. For customers using these devices, Xilinx recommends installing Vivado 2017.3.1. For other devices, please continue to use Vivado 2017.3.

NOTE: This update must be applied to an existing installation of Vivado 2017.3. After updating, the Vivado version will be 2017.3.1.

Download Includes

Last Updated

Answers

Vivado Design Suite HLx Editions (All Editions)

Oct 26, 2017

[2017.3.1 - Vivado Known Issues and Release notes](#)

📄 Vivado HLx 2017.3 Update 1 (TAR/GZIP - 3.28 GB)

MD5 SUM Value : d82c7cc29ce32c80e531863acea2be93

Vivado Design Suite - HLx Editions - 2017.3 Full Product Installation

Important

We strongly recommend to use the web installers as it reduces download time and saves significant disk space.

Please see Installer Information for details.

Download Includes

Download Type

Last Updated

Answers

Documentation

Enablement

Vivado Design Suite HLx Editions (All Editions)

Full Product Installation

Oct 9, 2017

[2017.x - Vivado Known Issues](#)

[2017.3 - Release Notes](#)

[License Solution Center](#)

📄 Vivado HLx 2017.3: WebPACK and Editions - Windows Self Extracting Web Installer (EXE - 51.22 MB)

MD5 SUM Value : f25ec28dab1a3711dd1346dcab2640e8

📄 Vivado HLx 2017.3: WebPACK and Editions - Linux Self Extracting Web Installer (BIN - 100.61 MB)

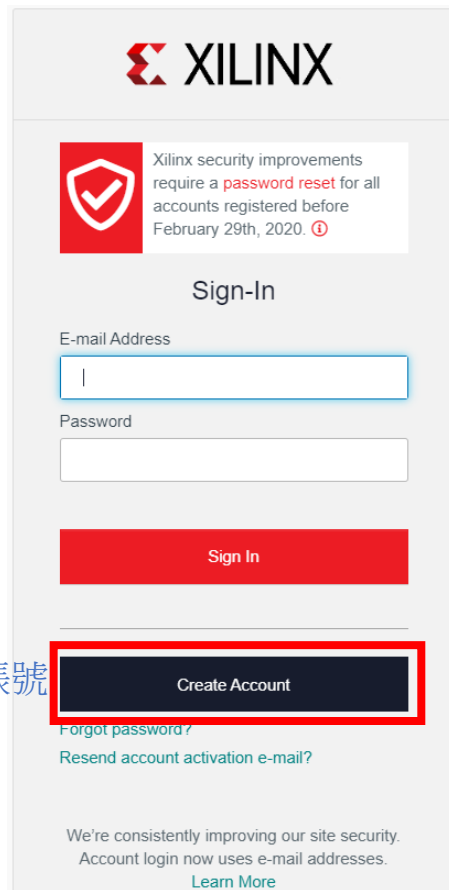
MD5 SUM Value : d80a2721483fd5b1a6a77c481f98f988

📄 Vivado HLx 2017.3: All OS Installer Single-File Download (TAR/GZIP - 16.23 GB)

MD5 SUM Value : d443f58d703ff691cebc59c2173ae782

Vivado安裝(3/9)

■ 註冊XILINX帳號 > 填寫表單 > email認證



The image shows the Xilinx website's login and registration interface. At the top is the XILINX logo. Below it is a security notice with a red shield icon. The 'Sign-In' section has fields for 'E-mail Address' and 'Password', followed by a red 'Sign In' button. Below the sign-in section is a 'Create Account' button, which is highlighted with a red rectangle. To the left of this button, the text '註冊帳號' is written in blue. At the bottom, there are links for 'Forgot password?' and 'Resend account activation e-mail?'. A footer note mentions site security improvements and a 'Learn More' link.

XILINX

Xilinx security improvements require a **password reset** for all accounts registered before February 29th, 2020. ⓘ

Sign-In

E-mail Address

Password

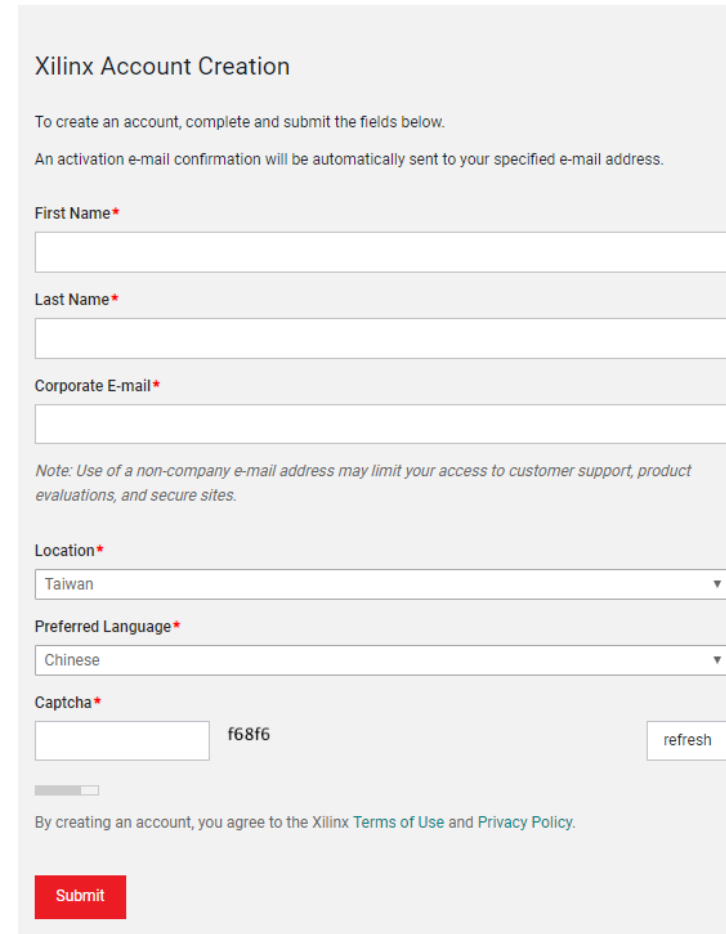
Sign In

註冊帳號 Create Account

[Forgot password?](#)

[Resend account activation e-mail?](#)

We're consistently improving our site security. Account login now uses e-mail addresses. [Learn More](#)



The image shows the 'Xilinx Account Creation' form. It starts with the title 'Xilinx Account Creation' and instructions to complete the fields below. A note states that an activation email will be sent. The form includes fields for 'First Name*', 'Last Name*', and 'Corporate E-mail*'. Below these is a note about using non-company email addresses. There are dropdown menus for 'Location*' (set to Taiwan) and 'Preferred Language*' (set to Chinese). A 'Captcha*' section shows a box with the text 'f68f6' and a 'refresh' button. At the bottom, there is a 'Submit' button and a checkbox for agreeing to the Terms of Use and Privacy Policy.

Xilinx Account Creation

To create an account, complete and submit the fields below.

An activation e-mail confirmation will be automatically sent to your specified e-mail address.

First Name*

Last Name*

Corporate E-mail*

Note: Use of a non-company e-mail address may limit your access to customer support, product evaluations, and secure sites.

Location*

Taiwan

Preferred Language*

Chinese

Captcha*

f68f6

refresh

Submit

By creating an account, you agree to the [Xilinx Terms of Use](#) and [Privacy Policy](#).

Vivado 安裝 (4/9)

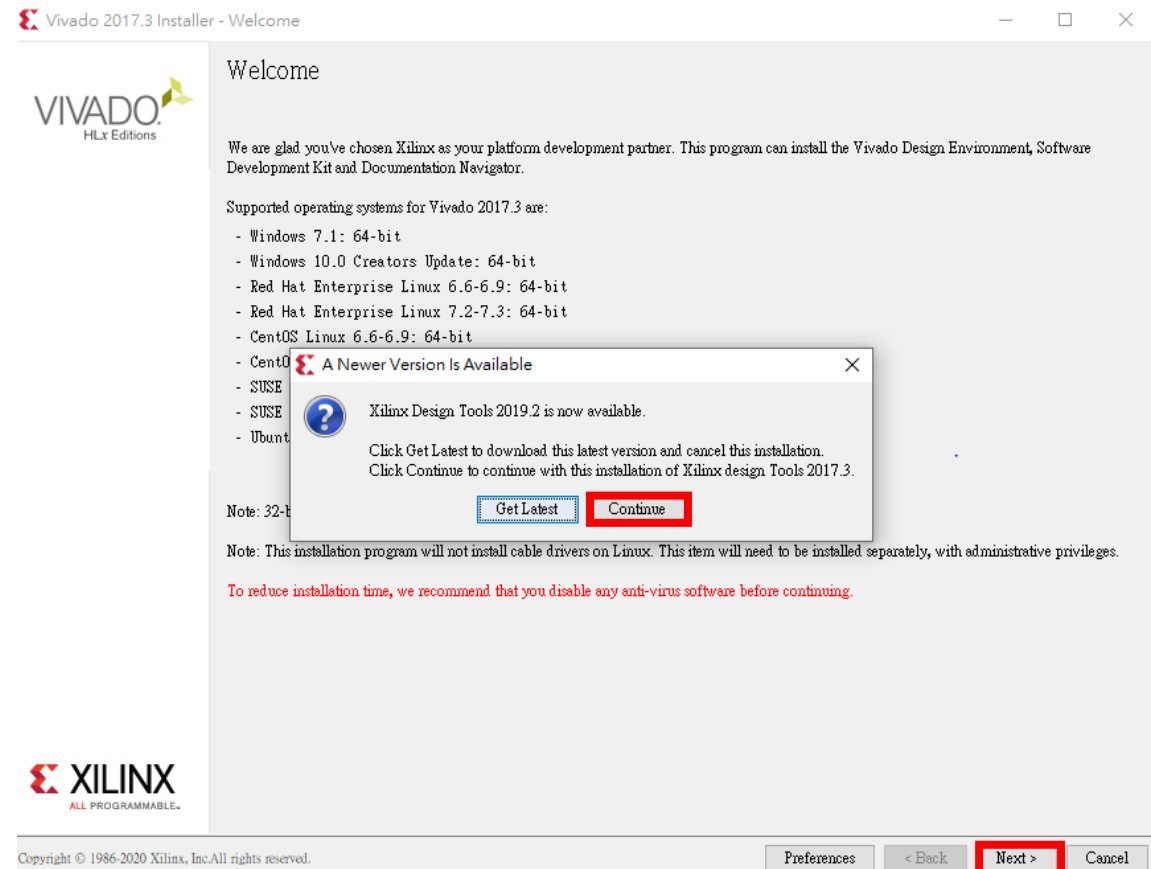
■ 登入完後填寫表單開始下載

<input type="text"/>	
First Name *	Last Name *
<input type="text"/>	<input type="text"/>
Corporate E-mail *	
<input type="text"/>	
Company Name *	
<input type="text" value="CCU University"/>	
Please enter your company's name, or "None" if not affiliated.	
Address 1 *	
<input type="text" value="Sec. 1, University Road, Minxiong Township, Chiayi County 621, Taiwan"/>	
Address 2	
<input type="text"/>	
City *	State *
<input type="text" value="Chiayi Minxiong"/>	<input type="text" value="TW"/>
	Please use 2-letter code for your US state or Canadian province .
Location *	Zip Code *
<input type="text" value="Taiwan"/>	<input type="text" value="168"/>
Phone	
<input type="text"/>	
Job Function *	
<input type="text" value="Select one"/>	
Primary Market *	
<input type="text" value="Select one"/>	
For more information about how we process your personal information, please see our privacy policy .	
<input type="button" value="Download"/>	

Vivado 安裝 (5/9)

■ 下載完後解壓縮

api-ms-win-crt-file-system-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	21 KB
api-ms-win-crt-heap-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	20 KB
api-ms-win-crt-locale-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	19 KB
api-ms-win-crt-math-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	29 KB
api-ms-win-crt-multibyte-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	27 KB
api-ms-win-crt-private-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	72 KB
api-ms-win-crt-process-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	20 KB
api-ms-win-crt-runtime-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	23 KB
api-ms-win-crt-stdio-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	25 KB
api-ms-win-crt-string-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	25 KB
api-ms-win-crt-time-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	21 KB
api-ms-win-crt-utility-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	19 KB
concr140.dll	2017/10/5 上午 10:31	應用程式擴充	240 KB
msvc140.dll	2017/10/5 上午 10:31	應用程式擴充	433 KB
ucrtbase.dll	2017/10/5 上午 10:31	應用程式擴充	880 KB
vccorlib140.dll	2017/10/5 上午 10:31	應用程式擴充	265 KB
vcruntime140.dll	2017/10/5 上午 10:31	應用程式擴充	84 KB
xsetup	2017/10/5 上午 10:31	檔案	3 KB
xsetup	2017/10/5 上午 10:01	應用程式	435 KB



Vivado安裝(6/9)

■ 按照下圖勾選

Vivado 2017.3 Installer - Accept License Agreements

Accept License Agreements

Please read the following terms and conditions and indicate that you agree by checking the I Agree checkboxes.

Xilinx Inc. End User License Agreement

By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

☒ I Agree

WebTalk Terms And Conditions

By checking "I AGREE" below, I also confirm that I have read [Section 13 of the terms and conditions](#) above concerning WebTalk and have been afforded the opportunity to read the WebTalk FAQ posted at <https://www.xilinx.com/products/design-tools/webtalk.html>. I understand that I am able to disable WebTalk later if certain criteria described in Section 13(c) apply. If they don't apply, I can disable WebTalk by uninstalling the Software or using the Software on a machine not connected to the internet. If I fail to satisfy the applicable criteria or if I fail to take the applicable steps to prevent such transmission of information, I agree to allow Xilinx to collect the information described in Section 13(a) for the purposes described in Section 13(b).

☒ I Agree

Third Party Software End User License Agreement

By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

☒ I Agree

Copyright © 1986-2020 Xilinx, Inc. All rights reserved.

< Back Next > Cancel

Vivado 2017.3 Installer - Select Edition to Install

Select Edition to Install

Select an edition to continue installation. You will be able to customize the content in the next page.

☐ Vivado HL WebPACK

Vivado HL WebPACK is the no cost, device limited version of Vivado HL Design Edition.

☒ **Vivado HL Design Edition**

Vivado HL Design Edition includes the full complement of Vivado Design Suite tools for design, including C-based design with Vivado High-Level Synthesis, implementation, verification and device programming. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add the Software Development Kit to this installation.

☐ Vivado HL System Edition

Vivado HL System Edition is a superset of Vivado HL Design Edition with the addition of System Generator for DSP. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add the Software Development Kit to this installation.

☐ Documentation Navigator (Standalone)

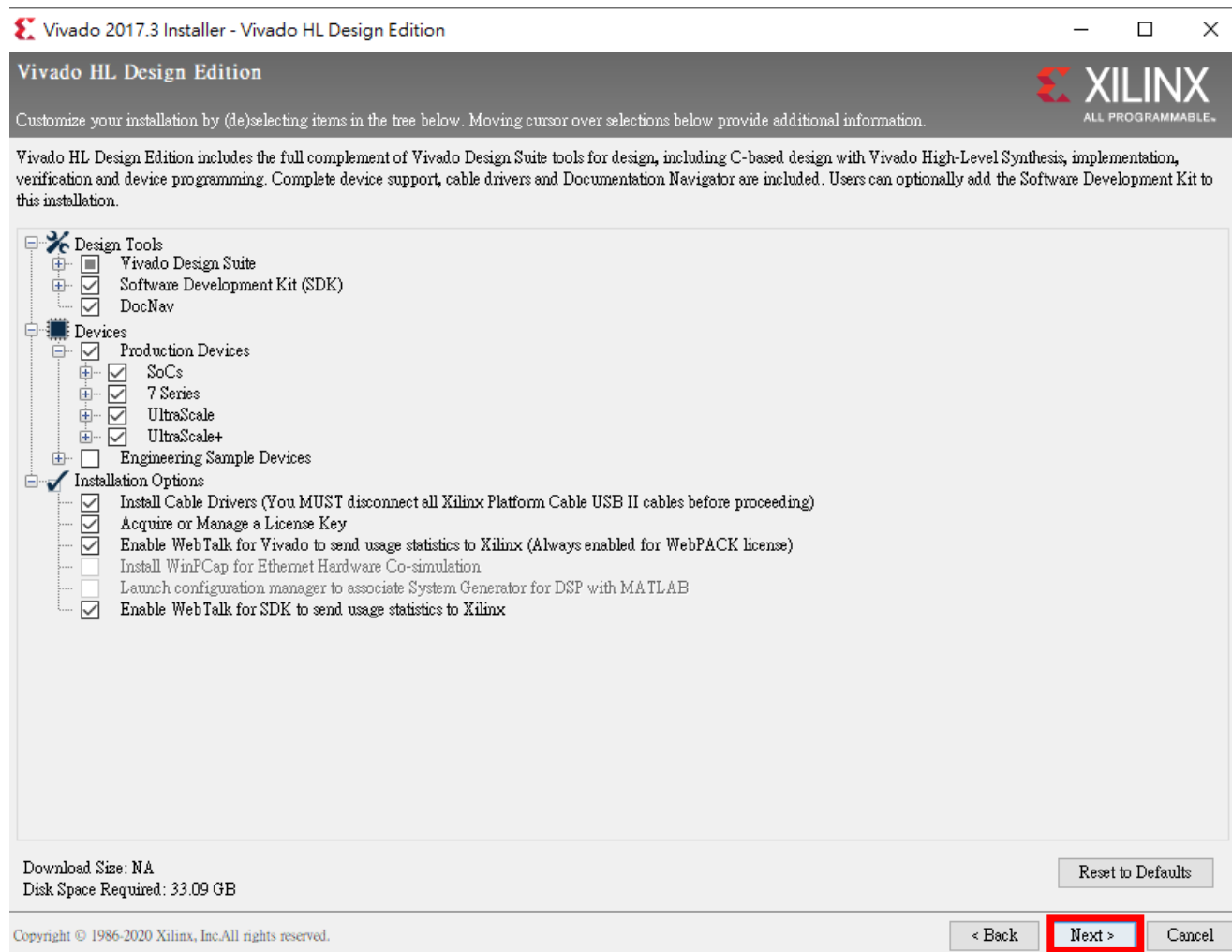
Xilinx Documentation Navigator (DocNav) provides access to Xilinx technical documentation both on the Web and on the Desktop. This is a standalone installation without Vivado Design Suite.

Copyright © 1986-2020 Xilinx, Inc. All rights reserved.

< Back Next > Cancel

Vivado安裝(7/9)

■ 按照下圖勾選



Vivado 安裝 (8/9)

■ 等待安裝



Vivado安裝(9/9)

- 雲端下載License
- 啟動Vivado > Help > Manage License
- Load License > Copy License > 選擇剛剛下載的License

