Clock generator & Reset fanout

File: clock_gen.kicad_sch

PCIe switch

File: pcie_switch.kicad_sch

RC 4-lanes PCIe

File: RC_4-lanes-PCIe.kicad_sch

4 x 1-lanes PCIe

File: 4_1-lanes_PCIe.kicad_sch

Direct PCIe

File: direct_PCIe.kicad_sch

H1 H2 H3 H4 H5 H6

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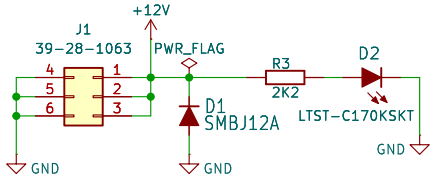
Sheet: /

File: openpci2-backplane.kicad_sch

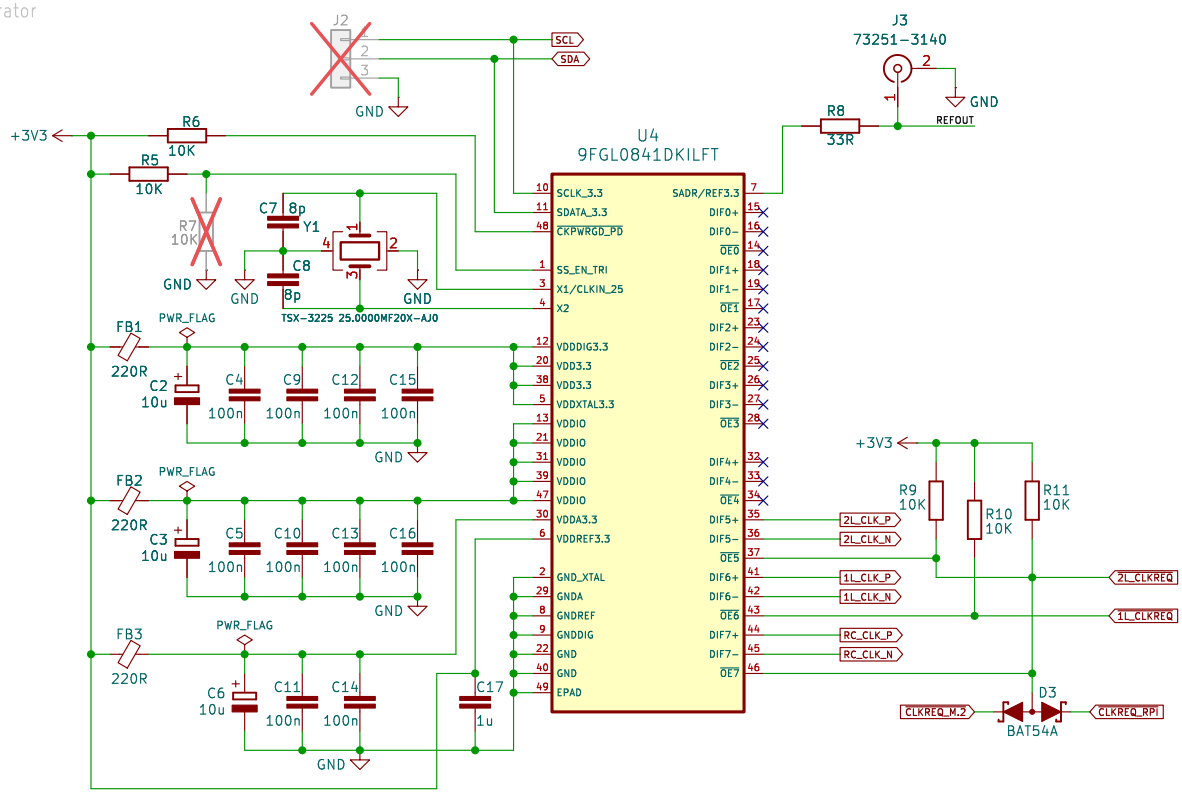
Title:

Size: A4	Date: 2025-07-01	Rev: r1B1
KiCad E.D.A. 9.0.2		Id: 1/6

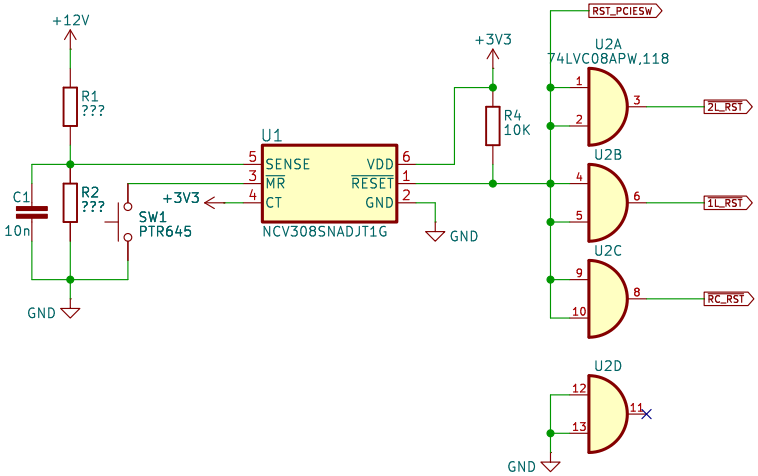
+12V Power input

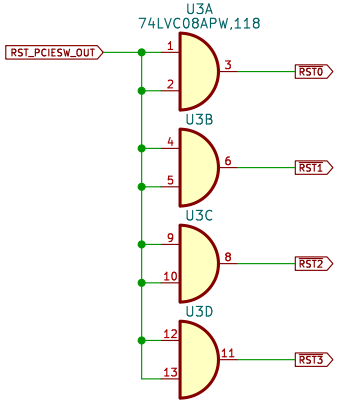


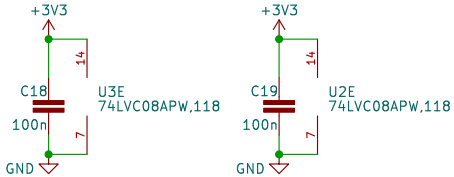
Clock generator



Voltage Supervisor, Manual Reset and Reset fanout







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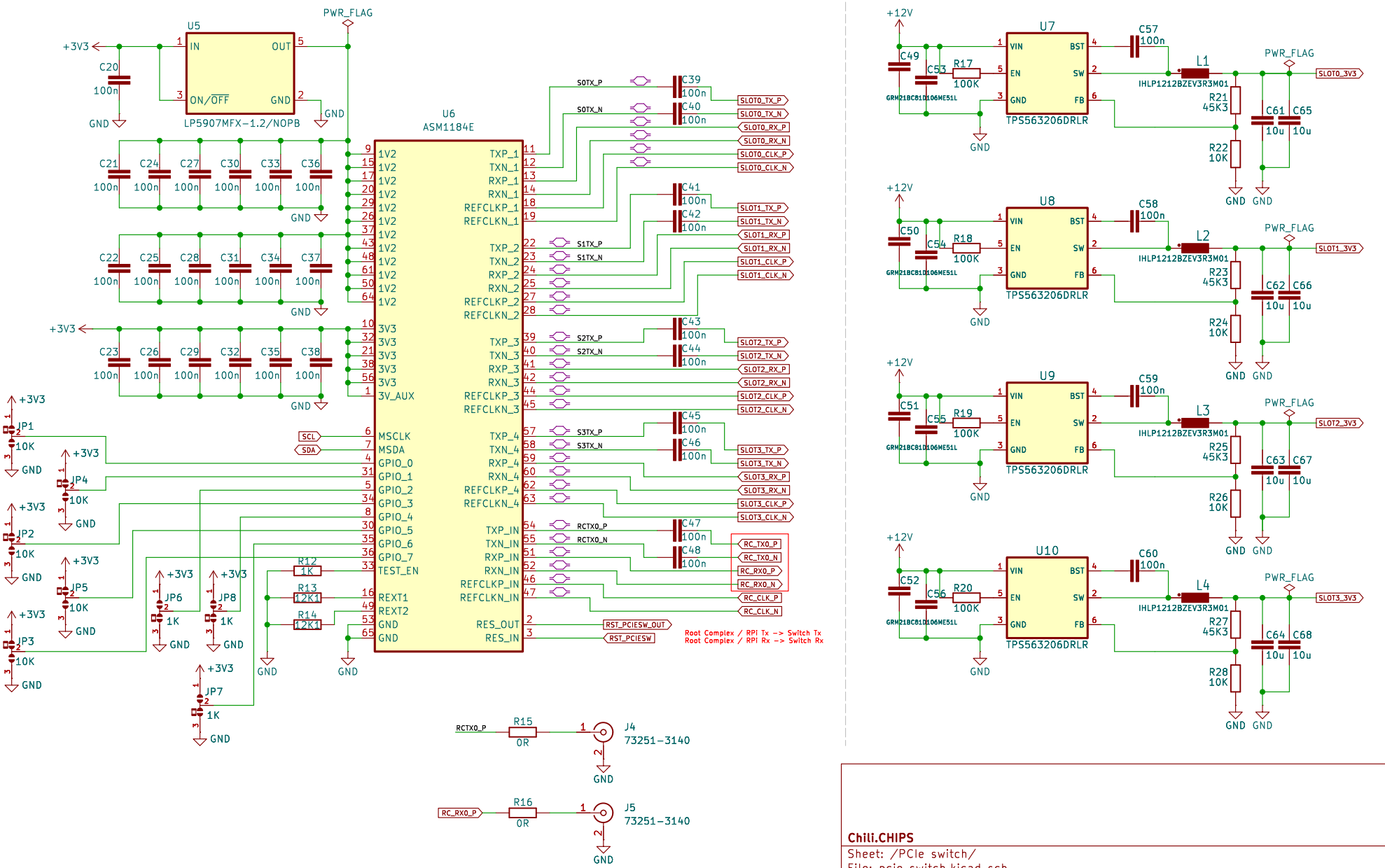
Sheet: /Clock generator & Reset fanout/
File: clock_gen.kicad_sch

Title:

Size: A4	Date: 2025-07-01	**Rev: r1B1**
KiCad E.D.A. 9.0.2		Id: 2/6

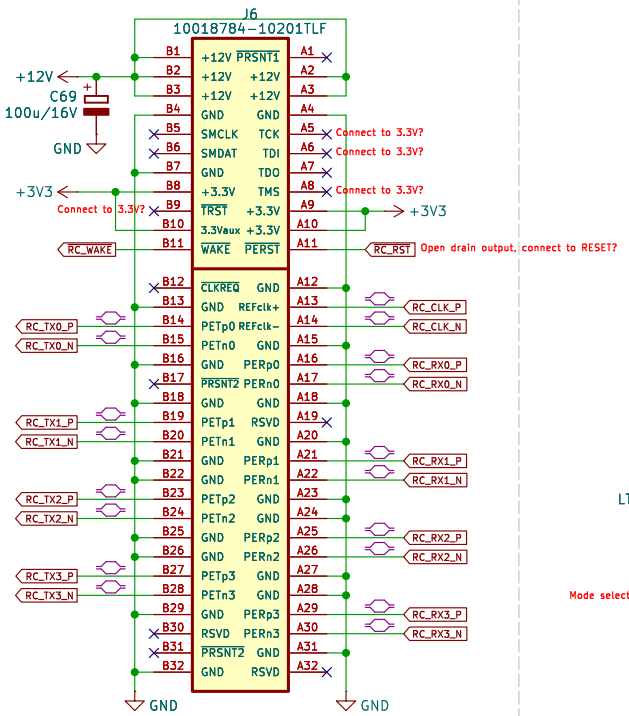
PCIe 4-slot switch

Point-of-load stepdown converters for 1-lanes PCIe



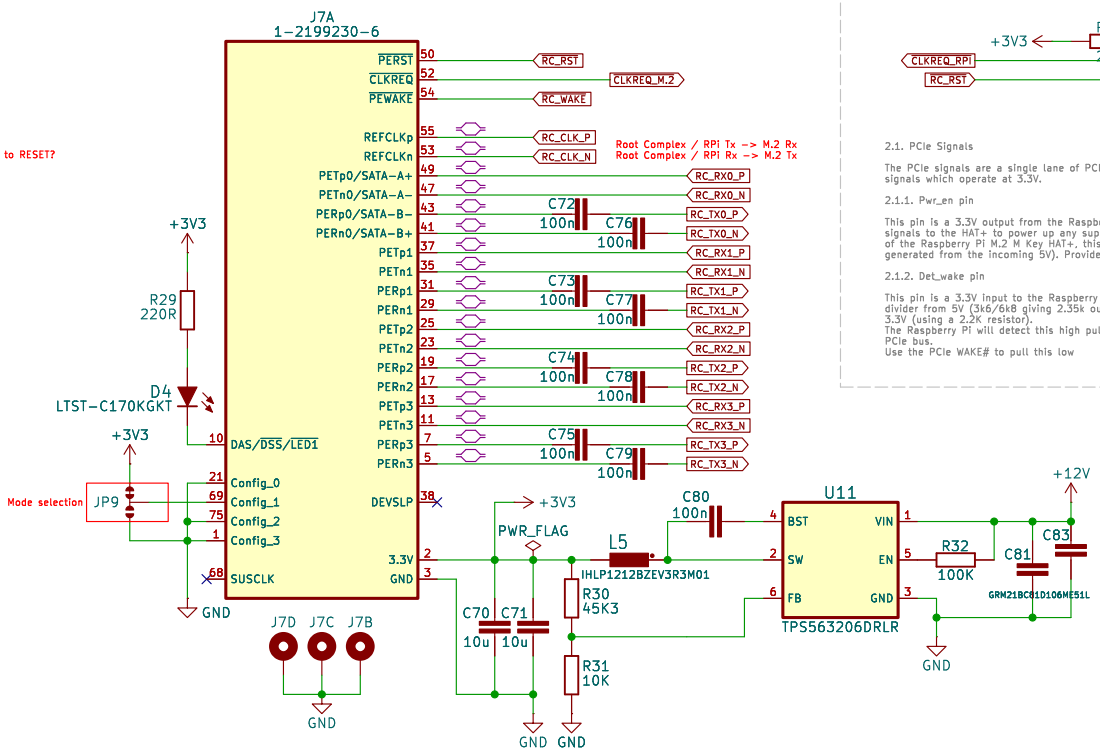
Chili.CHIPS		
Sheet: /PCIe switch/		
File: pcie_switch.kicad_sch		
Title:		
Size: A4	Date: 2025-07-01	**Rev: r1B1**
KiCad E.D.A. 9.0.2		Id: 3/6

4-lane PCIe for Root Complex

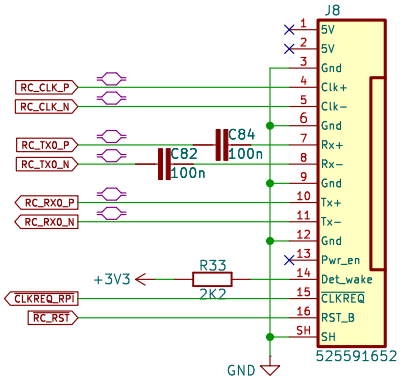


Lanes #	Device
0	PCIe switch for 4 x 1-lanes + 4 x M.2
1	1-lanes slot + M.2
2	2-lanes slot + M.2 (First)
3	2-lanes slot + M.2 (Second)

4-lane M.2 (Type M) for Root Complex



Raspberry Pi FPC 16-pin connector



2.1. PCIe Signals

The PCIe signals are a single lane of PCIe Gen 2, including CLKREQ and RST_B sideband signals which operate at 3.3V.

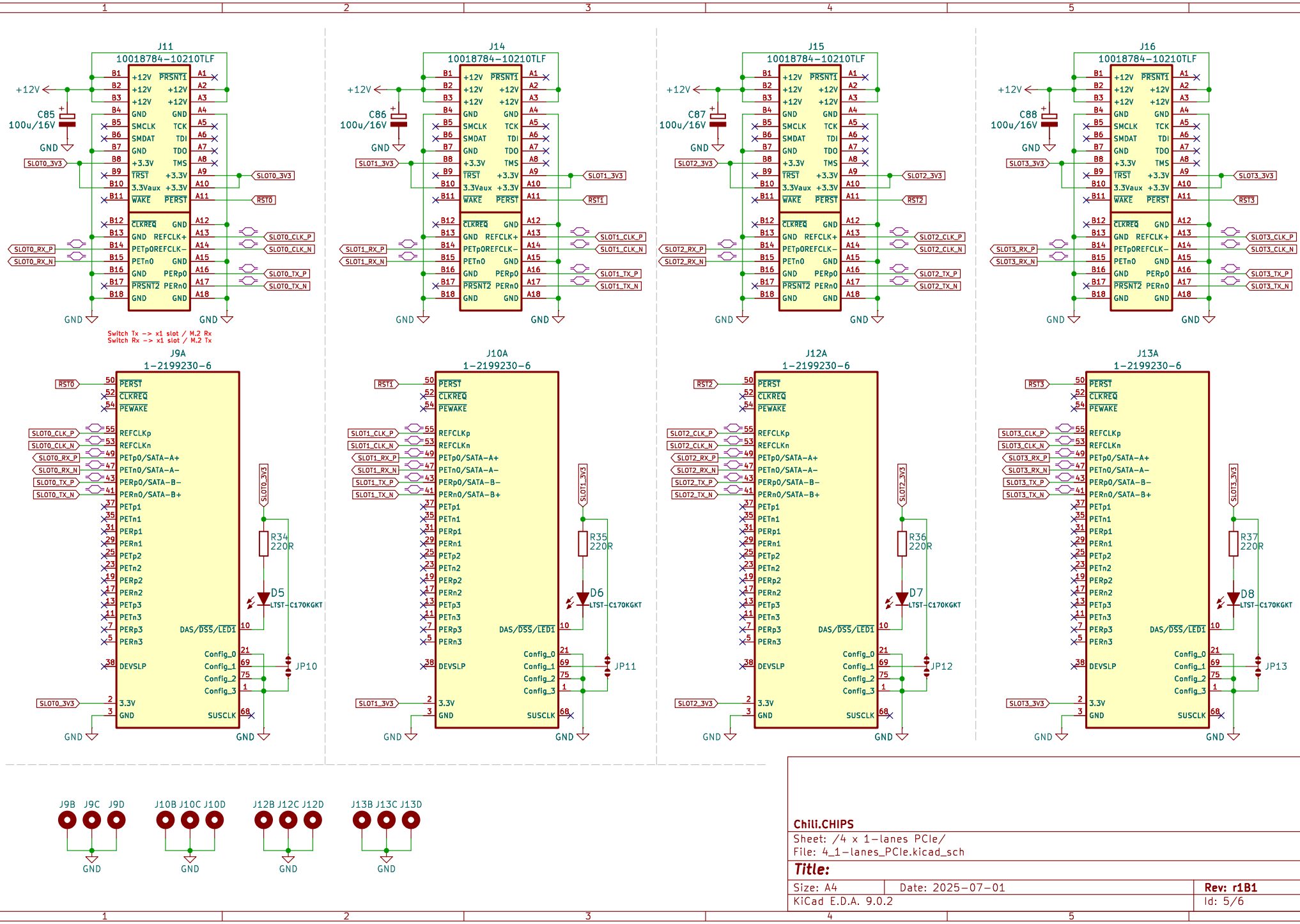
2.1.1. Pwr_en pin

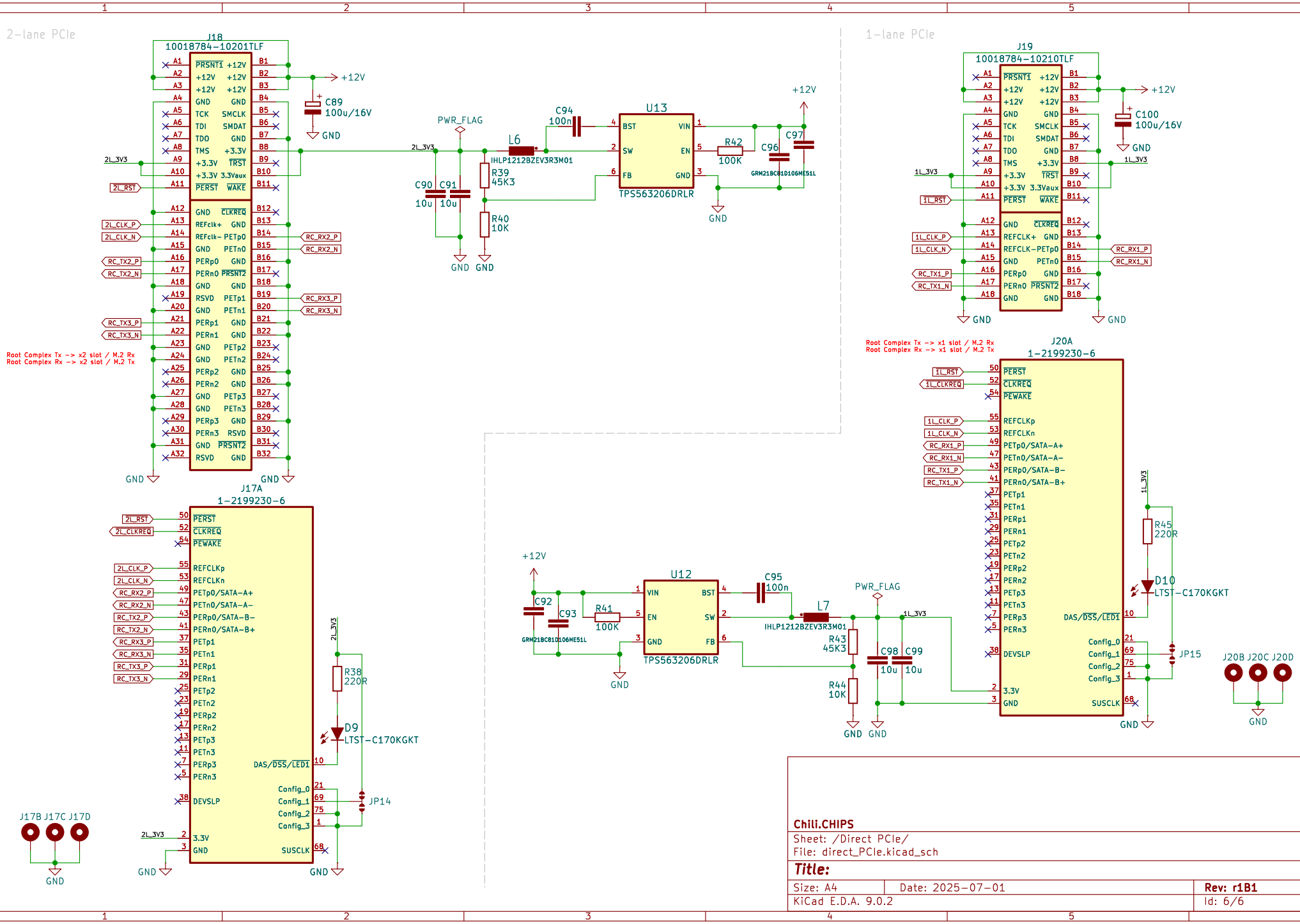
This pin is a 3.3V output from the Raspberry PI to a HAT+ or other add-on board, and signals to the HAT+ to power up any supplies. For example, in the instance of the Raspberry PI M.2 M Key HAT+, this enables the M.2 3.3V power (which is generated from the incoming 5V). Provide a 100K low pull on this pin on any HAT+.

2.1.2. Det_wake pin

This pin is a 3.3V input to the Raspberry PI. Pull high to 3.3V either from a resistive divider from 5V (3k6/6k8 giving 2.35k output impedance), or from permanently enabled 3.3V (using a 2.2K resistor).
The Raspberry PI will detect this high pull at boot time, and will automatically probe the PCIe bus.
Use the PCIe WAKE# to pull this low

Chili.CHIPS		
Sheet: /RC 4-lanes PCIe/		
File: RC_4-lanes-PCIe.kicad_sch		
Title:		
Size: A4	Date: 2025-07-01	**Rev: r1B1**
KiCad E.D.A. 9.0.2		Id: 4/6


J11
10018784-10210TLF
C85
100u/16V
+12V
GND
SLOT0_3V3
SLOT0_CLK_P
SLOT0_CLK_N
SLOT0_RX_P
SLOT0_RX_N
SLOT0_TX_P
SLOT0_TX_N
RST0
J14
10018784-10210TLF
C86
100u/16V
SLOT1_3V3
SLOT1_CLK_P
SLOT1_CLK_N
SLOT1_RX_P
SLOT1_RX_N
SLOT1_TX_P
SLOT1_TX_N
RST1
J15
10018784-10210TLF
C87
100u/16V
SLOT2_3V3
SLOT2_CLK_P
SLOT2_CLK_N
SLOT2_RX_P
SLOT2_RX_N
SLOT2_TX_P
SLOT2_TX_N
RST2
J16
10018784-10210TLF
C88
100u/16V
SLOT3_3V3
SLOT3_CLK_P
SLOT3_CLK_N
SLOT3_RX_P
SLOT3_RX_N
SLOT3_TX_P
SLOT3_TX_N
RST3
Switch Tx -> x1 slot / M.2 Rx
Switch Rx -> x1 slot / M.2 Tx
J9A
1-2199230-6
J10A
1-2199230-6
J12A
1-2199230-6
J13A
1-2199230-6
PERST
CLKREQ
PEWAKE
REFCLKp
REFCLKn
PETp0/SATA-A+
PETn0/SATA-A-
PERp0/SATA-B-
PERn0/SATA-B+
PETp1
PETn1
PERp1
PERn1
PETp2
PETn2
PERp2
PERn2
PETp3
PETn3
PERp3
PERn3
DEVSLP
DAS/DSS/LED1
Config_0
Config_1
Config_2
Config_3
3.3V
GND
SUSCLK
R34
220R
R35
220R
R36
220R
R37
220R
D5
LTST-C170KGKT
D6
LTST-C170KGKT
D7
LTST-C170KGKT
D8
LTST-C170KGKT
JP10
JP11
JP12
JP13
J9B J9C J9D
J10B J10C J10D
J12B J12C J12D
J13B J13C J13D
Chili.CHIPS
Sheet: /4 x 1-lanes PCIe/
File: 4_1-lanes_PCIe.kicad_sch
Title:
Size: A4
Date: 2025-07-01
Rev: r1B1
KiCad E.D.A. 9.0.2
Id: 5/6


2-lane PCIe
J18
10018784-10201TLF
PRSNT1 +12V
+12V +12V
+12V +12V
GND GND
TCK SMCLK
TDI SMDAT
TDO GND
TMS +3.3V
+3.3V TRST
+3.3V 3.3Vaux
PERST WAKE
GND CLKREQ
REFclk+ GND
REFclk- PETp0
GND PETn0
PERp0 GND
PERn0 PRSNT2
GND GND
RSVD PETp1
GND PETn1
PERp1 GND
PERn1 GND
GND PETp2
GND PETn2
PERp2 GND
PERn2 GND
GND PETp3
GND PETn3
PERp3 GND
PERn3 RSVD
GND PRSNT2
RSVD GND
+12V
C89
100u/16V
GND
2L_3V3
2L_RST
2L_CLK_P
2L_CLK_N
RC_TX2_P
RC_TX2_N
RC_TX3_P
RC_TX3_N
RC_RX2_P
RC_RX2_N
RC_RX3_P
RC_RX3_N
Root Complex Tx -> x2 slot / M.2 Rx
Root Complex Rx -> x2 slot / M.2 Tx
PWR_FLAG
L6
IHLP1212BZEV3R3M01
C94
100n
U13
BST VIN
SW EN
FB GND
TPS563206DRLR
R42
100K
C97
C96
GRM21BC81D106ME51L
R39
45K3
R40
10K
C90
10u
C91
10u
J17A
1-2199230-6
PERST
CLKREQ
PEWAKE
REFCLKp
REFCLKn
PETp0/SATA-A+
PETn0/SATA-A-
PERp0/SATA-B-
PERn0/SATA-B+
PETp1
PETn1
PERp1
PERn1
PETp2
PETn2
PERp2
PERn2
PETp3
PETn3
PERp3
PERn3
DEVSLP
3.3V
GND
DAS/DSS/LED1
Config_0
Config_1
Config_2
Config_3
SUSCLK
R38
220R
D9
LTST-C170KGKT
JP14
J17B J17C J17D
1-lane PCIe
J19
10018784-10210TLF
C100
100u/16V
1L_3V3
1L_RST
1L_CLK_P
1L_CLK_N
RC_TX1_P
RC_TX1_N
RC_RX1_P
RC_RX1_N
Root Complex Tx -> x1 slot / M.2 Rx
Root Complex Rx -> x1 slot / M.2 Tx
J20A
1-2199230-6
1L_CLKREQ
R45
220R
D10
LTST-C170KGKT
JP15
J20B J20C J20D
U12
VIN BST
EN SW
GND FB
TPS563206DRLR
C92
C93
GRM21BC81D106ME51L
R41
100K
C95
100n
L7
IHLP1212BZEV3R3M01
R43
45K3
R44
10K
C98
10u
C99
10u
Chili.CHIPS
Sheet: /Direct PCIe/
File: direct_PCIe.kicad_sch
Title:
Size: A4
Date: 2025-07-01
Rev: r1B1
KiCad E.D.A. 9.0.2
Id: 6/6