Clock generator & Reset fanout

File: clock_gen.kicad_sch

Direct 4-lane PCIe

File: direct_PCIe.kicad_sch

RC 1-lane and 2-lane PCIE

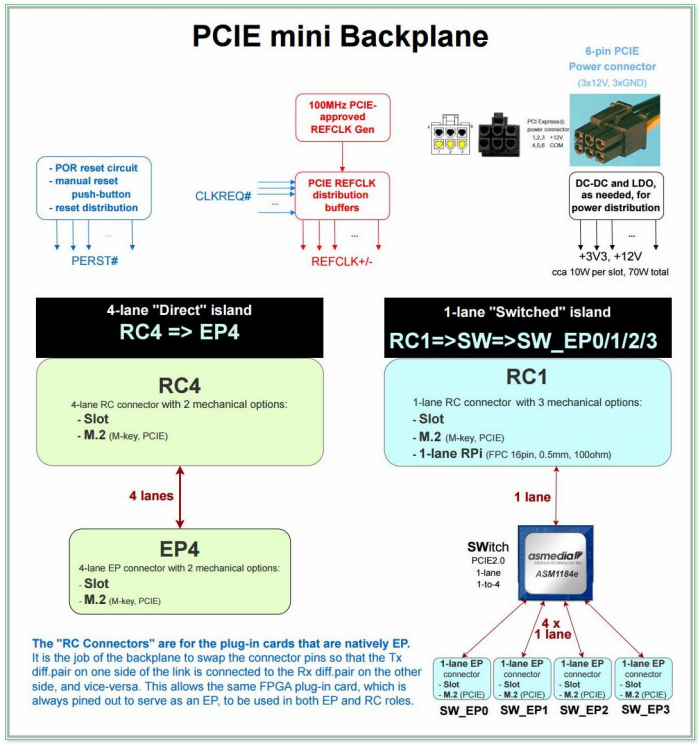
File: RC_4-lanes-PCIe.kicad_sch

PCIe switch

File: pcie_switch.kicad_sch

Switched 4 x 1-lanes PCIe

File: 4_1-lanes_PCIe.kicad_sch




H1 H2 H3 H4 H5 H6

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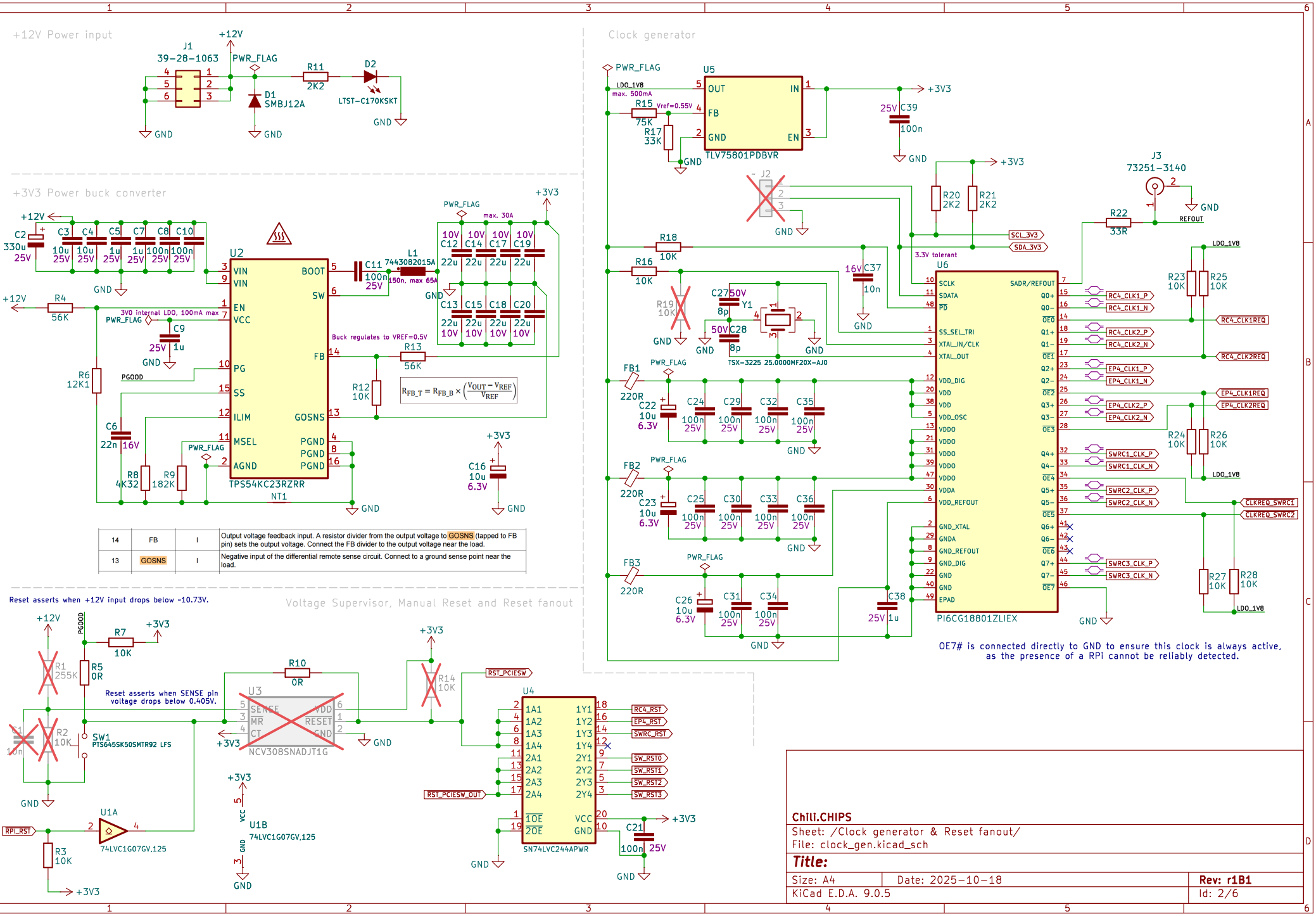
Sheet: /

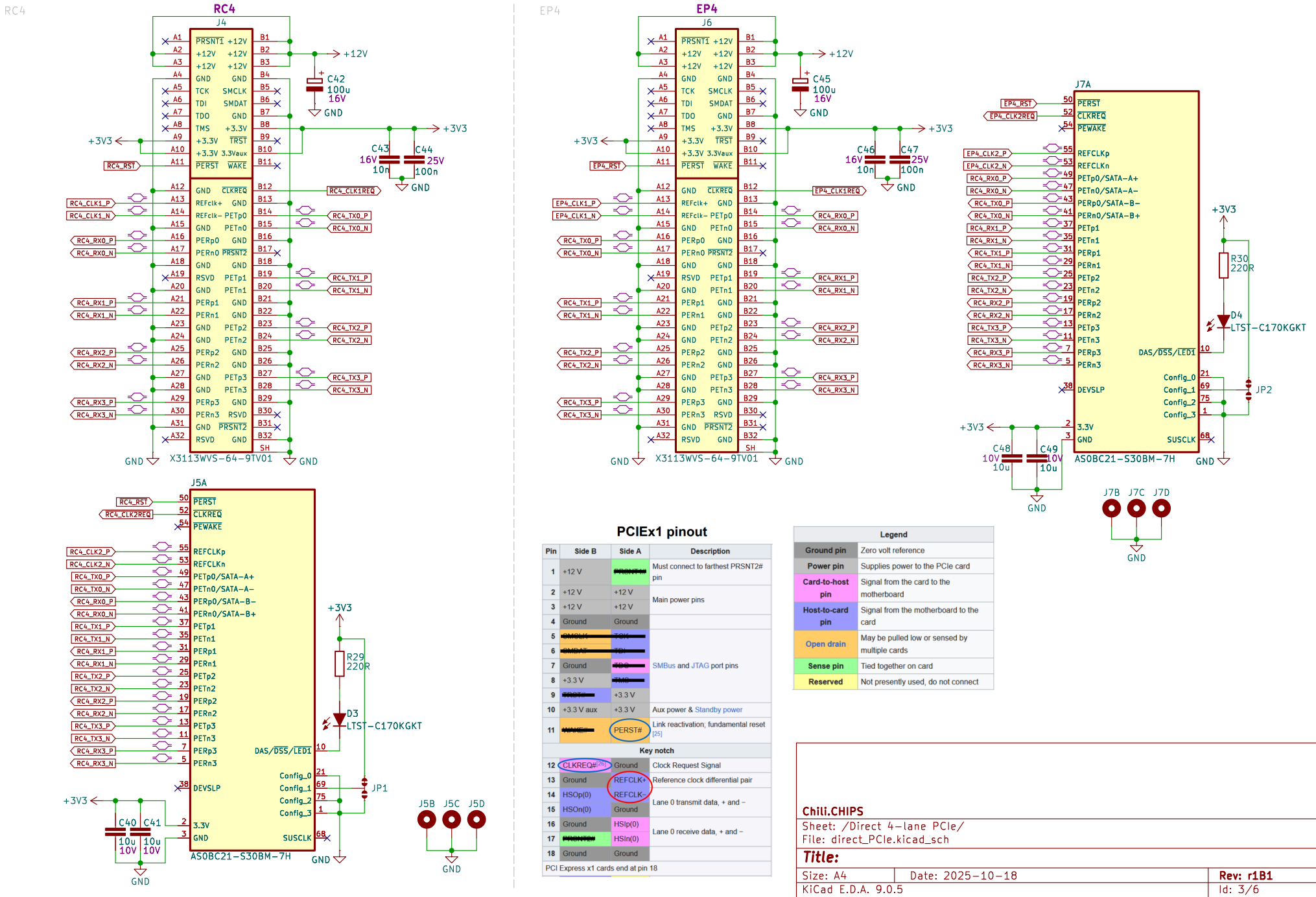
File: openpci2-backplane.kicad_sch

Title:

| Size: A4 | Date: 2025-10-18 | Rev: r1B1 |
|---|---|---|
| KiCad E.D.A. 9.0.5 | | Id: 1/6 |




| | | | |
|---|---|---|---|
| 14 | FB | I | Output voltage feedback input. A resistor divider from the output voltage to GOSNS (tapped to FB pin) sets the output voltage. Connect the FB divider to the output voltage near the load. |
| 13 | GOSNS | I | Negative input of the differential remote sense circuit. Connect to a ground sense point near the load. |




## PCIEx1 pinout

| Pin | Side B | Side A | Description |
|---|---|---|---|
| 1 | +12 V | ~~PRSNT1#~~ | Must connect to farthest PRSNT2# pin |
| 2 | +12 V | +12 V | Main power pins |
| 3 | +12 V | +12 V | |
| 4 | Ground | Ground | |
| 5 | ~~SMCLK~~ | TCK | SMBus and JTAG port pins |
| 6 | ~~SMDAT~~ | TDI | |
| 7 | Ground | ~~TDO~~ | |
| 8 | +3.3 V | ~~3.3Vaux~~ | |
| 9 | ~~PERST#~~ | +3.3 V | |
| 10 | +3.3 V aux | +3.3 V | Aux power & Standby power |
| 11 | ~~WAKE#~~ | PERST# | Link reactivation; fundamental reset [25] |
| **Key notch** | | | |
| 12 | CLKREQ# [26] | Ground | Clock Request Signal |
| 13 | Ground | REFCLK+ | Reference clock differential pair |
| 14 | HSOp(0) | REFCLK− | Lane 0 transmit data, + and − |
| 15 | HSOn(0) | Ground | |
| 16 | Ground | HSIp(0) | Lane 0 receive data, + and − |
| 17 | ~~PRSNT2#~~ | HSIn(0) | |
| 18 | Ground | Ground | |

PCI Express x1 cards end at pin 18

| Legend | |
|---|---|
| Ground pin | Zero volt reference |
| Power pin | Supplies power to the PCIe card |
| Card-to-host pin | Signal from the card to the motherboard |
| Host-to-card pin | Signal from the motherboard to the card |
| Open drain | May be pulled low or sensed by multiple cards |
| Sense pin | Tied together on card |
| Reserved | Not presently used, do not connect |

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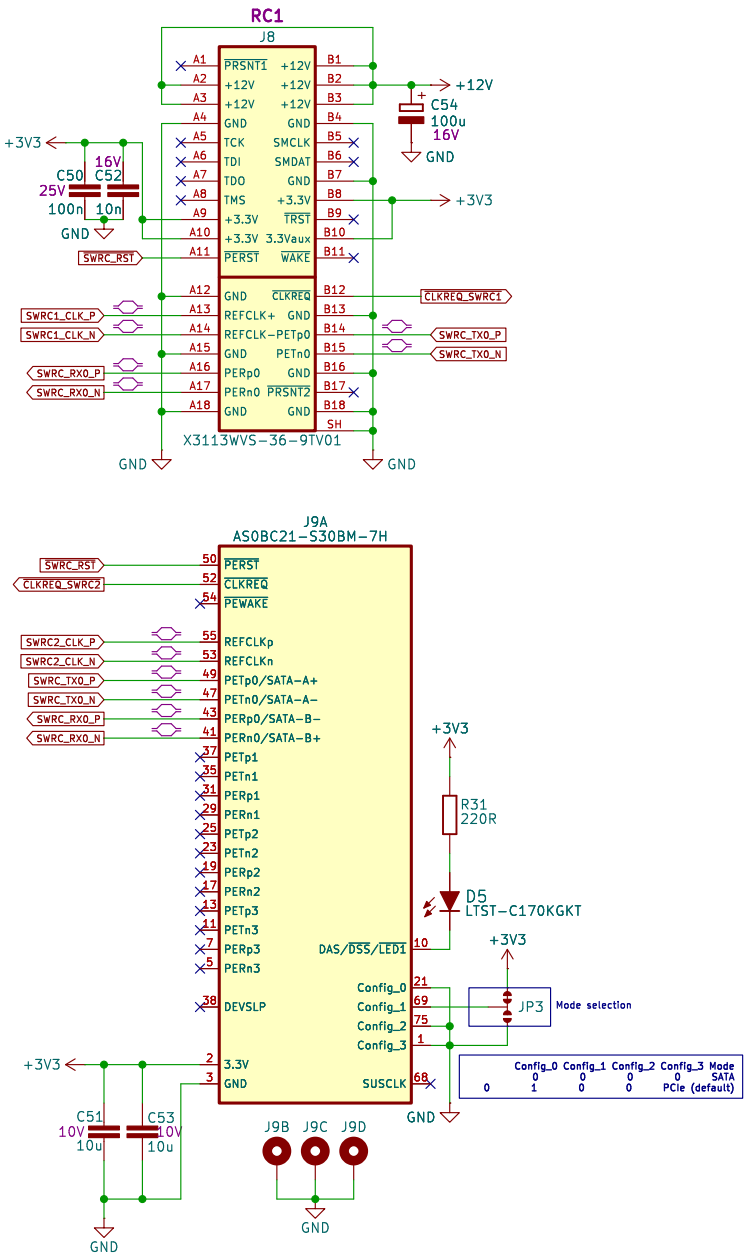
Sheet: /Direct 4−lane PCIe/
File: direct_PCIe.kicad_sch

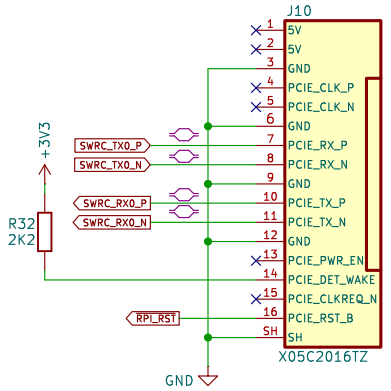
**Title:**

| | | |
|---|---|---|
| Size: A4 | Date: 2025−10−18 | **Rev: r1B1** |
| KiCad E.D.A. 9.0.5 | | Id: 3/6 |

1-lane PCIe for Root Complex




Raspberry Pi FPC 16-pin connector




As the Root Complex, the Raspberry Pi provides its own reference clock. The rest of the backplane does not need this clock, as all downstream PCIe devices receive their reference clock from the onboard generator (U5).

PCIE_RST_B (pin 16) is an active-low output from the Raspberry Pi, serving as the master reset for the downstream PCIe fabric.
This PCIE_RST_B signal is intended to be combined with the board's own reset sources through external logic to generate the final system reset.

2.1. PCIe Signals

The PCIe signals are a single lane of PCIe Gen 2, including CLKREQ and RST_B sideband signals which operate at 3.3V.

2.1.1. Pwr_en pin

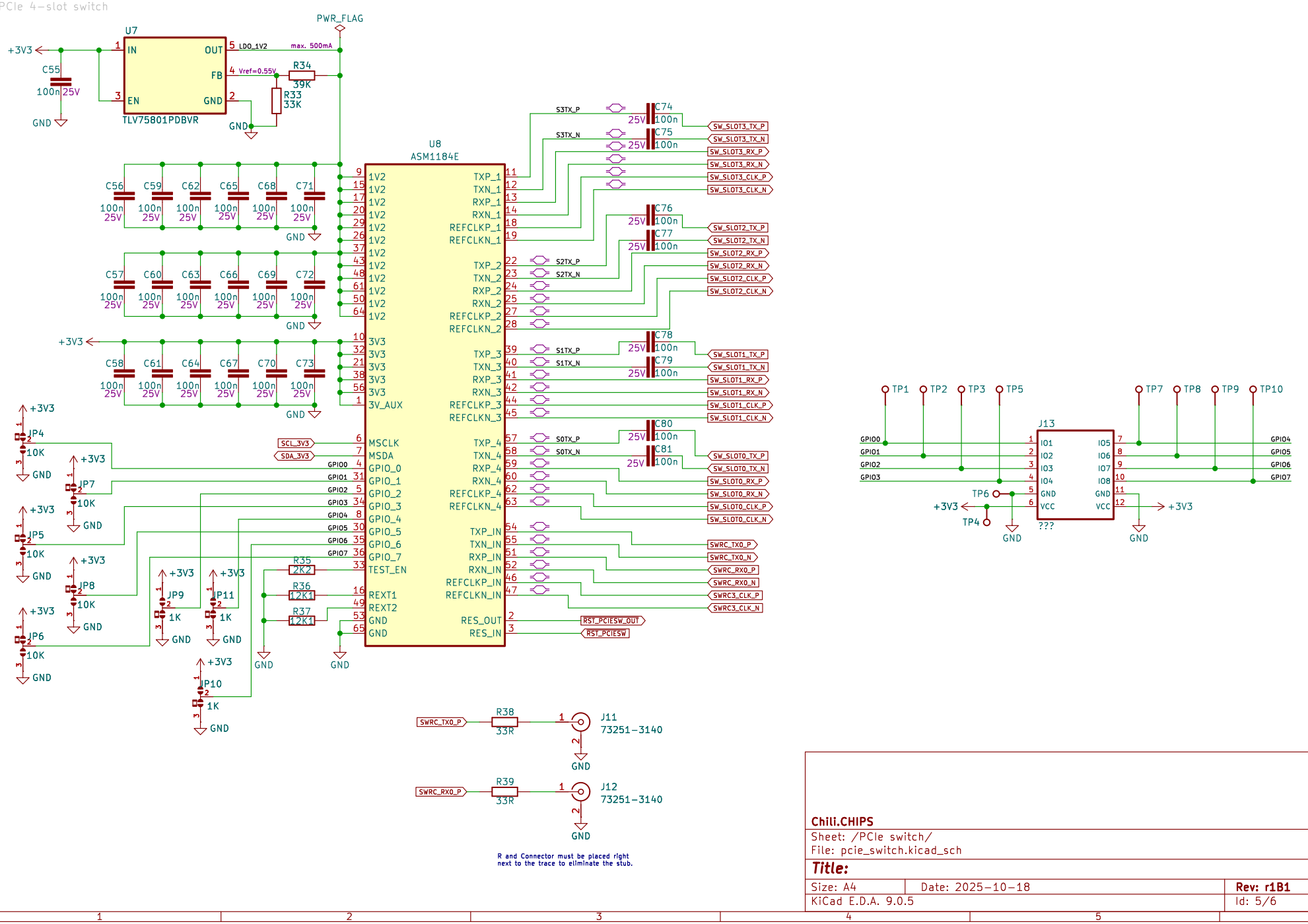
This pin is a 3.3V output from the Raspberry Pi to a HAT+ or other add-on board, and signals to the HAT+ to power up any supplies. For example, in the instance of the Raspberry Pi M.2 M Key HAT+, this enables the M.2 3.3V power (which is generated from the incoming 5V). Provide a 100K low pull on this pin on any HAT+.

2.1.2. Det_wake pin

This pin is a 3.3V input to the Raspberry Pi. Pull high to 3.3V either from a resistive divider from 5V (3k6/6k8 giving 2.35k output impedance), or from permanently enabled 3.3V (using a 2.2K resistor).
The Raspberry Pi will detect this high pull at boot time, and will automatically probe the PCIe bus.
Use the PCIe WAKE# to pull this low

| | | |
|---|---|---|
| Chili.CHIPS | | |
| Sheet: /RC 1-lane and 2-lane PCIE/ | | |
| File: RC_4-lanes-PCIe.kicad_sch | | |
| Title: | | |
| Size: A4 | Date: 2025-10-18 | Rev: r1B1 |
| KiCad E.D.A. 9.0.5 | | Id: 4/6 |

PCIe 4-slot switch

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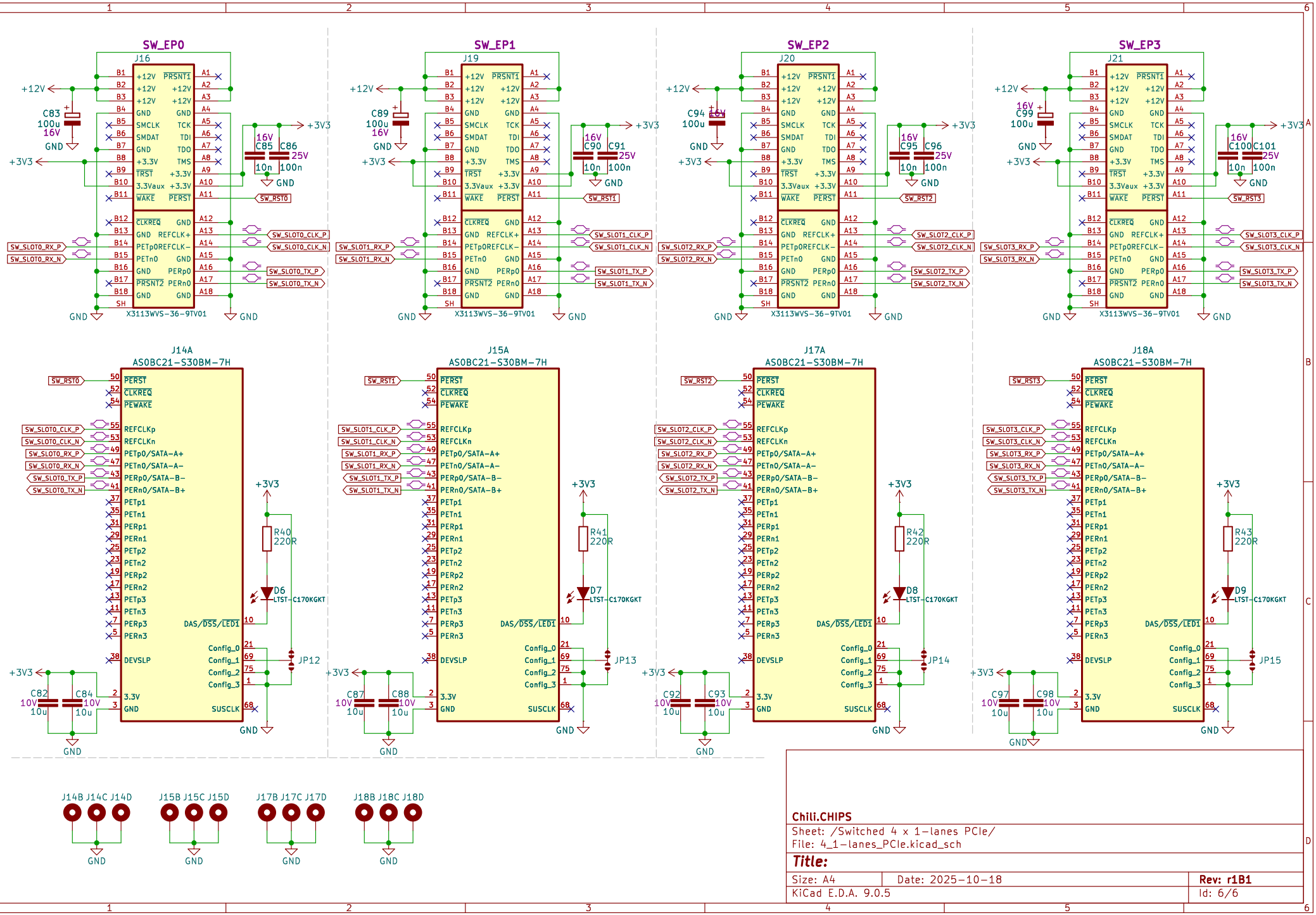
Sheet: /PCIe switch/

File: pcie_switch.kicad_sch

**Title:**

| Size: A4 | Date: 2025-10-18 | **Rev: r1B1** |
|---|---|---|
| KiCad E.D.A. 9.0.5 | | Id: 5/6 |

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Sheet: /Switched 4 x 1-lanes PCIe/

File: 4_1-lanes_PCIe.kicad_sch

**Title:**

| Size: A4 | Date: 2025-10-18 | **Rev: r1B1** |
|---|---|---|
| KiCad E.D.A. 9.0.5 | | Id: 6/6 |