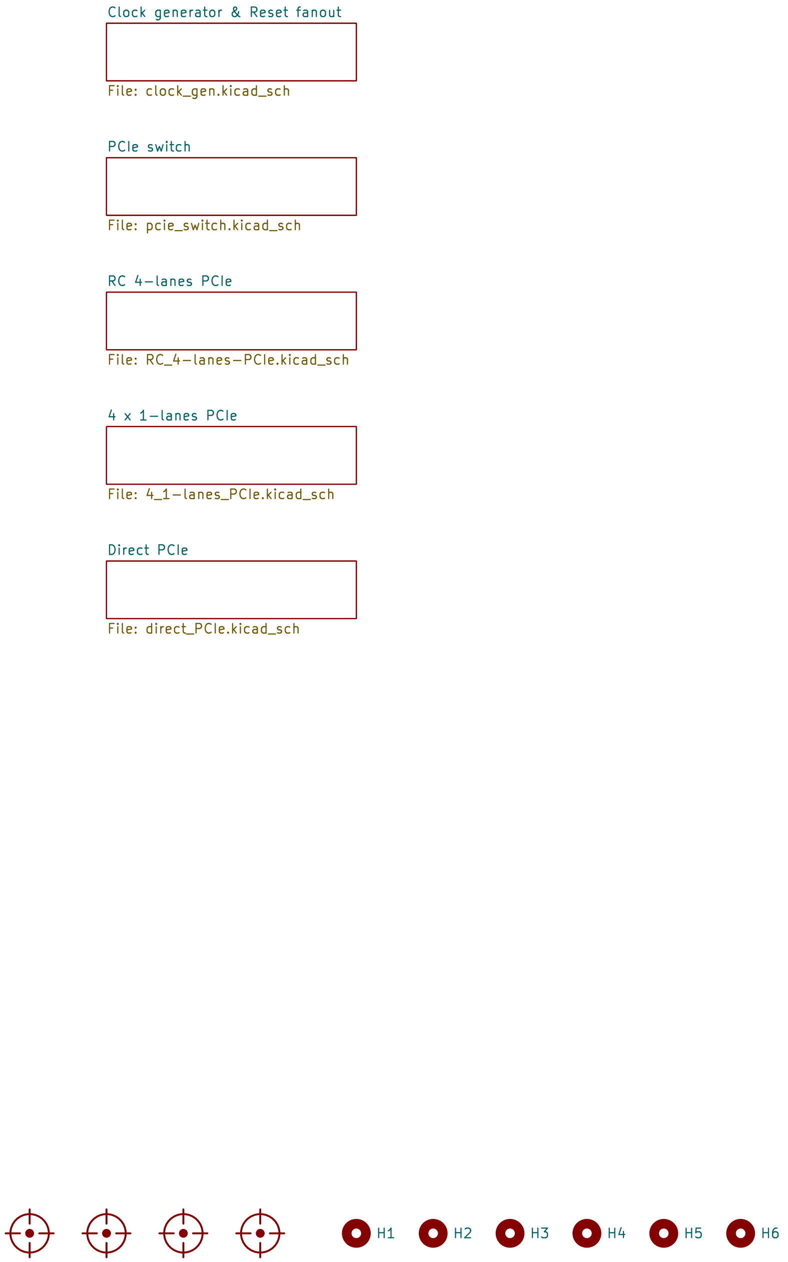
Clock generator & Reset fanout
File: clock_gen.kicad_sch
PCIe switch
File: pcie_switch.kicad_sch
RC 4–lanes PCIe
File: RC_4–lanes–PCIe.kicad_sch
4 x 1–lanes PCIe
File: 4_1–lanes_PCIe.kicad_sch
Direct PCIe
File: direct_PCIe.kicad_sch
H1
H2
H3
H4
H5
H6

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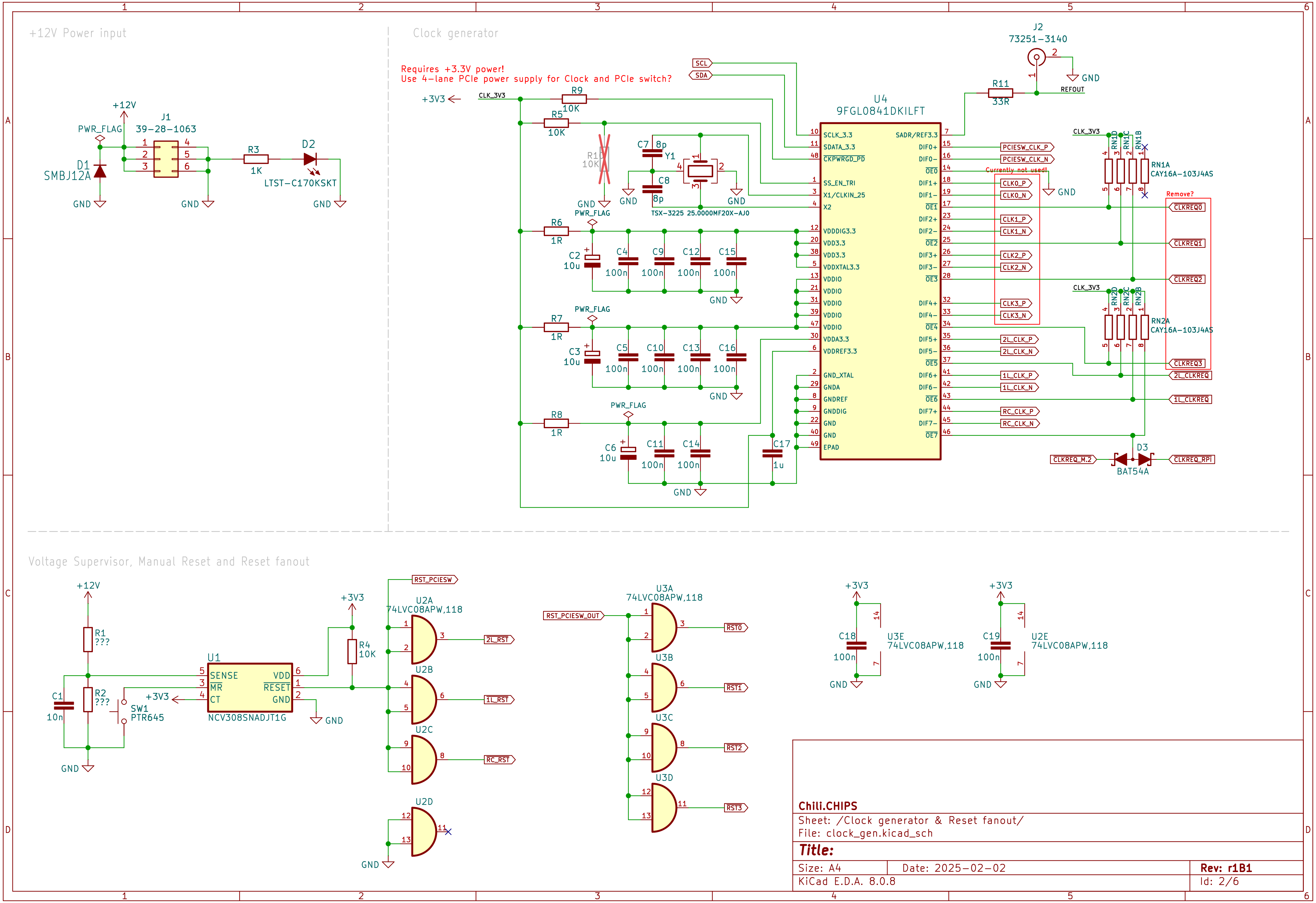
Sheet: /

File: openpci2–backplane.kicad_sch

Title:

Size: A4	Date: 2025–02–02	**Rev: r1B1**
KiCad E.D.A. 8.0.8		Id: 1/6



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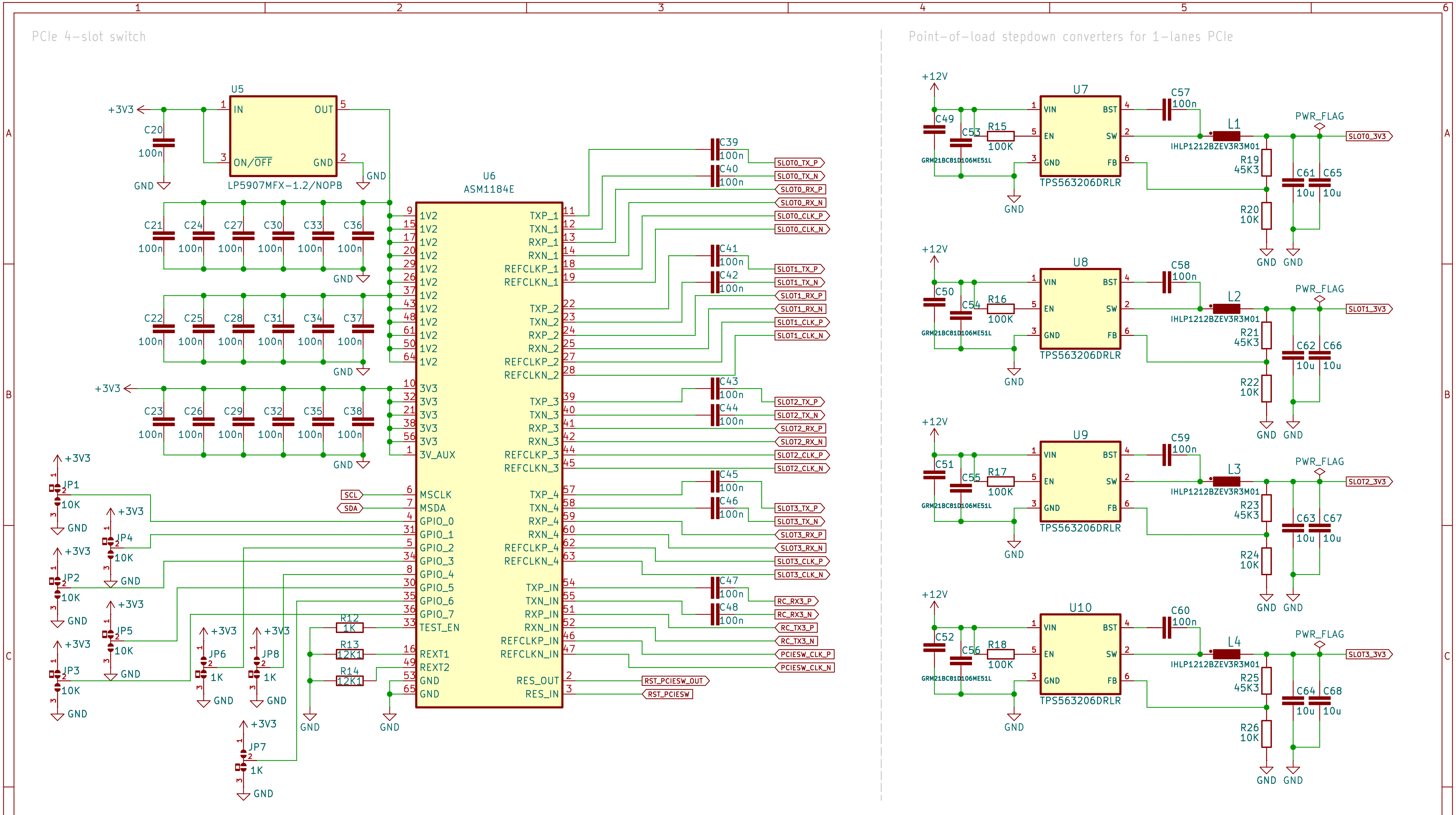
Sheet: /Clock generator & Reset fanout/
File: clock_gen.kicad_sch

Title:

Size: A4 Date: 2025-02-02 Rev: r1B1
KiCad E.D.A. 8.0.8 Id: 2/6



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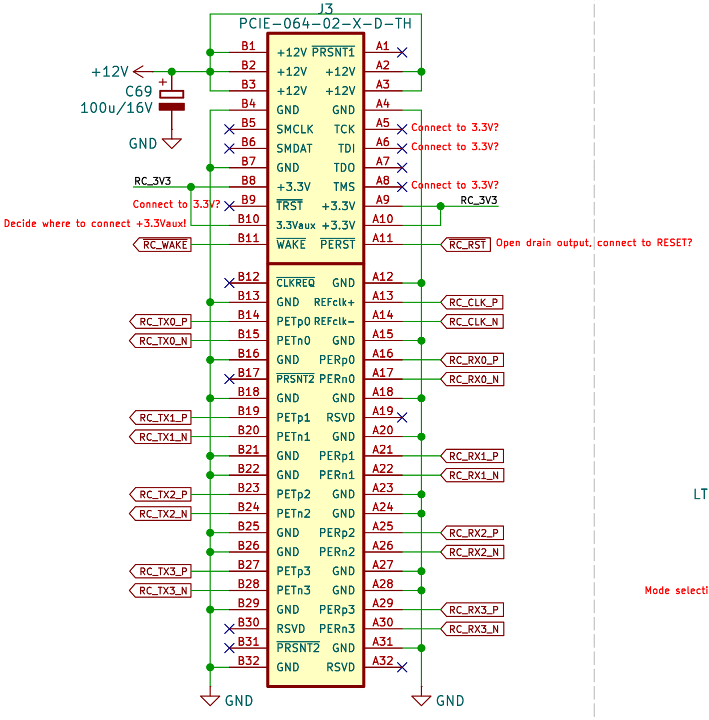
Sheet: /PCIe switch/

File: pcie_switch.kicad_sch

Title:

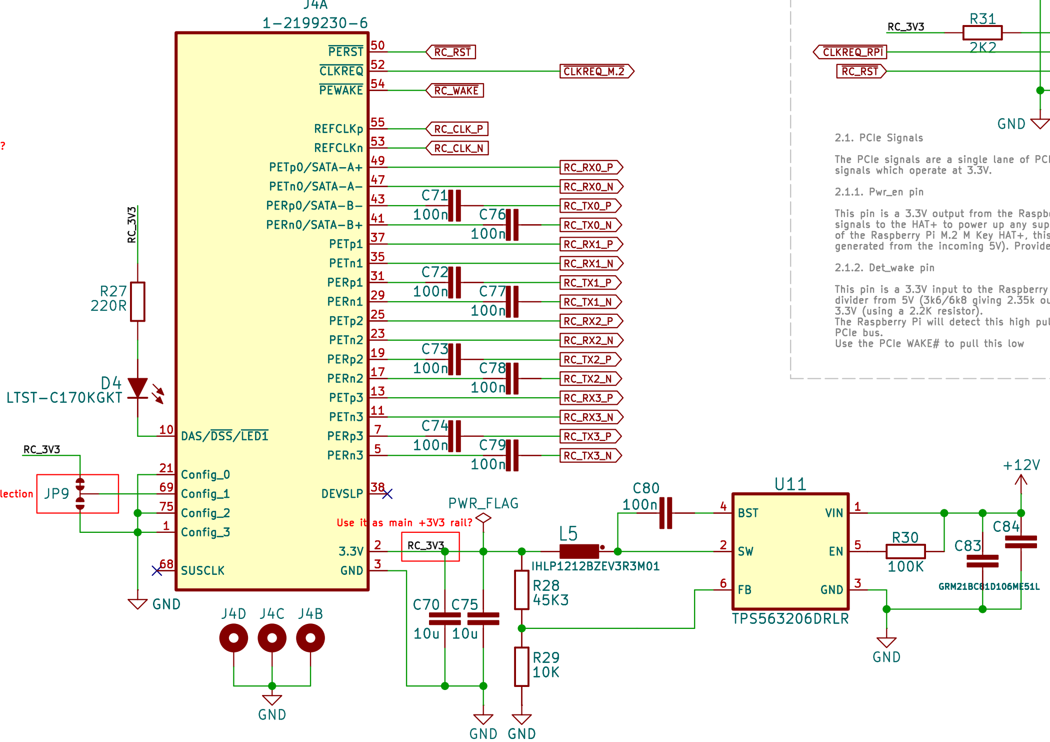
Size: A4	Date: 2025-02-02	**Rev: r1B1**
KiCad E.D.A. 8.0.8		Id: 3/6

4-lane PCIe for Root Complex

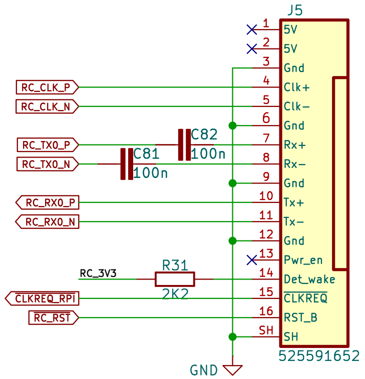


Lines #	Device
0	2-lines slot + M.2, Raspberry Pi PFC
1	2-lines slot + M.2
2	1-lines slot + M.2
3	PCIe switch for 4 x 1-lines + 4 x M.2

4-lane M.2 (Type M) for Root Complex



Raspberry Pi FPC 16-pin connector



2.1. PCIe Signals

The PCIe signals are a single lane of PCIe Gen 2, including CLKREQ and RST_B sideband signals which operate at 3.3V.

2.1.1. Pwr_en pin

This pin is a 3.3V output from the Raspberry Pi to a HAT+ or other add-on board, and signals to the HAT+ to power up any supplies. For example, in the instance of the Raspberry Pi M.2 M Key HAT+, this enables the M.2 3.3V power (which is generated from the incoming 5V). Provide a 100K low pull on this pin on any HAT+.

2.1.2. Det_wake pin

This pin is a 3.3V input to the Raspberry Pi. Pull high to 3.3V either from a resistive divider from 5V (3k6/6k8 giving 2.35k output impedance), or from permanently enabled 3.3V (using a 2.2K resistor).
The Raspberry Pi will detect this high pull at boot time, and will automatically probe the PCIe bus.
Use the PCIe WAKE# to pull this low

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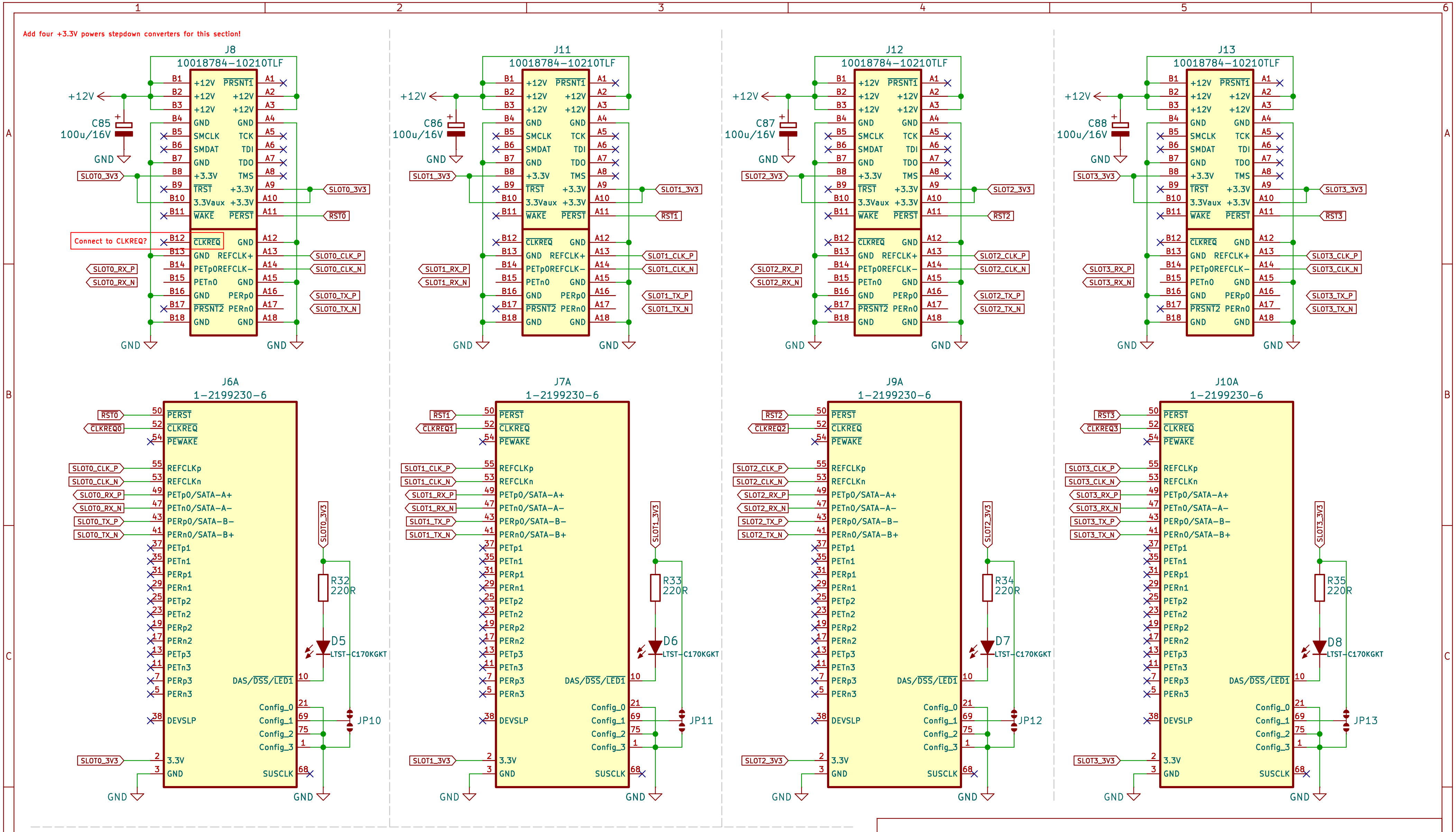
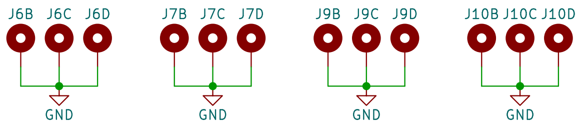
Sheet: /RC 4-lanes PCIe/
File: RC_4-lanes-PCIe.kicad_sch

Title:

Size: A4	Date: 2025-02-02	**Rev: r1B1**
KiCad E.D.A. 8.0.8		Id: 4/6

Add four +3.3V powers stepdown converters for this section!





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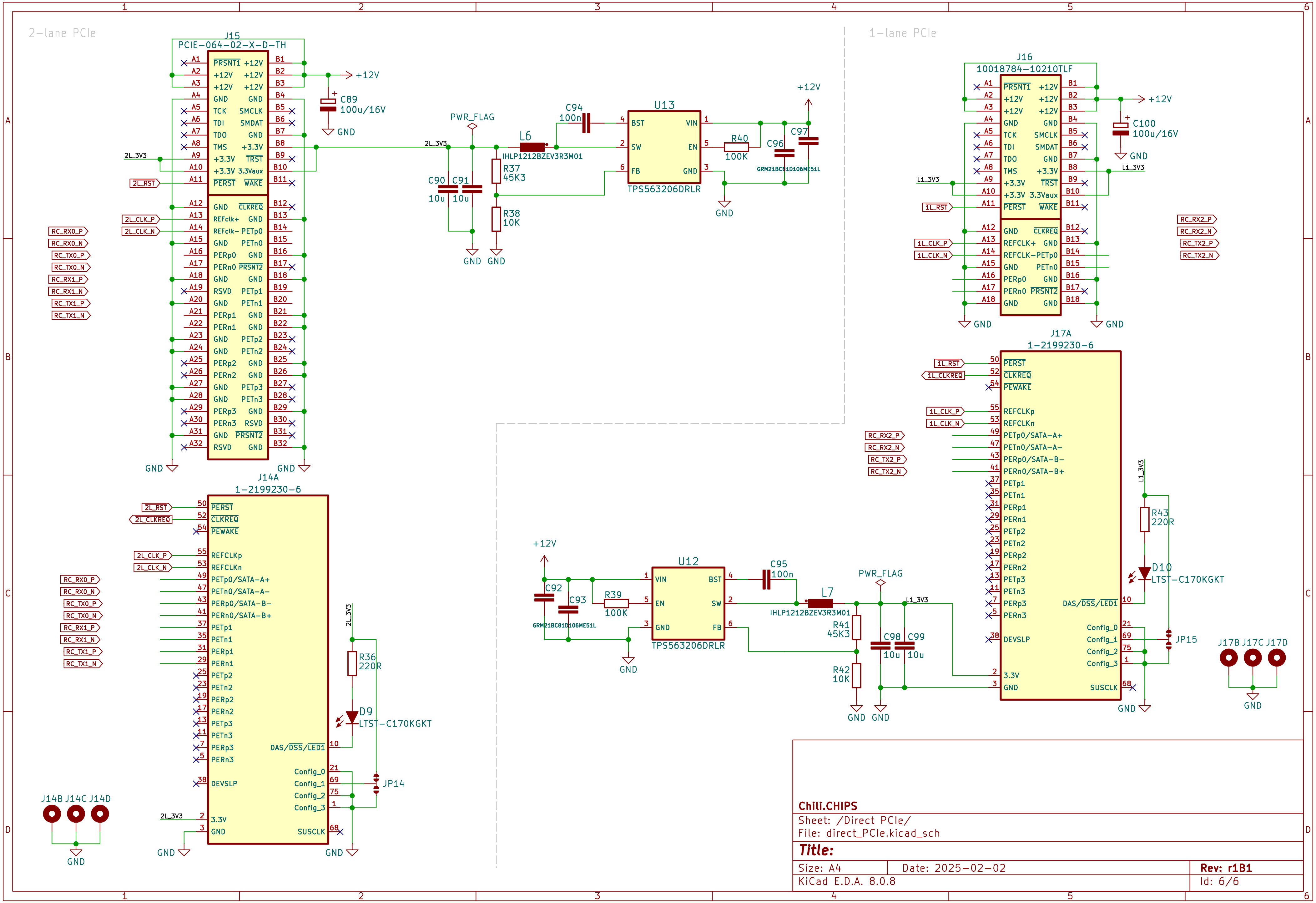
Sheet: /4 x 1-lanes PCIe/
File: 4_1-lanes_PCIe.kicad_sch

Title:

Size: A4	Date: 2025-02-02	**Rev: r1B1**
KiCad E.D.A. 8.0.8		Id: 5/6



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Sheet: /Direct PCIe/
File: direct_PCIe.kicad_sch

Title:

Size: A4 Date: 2025-02-02 Rev: r1B1
KiCad E.D.A. 8.0.8 Id: 6/6