PCIE mini Backplane

July 27, 2025

- POR reset circuit
- manual reset push-button
- reset distribution

PERST#

100MHz PCIE-approved REFCLK Gen

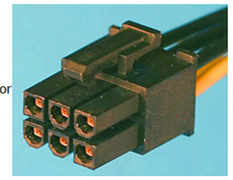
CLKREQ#

PCIE REFCLK distribution buffers

REFCLK+/-

6-pin PCIE Power connector
(3x12V, 3xGND)

PCI Express® power connector
1,2,3 +12V
4,5,6 COM



DC-DC and LDO, as needed, for power distribution

+3V3, +12V
cca 10W per slot, 70W total

4-lane "Direct" island
RC4 => EP4

RC4
4-lane RC connector with 2 mechanical options:
- **Slot**
- **M.2** (M-key, PCIE)

4 lanes

EP4
4-lane EP connector with 2 mechanical options:
- **Slot**
- **M.2** (M-key, PCIE)

1-lane "Switched" island
RC1=>SW=>SW_EP0/1/2/3

RC1
1-lane RC connector with 3 mechanical options:
- **Slot**
- **M.2** (M-key, PCIE)
- **1-lane RPi** (FPC 16pin, 0.5mm, 100ohm)

1 lane

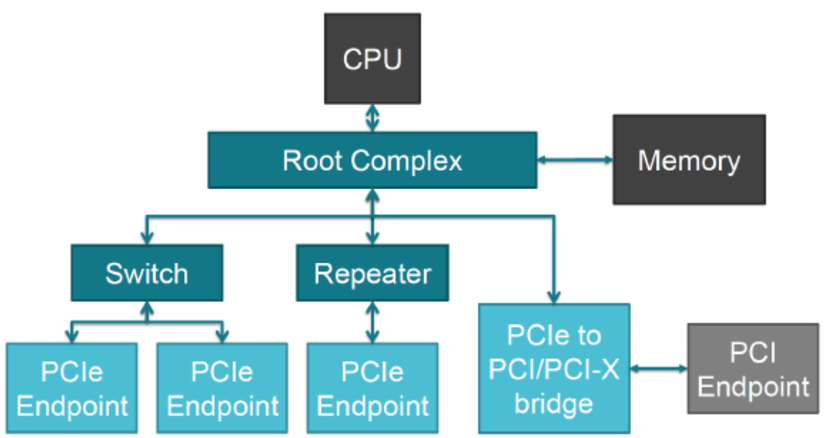
SWitch
PCIE2.0
1-lane
1-to-4

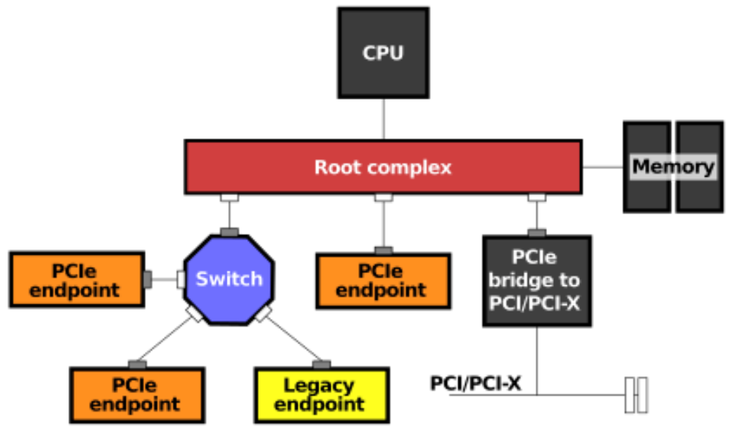
4 x 1 lane

SW_EP0	SW_EP1	SW_EP2	SW_EP3
1-lane EP connector - **Slot** - **M.2** (PCIE)	**1-lane EP** connector - **Slot** - **M.2** (PCIE)	**1-lane EP** connector - **Slot** - **M.2** (PCIE)	**1-lane EP** connector - **Slot** - **M.2** (PCIE)

The "RC Connectors" are for the plug-in cards that are natively EP.
It is the job of the backplane to swap the connector pins so that the Tx diff.pair on one side of the link is connected to the Rx diff.pair on the other side, and vice-versa. This allows the same FPGA plug-in card, which is always pined out to serve as an EP, to be used in both EP and RC roles.

General PCIE topology





PCIEx1 pinout

Pin	Side B	Side A	Description
1	+12 V	~~PRSNT1#~~	Must connect to farthest PRSNT2# pin
2	+12 V	+12 V	Main power pins
3	+12 V	+12 V	
4	Ground	Ground	
5	~~SMCLK~~	~~TCK~~	SMBus and JTAG port pins
6	~~SMDAT~~	~~TDI~~	
7	Ground	~~TDO~~	
8	+3.3 V	~~TMS~~	
9	~~TRST#~~	+3.3 V	
10	+3.3 V aux	+3.3 V	Aux power & Standby power
11	~~WAKE#~~	PERST#	Link reactivation; fundamental reset [25]
Key notch			
12	CLKREQ#[26]	Ground	Clock Request Signal
13	Ground	REFCLK+	Reference clock differential pair
14	HSOp(0)	REFCLK−	Lane 0 transmit data, + and −
15	HSOn(0)	Ground	
16	Ground	HSIp(0)	Lane 0 receive data, + and −
17	~~PRSNT2#~~	HSIn(0)	
18	Ground	Ground	
PCI Express x1 cards end at pin 18			

Legend	
Ground pin	Zero volt reference
Power pin	Supplies power to the PCIe card
Card-to-host pin	Signal from the card to the motherboard
Host-to-card pin	Signal from the motherboard to the card
Open drain	May be pulled low or sensed by multiple cards
Sense pin	Tied together on card
Reserved	Not presently used, do not connect