Clock generator & Reset fanout

File: clock_gen.kicad_sch

PCIe switch

File: pcie_switch.kicad_sch

RC 4-lanes PCIe

File: RC_4-lanes-PCIe.kicad_sch

4 x 1-lanes PCIe

File: 4_1-lanes_PCIe.kicad_sch

Direct PCIe

File: direct_PCIe.kicad_sch

H1 H2 H3 H4 H5 H6

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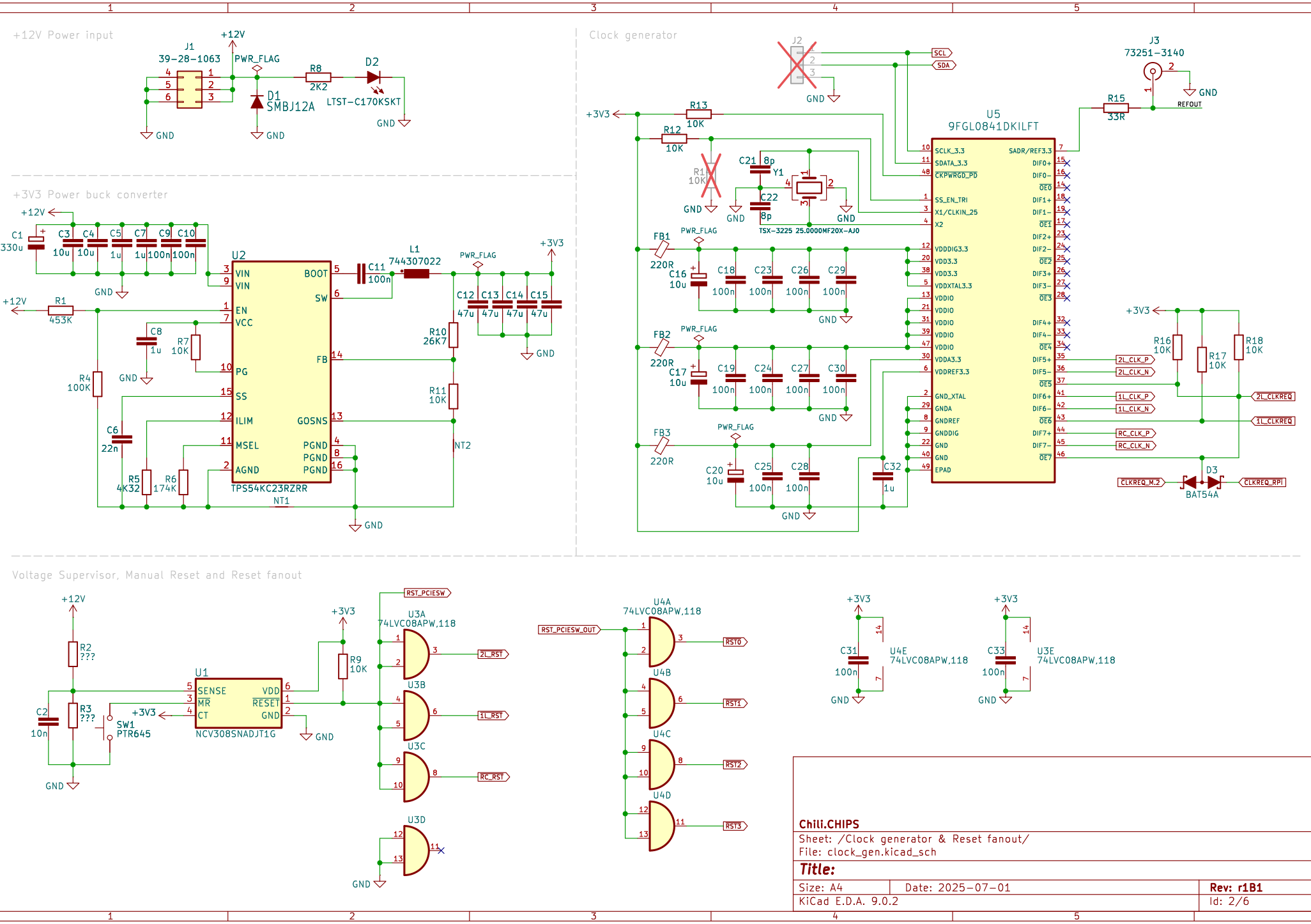
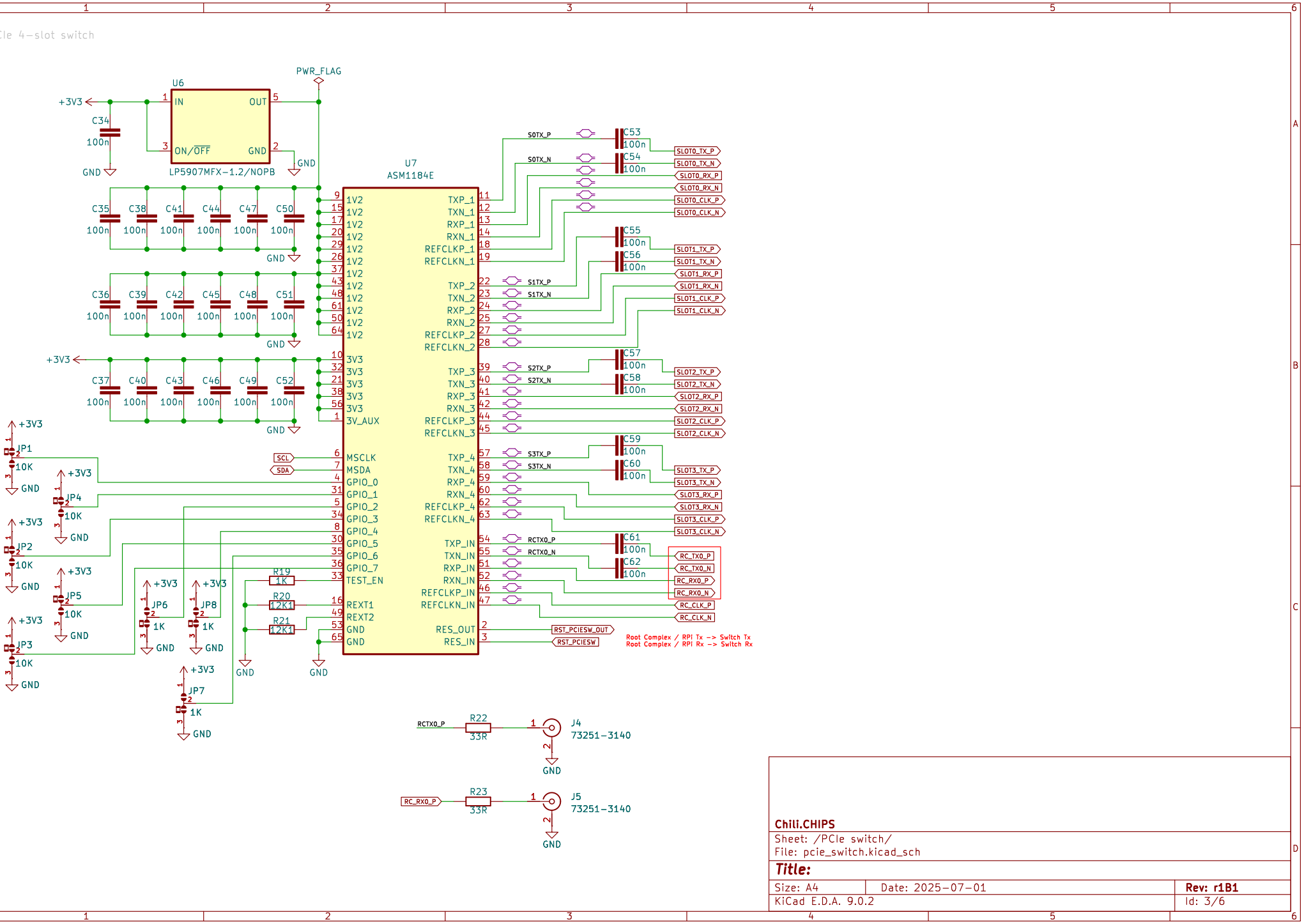
Sheet: /

File: openpci2-backplane.kicad_sch

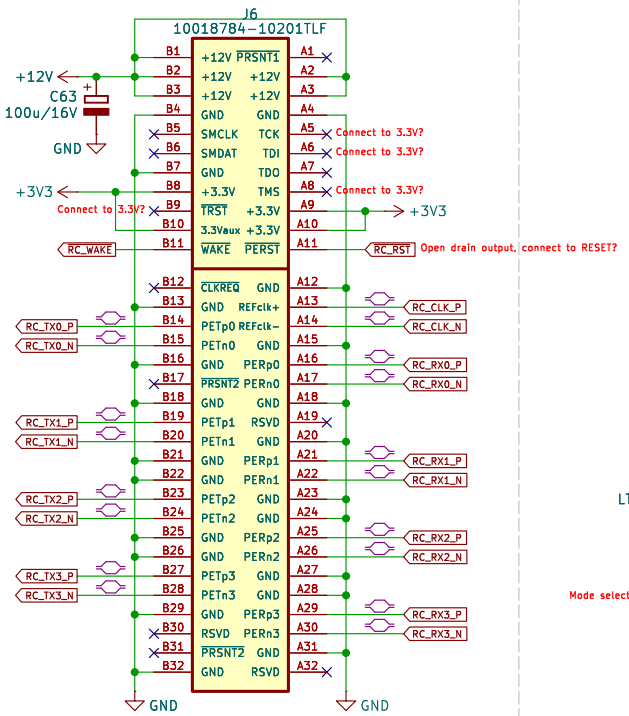
Title:

Size: A4	Date: 2025-07-01	Rev: r1B1
KiCad E.D.A. 9.0.2		Id: 1/6


+12V Power input
J1
39-28-1063
PWR_FLAG
R8
2K2
D2
LTST-C170KSKT
D1
SMBJ12A
+12V
GND
+3V3 Power buck converter
C1
330u
C3
10u
C4
10u
C5
1u
C7
1u
C9
100n
C10
100n
U2
VIN
VIN
EN
VCC
PG
SS
ILIM
MSEL
AGND
BOOT
SW
FB
GOSNS
PGND
PGND
PGND
TPS54KC23RZRR
L1
744307022
C11
100n
C12
47u
C13
47u
C14
47u
C15
47u
R1
453K
C8
1u
R7
10K
R4
100K
C6
22n
R5
4K32
R6
174K
R10
26K7
R11
10K
NT1
NT2
+3V3
Clock generator
J2
SCL
SDA
J3
73251-3140
REFOUT
R15
33R
U5
9FGL0841DKILFT
R13
10K
R12
10K
R14
10K
C21
8p
C22
8p
Y1
TSX-3225 25.0000MF20X-AJ0
FB1
FB2
FB3
220R
C16
10u
C17
10u
C18
100n
C19
100n
C20
10u
C23
100n
C24
100n
C25
100n
C26
100n
C27
100n
C28
100n
C29
100n
C30
100n
C32
1u
SCLK_3.3
SDATA_3.3
CKPWRGD_PD
SS_EN_TRI
X1/CLKIN_25
X2
VDDDIG3.3
VDD3.3
VDD3.3
VDDXTAL3.3
VDDIO
VDDIO
VDDIO
VDDIO
VDDIO
VDDA3.3
VDDREF3.3
GND_XTAL
GNDA
GNDREF
GNDDIG
GND
GND
EPAD
SADR/REF3.3
DIF0+
DIF0−
OE0
DIF1+
DIF1−
OE1
DIF2+
DIF2−
OE2
DIF3+
DIF3−
OE3
DIF4+
DIF4−
OE4
DIF5+
DIF5−
OE5
DIF6+
DIF6−
OE6
DIF7+
DIF7−
OE7
2L_CLK_P
2L_CLK_N
1L_CLK_P
1L_CLK_N
RC_CLK_P
RC_CLK_N
R16
10K
R17
10K
R18
10K
2L_CLKREQ
1L_CLKREQ
D3
BAT54A
CLKREQ_M.2
CLKREQ_RPI
Voltage Supervisor, Manual Reset and Reset fanout
R2
???
R3
???
C2
10n
SW1
PTR645
U1
SENSE
MR
CT
VDD
RESET
GND
NCV308SNADJT1G
R9
10K
RST_PCIESW
U3A
74LVC08APW,118
U3B
U3C
U3D
2L_RST
1L_RST
RC_RST
RST_PCIESW_OUT
U4A
74LVC08APW,118
U4B
U4C
U4D
RST0
RST1
RST2
RST3
C31
100n
U4E
74LVC08APW,118
C33
100n
U3E
74LVC08APW,118
Chili.CHIPS
Sheet: /Clock generator & Reset fanout/
File: clock_gen.kicad_sch
Title:
Size: A4
Date: 2025-07-01
Rev: r1B1
KiCad E.D.A. 9.0.2
Id: 2/6

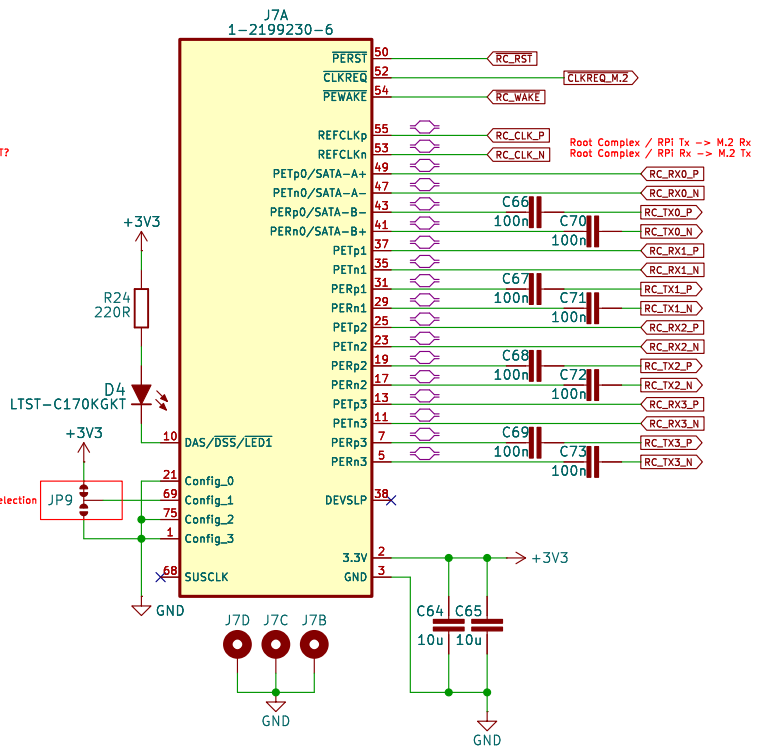

PCIe 4-slot switch
U6
LP5907MFX-1.2/NOPB
PWR_FLAG
U7
ASM1184E
Root Complex / RPi Tx -> Switch Tx
Root Complex / RPi Rx -> Switch Rx
Chili.CHIPS
Sheet: /PCIe switch/
File: pcie_switch.kicad_sch
Title:
Size: A4
Date: 2025-07-01
Rev: r1B1
KiCad E.D.A. 9.0.2
Id: 3/6

4-lane PCIe for Root Complex

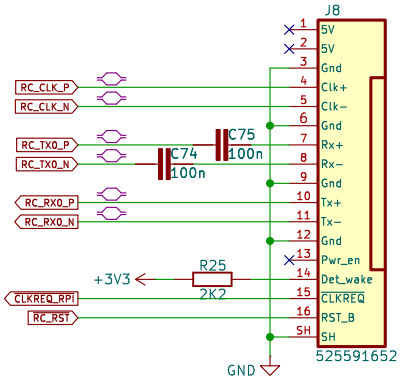


Lanes #	Device
0	PCIe switch for 4 x 1-lanes + 4 x M.2
1	1-lanes slot + M.2
2	2-lanes slot + M.2 (First)
3	2-lanes slot + M.2 (Second)

4-lane M.2 (Type M) for Root Complex



Raspberry Pi FPC 16-pin connector



2.1. PCIe Signals

The PCIe signals are a single lane of PCIe Gen 2, including CLKREQ and RST_B sideband signals which operate at 3.3V.

2.1.1. Pwr_en pin

This pin is a 3.3V output from the Raspberry PI to a HAT+ or other add-on board, and signals to the HAT+ to power up any supplies. For example, in the Instance of the Raspberry PI M.2 M Key HAT+, this enables the M.2 3.3V power (which is generated from the incoming 5V). Provide a 100K low pull on this pin on any HAT+.

2.1.2. Det_wake pin

This pin is a 3.3V input to the Raspberry PI. Pull high to 3.3V either from a resistive divider from 5V (3k6/6k8 giving 2.35k output impedance), or from permanently enabled 3.3V (using a 2.2K resistor).
The Raspberry PI will detect this high pull at boot time, and will automatically probe the PCIe bus.
Use the PCIe WAKE# to pull this low

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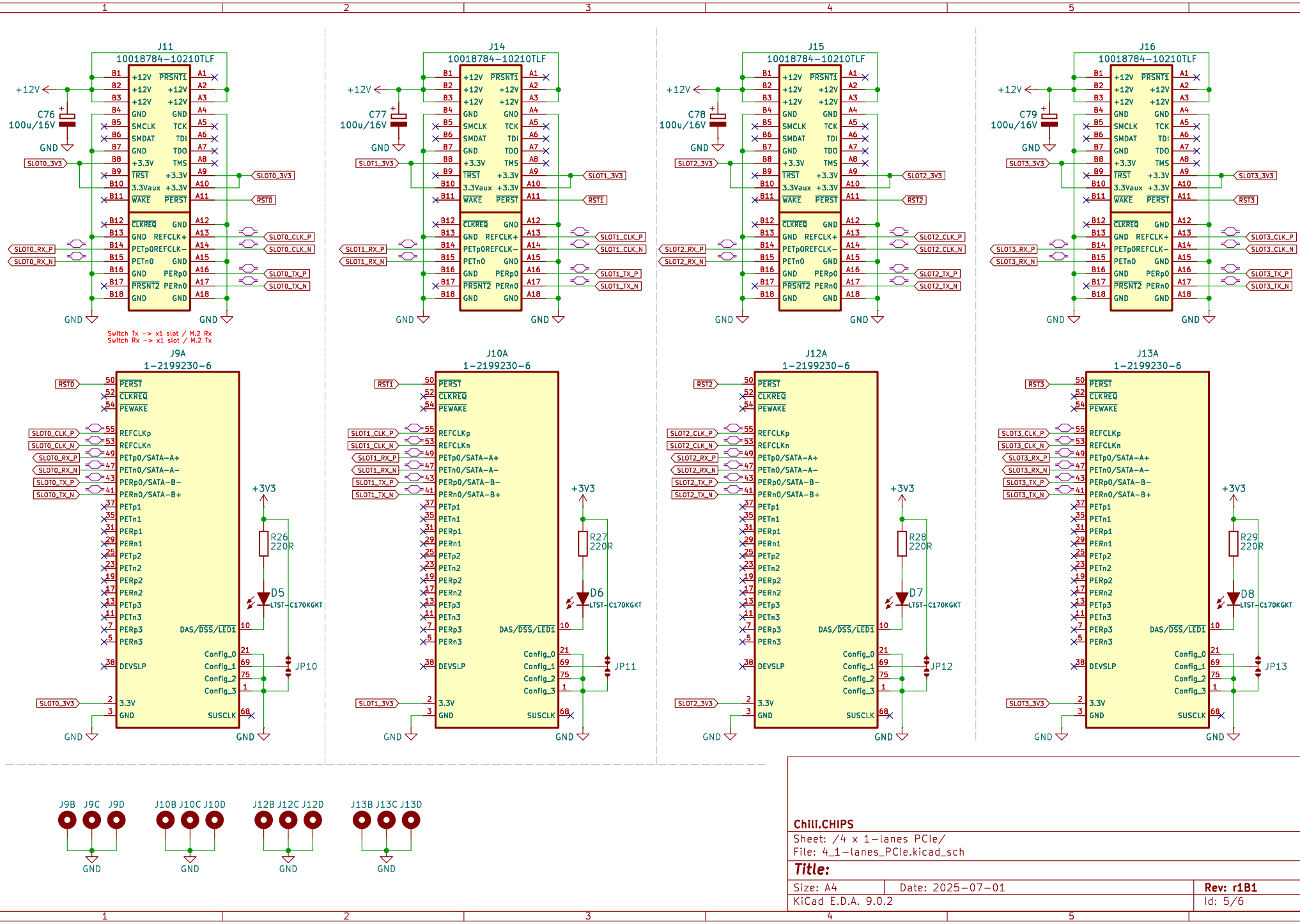
Sheet: /RC 4-lanes PCIe/
File: RC_4-lanes-PCIe.kicad_sch

Title:

Size: A4	Date: 2025-07-01	**Rev: r1B1**
KiCad E.D.A. 9.0.2		Id: 4/6



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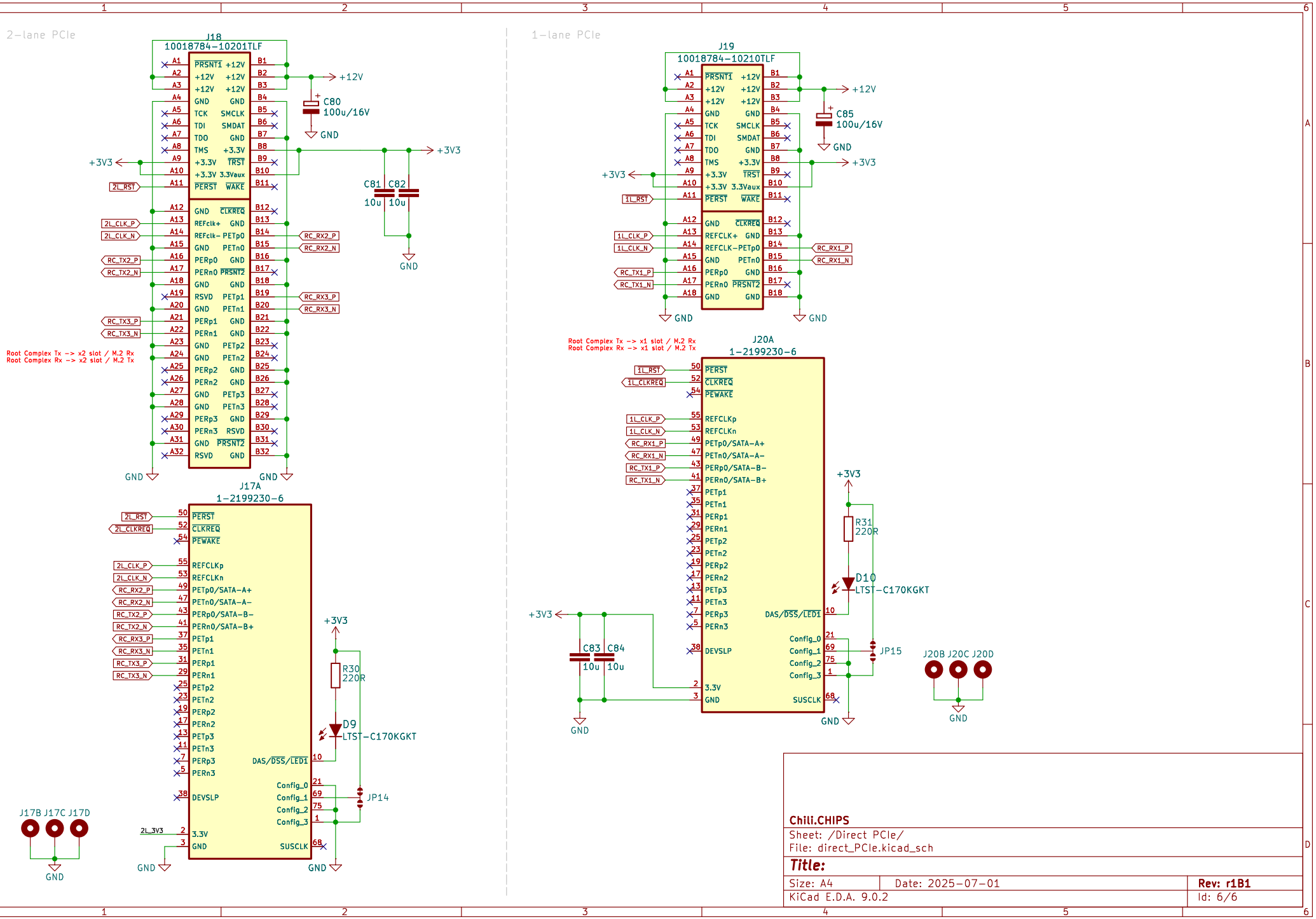
Sheet: /4 x 1-lanes PCIe/

File: 4_1-lanes_PCIe.kicad_sch

Title:

Size: A4	Date: 2025-07-01	**Rev: r1B1**
KiCad E.D.A. 9.0.2		Id: 5/6



Chili.CHIPS		
Sheet: /Direct PCIe/		
File: direct_PCIe.kicad_sch		
Title:		
Size: A4	Date: 2025-07-01	**Rev: r1B1**
KiCad E.D.A. 9.0.2		Id: 6/6