PCBA Functional Test Procedure

Prepared for: Elecrow
Project: openpci2-backplane

December 1, 2025

Introduction

This document outlines the mandatory functional test procedures for the openpci2-backplane PCBA after assembly. The purpose of this test is to verify the soldering quality, power supply stability, and basic signal integrity before the units are shipped.

Please follow the steps sequentially. If any step fails, the board should be marked as "Failed" and separated for inspection.

1 Power Supply Verification

1. **Step 1.1:** Connect the main power supply (**standard 6-pin PCIe power connector (3 × +12V, 3 × GND), up to 70W total**) to the board input connector.
2. **Step 1.2:** Using a Digital Multimeter, measure the voltages at the specific test points indicated in **Figure 1** below. Reference all measurements to the board Ground (GND).

   Verify the following voltage rails are present and stable:

   - **12V** (Main Input)
   - **3V3** (Output from DC/DC Buck Converter)
   - **1V8**
   - **1V2**

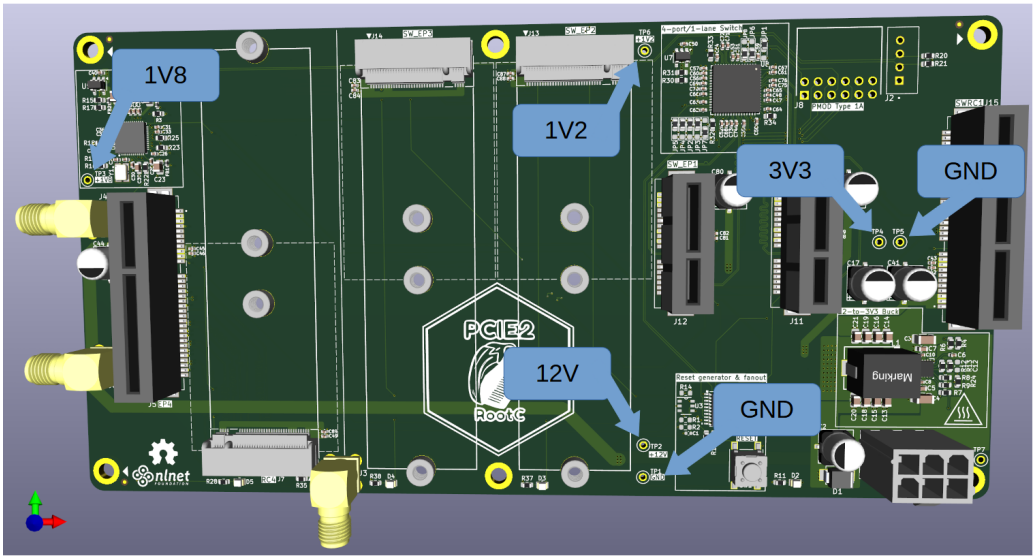

Figure 1: Voltage Measurement Points

2 Reset Circuit Verification

The objective of this section is to verify that the manual reset signal is correctly distributed to all destination points on the backplane.

1. **Step 2.1:** Ensure the board is powered (12V applied).
2. **Step 2.2:** Locate the **RESET Button** and the **7 specific Reset Test Points** indicated in **Figure 2**.
3. **Step 2.3: Idle State Check:** Without pressing the button, measure the voltage at **all 7 test points**.
   - Verify that **all 7 points** are at a **High Logic Level (≈ 3V3)**.
4. **Step 2.4: Active State Check:** Press and **hold** the RESET Button. While holding the button, measure the voltage at **all 7 test points** again.
   - Verify that **all 7 points** drop to a **Low Logic Level (≈ 0V / GND)**.
5. **Step 2.5:** Release the button and confirm that **all 7 test points** return to a **High Logic Level (≈ 3V3)**.

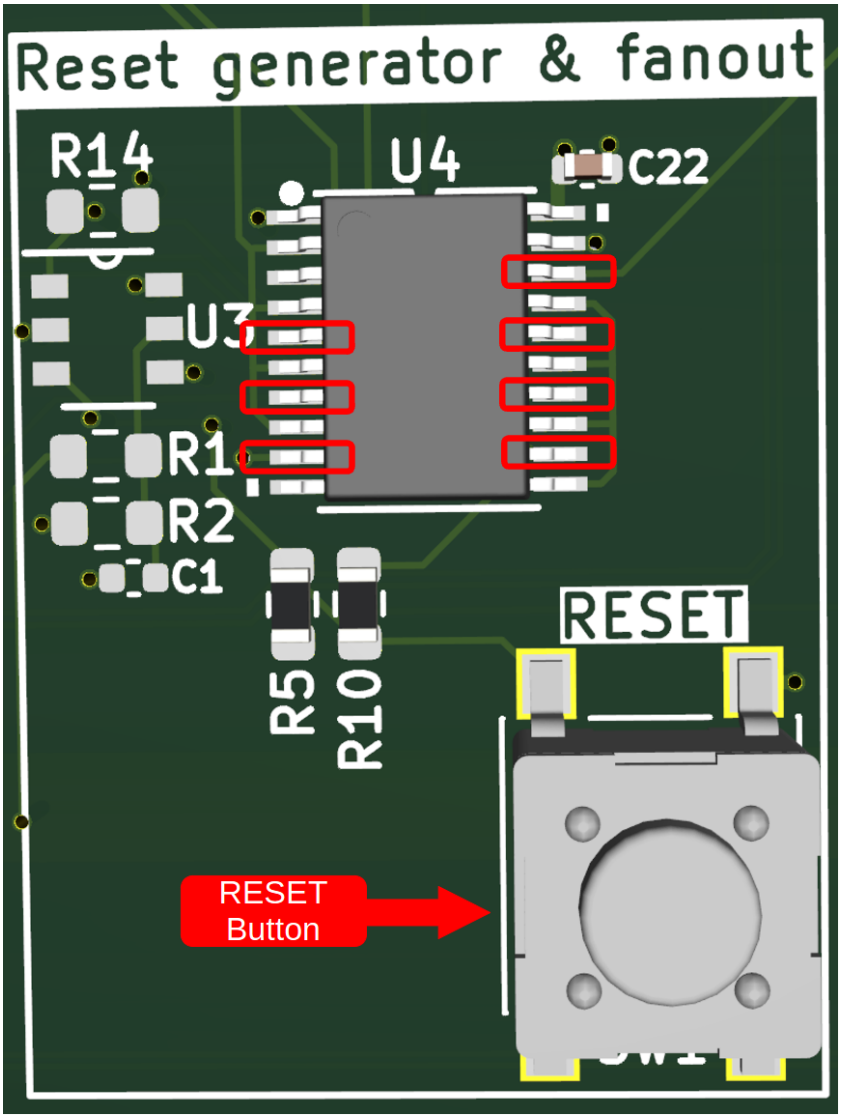

Figure 2: Location of Reset Button and the 7 Verification Points

3 Reference Clock Verification

The objective of this section is to verify the clock generator chip functionality. This is done in two parts: first by checking the primary reference output, and second by verifying the individual PCIe clocks.

3.1 Part 1: Primary Reference Check (25 MHz)

Objective: Verify that the clock generator is active and the crystal is oscillating.

1. **Step 3.1:** Ensure the board is powered (12V).
2. **Step 3.2:** Locate **Resistor R22** (Series resistor for the SMA connector J4). See **Figure 3**.
3. **Step 3.3:** Probe the signal on **R22**.
4. **Step 3.4:** Verify the signal parameters:
   - **Frequency: 25 MHz**
   - **Waveform:** Clean square/sine-like wave.
   - **Amplitude:** Logic High (V_{OH}) should be **>1.35V** (typically ≈ 1.8V). Logic Low (V_{OL}) should be **<0.45V** (typically ≈ 0V).
5. **Decision:** If this signal is **ABSENT**, the clock chip is not running. **STOP the test**. If present, proceed to Part 2.

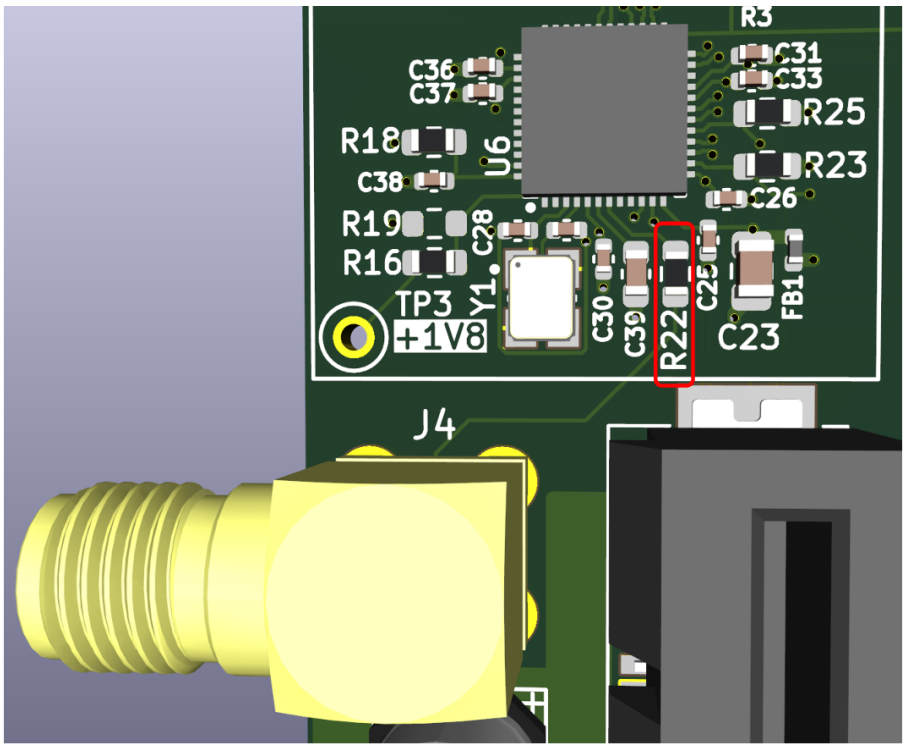

Figure 3: Location of Resistor R22 (25MHz Check)

3.2 Part 2: PCIe Output Verification (100 MHz)

Objective: Verify the presence of the 100 MHz PCIe reference clock outputs, confirm that the clock generator correctly drives the PCIe Switch, and verify that the Switch distributes the clock to downstream endpoints.

Test Strategy: We will activate the clock on the main upstream slot (**SWRC1**) by pulling its CLKREQ# signal low. This action enables the clock generator output which feeds both the SWRC1 slot and the PCIe Switch input. Once the Switch receives the reference clock, it should automatically distribute it to the downstream x1 slot (**SW_EP1**).

1. **Step 3.5: Activate Clock on SWRC1**
    - Locate the PCIe x4 slot labeled **SWRC1**.
    - Insert a jumper wire directly into the slot connector to bridge the **CLKREQ# pin (B12)** to **GND (B13)**.
    - Refer to **Figure 4** for the exact pin position and method.

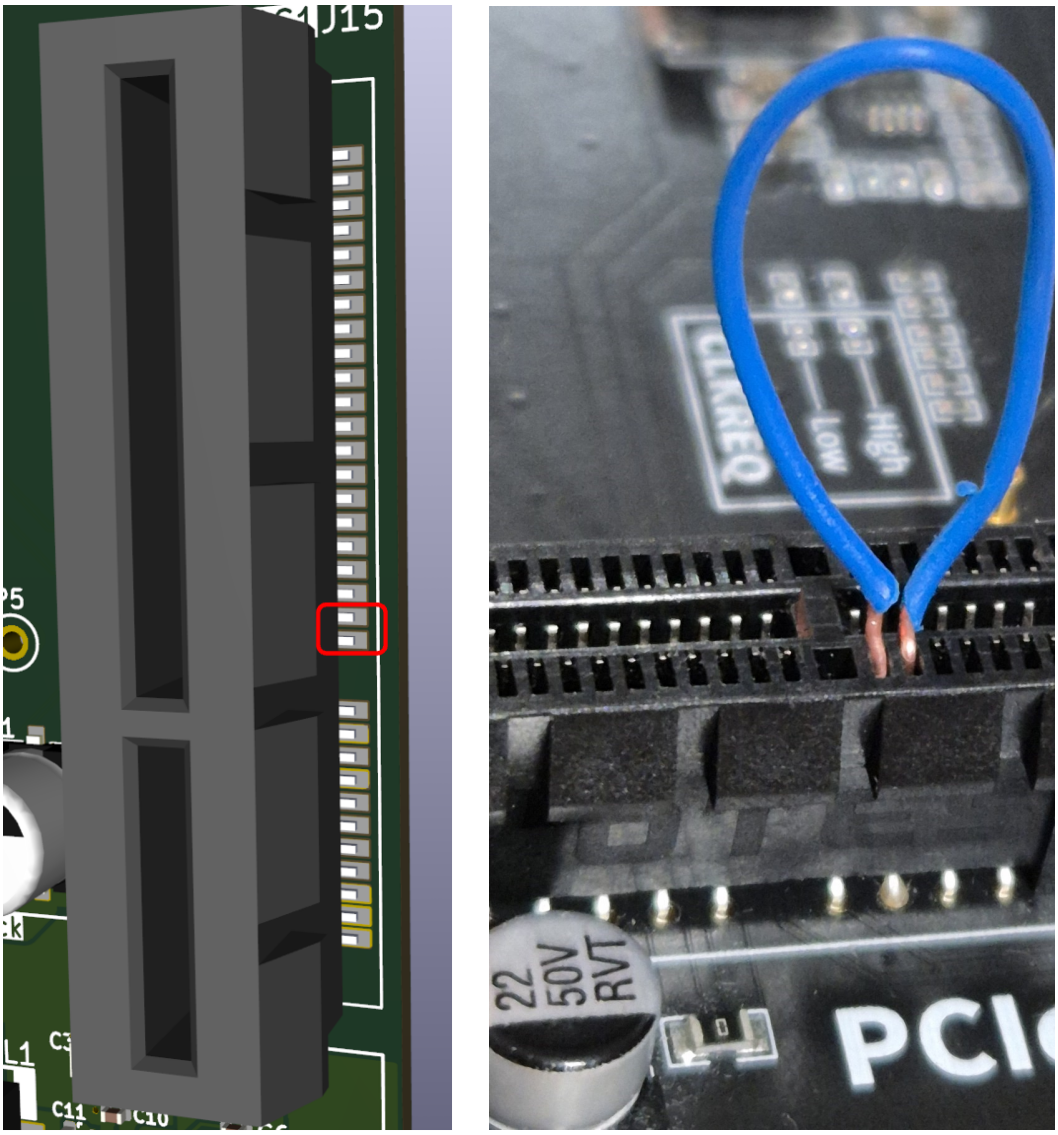

Figure 4: Activation Method: Shorting CLKREQ# to GND on SWRC1

2. **Step 3.6: Measure Input Clock (at SWRC1)**

   - While the jumper is inserted, probe the clock pins (A13/A14) on the **SWRC1** slot (at the connector entrance). **Refer to Figure 5.**
   - **Verify:** 100 MHz clock is present.

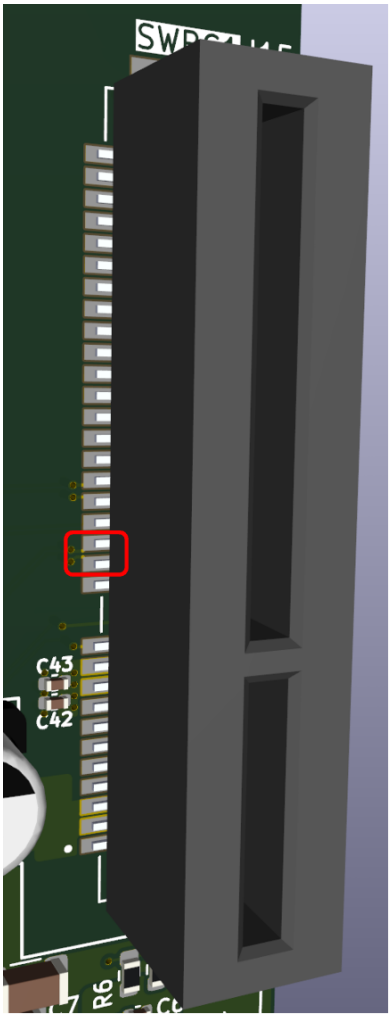

Figure 5: Measurement points on SWRC1

3. **Step 3.7: Measure Downstream Clock (at SW_EP1)**

   - Locate the PCIe x1 slot labeled **SW_EP1**.
   - Probe the clock pins (A13/A14) on **SW_EP1**. **Refer to Figure 6.**
   - **Verify:** 100 MHz clock is present.
   - *Note: If the clock is present here, it confirms the PCIe Switch is functioning.*

4. **Step 3.8: Signal Parameters Verification**

   - **Frequency: 100 MHz**
   - **Waveform:** Clean square/sine-like wave (HCSL).
   - **Amplitude:** Logic High (V_{OH}) approx. **0.7V - 0.8V**. Logic Low (V_{OL}) approx. **0V**.

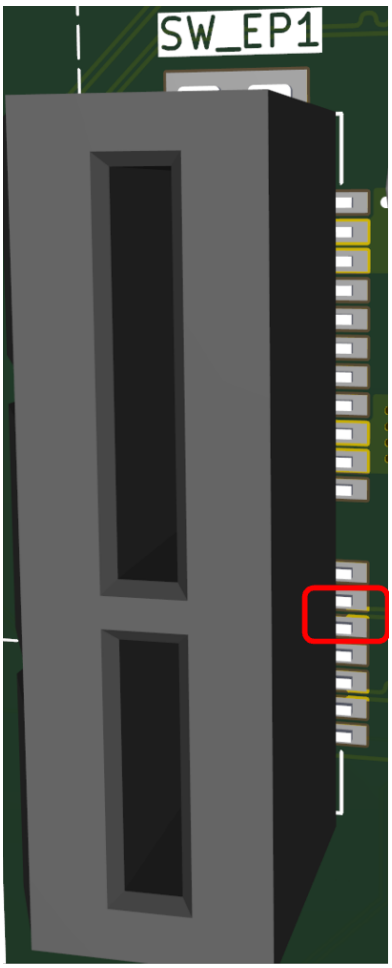

Figure 6: Measurement points on SW_EP1

End of Test Procedure
If all steps passed, mark the board as **"PASSED"**.