Clock generator & Reset fanout

File: clock_gen.kicad_sch

PCIe switch

File: pcie_switch.kicad_sch

RC 4-lanes PCIe

File: RC_4-lanes-PCIe.kicad_sch

4 x 1-lanes PCIe

File: 4_1-lanes_PCIe.kicad_sch

Direct PCIe

File: direct_PCIe.kicad_sch

H1 H2 H3 H4 H5 H6

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Sheet: /

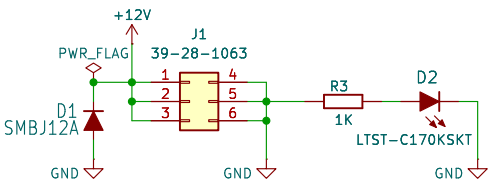
File: openpci2-backplane.kicad_sch

Title:

Size: A4	Date: 2025-01-29	**Rev: r1B1**
KiCad E.D.A. 8.0.8		Id: 1/6

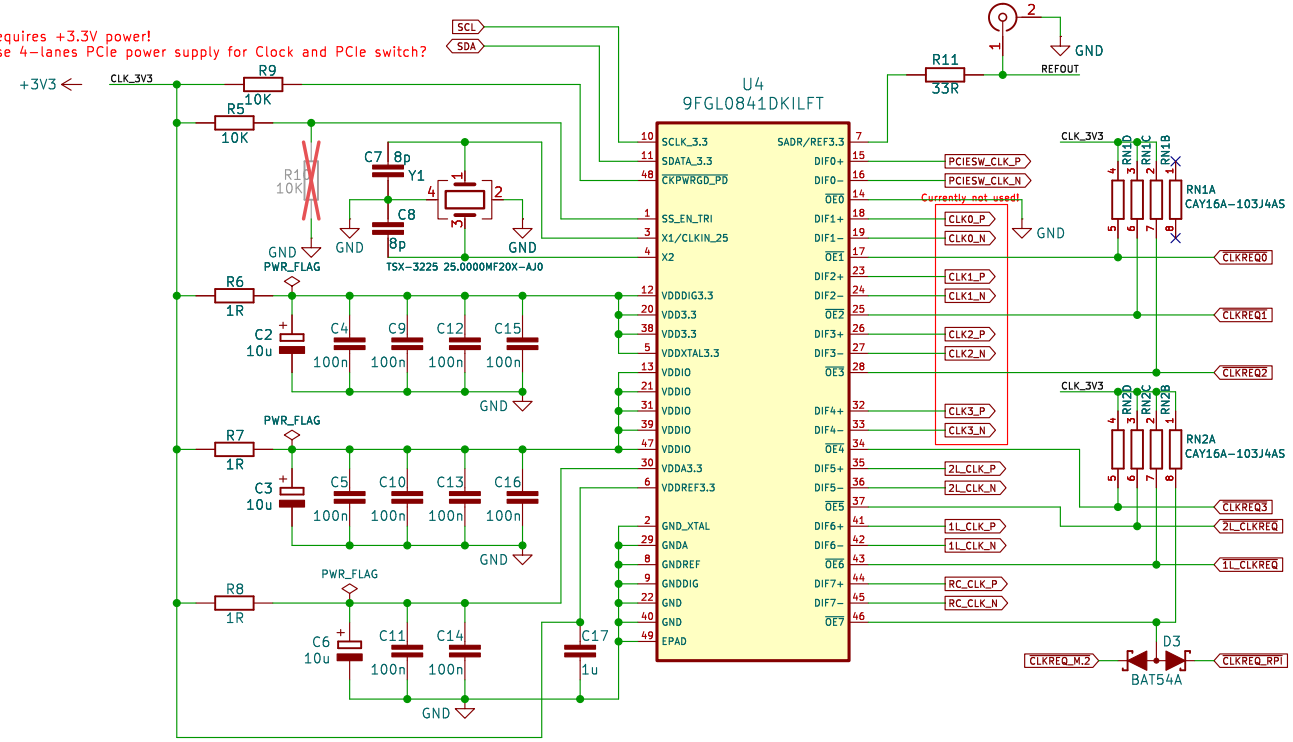
+12V Power input

One high power down converter or one per slot?

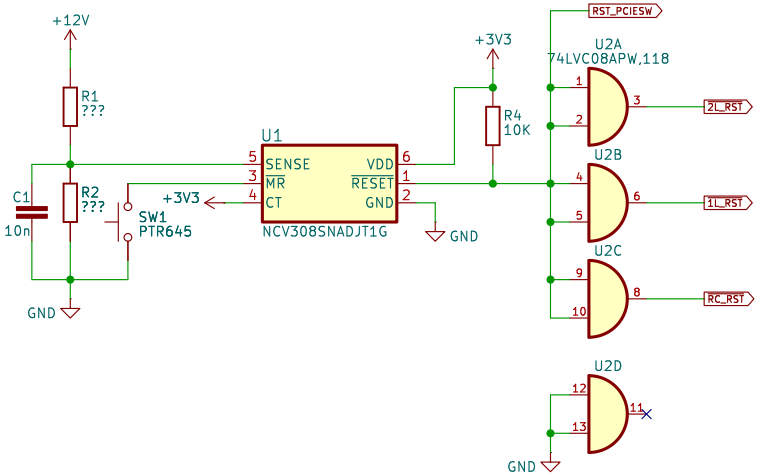


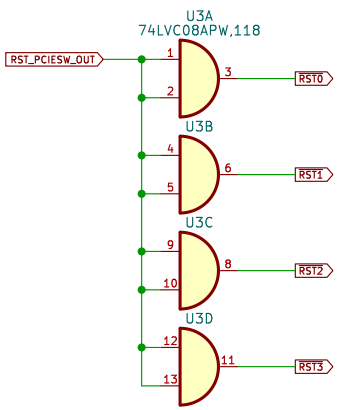
Clock generator

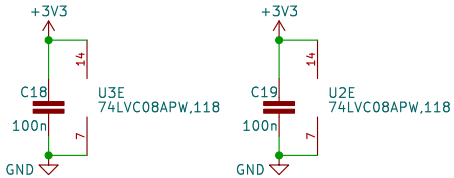
Requires +3.3V power!
Use 4-lanes PCIe power supply for Clock and PCIe switch?



Voltage Supervisor, Manual Reset and Reset fanout







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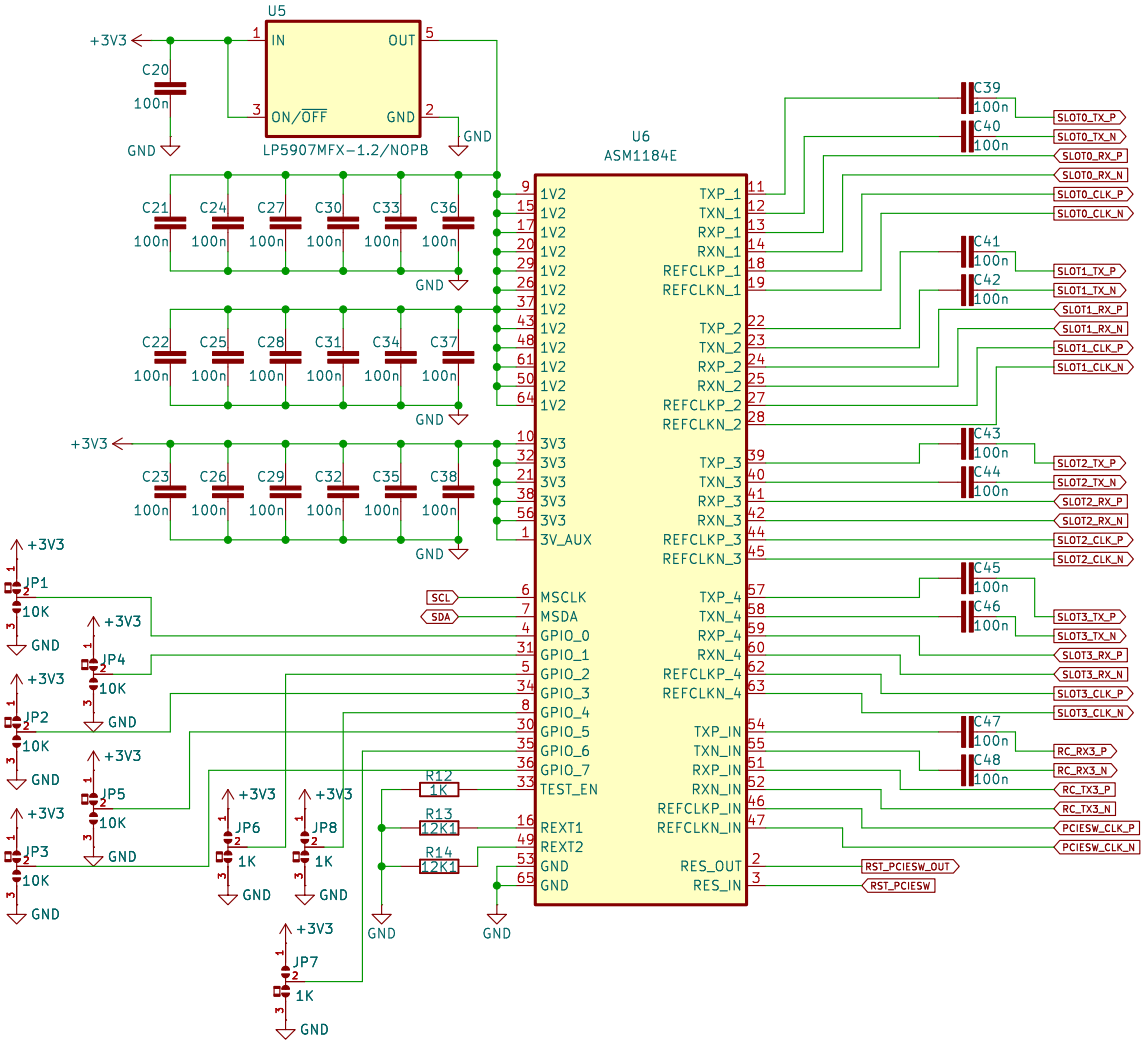
Sheet: /Clock generator & Reset fanout/
File: clock_gen.kicad_sch

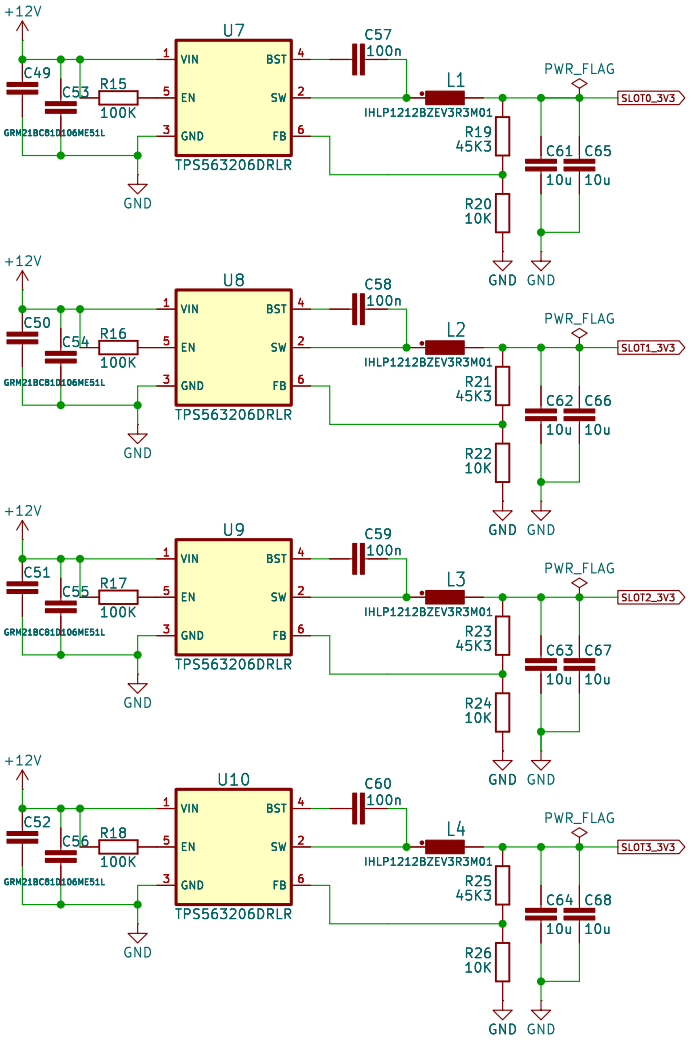
Title:

Size: A4	Date: 2025-01-29	**Rev: r1B1**
KiCad E.D.A. 8.0.8		Id: 2/6

PCIe 4-slot switch

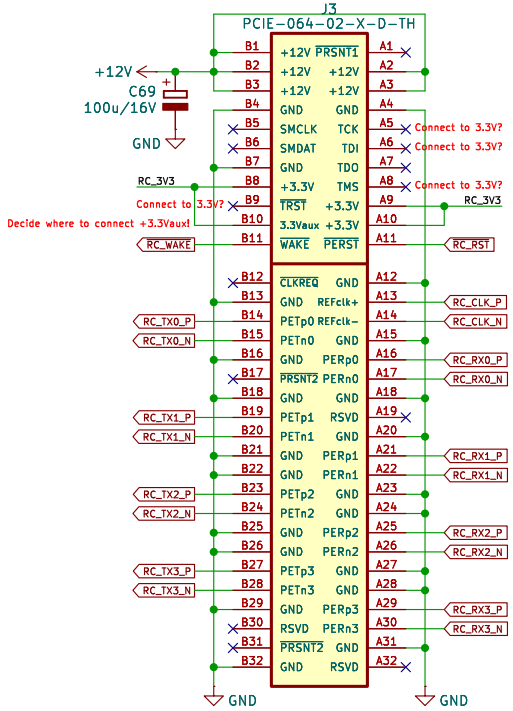


Point-of-load stepdown converters for 1-lanes PCIe



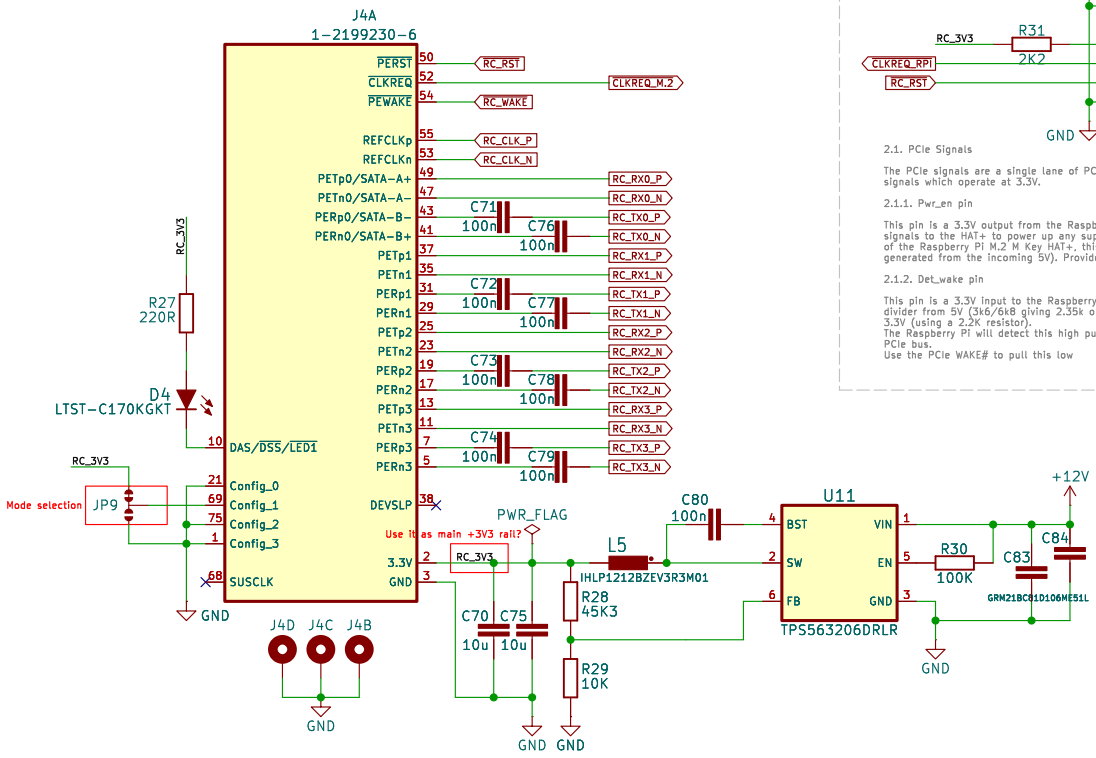
Chili.CHIPS	
Sheet: /PCIe switch/	
File: pcie_switch.kicad_sch	
Title:	
Size: A4	Date: 2025-01-29
KiCad E.D.A. 8.0.8	**Rev: r1B1**
	Id: 3/6

4-lanes PCIe for Root Complex

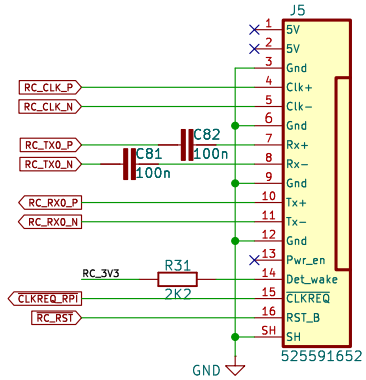


Lines #	Device
0	2-lines slot + M.2, Raspberry Pi PFC
1	2-lines slot + M.2
2	1-lines slot + M.2
3	PCIe switch for 4 x 1-lines + 4 x M.2

4-lanes M.2 (Type M) for Root Complex



Raspberry Pi FPC 16-pin connector



2.1. PCIe Signals

The PCIe signals are a single lane of PCIe Gen 2, including CLKREQ and RST_B sideband signals which operate at 3.3V.

2.1.1. Pwr_en pin

This pin is a 3.3V output from the Raspberry PI to a HAT+ or other add-on board, and signals to the HAT+ to power up any supplies. For example, in the Instance of the Raspberry PI M.2 M Key HAT+, this enables the M.2 3.3V power (which is generated from the incoming 5V). Provide a 100K low pull on this pin on any HAT+.

2.1.2. Det_wake pin

This pin is a 3.3V input to the Raspberry Pi. Pull high to 3.3V either from a resistive divider from 5V (3k6/6k8 giving 2.35k output impedance), or from permanently enabled 3.3V (using a 2.2K resistor).
The Raspberry PI will detect this high pull at boot time, and will automatically probe the PCIe bus.
Use the PCIe WAKE# to pull this low

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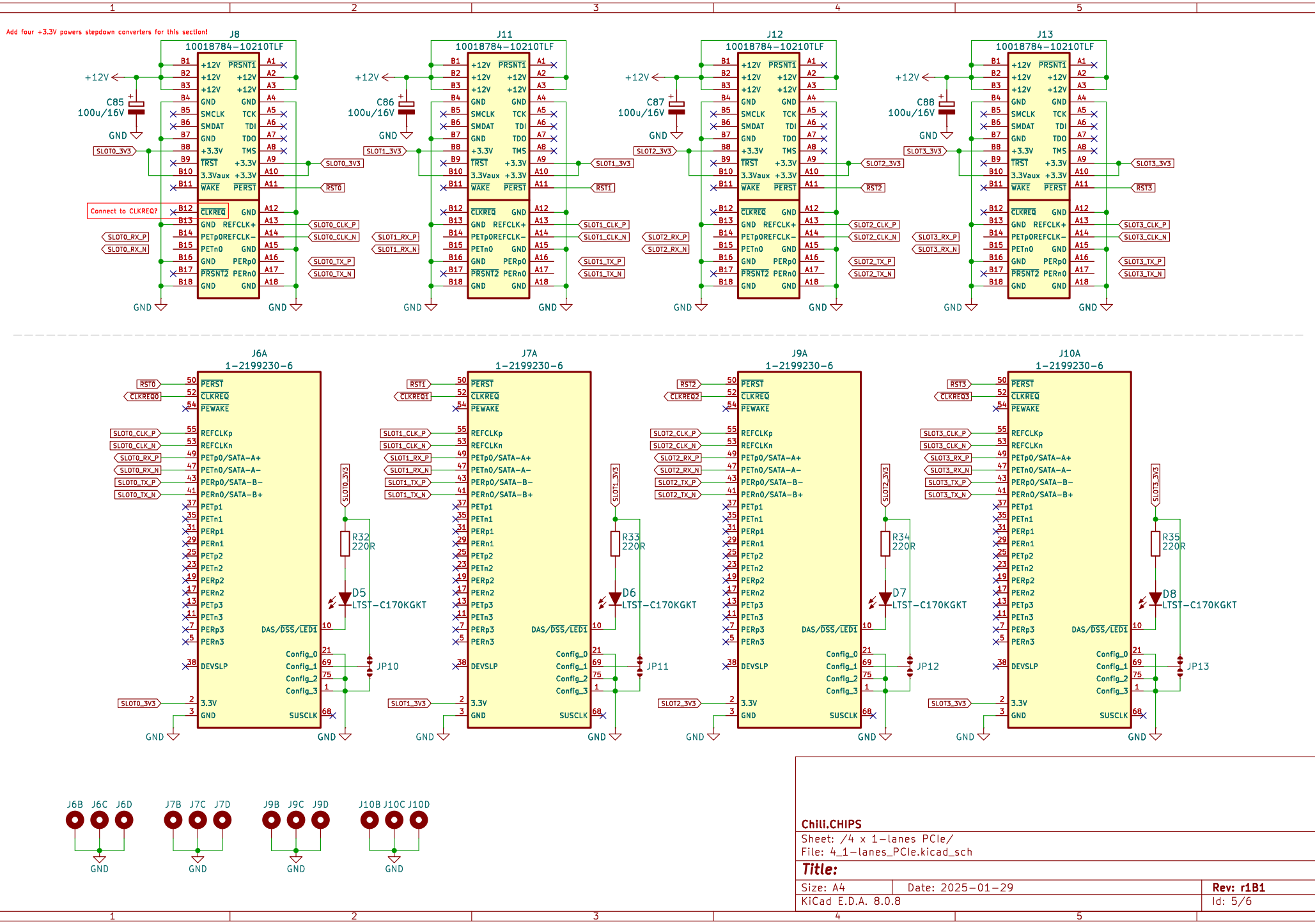
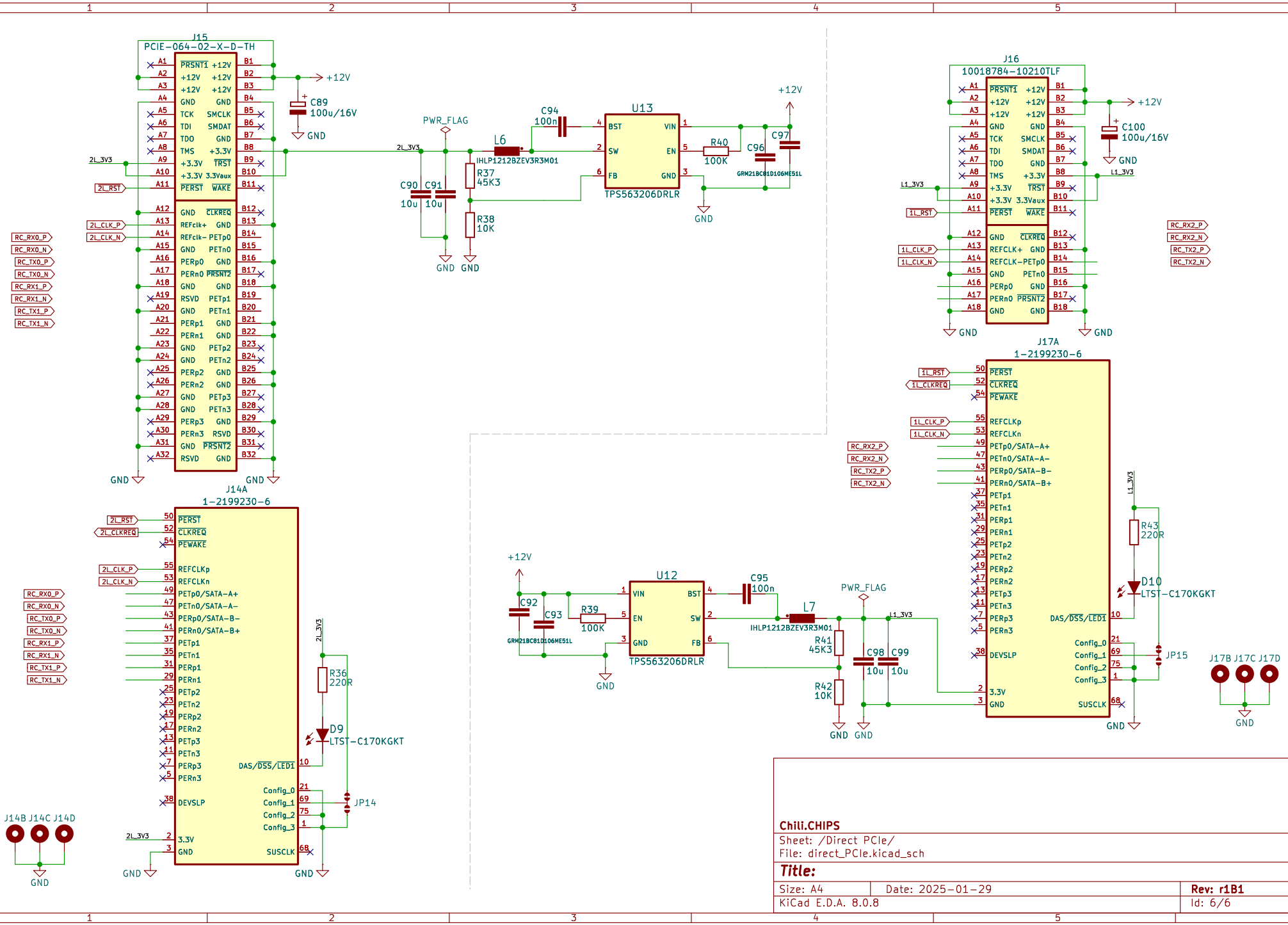
Sheet: /RC 4-lanes PCIe/
File: RC_4-lanes-PCIe.kicad_sch

Title:

Size: A4	Date: 2025-01-29	**Rev: r1B1**
KiCad E.D.A. 8.0.8		Id: 4/6


Add four +3.3V powers stepdown converters for this section!
J8
J11
J12
J13
10018784-10210TLF
+12V
C85
100u/16V
C86
C87
C88
GND
SLOT0_3V3
SLOT1_3V3
SLOT2_3V3
SLOT3_3V3
Connect to CLKREQ?
RST0
RST1
RST2
RST3
SLOT0_CLK_P
SLOT0_CLK_N
SLOT0_RX_P
SLOT0_RX_N
SLOT0_TX_P
SLOT0_TX_N
SLOT1_CLK_P
SLOT1_CLK_N
SLOT1_RX_P
SLOT1_RX_N
SLOT1_TX_P
SLOT1_TX_N
SLOT2_CLK_P
SLOT2_CLK_N
SLOT2_RX_P
SLOT2_RX_N
SLOT2_TX_P
SLOT2_TX_N
SLOT3_CLK_P
SLOT3_CLK_N
SLOT3_RX_P
SLOT3_RX_N
SLOT3_TX_P
SLOT3_TX_N
J6A
J7A
J9A
J10A
1-2199230-6
CLKREQ0
CLKREQ1
CLKREQ2
CLKREQ3
R32
R33
R34
R35
220R
D5
D6
D7
D8
LTST-C170KGKT
JP10
JP11
JP12
JP13
J6B J6C J6D
J7B J7C J7D
J9B J9C J9D
J10B J10C J10D
Chili.CHIPS
Sheet: /4 x 1-lanes PCIe/
File: 4_1-lanes_PCIe.kicad_sch
Title:
Size: A4
Date: 2025-01-29
Rev: r1B1
KiCad E.D.A. 8.0.8
Id: 5/6


J15
PCIE-064-02-X-D-TH
+12V
C89
100u/16V
GND
PWR_FLAG
L6
IHLP1212BZEV3R3M01
C94
100n
U13
TPS563206DRLR
R37
45K3
R38
10K
C90
10u
C91
10u
R40
100K
C96
C97
GRM21BC81D106ME51L
2L_3V3
2L_RST
2L_CLK_P
2L_CLK_N
RC_RX0_P
RC_RX0_N
RC_TX0_P
RC_TX0_N
RC_RX1_P
RC_RX1_N
RC_TX1_P
RC_TX1_N
J16
10018784-10210TLF
C100
100u/16V
L1_3V3
1L_RST
1L_CLK_P
1L_CLK_N
RC_RX2_P
RC_RX2_N
RC_TX2_P
RC_TX2_N
J14A
1-2199230-6
J17A
1-2199230-6
R36
220R
D9
LTST-C170KGKT
JP14
R43
220R
D10
LTST-C170KGKT
JP15
U12
TPS563206DRLR
C92
C93
GRM21BC81D106ME51L
R39
100K
C95
100n
L7
IHLP1212BZEV3R3M01
R41
45K3
R42
10K
C98
10u
C99
10u
J14B J14C J14D
J17B J17C J17D
Chili.CHIPS
Sheet: /Direct PCIe/
File: direct_PCIe.kicad_sch
Title:
Size: A4
Date: 2025-01-29
Rev: r1B1
KiCad E.D.A. 8.0.8
Id: 6/6