Clock generator & Reset fanout

File: clock_gen.kicad_sch

Direct 4-lane PCIe

File: direct_PCIe.kicad_sch

RC 1-lane and 2-lane PCIE

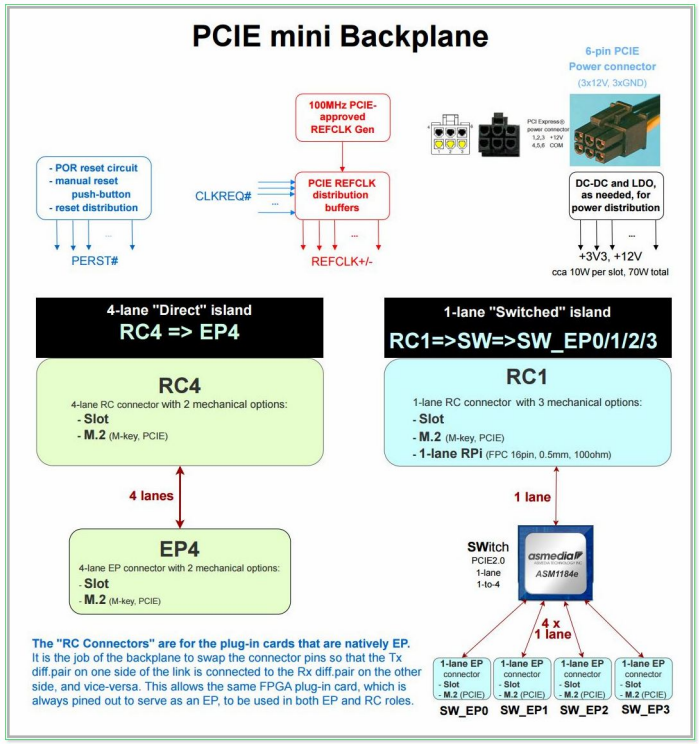
File: RC_4-lanes-PCIe.kicad_sch

Switched 4 x 1-lanes PCIe

File: 4_1-lanes_PCIe.kicad_sch

PCIe switch

File: pcie_switch.kicad_sch



H1 H2 H3 H4 H5 H6

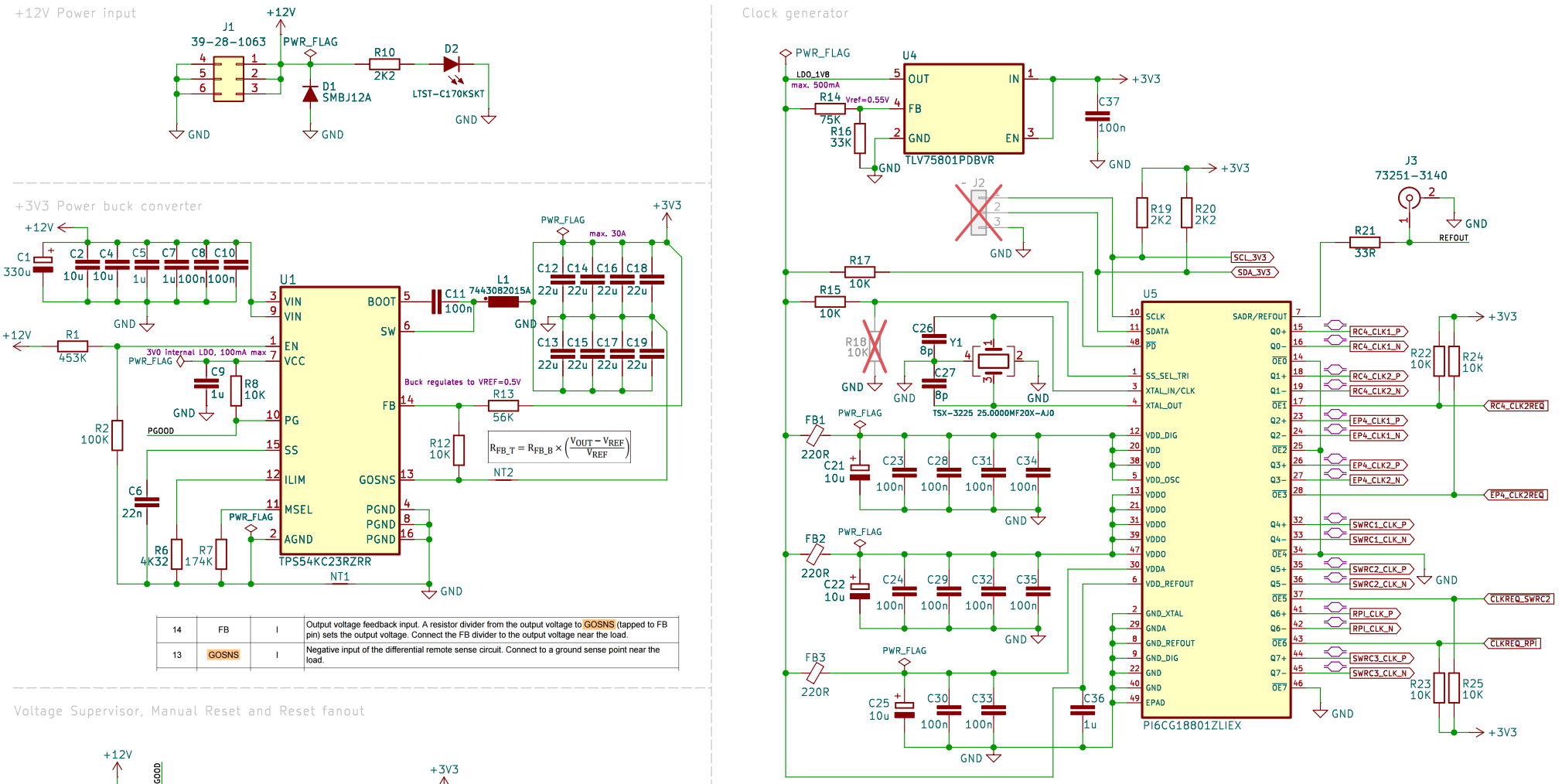
Chili.CHIPS

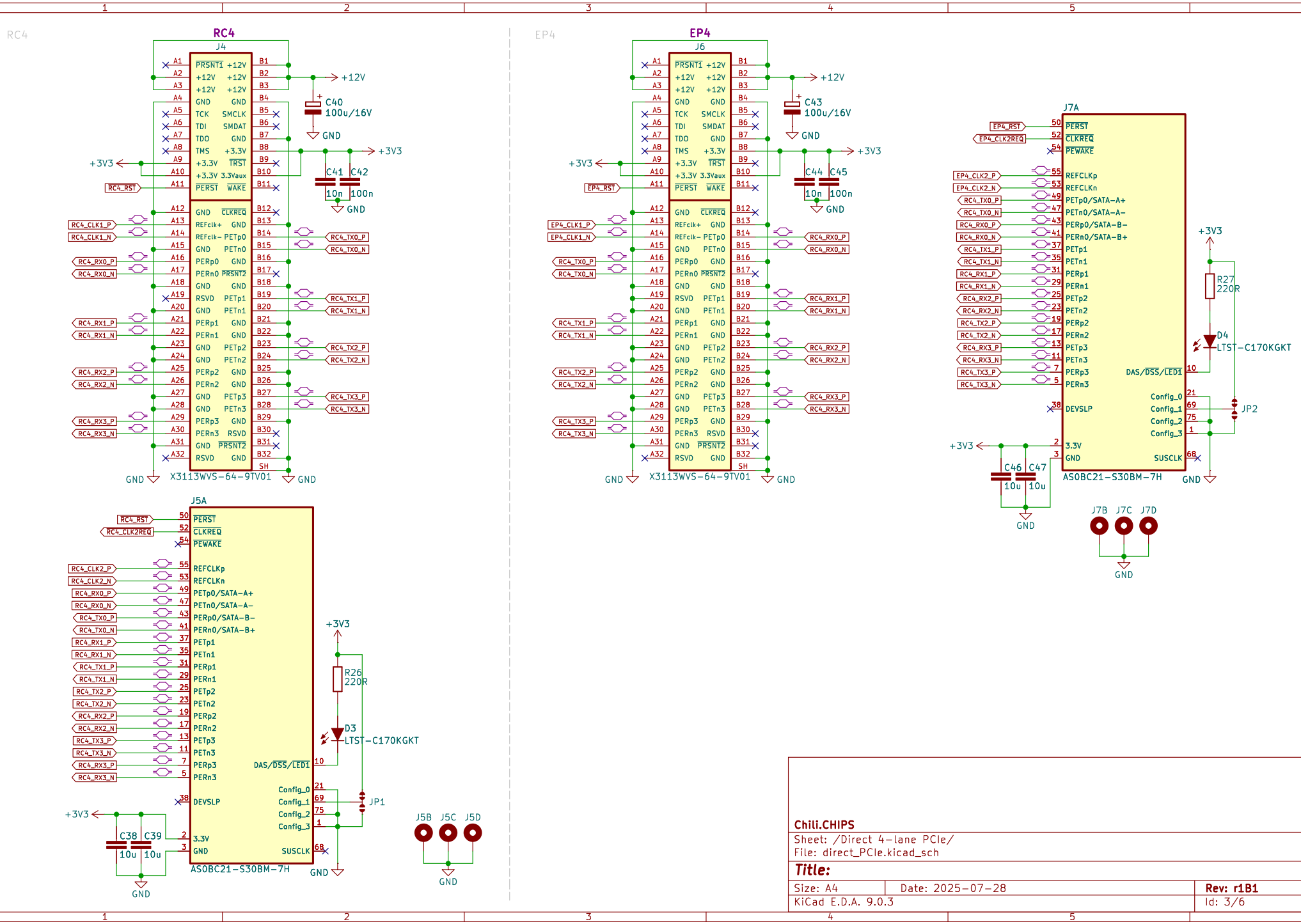
Sheet: /

File: openpci2-backplane.kicad_sch

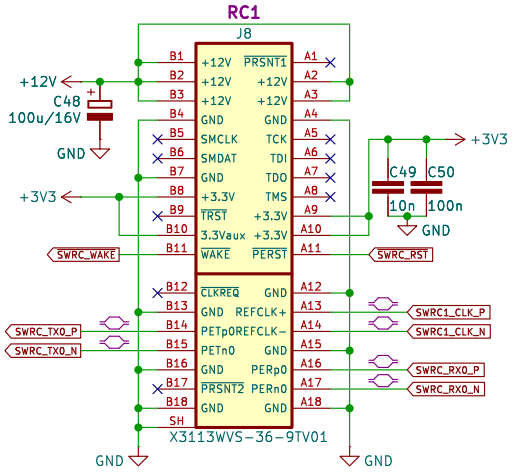
Title:

Size: A4	Date: 2025-07-28	Rev: r1B1
KiCad E.D.A. 9.0.3		Id: 1/6

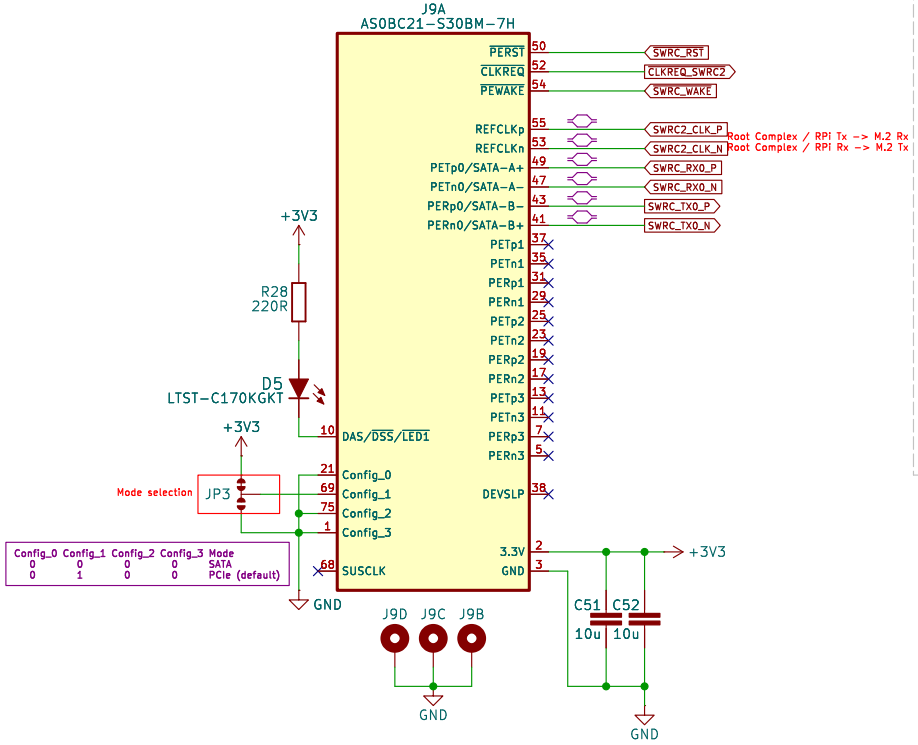

+12V Power input
J1
39-28-1063
PWR_FLAG
R10
2K2
D2
LTST-C170KSKT
D1
SMBJ12A
GND
+3V3 Power buck converter
U1
TPS54KC23RZRR
VIN
BOOT
SW
EN
VCC
FB
PG
SS
ILIM
GOSNS
MSEL
PGND
AGND
L1
7443082015A
max. 30A
3V0 internal LDO, 100mA max
Buck regulates to VREF=0.5V
PGOOD
NT1
NT2
$R_{FB\_T} = R_{FB\_B} \times \left(\frac{V_{OUT} - V_{REF}}{V_{REF}}\right)$
14 FB I Output voltage feedback input. A resistor divider from the output voltage to GOSNS (tapped to FB pin) sets the output voltage. Connect the FB divider to the output voltage near the load.
13 GOSNS I Negative input of the differential remote sense circuit. Connect to a ground sense point near the load.
Voltage Supervisor, Manual Reset and Reset fanout
U2
NCV308SNADJT1G
SENSE
MR
CT
VDD
RESET
GND
SW1
PTR645
U3
SN74LVC244APWR
RST_PCIESW
RST_PCIESW_OUT
RC4_RST
EP4_RST
SWRC_RST
SW_RST0
SW_RST1
SW_RST2
SW_RST3
Clock generator
U4
TLV75801PDBVR
LDO_1V8
max. 500mA
Vref=0.55V
U5
PI6CG18801ZLIEX
TSX-3225 25.0000MF20X-AJ0
SCL_3V3
SDA_3V3
J3
73251-3140
REFOUT
RC4_CLK1_P
RC4_CLK1_N
RC4_CLK2_P
RC4_CLK2_N
RC4_CLK2REQ
EP4_CLK1_P
EP4_CLK1_N
EP4_CLK2_P
EP4_CLK2_N
EP4_CLK2REQ
SWRC1_CLK_P
SWRC1_CLK_N
SWRC2_CLK_P
SWRC2_CLK_N
CLKREQ_SWRC2
RPI_CLK_P
RPI_CLK_N
CLKREQ_RPI
SWRC3_CLK_P
SWRC3_CLK_N
Chili.CHIPS
Sheet: /Clock generator & Reset fanout/
File: clock_gen.kicad_sch
Title:
Size: A4
Date: 2025-07-28
Rev: r1B1
KiCad E.D.A. 9.0.3
Id: 2/6


RC4
RC4
J4
X3113WVS-64-9TV01
C40
100u/16V
C41
10n
C42
100n
+12V
+3V3
GND
RC4_RST
RC4_CLK1_P
RC4_CLK1_N
RC4_RX0_P
RC4_RX0_N
RC4_TX0_P
RC4_TX0_N
RC4_RX1_P
RC4_RX1_N
RC4_TX1_P
RC4_TX1_N
RC4_RX2_P
RC4_RX2_N
RC4_TX2_P
RC4_TX2_N
RC4_RX3_P
RC4_RX3_N
RC4_TX3_P
RC4_TX3_N
EP4
J6
X3113WVS-64-9TV01
C43
100u/16V
C44
10n
C45
100n
EP4_RST
EP4_CLK1_P
EP4_CLK1_N
J7A
AS0BC21-S30BM-7H
EP4_CLK2REQ
EP4_CLK2_P
EP4_CLK2_N
EP4_TX0_P
EP4_TX0_N
EP4_RX0_P
EP4_RX0_N
EP4_TX1_P
EP4_TX1_N
EP4_RX1_P
EP4_RX1_N
EP4_TX2_P
EP4_TX2_N
EP4_RX2_P
EP4_RX2_N
EP4_TX3_P
EP4_TX3_N
R27
220R
D4
LTST-C170KGKT
JP2
C46
10u
C47
10u
J7B
J7C
J7D
J5A
AS0BC21-S30BM-7H
R26
220R
D3
LTST-C170KGKT
JP1
C38
10u
C39
10u
J5B
J5C
J5D
Chili.CHIPS
Sheet: /Direct 4-lane PCIe/
File: direct_PCIe.kicad_sch
Title:
Size: A4
Date: 2025-07-28
Rev: r1B1
KiCad E.D.A. 9.0.3
Id: 3/6

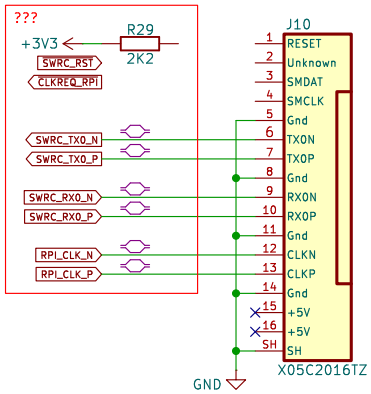
1-lane PCIe for Root Complex



1-lane M.2 (Type M) for Root Complex



Raspberry Pi FPC 16-pin connector



2.1. PCIe Signals

The PCIe signals are a single lane of PCIe Gen 2, including CLKREQ and RST_B sideband signals which operate at 3.3V.

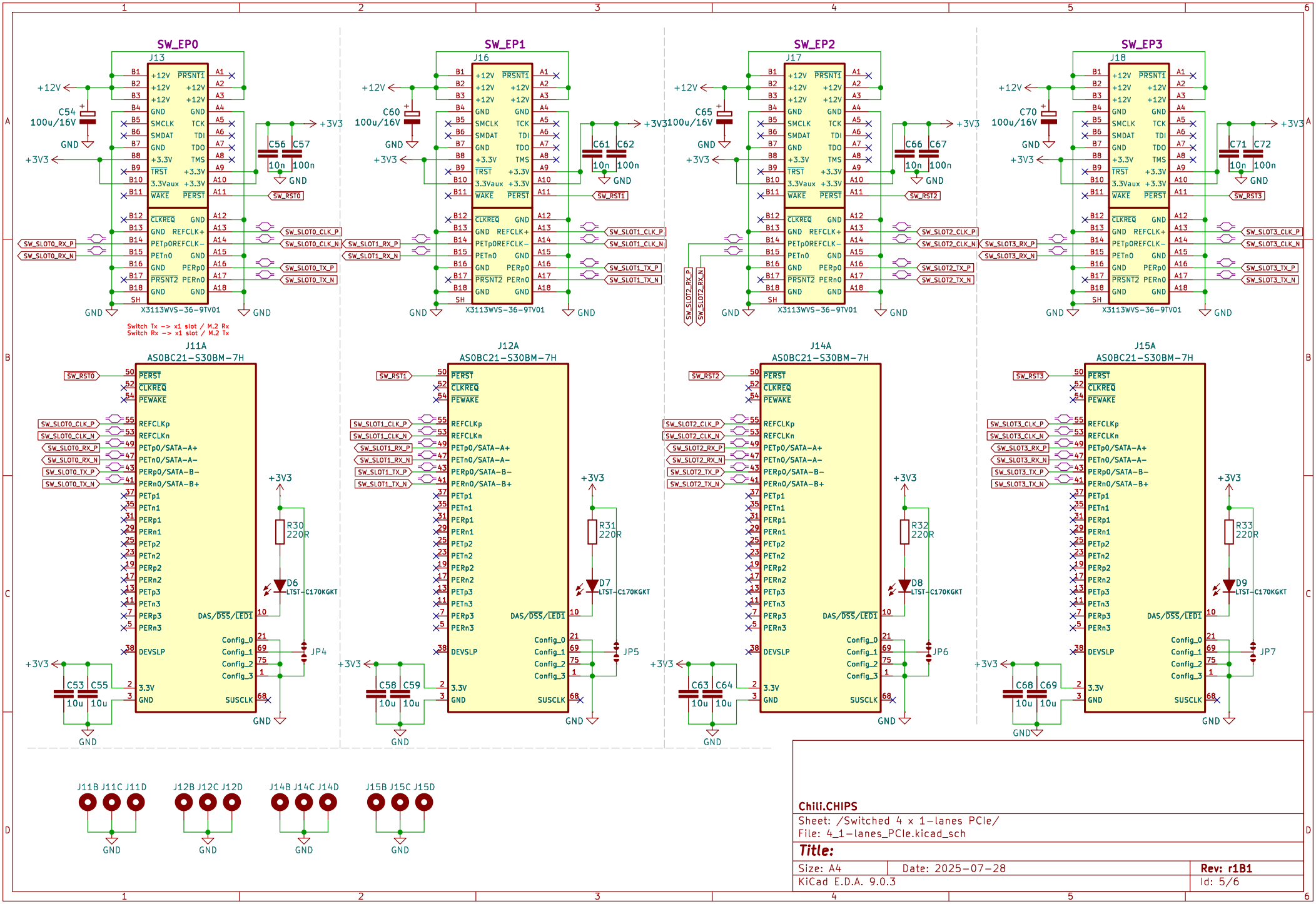
2.1.1. Pwr_en pin

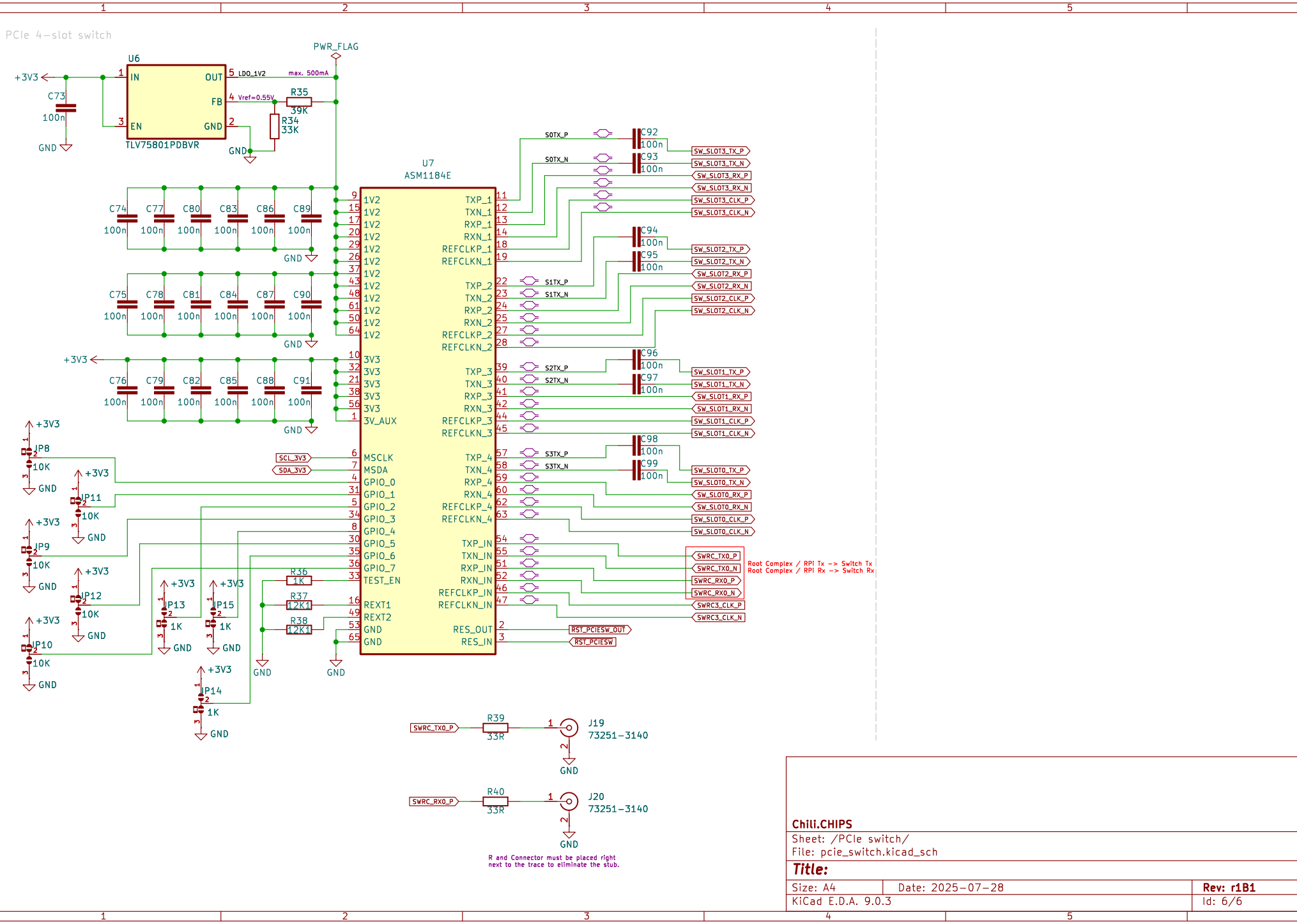
This pin is a 3.3V output from the Raspberry PI to a HAT+ or other add-on board, and signals to the HAT+ to power up any supplies. For example, in the instance of the Raspberry PI M.2 M Key HAT+, this enables the M.2 3.3V power (which is generated from the incoming 5V). Provide a 100K low pull on this pin on any HAT+.

2.1.2. Det_wake pin

This pin is a 3.3V input to the Raspberry PI. Pull high to 3.3V either from a resistive divider from 5V (3k6/6k8 giving 2.35k output impedance), or from permanently enabled 3.3V (using a 2.2K resistor).
The Raspberry PI will detect this high pull at boot time, and will automatically probe the PCIe bus.
Use the PCIe WAKE# to pull this low

Chili.CHIPS		
Sheet: /RC 1-lane and 2-lane PCIE/		
File: RC_4-lanes-PCIe.kicad_sch		
Title:		
Size: A4	Date: 2025-07-28	**Rev: r1B1**
KiCad E.D.A. 9.0.3		Id: 4/6


SW_EP0
SW_EP1
SW_EP2
SW_EP3
X3113WVS-36-9TV01
Switch Tx -> x1 slot / M.2 Rx
Switch Rx -> x1 slot / M.2 Tx
J11A
J12A
J14A
J15A
AS0BC21-S30BM-7H
J11B J11C J11D
J12B J12C J12D
J14B J14C J14D
J15B J15C J15D
Chili.CHIPS
Sheet: /Switched 4 x 1-lanes PCIe/
File: 4_1-lanes_PCIe.kicad_sch
Title:
Size: A4
Date: 2025-07-28
Rev: r1B1
KiCad E.D.A. 9.0.3
Id: 5/6


PCIe 4-slot switch
PWR_FLAG
U6
TLV75801PDBVR
+3V3
GND
C73
100n
R35
39K
R34
33K
LDO_1V2
max. 500mA
Vref=0.55V
U7
ASM1184E
1V2
3V3
3V_AUX
MSCLK
MSDA
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
TEST_EN
REXT1
REXT2
RES_OUT
RES_IN
TXP_1
TXN_1
RXP_1
RXN_1
REFCLKP_1
REFCLKN_1
TXP_2
TXN_2
RXP_2
RXN_2
REFCLKP_2
REFCLKN_2
TXP_3
TXN_3
RXP_3
RXN_3
REFCLKP_3
REFCLKN_3
TXP_4
TXN_4
RXP_4
RXN_4
REFCLKP_4
REFCLKN_4
TXP_IN
TXN_IN
RXP_IN
RXN_IN
REFCLKP_IN
REFCLKN_IN
S0TX_P
S0TX_N
S1TX_P
S1TX_N
S2TX_P
S2TX_N
S3TX_P
S3TX_N
SCL_3V3
SDA_3V3
SW_SLOT3_TX_P
SW_SLOT3_TX_N
SW_SLOT3_RX_P
SW_SLOT3_RX_N
SW_SLOT3_CLK_P
SW_SLOT3_CLK_N
SW_SLOT2_TX_P
SW_SLOT2_TX_N
SW_SLOT2_RX_P
SW_SLOT2_RX_N
SW_SLOT2_CLK_P
SW_SLOT2_CLK_N
SW_SLOT1_TX_P
SW_SLOT1_TX_N
SW_SLOT1_RX_P
SW_SLOT1_RX_N
SW_SLOT1_CLK_P
SW_SLOT1_CLK_N
SW_SLOT0_TX_P
SW_SLOT0_TX_N
SW_SLOT0_RX_P
SW_SLOT0_RX_N
SW_SLOT0_CLK_P
SW_SLOT0_CLK_N
SWRC_TX0_P
SWRC_TX0_N
SWRC_RX0_P
SWRC_RX0_N
SWRC3_CLK_P
SWRC3_CLK_N
Root Complex / RPI Tx -> Switch Tx
Root Complex / RPI Rx -> Switch Rx
RST_PCIESW_OUT
RST_PCIESW
JP8
JP9
JP10
JP11
JP12
JP13
JP14
JP15
10K
1K
R36
R37
R38
12K1
R39
R40
33R
J19
J20
73251-3140
R and Connector must be placed right
next to the trace to eliminate the stub.
Chili.CHIPS
Sheet: /PCIe switch/
File: pcie_switch.kicad_sch
Title:
Size: A4
Date: 2025-07-28
Rev: r1B1
KiCad E.D.A. 9.0.3
Id: 6/6