Clock generator & Reset fanout

File: clock_gen.kicad_sch

Switched 4 x 1-lanes PCIe

File: 4_1-lanes_PCIe.kicad_sch

RC 1-lane and 2-lane PCIE

File: RC_4-lanes-PCIe.kicad_sch

PCIe switch

File: pcie_switch.kicad_sch

Direct 4-lane PCIe

File: direct_PCIe.kicad_sch

H1 H2 H3 H4 H5 H6

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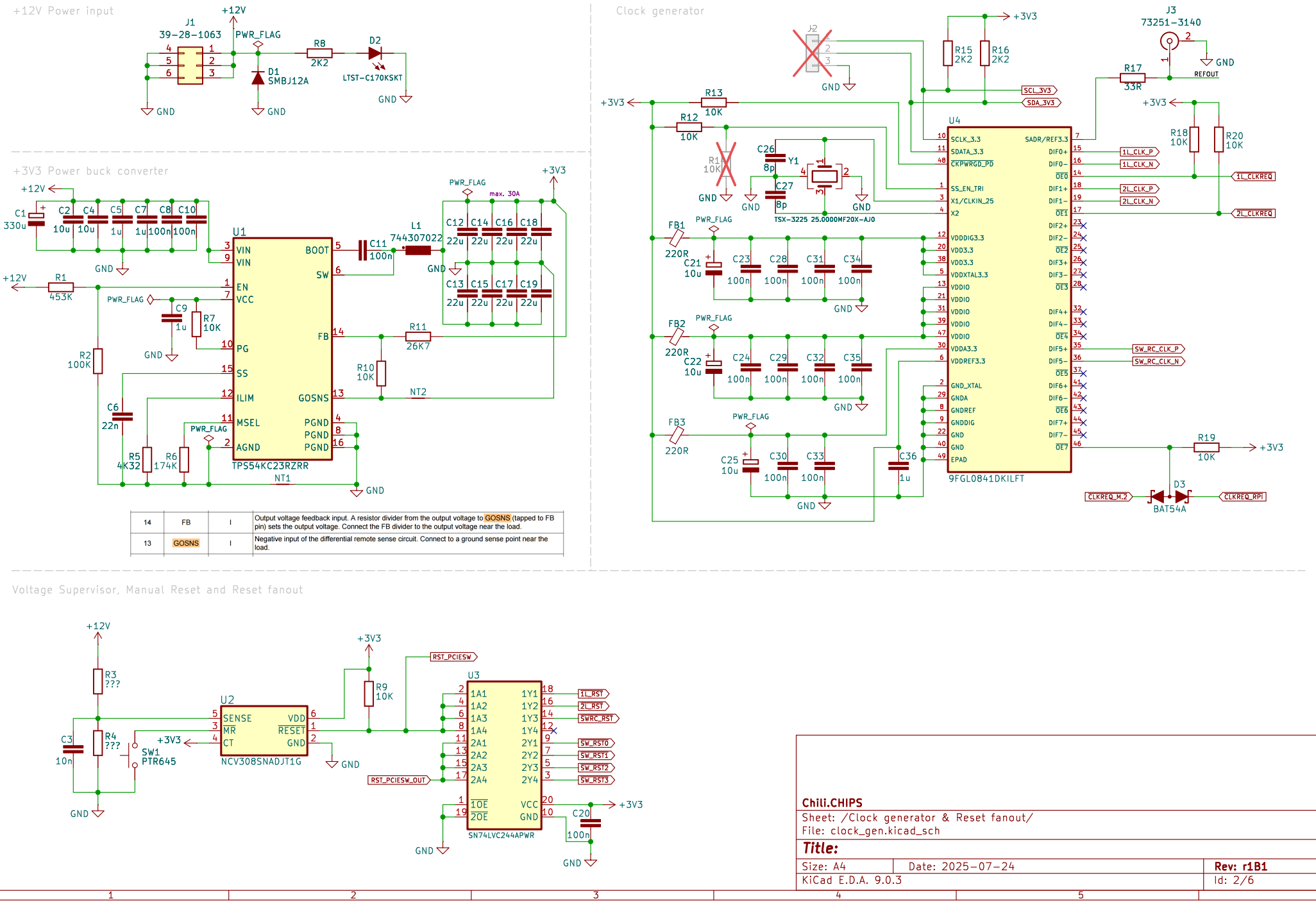
Sheet: /

File: openpci2-backplane.kicad_sch

Title:

Size: A4	Date: 2025-07-24	Rev: r1B1
KiCad E.D.A. 9.0.3		Id: 1/6



14	FB	I	Output voltage feedback input. A resistor divider from the output voltage to GOSNS (tapped to FB pin) sets the output voltage. Connect the FB divider to the output voltage near the load.
13	GOSNS	I	Negative input of the differential remote sense circuit. Connect to a ground sense point near the load.

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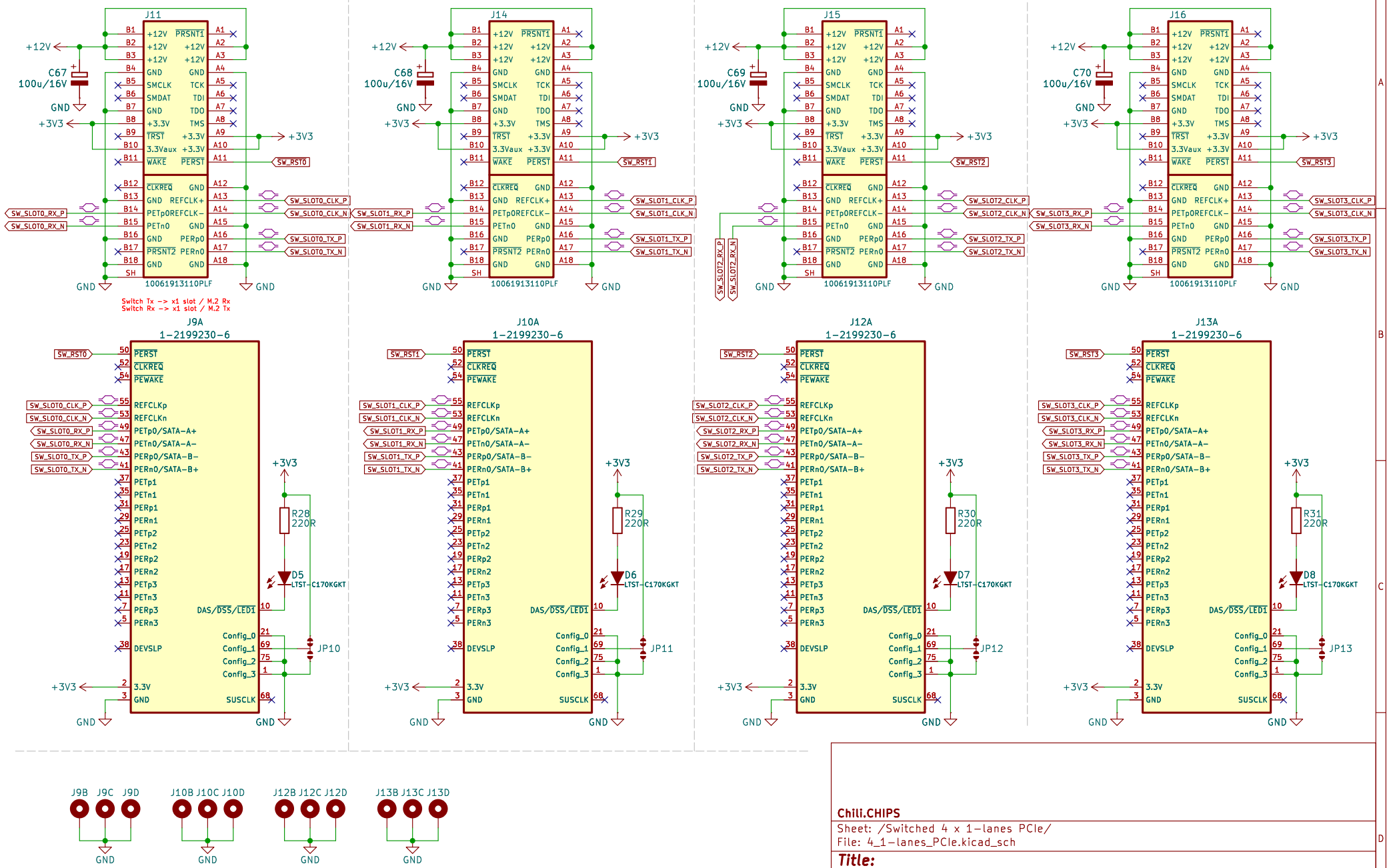
Sheet: /Clock generator & Reset fanout/

File: clock_gen.kicad_sch

Title:

Size: A4	Date: 2025-07-24	**Rev: r1B1**
KiCad E.D.A. 9.0.3		Id: 2/6



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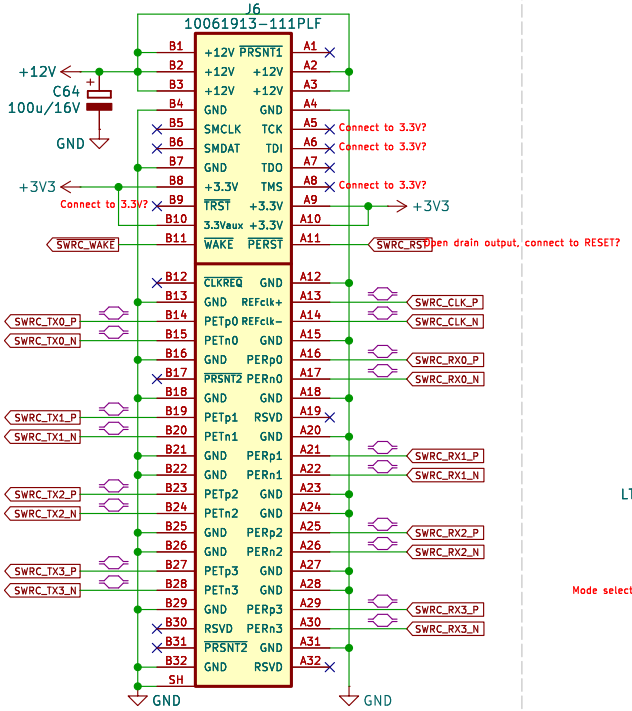
Sheet: /Switched 4 x 1-lanes PCIe/

File: 4_1-lanes_PCIe.kicad_sch

Title:

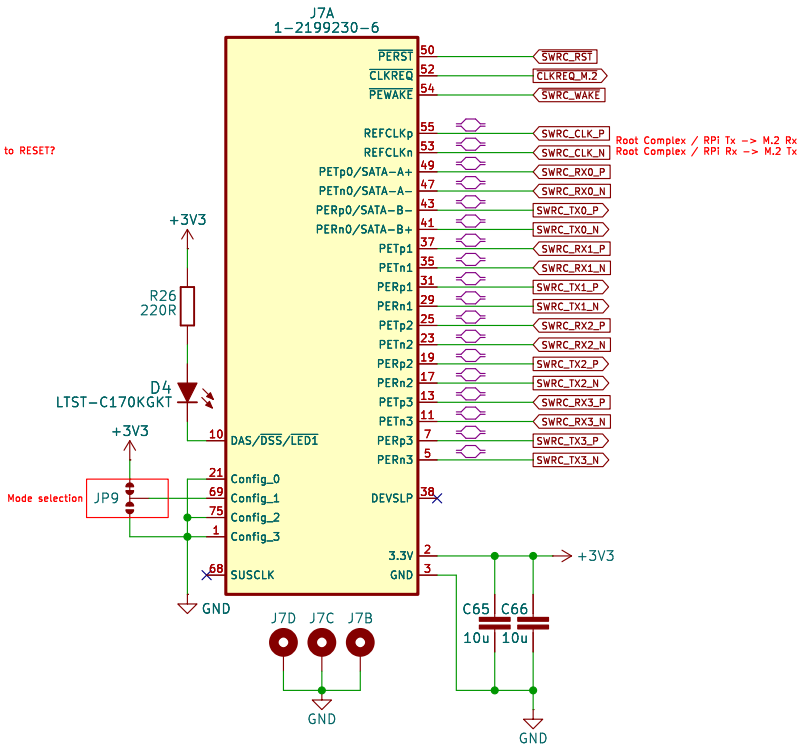
Size: A4	Date: 2025-07-24	**Rev: r1B1**
KiCad E.D.A. 9.0.3		Id: 5/6

4-lane PCIe for Root Complex

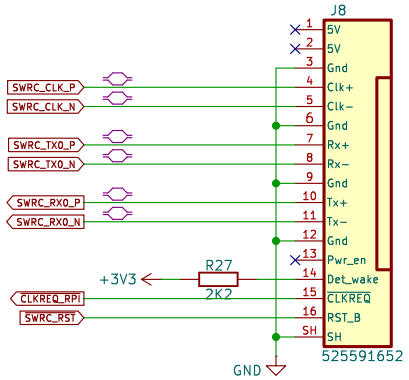


Lanes #	Device
0	PCIe switch for 4 x 1-lanes + 4 x M.2
1	1-lanes slot + M.2
2	2-lanes slot + M.2 (First)
3	2-lanes slot + M.2 (Second)

4-lane M.2 (Type M) for Root Complex



Raspberry Pi FPC 16-pin connector



2.1. PCIe Signals

The PCIe signals are a single lane of PCIe Gen 2, including CLKREQ and RST_B sideband signals which operate at 3.3V.

2.1.1. Pwr_en pin

This pin is a 3.3V output from the Raspberry PI to a HAT+ or other add-on board, and signals to the HAT+ to power up any supplies. For example, in the Instance of the Raspberry PI M.2 M Key HAT+, this enables the M.2 3.3V power (which is generated from the incoming 5V). Provide a 100K low pull on this pin on any HAT+.

2.1.2. Det_wake pin

This pin is a 3.3V input to the Raspberry PI. Pull high to 3.3V either from a resistive divider from 5V (3k6/6k8 giving 2.35k output impedance), or from permanently enabled 3.3V (using a 2.2K resistor).
The Raspberry PI will detect this high pull at boot time, and will automatically probe the PCIe bus.
Use the PCIe WAKE# to pull this low

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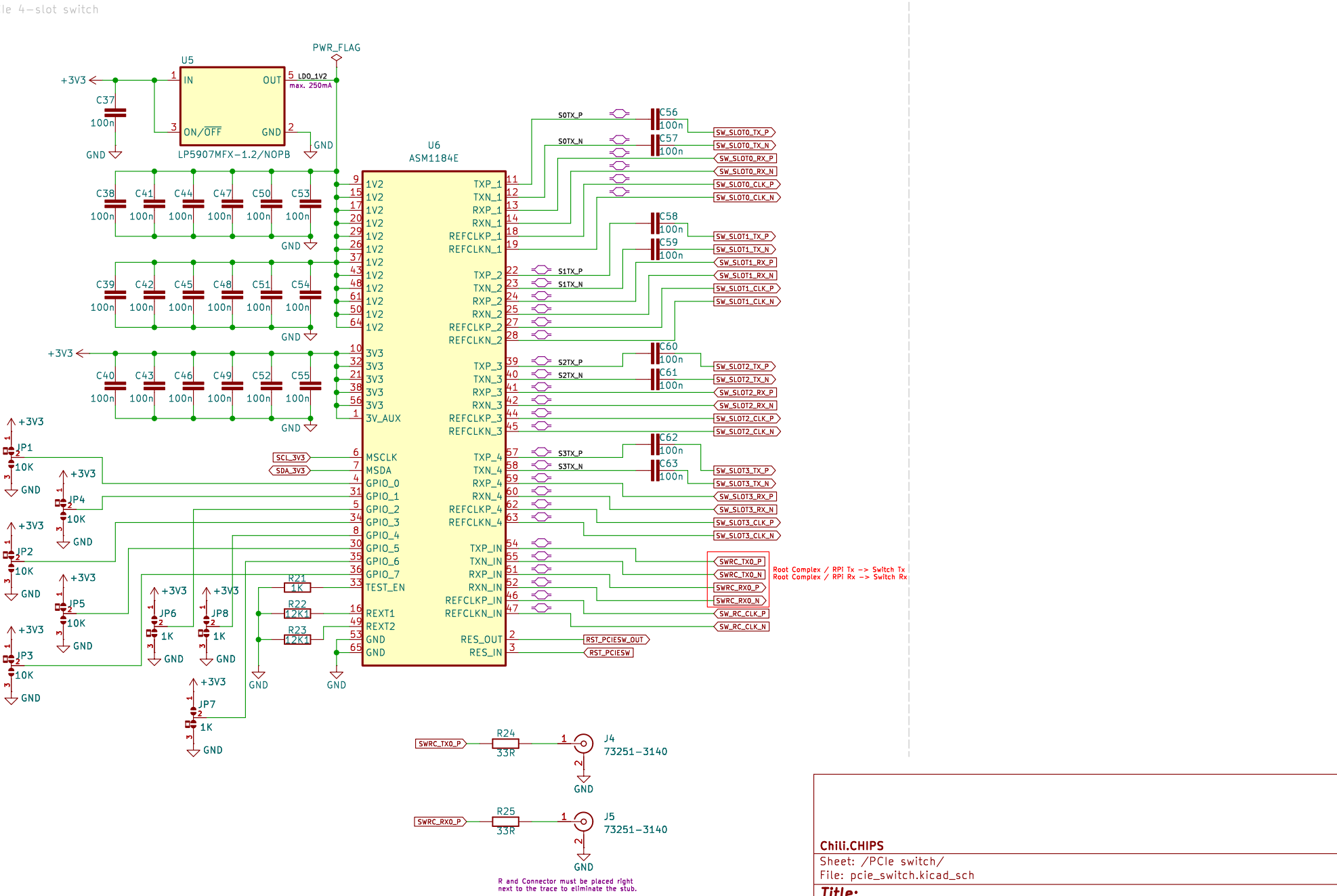
Sheet: /RC 1-lane and 2-lane PCIE/
File: RC_4-lanes-PCIe.kicad_sch

Title:

Size: A4	Date: 2025-07-24	**Rev: r1B1**
KiCad E.D.A. 9.0.3		Id: 4/6


PCIe 4-slot switch
PWR_FLAG
U5
LP5907MFX-1.2/NOPB
LDO_1V2
max. 250mA
U6
ASM1184E
Root Complex / RPI Tx -> Switch Tx
Root Complex / RPI Rx -> Switch Rx
R and Connector must be placed right
next to the trace to eliminate the stub.
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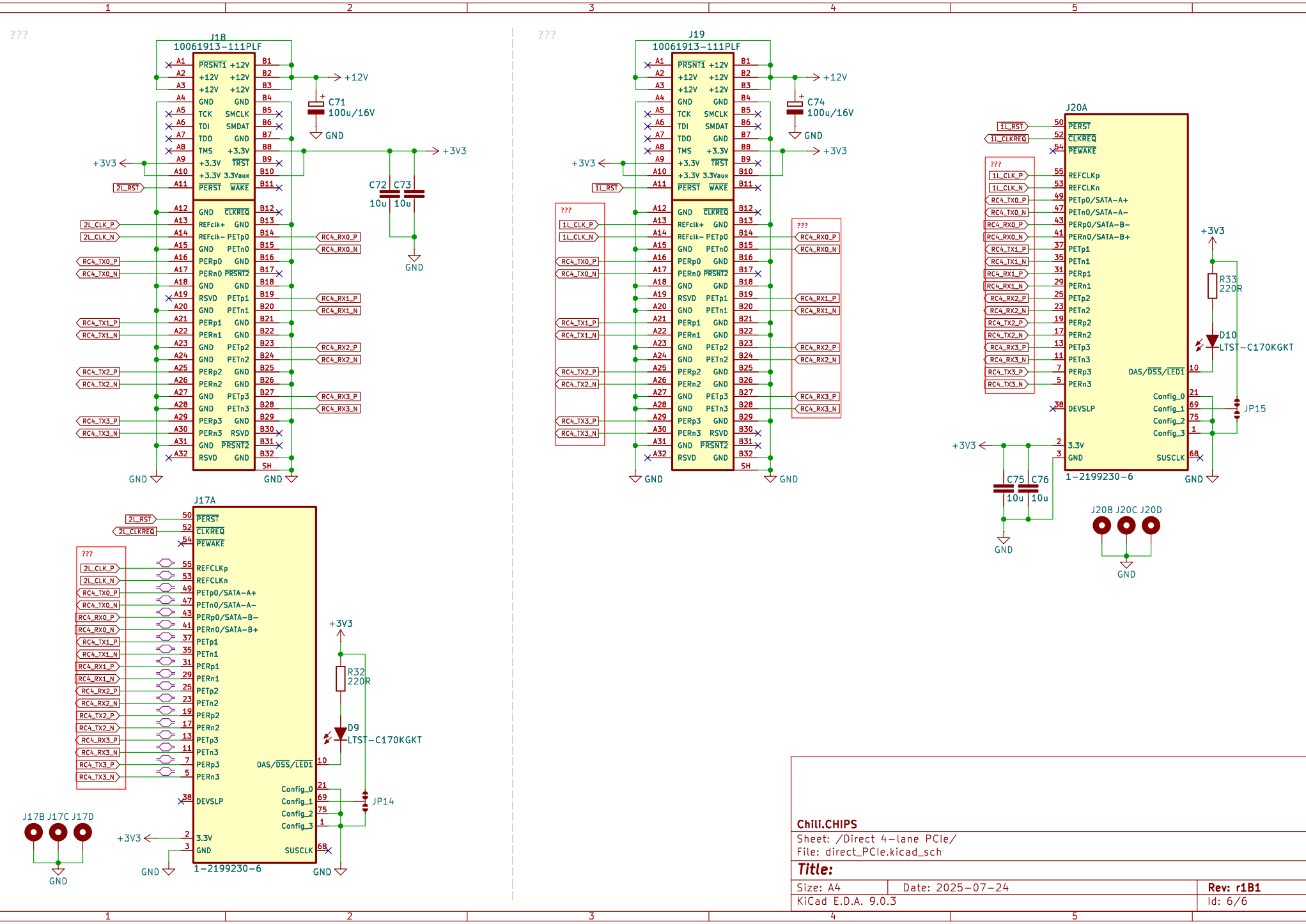
Sheet: /PCIe switch/
File: pcie_switch.kicad_sch
Title:
Size: A4
Date: 2025-07-24
Rev: r1B1
KiCad E.D.A. 9.0.3
Id: 3/6


J18
10061913-111PLF
J19
10061913-111PLF
J17A
1-2199230-6
J20A
1-2199230-6
J17B J17C J17D
J20B J20C J20D
C71
100u/16V
C74
100u/16V
C72 C73
10u 10u
C75 C76
10u 10u
R32
220R
R33
220R
D9
LTST-C170KGKT
D10
LTST-C170KGKT
JP14
JP15
+12V
+3V3
GND
2L_RST
2L_CLKREQ
2L_CLK_P
2L_CLK_N
1L_RST
1L_CLKREQ
1L_CLK_P
1L_CLK_N
RC4_TX0_P
RC4_TX0_N
RC4_RX0_P
RC4_RX0_N
RC4_TX1_P
RC4_TX1_N
RC4_RX1_P
RC4_RX1_N
RC4_TX2_P
RC4_TX2_N
RC4_RX2_P
RC4_RX2_N
RC4_TX3_P
RC4_TX3_N
RC4_RX3_P
RC4_RX3_N
PERST
CLKREQ
PEWAKE
REFCLKp
REFCLKn
PETp0/SATA-A+
PETn0/SATA-A-
PERp0/SATA-B-
PERn0/SATA-B+
PETp1
PETn1
PERp1
PERn1
PETp2
PETn2
PERp2
PERn2
PETp3
PETn3
PERp3
PERn3
DEVSLP
DAS/DSS/LED1
Config_0
Config_1
Config_2
Config_3
3.3V
SUSCLK
Chili.CHIPS
Sheet: /Direct 4-lane PCIe/
File: direct_PCIe.kicad_sch
Title:
Size: A4
Date: 2025-07-24
Rev: r1B1
KiCad E.D.A. 9.0.3
Id: 6/6