Clock generator & Reset fanout

File: clock_gen.kicad_sch

Direct 4-lane PCIe

File: direct_PCIe.kicad_sch

RC 1-lane and 2-lane PCIE

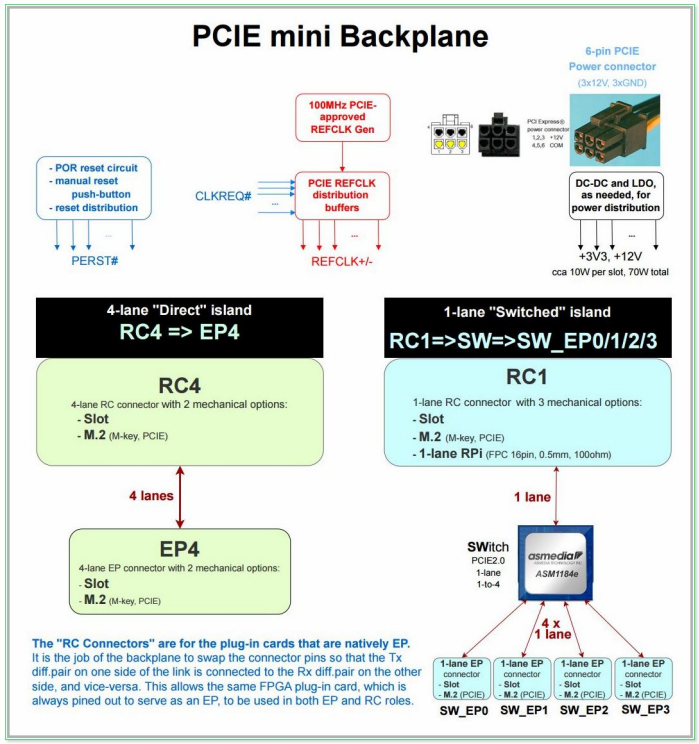
File: RC_4-lanes-PCIe.kicad_sch

PCIe switch

File: pcie_switch.kicad_sch

Switched 4 x 1-lanes PCIe

File: 4_1-lanes_PCIe.kicad_sch



H1 H2 H3 H4 H5 H6

Chili.CHIPS

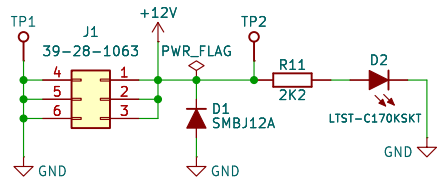
Sheet: /

File: openpci2-backplane.kicad_sch

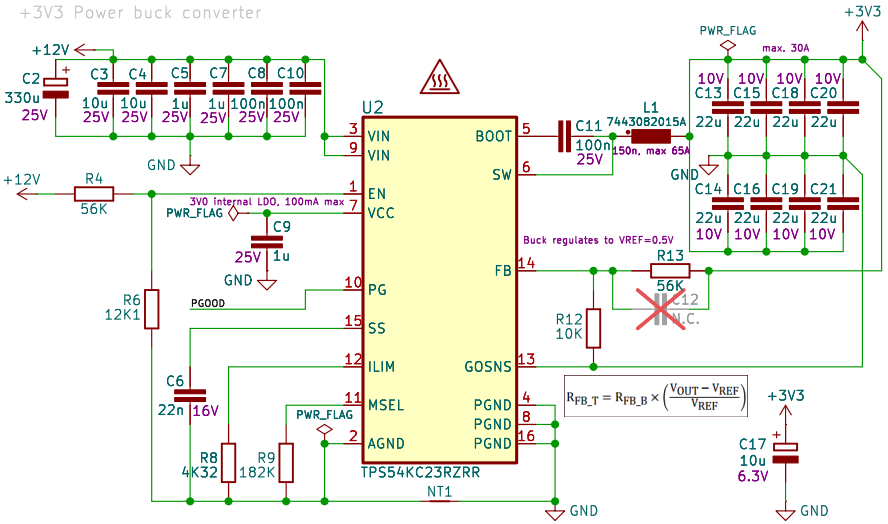
Title:

Size: A4	Date: 2025-10-20	Rev: r1B1
KiCad E.D.A. 9.0.5		Id: 1/6

+12V Power input



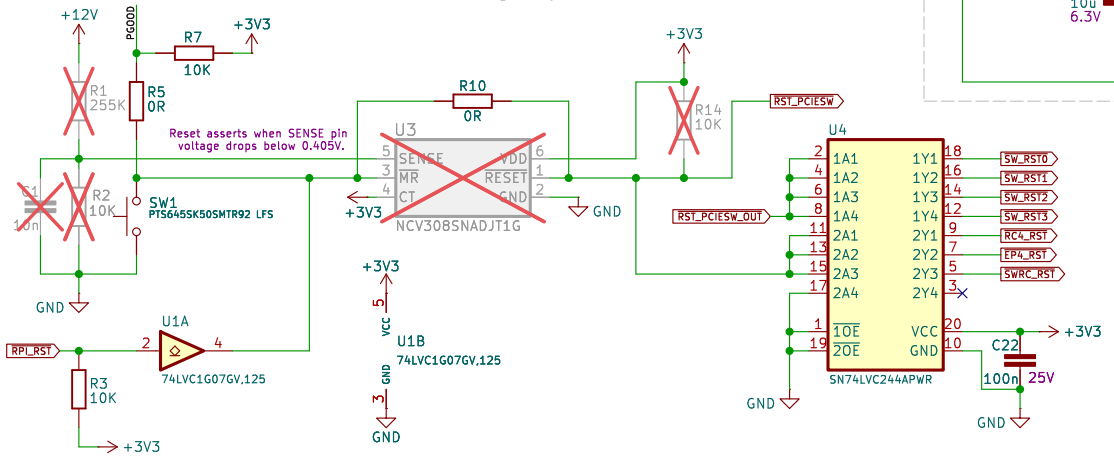
+3V3 Power buck converter



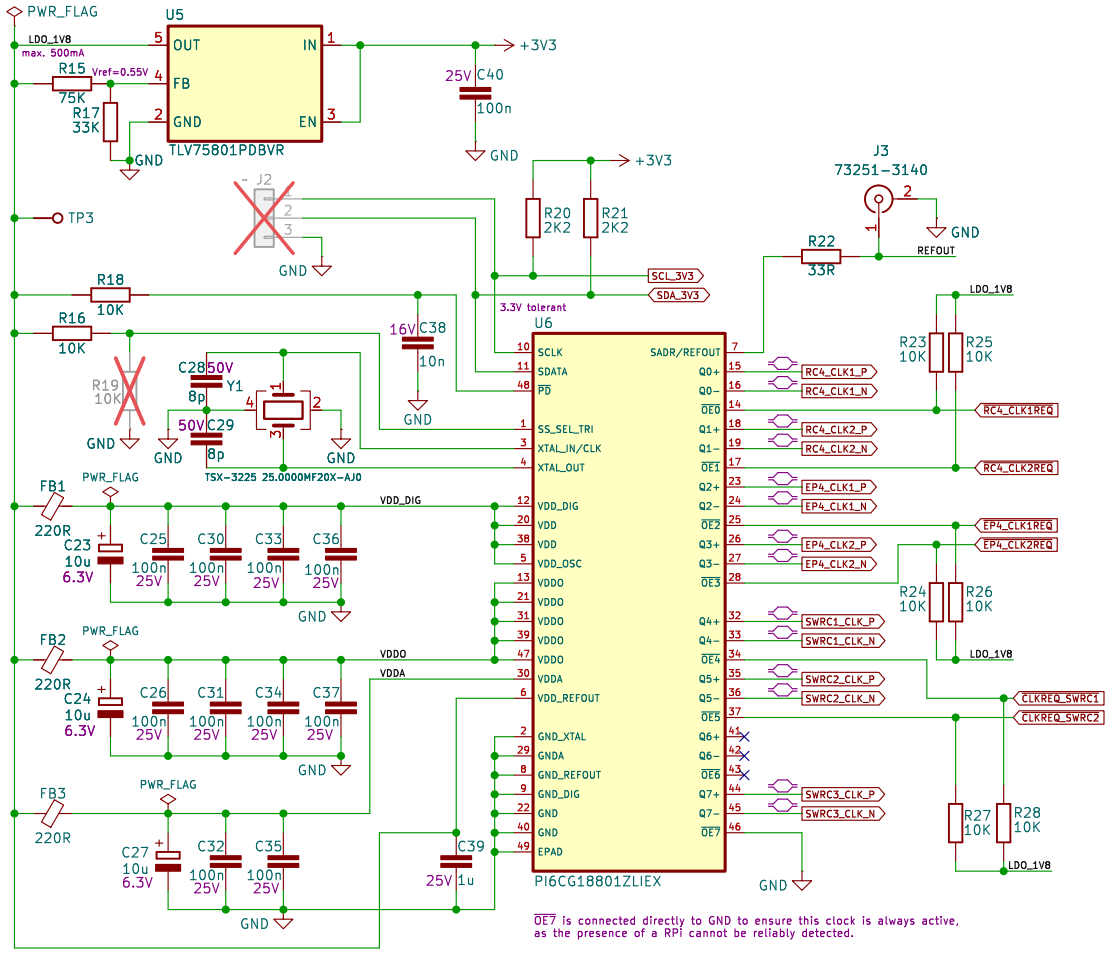
14	FB	I	Output voltage feedback input. A resistor divider from the output voltage to GOSNS (tapped to FB pin) sets the output voltage. Connect the FB divider to the output voltage near the load.
13	GOSNS	I	Negative input of the differential remote sense circuit. Connect to a ground sense point near the load.

Voltage Supervisor, Manual Reset and Reset fanout

Reset asserts when +12V input drops below ~10.73V.



Clock generator



OE7 is connected directly to GND to ensure this clock is always active, as the presence of a RPi cannot be reliably detected.

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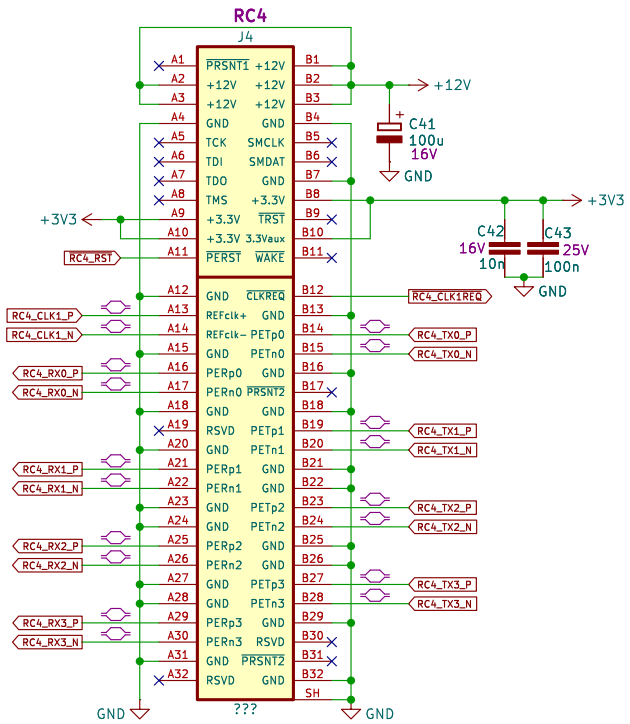
Sheet: /Clock generator & Reset fanout/
File: clock_gen.kicad_sch

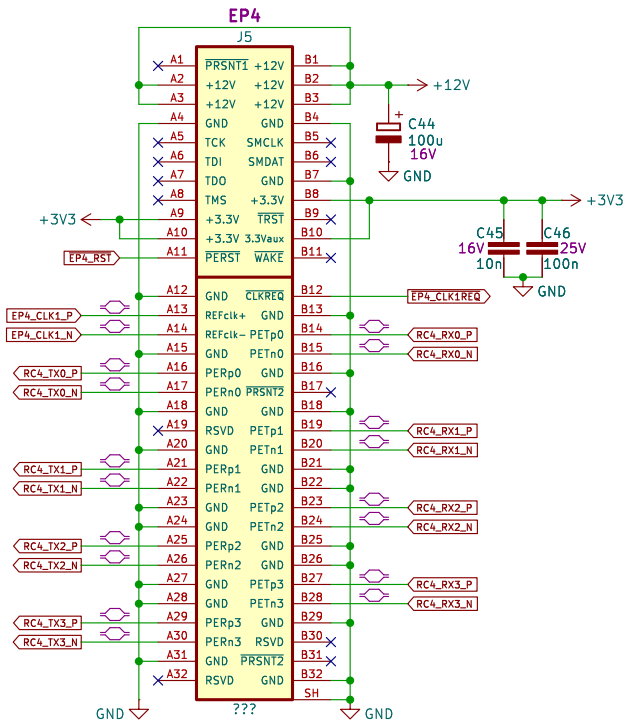
Title:

Size: A4	Date: 2025-10-20	**Rev: r1B1**
KiCad E.D.A. 9.0.5		Id: 2/6

RC4



EP4



PCIEx1 pinout

Pin	Side B	Side A	Description
1	+12 V	~~PRSNT1#~~	Must connect to farthest PRSNT2# pin
2	+12 V	+12 V	Main power pins
3	+12 V	+12 V	
4	Ground	Ground	
5	~~SMCLK~~	~~TCK~~	SMBus and JTAG port pins
6	~~SMDAT~~	~~TDI~~	
7	Ground	~~TDO~~	
8	+3.3 V	~~TMS~~	
9	~~TRST#~~	+3.3 V	
10	+3.3 V aux	+3.3 V	Aux power & Standby power
11	~~WAKE#~~	PERST#	Link reactivation; fundamental reset [25]
	Key notch		
12	CLKREQ#[25]	Ground	Clock Request Signal
13	Ground	REFCLK+	Reference clock differential pair
14	HSOp(0)	REFCLK–	Lane 0 transmit data, + and –
15	HSOn(0)	Ground	
16	Ground	HSIp(0)	Lane 0 receive data, + and –
17	~~PRSNT2#~~	HSIn(0)	
18	Ground	Ground	
PCI Express x1 cards end at pin 18			

Legend	
Ground pin	Zero volt reference
Power pin	Supplies power to the PCIe card
Card-to-host pin	Signal from the card to the motherboard
Host-to-card pin	Signal from the motherboard to the card
Open drain	May be pulled low or sensed by multiple cards
Sense pin	Tied together on card
Reserved	Not presently used, do not connect

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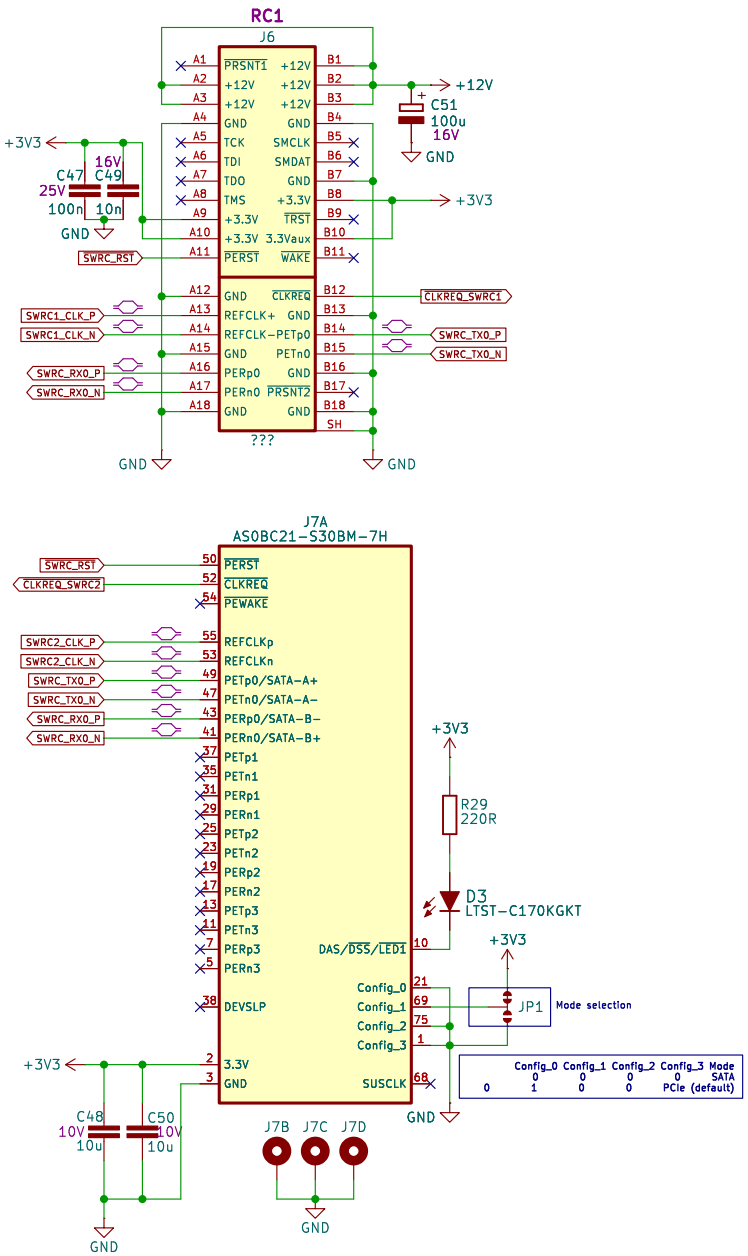
Sheet: /Direct 4–lane PCIe/

File: direct_PCIe.kicad_sch

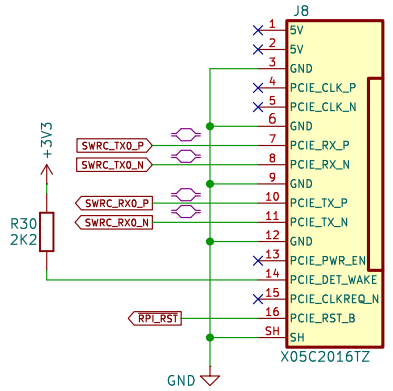
Title:

Size: A4	Date: 2025–10–20	**Rev: r1B1**
KiCad E.D.A. 9.0.5		Id: 3/6

1-lane PCIe for Root Complex



Raspberry PI FPC 16-pin connector



As the Root Complex, the Raspberry PI provides its own reference clock. The rest of the backplane does not need this clock, as all downstream PCIe devices receive their reference clock from the onboard generator (U5).

PCIE_RST_B (pin 16) is an active-low output from the Raspberry PI, serving as the master reset for the downstream PCIe fabric.
This PCIE_RST_B signal is intended to be combined with the board's own reset sources through external logic to generate the final system reset.

2.1. PCIe Signals

The PCIe signals are a single lane of PCIe Gen 2, including CLKREQ and RST_B sideband signals which operate at 3.3V.

2.1.1. Pwr_en pin

This pin is a 3.3V output from the Raspberry PI to a HAT+ or other add-on board, and signals to the HAT+ to power up any supplies. For example, in the instance of the Raspberry PI M.2 M Key HAT+, this enables the M.2 3.3V power (which is generated from the incoming 5V). Provide a 100K low pull on this pin on any HAT+.

2.1.2. Det_wake pin

This pin is a 3.3V input to the Raspberry PI. Pull high to 3.3V either from a resistive divider from 5V (3k6/6k8 giving 2.35k output impedance), or from permanently enabled 3.3V (using a 2.2K resistor).
The Raspberry PI will detect this high pull at boot time, and will automatically probe the PCIe bus.
Use the PCIe WAKE# to pull this low

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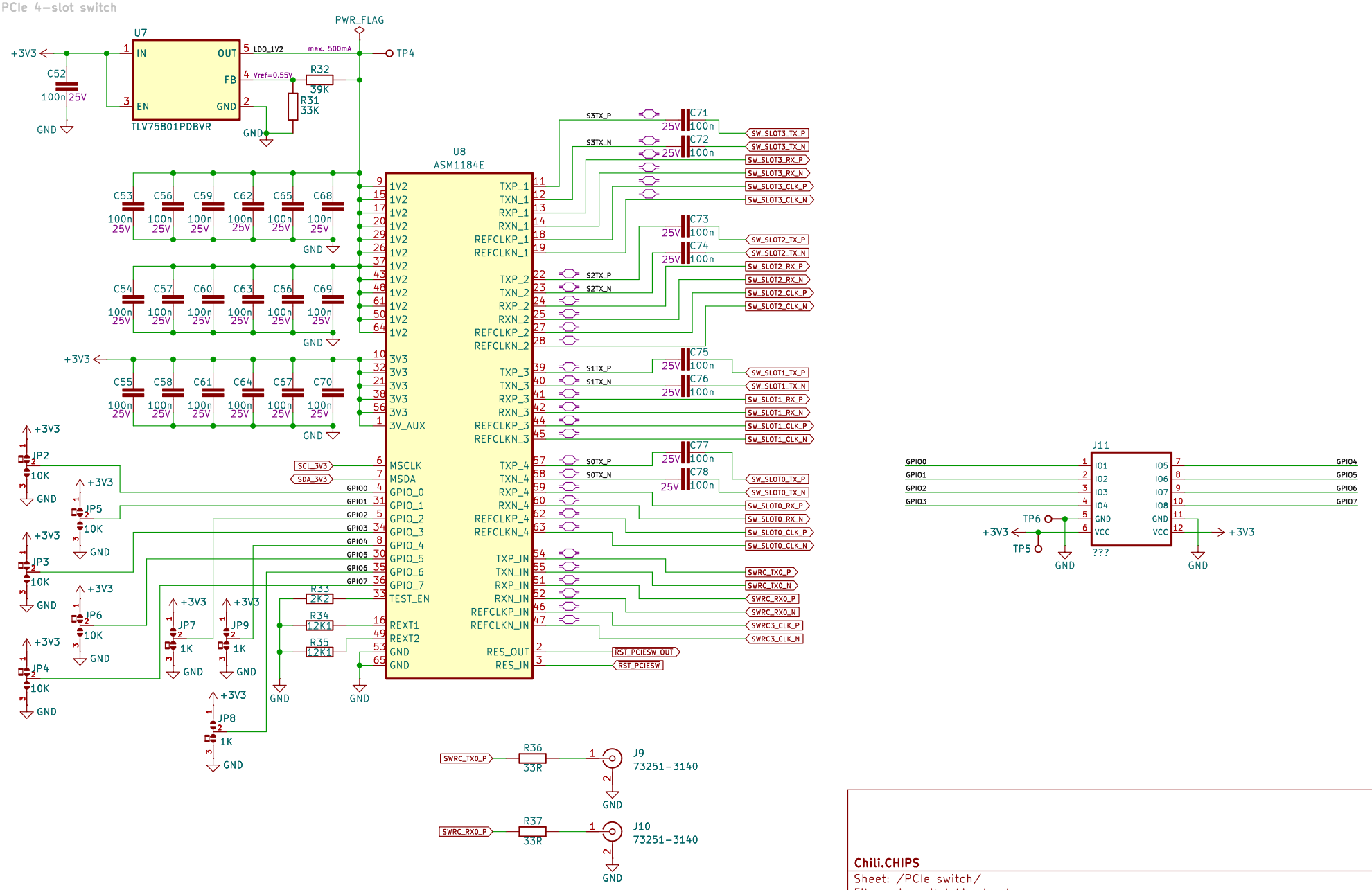
Sheet: /RC 1-lane and 2-lane PCIE/
File: RC_4-lanes-PCIe.kicad_sch

Title:

Size: A4	Date: 2025-10-20	**Rev: r1B1**
KiCad E.D.A. 9.0.5		Id: 4/6

PCIe 4-slot switch



R and Connector must be placed right next to the trace to eliminate the stub.

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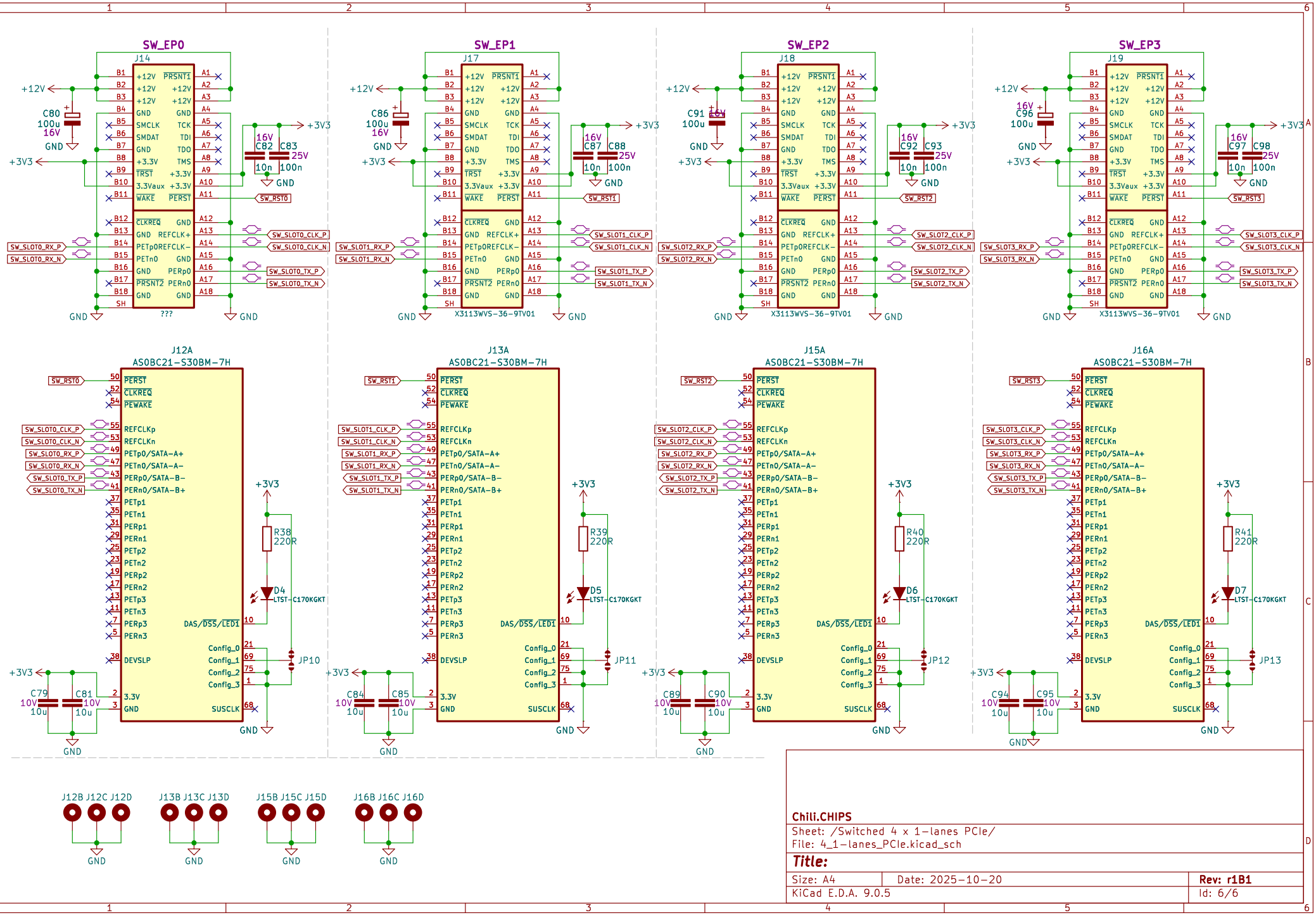
Sheet: /PCIe switch/

File: pcie_switch.kicad_sch

Title:

Size: A4	Date: 2025-10-20	**Rev: r1B1**
KiCad E.D.A. 9.0.5		Id: 5/6


SW_EP0
SW_EP1
SW_EP2
SW_EP3
J14
J17
J18
J19
X3113WVS-36-9TV01
J12A
J13A
J15A
J16A
AS0BC21-S30BM-7H
+12V
+3V3
GND
SW_RST0
SW_RST1
SW_RST2
SW_RST3
SW_SLOT0_CLK_P
SW_SLOT0_CLK_N
SW_SLOT0_RX_P
SW_SLOT0_RX_N
SW_SLOT0_TX_P
SW_SLOT0_TX_N
SW_SLOT1_CLK_P
SW_SLOT1_CLK_N
SW_SLOT1_RX_P
SW_SLOT1_RX_N
SW_SLOT1_TX_P
SW_SLOT1_TX_N
SW_SLOT2_CLK_P
SW_SLOT2_CLK_N
SW_SLOT2_RX_P
SW_SLOT2_RX_N
SW_SLOT2_TX_P
SW_SLOT2_TX_N
SW_SLOT3_CLK_P
SW_SLOT3_CLK_N
SW_SLOT3_RX_P
SW_SLOT3_RX_N
SW_SLOT3_TX_P
SW_SLOT3_TX_N
R38 220R
R39 220R
R40 220R
R41 220R
D4 LTST-C170KGKT
D5 LTST-C170KGKT
D6 LTST-C170KGKT
D7 LTST-C170KGKT
JP10
JP11
JP12
JP13
J12B J12C J12D
J13B J13C J13D
J15B J15C J15D
J16B J16C J16D
Chili.CHIPS
Sheet: /Switched 4 x 1-lanes PCIe/
File: 4_1-lanes_PCIe.kicad_sch
Title:
Size: A4
Date: 2025-10-20
Rev: r1B1
KiCad E.D.A. 9.0.5
Id: 6/6