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H1



H2



H3



O **H**



5 •

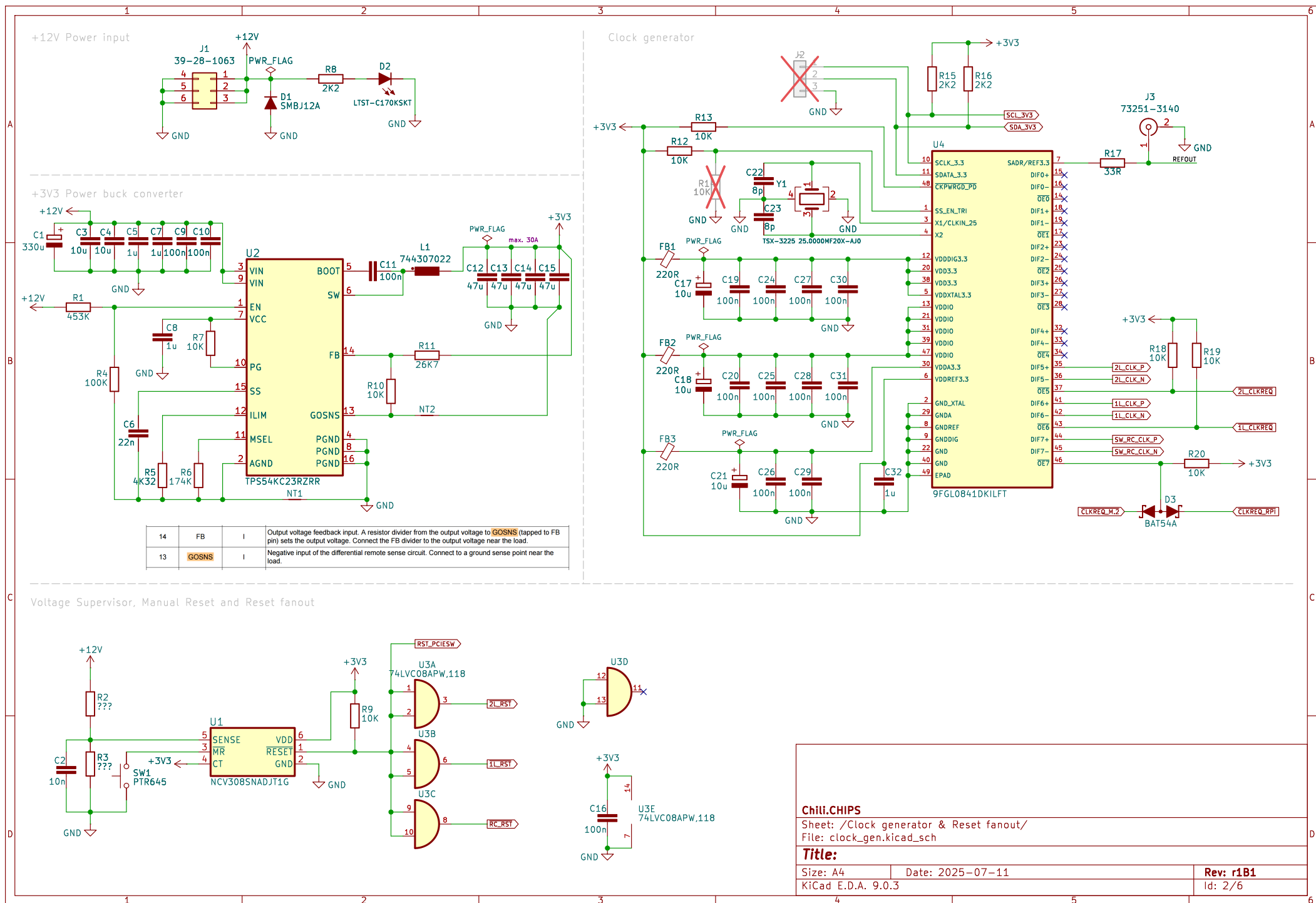
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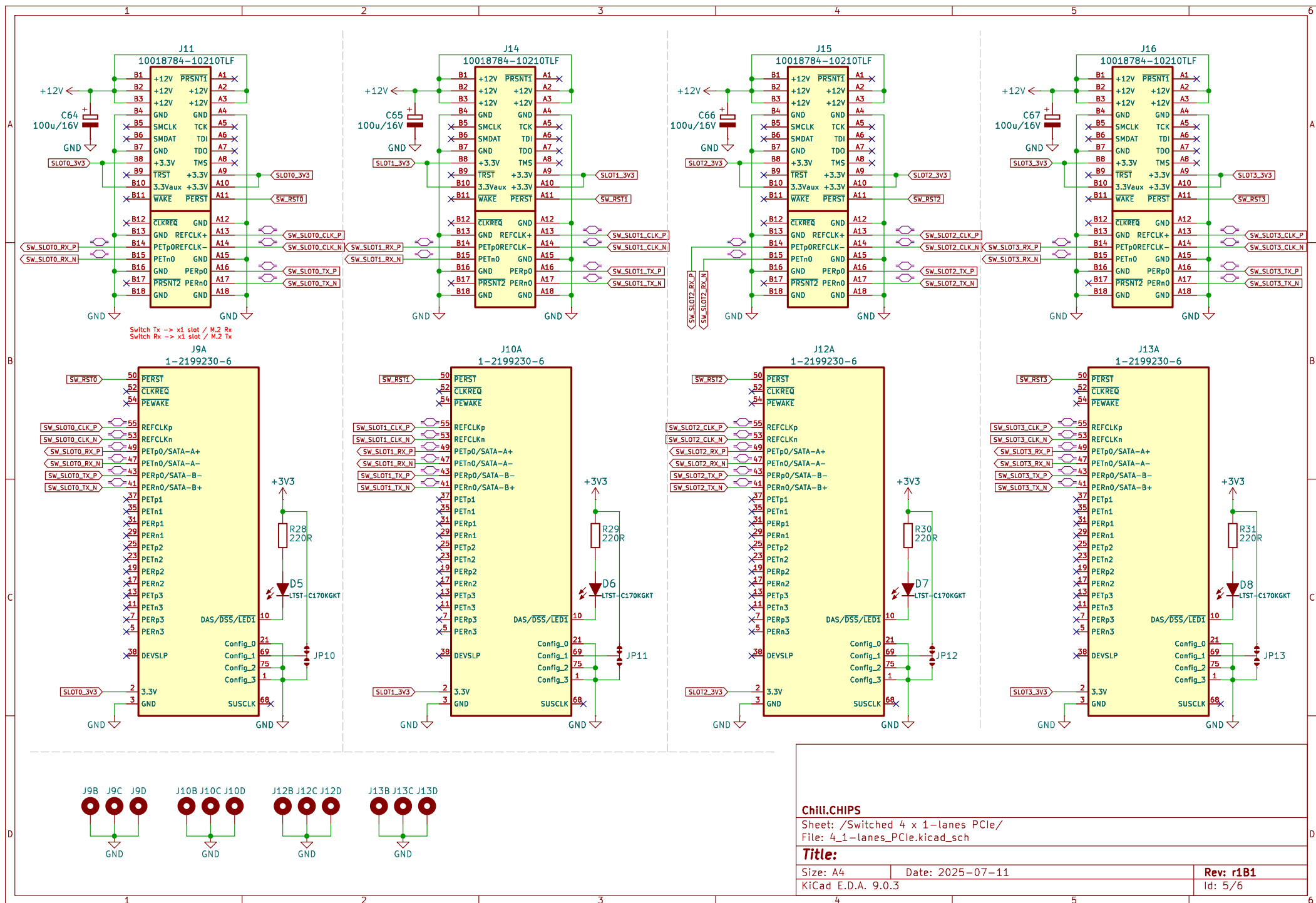
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Date: 2025-07-11

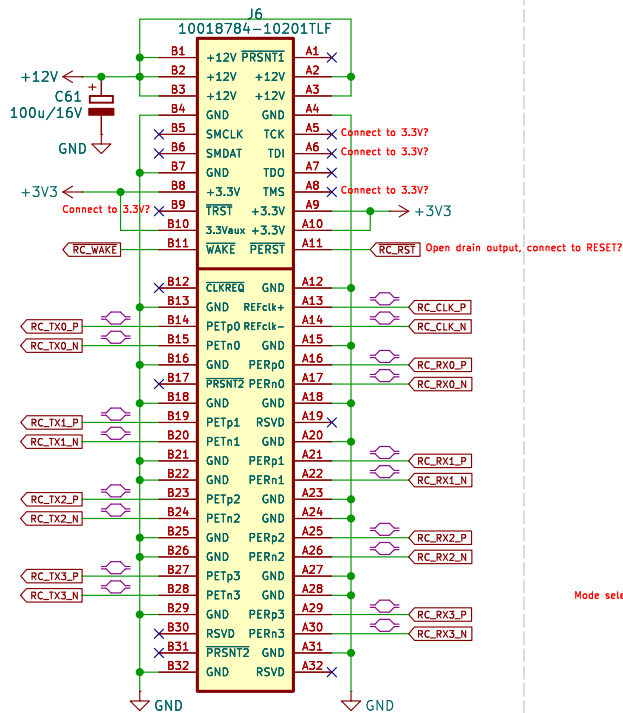
Rev: r1B1

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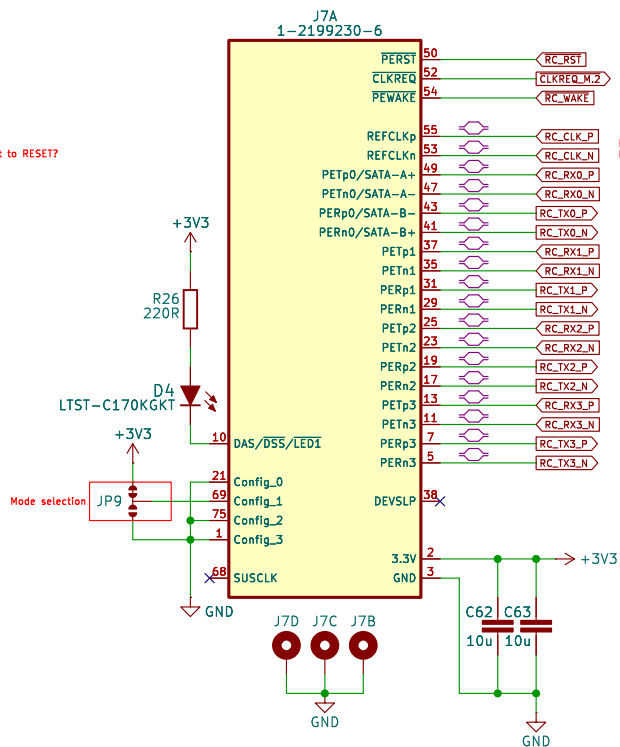


4-lane PCIe for Root Complex

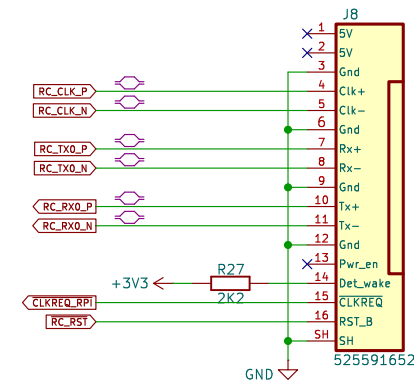


Lanes #	Device
0	PCIe switch for 4 x 1-lanes + 4 x M.2
1	1-lanes slot + M.2
2	2-lanes slot + M.2 (First)
3	2-lanes slot + M.2 (Second)

4-lane M.2 (Type M) for Root Complex



Raspberry Pi FPC 16-pin connector



2.1. PCIe Signals

The PCIe signals are a single lane of PCIe Gen 2, including $\overline{\text{CLKREQ}}$ and RST_B sideband signals which operate at 3.3V.

2.1.1. Pwr_en pin

This pin is a 3.3V output from the Raspberry Pi to a HAT+ or other add-on board, and signals to the HAT+ to power up any supplies. For example, in the instance of the Raspberry Pi M.2 M Key HAT+, this enables the M.2 3.3V power (which is generated from the Incoming 5V). Provide a 100K low pull on this pin on a HAT+.

2.1.2. Det_wake pin

This pin is a 3.3V Input to the Raspberry Pi. Pull high to 3.3V either from a resistive divider from 5V (3k6/6k8 giving 2.35k output impedance), or from permanently enabled 3.3V (using a 2.2K resistor). The Raspberry Pi will detect this high pull at boot time, and will automatically probe the PCIe bus. Use the PCIe WAKE# to pull this low

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Sheet: /RC 1-lane and 2-lane PCIe/
File: RC_4-lanes-PCIe.kicad_sch

Title:

Size: A4

Date: 2025-07-11

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Rev: r1B1

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