PCBA Functional Test Procedure

Prepared for: Elecrow
Project: openpci2-backplane

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Introduction

This document outlines the mandatory functional test procedures for the openpci2-backplane PCBA after assembly. The purpose of this test is to verify the soldering quality, power supply stability, and basic signal integrity before the units are shipped.

Please follow the steps sequentially. If any step fails, the board should be marked as "Failed" and separated for inspection.

1 Power Supply Verification

1. **Step 1.1:** Connect the main power supply (**standard 6-pin PCIe power connector (3 × +12V, 3 × GND), up to 70W total**) to the board input connector.

2. **Step 1.2:** Using a Digital Multimeter, measure the voltages at the specific test points indicated in **Figure 1** below. Reference all measurements to the board Ground (GND).

   Verify the following voltage rails are present and stable:

   - **12V** (Main Input)
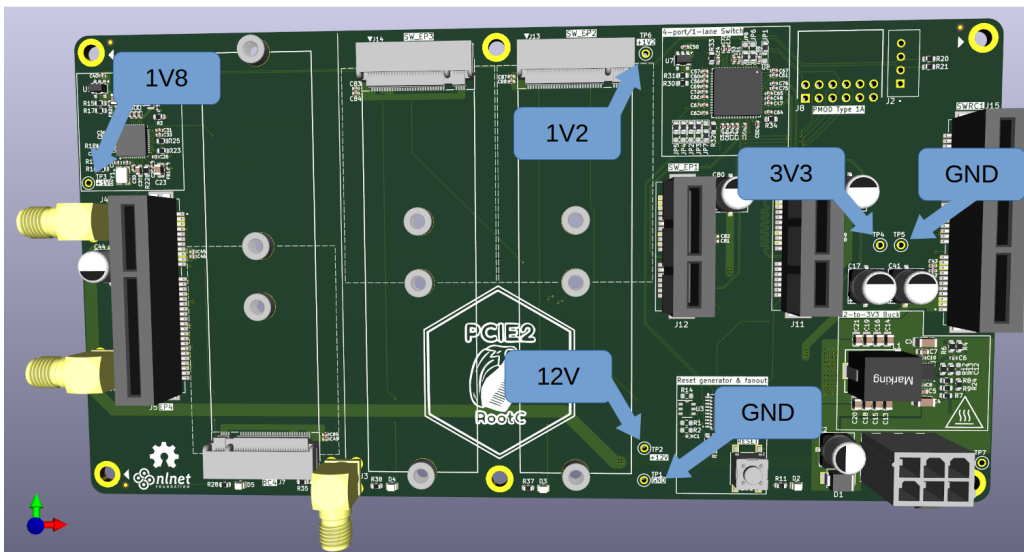   - **3V3** (Output from DC/DC Buck Converter)
   - **1V8**
   - **1V2**

Figure 1: Voltage Measurement Points

2 Reset Circuit Verification

The objective of this section is to verify that the manual reset signal is correctly distributed to all destination points on the backplane.

1. **Step 2.1:** Ensure the board is powered (12V applied).

2. **Step 2.2:** Locate the **RESET Button** and the **7 specific Reset Test Points** indicated in **Figure 2**.

3. **Step 2.3: Idle State Check:** Without pressing the button, measure the voltage at **all 7 test points**.

   - Verify that **all 7 points** are at a **High Logic Level ($\approx$ 3V3)**.

4. **Step 2.4: Active State Check:** Press and **hold** the RESET Button. While holding the button, measure the voltage at **all 7 test points** again.

   - Verify that **all 7 points** drop to a **Low Logic Level ($\approx$ 0V / GND)**.

5. **Step 2.5:** Release the button and confirm that **all 7 test points** return to a **High Logic Level ($\approx$ 3V3)**.
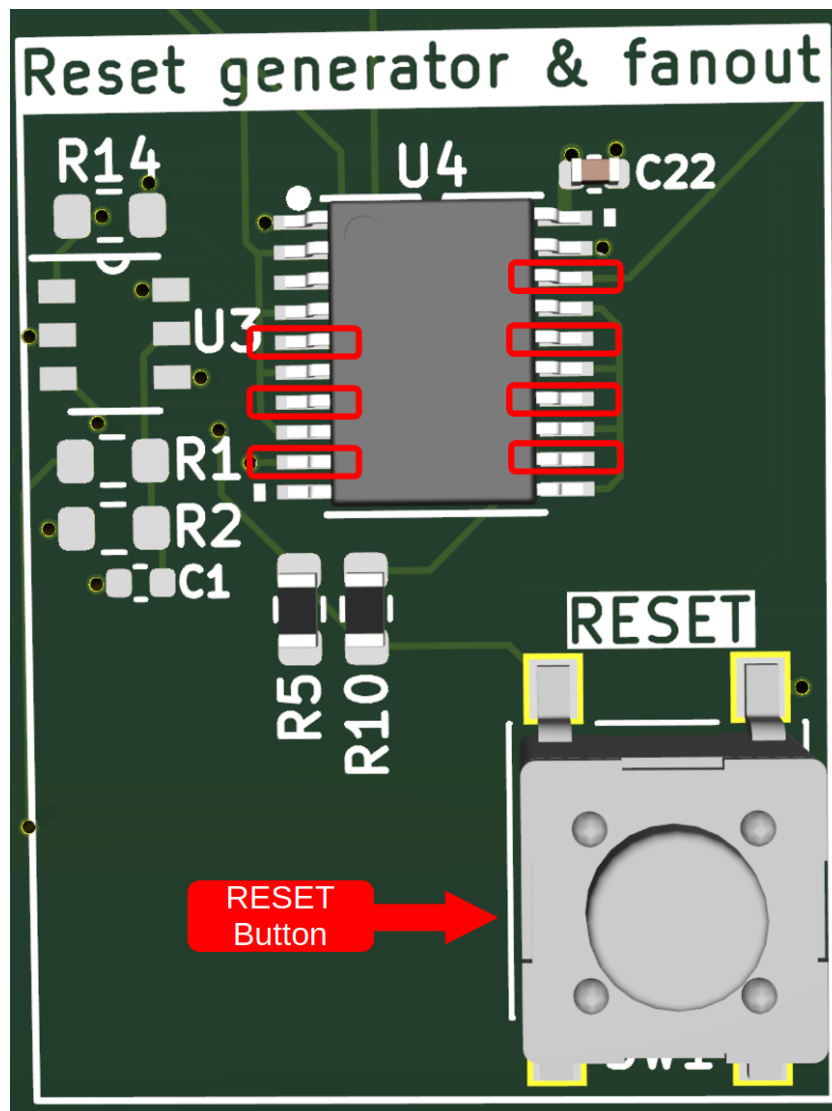

Figure 2: Location of Reset Button and the 7 Verification Points

3 Reference Clock Verification

The objective of this section is to verify the clock generator chip functionality. This is done in two parts: first by checking the primary reference output, and second by verifying the individual PCIe clocks.

3.1 Part 1: Primary Reference Check (25 MHz)

Objective: Verify that the clock generator is active and the crystal is oscillating.

1. **Step 3.1:** Ensure the board is powered (12V).

2. **Step 3.2:** Locate **Resistor R22** (Series resistor for the SMA connector J4). See **Figure 3**.

3. **Step 3.3:** Probe the signal on **R22**.

4. **Step 3.4:** Verify the signal parameters:

   - **Frequency: 25 MHz**
   - **Waveform:** Clean square/sine-like wave.
   - **Amplitude:** Logic High (V_{OH}) should be >**1.35V** (typically ≈ 1.8V). Logic Low (V_{OL}) should be <**0.45V** (typically ≈ 0V).

5. **Decision:** If this signal is **ABSENT**, the clock chip is not running. **STOP the test**. If present, proceed to Part 2.
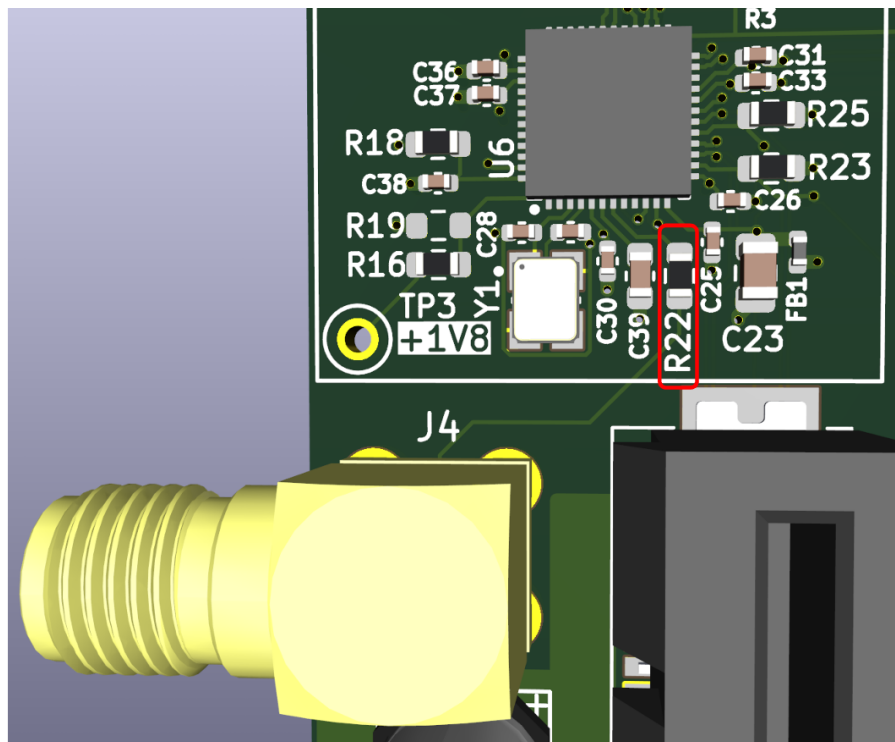

Figure 3: Location of Resistor R22 (25MHz Check)

3.2   Part 2: PCIe Output Verification (100 MHz)

Objective: Verify signal integrity on all 7 PCIe connectors (14 differential signal lines in total).
   IMPORTANT NOTES:

- **Activation:** The clocks are controlled by **CLKREQ# signals** which are Disabled (High) by default. To measure a clock, the operator **must force the specific CLKREQ# pin to GND**.

- **Probing Safety:** Extreme caution is required when probing **M.2 connectors** (0.2mm gap between pads).

1. **Step 3.5:** Locate the test points on the connectors as defined below:

   - **3x M.2 Connectors:** Pins **53** and **55**.
     Refer to **Figure 4**. Note the two different orientations (Up and Down).
     *Note: Probe directly on the **solder pads**.*

   - **2x PCIe x1 Slots:** Pins **A13** and **A14**.
     Refer to **Figure 5**.
     *Note: While probing solder pads is possible, it is **safer and easier** to probe the metal pins directly at the **connector entrance**.*

   - **2x PCIe x4 Slots:** Pins **A13** and **A14**.
     Refer to **Figure 6**. Note the two different orientations (Left and Right).
     *Note: While probing solder pads is possible, it is **safer and easier** to probe the metal pins directly at the **connector entrance**.*

2. **Step 3.6:** Perform the measurement for **each of the 7 slots**:

   (a) Use a jumper wire to **short the corresponding CLKREQ# signal to GND**.

   (b) Carefully probe the indicated pins (A13/A14 or 53/55) with the oscilloscope.

   (c) Verify the clock is present.

3. **Step 3.7:** Verify the signal parameters for all points:

   - **Frequency: 100 MHz**
   - **Waveform:** Clean square/sine-like wave.
   - **Amplitude:** Logic High (V_{OH}) should be approx. **0.7V - 0.8V**. Logic Low (V_{OL}) approx. **0V**.
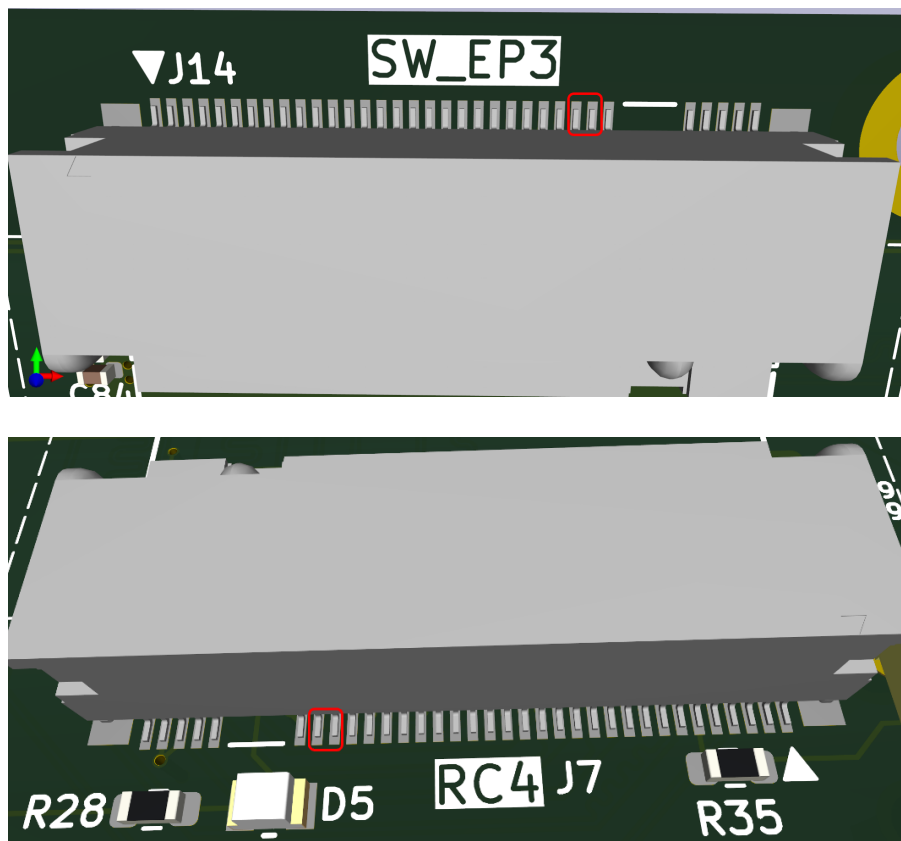   - **Status:** Signal must appear ONLY when CLKREQ# is grounded.

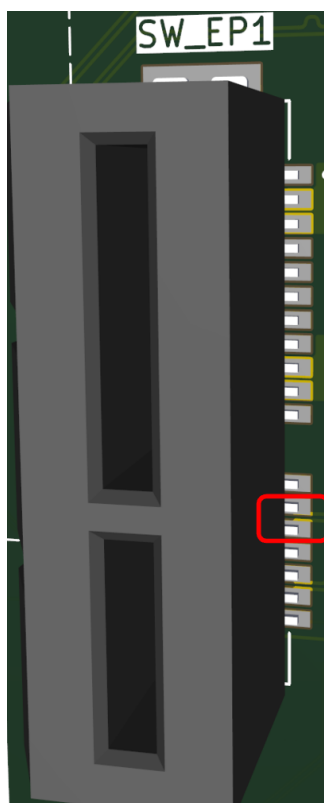Figure 4: M.2 Connector Clock Points (Up and Down Orientations)
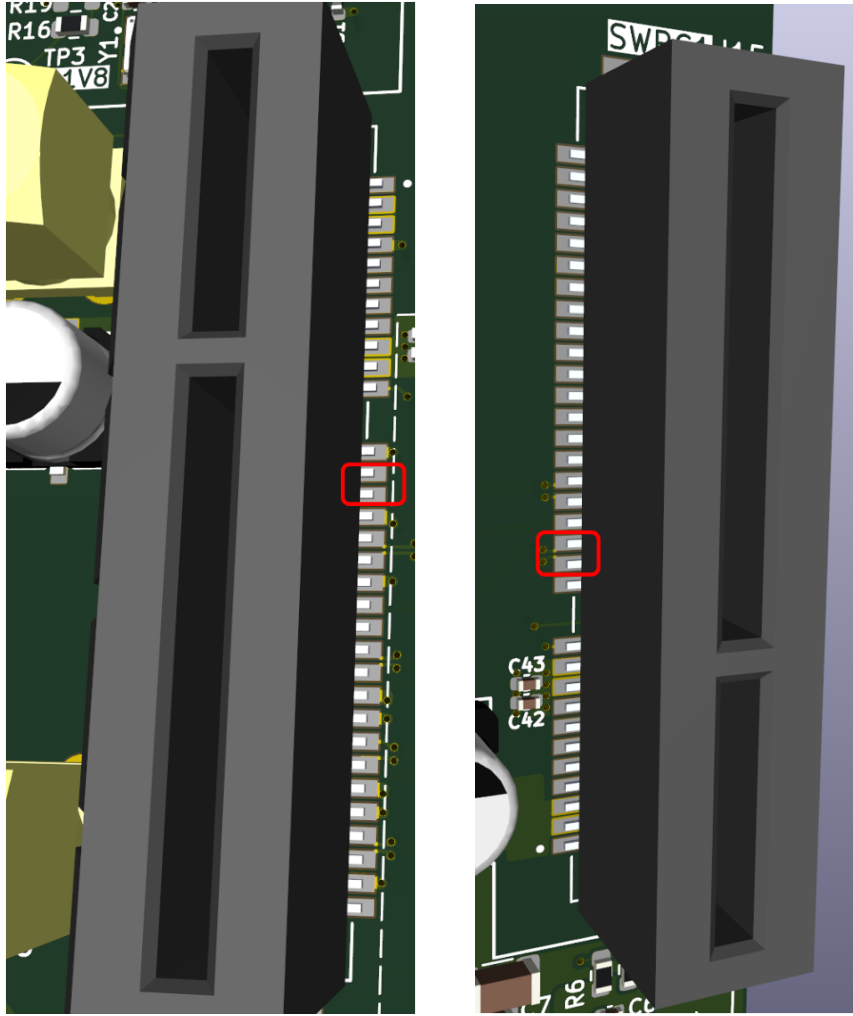

Figure 5: PCIe x1 Slot Clock Points (Pins A13, A14)

Figure 6: PCIe x4 Slot Clock Points (Left and Right Orientations)

End of Test Procedure
If all steps passed, mark the board as **"PASSED"**.