

# Chili.CHIPS

Sheet: /Clock generator & Reset fanout/  
File: clock\_gen.kicad\_sch

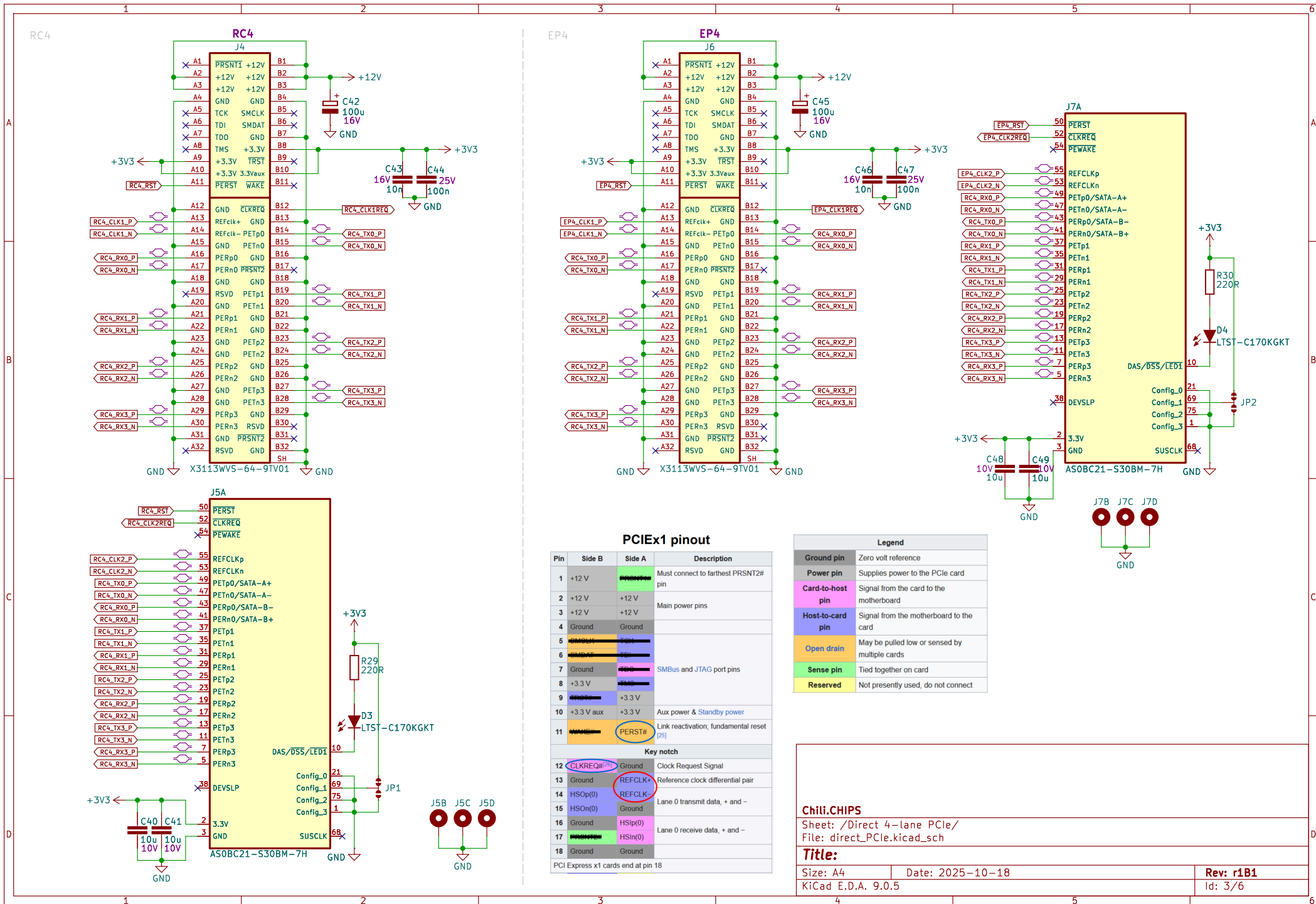
## Title:

Size: A4  
KiCad E.D.A. 9.0.5

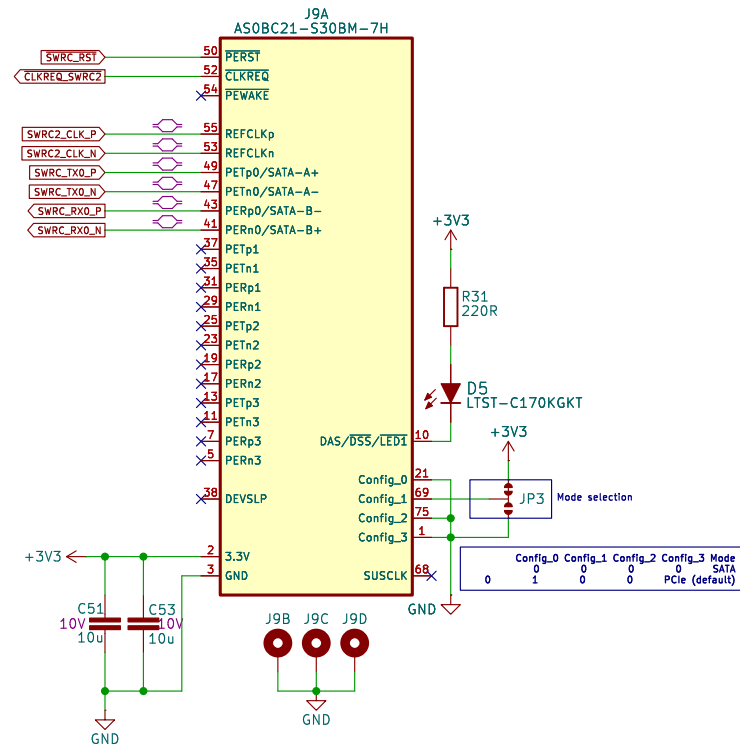
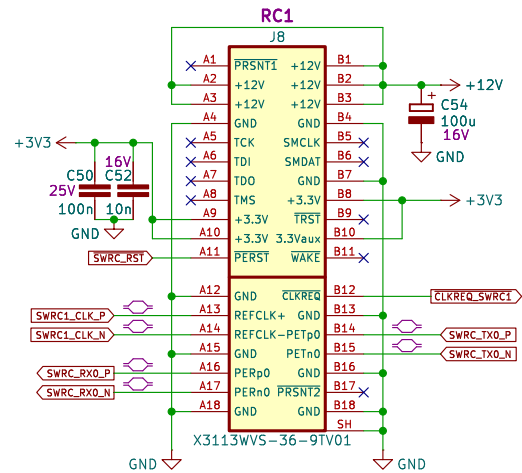
Date: 2025-10-18

Rev: r1B1

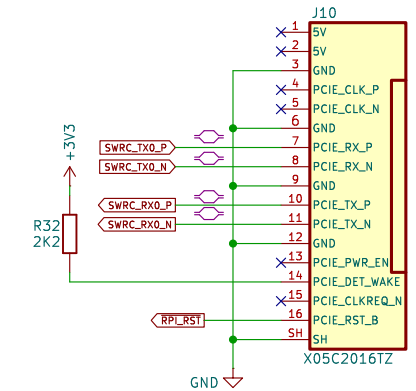
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1-lane PCIe for Root Complex



Raspberry Pi FPC 16-pin connector



As the Root Complex, the Raspberry Pi provides its own reference clock. The rest of the backplane does not need this clock, as all downstream PCIe devices receive their reference clock from the onboard generator (U5).

PCIE\_RST\_B (pin 16) is an active-low output from the Raspberry PI, serving as the master reset for the downstream PCIe fabric. This PCIE\_RST\_B signal is intended to be combined with the board's own reset sources through external logic to generate the final system reset.

## 2.1. PCIe Signals

The PCIe signals are a single lane of PCIe Gen 2, including  $\overline{\text{CLKREQ}}$  and RST\_B sideband signals which operate at 3.3V.

### 2.1.1. Pwr\_en pin

This pin is a 3.3V output from the Raspberry PI to a HAT+ or other add-on board, and signals to the HAT+ to power up any supplies. For example, in the instance of the Raspberry PI M.2 M Key HAT+, this enables the M.2 3.3V power (which is generated from the incoming 5V). Provide a 100K low pull on this pin on any HAT+.

### 2.1.2. Det\_wake pin

This pin is a 3.3V input to the Raspberry Pi. Pull high to 3.3V either from a resistive divider from 5V (3k6/6k8 giving 2.35k output impedance), or from permanently enabled 3.3V (using a 2.2k resistor). The Raspberry Pi will detect this high pull at boot time, and will automatically probe the pin.

Use the PCIe WAKE# to pull this low

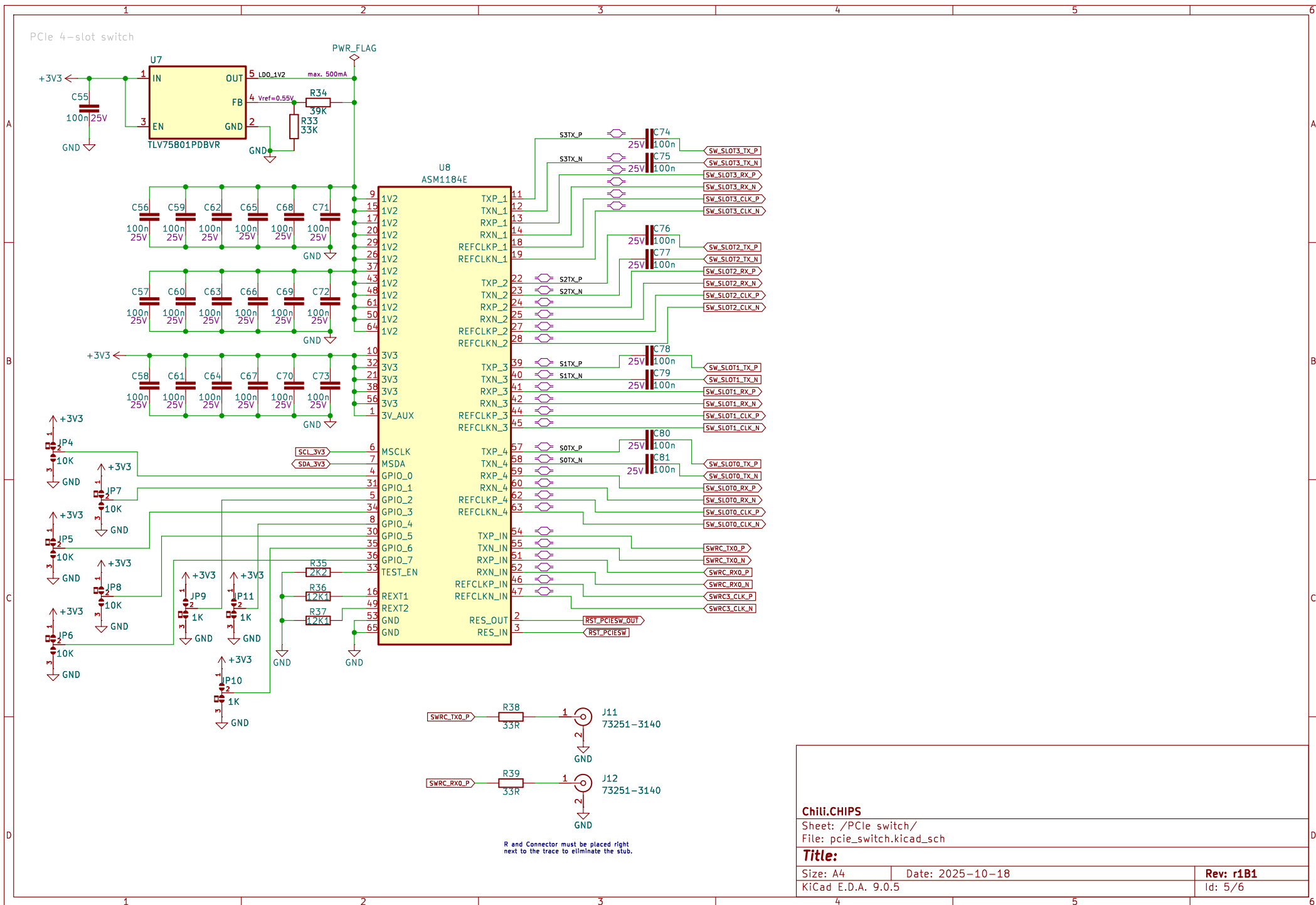
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Sheet: /RC 1-lane and 2-lane PCIe/  
File: RC\_4-lanes-PCle.kicad\_sch

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Size: A4	Date: 2025-10-18
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# Chili.CHIPS

Sheet: /PCle switch/  
File: pcie\_switch.kicad\_sch

## Title:

Size: A4  
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