

Clock generator & Reset fanout

File: clock_gen.kicad_sch

Direct 4-lane PCIe

File: direct_PCl_e.kicad_sch

RC 1-lane and 2-lane PCIe

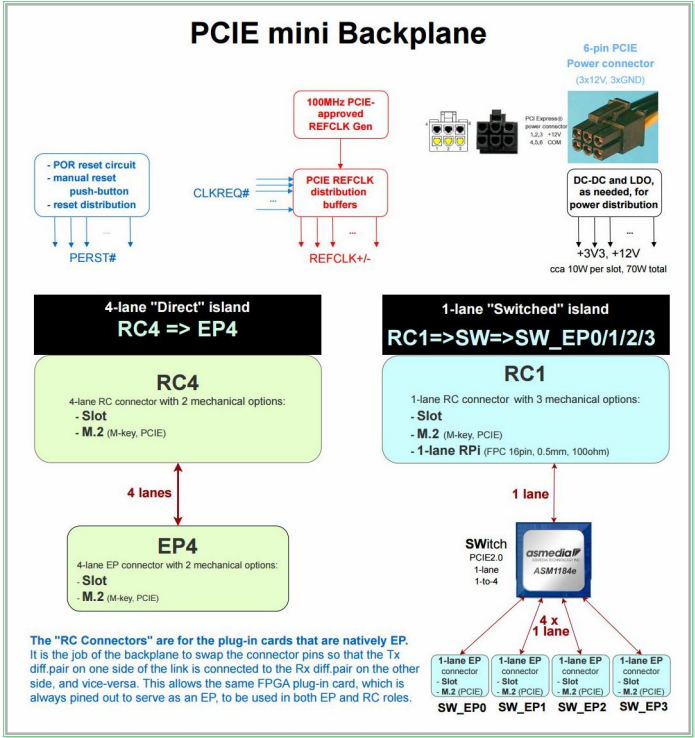
File: RC_4-lanes-PCl_e.kicad_sch

PCIe switch

File: pcie_switch.kicad_sch

Switched 4 x 1-lanes PCIe

File: 4_1-lanes_PCl_e.kicad_sch



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Sheet: /
File: openpci2-backplane.kicad_sch

Title:

Size: A4

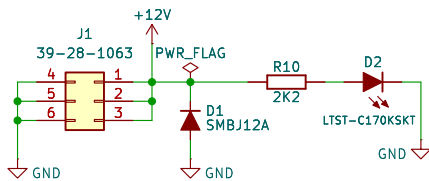
Date: 2025-07-31

KiCad E.D.A. 9.0.3

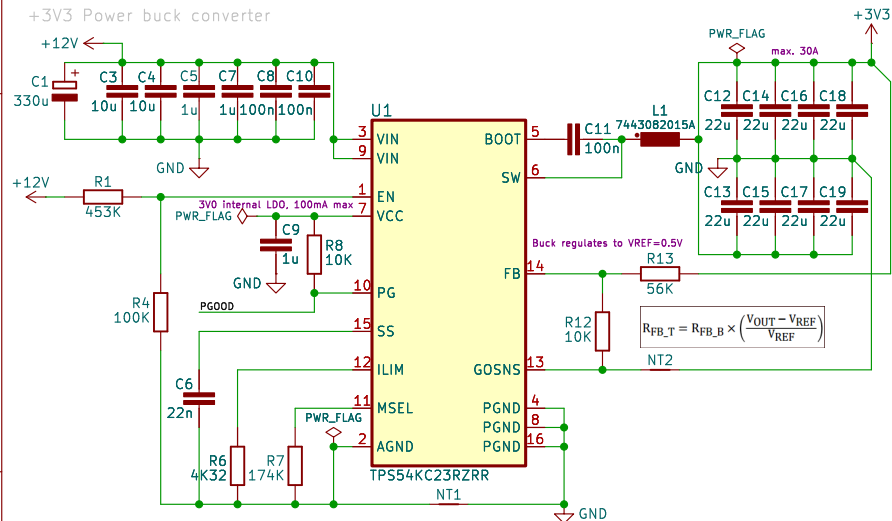
Rev: r1B1

Id: 1/6

+12V Power input

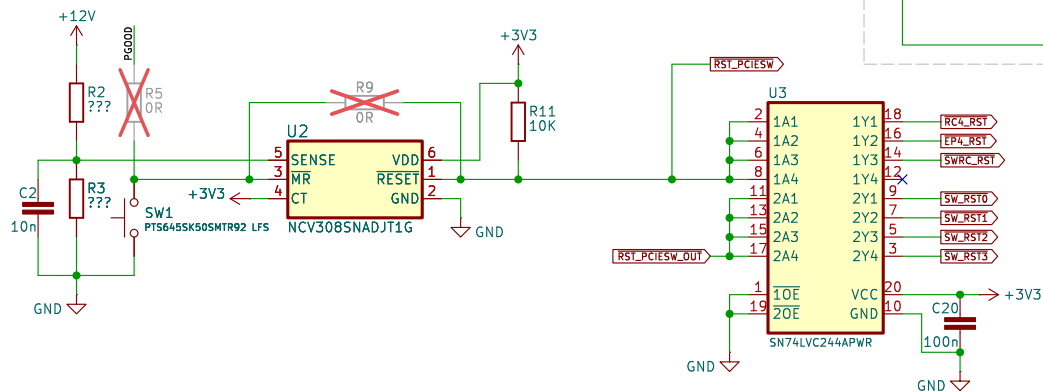


+3V3 Power buck converter

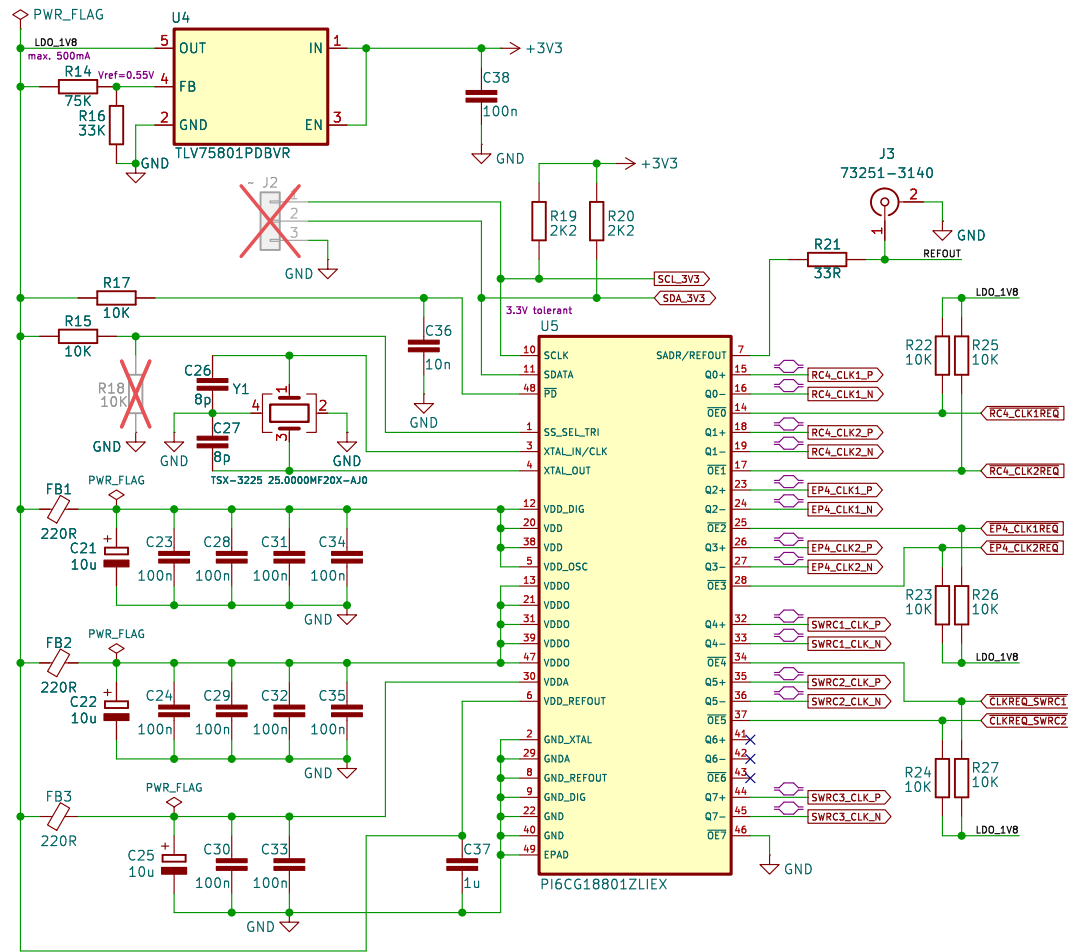


14	FB	I	Output voltage feedback input. A resistor divider from the output voltage to GOSNS (tapped to FB pin) sets the output voltage. Connect the FB divider to the output voltage near the load.
13	GOSNS	I	Negative input of the differential remote sense circuit. Connect to a ground sense point near the load.

Voltage Supervisor, Manual Reset and Reset fanout



Clock generator



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Sheet: /Clock generator & Reset fanout/
File: clock_gen.kicad_sch

Title:

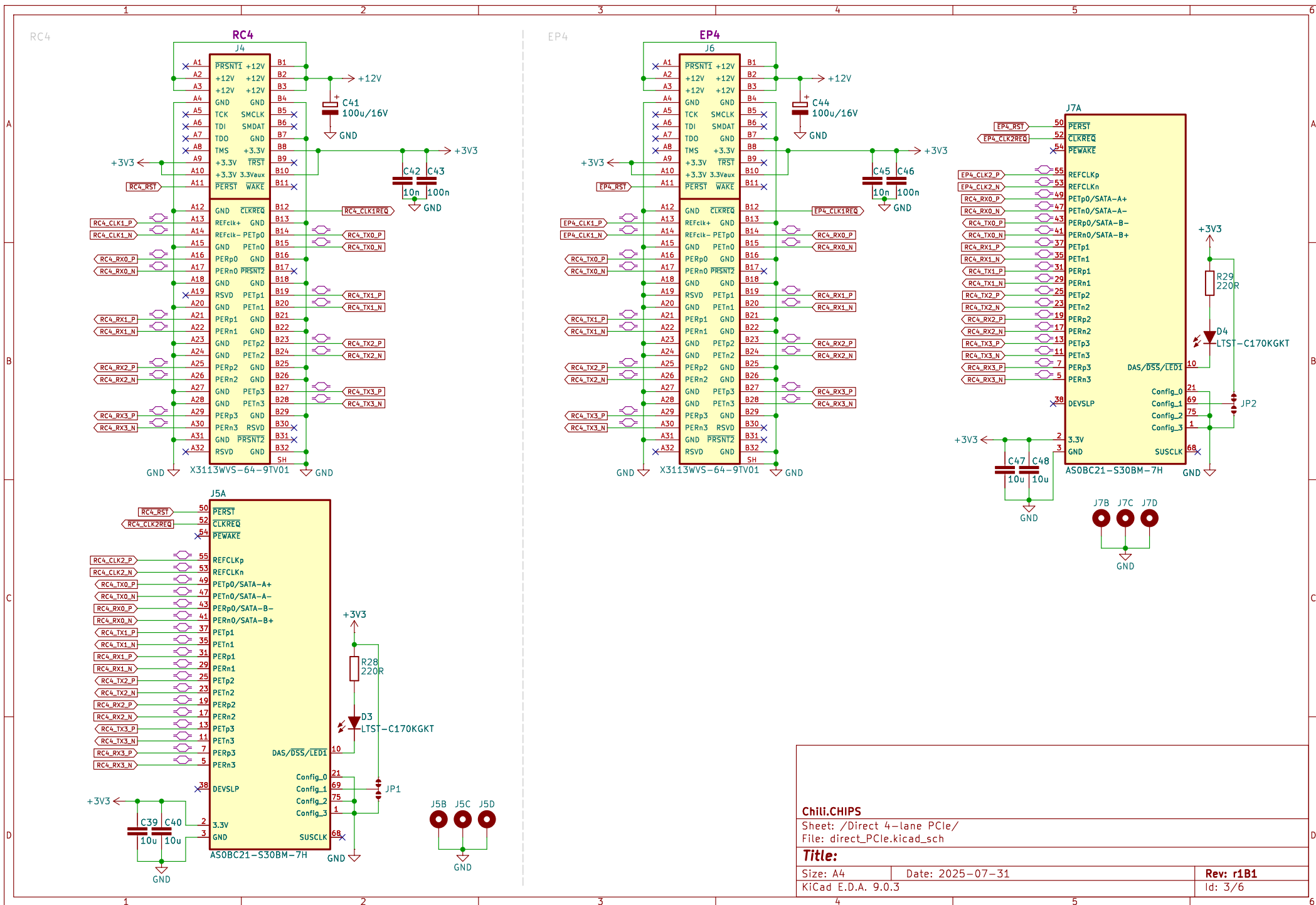
Size: A4

Date: 2025-07-31

Rev: r1B1

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Id: 2/6



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Sheet: /Direct 4-lane PCIe/
File: direct_PCE.kicad_sch

Title:

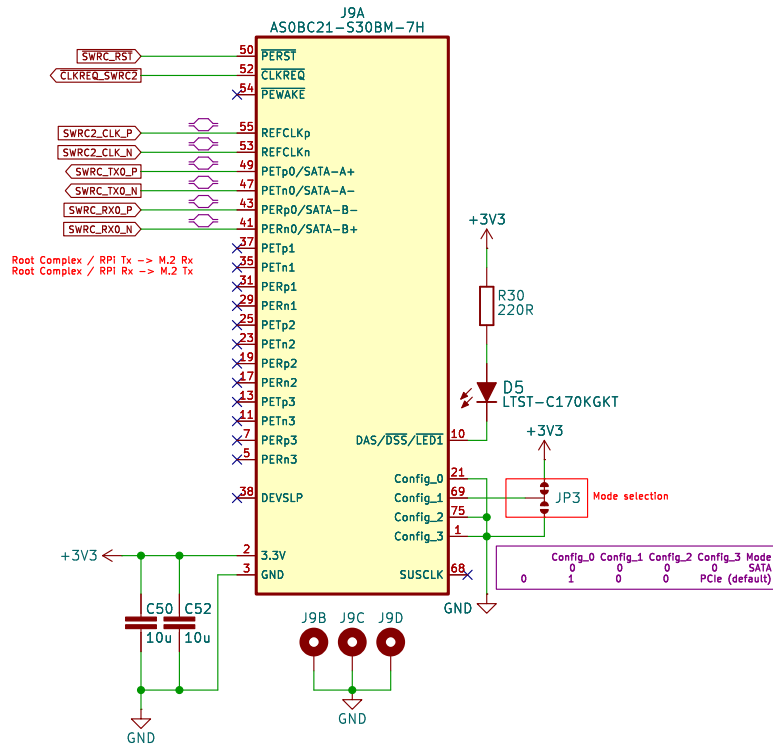
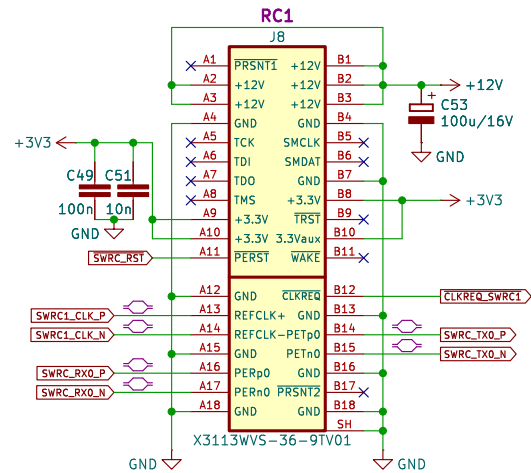
Size: A4
KiCad E.D.A. 9.0.3

Date: 2025-07-31

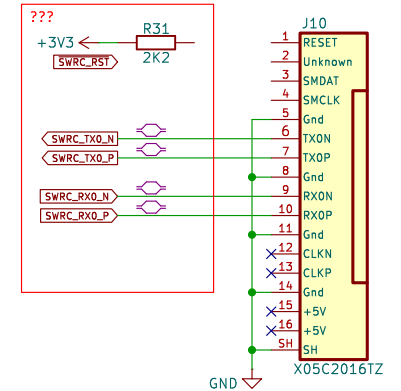
Rev: r1B1

Id: 3/6

1-lane PCIe for Root Complex



Raspberry Pi FPC 16-pin connector



2.1. PCIe Signals

The PCIe signals are a single lane of PCIe Gen 2, including $\overline{\text{CLKREQ}}$ and RST_B sideband signals which operate at 3.3V.

2.1.1. Pwr_en pin

This pin is a 3.3V output from the Raspberry Pi to a HAT+ or other add-on board, and signals to the HAT+ to power up any supplies. For example, in the instance of the Raspberry Pi M.2 M Key HAT+, this enables the M.2 3.3V power (which is generated from the Incoming 5V). Provide a 100K low pull on this pin on any HAT+.

2.1.2. DeL_wake pin

This pin is a 3.3V Input to the Raspberry Pi. Pull high to 3.3V either from a resistive divider from 5V (3k6/6k8 giving 2.35k output impedance), or from permanently enabled 3.3V (using a 2.2K resistor). The Raspberry Pi will detect this high pull at boot time, and will automatically probe the PCIe bus. Use the PCIe WAKE# to pull this low

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Sheet: /RC 1-lane and 2-lane PCIe/
File: RC_4-lanes-PCIe.kicad_sch

Title:

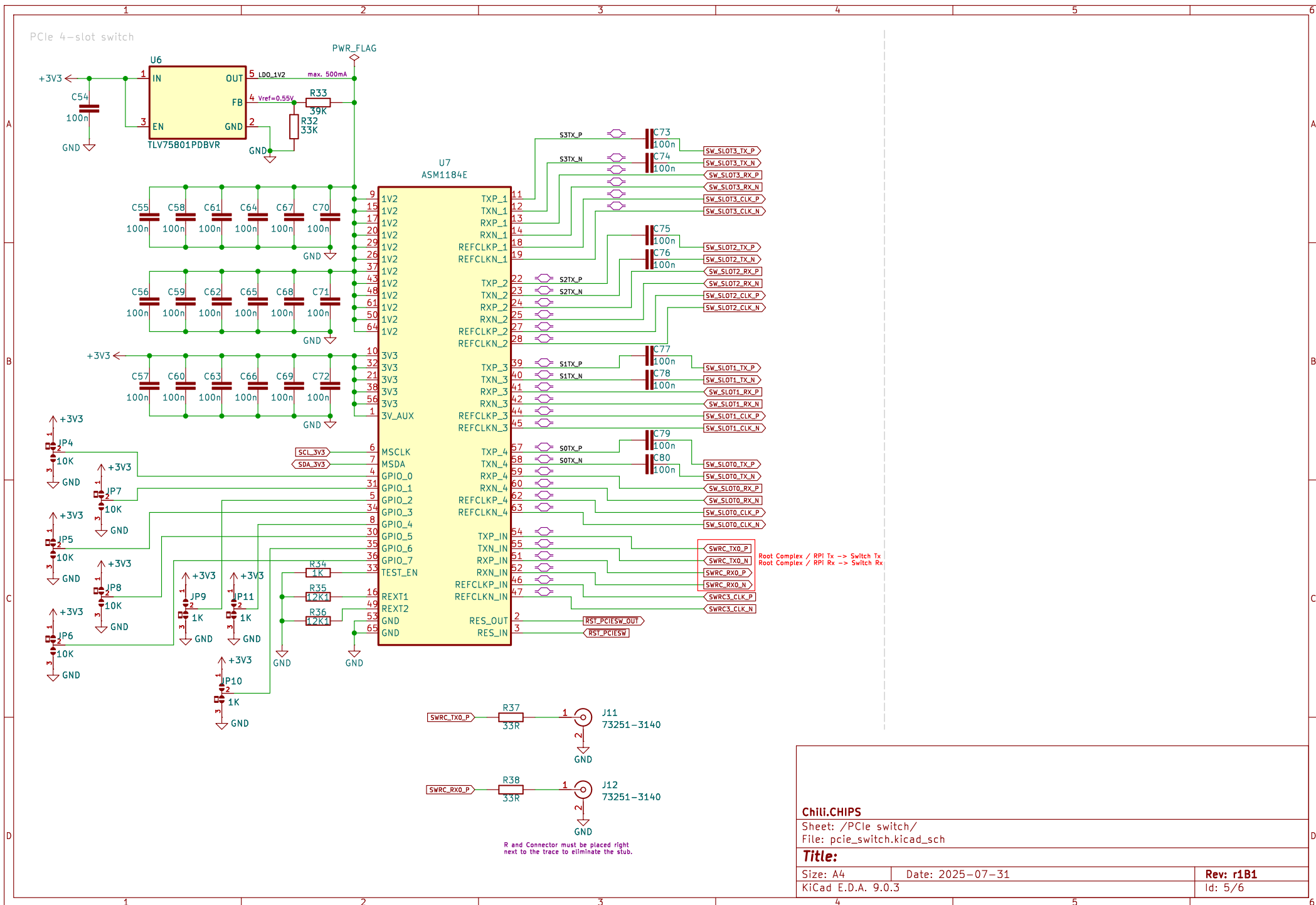
Size: A4

Date: 2025-07-31

Rev: r1B1

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Id: 4/6



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Sheet: /PCle switch/
File: pcie_switch.kicad_sch

Title:

Size: A4
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Date: 2025-07-31

Rev: r1B1

Id: 5/6

