Clock generator

File: clock_gen.kicad_sch

PCIe switch

File: pcie_switch.kicad_sch

RC 4-lines PCIe

File: RC_4-lines-PCIe.kicad_sch

4 x 1-lines PCIe

File: 4_1-lines_PCIe.kicad_sch

Direct PCIe

File: direct_PCIe.kicad_sch

H1 H2 H3 H4 H5 H6

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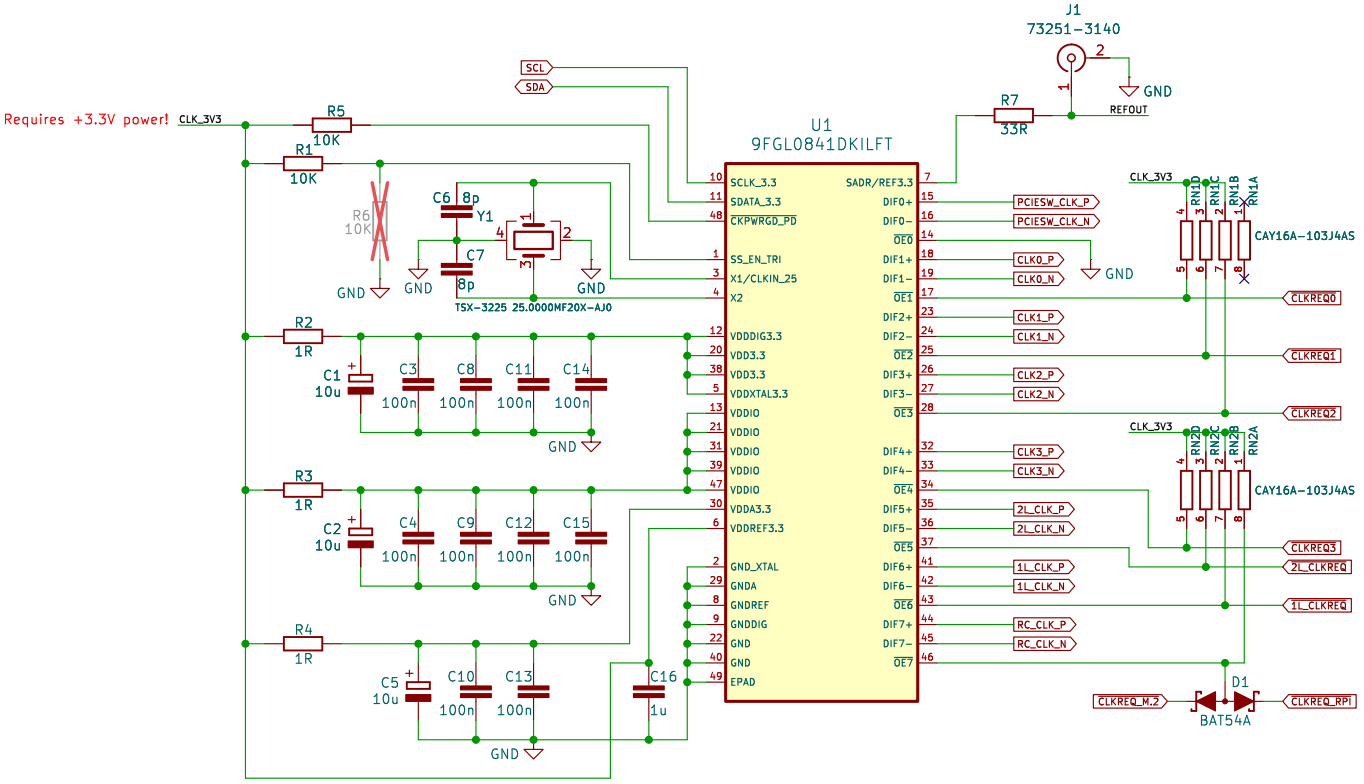
Sheet: /

File: openpci2-backplane.kicad_sch

Title:

Size: A4	Date: 2025-01-28	**Rev: r1B1**
KiCad E.D.A. 8.0.8		Id: 1/6

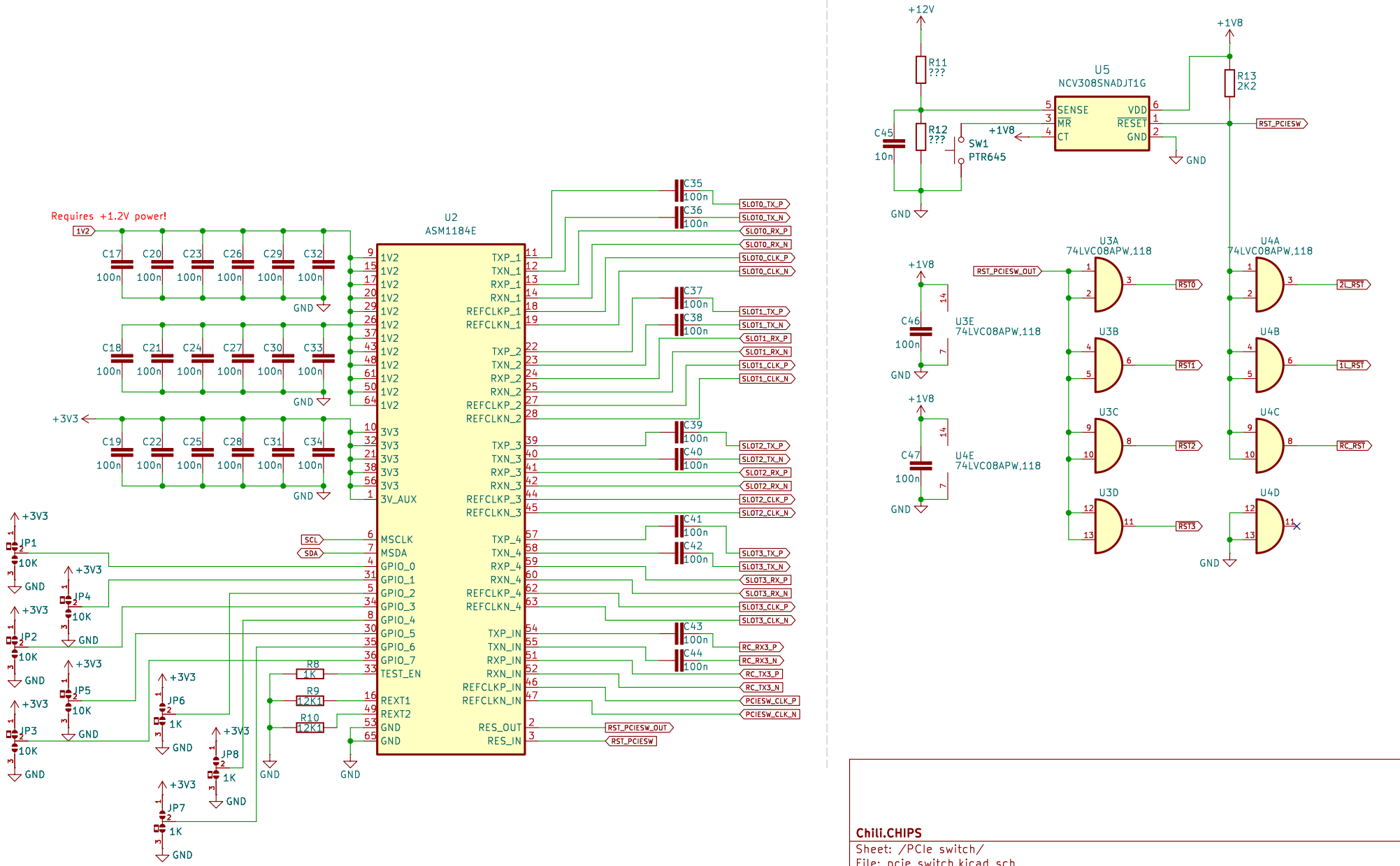
Clock generator & fanout



Chili.CHIPS		
Sheet: /Clock generator/		
File: clock_gen.kicad_sch		
Title:		
Size: A4	Date: 2025-01-28	**Rev: r1B1**
KiCad E.D.A. 8.0.8		Id: 2/6

PCIe 4-slot switch

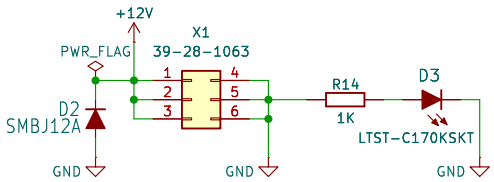
Voltage Supervisor, Manual Reset and Reset fanout



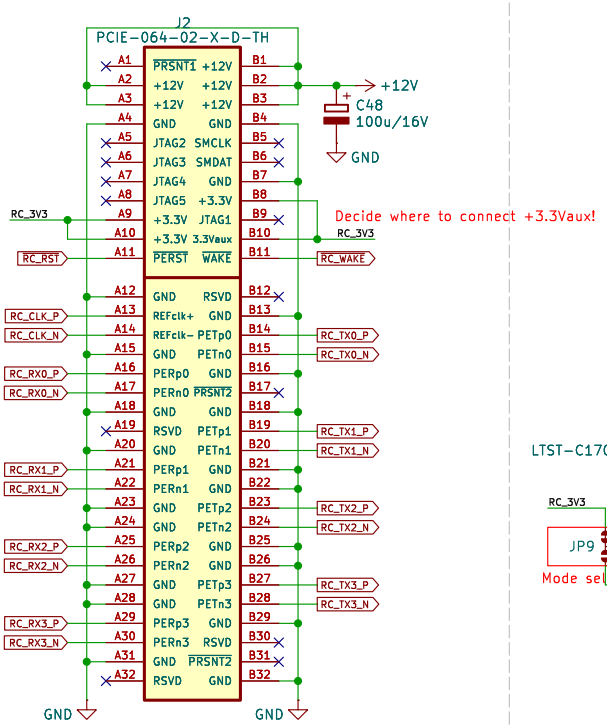
Chili.CHIPS		
Sheet: /PCIe switch/		
File: pcie_switch.kicad_sch		
Title:		
Size: A4	Date: 2025-01-28	**Rev: r1B1**
KiCad E.D.A. 8.0.8		Id: 3/6

+12V Power input

One high power down converter or one per slot?

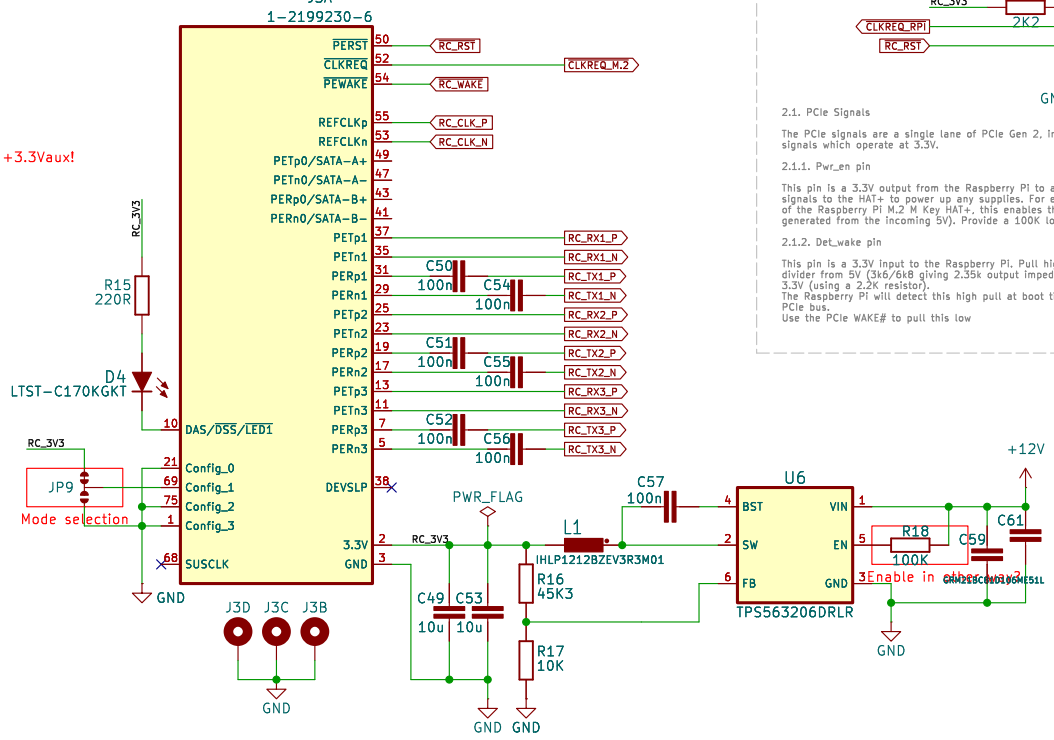


4-lines PCIe for Root Complex

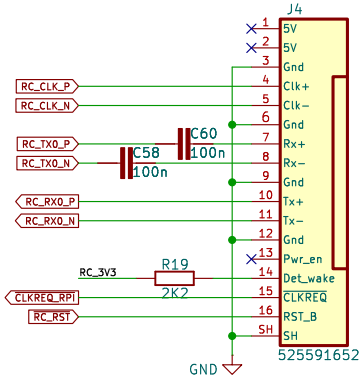


Lines #	Device
0	2-lines slot + M.2, Raspberry Pi PFC
1	2-lines slot + M.2
2	1-lines slot + M.2
3	PCIe switch for 4 x 1-lines + 4 x M.2

4-lines M.2 (Type M) for Root Complex



Raspberry Pi FPC 16-pin connector



2.1. PCIe Signals

The PCIe signals are a single lane of PCIe Gen 2, including CLKREQ and RST_B sideband signals which operate at 3.3V.

2.1.1. Pwr_en pin

This pin is a 3.3V output from the Raspberry PI to a HAT+ or other add-on board, and signals to the HAT+ to power up any supplies. For example, in the instance of the Raspberry PI M.2 M Key HAT+, this enables the M.2 3.3V power (which is generated from the incoming 5V). Provide a 100K low pull on this pin on any HAT+.

2.1.2. Det_wake pin

This pin is a 3.3V input to the Raspberry PI. Pull high to 3.3V either from a resistive divider from 5V (3k6/6k8 giving 2.35k output impedance), or from permanently enabled 3.3V (using a 2.2K resistor).
The Raspberry PI will detect this high pull at boot time, and will automatically probe the PCIe bus.
Use the PCIe WAKE# to pull this low

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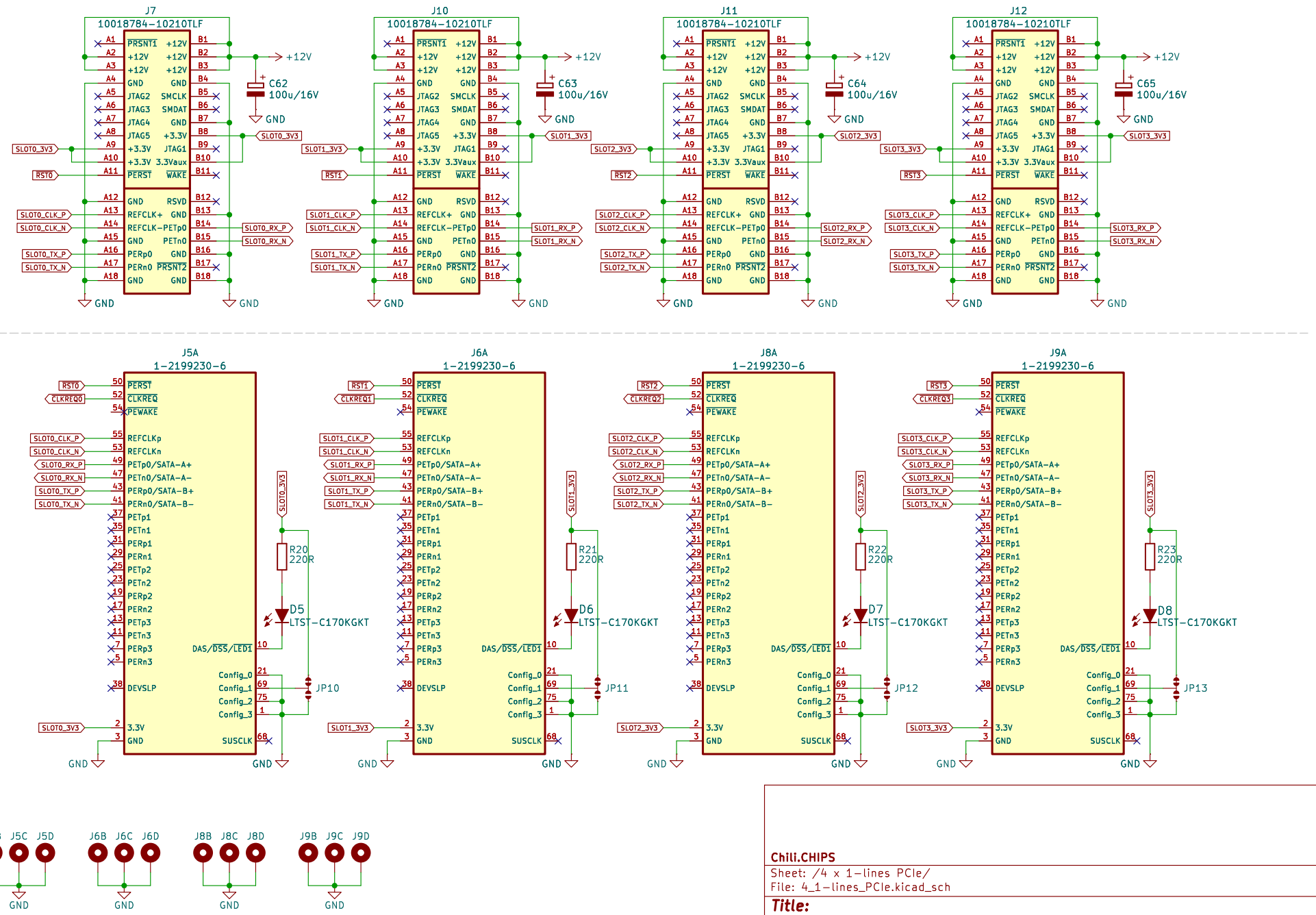
Sheet: /RC 4-lines PCIe/
File: RC_4-lines-PCIe.kicad_sch

Title:

Size: A4	Date: 2025-01-28	**Rev: r1B1**
KiCad E.D.A. 8.0.8		Id: 4/6



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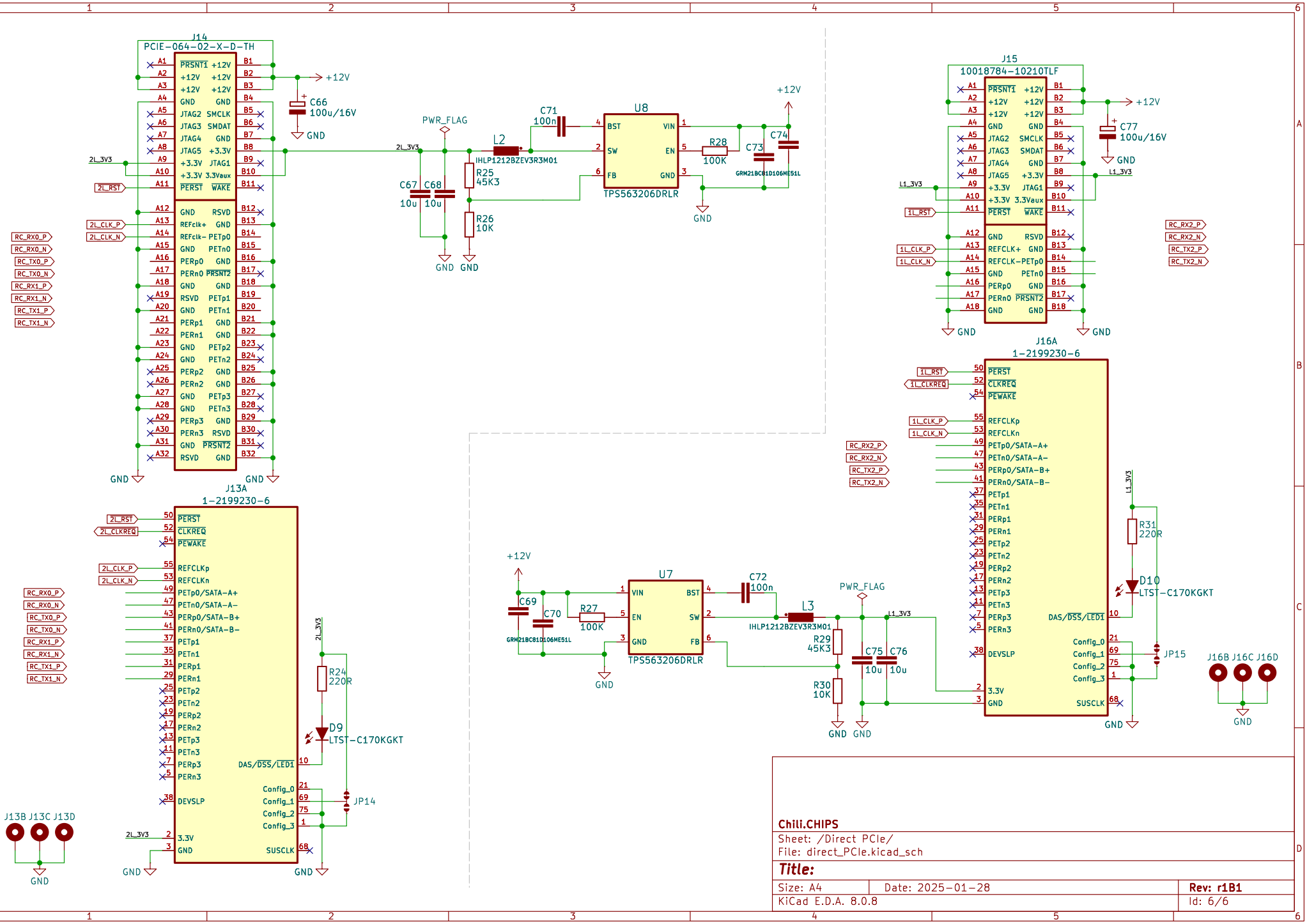
Sheet: /4 x 1-lines PCIe/

File: 4_1-lines_PCIe.kicad_sch

Title:

Size: A4	Date: 2025-01-28	**Rev: r1B1**
KiCad E.D.A. 8.0.8		Id: 5/6


J14
PCIE-064-02-X-D-TH
+12V
C66
100u/16V
GND
PWR_FLAG
2L_3V3
L2
IHLP1212BZEV3R3M01
C71
100n
U8
BST
VIN
SW
EN
FB
GND
TPS563206DRLR
R28
100K
C74
C73
GRM21BC81D106ME51L
C67
C68
10u
R25
45K3
R26
10K
2L_RST
2L_CLK_P
2L_CLK_N
RC_RX0_P
RC_RX0_N
RC_TX0_P
RC_TX0_N
RC_RX1_P
RC_RX1_N
RC_TX1_P
RC_TX1_N
J15
10018784-10210TLF
C77
100u/16V
L1_3V3
1L_RST
1L_CLK_P
1L_CLK_N
RC_RX2_P
RC_RX2_N
RC_TX2_P
RC_TX2_N
J16A
1-2199230-6
1L_CLKREQ
R31
220R
D10
LTST-C170KGKT
JP15
J16B J16C J16D
J13A
1-2199230-6
2L_CLKREQ
R24
220R
D9
LTST-C170KGKT
JP14
J13B J13C J13D
U7
C69
C70
R27
100K
C72
100n
L3
IHLP1212BZEV3R3M01
R29
45K3
R30
10K
C75
C76
10u
Chili.CHIPS
Sheet: /Direct PCIe/
File: direct_PCIe.kicad_sch
Title:
Size: A4
Date: 2025-01-28
Rev: r1B1
KiCad E.D.A. 8.0.8
Id: 6/6