

Clock generator & Reset fanout

File: clock\_gen.kicad\_sch

Direct 4-lane PCIe

File: direct\_PClc.kicad\_sch

RC 1-lane and 2-lane PCIe

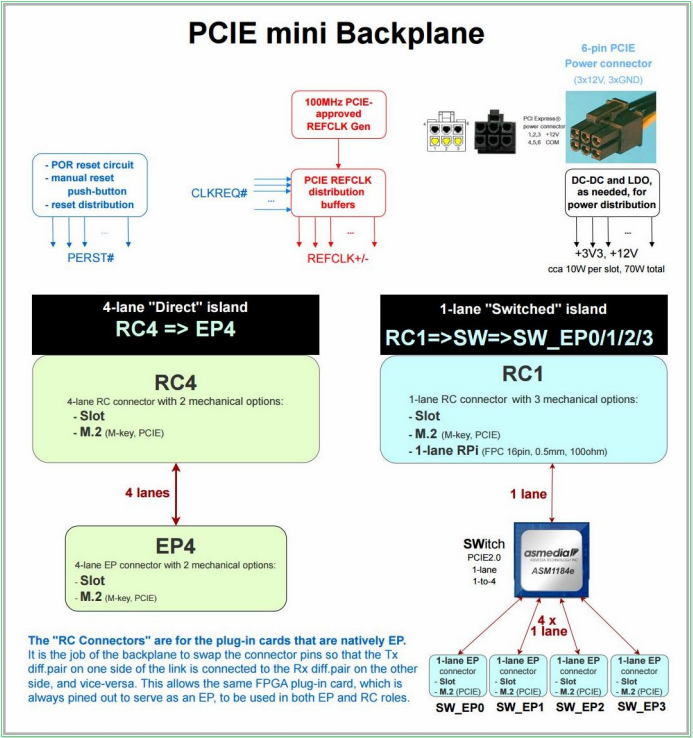
File: RC\_4-lanes-PClc.kicad\_sch

PClc switch

File: pcic\_switch.kicad\_sch

Switched 4 x 1-lanes PCIe

File: 4\_1-lanes\_PClc.kicad\_sch



Chili.CHIPS

Sheet: /  
File: openpci2-backplane.kicad\_sch

Title:

Size: A4

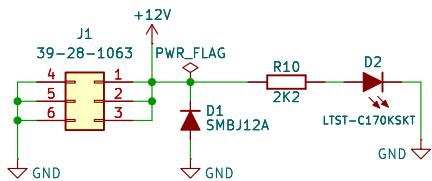
Date: 2025-07-31

KiCad E.D.A. 9.0.3

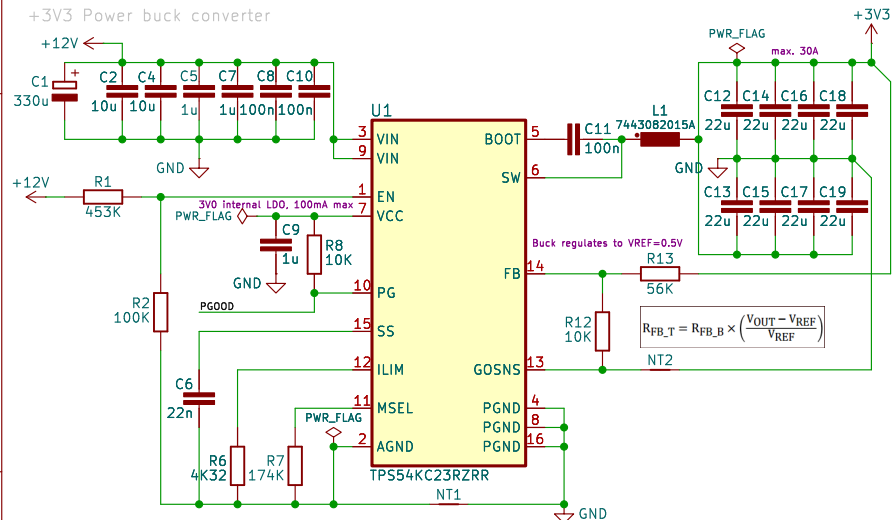
Rev: r1B1

Id: 1/6

# +12V Power input

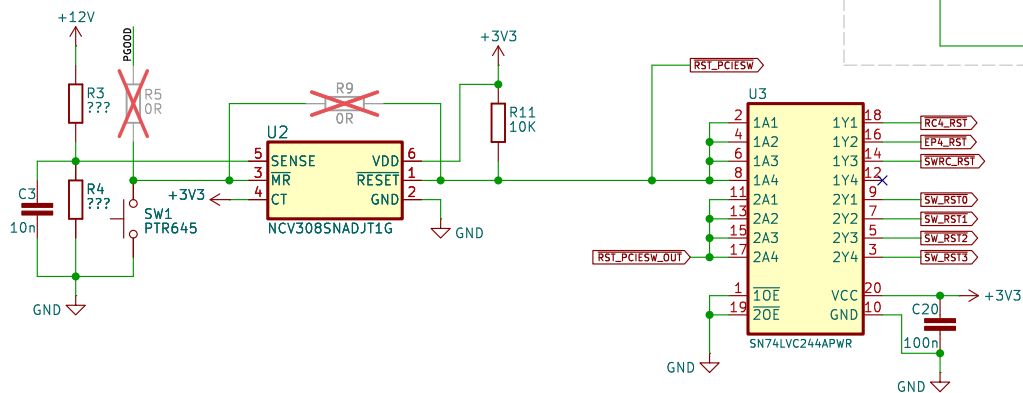


# +3V3 Power buck converter

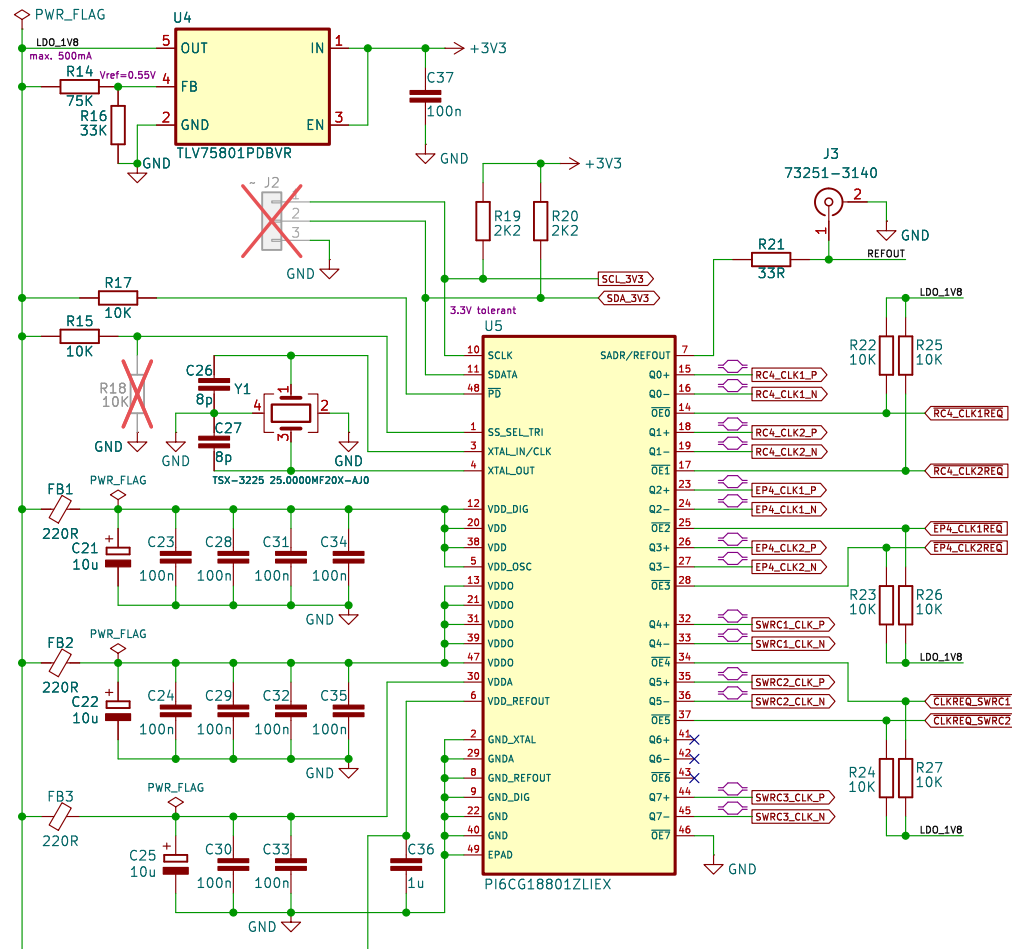


14	FB	I	Output voltage feedback input. A resistor divider from the output voltage to <b>GOSNS</b> (tapped to FB pin) sets the output voltage. Connect the FB divider to the output voltage near the load.
13	<b>GOSNS</b>	I	Negative input of the differential remote sense circuit. Connect to a ground sense point near the load.

# Voltage Supervisor, Manual Reset and Reset fanout



# Clock generator



## Chili.CHIPS

Sheet: /Clock generator & Reset fanout/  
File: clock\_gen.kicad\_sch

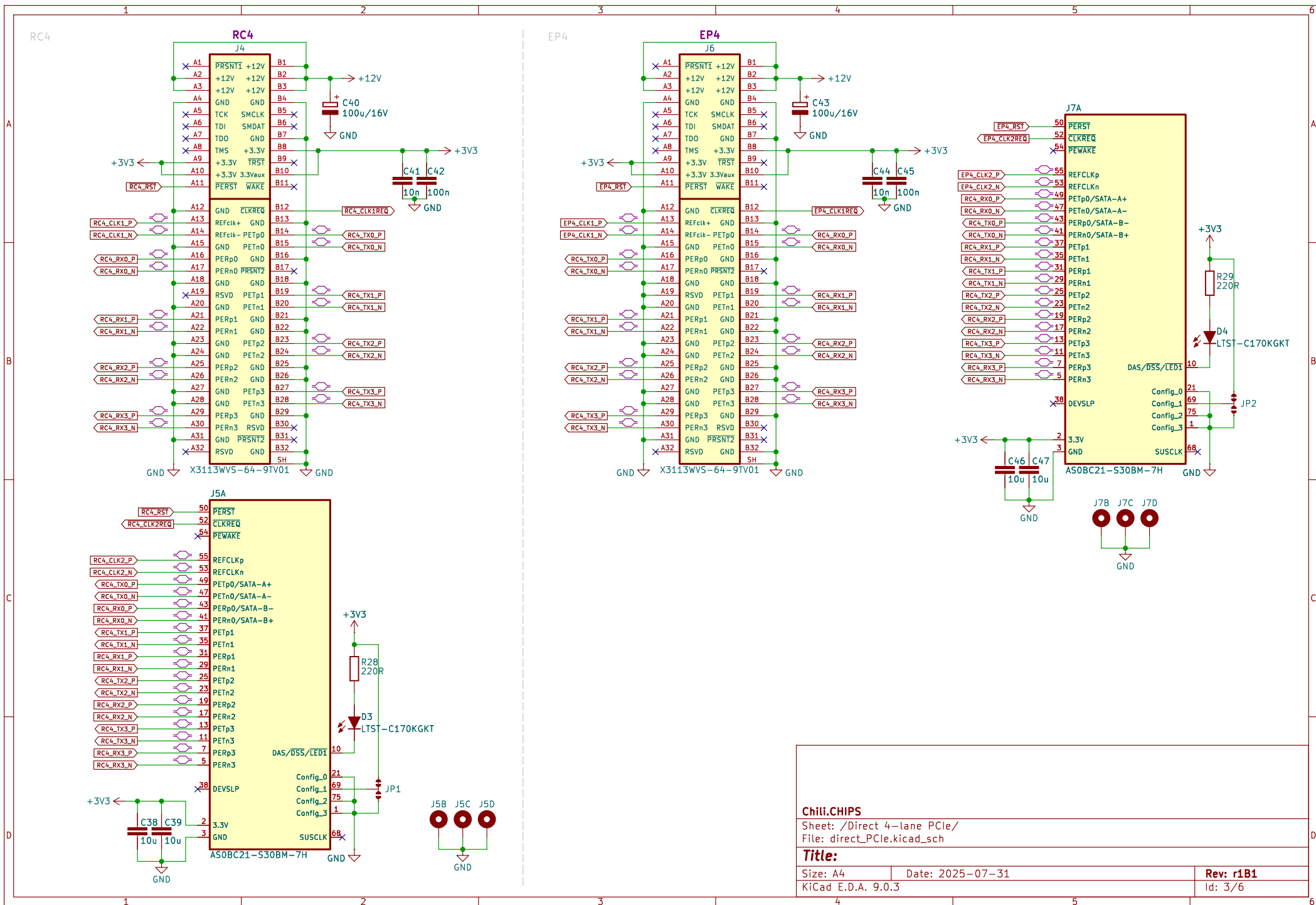
## Title:

Size: A4  
KiCad E.D.A. 9.0.3

Date: 2025-07-31

Rev: r1B1

Id: 2/6



# Chili.CHIPS

Sheet: /Direct 4-lane PCIe/  
File: direct\_PCE.kicad\_sch

## Title:

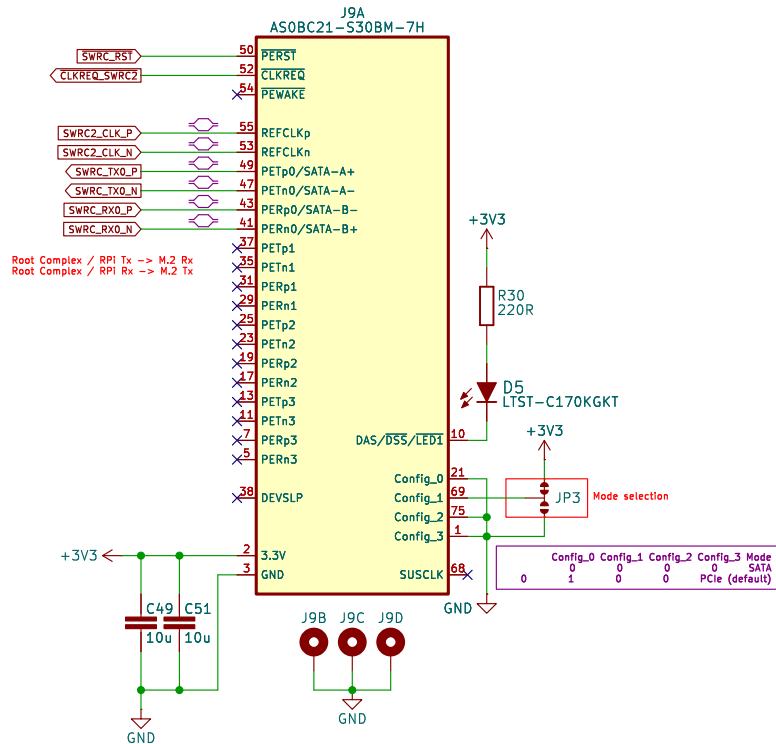
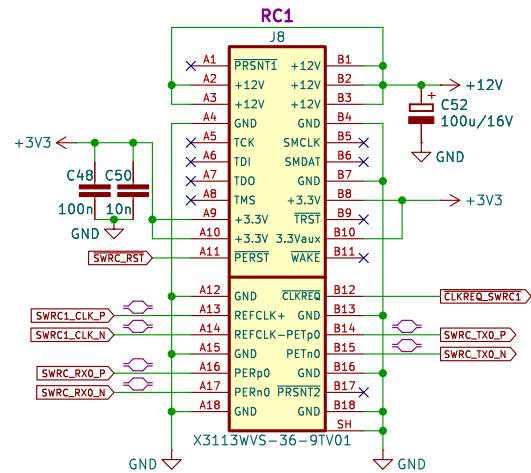
Size: A4  
KiCad E.D.A. 9.0.3

Date: 2025-07-31

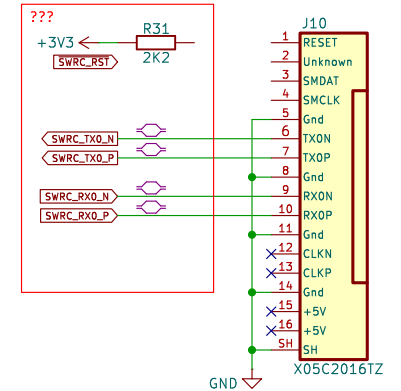
Rev: r1B1

Id: 3/6

1-lane PCIe for Root Complex



Raspberry Pi FPC 16-pin connector



#### 2.1. PCIe Signals

The PCIe signals are a single lane of PCIe Gen 2, including  $\overline{\text{CLKREQ}}$  and  $\text{RST}_B$  sideband signals which operate at 3.3V.

##### 2.1.1. Pwr\_en pin

This pin is a 3.3V output from the Raspberry Pi to a HAT+ or other add-on board, and signals to the HAT+ to power up any supplies. For example, in the instance of the Raspberry Pi M.2 M Key HAT+, this enables the M.2 3.3V power (which is generated from the Incoming 5V). Provide a 100K low pull on this pin on any HAT+.

##### 2.1.2. DeL\_wake pin

This pin is a 3.3V Input to the Raspberry Pi. Pull high to 3.3V either from a resistive divider from 5V (3k6/6k8 giving 2.35k output impedance), or from permanently enabled 3.3V (using a 2.2K resistor). The Raspberry Pi will detect this high pull at boot time, and will automatically probe the PCIe bus. Use the PCIe WAKE# to pull this low

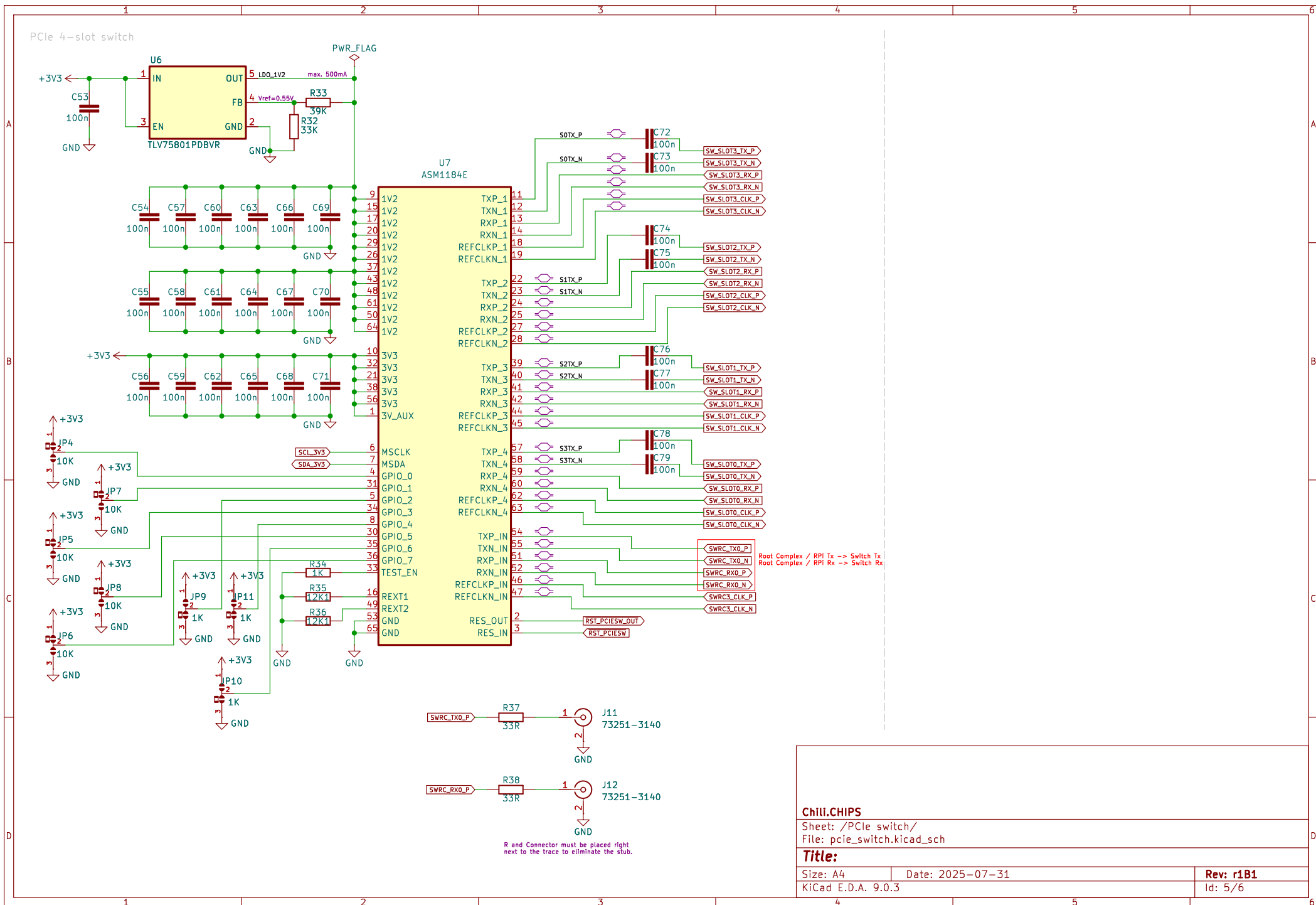
#### Chili.CHIPS

Sheet: /RC 1-lane and 2-lane PCIe/  
File: RC\_4-lanes-PCIe.kicad\_sch

#### Title:

Size: A4 Date: 2025-07-31  
KiCad E.D.A. 9.0.3

Rev: r1B1  
Id: 4/6



# Chili.CHIPS

Sheet: /PCle switch/  
File: pcie\_switch.kicad\_sch

## Title:

Size: A4  
KiCad E.D.A. 9.0.3

Date: 2025-07-31

Rev: r1B1

Id: 5/6

