Compa Family CPLDs Embedded Flash (EFlash) User Guide

(UG030006, V1.2)

(03.03.2020)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.2	03.03.2020	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
JTAG	Joint Test Action Group
SPI	Serial Peripheral Interface
I^2C	Inter-Integrated Circuit
APB	Advanced Peripheral Bus
CCS	Configuration Control System

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Chapter 1 Introduction

Compa Family CPLDs devices include an embedded Flash (EFlash) that can be used to store configuration information or provide general Flash storage space for the user. Embedded Flash has the following functions:

- Up to 5120 Kbits of storage space
- 1 page contains 2Kbits
- Less than 1μA leakage current
- 38ns read access time
- At least 100,000 programming/erasing cycles
- 32-bit data bus
- Supports JTAG, Slave I2C, Slave SPI, and APB interfaces
- +1.2V supply independently
- Operating Temperature Range (junction): -40℃ to 100℃

Table 1-1 Compa Family CPLDs EFlash Resources

Device	**EFLASH Capacity (Kbits)**
PGC1K	664
PGC2K	664
PGC4K	2560
PGC7K	3616
PGC10K	5120

Chapter 2 Function Description

2.1 User Programming Interfaces

Users can access Embedded Flash through JTAG, Slave I2C, Slave SPI, and APB interfaces.

2.1.1 JTAG Interface

The JTAG interface is shown in the following figure:

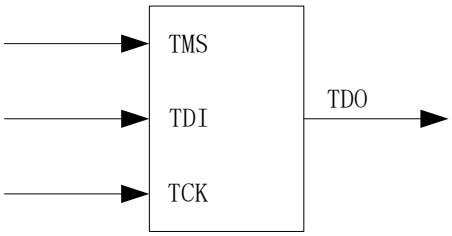

Figure 2-1 JTAG Interface Diagram

2.1.1.1 Port List

Table 2-1 List of JTAG Ports

Name	Direction	Description
TCK	Input	Test Clock input. TCK provides the clock for chip test logic
TMS	Input	Test Mode Select. Used to control the status switching of the test access port controller state machine on the rising edge of TCK to move test instructions and test data.
TDI	Input	Test Data In. Serial input pin. Used to move the test instructions into the instruction register and the test data into the test data register on the rising edge of TCK.
TDO	Output	Test Data Out. Serial output pin. During the instruction shift state, it is used to shift the test instructions out from the instruction register on the falling edge of the TCK signal. During the data shift state, it is used to shift out the test data stored in the test data register that is placed on the scan chain from TDI to TDO on the falling edge of the TCK signal.

2.1.1.2 Interface Timing

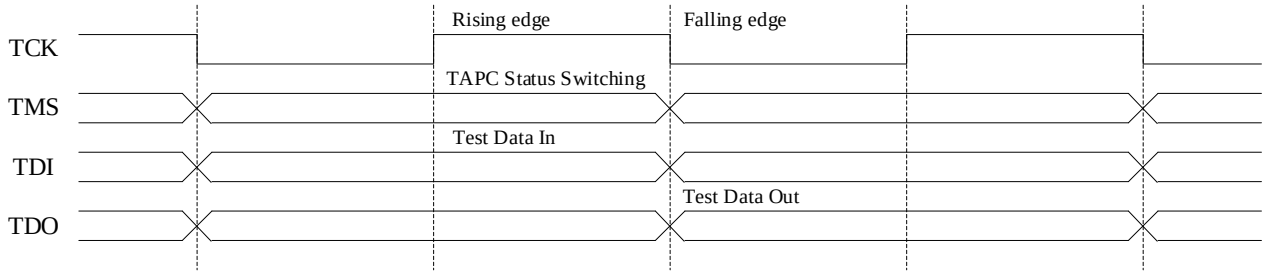

Figure 2-2 JTAG Interface Timing

2.1.1.3 Instruction Set

Table 2-2 JTAG Instruction Set

Instruction	**Op Code**	**Description**
BYPASS	1111111111	Bypass instruction
SAMPLE/PRELOAD	1010000000	Sample/preload instruction
EXTEST	1010000001	External test instruction
INTEST	1010000010	Internal test instruction
IDCODE	1010000011	Identification instruction
HIGHZ	1010000101	High-Z instruction
JRST	1010001010	Reset instruction
READ_UID	0101001100	Read-UID instruction
RDSR	0101011001	Read-Status-Register instruction
WADR	0101011010	Write-Address instruction
ERASE	0101011101	Erase instruction
ERASE_PAGE	0101011110	Page-Erase instruction
ERASE_CTL	0101011111	Control-Erase instruction
PROGRAM	0101100000	Program instruction
PROGRAM_CTL	0101100001	Program-Control instruction
READ	0101100010	Read instruction
READ_CTL	0101100011	Control-Read instruction
PROGRAM_LOCK	0101100100	Lock-Embedded-Flash instruction
READ_LOCK	0101100101	READ-Embedded-Flash-Lock-Flag instruction
EFlash_SLEEP	0101100110	Embedded-Flash-Sleep instruction
EFlash_WAKEUP	0101100111	Embedded-Flash-Wakeup instruction

2.1.2 Slave SPI Interface

Slave SPI interface is shown in the figure below.

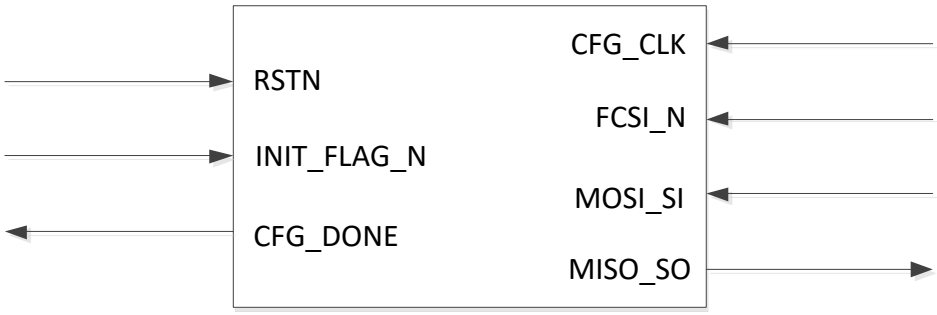

Figure 2-3 SPI Interface

2.1.2.1 Port List

Table 2-3 Slave SPI Port List

Name	Direction	Description
RSTN	Input	Reset pin; active-low
CFG_CLK	Input	Input clock, up to 100 MHz.
INIT_FLAG_N	Open-drain	It is a bidirectional open-drain pin indicating the completion of device initialization or a configuration error During configuration,if an error occurs, the pin is driven by the internal circuit to output a low level while feedbacking the pin's state to the inside of the chip.
CFG_DONE	Open-drain	It is a bidirectional open-drain pin that indicates configuration completion. 0: Compa Family CPLDs device not configured 1: Compa Family CPLDs device configured
FCSI_N	Input	Chip select input pin, active low.
MOSI_SI	Input	Data input pin, that carries output data from the external SPI master to Compa device
MISO_SO	Output	Data output pin, that carries output data from Compa device to the external SPI master

2.1.2.2 Instruction Set

Table 2-4 Slave SPI Instruction Set

Instruction	Description	Op Code
NOP	No Operation	FF
RDID	Read Identification	A1
RDSR	Read Status Register	A3
RDLOCK	Read Embedded Flash Lock Information	A5
WREN	Write Enable	51
WRDIS	Write Disable	52
RESET	Reset	60
ERASE	Erase Bulk	10

Instruction	Description	Op Code
ERASE_PAGE	Erase Page	11
ERASE_CTL	Erase Feature Control Page	12
PROGRAM	Program Page	20
READ	Read	30
READ_CTL	Read Feature Control Page	31
PROGRAM_LOCK	Lock Embedded Flash	40
EFlash_SLEEP	Embedded Flash Sleep	70
EFlash_WAKEUP	Embedded Flash Wake Up	71

2.1.3 Slave I^{2}C interface

The slave I^{2}C mode interface is as follows:

Figure 2-4 Slave I^{2}C Port Diagram

2.1.3.1 Port List

Table 2-5 Slave I^{2}C Port List

Name	Direction	Description
SCL	Input	Serial clock, with a maximum frequency of 400KHz
SDA	Input/Output	Serial Data

2.1.3.2 Interface Timing

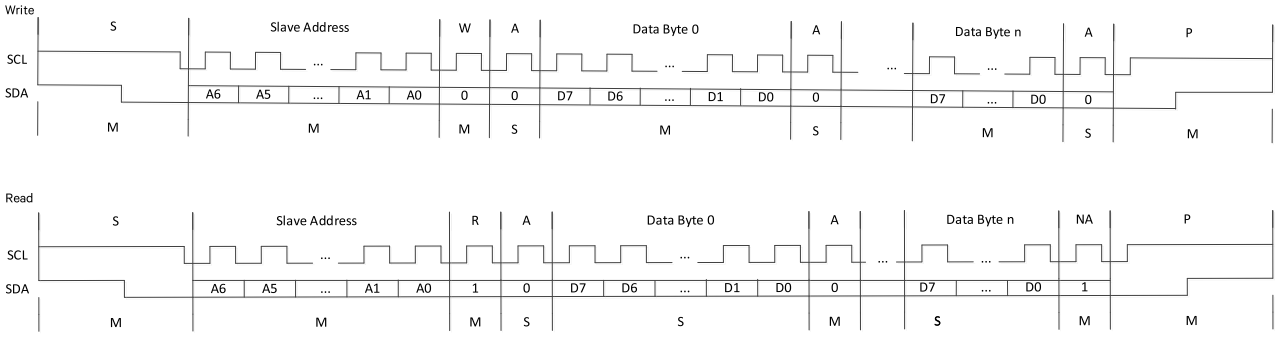

Figure 2-5 Slave I^{2}C Interface Timing

2.1.3.3 Instruction Set

Table 2-6 Slave I2C Instruction Set

Instruction	**Description**	**Op Code**
NOP	No Operation	FF
RDID	Read Identification	A1
RDSR	Read Status Register	A3
RDLOCK	Read Embedded Flash Lock Information	A5
WREN	Write Enable	51
WRDIS	Write Disable	52
RESET	Reset	60
ERASE	Erase Bulk	10
ERASE_PAGE	Erase Page	11
ERASE_CTL	Erase Feature Control Page	12
PROGRAM	Program Page	20
READ	Read	30
READ_CTL	Read Feature Control Page	31
PROGRAM_LOCK	Lock Embedded Flash	40
EFlash_SLEEP	Embedded Flash Sleep	70
EFlash_WAKEUP	Embedded Flash Wake Up	71

2.1.4 Internal Slave APB Interface

The internal slave APB interface is shown below:

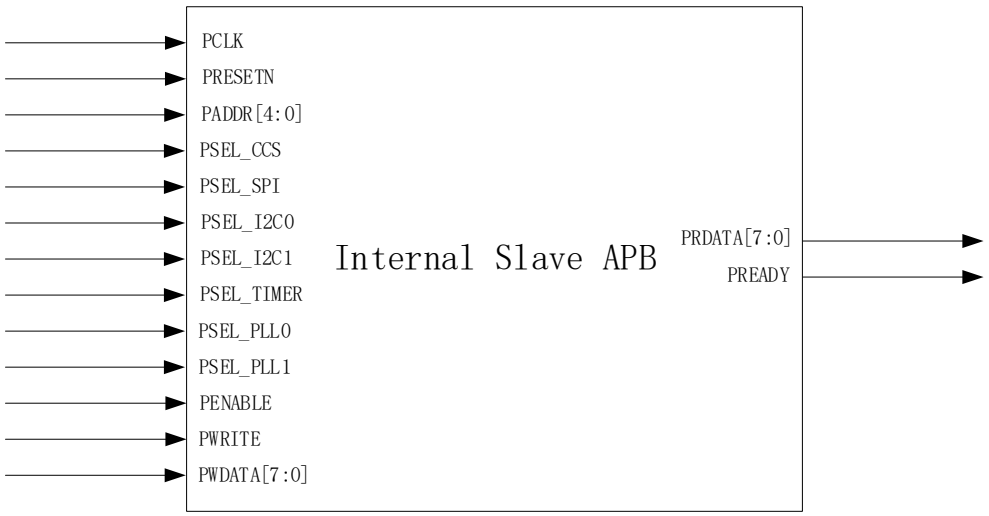

Figure 2-6 Internal Slave APB Interface

2.1.4.1 Port List

Table 2-7 Internal Slave APB Port List

Item	Direction	Description
pclk	Input	Clock, sampled on the rising edge
presetn	Input	Asynchronous reset, active low
paddr[4:0]	Input	Address Bus
psel	Input	Indicates that at the current moment, only 1 of the 7 slave devices can be selected, active high
penable	Input	Enable signal, indicating that the transmitted data is valid
pwrite	Input	Read and write enable 0: Read 1: Write
pwdata[7:0]	Input	Data bus input
prdata[7:0]	Output	Data bus output
pready	Output	Ready signal, indicating the end of a normal operation, active high

2.1.4.2 Interface Timing

Write without wait

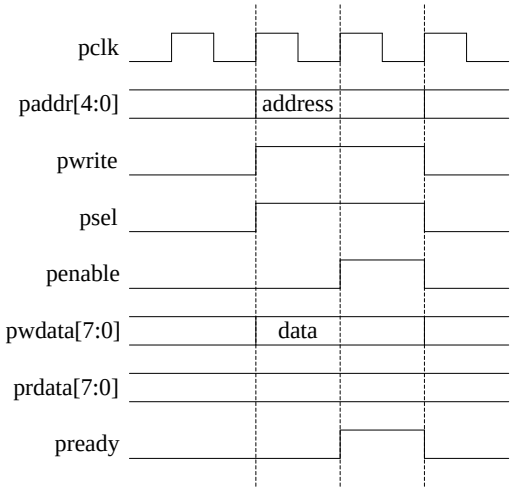

Figure 2-7 Write Without Wait

Write with wait

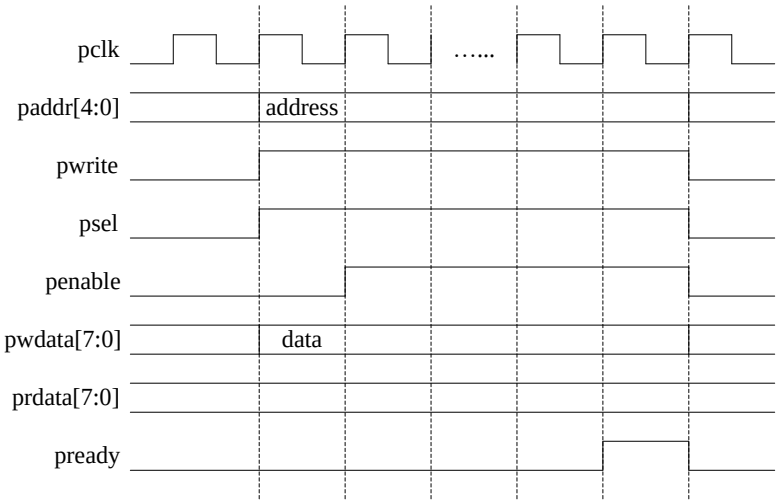

Figure 2-8 Write With Wait

Read without wait

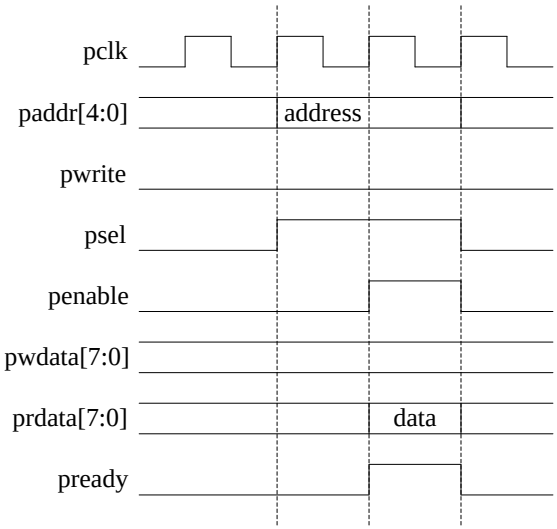

Figure 2-9 Read Without Wait

Read with wait

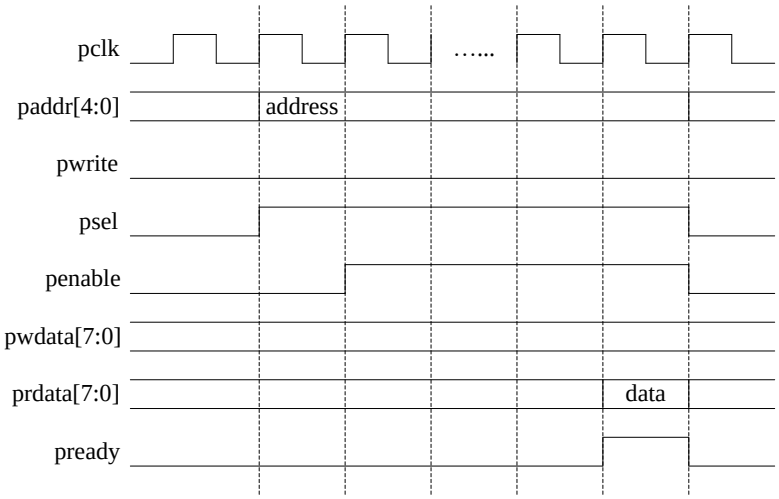

Figure 2-10 Read With Wait

2.1.4.3 Register

Table 2-8 Internal Slave APB Registers

Name	**R/W**	**Address**	**Description**
IDCODER0	R	00000	IDCODE Register 0
IDCODER1	R	00001	IDCODE Register 1
IDCODER2	R	00010	IDCODE Register 2
IDCODER3	R	00011	IDCODE Register 3
STATUSR0	R	10000	CCS Status Register 0
STATUSR1	R	10001	CCS Status Register 1
STATUSR2	R	10010	CCS Status Register 2
STATUSR3	R	10011	CCS Status Register 3
IRQCTLR	R/W	10100	Interrupt Control Register
CMDR	R/W	10101	Command register
ADR0	R/W	10110	Address Register 0
ADR1	R/W	10111	Address Register 1
ADR2	R/W	11000	Address Register 2
DATATR	W	11001	Data Transmit Registers
DATARR	R	11010	Data Receive Registers
STATUSR	R	11011	Status register
IRQSTATUSR	R	11100	Interrupt Status Registers
IRQR	R	11101	Interrupt Registers
LOCKRAR0	R	11110	Lock Page Register 0
LOCKRAR1	R	11111	Lock Page Register 1

2.2 EFlash Programming

The EFlash is integrated within the chip, supporting in-system programming. In-system programming includes direct in-system programming and indirect in-system programming.

Direct In-System Programming: Operations on the EFlash via JTAG, SPI, and I^2C interfaces.

Indirect In-System Programming: Operations on the EFlash through the internal slave APB interface with user logic. The input to user logic can be from JTAG, SPI interface, I2C interface or a user-defined interface. The user logic is to implement the interface conversion between APB and the interface mentioned above.

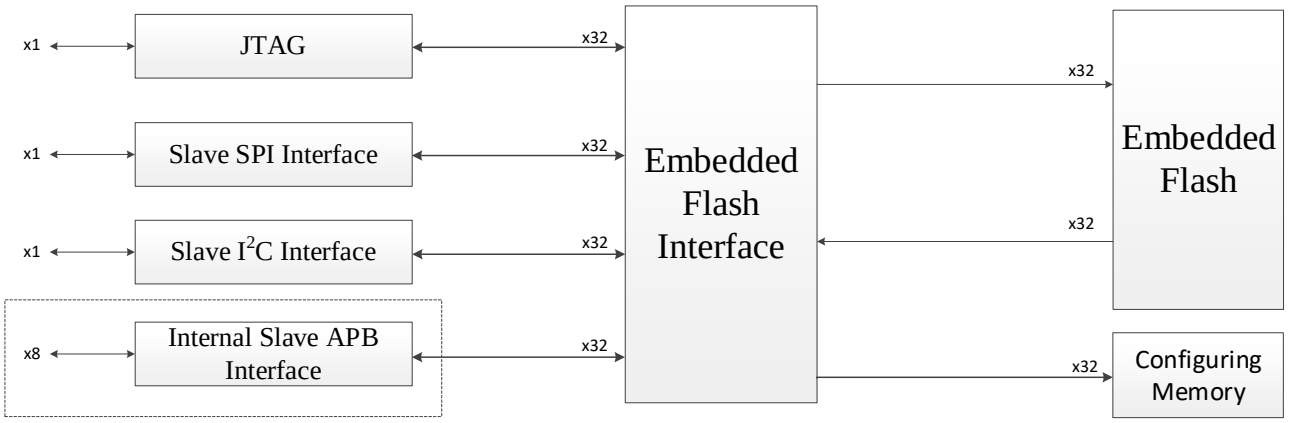

Figure 2-11 EFlash Programming Method

As shown in Figure 2-11, users operate the EFlash through the in-system programming method. When Master Self Configuration is enabled, bitstream stored in the EFlash can be downloaded into configuration register, then the device begins to work.

For the process of users operating the EFlash through in-system programming, refer to the document "***UG030004_Compa Family CPLDs Configuration User Guide*****".**

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