Logos2 Family 6G-SDI IP Reference Design Guide

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.0	28.07.2022	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
3G-SDI	SMPTE STANDARD, Source Image Format and Ancillary Data Mapping for the 3 Gb/s Serial Interface.
APB	Advanced Peripheral Bus
HD-SDI	SMPTE STANDARD, 1.5 Gb/s Signal/Data Serial Interface
HSSTHP	High Speed Serial Transceiver High Performance
SMPTE	The Society of Motion Picture and Television Engineers
SMPTE 165	RP 165 1994 Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television
SMPTE 168	RP 168 2002 Definition of Vertical Interval Switching Point for Synchronous Video Switching
SMPTE 292	ST 292- 1 2012 1.5 Gb/s Signal / Data Serial Interface
SMPTE 352	ST 352 2013 Payload Identification Codes for Serial Digital Interfaces
SMPTE 372	ST 372 2017 Dual Link 1.5 Gb/s Digital Interface for 1920 × 1080 and 2048 ×1080 Picture Formats
SMPTE 424	ST 424 2012 3 Gb/s Signal/Data Serial Interface
SMPTE 425	ST 425- 1 2017 Source Image Format and Ancillary Data Mapping for the 3 Gb/s Serial Interface
SMPTE 2081	ST 2081- 1 2015 6 Gb/s Signal / Data Serial Interface - Electrical
IPC	IP Compiler
PDS	Pango Design Suite

Related Documentation

The following documentation is related to this manual:

1. ***Pango_Design_Suite_Quick_Start_Tutorial***
2. ***Pango_Design_Suite_User_Guide***
3. ***IP_Compiler_User_Guide***
4. ***Simulation_User_Guide***
5. ***User_Constraint_Editor_User_Guide***
6. ***Physical_Constraint_Editor_User_Guide***
7. ***Route_Constraint_Editor_User_Guide***
8. ***UG050008_Titan2 Family FPGAs High-Speed Serial Transceiver (HSSTHP) User Guide***
9. ***UG051004_Titan2_HSSTHP_IP_UserGuide***

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Chapter 1 Preface

This chapter describes the scope, structure, and writing standards of this manual to help users quickly find the information they need.

1.1 Introduction of the Manual

This manual is a user guide for the 6G-SDI reference design launched by Pango Microsystems, applicable to PG2L100H FPGA products. This manual primarily includes the reference design user guide and related appendices. Users can use this manual to quickly understand the related features and usage methods related to the 6G-SDI reference design.

1.2 Writing Standards of the Manual

Table 1-1 Description of Writing Standards

Text	**Rules**
Attention	If users ignore the attention contents, they may suffer adverse consequences or fail to operate successfully due to incorrect actions.
Description	Instructions and tips provided for users.
Recommendation	Recommended settings and instructions for users.

Chapter 2 Reference Design User Guide

This chapter provides a guide on the use of 6G-SDI, including an introduction to IP, IP block diagram, IP generation process, Example Design, Example Design, IP interface description, IP register description, typical applications, descriptions and considerations, and IP debugging methods. More details on the design process can be found in the following PDS help documentation.

- Pango_Design_Suite_Quick_Start_Tutorial[1]
- Pango_Design_Suite_User_Guide[2]
- IP_Compiler_User_Guide[3]
- Simulation_User_Guide[4]

2.1 IP Introduction

6G-SDI IP is an IP provided by Pango Microsystems based on Logos2 FPGAs Family HSSTHP resources for transmitting videos in SMPTE format. Users can complete the configuration and usage of IP Module through the company's PDS (Pango Design Suite) development software and reference design.

2.1.1 Main Features

6G-SDI IP is designed according to SMPTE standards with the main features as follows.

2.1.1.1 Interface Rates

- SD-SDI (SMPTE 259) has an interface rate of 270 Mb/s;
- HD-SDI (SMPTE 292) has an interface rate of 1.485 Gb/s or 1.485/1.001 Gb/s;
- 3G-SDI[1](SMPTE 424&SMPTE 425, Level A) has an interface rate of 2.97 Gb/s or 2.97/1.001 Gb/s;
- 6G-SDI[2] (SMPTE 2081) has an interface rate of 5.94 Gb/s or 5.94/1.001 Gb/s;

[1] 3G-SDI only supports Level A, the same for below.

2.1.1.2 SDI Receiver

- Supports the SDI rate modes for automatic detection of received data;
- Supports dynamic switching of SD-SDI, HD-SDI, 3G-SDI, and 6G-SDI receive modes;
- Supports automatic detection of video transmission formats;
- Detects and captures SMPTE 352 (Payload ID) packets;
- In the HD-SDI, 3G-SDI, and 6G-SDI modes, checks for CRC errors;
- In the SD-SDI mode, optionally checks EDH (SMPTE 165) packet errors;
- Tolerates up to ±200 ppm frequency offset.

2.1.1.3 SDI Transmitter

- Supports dynamic switching of SD-SDI, HD-SDI, 3G-SDI, and 6G-SDI transmission modes;
- In the HD-SDI, 3G-SDI, and 6G-SDI modes, supports the rate of 1 or 1/1.001 times and times[3], but does not support mutual dynamic switching;
- Supports the generation and insertion of SMPTE 352 (Payload ID) packets;
- In the HD-SDI, 3G-SDI, and 6G-SDI modes, supports the generation and insertion of CRC and Line Numbers (LN);
- In the SD-SDI mode, supports optional generation and insertion of EDH (SMPTE 165) packets.

2.1.1.4 Video Format

Table 2-1 6G-SDI IP Supported Interface Protocols/Video Formats

Interface Protocols	**Video Standards**	**Sampling Structure/Bit Depth**	**Frame/Field Rate (Hz)**
SD-SDI SMPTE 259-C	PAL	4:2:2 Y'CB'CR' 10-bit or 8-bit	50
	NTSC	4:2:2 Y'CB'CR' 10-bit or 8-bit	59.94
HD-SDI SMPTE 292	SMPTE 274	4:2:2 Y'CB'CR' 10-bit	1080p[4]: 23.98, 24, 25, 29.97, 30 1080i[5]: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
	SMPTE 296	4:2:2 Y'CB'CR' 10-bit	720p: 23.98, 24, 25. 29.97, 30, 50, 59.94, 60
	SMPTE 260	4:2:2 Y'CB'CR' 10-bit	1035i: 59.94, 60
	SMPTE	4:2:2 Y'CB'CR' 10-bit	1080p: 23.98, 24, 25, 29.97, 30

[2] 6G-SDI supports Type 1 and Type 2, the same for below.

[3] For HD-SDI, 1 times rate indicates 1.485 Gb/s and 1/1.001 times rate indicates 1.485/1.001 Gb/s; for 3G-SDI, 1 times rate indicates 2.97 Gb/s and 1/1.001 times rate indicates 2.97/1.001 Gb/s; for 6G-SDI, 1 times rate indicates 5.94 Gb/s and 1/1.001 times rate indicates 5.94/1.001 Gb/s; the same for below.

[4] p: progressive, the same for below.

[5] i: interlaced, the same for below.

Interface Protocols	Video Standards	Sampling Structure/Bit Depth	Frame/Field Rate (Hz)
	2048-2		
3G-SDI Level A SMPTE 425-A	SMPTE 274	4:2:2 Y'CB'CR' 10-bit	1080p: 50, 59.94, 60
		4:4:4 Y'CB'CR' or RGB 10-bit 4:4:4:4 Y'CB'CR'A or RGBA 10-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
		4:4:4 Y'CB'CR' or RGB 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
		4:2:2 Y'CB'CR' 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
	SMPTE 296	4:4:4 or 4:4:4:4 Y'CB'CR' or RGB 10-bit	720p: 23.98, 24, 25. 29.97, 30, 50, 59.94, 60
	SMPTE 428-9	4:4:4 X'Y'Z' 12-bit	1080p: 24 1080PsF: 24
	SMPTE 428- 19	4:4:4 X'Y'Z' 12-bit	1080p: 25, 30 1080PsF: 25, 30
	SMPTE 2048-2	4:2:2 Y'CB'CR' 10-bit	1080p: 47.95, 48, 50, 59.94, 60
		4:4:4 Y'CB'CR' or RGB 10-bit 4:4:4:4 Y'CB'CR'A or RGBA 10-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
		4:4:4 Y'CB'CR' or RGB 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
		4:2:2 Y'CB'CR' 12-bit 4:2:2:4 Y'CB'CR'A 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
6G-SDI ST 2081- 1	SMPTE 2036- 1	4:2:2 Y'CB'CR' 10-bit	3840x2160p: 23.98/24/25/29.97/30
		4:2:0 Y'CB'CR' 10-bit	
	SMPTE 2048- 1	4:2:2 Y'CB'CR' 10-bit	4096x2160p: 23.98/24/25/29.97/30
	SMPTE 274	4:4:4 Y'CB'CR' or RGB 10-bit 4:4:4:4 Y'CB'CR'A or RGBA 10-bit	1920x1080p: 50/59.94/60
	SMPTE 2048-2	4:4:4 Y'CB'CR' or RGB 10-bit 4:4:4:4 Y'CB'CR'A or RGBA 10-bit	2048x1080p: 47.95/48/50/59.94/60
	SMPTE 274	4:4:4 Y'CB'CR' or RGB 12-bit	1920x1080p: 50/59.94/60
	SMPTE 2048-2	4:4:4 Y'CB'CR' or RGB 12-bit	2048x1080p: 47.95/48/50/59.94/60
	SMPTE 274	4:2:2 Y'CB'CR' 12-bit	1920x1080p: 50/59.94/60
	SMPTE 2048-2	4:2:2 Y'CB'CR' 12-bit	2048x1080p: 47.95/48/50/59.94/60
	SMPTE 2048-2	4:2:2:4 Y'CB'CR'A 12-bit	2048x1080p: 47.95/48/50/59.94/60
	SMPTE 2036- 1	4:2:2 Y'CB'CR' 12-bit 4:2:0 Y'CB'CR' 12-bit	3840x2160p: 23.98/24/25/29.97/30
	SMPTE 2048- 1	4:2:2 Y'CB'CR' 12-bit	4096x2160p: 23.98/24/25/29.97/30
	SMPTE 2048- 1	4:2:2:4 Y'CB'CR'A 12-bit	4096x2160p: 23.98/24/25/29.97/30

2.1.2 Applicable Devices and Packages

Table 2-2 6G-SDI IP Applicable Devices and Packages

Applicable Devices	Supported Package Type(s)
PG2L100H	ALL

2.2 IP Block Diagram

6G-SDI IP includes three parts: HSSTHP_SDI, SDI Core and APB Arbiter; the system block diagram is shown in Figure 2-1.

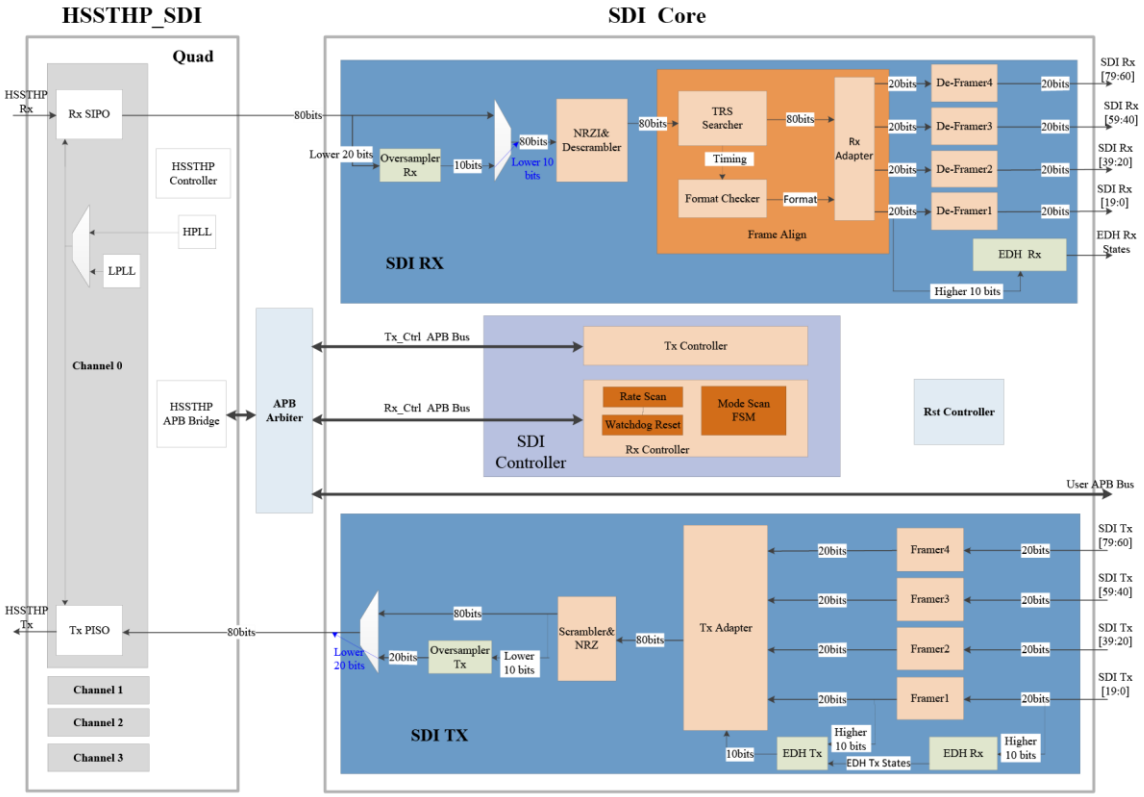

Figure 2-1 6G-SDI IP System Block Diagram

2.2.1 HSSTHP_SDI

HSSTHP_SDI is instantiated using Logos2 HSSTHP IP, including HSSTHP hard core resources, as well as HSSTHP Controller and HSSTHP APB Bridge soft core logic.

Attention:

For HSSTHP IP, please use the HSSTHP_SDI module included in the 6G-SDI IP reference design.

- HSSTHP Channel 0 is used as the SDI high-speed serial data transmission channel, only accomplishing data serial-to-parallel conversion and handling timing paths across clock domain without protocol encoding or decoding. The parallel data interface bit width is fixed at 80 bits; for the valid bit width under different SDI rate modes, please refer to Table 2-3; for optional external reference clock frequencies, please refer to Table 2-4.
- HSSTHP Controller performs HSSTHP power-up/reset and rate switching control.
- HSSTHPAPB Bridge controls the APB bus interface of HSSTHP.

Table 2-3 HSSTHP Channel 0 Valid Bit Widths

SDI Rate Mode	**Valid Bit Width Description**
SD-SDI	The lower 20 bits of Channel 0 are valid
HD-SDI	The lower 10 bits of Channel 0 are valid
3G-SDI	The lower 20 bits of Channel 0 are valid
6G-SDI	The lower 40 bits of Channel 0 are valid

Table 2-4 HSSTHP Optional External Reference Clock Frequency

SDI Rate Mode	**PLL**	**Optional external reference clock frequency**	**Description**
SD/HD/3G-SDI/6G	PLL0/PLL1	PLL_REF_CLK, PLL_REF_CLK/1.001[6]	The default value of PLL_REF_CLK is 148.5MHz.

2.2.2 SDI Core

SDI Core is a Soft Core resource, performing the following logic functions: Handles SDI reception and SDI transmission; serves as SDI controller and reset controller.

2.2.3 APB Arbiter

APB Arbiter is an APB bus arbitration module that uses a round-robin scheduling arbitration mechanism. Each bus group weighs 1/3, used to support Tx Controller APB, Rx Controller APB, and User APB to access HSSTHP_SDI simultaneously Bus Arbitration of Internal Registers.

In the Windows operating system, after the IP is generated, simulation can be run by double-clicking the "*.bat" file in the "<project_path>/sim/modelsim" directory. The file can run

[6] Logos2 PMA supports this frequency offset range. When the external reference clock selects this frequency, there is no need to change HSSTHP parameters, and the same applies below.

simulations using the simulation tool modelsim10.1a. When the simulation ends, the specific simulation results will be saved in the vsim.log file. The Modelsim simulation waveform is shown in Figure 2-2.

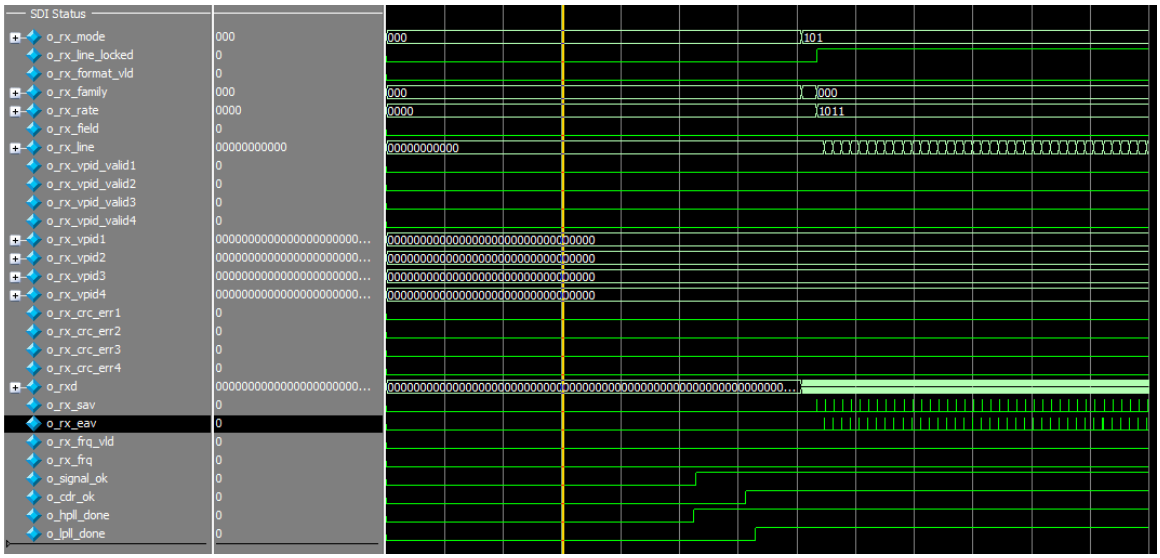

Figure 2-2 Modelsim Simulation Waveform

2.2.4 Synthesis and Placement/Routing

The specific usage of PDS synthesis tools and placement/routing tools can be found in the help documents within the PDS installation path.

Attention:

The "Example Design" project files .pds and the pin constraint files .fdc generated with the IP are located in the "/pnr/example_design".

Physical constraints must be adjusted according to the actual device used and the routing of the PCB board. For details, please refer to "2.6 Descriptions and Considerations".

2.2.5 Resource Utilization

For 6G-SDI typical resource utilisation values for IP based on applicable devices, please refer to Table 2-5.

Table 2-5 6G-SDI Typical Resource Utilisation Values for IP Based on Applicable Devices

	Configuration Mode	Typical Resource Utilisation Values			
		LUT	FF	HSSTLP	USCM
PG2L100H	Tx/Rx Maximum Line Rate: 6G-SDI Tx EDH Feature: Enabled Rx EDH Feature: Enabled	3184	3106	1	3

2.3 Example Design

This section mainly introduces the Example Design scheme based on 6G-SDI IP. This scheme instantiates a 6G-SDI IP, sends and receives data via self-loop, and tests video data transmission under different SDI rate modes. The host computer interacts with the test board through serial port communication to control the IP operating mode as well as configure different transmitted video data and receive the returned detection information.

2.3.1 Design Block Diagram

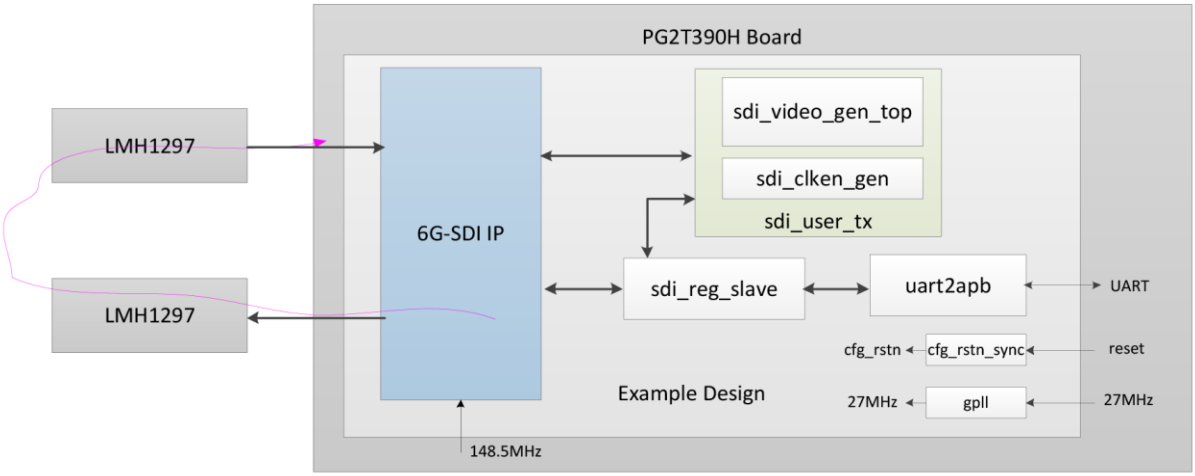

Figure 2-3 Example Design System Block Diagram

The Example Design system block diagram, as shown in Figure 2-3, uses the P04W100AS101_A0 single board as the upper board scheme. It incorporates the serial differential/single-ended conversion relay board (LMH1297) in a loopback configuration. Users need to modify the design according to actual conditions.

The Example Design top-level integrates 6G-SDI IP, sdi_user_tx, sdi_reg_slave, uart2apb, Cfg_rstn_sync, and gpll_100m modules.

2.3.2 Interface Description

The interface descriptions of the Example Design are shown in Table 2-6.

Table 2-6 Example Design Interface List

Port	I/O	Bit width	Description	Pin constraints
i_clk_27m	I	1	External input clock (with a frequency of 27 MHz)	AB27
i_hsst_refclk_n	I	1	HSSTHPPLL differential reference clock N side	-
i_hsst_refclk_p	I	1	HSSTHPPLL differential reference clock P side	-
i_cfg_rstn	I	1	External input system reset (active-low)	AB30
i_uart_rxd	I	1	Serial port input (connected to the data transmitting port of the host computer)	AF28
o_uart_txd	O	1	Serial port output (connected to the data receiving port of the host computer)	AE28
o_p_tx_sdn	O	1	HSSTHP TX differential interface N side	-
o_p_tx_sdp	O	1	HSSTHP TX differential interface P side	-
i_p_rx_sdn	I	1	HSSTHP RX differential interface N side	-
i_p_rx_sdp	I	1	HSSTHP RX differential interface P side	-
o_gpll_lock	O	1	gpll_ 100m LOCK indicator 1: GPLL LOCK achieved 0: GPLL LOCK unachieved	AB29

Note: "- " indicates the location constraint has been applied through HSSTHP-related constraints.

2.3.3 Module Description

2.3.3.1 6G-SDI IP Module

This section includes three parts: HSSTHP_SDI, SDI Core, and APB Arbiter.

2.3.3.2 sdi_user_tx Module

This section includes two submodules: sdi_clken_gen and sdi_video_gen_top. sdi_clken_gen generates, based on the SDI rate mode, corresponding clock enable signal. sdi_video_gen_top generates, based on the SDI rate mode, corresponding formatted colorbars video content. For video formats generated in different SDI rate modes, refer to Table 2-7.

Table 2-7 sdi_video_gen_top Module Generated Video Format Description

SDI Rate Mode	Video Format
SD-SDI	625i 50Hz
HD-SDI	1080p 30Hz

SDI Rate Mode	Video Format
3G-SDI	1080p 60Hz
6G-SDI	2160p 30Hz

2.3.3.3 sdi_reg_slave Module

Custom register module used for debugging. For relevant register descriptions, please refer to Table 2-8.

Table 2-8 sdi_reg_slave Register Description

Register address[7] (16bit)	R/W	Description	Reset value (32 bit)
0x8001	W	bit[31:9]: 23'b 0 bit[8]: Receiver reset configuration 1'b 0: Reset (default) 1'b 1: Reset release bit[7:5]: 3'b 0 bit[4]: Transmitter reset configuration 1'b 0: Reset (default) 1'b 1: Reset release bit[3:1]: 3'b 0 bit[0]: General reset configuration 1'b 0: Reset (default) 1'b 1: Reset release	0x00000111
0x8002	W	bit[31:21]: 11'b 0 bit[20]: Transmitter 6G-Type2 enable configuration 1'b 0: Disabled (default) 1'b 1: Enabled bit[19:9]: 11'b 0 bit[8]: Transmitter line number value insertion configuration 1'b 0: Do not insert line number values after eav 1'b 1: Insert line number values (default) bit[7:5] after eav: 3'b 0 bit[4]: Transmitter CRC enable configuration 1'b 0: Disabled 1'b 1: Enabled (default) bit[3]: 1'b 0 bit[2:0]: Transmitter rate mode configuration 3'b 100: 6G-SDI 3'b 010: 3G-SDI (default) 3'b 001: HD-SDI 3'b 000: SD-SDI	0x00001112

[7] Only supports access to the register addresses listed in Table 2-8. Accessing other register addresses may cause logical errors.

Register address[7] (16bit)	R/W	Description	Reset value (32 bit)
0x8008	W	bit[31:3]: 29'b 0 bit[2:0]: Configuration of video transmission format at the transmitter. In the 6G-SDI rate mode, the configured format is the format of the Sub Image. 3'b 001: 1080p (default) 3'b 010: 1080i 3'b 011: 720p 3'b 100: 1035i 3'b 101: 625i Others: 525i	0x00000001
0x9000	R	bit[31:19]: Not used bit[18]: Detection indicator of the receiver frequency type 1'b 1: 1/1.001 times rate 1'b 0: 1 times rate bit[17]: Lock indicator for receiving image Frame on the receiver 1'b 1: Locked 1'b 0: Unlocked bit[16]: Indicates whether the video data received by the receiver is valid 1' b 1: Valid 1'b 0: Invalid bit[15]: HSSTHPP_RX_SIGDET_STATUS pass-through signal (asynchronous signal) 1'b 1: HSSTHP high-speed serial input signal detected 1'b 0: HSSTHP high-speed serial input signal not detected bit[14]: HSSTHP CDR ALIGN pass-through signal (asynchronous signal) 1'b 1: HSSTHP CDR input signal locked 1'b 0: HSSTHP CDR input signal unlocked bit[13]: Resistor calibration complete indicator 1'b 1: Resistor calibration complete 1'b 0: Resistor calibration incomplete bit[12]: HSSTHP LPLL LOCK indicator 1'b 1: LOCK achieved 1'b 0: Indicates reset or LOCK not achieved. bit[11]: HSSTHPHPLL LOCK indicator 1'b 1: LOCK achieved 1'b 0: Indicates reset or LOCK not achieved. bit[10]: Indicates that receiver channel 2 receives 352 packets 1'b 1: 352 packets available 1'b 0: No 352 packets bit[9]: Indicates that receiver channel 4 receives 352 packets 1'b 1: 352 packets available 1'b 0: No 352 packets bit[8]: Indicates that receiver channel 6 receives 352 packets 1'b 1: 352 packets available 1'b 0: No 352 packets bit[7]: Indicates that receiver channel 8 receives 352 packets 1'b 1: 352 packets available 1'b 0: No 352 packets bit[6]: Indicates presence of CRC errors in receiver channels 1 or 2 1'b 1: CRC error present 1'b 0: No CRC error bit[5]: Indicates presence of CRC errors in receiver channels 3 or 4 1'b 1: CRC error present 1'b 0: No CRC error bit[4]: Indicates presence of CRC errors in receiver channels 5 or 6	0x00000000

Register address[7] (16bit)	R/W	Description	Reset value (32 bit)
		1'b 1: CRC error present 1'b 0: No CRC error bit[3]: Indicates presence of CRC errors in receiver channels 7 or 8 1'b 1: CRC error present 1'b 0: No CRC error bit[2]: Indicates whether receiver o_rx_frq is valid 1'b 1: Detection complete 1'b 0: Detection incomplete bit[1:0]: Not used	
0x9001	R	bit[31:21]: Not used bit[20]: Receiver 6G-Type2 indicator 1'b 0: 6G-Type1 1'b 1: 6G-Type2 bit[19]: Not used bit[18:16]: Rate mode received by the receiver 3'b 100: 6G-SDI 3'b 010: 3G-SDI 3'b 001: HD-SDI 3'b 000: SD-SDI bit[15]: Not used bit[14:12]: Video transmission format received by the receiver (refer to Table 2-12)bit[11:8]: Video transmission frame rate received by the receiver (refer to Table 2-13)bit[7:5]: Not used bit[4]: Video scan format received by the receiver 1'b 1: Interlaced 1'b 0: Progressive bit[3:0]: Not used	0x00000000

2.3.3.4 uart2apb Module

A serial port module used for debugging, for receiving UART data with a fixed baud rate of 115200, outputting in data formats required by the APB protocol. For read and write operations, the address width is 24 bits, and the data width is 32 bits. The read and write operations are described as below:

- Read operation format: "0x72 " + "Address";
- Write operation format: Write operation format: "0x77" + "address" + "data".

For examples of related read and write operations, please refer to "2.6.6 uart2apb Module Read/Write Operation Example".

2.3.3.5 cfg_rstn_sync Module

External input reset signal, synchronized with a 27 MHz clock.

2.3.3.6 GPLL Module

It generates a 27 MHz clock from an external input clock.

2.3.4 Test Method

In the Example Design, the user sends serial port commands via the host computer and writes values to the register of the sdi_reg_slave module to configure the 6G-SDI IP; it receives serial port information via the host computer to read register values of the sdi_reg_slave module to monitor the IP reception status. For the register description of sdi_reg_slave module, refer to Table 2-8.

Take the P05W100AS01_A0 test board loopback test as an example; for serial port transmission and reception data, please refer to Table 2-9. The following test can be performed: the data format at the transmitter is configured as 6G-SDI 3840x2160p 30Hz and the data format at the receiver as 6G-SDI 3840x2160p 30Hz.

Table 2-9 Example Design Serial Port Data Transmission and Reception Description

Steps	**Serial port transmitted data**	**Serial port received data**	**Description**
Step 1	7701800000000111 7702800000001115 7707800000000005 7708800000000001	-	1) The host computer sends each row of data in the serial port transmitted data column, one by one through the serial port to the test board, to perform write register operations. 2) No serial port received data.
Step 2	72009000 72019000	0003F80600050B00	1) The host computer sends each row of data in the serial port transmitted data column, one by one through the serial port to the test board, to perform read register operations. 2) The data values in the serial port received data column indicate that the received image Frame is locked at the receiver, and the data format is as expected.

Note: "- " means no serial port received data.

Attention:

Do not directly use the Example Design generated by the IP for Flow on-board testing. Constrain pins according to the actual pin connections of the single board, and then proceed with Flow on-board testing.

2.3.5 Example Simulation

In the Windows system, after IP generation, double-click the "*.bat"file [8] under the "<project_path>/sim/modelsim" path to run simulation.

2.4 IP Interface Description

This section provides the 6G-SDI IP related interface instructions and timing descriptions.

2.4.1 Interface Description

For 6G-SDI IP top-level interface description, please refer to Table 2-10. For bit definitions of client-side data interface and description of valid bit width, please refer to Table 2-11.

Table 2-10 6G-SDI IP Interface Signal List

Port	I/O	Bit width	Description
Clock Interface			
i_free_clk	I	1	free_clk interface provided by user.
i_pll_refclk_p(n)	I	1	HSSTHPPLL reference clock.
o_tx_clk	I	1	sdi_tx_clk clock domain output port.
o_rx_clk	I	1	sdi_rx_clk clock domain output port.
Reset interface(If not otherwise specified, all are in free_clk clock domain)			
i_rstn	I	1	For 6G-SDI IP global logic reset input (active-low), please refer to "2.6.4 IP Reset Scheme".
i_tx_rstn	I	1	For 6G-SDI IP TX logic reset input (active-low), please refer to "2.6.4 IP Reset Scheme".
i_rx_rstn	I	1	For 6G-SDI IP RX logic reset input (active-low), please refer to "2.6.4 IP Reset Scheme".
i_cfg_rstn	I	1	For the logic reset input of HSSTHP APB Bridge and APB Arbiter (active-low), please refer to"2.6.4 IP Reset Scheme".
o_tx_rstn	O	1	For 6G-SDI IP TX reset signal output (active-low), please refer to "2.6.4 IP Reset Scheme"; sdi_tx_clk clock domain signal.
o_rx_rstn	O	1	For 6G-SDI IP RX reset signal output (active-low), refer to "2.6.4 IP Reset Scheme"; sdi_rx_clk clock domain signals.
APB bus interface (all within free_clk clock domain)			
i_cfg_psel	I	1	HSSTHP_SDIAPB interface.
i_cfg_enable	I	1	
i_cfg_write	I	1	
i_cfg_addr	I	16	
i_cfg_wdata	I	8	
o_cfg_rdata	O	8	

[8] For IP-generated output files, please refer to Error! Reference source not found.

Port	I/O	Bit width	Description
o_cfg_int	O	1	
o_cfg_ready	O	1	
HSSTHP differential interface			
o_p_tx_sdn	O	1	HSSTHP TX differential interface N side.
o_p_tx_sdp	O	1	HSSTHP TX differential interface P side.
i_p_rx_sdn	I	1	HSSTHP RX differential interface N side.
i_p_rx_sdp	I	1	HSSTHP RX differential interface P side.
SDI TX client-side interface (unless otherwise noted, all are sdi_tx_clk clock domain signals)			
i_tx_ce	I	1	Transmitter clock enable The timing requirements of SD-SDI mode are shown in Figure 2-6; The timing requirements of HD-SDI and 6G-SDI Type 2 modes are shown in Figure 2-7; In other modes, i_tx_ce should always be "1". For more details, please refer to "2.4.2.2 Clock Enable Signal Timing".
i_tx_mode	I	3	Transmission mode configuration, free_clk clock domain signal. 000: SD; 001: HD; 010: 3G; 100: 6G; Others: Reserved.
i_tx_level_b_en	I	1	Configuration of the transmitter transmission type, only valid for 6G-SDI mode; for other modes, always inputs "0" with static configuration[9]. 1: 6G-SDI Type 2; 0: 6G-SDI Type 1.
i_tx_crc_en	I	1	Transmitter CRC insertion enable, valid only for HD-SDI, 3G-SDI, and 6G-SDI modes; for other modes, always inputs "0" with static configuration. 1: Automatically insert CRC; 0: Pass through the corresponding field data.
i_tx_ln_en	I	1	Transmitter Line Numbers insertion enable, valid only for HD-SDI, 3G-SDI, and 6G-SDI modes; for other modes, always inputs "0" with static configuration. 1: Automatically insert Line Numbers; 0: Pass through the corresponding field data.
i_tx_vpid_en	I	1	Transmitter ST 352 packet insertion enable, static configuration. 1: Automatically insert ST 352 packets; 0: Pass through the corresponding field data.
i_tx_edh_en	I	1	Transmitter EDH packet insertion enable, valid only for SD-SDI mode; for other modes, always inputs "0" with static configuration. 1: Automatically insert EDH packets; 0: Pass through the corresponding field data. When instantiating the IP, check [Enable Tx EDH Feature] to make this port visible.
i_txd	I	80	The transmitted video data stream contains information

[9] Static configuration: Only supports changes before logical reset release, the same for below.

Port	I/O	Bit width	Description
			such TRS/SAV/EAV. Please refer to Table 2-11 for bit definitions and Figure 2-4 for timing.
i_tx_line1	I	11	Channels[10] 1&2 Send Line Numbers.Please refer to Figure 2-4 for timing.
i_tx_line2	I	11	Channels 3&4 transmit Line Numbers. Please refer to Figure 2-4 for timing.
i_tx_line3	I	11	Channels 5&6 transmit Line Numbers. Please refer to Figure 2-4 for timing.
i_tx_line4	I	11	Channels 7&8 transmit Line Numbers. Please refer to Figure 2-4 for timing.
i_tx_vpid1	I	32	Channel 2 transmits ST 352 packets. Please refer to Figure 2-4 for timing.
i_tx_vpid2	I	32	Channel 4 transmits ST 352 packets. Please refer to Figure 2-4 for timing.
i_tx_vpid3	I	32	Channel 6 transmits ST 352 packets. Please refer to Figure 2-4 for timing.
i_tx_vpid4	I	32	Channel 8 transmits ST 352 packets. Please refer to Figure 2-4 for timing.
i_tx_vpid_line_f1	I	11	For Insertion position of the ST 352 packet's Line Numbers on the transmitter (field 1), please refer to i_tx_vpid_line_f2_en, static configuration.
i_tx_vpid_line_f2	I	11	For Insertion position of the ST 352 packet's Line Numbers on the transmitter (field 2), please refer to i_tx_vpid_line_f2_en, static configuration.
i_tx_vpid_line_f2_en	I	1	i_tx_vpid_line_f2 valid indicator, static configuration. 1: i_tx_vpid_line_f1 and i_tx_vpid_line_f2 are both valid 0: only i_tx_vpid_line_f1 is valid
o_tx_ce_err	O	1	i_tx_ce signal is an indicator of whether timing requirements are met, used in SD-SDI, HD-SDI , and 6G-SDI Type 2 modes; for other modes, always outputs "0". 1: i_tx_ce signal does not meet timing requirements; 0: i_tx_ce signal meets timing requirements.
o_tx_sd_switch	O	1	Check if the transmitted SD-SDI data stream has switching (SMPTE RP168); valid only in SD-SDI mode; for other modes, always outputs "0". 1: transmitted SD-SDI data stream undergoes switching; 0: transmitted SD-SDI data stream does not undergo switching. When instantiating the IP, check [Enable Tx EDH Feature] to make this port visible.
SDI RX client-side interface (unless otherwise noted, all are sdi_rx_clk clock domain signals)			
o_rx_ce	O	1	Capture clock enable, used for SD-SDI, HD-SDI and 6G-SDI Type2 modes; for other modes, always outputs "1".
i_rx_mode	I	3	Receive mode detection configuration, free_clk clock domain signal. 000: Force SD-SDI; 001: Force HD-SDI; 010: Force 3G-SDI; 100: Force 6G-SDI;

[10] Channels: The lower 10 bits of the 20 bits of Framer1/De-Framer1 are defined as channel 1 and the upper 10 bits are defined as channel 2;the lower 10 bits of the 20 bits of Framer2/De-Framer2 are defined as channel 3 and the upper 10 bits are defined as channel 4; thelower 10 bits of the 20 bits of Framer3/De-Framer3 are defined as channel 5 and the upper 10 bits are defined as channel 6; the lower 10 bits of the 20 bits of the Framer4/De-Framer4 are defined as channel 7 and the upper 10 bits are defined as channel 8. The same for below.

Port	I/O	Bit width	Description
			111: Auto-detect SDI mode.
o_rx_mode	O	I	Received data Mode. 000: SD-SDI; 001: HD-SDI; 010: 3G-SDI; 100: 6G-SDI; Others: Reserved.
o_rx_line_locked	O	1	Indicator for received image Frame lock. 1: Locked; 0: Unlocked.
o_rx_format_vld	O	1	Indicates whether the received video data is valid; refer to the specific port description. It is valid only when o_rx_line_locked=1. 1: Valid; 0: Invalid.
o_rx_family	O	3	Format of the received video transmission; please refer to Table 2-12. It is valid only when o_rx_format_vld=1.
o_rx_rate	O	4	Frame rate of the received video transmission; refer to Table 2-13. It is valid only when o_rx_format_vld=1, it needs to be determined together with o_rx_frq whether there is a 1/1.001 relationship.
o_rx_frq_vld	O	1	o_rx_frq valid indicator, valid only when o_rx_format_vld=1; free_clk clock domain signal. 1: Detection complete; 0: Detection incomplete.
o_rx_frq	O	1	Valid only when o_rx_frq_vld=1, indicating the type of received frequency; free_clk clock domain signal. 1: The data is received at a rate of 1/1.001 times; 0: The data is received at a rate of 1 times.
o_rx_field	O	1	Received video scan format, valid only when o_rx_format_vld=1. 1: Interlaced; 0: Progressive.
o_rx_level_b_ind	O	1	Received transmission type indicator, valid only in 6G-SDI mode; always outputs "0" in other modes. 1: 6G-SDI Type 2; 0: 6G-SDI Type 1.
o_rx_line1	O	11	Line Numbers received by channels 1&2, valid only in HD-SDI, 3G-SDI, and 6G-SDI modes and only when o_rx_format_vld=1; always outputs "0" in other modes.
o_rx_line2	O	11	Line Numbers received by channels 3&4, valid only in 6G-SDI mode and only when o_rx_format_vld=1; always outputs "0" in other modes.
o_rx_line3	O	11	Line Numbers received by channels 5&6, valid only in 6G-SDI (Type 2) mode and only when o_rx_format_vld=1; always outputs "0" in other modes.
o_rx_line4	O	11	Line Numbers received by channels 7&8, valid only in 6G-SDI (Type 2) mode and only when o_rx_format_vld=1; always outputs "0" in other modes.
o_rx_vpid_valid1	O	1	Indicates whether the ST 352 packet received by channel 2 is valid and only when o_rx_format_vld=1. 1: Channel 2 ST 352 packet is valid; 0: Channel 2 ST 352 packet is invalid.
o_rx_vpid1	O	32	ST 352 packet received by channel 2 , only valid when o_rx_vpid_valid1=1.
o_rx_vpid_valid2	O	1	Indicates whether the ST 352 packet received by channel 4 is valid and only valid in 6G-SDI mode and when

Port	I/O	Bit width	Description
			o_rx_format_vld=1 ; always outputs "0" in other modes. 1: The ST 352 packet received by Channel 4 is valid; 0: The ST 352 packet received by Channel 4 is invalid.
o_rx_vpid2	O	32	ST 352 packet received by channel 4 , only valid when o_rx_vpid_valid2=1.
o_rx_vpid_valid3	O	1	Indicates whether the ST 352 packet received by channel 6 is valid and only valid in 6G-SDI (Type 2) mode and when o_rx_format_vld=1 ; always outputs "0" in other modes. 1: The ST 352 packet received by Channel 6 is valid; 0: The ST 352 packet received by Channel 6 is invalid.
o_rx_vpid3	O	32	ST 352 packet received by channel 6 , only valid when o_rx_vpid_valid3=1.
o_rx_vpid_valid4	O	1	Indicates whether the ST 352 packet received by channel 8 is valid and only valid in 6G-SDI (Type 2) mode and when o_rx_format_vld=1 ; always outputs "0" in other modes. 1: The ST 352 packet received by Channel 8 is valid; 0: The ST 352 packet received by Channel 8 is invalid.
o_rx_vpid4	O	32	ST 352 packet received by channel 8, only valid when o_rx_vpid_valid4=1
o_rx_crc_err1	O	1	Indicates Channels 1&2 received CRC error, valid only in HD-SDI, 3G-SDI, and 6G-SDI modes; always outputs "0" in other modes. 1: Channel 1 or Channel 2 has CRC errors; 0: Channel 1 or Channel 2 has no CRC error;
o_rx_crc_err2	O	1	Indicates Channels 3&4 received CRC error, only valid in 6G-SDI mode; always outputs "0" in other modes. 1: Channel 3 or Channel 4 has CRC errors; 0: Channel 3 or Channel 4 has no CRC error;
o_rx_crc_err3	O	1	Indicates Channels 5&6 received CRC error, only valid in 6G-SDI (Type 2) mode; always outputs "0" in other modes. 1: Channel 5 or Channel 6 has CRC errors; 0: Channel 5 or Channel 6 has no CRC error;
o_rx_crc_err4	O	1	Indicates channels 7&8 received CRC error, only valid in 6G-SDI (Type 2) mode; always outputs "0" in other modes. 1: Channel 7 or Channel 8 has CRC errors; 0: Channel 7 or Channel 8 has no CRC error;
o_rxd	O	80	Received video data stream, only valid when o_rx_format_vld=1. Please refer to Table 2-11 for bit definitions and Figure 2-5 for timing.
o_rx_eav	O	1	Indicates the position of EAV field XYZ word, only valid when o_rx_format_vld=1; please refer to Figure 2-5. 1: Indicates it is the EAV XYZ word; 0: Indicates it is not the EAV XYZ word.
o_rx_sav	O	1	Indicates the position of SAV field XYZ word, only valid when o_rx_format_vld=1. 1: Indicates it is the SAV XYZ word; 0: Indicates it is not the SAV XYZ word.
o_rx_sd_switch	O	1	Detect whether the received SD-SDI data stream has switching (SMPTE RP168), only valid in SD-SDI mode; always outputs "0" in other modes. 1: The received SD-SDI data stream undergoes switching; 0: The received SD-SDI data stream does not under goes

Port	I/O	Bit width	Description
			switching. When instantiating IP, check [Enable Rx EDH Feature] to make this port visible.
o_rx_edh_ap_crc_err	O	1	Indicates an Active Picture CRC error in the received EDH packet, only valid in SD-SDI mode; always outputs "0" in other modes. 1: The received EDH packet has an Active Picture CRC error; 0: The received EDH packet has no Active Picture CRC error. When instantiating IP, check [Enable Rx EDH Feature] to make this port visible.
o_rx_edh_ff_crc_err	O	1	Indicates a Full Field CRC error in the received EDH packet, only valid in SD-SDI mode; always outputs "0" in other modes. 1: The received EDH packet has a Full Field CRC error; 0: The received EDH packet has no Full Field CRC error. When instantiating IP, check [Enable Rx EDH Feature] to make this port visible.
o_rx_edh_ap_err_flags	O	5	Only valid in SD-SDI mode, outputs the AP error flags for the received EDH packet: from high bit to low bit in order: ues, ida, idh, eda, edh. Always outputs "0" in other modes. When instantiating IP, check [Enable Rx EDH Feature] to make this port visible.
o_rx_edh_ff_err_flags	O	5	Only valid in SD-SDI mode, outputs the FF error flags for the received EDH packet: From high bit to low bit in order: ues, ida, idh, eda, edh. Always outputs "0" in other modes. When instantiating IP, check [Enable Rx EDH Feature] to make this port visible.
o_rx_edh_anc_err_flags	O	5	Only valid in SD-SDI mode, outputs the ANC error flags for the received EDH packet: From high bit to low bit in order: ues, ida, idh, eda, edh. Always outputs "0" in other modes. When instantiating IP, check [Enable Rx EDH Feature] to make this port visible.
o_rx_edh_header_err	O	1	Only valid in SD-SDI mode, "1" indicates that in the received EDH packet, at least one of the first 4 words (including 3 Ancillary Data Headers and 1 Data ID) does not match the expected value; can be considered as EDH packet loss error indicator. Always outputs "0" in other modes. When instantiating IP, check [Enable Rx EDH Feature] to make this port visible.
o_rx_edh_parity_err	O	1	Indicates a Parity verification error in the received EDH packet, only valid in SD-SDI mode; always outputs "0" in other modes. 1: The received EDH packet has a Parity verification error; 0: The received EDH packet has no Parity verification error. When instantiating IP, check [Enable Rx EDH Feature] to make this port visible.
o_rx_edh_checksum_err	O	1	Indicates a Checksum error in the received EDH packet, only valid in SD-SDI mode; always outputs "0" in other modes. 1: The received EDH packet has a Checksum error; 0: The received EDH packet has no Checksum error.

Port	I/O	Bit width	Description
			When instantiating IP , check [Enable Rx EDH Feature] to make this port visible.
o_rx_edh_fmt_err	O	1	Indicates if the Block Number and Data Count of the received EDH packet match the expected value; valid only in SD-SDI mode; always outputs "0" in other modes. 1: The Block Number and Data Count of the received EDH packet does not match the expected value; 0: The Block Number and Data Count of the received EDH packet matches the expected value. When instantiating IP , check [Enable Rx EDH Feature] to make this port visible.
DEBUG Signal			
o_signal_ok	O	1	HSSTHPP_RX_SIGDET_STATUS pass-through signal (asynchronous signal). 1: HSSTHP high-speed serial input signal detected; 0: HSSTHP high-speed serial input signal not detected.
o_cdr_ok	O	1	HSSTHP CDR ALIGN pass-through signal (asynchronous signal). 1: HSSTHP CDR input signal locked; 0: HSSTHP CDR input signal unlocked.
o_lpll_done	O	1	HSSTHP LPLL LOCK indicator, free_clk clock domain signal. 1: Indicates LOCK achieved; 0: Indicates during reset or LOCK not achieved.
o_hpll_done	O	1	HSSTHP HPLL LOCK indicator, free_clk clock domain signal. 1: Indicates LOCK achieved; 0: Indicates during reset or LOCK not achieved.
o_rxstatus	O	6	HSSTHP RX PCS status signal[11], sdi_rx_clk clock domain signal.
i_lpll_wtchdg_clr	I	1	HSSTHP LPLL watchdog clear signal, free_clk clock domain signal. 1: The watchdog signal clears; 0: The watchdog signal does not clear.
i_hpll_wtchdg_clr	I	1	HSSTHP HPLL watchdog clear signal, free_clk clock domain signal. 1: The watchdog signal clears; 0: The watchdog signal does not clear.
o_p_calib_done	O	1	Resistor calibration complete indicator, o_p_calib_done port, free_clk clock domain signal. Note: If HSSTHP_SDI constraint is in HSSTHP_4 position, the external logic of IP needs to detect the o_calib_done signal. Once the signal is pulled high, i_tx_rstn and i_rx_rstn, or i_rstn can be released. 1: Resistor calibration completed; 0: Resistor calibration not completed;

[11] For bit definitions, please refer to "***UG051004_Titan2_HSSTHP_IP_UserGuide***".

Table 2-11 Bit Definitions of Customer Side Data Interface

SDI Rate mode	**i_txd/o_rxd Bit Definitions**							
	[9:0]	[19:10]	[29:20]	[39:30]	[49:40]	[59:50]	[69:60]	[79:70]
	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8
	Framer/De-Framer Module 1		Framer/De-Framer Module 2		Framer/De-Framer Module 3		Framer/De-Framer Module 4	
SD-SDI	Unused	Y&C component	Unused					
HD-SDI	C component	Y component	Unused					
3G-SDI Level A	Data stream 2	Data stream 1	Unused					
6G-SDI Type 1	Sub Image 1		Sub Image 2		Unused			
	Data stream 2	Data stream 1	Data stream 4	Data stream 3				
6G-SDI Type 2	Sub Image 1		Sub Image 2		Sub Image 3		Sub Image 4	
	Data stream 1	Data stream 1	Data stream 2	Data stream 2	Data stream 3	Data stream 3	Data stream 4	Data stream 4
	C component	Y component	C component	Y component	C component	Y component	C component	Y component

Table 2-12 Definition of Ports for Receiving Video Transmission Standards

o_rx_family	Video Transmission Standards
000	SMPTE ST 274 (1920 x 1080)
001	SMPTE ST 296 (1280 x 720)
010	SMPTE 2048-2 (2048x1080)
100	NTSC (720x486)
101	PAL (720x576)
111	Formats not supported
Others	Reserved

Notes: For the 6G rate mode, it refers to the transmitted Sub Image video standard.

Table 2-13 Definition of Ports for Receiving Video Transmission Frame Rate

o_rx_rate	o_rx_frq	Video Transmission Frame Rate
0000	-	None
0011	1	23.98 Hz (Progressive) or 47.95 Hz (Interlaced)
0011	0	24 Hz (Progressive) or 48 Hz (Interlaced)
0101	0	25 Hz (Progressive) or 50 Hz (Interlaced)
0111	1	29.97 Hz (Progressive) or 59.94 Hz (Interlaced)
0111	0	30 Hz (Progressive) or 60 Hz (Interlaced)
1000	1	47.95 Hz
1000	0	48 Hz
1001	0	50 Hz
1011	1	59.94 Hz
1011	0	60 Hz
Others	-	Reserved

Note:"-" represents any value.

2.4.2 Timing Description

2.4.2.1 Client-Side Interface Timing

6G-SDI IP Client-side interface timing diagrams are shown in Figure 2-4 and Figure 2-5. The clock enable signals (o_rx_ce andi_tx_ce) are not shown in the figures. In actual use, please refer to Table 2-13 for the client-side data interface bit definition.

- In 3G-SDI Level A and6G-SDI Type 1 modes, the clock enable signal is always 1;
- In SD-SDI, HD-SDI, and 6G-SDI Type 2 modes, the clock enable signal is valid and the logical timing will not change.

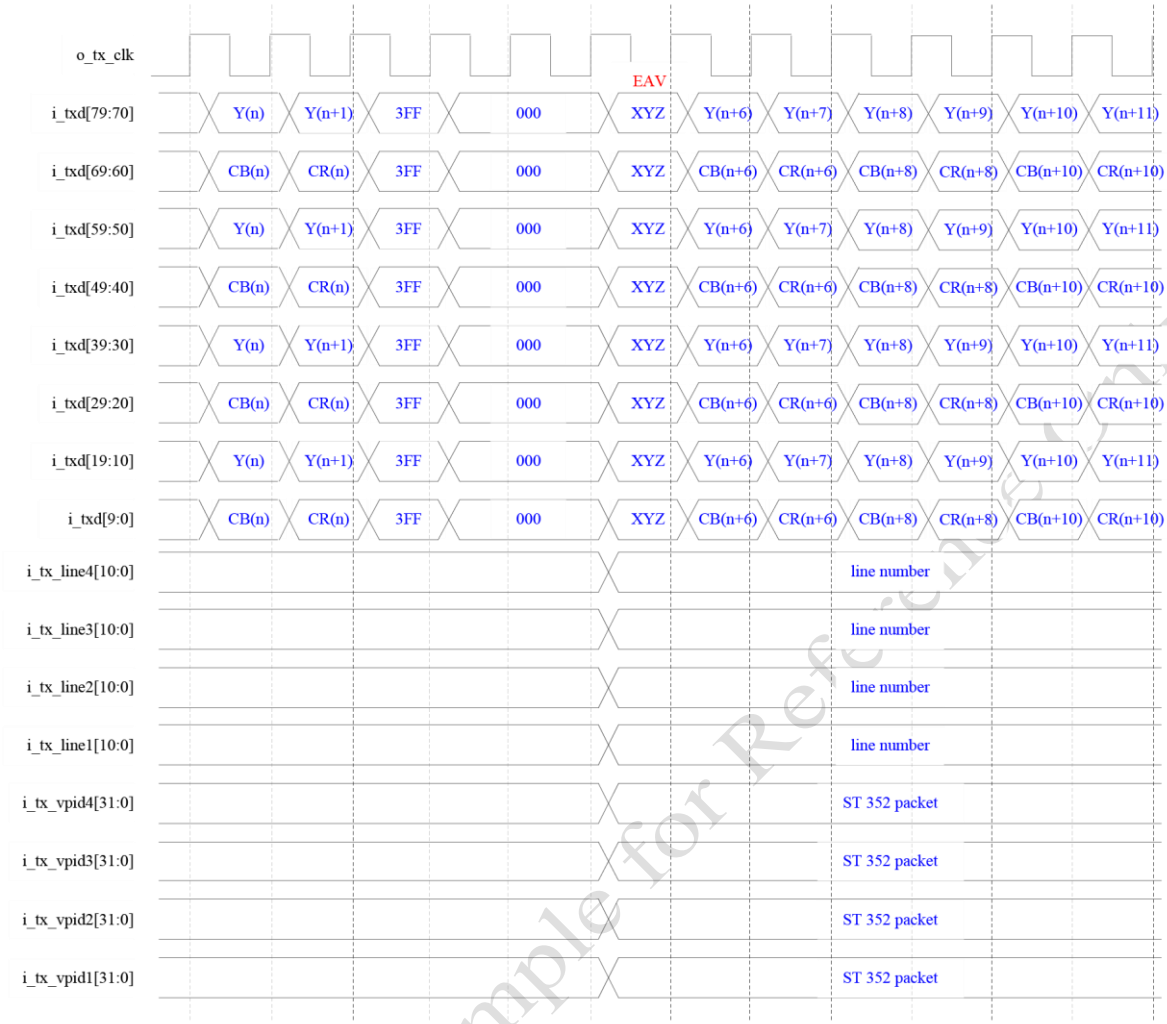

Figure 2-4 6G-SDI IP TX Client-Side Interface Timing Diagram

Attention:

Multichannel signal input at the 6G-SDI IP TX client side requires that signals from multiple channels be aligned at the same EAV position, supporting signal input of up to 8 channels.

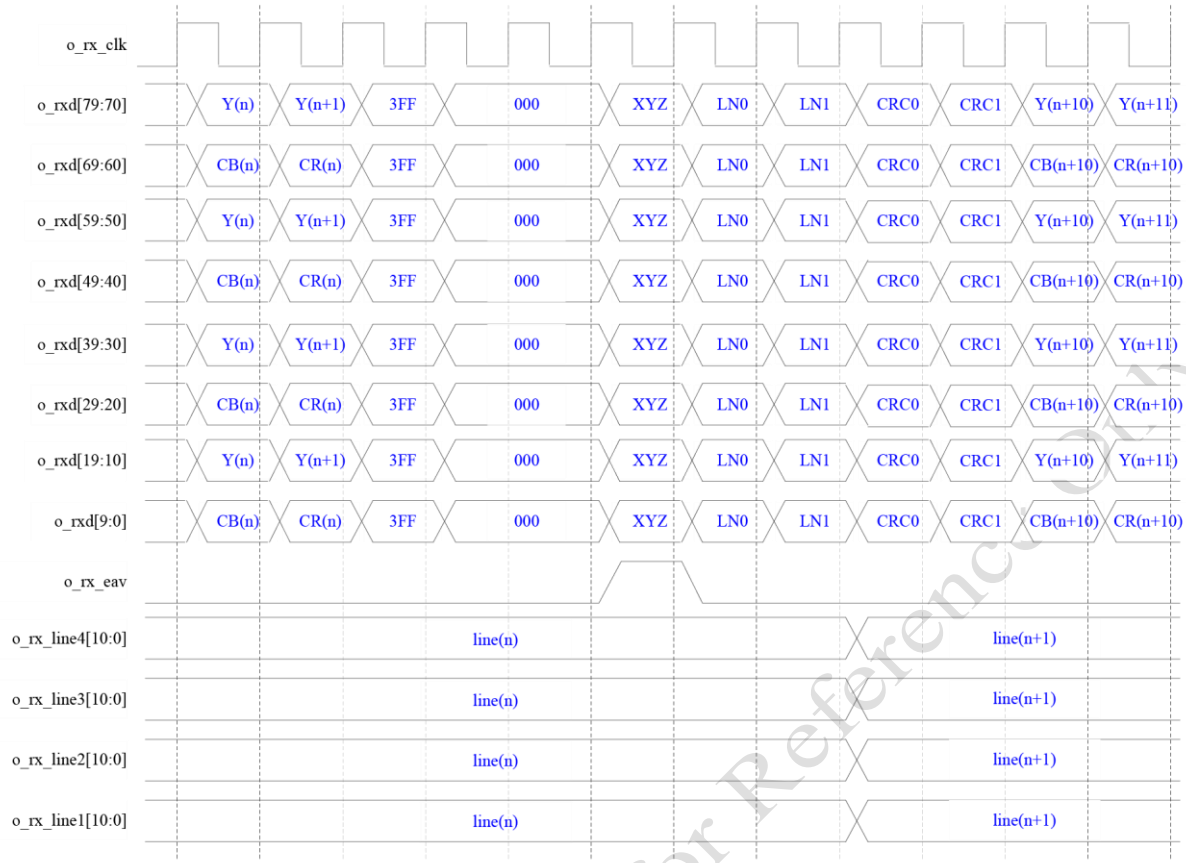

Figure 2-5 6G-SDI IP RX Client-Side Interface Timing Diagram

2.4.2.2 Clock Enable Signal Timing

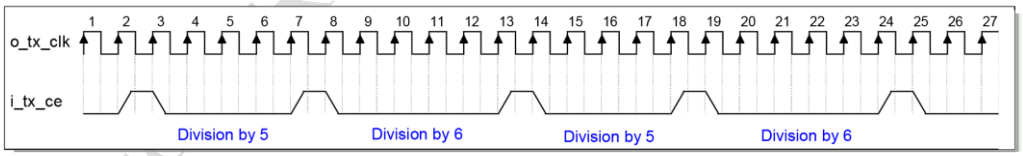

Figure 2-6 Requirements for Transmitting Clock Enable Timing in SD-SDI Mode

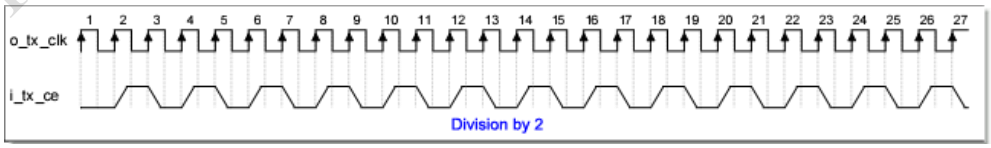

Figure 2-7 Requirements for Transmitting Clock Enable Timing in HD/6G-SDI Type 2 Mode

2.5 Typical Applications

For 6G-SDI IP typical applications please refer to "2.3 Example Design".

2.6 Descriptions and Considerations

2.6.1 Clock Constraints

In the generated Example Design project constraint file ipsl_sgmii_onboard.fdc, the output clock of HSSTHP IP has been constrained to the global clock. Taking the Example Design project as an example:

```
create_clock -name {clk_27m} [get_nets {o_clk_27m}] -period {37} -waveform {0.000 18.500}
create_clock -name {i_clk_100m} [get_ports {i_clk_100m}] -period {10} -waveform {0.000 5.000}
create_clock -name {tx_clk} [get_nets {tx_clk}] -period {6.7} -waveform {0.000 3.35}
create_clock -name {rx_clk} [get_nets {rx_clk}] -period {6.7} -waveform {0.000 3.35}
```

2.6.2 HSSTHP Physical Location Constraints

```
define_attribute {i:u_sdi_top.u_sdi_hssthp.U_GTP_HSSTHP_WRAPPER.CHANNEL0_ENABLE.U_LANE0_WRAP.U_LANE0} {PAP_LOC} {HSSTHP_664_1530:U0_HSSTHP_LANE}
define_attribute {i:u_sdi_top.u_sdi_hssthp.U_GTP_HSSTHP_WRAPPER.HPLL_ENABLE.U_HPLL_WRAP.U_HPLL} {PAP_LOC} {HSSTHP_664_1530:U_HSSTHP_COMMON}
```

According to the actual conditions of the single board, Users can refer to the***"UG051004_Titan2_HSSTHP_IP_UserGuide"***[9] to modify the constraints to meet practical usage requirements.

2.6.3 IP Clock Scheme

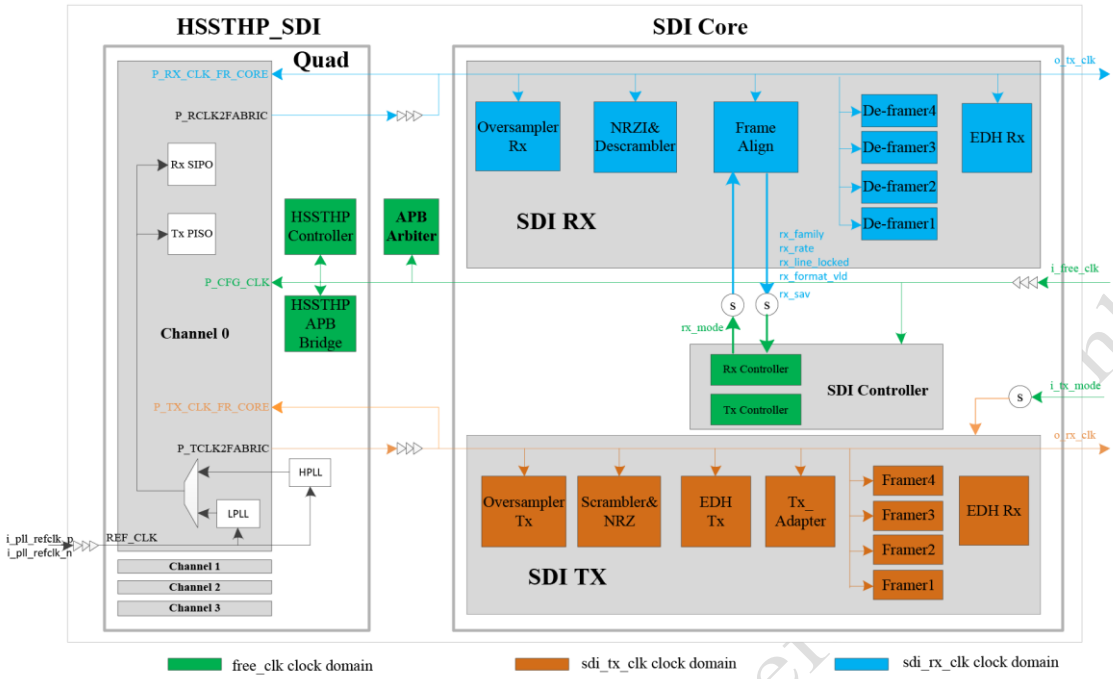

Figure 2-8 6G-SDI IP Clock Scheme Block Diagram

Attention:

In the IP Clock Scheme Diagram, OS indicates that signals are handled across clock domains here, and OS separates the signals into different clock domains.

2.6.3.1 HSSTHP_SDI Clock Scheme

HSSTHP_SDI Clock Scheme is determined by the working mode chosen when configuring the IP.

TX Data Path Clock:

- From the local reference clock.

RX Data Path Clock:

- In the HD-SDI, 3G-SDI, and 6G-SDI modes, from the CDR recovered clock;
- In the SD-SDI mode, from the local reference clock.

2.6.3.2 SDI Core Clock Scheme

SDI Core is divided into three clock domains, as shown in .

2.6.3.2.1 free_clk clock domain

The clock of this clock domain is provided by the user and needs to be stable, with a frequency of 27MHz;; It is used for SDI Controller, APB_Arbiter, and the APB Bridge and Controller of HSSTHP, and drives the HSSTHP 's P_CFG_CLK clock port.

2.6.3.2.2 sdi_tx_clk Clock Domain

The clock of this clock domain comes from the HSSTHP's P_TCLK2FABRIC output port. After passing through the clock tree, it drives the o_tx_clk outputs to the IP external for the user's transmitter logic. It also serves as the working clock for SDI TX logic and drives the HSSTHP's P_TX_CLK_FR_CORE input port. Frequency points are as shown in Table 2-14.

Table 2-14 sdi_tx_clk Frequency Points in Different SDI Rate Modes

Reference Clock Frequency	**sdi_tx_clk[12] Frequency (MHz)**
	SD-SDI/HD-SDI/3G-SDI/6G-SDI
REF_CLK	148.5
REF_CLK/1.001	148.5/1.001

2.6.3.2.3 sdi_rx_clk Clock Domain

The clock of this clock domain comes from HSSTHP's P_RCLK2FABRIC output port. After passing through the clock tree, it drives the o_rx_clk outputs to the IP external for the user's receiver logic. It also serves as the working clock for SDI RX logic and drives HSSTHP's P_RX_CLK_FR_CORE input port. Frequency points are as shown in Table 2-15.

Table 2-15 sdi_rx_clk Frequency Points in Different SDI Rate Modes

SDI Rate Mode	**sdi_rx_clk Frequency (MHz)**
SD-SDI	148.5
HD-SDI	HSSTHP RX differential interface rate/10

[12] In SD-SDI mode, the clock needs to be used with the clock enable signal shown in Figure 2-6;In HD-SDI and 6G-SDI Type2 modes, the clock needs to be used with the clock enable signal shown in Figure 2-6.

SDI Rate Mode	sdi_rx_clk Frequency (MHz)
3G-SDI	HSSTHP RX differential interface rate/20
6G-SDI	HSSTHP RX differential interface rate/40

2.6.4 IP Reset Scheme

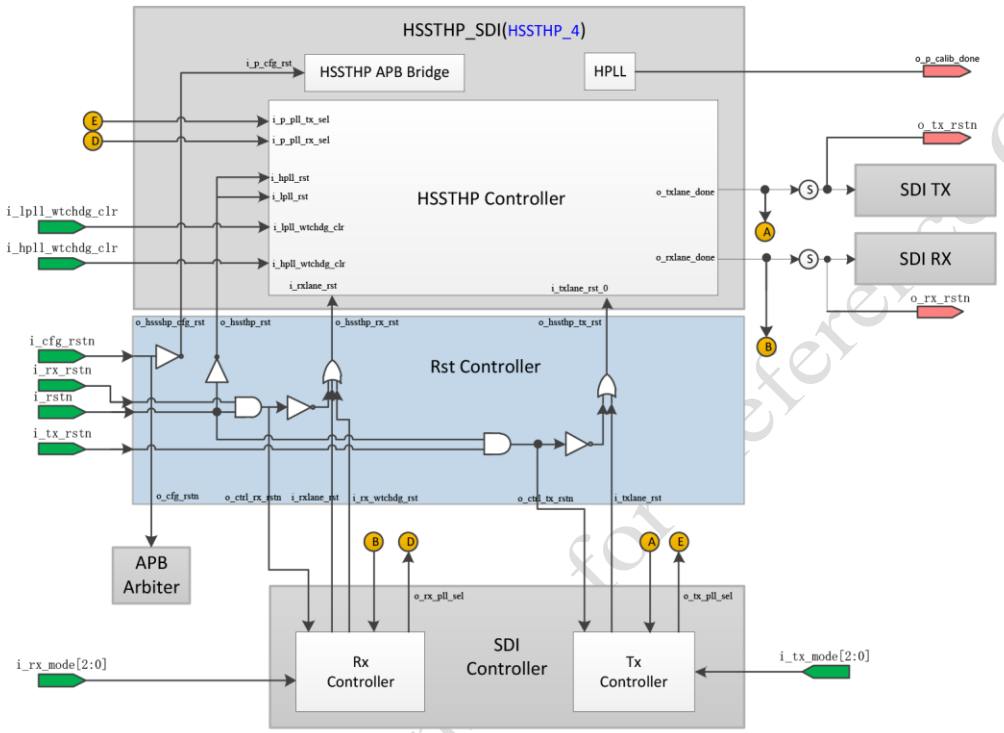

Figure 2-1 6G-SDI IP Reset Scheme Block Diagram

Reset ports are divided into configuration reset (i_cfg_rstn) and logic reset (i_rstn , i_tx_rstn , and i_rx_rstn).

2.6.4.1 Configuration reset

i_cfg_rstn controls HSSTHPAPB Bridge and APB Arbiter reset.

Attention:

In the IP reset scheme diagram, ○s indicates that signals are handled across clock domains here and ○s separates the signals into different clock domains.

The i_cfg_rstn signal will reset all internal register values of HSSTHP_SDI. After i_cfg_rstn is released, i_rstn should be initiated, resetting the entire SDI TX and SDI RX.

2.6.4.2 Logical Reset

2.6.4.2.1 SDI Core Reset

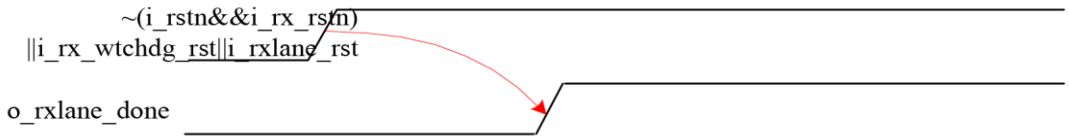

Figure 2-2 SDI RX Reset Timing Diagram

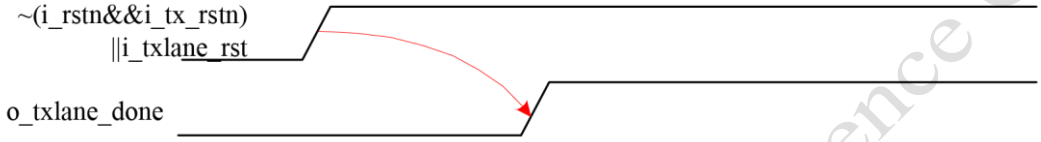

Figure 2-3 SDI TX Reset Timing Diagram

- i_rstn and i_tx_rstn control the Tx Controller. When i_rstn and i_tx_rstn reset are released, the Tx Controller starts operating;
- i_rstn and i_rx_rstn control the Rx Controller. When i_rstn and i_rx_rstn reset are released, the Rx Controller starts operating;
- After HSSTHP_SDI TX/RX reset completes, the txlane_done and rxlane_done will be output, controlling the SDI TX reset and SDI RX reset respectively.

2.6.4.2.2 HSSTHP_SDI Reset

i_rstn ,i_tx_rstn and i_rx_rstn serve as global logic reset, TX logic reset, and RX logic reset, controlling the HSSTHP Controller to perform a reset on HSSTHP_SDI according to the valid reset sequence.

- When txlane_done=1 is achieved, the rate can be switched by dynamically changing the value of i_tx_mode.Tx Controller configures the HSSTHP registers according to the value of i_tx_mode; it then outputs o_tx_pll_sel, controlling the HSSTHP Controller to select the Tx-side HPLL or LPLL based on the valid rate; finally, it outputs the o_rxlane_rst signal to reset HSSTHP TX.
- When rxlane_done=1 is achieved, the Rx Controller mode state machine confirms the initial state according to i_rx_mode, and based on the value of i_rx_mode , configures the HSSTHP

registers accordingly; it then outputs o_rx_pll_sel, controlling the HSSTHP Controller to select the Rx-side HPLL or LPLL based on the valid rate; finally, it outputs the o_rxlane_rst signal to reset HSSTHPRX.

Attention:

o_p_calib_done signal indicates HSSTHP resistor calibration state. Only after this signal is pulled high can users release i_tx_rstn and i_rx_rstn or i_rstn .If HSSTHP_SDI is not constrained to HSSTHP_4 position, then o_p_calib_done signal output by the IP is invalid. The user needs to manually instantiate the HPLL configuration module. For detailed information, please refer to "2.6.5 Resistor Calibration."

2.6.5 Resistor Calibration

When enabling the resistor calibration function, based on the used HSSTHP, there are two scenarios.

2.6.5.1 Scenario 1

If the IP uses HPLL and the HPLL is constrained to HSSTHP_4, then the IP port o_p_calib_done is valid; only after the o_p_calib_done is pulled high can users release the reset on i_tx_rstn and i_rx_rstn.

2.6.5.2 Other Scenarios

For application scenarios other than the above "Scenario 1," the IP port o_p_calib_done is invalid. The user needs to manually migrate the contents of <project_path>/rtl/hssthp/ipsxe_sdi_hssthp_tmplc.v to the project, connect the corresponding ports, and add physical location constraints in the .fdc file.

2.6.6 uart2apb Module Read/Write Operation Example

2.6.6.1 Read Operation

Reading data from address 0x000001: "0x72 "+"0x010000", which is 0x72010000.

2.6.6.2 Write Operation

Writing to address 0x000001 0x02:"0x77 "+"0x010000 "+"0x00000002 ", which is 0x7701000000000002.

2.7 IP Debugging Methods

Example Design can be debugged through the UART interface. The UART interface can be used to configure the IP to transmit different video data and read For detection signal of the IP output and the usage of the UART interface, please refer to "2.3.3.4 uart2apb Module".

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