PG2L100H Gigabit Ethernet Application Guide

(V1.0)

(13.05.2020)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.0	13.05.2020	Initial release.

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Chapter 1 Overview

1.1 Introduction

This is an application document for the PG2L100H Ethernet Interface product launched by Shenzhen Pango Microsystems Co., Ltd. It mainly introduces the function list, design architecture, interface definition, interface timing, supported devices and reference designs of Ethernet.

1.2 Design Information

Table 1-1 Design Information

Supported Devices	PG2L100H
Hardware Environment	PG2L100KF01_A1 board
Software	Pango Design Suite 2020.1-SP1
Simulation Tool	Modelsim10.2c

1.3 Resource Usage

Table 1-2 Resource Usage Rate

	Logic Utilization	Used	Available	Utilization(%)
1	APM	0	240	0
2	FF	1480	133200	2
3	LUT	1865	66600	3
4	Distributed RAM	0	19900	0
5	DRM	2	155	2
6	IO	29	300	10
7	RCKB	0	24	0
8	SCANCHAIN	1	1	100
9	USCM	4	32	13
10	CCS	1	1	100
11	ADC	0	1	0
12	DDR_PHY	0	24	0
13	HSSTLP	0	2	0
14	GPLL	1	6	17
15	PPLL	0	6	0
16	DDRPHY_CPD	0	12	0
17	HCKB	0	96	0
18	IOCKB	0	24	0
19	MRCKB	0	12	0
20	PCIE	0	1	0
21	DDRPHY_IOCLK_DIV	0	6	0

Chapter 2 Function Description

2.1 Register Configuration Operation

Users can achieve various working modes of the Ethernet MAC layer through register configuration. Users can read from and write to PHY registers via APB interface, and TS_MAC IP will convert APB interface signals into MDIO interface signals to read and write PHY registers. For detailed register descriptions and APB read and write register operations, please refer to the "***Titan Family 10/100/1000M Ethernet MAC IP User Guide V1.6***".

2.2 Transmit Operation

During transmission, users transmit data to the MAC through the user interface, which is then packaged in MAC frame format in the MAC transmitter.MAC parameter configuration determines whether to perform short frame padding and whether to add a frame check sequence. According to frame interval parameters and MAC interface configuration parameters, the data is transmitted through the RGMII interface to PHY.

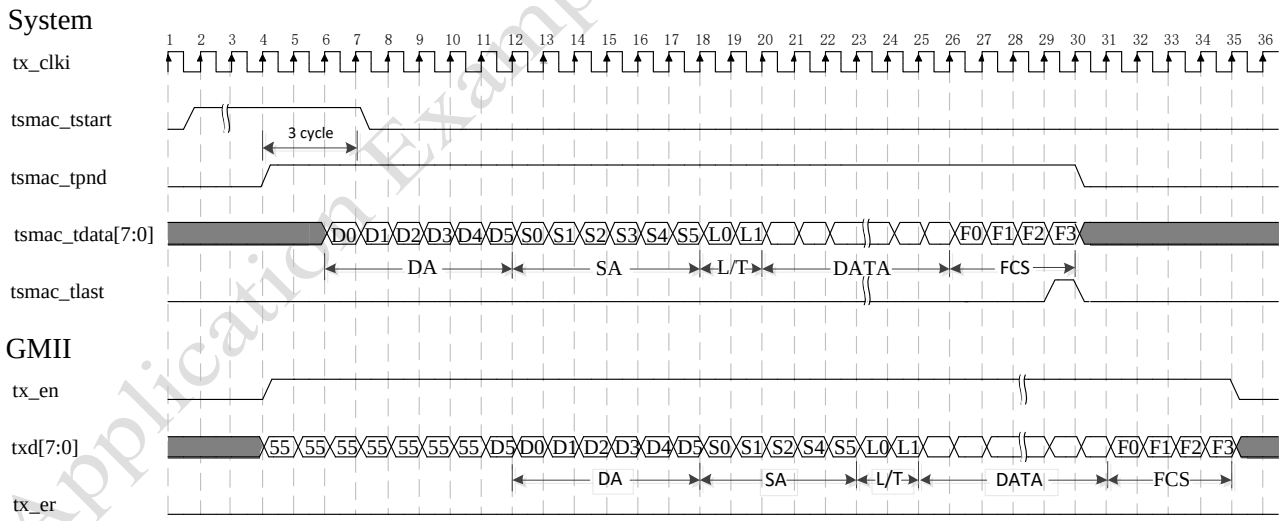

Figure 2-1 Transmit Timing Diagram

1. When transmitting a frame, first pull the tsmac_tstart signal high.
2. When detecting tsmac_tpnd has been pulled high for three cycles, pull down the tsmac_tstart signal.
3. When tsmac_tpnd is pulled high in the third cycle, transmit the first data tsmac_tdata[7:0].
4. When transmitting the last data, pull the tsmac_tlast signal high for a cycle indicates the end of a transmission.In this mode,FCS is provided by the user, therefore, via IP module, only the preamble and SFD are attached to the front before transmission.

2.3 Receive Operation

During reception, MAC receives data from PHY through RGMII, discarding inactive data frames, and decomposing the data into the format required by the user. After removing the frame preamble, frame delimiter, and frame check sequence (whether the frame check sequence is removed depending on the actual configuration),finally,the user receives date througth the user interface.

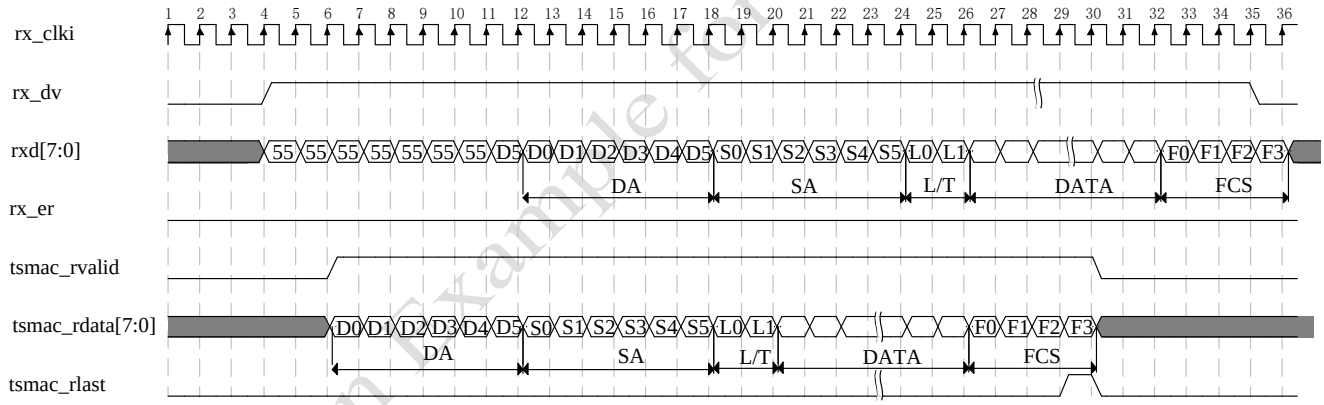

Figure 2-2 Reception Timing Diagram

1. PHY transmits a frame of data to MAC via the GMII interface.
2. MAC begins to output a frame of data tsmac_rdata[7:0], and pulls the tsmac_rvalid signal high.
3. For the last data, MAC pulls down tsmac_rvalid, and pulls high tsmac_rlast by one cycle.

2.4 RGMII Interface Conversion Operation

To adapt to RGMII interface of PHY chip, it is necessary to convert the GMII interface to the RGMII interface. RGMII interface employs the working mode of simultaneous sampling on both rising and falling edges. The specific conversion operation needs to be implemented through GTP_ISERDES_E2 and GTP_OSERDES_E2, as shown below.

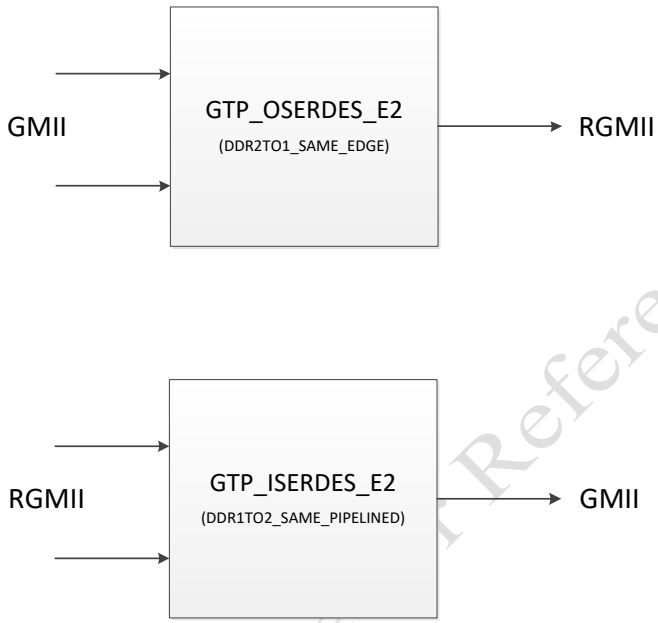

Figure 2-3 Interface Conversion Operation

Chapter 3 Reference Design

3.1 Reference Function Design

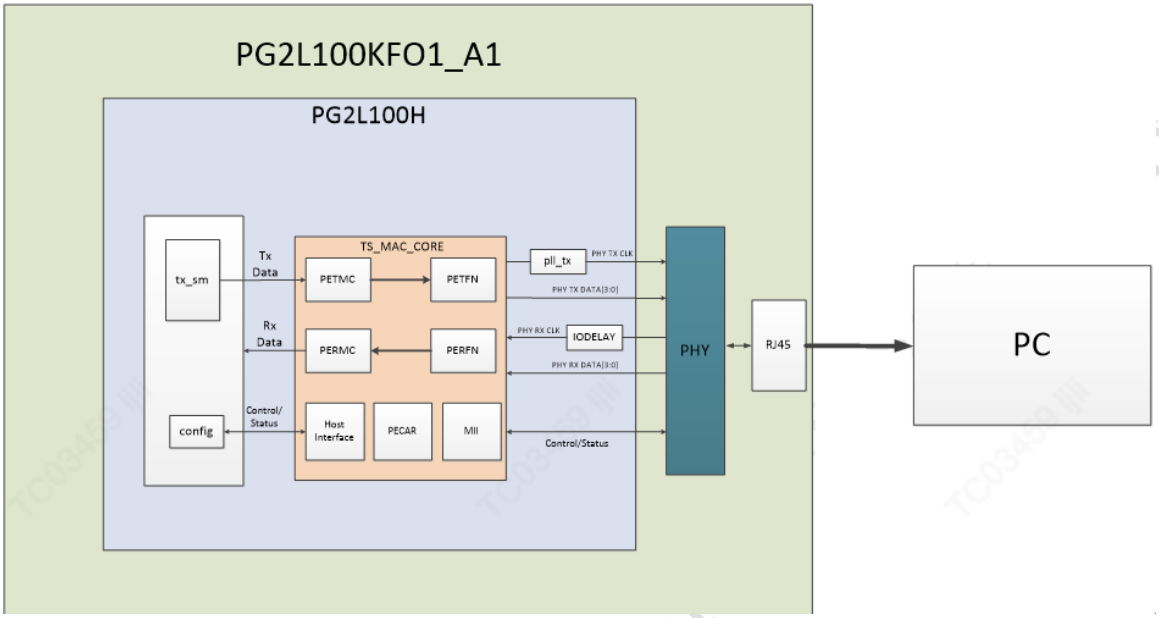

Figure 3-1 Reference Design Function Block Diagram

The user can test if the Ethernet interface can transmit and receive data correctly by docking two boards, or judge whether the received data packets meet the Ethernet standards through packet capture software on the host computer. PG2L100KF01_A1 board has two Ethernet interfaces, and Ethernet0 interface (J7) is used in this reference design.

3.2 Reference Design Interface List

Table 3-1 Interface Definitions and Descriptions

Port	Width	Input/Output	Description
free_clk	1	Input	External reference clock, 50MHz by default
external_rst	1	Input	System reset signal, reset at a low level
phy_rst_n	1	Output	PHY chip reset signal
rx_clki	1	Input	RGMII receive clock signal
phy_rx_dv	1	Input	RGMII receive control signal
phy_rxd0	1	Input	RGMII receive data signal
phy_rxd1	1	Input	RGMII receive data signal
phy_rxd2	1	Input	RGMII receive data signal

Port	Width	Input/Output	Description
phy_rxd3	1	Input	RGMII receive data signal
l0_sgmii_clk_shft	1	Output	RGMII transmit clock signal
phy_tx_en	1	Output	RGMII transmit control signal
phy_txd0	1	Output	RGMII transmit data signal
phy_txd1	1	Output	RGMII transmit data signal
phy_txd2	1	Output	RGMII transmit data signal
phy_txd3	1	Output	RGMII transmit data signal
mdc	1	Output	MII interface module management clock
mdio	1	Input/Output	MII interface module management data input and output

3.3 Reference Design Project Directory

The reference design project directory is shown in the figure below.

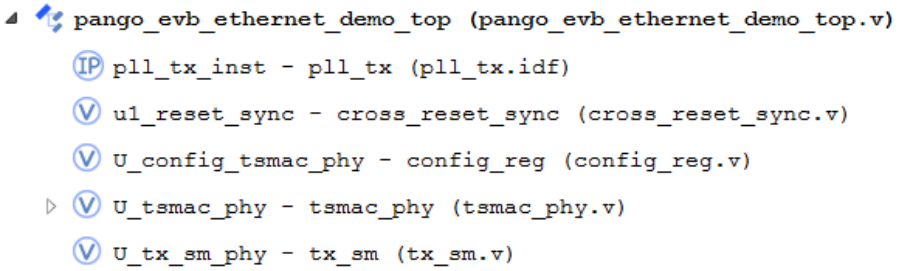

Figure 3-2 File Directory

pango_evb_ethernet_demo_top: Top-level file

pll_tx_inst: Generates 125M RGMII transmit clock and 50M configuration clock through PLL

u1_reset_sync: External reset debounce module

U_config_tsmac_phy: Configures the Ethernet MAC layer's working mode

U_tsmac_phy: TS-MAC IP reference design and RGMII interface conversion

U_tx_sm_phy: Packet transmission module, generating the user-side transmission data

RGMII receive clock and data output through the PHY chip may exhibit phase offset, causing incorrect data sampling. Users can use the GTP_IODELAY_E2 unit to adjust the RGMII receive clock delay to ensure correct sampling.

3.4 Reference Design Simulation

Simulation-related files are in the simulation folder. Use modelsim10.2c as the simulation tool.

1. Users need to modify the file paths from line 5 to 31 of pango_evb_ethernet_demo.do file based on the PDS version and installation location.
2. Run the sim.bat file for project simulation.

3.5 Reference Design On-board Verification

Data from the transmitter and receiver can be captured separately through docking board test, as shown below.

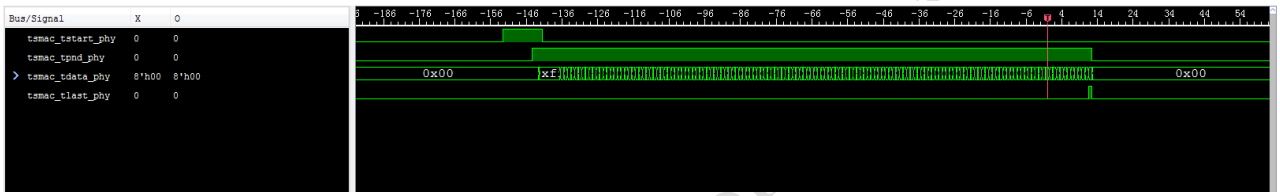

Figure 3-3 Transmitter Data Timing

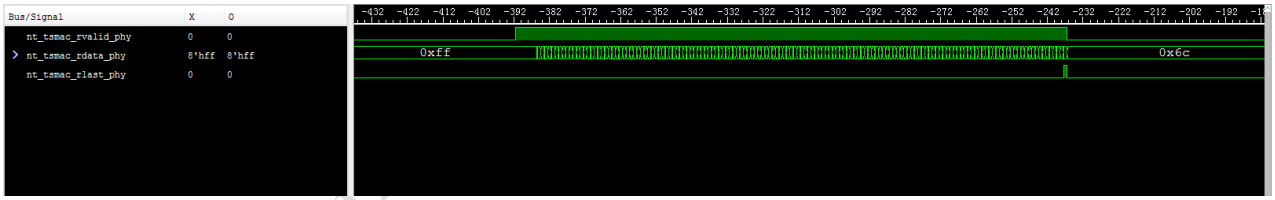

Figure 3-4 Receiver Data Timing

By docking the board to a PC and using a packet capture tool on the PC, users can also capture the data transmitted by FPGA. The operating procedure is as shown in the figure, using the default configuration.

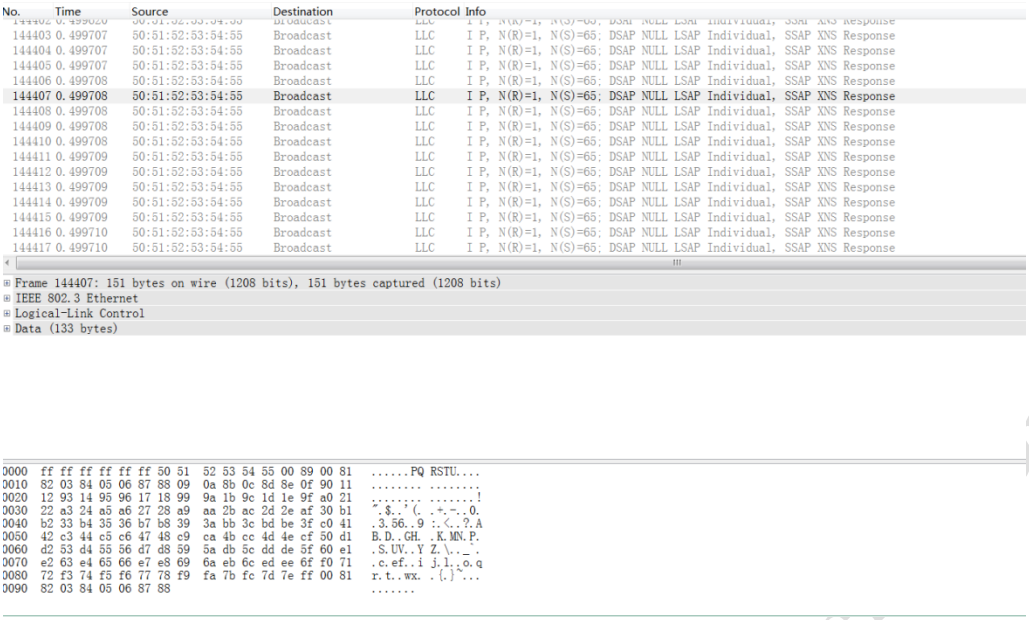

Figure 3-5 Wiresharke Data Packet Capture

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