2.5G Ethernet System Application Guide

(AN05009, V1.5)

(04.03.2024)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.5	04.03.2024	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
HSSTLP	High Speed Serial Transceiver Low Performance
PCS	Physical Code Sublayer
PM A	Physical Media Attachment
GM II	1Gigabit Media Independent Interface

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Chapter 1 Overview

1.1 Introduction

This is an application document for the 2.5G Ethernet system interface product launched by Shenzhen Pango Microsystems Co., Ltd. It mainly introduces the function list, design architecture, interface definition, interface timing, supported devices and reference design, etc. of the 2.5G Ethernet system.

This product provides users with a complete 2.5G Ethernet protocol, including PMA, PCS and MAC functions, with a line rate of 3.125G.

1.2 Main Functions

The 2.5G Ethernet system mainly supports the following functions:

- 802.3 Ethernet MAC standards
- 802.3 Ethernet PCS standards (excluding auto-negotiation mode)
- Internal GMII interface (16-bit)
- User-side interface data bus (16-bit)
- APB management interface
- Preamble insertion and deletion
- CRC detection and generation, addition and deletion
- Message classification and statistics in both receive and transmit directions
- Flexible control of inter-frame gap, 12-byte as default
- Flow control and priority flow control
- Transmits and receives independent configuration of maximum packet length (MTU)
- Padding function
- Preamble compression (minimum to two bytes)

1.3 Design Information

Table 1-1 2.5G Ethernet System Design Information

2.5G Ethernet System	
Supported Devices	PG2T390H,PG2L100H, and PGL100H family FPGA products
Supported User Interface	User-defined interface
Provided Design Files	
2.5G Ethernet System Design File	Encrypted file
2.5G Ethernet System Reference Design	Verilog files
Simulation File	Encrypted file
Constraint File	fdc file
Development Tools	
Design Tools	PDS development suite Pango Design Suite 2021.4-SP1 and later versions supported
Simulation Tool	Modelsim

1.4 Resource Usage

Table 1-2 Resource Usage Rate

Device	DRM	FF	LUT	PLL	Function
PG2L100H	0	2312	1616	0	Excluding pause and PFC
PG2L100H	0	2487	1727	0	Including pause but excluding PFC
PG2L100H	0	3583	2401	0	Fully-featured

Chapter 2 Function Description

The typical application of 2.5G Ethernet system is shown in Figure 2-1. The system uses a GMII (16-bit) interface on the PCS side and a custom packet interface format at the user side (refer to the following descriptions for the specific format). It supports 802.3 protocol MAC layer functions.

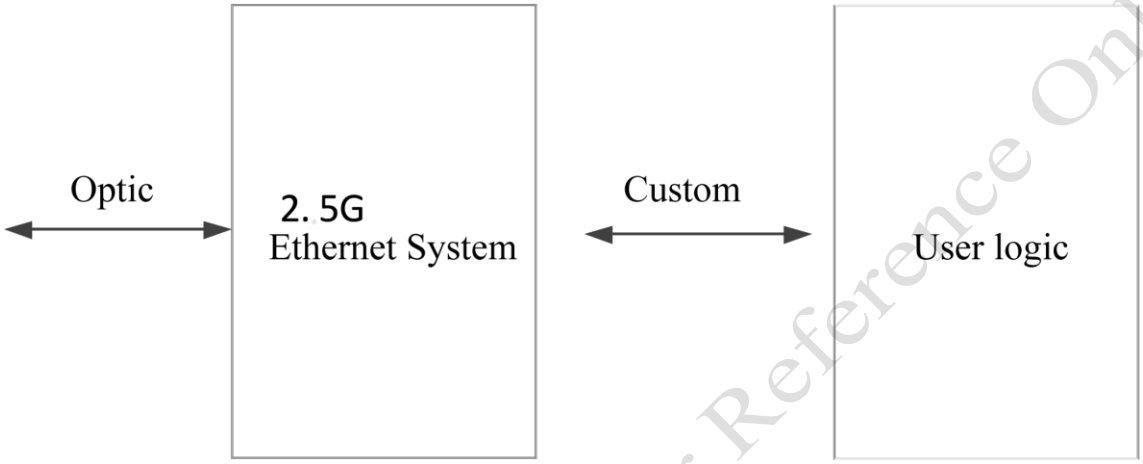

Figure 2-1 Typical Application of 2.5G Ethernet System

2.1 2.5G Ethernet System Design Architecture

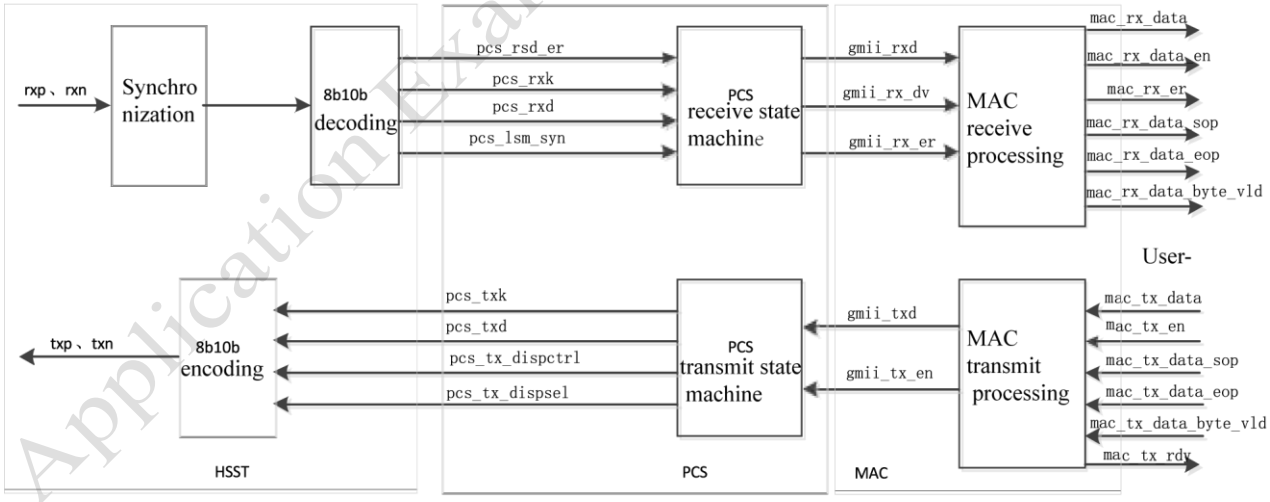

Figure 2-2 Functional Block Diagram of 2.5G Ethernet System

2.5G Ethernet system design consists of HSST, PCS and MAC. Their specific functions are described as follows:

- HSST:

  mainly implements PMA layer functions, integrated with some PCS functions such as block synchronization and 8b/10b encoding/decoding.

- PCS:

  mainly implements receive and transmit state machines based on the 1000Base-X chapter in 802.3 protocol.

- MAC:

  mainly for MAC functions, preamble addition/removal, CRC generation and detection, CRC addition/removal, message classification and statistics, inter-frame gap control, MTU setting and flow control functions.

2.2 Interface List

Table 2-1 Interface List

Signal Name	Input/Output	Bit width	Description
Global signals			
sys_rst	Input	1	Global reset signal, active-high
i_free_clk	Input	1	Configuration clock, 10–100M
HSST interfaces			
ref_clk_n	Input	1	HSST reference clock. 125M or 156.25M
ref_clk_p	Input	1	HSST reference clock. 125M or 156.25M
txn_2g5	Output	1	Hsst output n side
txp_2g5	Output	1	Hsst output p side
rxn_2g5	Input	1	Hsst input n side
rxn_2g5	Input	1	Hsst input p side
User-side message interfaces			
mac_tx_data	Input	16	Data transmission through the user-side message interface
mac_tx_data_en	Input	1	Enables data transmission through the user-side message interface
mac_tx_data_sop	Input	1	Message start bit of data transmitted through the user-side message interface
mac_tx_data_eop	Input	1	Message end bit of data transmitted through the user-side message interface
mac_tx_data_byte_vaild	Input	1	Indicates the number of valid bytes of data transmitted through the user-side data interface, 1 indicates 1 valid byte, and 0 indicates 2 valid bytes, judged at eop
mac_tx_ready	Output	1	Transmit module ready indicator signal, to backpress data transmitted by the user
mac_rx_data	Output	16	Data reception through the user-side data interface

Signal Name	Input/Output	Bit width	Description
mac_rx_data_en	Output	1	Enables data reception through the user-side message interface
mac_rx_data_sop	Output	1	Message start bit of data received through the user-side message interface
mac_rx_data_eop	Output	1	Message end bit of data received through the user-side message interface
mac_rx_data_byte_vaild	Output	1	Indicates the number of valid bytes of data received through the user-side data interface,1 indicates 1 valid byte,and 0 indicates 2 valid bytes, judged at eop
mac_rx_data_err	Output	1	Indicates message reception error, aligned with eop, 1 indicates message error, and 0 indicates no error.
Flow control interfaces			
tx_pause_en	Input	1	Pause-frame global transmit enable, active-high
rx_pause_en	Input	1	Pause-frame global receive enable, active-high
pause_req	Input	1	Pause-frame transmit request, active-high
pause_req_time	Input	16	Pause_time value, in quanta, one quanta=204.8ns
send_interval	Input	16	Transmit interval between two Pause frames, in quanta, one quanta=204.8ns
rx_pfc_pause_stop	Output	8	bit0 indicates pri0,bit1 indicates pri1... 1 indicates stopping transmission, and 0 indicates transmission allowed.
Configuration signals			
apb_clk	Input	1	Configuration clock signal, with a frequency range of 10–100MHz
apb_penable	Input	1	Configuration access enable
apb_pwrite	Input	1	Read/write selection configuration signal, high for write, and low for read
apb_paddr	Input	19	Configuration address bus
apb_pwdata	Input	32	Configuration write data
apb_psel	Input	1	Configuration selection signal
apb_prdata	Output	32	Configuration read data
apb_pready	Output	1	Configure read/write ready output

2.3 Interface Timing

The 2.5G Ethernet system uses an user-defined interface. The user transmit timing is shown in the figure below:

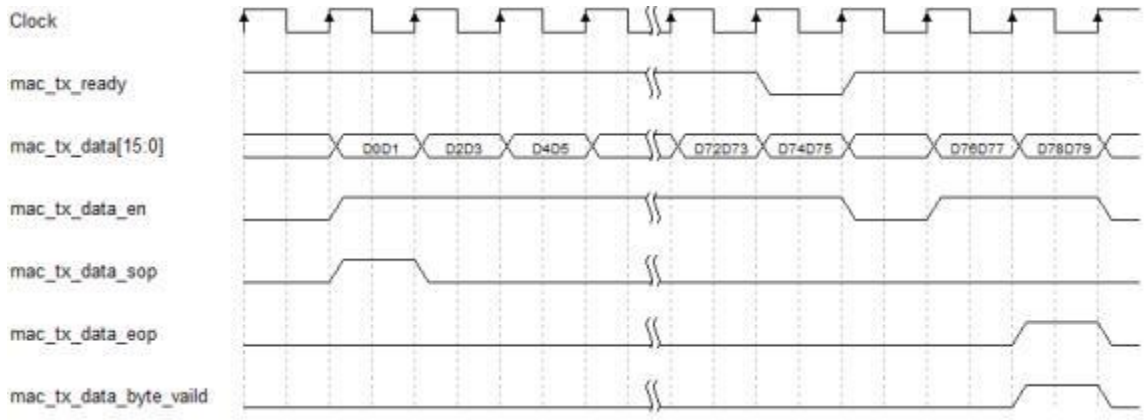

Figure 2-3 User-side Transmit Interface Timing

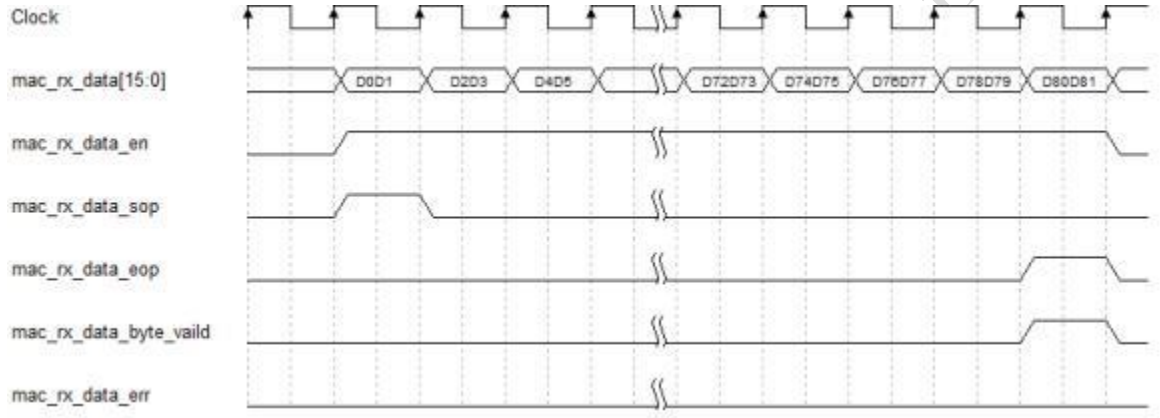

Figure 2-4 Example of User Receiving Normal Data Timing

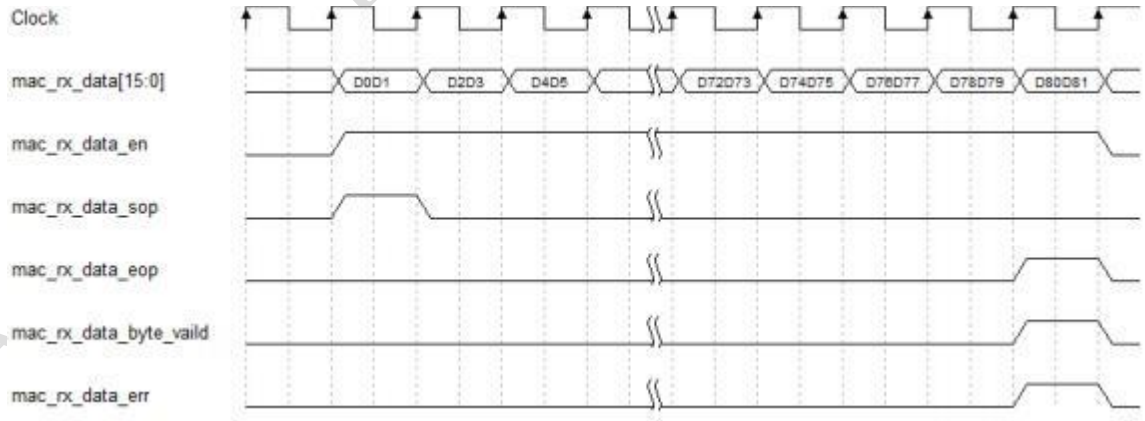

Figure 2-5 Example of User Receiving Normal Data Timing

2.4 Parameter Descriptions

Table 2-2 Parameter Descriptions

Parameter Name	**Parameter Description**
PAUSE_FLOW_CTRL	"TRUE" indicates enabling the pause frame function, "FALSE" indicates disabling the pause frame function
PFC_FLOW_CTRL	"TRUE" indicates enabling the PFC frame function, "FALSE" indicates disabling the PFC frame function
STSTISTICS_REG	"TRUE" indicates enabling the statistics function, "FALSE" indicates disabling the statistics function
COMPRESS_PREAMBLE	"TRUE" indicates enabling the preamble compression function, "FALSE" indicates disabling the preamble compression function Function

Chapter 3 Register Descriptions

Users can access MAC space through the APB configuration interface and perform operations, including register read/write, message transmit statistics, and message receive statistics.

Address management is for APB interface address partitioning. Users can allocate the register address space as needed.

Table 3-1 Address Allocation

Addr [18:9] == 10'd1 & Addr[8:7]=2'b00	Configuration register
Addr [18:9] == 10'd1 & Addr[8:7]=2'b01	Receive statistics
Addr [18:9] == 10'd1 & Addr[8:7]=2'b10	Transmit statistics
Addr [18:9] == 10'd1 & Addr[8:7]=2'b11	Reserved

Register read/write is for configuration register read/write and status register read.

Table 3-2 Configuration Register Addresses

Register	Defaults	Address	Description
Global registers			
Version	32'h11346545	0x0	Current version number and time
pause_mac	32'h0	0x1	Lower 32 bits of pause-frame source MAC address
pause_mac	16'h0	0x2	Higher 16 bits of pause-frame source MAC address
packet_sta_clr_tx	1'b0	0x3	TX statistics clear, 1 indicates clear, write 1 then 0 to complete Clear operation
packet_sta_clr_rx	1'b0	0x4	RX statistics clear, 1 indicates clear, write 1 then 0 to complete Clear operation
Receive-side registers			
rx_mtu_en	1'b0	0x13	Receive mtu enable, 1 indicates enabled
rx_mtu_size	15'd0	0x14	Receive mtu setting value
rx_pfc_en	1'b0	0x15	Global Pfc frame receive enable,1 indicates enabled
Transmit-side registers			
tx_mtu_en	1'b0	0x21	Transmit mtu enable, 1 indicates enabled
tx_mtu_size	15'd0	0x22	Transmit mtu setting value
tx_ipg_en	1'b0	0x23	Transmit ipg enable, 1 indicates enabled
tx_ipg_value	6'd0	0x24	Transmit ipg setting value, with a range of 12–63
xon	1'b0	0x25	1: xon function enabled
tx_pfc_en	1'b0	0x26	Global Pfc frame transmit enable, 1 indicates enabled

Register	Defaults	Address	Description
pfc_pri_req	8'b0	0x27	Pfc frame transmit request, bit0 corresponds to pri0, 1 indicates enabled
tx_pfc_pri_en	8'b0	0x28	Pfc priority transmit enable, bit0 corresponds to pri0, 1 indicate enabled
pfc0_pause_req_time	16'b0	0x29	Pfc0 flow control transmit request time, in quanta, one quanta=204.8ns
pfc0_send_interval	16'b0	0x2a	Pfc0 flow control transmit interval time, in quanta, one quanta=204.8ns
pfc1_pause_req_time	16'b0	0x2b	Pfc1 flow control transmit request time, in quanta, one quanta=204.8ns
pfc1_send_interval	16'b0	0x2c	Pfc1 flow control transmit interval time, in quanta, one quanta=204.8ns
pfc2_pause_req_time	16'b0	0x2d	Pfc2 flow control transmit request time, in quanta, one quanta=204.8ns
pfc2_send_interval	16'b0	0x2e	Pfc2 flow control transmit interval time, in quanta, one quanta=204.8ns
pfc3_pause_req_time	16'b0	0x2f	Pfc3 flow control transmit request time, in quanta, one quanta=204.8ns
pfc3_send_interval	16'b0	0x30	Pfc3 flow control transmit interval time, in quanta, one quanta=204.8ns
pfc4_pause_req_time	16'b0	0x31	Pfc4 flow control transmit request time, in quanta, one quanta=204.8ns
pfc4_send_interval	16'b0	0x32	Pfc4 flow control transmit interval time, in quanta, onequanta=204.8ns
pfc5_pause_req_time	16'b0	0x33	Pfc5 flow control transmit request time, in quanta, one quanta=204.8ns
pfc5_send_interval	16'b0	0x34	Pfc5 flow control transmit interval time, in quanta, one quanta=204.8ns
pfc6_pause_req_time	16'b0	0x35	Pfc6 flow control transmit request time, in quanta, one quanta=204.8ns
pfc6_send_interval	16'b0	0x36	Pfc6 flow control transmit interval time, in quanta, one quanta=204.8ns,
pfc7_pause_req_time	16'b0	0x37	Pfc7 flow control transmit request time, in quanta, one quanta=204.8ns
pfc7_send_interval	16'b0	0x38	Pfc7 flow control transmit interval time, in quanta, one quanta=204.8ns

Transmit statistics is for various statistical functions for messages transmitted.

Table 3-3 Transmission Statistics Register Addresses

Register	Defaults	Address	Description
tx_total	64'h0	0x0/0x1	Total transmitted message statistics
tx_byte	64'h0	0x2/0x3	Total transmitted message bytes statistics
tx_less_64byte	64'h0	0x4/0x5	Statistics of transmitted messages with less than 64 bytes
tx_64byte	64'h0	0x6/0x7	Statistics of 64-byte messages transmitted
tx_65_ 127byte	64'h0	0x8/0x9	Statistics of transmitted messages with 65-127 bytes
tx_ 128_255byte	64'h0	0xa/0xb	Statistics of transmitted messages with 128-255 bytes
tx_256_511byte	64'h0	0xc/0xd	Statistics of transmitted messages with 256-511 bytes

tx_512_ 1023byte	64'h0	0xe/0xf	Statistics of transmitted messages with 512-1023 bytes
tx_ 1024_ 1518byte	64'h0	0x10/0x11	Statistics of transmitted messages with 1024-1518 bytes
tx_ 1518_max	64'h0	0x12/0x13	Statistics of transmitted messages with greater than 1518 bytes
tx_control	64'h0	0x18/0x19	Statistics of control frames transmitted
tx_puase	64'h0	0x1a/0x1b	Statistics of pause frames transmitted
tx_pfc	64'h0	0x1c/0x1d	Statistics of pfc frames transmitted

Note: Each statistic item corresponds to two addresses, the lower address corresponds to the lower 32 bits of the statistical value, and the upper address corresponds to the upper 32 bits of the statistical value.

Receive statistics is for various statistical functions of messages received.

Table 3-4 Reception Statistics Register Addresses

Register	**Defaults**	**Address**	**Description**
rx_total	64'h0	0x0/0x1	Total statistics of messages received
rx_byte	64'h0	0x2/0x3	Total byte statistics of messages received
rx_less_64byte	64'h0	0x4/0x5	Statistics of received messages with less than 64 bytes
rx_64byte	64'h0	0x6/0x7	Statistics of 64-byte messages received
rx_65_ 127byte	64'h0	0x8/0x9	Statistics of received messages with 65–127 bytes
rx_ 128_255byte	64'h0	0xa/0xb	Statistics of received messages with 128–255 bytes
rx_256_511byte	64'h0	0xc/0xd	Statistics of received messages with 256–511 bytes
rx_512_ 1023byte	64'h0	0xe/0xf	Statistics of received messages with 512–1023 bytes
rx_ 1024_ 1518byte	64'h0	0x10/0x11	Statistics of received messages with 1024–1518 and above bytes
rx_ 1518_max	64'h0	0x12/0x13	Statistics of received messages with greater than 1518 bytes
rx_crc_err	64'h0	0x14/0x15	Statistics of received CRC error messages
rx_good	64'h0	0x16/0x17	Statistics of received correct messages
rx_control	64'h0	0x18/0x19	Statistics of received control frames
rx_puase	64'h0	0x1a/0x1b	Statistics of received pause frames
rx_pfc	64'h0	0x1c/0x1d	Statistics of received pfc frames

Note: Each statistic item corresponds to two addresses, the lower address corresponds to the lower 32 bits of the statistical value, and the upper address corresponds to the upper 32 bits of the statistical value.

Chapter 4 Reference Design

4.1 Reference Function Design

The following figure shows the block diagram of the reference design provided. The 2.5G Ethernet system can verify the data transmitted and received through docking with third-party devices. The module functions are introduced as follows:

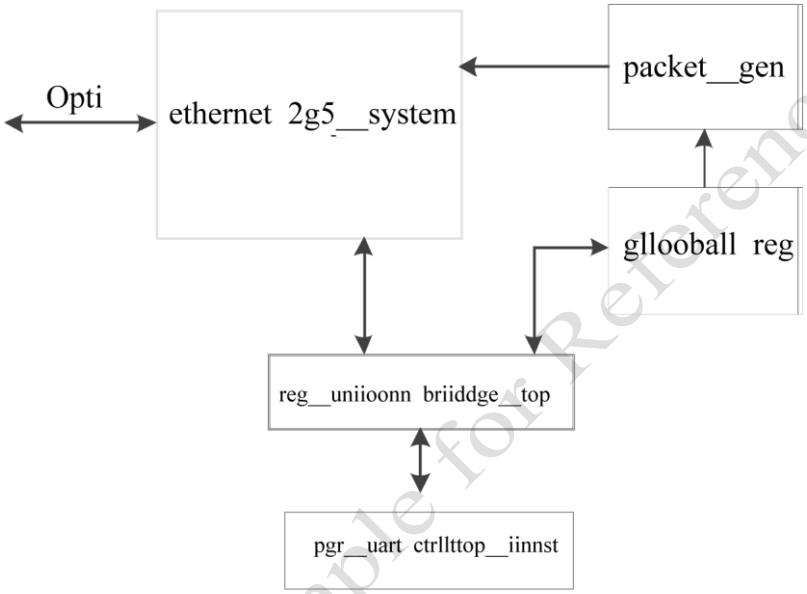

Figure 4-1 2.5G Ethernet Design

packet_gen module

Generates messages with random or fixed packet lengths based on configurations.

Ethernet_2g5_system module

2.5G Ethernet system reference design

global_reg module

Global configuration register, configuring packet transmit modes, etc.

reg_union_bridge_top module

Register address space allocation

Table 4-1 Register Address Allocation

Addr[20]=1'b0	Access global register space
Addr[20]=1'b1	Access PCS/MAC register space

pgr_uart_ctrl_top_inst module

The serial port module, with a fixed baud rate of 115200, receives UART data and outputs data in the format required by the APB protocol during debugging. For read and write operations, the address width is 24 bits (higher 5 bits are 0), and the data width is 32 bits.

The format for read and write operations through UART is:

Read: 72 + address (byte-reversed)

Write: 77 + address (byte-reversed) + data (byte-reversed)

Example of serial port read and write:

Read the value of the configuration register at address 0x13 and change the value of this register to 1.

Read: 72130000

Write: 7713000001000000

4.2 Reference Design Interface List

Table 4-2 Reference Design Interface List

Signal Name	**I/O**	**Bit width**	**Description**
Global signals			
i_free_clk	Input	1	External clock input, with a frequency of 50MHz
sys_rst	Input	1	System reset interface, reset at a high level
HSSTHP-port signal			
ref_clk_n	Input	1	HSSTHP differential reference clock negative end, 125MHz
ref_clk_p	Input	1	HSSTHP differential reference clock positive end, 125MHz
rxn_2g5	Input	1	HSSTHP differential data input negative end
rxp_2g5	Input	1	HSSTHP differential data input positive end
txn_2g5	Output	1	HSSTHP differential data output negative end

Signal Name	I/O	Bit width	Description
txp_2g5	Output	1	HSSTHP differential data output positive end
Status signals			
led1	Output	1	Test signals
led2	Output	1	Test signals
SFP_TX_DISABLE	Output	2	Optical module enable signal
Serial port signals			
txd	Output	1	Serial port transmit
rxd	Input	1	Serial port receive

4.3 Reference Design File Directory

Design Instance Directory Structure Diagram

```
├─docs                                  //Application guide
├─ipcore                                //IP directory
│  ├─hsst_2g5                           //HSSTLP ip
├─pnr                                   //Project directory
│  ├─ethernet_2g5_system_ads            //ADS project directory
│  │  ├─seth_2g5.fdc                    //Constraint file
│  │  ├─ethernet_2g5_system_ads.pds     //Project files
│  ├─ethernet_2g5_system_syn            //Synplify project directory
│  │  ├─seth_2g5.fdc                    //Constraint file
│  │  ├─ethernet_2g5_system_syn.pds     //Project files
├─source                                //Source file directory
│  ├─eth_2g5_top_pg21100h.v             //Test project top level
│  ├─packet_gen_16bit.v                 //Packet transmission module
│  ├─global_reg.v                       //Test project global register file
│  ├─reg_union_bridge_top.v             //Test project address allocation file
│  ├─apb_addr_divide.v                  //Test project register address allocation module
│  ├─clk_cal.v                          //Frequency test module
│  ├─reg_sync.v                         //Synchronization module
│  ├─prbs_any.v                         //PRBS generation module
│  ├─pcs_mac                            //ADS synthesis encryption code
│  │  ├─ethernet_2g5_sytem.v            //Reference design top level module
│  │  ├─eth_2g5_v1_5_vpAll.vp           //Reference design synthesis and simulation encryption source code (supports ADS,synplify synthesis and modelsim, VCS simulation)
│  │  ├─apb_addr_divide.v               //Reference design address allocation module
│  │  ├─system_global_reg.v             //Reference design global register file
│  ├─uart_ctrl_32bit                    //Serial port to APB interface code
├─sim                                   //Modelsim simulation script directory
│  ├─eth_2g5_system_filelist.f          //Simulation file lis
│  ├─eth_2g5_system_sim.do              //Simulation script
│  ├─eth_2g5_system_wave.do             //Waveform file
├─sim_vcs                               //VCS simulation script directory
│  ├─eth_2g5_system_filelist.f          //Simulation file list
│  ├─makefile                           //Simulation script
│  ├─hsst_2g5_vcs.v                     //HSST VCS simulation top layer
├─testbench                             //Simulation top level
│  ├─ethernet_2g5_sytem_tb.v            //Simulation top level file
```

Figure 4-2 File Directory

4.4 Reference Design Simulation

After setting up the simulation environment, open the "sim" directory to run the "sim.bat" script. For detailed simulation steps, refer to sgmii ip or qsgmiiip simulation description.

4.5 Reference Design On-board Verification

For on-board verification, P02L100KF01_A0 board docks with a third-party IP for testing, achieving board-to-board docking via optic fibre. The 100H demo board transmits random or fixed packet lengths. The third-party IP performs loopback and reads MAC statistics transmitted and received on the 100H demo board to check for consistency and CRC errors.

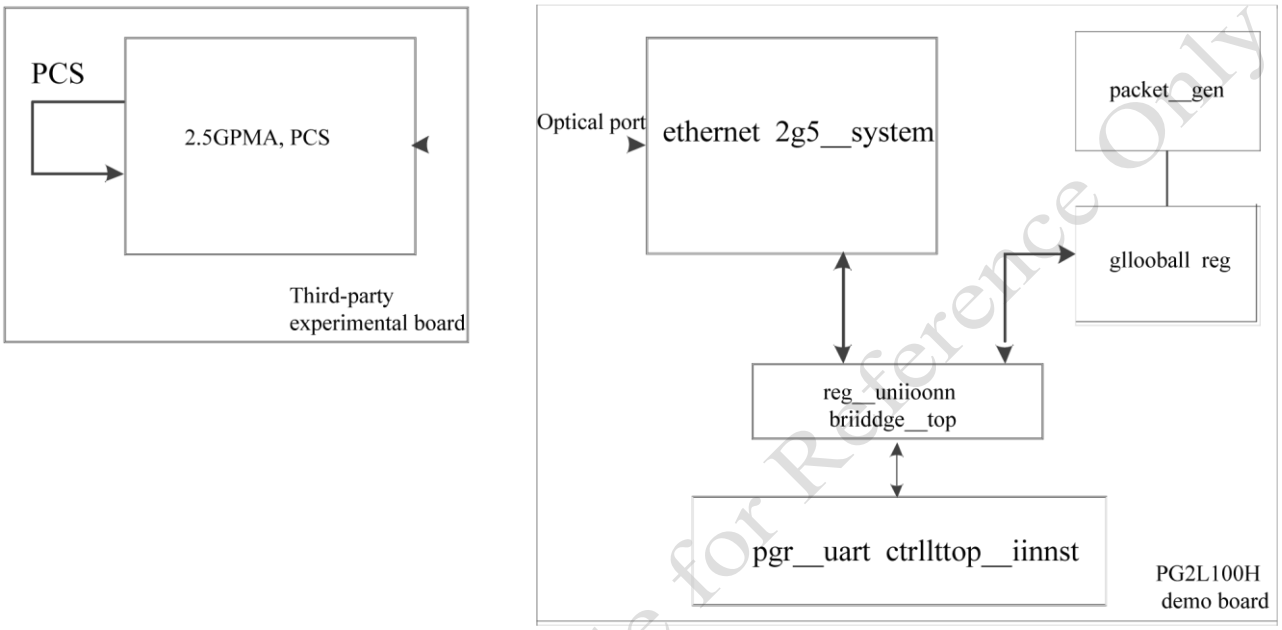

Figure 4-3 Reference Design On-board Verification Block Diagram

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