3G-SDI IP

User Guide

(UG042002, V1.4)

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Revisions History

Document Revisions

Version	Date of Release	Revisions	Applicable IP and Corresponding Versions
V1.4	04.08.2023	Initial release.	V1.4

IP Revisions

IP Version	Date of Release	Revisions
V1.4	04.08.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
3G-SDI	SMPTE STANDARD, Source Image Format and Ancillary Data Mapping for the 3 Gb/s Serial Interface.
APB	Advanced Peripheral Bus
HD-SDI	SMPTE STANDARD, 1.5 Gb/s Signal/Data Serial Interface
HSSTLP	High Speed Serial Transceiver Low Performance
SMPTE	The Society of Motion Picture and Television Engineers
SMPTE 165	RP 165 1994 Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television
SMPTE 168	RP 168 2002 Definition of Vertical Interval Switching Point for Synchronous Video Switching
SMPTE 292	ST 292-1 2012 1.5 Gb/s Signal / Data Serial Interface
SMPTE 352	ST 352 2013 Payload Identification Codes for Serial Digital Interfaces
SMPTE 372	ST 372 2017 Dual Link 1.5 Gb/s Digital Interface for 1920 ×1080 and 2048 ×1080 Picture Formats
SMPTE 424	ST 424 2012 3 Gb/s Signal/Data Serial Interface
SMPTE 425	ST 425-1 2017 Source Image Format and Ancillary Data Mapping for the 3 Gb/s Serial Interface
UI	User Interface
IPC	IP Compiler
PDS	Pango Design Suite

Related Documentation

The following documentation is related to this manual:

1. ***Pango_Design_Suite_Quick_Start_Tutorial***
2. ***Pango_Design_Suite_User_Guide***
3. ***IP_Compiler_User_Guide***
4. ***Simulation_User_Guide***
5. ***User_Constraint_Editor_User_Guide***
6. ***Physical_Constraint_Editor_User_Guide***
7. ***Route_Constraint_Editor_User_Guide***
8. ***Fabric_Debugger_User_Guide***
9. ***Fabric_Inserter_User_Guide***

10. UG041004_HSSTLP_IP

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Chapter 1 Preface

This chapter describes the scope, structure, and writing standards of this manual to help users quickly find the information they need.

1.1 Introduction of the Manual

This manual serves as a user guide for the 3G-SDI IP product launched by Pango Microsystems, primarily including the IP user guide and related information. This manual helps users quickly understand the features and usage of 3G-SDI IP.

1.2 Writing Standards of the Manual

Table 1-1 Description of Writing Standards

Text	**Rules**
Attention	If users ignore the attention contents, they may suffer adverse consequences or fail to operate successfully due to incorrect actions.
Description	Instructions and tips provided for users.
Recommendation	Recommended settings and instructions for users.

Chapter 2 IP User Guide

This chapter provides a guide on the use of 3G-SDI IP, including an introduction to IP, IP block diagram, IP generation process, Example Design, IP interface description, IP register description, typical applications, instructions and considerations, and IP debugging methods. More details on the design process can be found in the following PDS help documentation.

- "***Pango_Design_Suite_Quick_Start_Tutorial***"
- "***Pango_Design_Suite_User_Guide***"
- "***IP_Compiler_User_Guide***"
- "***Simulation_User_Guide***"

2.1 IP Introduction

3G-SDI IP is to implement SMPTE format video transmission by Pango Microsystems, which can be configured and generated using the IPC (IP Compiler) tool in the company's PDS (Pango Design Suite).

2.1.1 Key Features

3G-SDI IP is designed according to SMPTE standards, with the main features as follows.

- SD-SDI (SMPTE 259) interface rate 270 Mb/s;
- HD-SDI (SMPTE 292) interface rate 1.485 Gb/s or 1.485/1.001 Gb/s;
- 3G-SDI (SMPTE 424 & SMPTE 425, Level A, Level B-DL, Level B-DS) interface rate 2.97 Gb/s or 2.97/1.001 Gb/s;
- Automatic detection of SDI standards and code rates for received data;
- Automatic detection of video transmission format;
- Detect and capture SMPTE 352 (Payload ID) packets;
- Check for CRC errors in HD-SDI and 3G-SDI;
- Check for EDH (SMPTE 165) errors in SD-SDI (optional);
- Allow for a maximum frequency offset of ±200ppm;

- Supports dynamic switching of SD-SDI, HD-SDI and 3G-SDI interface modes;
- HD-SDI and 3G-SDI support 1x rate or 1/1.001x rate[1] (dynamic rate switching not supported);
- Supports generation and insertion of SMPTE 352 (Payload ID) packets in all SDI modes;
- Supports generation and insertion of CRC and line numbers (LN) in HD-SDI and 3G-SDI modes;
- Supports generation and insertion of EDH (SMPTE 165) packets in SD-SDI mode (optional);
- Generation of Dual Link HD (optional);
- The supported interface protocols/video formats are shown in Table 2-1.

Table 2-1 List of Interface Protocols/Video Formats

Interface Protocols	**Video Standards**	**Sampling Structure/Bit Depth**	**Frame/Field Rate (Hz)**
SD-SDI SMPTE 259-C	PAL	4:2:2 Y'CB'CR' 10-bit or 8-bit	50
	NTSC	4:2:2 Y'CB'CR' 10-bit or 8-bit	59.94
HD-SDI SMPTE 292	SMPTE 274	4:2:2 Y'CB'CR' 10-bit	1080p[2]: 23.98, 24, 25, 29.97, 30 1080i[3]: 50, 59.94, 60 1080PsF[4]: 23.98, 24, 25, 29.97, 30
	SMPTE 296	4:2:2 Y'CB'CR' 10-bit	720p: 23.98, 24, 25. 29.97, 30, 50, 59.94, 60
	SMPTE 260	4:2:2 Y'CB'CR' 10-bit	1035i: 59.94, 60
	SMPTE 2048-2	4:2:2 Y'CB'CR' 10-bit	1080p: 23.98, 24, 25, 29.97, 30
3G-SDI Level A SMPTE 425-A	SMPTE 274	4:2:2 Y'CB'CR' 10-bit	1080p: 50, 59.94, 60
		4:4:4 Y'CB'CR' or RGB 10-bit 4:4:4:4 Y'CB'CR'A or RGBA 10-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
		4:4:4 Y'CB'CR' or RGB 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
		4:2:2 Y'CB'CR' 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
	SMPTE 296	4:4:4 or 4:4:4:4 Y'CB'CR' or RGB 10-bit	720p: 23.98, 24, 25. 29.97, 30, 50, 59.94, 60
	SMPTE 428-9	4:4:4 X'Y'Z' 12-bit	1080p: 24 1080PsF: 24

1 For HD-SDI, 1x rate represents 1.485Gb/s while 1/1.001x rate represents 1.485/1.001 Gb/s; for 3G-SDI, 1x rate represents 2.97 Gb/s while 1/1.001x rate represents 2.97/1.001 Gb/s; the same for below.

2 p: Progressive.

3 i: Interlaced.

4 PsF: Progressive segmented frame.

Interface Protocols	Video Standards	Sampling Structure/Bit Depth	Frame/Field Rate (Hz)
	SMPTE 428-19	4:4:4 X'Y'Z' 12-bit	1080p: 25, 30 1080PsF: 25, 30
	SMPTE 2048-2	4:2:2 Y'CB'CR' 10-bit	1080p: 47.95, 48, 50, 59.94, 60
		4:4:4 Y'CB'CR' or RGB 10-bit 4:4:4:4 Y'CB'CR'A or RGBA 10-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
		4:4:4 Y'CB'CR' or RGB 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
		4:2:2 Y'CB'CR' 12-bit 4:2:2:4 Y'CB'CR'A 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
3G-SDI Level A SMPTE 425-B-DL	SMPTE 372	Refer to Dual Link HD-SDI SMPTE 372	
3G-SDI Level A SMPTE 425-B-DS	2 x HD-SDI Streams	Refer to HD-SDI SMPTE 292	
Dual Link HD-SDI SMPTE 372	SMPTE 274	4:2:2 Y'CB'CR' 10-bit	1080p: 50, 59.94, 60
		4:4:4 or 4:4:4:4 Y'CB'CR' or RGB 10-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
		4:4:4 Y'CB'CR' or RGB 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
		4:2:2 Y'CB'CR' 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080i: 50, 59.94, 60 1080PsF: 23.98, 24, 25, 29.97, 30
	SMPTE 428-9	4:4:4 X'Y'Z' 12-bit	2048 X 1080p: 24
	SMPTE 428-19	4:4:4 X'Y'Z' 12-bit	1080p: 25, 30 1080PsF: 25, 30
	SMPTE 2048-2	4:2:2 Y'CB'CR' 10-bit	1080p: 47.95, 48, 50, 59.94, 60
		4:4:4 Y'CB'CR' or RGB 10-bit 4:4:4:4 Y'CB'CR'A or RGBA 10-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
		4:4:4 Y'CB'CR' or RGB 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30
		4:2:2 Y'CB'CR' 12-bit 4:2:2 Y'CB'CR'A 12-bit	1080p: 23.98, 24, 25, 29.97, 30 1080PsF: 23.98, 24, 25, 29.97, 30

2.1.2 Applicable Devices and Packages

Table 2-2 3G-SDI IP Applicable Devices and Package

Applicable Devices	Supported Packages
PG2L100H	ALL
PG2L100HX	ALL

2.2 IP Block Diagram

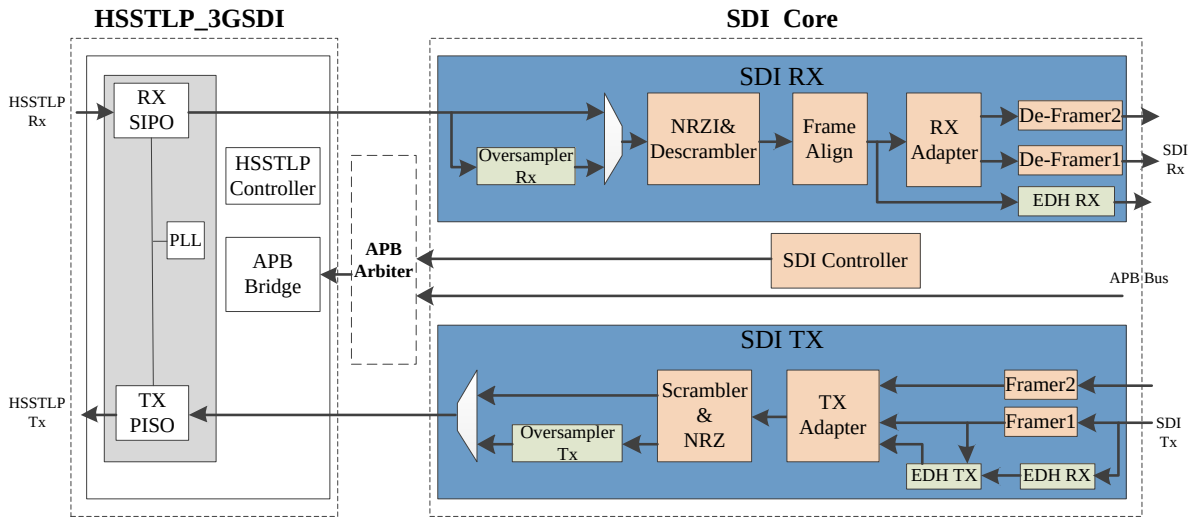

Figure 2-1 3G-SDI IP System Block Diagram

The 3G-SDI IP system block diagram is shown in Figure 2-1. 3G-SDI IP comprises of HSSTLP_3GSDI, SDI Core, and APB Arbiter.

2.2.1 HSSTLP_3GSDI

HSSTLP_3GSDI is instantiated from HSSTLP IP, including HSSTLP hard core resources as well as HSSTLP Controller and APB Bridge soft core logic.

- HSSTLP_3GSDI is only responsible for serial-to-parallel conversion and data processing across clock regions without protocol processing such as encoding/decoding, the parallel interface width being fixed at 20 bits;
- REF_CLK or REF_CLK/1.001 can be selected as the HSSTLP_3GSDI reference clock frequency, and REF_CLK can be configured through the HSSTLP IP interface, with a default value of 148.5MHz;
- HSSTLP Controller manages power-up/reset/rate switching control for HSSTLP_3GSDI, and APB Bridge controls the APB interface.

Attention:

For HSSTLP IP, please use the built-in HSSTLP_3GSDI module instantiated by 3G-SDI IP. Please refer to "2.4.3.4.1 HSSTLP_3GSDI Description" for the details.

2.2.2 SDI Core

SDI Core is the soft core resource to implement logical functions including the SDI receiver, transmitter and controller.

2.2.3 APB Arbiter

Access to internal registers of HSSTLP_3GSDI.

2.3 IP Generation Process

2.3.1 Module Instantiation

Users can customise the configuration of 3G-SDI IP via the IPC tool to instantiate the required IP modules. For detailed instructions on using the IPC tool, please refer to ***"IP_Compiler_User_Guide"***.

The main steps for instantiating the 3G-SDI IP module are described as follows.

2.3.1.1 Selecting IP

Open IPC and click File > Update in the main window to open the Update IP dialog box, where you add the corresponding version of the IP model.

After selecting the FPGAs device type, the Catalog interface displays the loaded IP models. Select the corresponding version of HD/3G-SDI under the "System/Ethernet" directory. The IP selection path is shown in Figure 2-2. Then set the Pathname and Instance Name on the right side of the page. The project instantiation interface is shown in Figure 2-3.

Attention:

The software version must be 2021.1 or above.

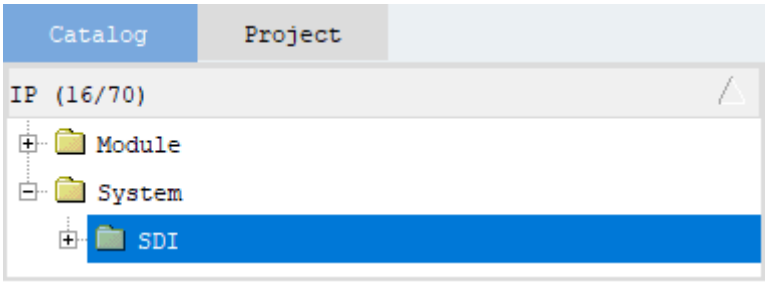

Figure 2-2 3G-SDI IP Selection Path

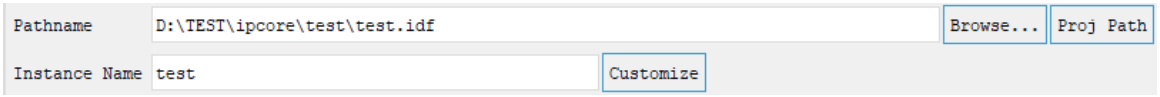

Figure 2-3 Project Instantiation Interface

2.3.1.2 IP Parameter Configuration

After selecting the IP, click <Customize> to enter the 3G-SDI IP parameter configuration interface. The left Symbol is the interface block diagram, as shown in Figure 2-4; the Parameter Configuration window is shown on the right side, as shown in Figure 2-5.

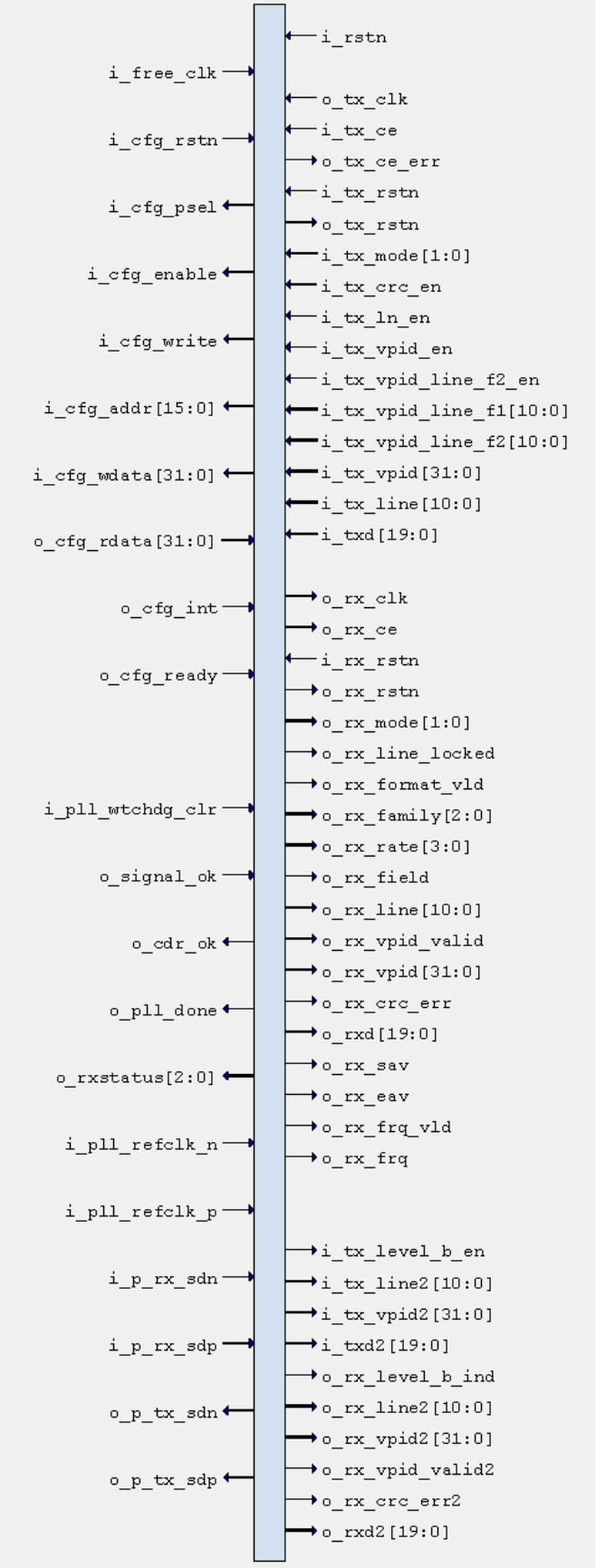

Figure 2-4 3G-SDI IP Interface Block Diagram

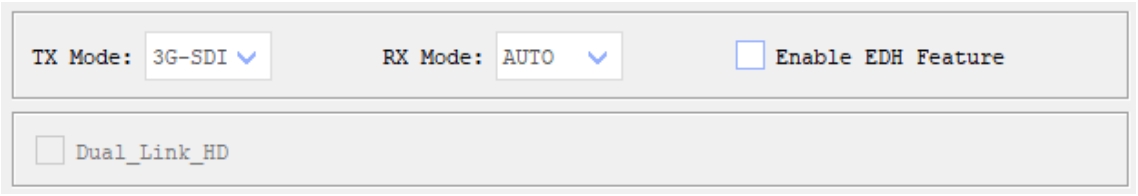

Figure 2-5 3G-SDI IP Parameter Configuration Interface

Table 2-3 3G-SDI IP Configuration Parameter Description

Parameter/Configuration Options	**Parameter Description**	**Default Value**
TX Mode	Transmitter mode configuration SD-SDI: The TX power-up initial state is in SD-SDI mode HD-SDI: The TX power-up initial state is in HD-SDI mode 3G-SDI: The TX power-up initial state is in 3G-SDI mode	3G-SDI
RX Mode	Receiver mode configuration AUTO: Automatic detection of the received data by RX (3G-SDI/HD-SDI/SD-SDI) SD-SDI: Fixed detection by RX to verify if the received data is SD-SDI data HD-SDI: Fixed detection by RX to verify if the received data is HD-SDI data 3G-SDI: Fixed detection by RX to verify if the received data is 3G-SDI data	AUTO
Enable EDH Feature	EDH packet processing function enable control Valid only when TX MODE is set to SD-SDI or RX MODE is set to SD-SDI/AUTO	Disabled
Dual_Link_HD	Dual Link HD application reference design generation control Valid only when TX MODE is set to HD-SDI and the RX MODE is set to HD-SDI	Do not generate

2.3.1.3 Generating IP

After completing the parameter configuration, click the <Generate> button in the top left corner to generate the 3G-SDI IP code corresponding to the user-specific settings. The information report interface for IP generation is shown in Figure 2-6.

Figure 2-6 3G-SDI IP Generation Report Interface

Attention:

The .pds and .fdc files generated with the IP apply to PG2L100H-6FBG676 and are for reference only; please modify the pin constraints according to the actual pin connections when in use.

Upon successful IP generation, the files indicated in Table 2-4 will be output to the Project path specified in Figure 2-3.

Table 2-4 Output Files after 3G-SDI IP Generation

Output File[5]	**Description**
<instance_name>.v	The top-level .v file of the generated IP.
<instance_name>.idf	The Configuration file of the generated IP.
< project_path >/rtl/*.v	The plaintext RTL files of the generated IP.
<project_path>/rtl/hsstlp/ips_sdi_hsstlp/	The plaintext RTL files of the generated IP; this folder contains related files of the HSSTLP module.
<project_path>/rtl/hsstlp/hsstlp_txdl_rxdl/	The plaintext RTL files of the generated IP; this folder contains related files of the Dual Link HD HSSTLP module.
<project_path>/rtl/synplify/*.vp	The non-plaintext RTL code files of the generated IP.
<project_path>/sim_lib/ModelSim/*_sim.vp	The non-plaintext RTL files of the generated IP, which can only be used for ModelSim simulation.
<project_path>/sim/modelsim/*.f	The list of .v and .vp files required for ModelSim simulation of the generated Example Design.
<project_path>/sim/modelsim/*.do	The do script files and do waveform files for ModelSim simulation of the generated Example Design.
<project_path>/sim/modelsim/*.bat	The script for ModelSim simulation of the generated Example Design.
<project_path>/example_design/bench/ips_sdi_onboard_tb.v	DUT layer simulation test bench.
<project_path>/example_design/bench/ips_sdi_dl_onboard_top_tb.sv	Dual Link HD DUT layer simulation test bench.
<instance_name>/example_design/rtl/*.v	Several used module files, and DUT layer and top-level files of the Example Design. For specific details, please refer to the module description of the Example Design in this chapter.
<project_path>/pnr/example_design/ips_sdi_onboard_top.pds	The project file of the Example Design.
<project_path>/pnr/example_design/ips_sdi_onboard_top.fdc	The constraint file of the Example Design.
<project_path>/pnr/example_design/ips_sdi_dl_onboard_top.pds	The project file of the Dual Link HD Example Design.

5 <$instname> is the instantiation name entered by the user; "*" is a wildcard character used to replace files of the same type.

Output File[5]	Description
<project_path>/pnr/example_design/ips_sdi_dl_onboard_top.fdc	The constraint file of the Dual Link HD Example Design.
/rev_1	The default output path for synthesis reports. (This folder is generated only after specifying the synthesis tool)
readme.txt	The readme file describes the structure of the generation directory after the IP is generated.

2.3.2 Constraint Configuration

For the specific configuration method of constraint files, please refer to the relevant help documents in the PDS installation path: "***User_Constraint_Editor_User_Guide***", "***Physical_Constraint_Editor_User_Guide***", "***Route_Constraint_Editor_User_Guide***".

2.3.3 Simulation Runs

The simulation of 3G-SDI IP is based on the Test Bench of the Example Design. For detailed information about Example Design, please refer to "2.4 Example Design".

For more details about the PDS simulation functions and third-party simulation tools, please consult the related help documents in the PDS installation path: "***Pango_Design_Suite_User Guide***", "***Simulation_User_Guide***".

In the Windows system, after IP generation, double-click the *.bat file under the <project_path>/sim/modelsim directory to run the simulation using modelsim10.1a. After the simulation finishes, the specific simulation results will be saved in the vsim_ips_sdi_onboard.log file. The Modelsim simulation waveform is shown as Figure 2-7.

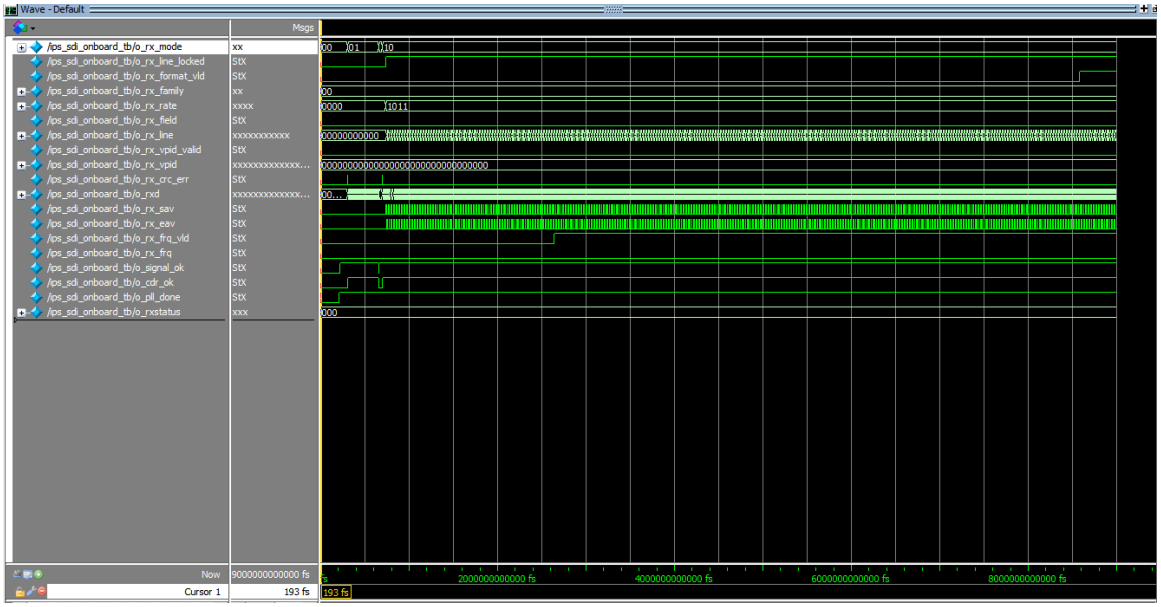

Figure 2-7 Modelsim Simulation Waveform

2.3.4 Synthesis and Placement/Routing

The specific usage of PDS synthesis tools and placement/routing tools can be found in the help documents within the PDS installation path.

Attention:

Example Design project files .pds and pin constraint files .fdc generated with the IP are located in the "/pnr/example_design" directory, and physical constraints need to be modified according to the actual devices and PCB trace routing. For details, please refer to "2.8 Descriptions and Considerations".

2.3.5 Resources Utilization

Table 2-5 Typical Resource Utilization Values for 3G-SDI IP Based on Applicable Device

Device	Configuration Mode			Typical Resource Utilization Values			
	TX Mode	RX Mode	EDH	LUT	FF	HSSTLP	USCM
PG2L100H	3G-SDI	AUTO	Disabled	1982	2079	0.5[6]	3
	3G-SDI	AUTO	Enabled	2293	2328	0.5	3
	SD-SDI	AUTO	Disabled	1761	1847	0.5	3
	SD-SDI	AUTO	Enabled	2497	2622	0.5	3

2.4 Example Design

This section mainly introduces the Example Design scheme based on 3G-SDI IP. This scheme illustrates the instantiation of self-loopback data transmission and reception by 3G-SDI IP, verifying the correctness of received data through cyclic redundancy check (CRC) and reflecting the link status via DebugCore.

2.4.1 Design Block Diagram

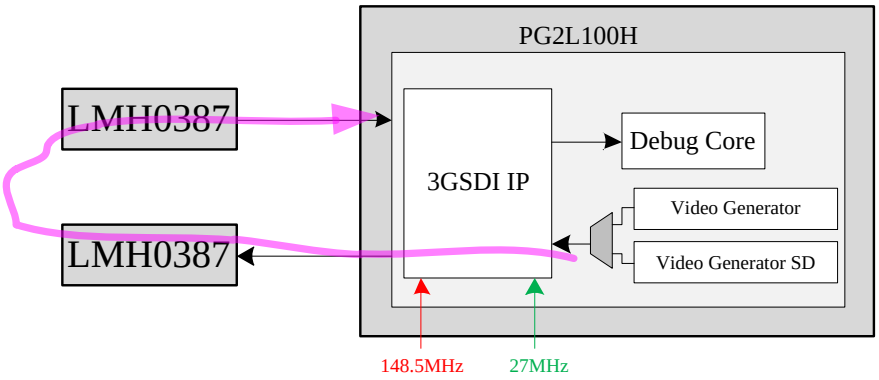

Figure 2-8 Example Design System Block Diagram

The system block diagram of the Example Design is as shown in Figure 2-8. The

6 The utilization of 0.5 for HSSTLP indicates that only 1 channel was used. If not all the 4 channels are used, the HSSTLP utilization rate is 0.5.

PG2L100RD04_A0 single board is used for on-boarding, allowing self-loopback by serial connection of a differential/single-ended conversion relay board (LMH0387). Users need to modify the design according to actual conditions.

The logic top layer of the on-board scheme integrates 3G-SDI IP, Video Generator, Video Generator SD and Debug Core.

2.4.2 Descriptions of Ports

The interface descriptions of the Example Design are shown in Table 2-6.

Table 2-6 Example Design Interface List

Signal Name	Pin constraints	I/O	Description
Clock and reset			
i_clk_27m	D4	I	Input clock (27MHz) Used for initialization logic and configuration interface Also serves as the clock for the APB
i_arstn	Y20	I	Reset signal 1: Reset release 0: Reset
User-side signal			
i_3g_hd_sel	H24	I	TX mode configuration 0: i_tx_mode=01 1: i_tx_mode=10
i_sd_sel	G24	I	TX mode configuration 0: i_tx_mode=10 or 01 1: i_tx_mode=00
HSSTLP_3GSDI-end signal			
i_hsst_refclk_p	CLK_0_P	I	Reference clock differential input positive end (HSSTLP dedicated pin) Frequency 148.5MHz
i_hsst_refclk_n	CLK_0_N	I	Reference clock differential input negative end (HSSTLP dedicated pin) Frequency 148.5MHz

2.4.3 Module Description

The modules in the Example Design are described as follows.

2.4.3.1 Video Generator Module

The Video Generator is used to generate 1080p 60Hz RGB colorbars video contents in 3G-SDI mode, and for the 1080p 30Hz RGB colour bars video contents in HD-SDI mode.

Table 2-7 Video Generator and 3G-SDI IP-side Interconnection Interface List

Interface	I/O	Description
i_clk	I	Clock interface (connected to 3G-SDI IP top-level interface o_tx_clk)
i_arstn	I	Asynchronous reset (active low)
o_txd[19:0]	O	Video data stream (connected to 3G-SDI IP top-level interface i_txd[19:0]) i_clk clock domain
o_tx_line[10:0]	O	Line Number (connected to 3G-SDI IP top-level interface i_tx_line[10:0]) i_clk clock domain

2.4.3.2 Video Generator SD Module

In SD-SDI mode, the Video Generator SD generates 625i 50Hz RGB colorbars video contents.

Table 2-8 Video Generator SD and 3G-SDI IP-side Interconnection Interface List

Interface	I/O	Description
i_clk	I	Clock interface (connected to 3G-SDI IP top-level interface o_tx_clk)
i_arstn	I	Asynchronous reset (active low)
i_tx_ce	I	TX clock enable (used only in SD-SDI mode)
o_txd[19:0]	O	Video data stream (connected to 3G-SDI IP top-level interface i_txd[19:0]) i_clk clock domain
o_tx_line[10:0]	O	Line Number (connected to 3G-SDI IP top-level interface i_tx_line[10:0]) i_clk clock domain

2.4.3.3 Debug_core Module

Samples the status signals of 3G-SDI IP, facilitating the observation of the status of 3G-SDI IP.

2.4.3.4 3G-SDI IP Module

The 3G-SDI IP module comprises of SDI Core, HSSTLP_3GSDI, and APB Arbiter modules.

2.4.3.4.1 HSSTLP_3GSDI Description

The HSSTLP_3GSDI instantiated by 3G-SDI IP is generated by Logos2 HSSTLP IP V1.7. In case

of no special requirements, users don't need to modify any documents under the IP directory. Please modify as per actual requirements if necessary (e.g. changing the reference clock source/frequency point).

- Open the -/rtl/hsstlp/ips_sdi_hsstlp/ ips_sdi_hsstlp.idf in the IPC interface to modify the configuration of HSSTLP_3GSDI;
- Modify the top-level logic interface of 3G-SDI IP (-/ <instance_name>.v).

Attention:

For detailed modification methods, please refer to "***UG041004_HSSTLP_IP***".

2.4.3.4.2 SDI Core HSSTLP_3GSDI-side Interconnection Interface Description

Table 2-9 SDI Core HSSTLP_3GSDI-side Interconnection Interface List

Signal Name	I/O	Description
Clock Interface		
i_p_tclk2fabric	I	P_TCLK2FABRIC interface of HSSTLP_3GSDI in clocking scheme
i_p_rclk2fabric	I	P_RCLK2FABRIC interface of HSSTLP_3GSDI in clocking scheme
Reset Interface (free_clk Clock Domain)		
o_hsstlp_rst	O	Global logic reset (active high)
o_hsstlp_tx_rst	O	HSSTLP_3GSDI TX logic reset (active high)
o_hsstlp_rx_rst	O	HSSTLP_3GSDI RX logic reset (active high)
o_hsstlp_cfg_rst	O	HSSTLP_3GSDI APB reset (active high)
SDI Core and HSSTLP_3GSDI Data Interfaces		
o_txd[19:0]	O	TX parallel data (sdi_rx_clk clock domain)
i_rxd[19:0]	I	RX parallel data (sdi_tx_clk clock domain)
HSSTLP_3GSDI RX Status Signal		
i_signal_ok	I	HSSTLP_3GSDI P_RX_SIGDET_STATUS transparent transmission signal (asynchronous signal)
HSSTLP_3GSDI Reset and Rate Switching Interfaces		
i_rxlane_done	I	HSSTLP_3GSDI RX reset completion indication (active high, please refer to "2.8.4 IP Reset Scheme")
i_txlane_done	I	HSSTLP_3GSDI TX reset completion indication (active high, please refer to "2.8.4 IP Reset Scheme")
o_tx_rate_chng	I	High pulse indicates TX rate switching request
o_tx_ckdiv[1:0]	I	01: HD-SDI rate 10: 3G-SDI/SD-SDI rate
o_rx_rate_chng	I	High pulse indicates RX rate switching request

Signal Name	I/O	Description
o_rx_ckdiv[1:0]	I	01: HD-SDI rate 10: 3G-SDI/SD-SDI rate
HSSTLP_3GSDI Register Configuration Interface		
i_p_cfg bus	I	input wire i_cfg_rst input wire i_cfg_psel input wire i_cfg_enable input wire i_cfg_write input wire [15:0] i_cfg_addr input wire [7:0] i_cfg_wdata output wire [7:0] o_cfg_rdata output wire o_cfg_int output wire o_cfg_ready

2.4.3.4.3 APB Arbiter Module

To support oversampling in SD-SDI mode at the receiver, it is necessary to dynamically configure the corresponding registers of HSSTLP_3GSDI. Additionally, 3G-SDI IP also supports access to HSSTLP_3GSDI registers by external APB interfaces. Therefore, the APB Arbiter module is used to enable simultaneous access to HSSTLP_3GSDI internal registers from two APB bus groups. The APB Arbiter module adopts a polling arbitration mechanism, with each bus group weighing 50%.

Taking the first bus group access as an example, the simulation timing waveform is shown in Figure 2-9. When the state machine is in the IDLE state, the sel signal toggles every clock cycle. For the IDLE state (0), when both the i_cfg_psel_0 signal and the i_cfg_enable_0 signal of the first bus group are detected at 1, and the sel signal is 0, then the state machine enters the BUSY state (1), strobes the first (number 0) APB bus group, and allows access to the internal registers of HSSTLP_3GSDI. After the APB interface of HSSTLP_3GSDI returns the i_cfg_rdata_mux signal, the state machine enters the WAIT state (2). In the WAIT state, the IDLE state won't be resumed until the p_cfg_psel_0 signal of the first bus group goes low.

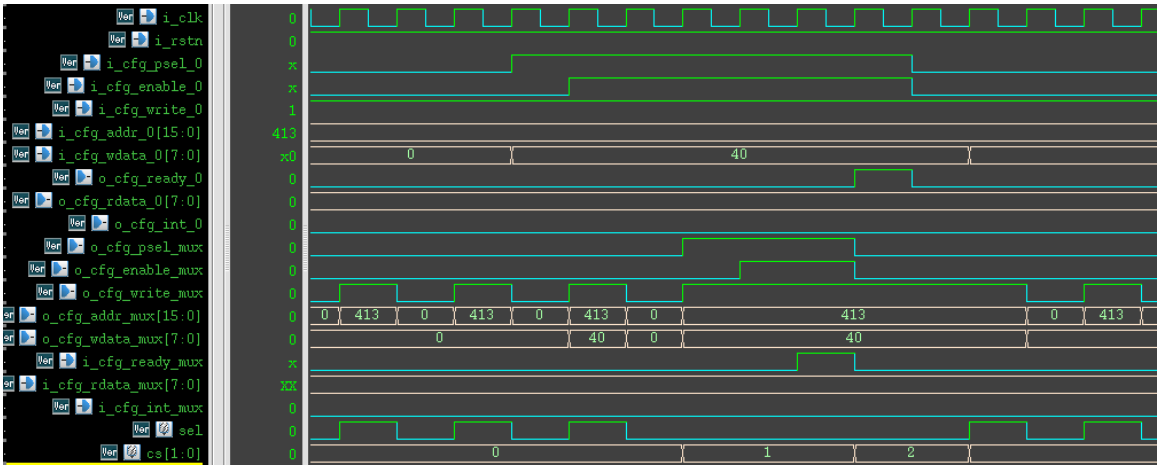

Figure 2-9 APB Arbiter Internal Logical Timing Diagram

2.4.4 Test Method

In the Example Design, users can configure the 3G-SDI IP as needed and detect the link error status via DebugCore. The Debug Core signals are listed in Table 2-10.

Table 2-10 Debug Core Signal List

DEBUG CORE signal	**Project Signal Name**	**Description**
TriggerPort0[255:87]	Not used	The value is 0.
TriggerPort0[86:85]	o_rx_mode[1:0]	00: SD 01: HD (including Dual Link HD) 10: 3G Others: Reserved
TriggerPort0[84]	o_rx_line_locked	1: Received image frame locked
TriggerPort0[83]	o_rx_format_vld	1: Video transmission format valid Valid only when o_rx_line_locked=1
TriggerPort0[82:80]	o_rx_family[2:0]	Video transmission format (valid only when o_rx_format_vld=1) 000: SMPTE ST 274 (1920 x 1080) 001: SMPTE ST 296 (1280 x 720) 010: SMPTE 2048-2 (2048 x 1080) 100: NTSC (720 x 486) 101: PAL (720 x 576) 111: Unsupported format Others: Reserved

DEBUG CORE signal	Project Signal Name	Description
TriggerPort0[79:76]	o_rx_rate[3:0]	Video transmission format Valid only when o_rx_format_vld=1 (requiring to determine the presence of 1/1.001 relationship in conjunction with o_rx_frq) 0000: None 0011: 24 Hz (progressive) or 48 Hz (interlaced) 0101: 25 Hz (progressive) or 50 Hz (interlaced) 0111: 30 Hz (progressive) or 60 Hz (interlaced) 1000: 48 Hz 1001: 50 Hz 1011: 60 Hz Others: Reserved
TriggerPort0[75]	o_rx_field	Video transmission format (valid only when o_rx_format_vld=1) 1: Interlaced 0: Progressive
TriggerPort0[74:64]	o_rx_line[10:0]	Line Number Valid only in HD-SDI or 3G-SDI mode and when o_rx_format_vld=1
TriggerPort0[63]	o_rx_vpid_valid	1: SMPTE 352 Packet valid Valid only when o_rx_format_vld=1
TriggerPort0[62:31]	o_rx_vpid[31:0]	SMPTE 352 Packet Valid only when o_rx_vpid_valid=1
TriggerPort0[30]	o_rx_crc_err	1: CRC error Valid only in HD-SDI or 3G-SDI mode and when in o_rx_format_vld=1
TriggerPort0[29:10]	o_rxd[19:0]	Valid only when o_rx_format_vld=1 bit19~10: HD-SDI: Y data stream 3G-SDI level A: Data stream 1 SD-SDI: Y&C component bit9~0: HD-SDI: C data stream 3G-SDI level A: Data stream 2 SD-SDI: Not used
TriggerPort0[9]	o_rx_sav	SAV field XYZ words valid indication Valid only when o_rx_format_vld=1
TriggerPort0[8]	o_rx_eav	EAV field XYZ words valid indication Valid only when o_rx_format_vld=1
TriggerPort0[7]	o_rx_frq_vld	o_rx_frq valid indication (free_clk clock domain) Valid only when o_rx_format_vld=1 0: Detection incomplete 1: Detection complete
TriggerPort0[6]	o_rx_frq	Indicates specific frequency (free_clk clock domain) Valid only when o_rx_frq_vld=1 0: Receiving data at 1x rate 1: Receiving data at 1/1.001x rate
TriggerPort0[5]	o_signal_ok	HSSTLP_3GSDI P_RX_SIGDET_STATUS transparent transmission signal (asynchronous signal)
TriggerPort0[4]	o_cdr_ok	HSSTLP_3GSDI CDR ALIGN transparent transmission signal (asynchronous signal)
TriggerPort0[3]	o_pll_done	1: HSSTLP_3GSDI PLL ready (asynchronous signal)
TriggerPort0[2:0]	o_rxstatus[2:0]	HSSTLP_3GSDI RXPCS status signal (sdi_rx_clk clock domain)

Taking a PG2L100RD04_A0 self-loopback connection test as an example, the data from the receiver is fetched through DebugCore (capturing corresponding signals and generating the waveform based on the assignment in the Example Design), as is shown in Figure 2-10.

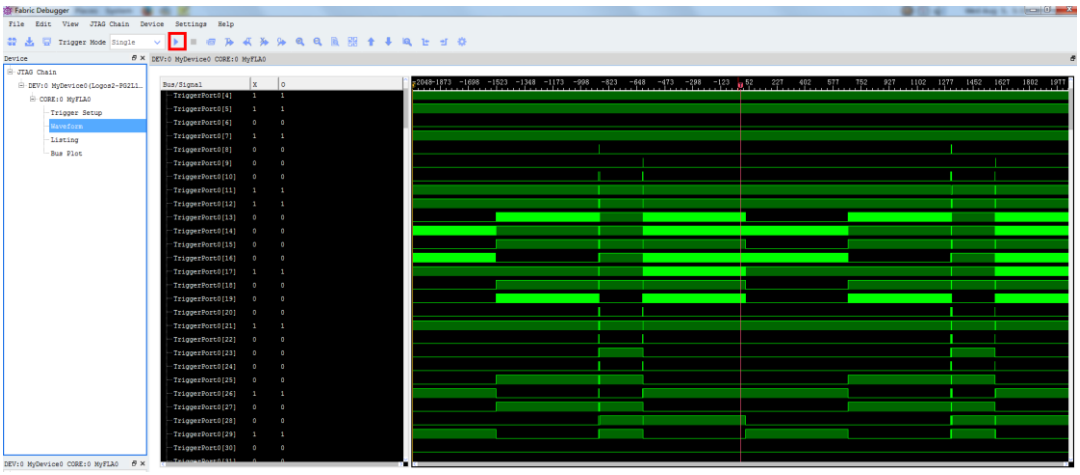

Figure 2-10 Debug Core Waveform Capture

Attention:

Since the on-board testing and verification of the Example Design adopts a self-loopback scheme, the IP interface parameters do not support configuring as the following asymmetric modes.

TX MODE=3G-SDI and RX MODE= HD-SDI;

TX MODE=3G-SDI and RX MODE= SD-SDI;

TX MODE=HD-SDI and RX MODE= 3G-SDI;

TX MODE=HD-SDI and RX MODE= SD-SDI;

TX MODE=SD-SDI and RX MODE= 3G-SDI;

TX MODE=SD-SDI and RX MODE= HD-SDI.

2.5 Descriptions of IP Interfaces

This section provides the interface instructions and timing descriptions related to 3G-SDI IP.

2.5.1 3G-SDI IP Interface Description

Table 2-11 3G-SDI IP Interface Signal List

Signal Name	I/O	Description
Clock Interface		
i_free_clk	I	Input interface of free_clk clock domain (refer to "2.8.3 IP Clock Scheme").
i_pll_refclk_p	I	HSSTLP_3GSDI reference clock differential input positive end (frequency 148.5M, from HSSTLP).
i_pll_refclk_n	I	HSSTLP_3GSDI reference clock differential input negative end (frequency 148.5M, from HSSTLP).
o_tx_clk	O	Output port of sdi_tx_clk clock domain (refer to "2.8.3 IP Clock Scheme").
o_rx_clk	O	Output port of sdi_rx_clk clock domain (refer to "2.8.3 IP Clock Scheme").
Reset Interface[7]		
i_rstn	I	3G-SDI IP global logic reset input (active low, free_clk clock domain).
i_tx_rstn	I	3G-SDI IP TX logic reset input (active low, free_clk clock domain).
i_rx_rstn	I	3G-SDI IP RX logic reset input (active low, free_clk clock domain).
o_tx_rstn	O	3G-SDI IP TX reset signal output (active low, sdi_tx_clk clock domain).
o_rx_rstn	O	3G-SDI IP RX reset signal output (active low, sdi_rx_clk clock domain).
APB Bus Interface (free_clk Clock Domain)		
i_cfg_rstn	I	APB interface reset (For details, please refer to "2.8.4 IP Reset Scheme").
i_cfg_psel	I	HSSTLP_3GSDI APB interface.
i_cfg_enable	I	
i_cfg_write	I	
i_cfg_addr[15:0]	I	
i_cfg_wdata[31:0]	I	
o_cfg_rdata[31:0]	O	
o_cfg_int	O	
o_cfg_ready	O	
HSSTLP_3GSDI Differential Interface		
o_p_tx_sdn	O	HSSTLP_3GSDI TX differential interface N-terminal.
o_p_tx_sdp	O	HSSTLP_3GSDI TX differential interface P-terminal
i_p_rx_sdn	I	HSSTLP_3GSDI RX differential interface N-terminal.
i_p_rx_sdp	I	HSSTLP_3GSDI RX differential interface P-terminal.
3G SDI IP TX Client Side Interface (sdi_tx_clk clock domain signals for all unless otherwise specified)		
i_tx_ce	I	TX clock enable, used for SD-SDI and 3G-SDI Level B modes (refer to Figure 2-13 and Figure 2-14 for timing), and should always be "1" in HD-SDI and 3G-SDI Level A modes.

7 please refer to "2.8.4 IP Reset Scheme" for details.

Signal Name	I/O	Description
i_tx_mode[1:0]	I	TX mode configuration (initial configuration consistent with interface parameter TX MODE, free_clk clock domain). 00: SD-SDI; 01: HD-SDI (including Dual Link HD); 10: 3G-SDI; 11: Reserved.
i_tx_level_b_en[8]	I	Transmitter transmission type configuration, only valid for 3G-SDI mode and fixed input "0" for other modes; only visible when 3G-SDI mode is selected for transmission (static configuration). 1: 3G-SDI Level B; 0: 3G-SDI Level A.
i_tx_crc_en	I	Enable CRC insertion (only valid for HD-SDI and 3G-SDI modes, static configuration[9]). 1: Automatic CRC insertion; 0: Transparent transmission of the corresponding field data.
i_tx_ln_en	I	Enable Line Number insertion (only valid for HD-SDI and 3G-SDI modes, static configuration). 1: Automatic Line Number insertion; 0: Transparent transmission of the corresponding field data.
i_tx_vpid_en	I	Enable SMPTE 352 packet insertion (static configuration). 1: Automatic SMPTE 352 packet insertion; 0: Transparent transmission of the corresponding field data.
i_tx_edh_en[10]	I	Enable EDH packet insertion, only valid for SD-SDI mode (static configuration). 1: Automatic EDH packet insertion; 0: Transparent transmission of the corresponding field data.
i_txd[19:0]	I	The first group of video data stream being transmitted (including TRS/SAV/EAV and other information, please refer to Table 2-12 for bit definitions and Figure 2-11 for timing).
i_txd2[19:0][8]	I	The second group of video data stream being transmitted, used for 3G-SDI Level B mode (including TRS/SAV/EAV and other information, please refer to Table 2-12 for bit definitions and Figure 2-11 for timing).
i_tx_line[10:0]	I	Line Number transmitted by Channel[11] 1&2 (for timing, please refer to Figure 2-11).
i_tx_line2[10:0][8]	I	Line Number transmitted by Channels 3&4, used for 3G-SDI Level B mode (for timing, please refer to Figure 2-11).
i_tx_vpid[31:0]	I	SMPTE 352 Packet transmitted by Channel 2 Y-Stream (for timing, please refer to Figure 2-11).
i_tx_vpid2[31:0][8]	I	SMPTE 352 Packet transmitted by Channel 4 Y-Stream, used for 3G-SDI Level B mode (for timing, please refer to Figure 2-11).

8 When instantiating the IP, the port is only visible when the TX Mode is set to 3G-SDI.

9 Static configuration: Only supports changing before logic reset release; the same for below.

10 When instantiating the IP, the port is only visible when Enable EDH Feature is selected and TX MODE is set to SD-SDI.

11 Channels: For the 20 bits of Framer1/De-Framer1, the lower 10 bits are defined as channel 1, and the higher 10 bits are defined as channel 2; For the 20 bits of Framer2/De-Framer2, the lower 10 bits are defined as channel 3, and the higher 10 bits are defined as channel 4; the same for below.

Signal Name	I/O	Description
i_tx_vpid_line_f1[10:0]	I	Line Number (Field 1) in which the SMPTE 352 Packet is inserted, please refer to i_tx_vpid_line_f2_en (static configuration).
i_tx_vpid_line_f2[10:0]	I	Line Number (Field 2) in which the SMPTE 352 Packet is inserted, please refer to i_tx_vpid_line_f2_en (static configuration).
i_tx_vpid_line_f2_en	I	i_tx_vpid_line_f2 valid indication (static configuration). 1: Both i_tx_vpid_line_f1 and i_tx_vpid_line_f2 valid; 0: Only i_tx_vpid_line_f1 valid.
o_tx_ce_err	O	Valid in SD-SDI and 3G-SDI Level B modes, fixed output "0" for other modes. 1: i_tx_ce signal does not meet timing requirements; 0: i_tx_ce signal meets timing requirements.
o_tx_sd_switch[10]	O	Detect whether a switching (SMPTE RP168) event occurs in the transmitted SD-SDI data stream; only valid in SD-SDI mode, fixed output "0" in other modes. 1: Switching occurred; 0: No switching occurred.
3G-SDI IP RX Client Side Interface (sdi_rx_clk clock domain signals for all unless otherwise specified)		
o_rx_ce	O	RX clock enable, used for SD-SDI and 3G-SDI Level B modes, output "1" in HD-SDI and 3G-SDI Level A modes.
o_rx_mode[1:0]	O	Received data Mode. 00: SD; 01: HD (including Dual Link HD); 10: 3G; Others: Reserved.
o_rx_line_locked	O	Received image frame locked indication, 1: Locked; 0: Unlocked.
o_rx_format_vld	O	Indicates whether the received video detection information is valid, please refer to the specific port description, only valid when o_rx_line_locked=1. 1: Valid; 0: Invalid.
o_rx_family[1:0]	O	Video transmission format, only valid when o_rx_format_vld=1. 000: SMPTE ST 274 (1920 x 1080); 001: SMPTE ST 296 (1280 x 720); 010: SMPTE 2048-2 (2048 x 1080); 100: NTSC (720 x 486); 101: PAL (720 x 576); 111: Unsupported format; others: Reserved.
o_rx_rate[3:0]	O	Video transmission format, only valid when o_rx_format_vld=1 (requiring to determine the presence of 1/1.001 relationship in conjunction with o_rx_frq) 0000: None; 0011: 24 Hz (progressive) or 48 Hz (interlaced); 0101: 25 Hz (progressive) or 50 Hz (interlaced); 0111: 30 Hz (progressive) or 60 Hz (interlaced); 1000: 48 Hz; 1001: 50 Hz; 1011: 60 Hz; others: Reserved.
o_rx_field	O	Video transmission format (only valid when o_rx_format_vld=1). 1: Interlaced; 0: Progressive.

Signal Name	I/O	Description
o_rx_level_b_ind[12]	O	Received transmission type indication, only valid when o_rx_format_vld=1 and in 3G-SDI mode, fixed output '0' for other modes. 1: 3G-SDI Level B; 0: 3G-SDI Level A.
o_rx_line[10:0]	O	Line Number received by Channels 1&2. Only valid in HD-SDI and 3G-SDI modes and when o_rx_format_vld=1.
o_rx_line2[10:0][12]	O	Line Number received by Channels 3&4. Only valid in 3G-SDI Level B mode and when o_rx_format_vld=1, meaningless for other modes.
o_rx_vpid_valid	O	Indicates whether the ST 352 packet received by Channel 2 Y-Stream is valid, valid when o_rx_format_vld=1. 1: Channel 2 ST 352 packet is valid; 0: Channel 2 ST 352 packet is invalid.
o_rx_vpid[31:0]	O	SMPTE 352 packet received by Channel 2 Y-Stream, only valid when rx_vpid_valid=1.
o_rx_vpid_valid2[12]	O	Indicates whether the ST 352 packet received by Channel 4 Y-Stream is valid, only valid in 3G-SDI Level B mode and when o_rx_format_vld=1, meaningless for other modes. 1: Channel 4 ST 352 packet is valid; 0: Channel 4 ST 352 packet is invalid.
o_rx_vpid2[31:0][12]	O	ST 352 packet received by Channel 4 Y-Stream, only valid in 3G-SDI Level B mode and when o_rx_vpid_valid2=1, meaningless for other modes.
o_rx_crc_err	O	Indicates the CRC check errors that occurred for reception operations at Channels 1&2, only valid in HD-SDI and 3G-SDI modes, fixed output "0" for other modes. 1: CRC error present at Channel 1 or 2; 0: No CRC error at Channel 1 or 2;
o_rx_crc_err2[12]	O	Indicates the CRC check errors that occurred for reception operations at Channels 3&4, only valid in 3G-SDI Level B mode, meaningless for other modes. 1: CRC error present at Channel 3 or 4; 0: No CRC error at Channel 3 or 4.
o_rxd[19:0]	O	The first group of video data stream received, only valid when o_rx_format_vld=1 (please refer to Table 2-12 for bit definitions and Figure 2-12 for timing).
o_rxd2[19:0][12]	O	The second group of video data stream received, only valid in 3G-SDI Level B mode and when o_rx_format_vld=1, meaningless for other modes. (please refer to Table 2-12 for bit definitions and Figure 2-12 for timing).
o_rx_eav	O	EAV field XYZ words valid indication, only valid when o_rx_format_vld=1 (refer to Figure 2-12).
o_rx_sav	O	SAV field XYZ words valid indication, only valid when o_rx_format_vld=1 (refer to Figure 2-12).
o_rx_frq_vld	O	o_rx_frq valid indication, only valid when o_rx_format_vld=1 (free_clk clock domain). 1: Detection complete; 0: Detection incomplete.
o_rx_frq	O	Indicates specific frequency, only valid when o_rx_frq_vld=1 (free_clk clock domain). 1: Receiving data at 1/1.001x rate; 0: Receiving data at 1x rate.

12 When instantiating the IP, the port is only visible when the RX Mode is set to 3G-SDI or AUTO.

Signal Name	I/O	Description
o_rx_sd_switch[13]	O	Detect whether a switching (SMPTE RP168) event occurs in the received SD-SDI data stream; only valid in SD-SDI mode, fixed output "0" in other modes. 1: Switching occurred; 0: No switching occurred.
o_rx_edh_ap_crc_err[13]	O	Indicates the Active Picture CRC check errors that occurred for the received EDH packet; only valid in SD-SDI mode, fixed output "0" for other modes. 1: CRC error present; 0: No CRC error.
o_rx_edh_ff_crc_err[13]	O	Indicates the Full Field CRC check errors that occurred for the received EDH packet; only valid in SD-SDI mode, fixed output "0" for other modes. 1: CRC error present; 0: No CRC error.
o_rx_edh_ap_err_flags[4:0][13]	O	Only valid in SD-SDI mode; outputs the AP error flags of the received EDH packet from high to low: ues, ida, idh, eda, edh. Fixed output "0" for other modes.
o_rx_edh_ff_err_flags[4:0][13]	O	Only valid in SD-SDI mode; outputs the FF error flags of the received EDH packet from high to low: ues, ida, idh, eda, edh. Fixed output "0" for other modes.
o_rx_edh_anc_err_flags[4:0][13]	O	Only valid in SD-SDI mode; outputs the ANC error flags of the received EDH packet from high to low: ues, ida, idh, eda, edh. Fixed output "0" for other modes.
o_rx_edh_header_err[13]	O	Indicates whether at least one of the former 4 words (including 3 Ancillary Data Headers and 1 Data ID) of the received EDH packet matches the expected value, and possibly used as an indication of EDH packet loss error. Only valid in SD-SDI mode, fixed output "0" for other modes. 1: No match; 0: Match.
o_rx_edh_parity_err[13]	O	Indicates whether a Parity check error occurred for the received EDH packet; only valid in SD-SDI mode, fixed output "0" for other modes. 1: Error present; 0: No error.
o_rx_edh_checksum_err[13]	O	Indicates whether a Checksum error occurred for the received EDH packet; only valid in SD-SDI mode, fixed output "0" for other modes. 1: Error present; 0: No error.
o_rx_edh_fmt_err[13]	O	Indicates whether the Block Number or Data Count of the received EDH packet matches the expected value; only valid in SD-SDI mode, fixed output "0" for other modes. 1: No match; 0: Match.
Debug Signal		
o_signal_ok	O	HSSTLP_3GSDI P_RX_SIGDET_STATUS transparent transmission signal (asynchronous signal). 1: A high-speed serial input signal is detected by HSSTLP_3G SDI; 0: No high-speed serial input signals are detected by HSSTLP_3G SDI.
o_cdr_ok	O	HSSTLP_3GSDI CDR ALIGN transparent transmission signal (asynchronous signal). 1: The input signal has been locked by HSSTLP_3G SDI; 0: The input signal hasn't been locked by HSSTLP_3G SDI.

13 When instantiating the IP, the port is only visible when Enable EDH Feature is selected and RX MODE is set to SD-SDI or AUTO.

Signal Name	I/O	Description
o_pll_done	O	HSSTLP_3GSDI PLL LOCK indication (free_clk clock domain signal). 1: LOCK complete; 0: During reset or LOCK incomplete.
o_rxstatus[2:0]	O	HSSTLP_3GSDI RXPCS status signal (sdi_rx_clk clock domain signal).
i_pll_wtchdg_clr	I	HSSTLP_3GSDI PLL watchdog clear signal (free_clk clock domain signal). 1: Watchdog signal cleared; 0: Watchdog signal not cleared.

Table 2-12 IPS_SDI IP Client Side Data Interface Bit Definition

SDI Rate Mode	i_txd/o_rxd Bits			
	txd/rxd[9:0]	txd/rxd[19:10]	txd2/rxd2[9:0]	txd2/rxd2[19:10]
	Channel 1	Channel 2	Channel 3	Channel 4
	Framer/De-Framer Module 1		Framer/De-Framer Module 2	
SD-SDI	Unused	Y&C component	Unused	
HD-SDI	C component	Y component	Unused	
3G-SDI Level A	Data stream 2	Data stream 1	Unused	
3G-SDI Level B	Link A	Link A	Link B	Link B
	Data stream 1	Data stream 1	Data stream 2	Data stream 2
	C component	Y component	C component	Y component

2.5.2 3G-SDI IP Interface Timing Description

The 3G-SDI IP interface timing complies with the SMPTE format, and the description is shown in Figure 2-11, Figure 2-12, Figure 2-13 and Figure 2-14.

2.5.2.1 TX Client Side Interface Timing

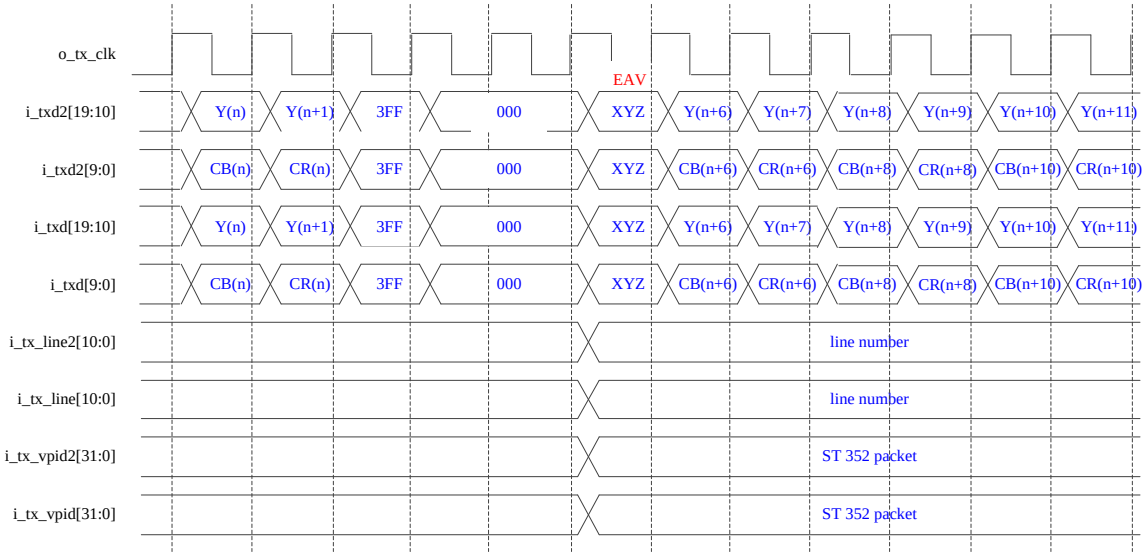

Figure 2-11 3G-SDI IP TX Client Side Interface Timing Diagram

2.5.2.2 RX Client Side Interface Timing

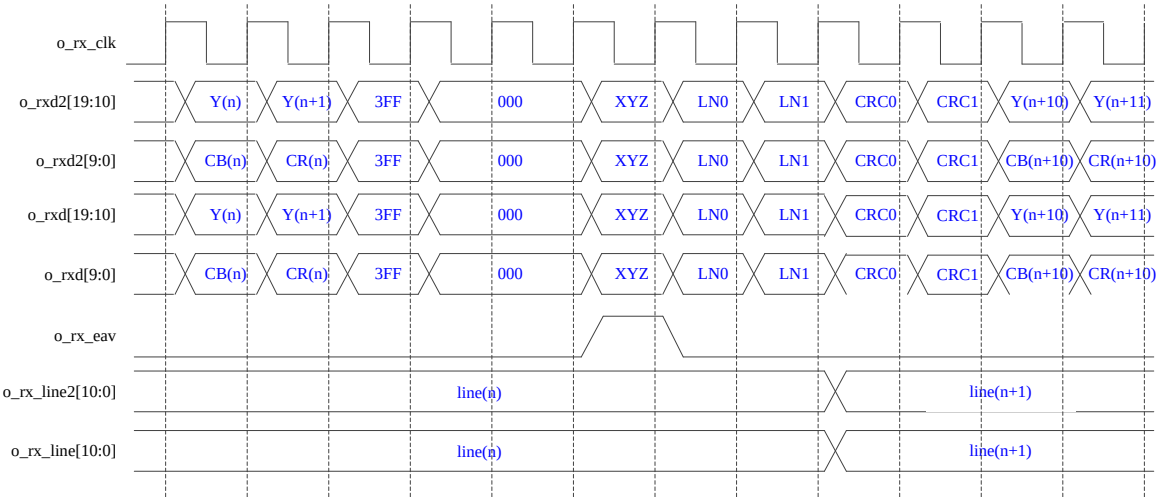

Figure 2-12 3G-SDI IP RX Client Side Interface Timing Diagram

2.5.2.3 TX Clock Enable Signal Timing in SD-SDI Mode

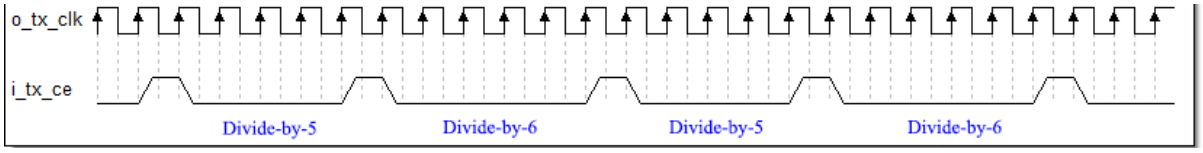

Figure 2-13 TX Clock Enable Signal Timing Diagram in SD-SDI Mode

2.5.2.4 TX Clock Enable Signal Timing in 3G-SDI Level B Mode

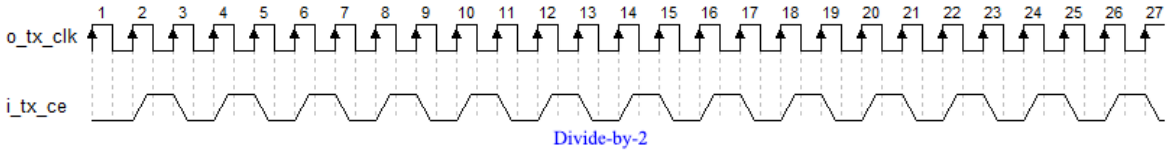

Figure 2-14 TX Clock Enable Signal Timing Diagram in 3G-SDI Level B Mode

2.6 Description of the IP Register

None.

2.7 Typical Applications

2.7.1 Single Link Typical Applications

For the typical single link applications of 3G-SDI IP, please refer to "2.4 Example Design".

2.7.2 Dual Link HD Typical Applications

2.7.2.1 Design Scheme

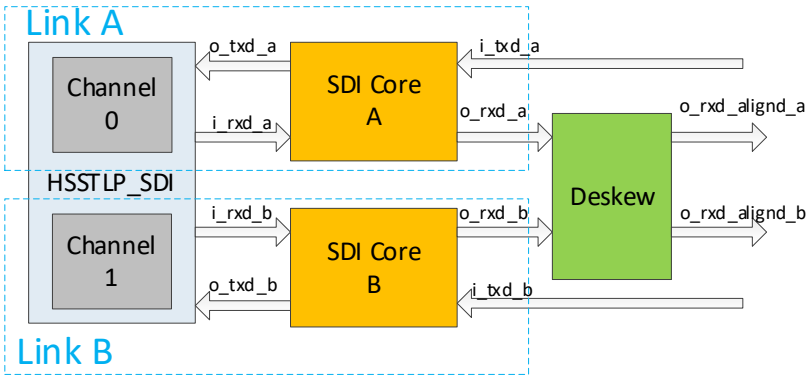

Figure 2-15 Dual Link HD Application Diagram

The applications of 3G-SDI IP in the dual link HD scenarios are depicted in Figure 2-15. Two 3G-SDI IPs form a pair to transmit Link A and Link B respectively, both operating in HD-SDI mode. Two 3G-SDI IPs share the same HSSTLP_3GSDI, with two channels enabled.

On the receiver, the Deskew module is responsible for aligning client-side data. Due to the inconsistent transmission delays between the two Links, it is necessary to align the client-side data sent from the IP.

Attention:

The Deskew module is not part of the 3G-SDI IP.

2.7.2.1.1 Clock Scheme

The clock scheme based on dual link HD applications is shown in Figure 2-16. Despite the availability of two SDI links, a single clock is sufficient for both the TX and RX on the client side.

- Transmit direction: The TCLK2FABRIC0 clock of Link A serves as the working clock for the entire transmitting logic;
- Receive direction: The RCLK2FABRIC0/1 clocks of Link A and Link B serve as the working clocks for their respective receiving logics;
- Within the Deskew module: The RCLK2FABRIC0 clock of Link A also serves as the common clock for the client side to output the received data from the two links.

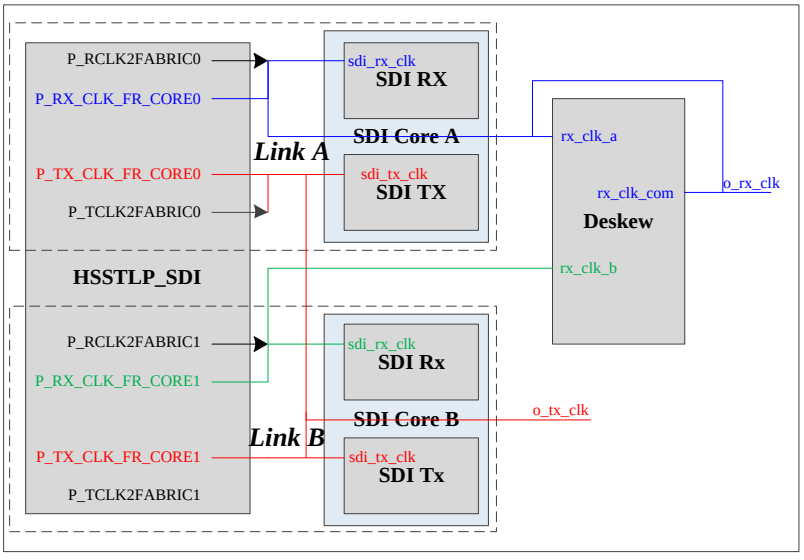

Figure 2-16 Dual Link HD Application Clock Scheme Diagram

2.7.2.1.2 Reset Scheme

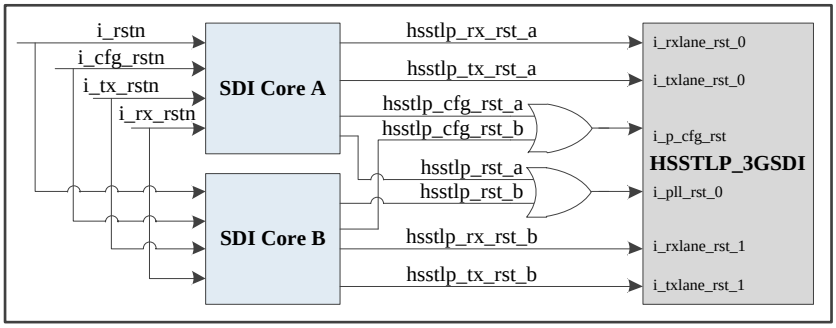

Figure 2-17 Dual Link HD Application Reset Scheme Diagram

The reset scheme based on Dual Link HD applications is shown in Figure 2-17. Since the two links share the same HSSTLP_3GSDI, it requires certain modifications on the reset control of HSSTLP_3GSDI compared to the single Link IP, as is shown in Figure 2-17.

2.7.2.2 Design Considerations

2.7.2.2.1 Single Link to Dual Link Mapping

In the transmit direction, the 3G-SDI IP does not implement single link to dual link mapping internally in Dual Link HD mode. Therefore, client-side users need to complete the logic design of the mapping function by their own according to the SMPTE ST 372 protocol.

2.7.2.2.2 Dual Link HD Data Stream Determination

Since the ST352 packet must be inserted in Dual Link HD mode, when transmitting 1080-line video payloads in this mode, the 3G-SDI IP receiver can determine whether the current data stream is dual link HD by detecting the Byte1 value in the ST352 packet. As per the protocol definition, the byte value is 0x87.

2.7.2.3 Delay Difference Design Guarantee

The reference design based on Dual Link HD applications supports a maximum delay difference of 700ns by default.

According to the SMPTE ST 372 protocol, the delay difference between Link A and Link B at the source end should not exceed 400ns. This reference design also takes into account the link transmission delay and the data recovery delay at the receiver, and compensates the delay difference through the FIFO inside the Deskew to align the outputs of Link A and Link B to the user-side logic.

2.7.2.3.1 Calculation Equation

The maximum delay difference skew that this reference design supports is relevant with the FIFO depth inside the Deskew module. The minimum FIFO depth value can be derived from the supported skew value. The calculation formula is as follows:

$$\text{FIFO Depth} = Round\left(0.5 + \frac{\text{Skew} \times 74.25}{1000}\right) + 6$$

2.7.2.3.2 Calculation Basis

Based on the above calculation formula, the minimum FIFO depth is calculated as 58 when the skew value is set to 700. With the address width set to 6, the actual depth of the FIFO is 64[14], indicating that this reference design can actually support a skew greater than 700ns.

2.7.2.4 On-board Project

When instantiating the IP, with the "Dual Link HD" option selected, the Dual Link HD reference design will be automatically generated for user reference. For the detailed configuration method, please refer to "2.3.1.2 IP Parameter Configuration". The "Dual Link HD" option is only available when both the transmitter and receiver are set as "HD-SDI" mode.

The Dual Link HD reference design uses the PG2L100RD04_A0 single board, and the project design structure is shown in Figure 2-18. In addition to the SDI Core, the Dual Link HD also incorporates stimulus generation and verification, as well as clock, alarm and debug modules. For

14 Generally, to better utilise the RAM resources inside the FPGA, the FIFO depth is set to an integer power of 2.

explanations of some signals in the design, please refer to the comments in the RTL source file.

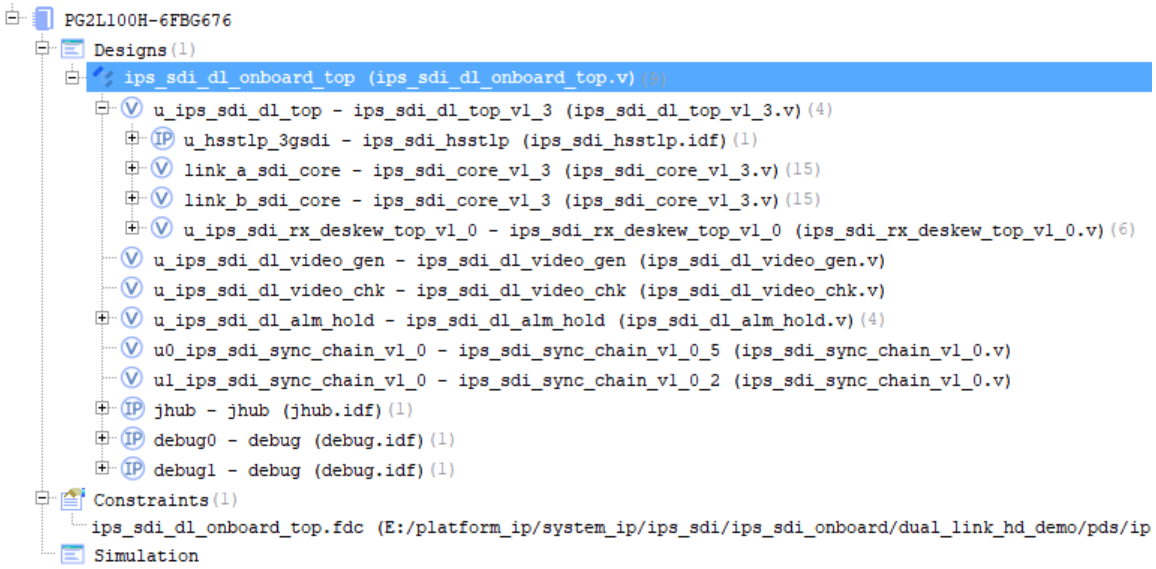

Figure 2-18 Dual Link HD PDS Project Design Structure Diagram

2.7.2.4.1 Stimulus Module

The u_ips_sdi_dl_video_gen module maps 1080P 4:2:2 Y'CB'CR' 10-bit, 60Hz format video frame data to dual links as per the SMPTE372 protocol. Meanwhile, the corresponding 352 packets are inserted into the data frame. The video content is RP 198 checkfield, with the upper part of the active area being purple and the lower part grey. The blank area is black.

2.7.2.4.2 Verification and Alarm Modules

The u_ips_sdi_dl_video_chk module compares the received dual-channel video frame data and frame format with the expected values, and outputs the corresponding error indications. Additionally, it also outputs the Deskew error indications.

The ips_sdi_dl_alm_hold module stores all historical errors, combining all these signals by "OR" and outputting them through the o_err_all pin. The definitions of error indications can be found in Table 2-13. Historical errors are cleared only when a falling edge of the input pin signal i_clr_err is detected.

Table 2-13 Dual Link HD Reference Design Error Indication Bit Definitions

Error Indication Bit	Definition
0	CRC check error occurred at Link A HD-SDI reception frame.
1	352 packets received by Link A HD-SDI do not match the expected values.
2	Progressive/Interlaced value of Link A HD-SDI reception frame does not match the expected values.
3	Frequency of Link A HD-SDI reception frame does not match the expected values.
4	Video format of Link A HD-SDI reception frame does not match the expected values.
5	Link A HD-SDI reception unlocked.
6	Link A HD-SDI reception mode error.
7	Link A HD-SDI frame data error.
8	CRC check error occurred at Link B HD-SDI reception frame.
9	352 packets received by Link B HD-SDI do not match the expected values.
10	Progressive/Interlaced value of Link B HD-SDI reception frame does not match the expected values.
11	Frequency of Link B HD-SDI reception frame does not match the expected values.
12	Video format of Link B HD-SDI reception frame does not match the expected values.
13	Link B HD-SDI reception unlock.
14	Link B HD-SDI reception mode error.
15	Link B HD-SDI frame data error.
16	Both Link A and Link B receptions are correct, but the dual link skew exceeds the supported range. (Note: The default maximum skew value is 58 74.25M clock cycles)

2.7.2.4.3 Testbench Description

The two high-speed serial interface TXs of the DUT are directly looped back to RXs within Testbench. The Testbench also allows modifying the skew of the dual link.

```
ips_sdi_dl_onboard_top u_ips_sdi_dl_onboard_top (
    .i_hsst_refclk_n        (~clk_ref           ),
    .i_hsst_refclk_p        (clk_ref            ),
    .i_clk_27m              (clk_free           ),
    .i_arstn                (i_arstn            ),
    .o_p_tx_sdn_a           (o_p_tx_sdn_a       ),
    .o_p_tx_sdp_a           (o_p_tx_sdp_a       ),
```

```
    .i_p_rx_sdn_a           (o_p_tx_sdn_a       ),
    .i_p_rx_sdp_a           (o_p_tx_sdp_a       ),
    .o_p_tx_sdn_b           (o_p_tx_sdn_b       ),
    .o_p_tx_sdp_b           (o_p_tx_sdp_b       ),
    .i_p_rx_sdn_b           (o_p_tx_sdn_b       ),
    .i_p_rx_sdp_b           (o_p_tx_sdp_b       ),
    .i_clr_err              (i_clr_err          ),
    .o_err_all              (o_err_all          )
)
```

Additionally, the parameter NO_HSSTLP can be set to 1 for simulation acceleration.

```
initial begin
    if (NO_HSSTLP) begin
    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.txlane_done_a = 1'b0;
    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.rxlane_done_a = 1'b0;
    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.txlane_done_b = 1'b0;
    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.rxlane_done_b = 1'b0;
    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.hsstlp_rst = 1'b1;
    #1000
    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.txlane_done_a = 1'b1;
    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.rxlane_done_a = 1'b1;
    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.o_signal_ok_a = 1'b1;
    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.o_cdr_ok_a = 1'b1;
```

```
    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.p_clk2core_tx_a = clk_hd;

    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.p_clk2core_rx_a = clk_hd_dly;

    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.rxd_a = txd_a;

    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.txlane_done_b = 1'b1;

    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.rxlane_done_b = 1'b1;

    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.o_signal_ok_b = 1'b1;

    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.o_cdr_ok_b = 1'b1;

    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.p_clk2core_rx_b = clk_hd;

    force u_ips_sdi_dl_onboard_top.u_ips_sdi_dl_top.rxd_b = txd_b;

end
```

2.7.2.4.4 Simulation Example

The Dual Link HD reference design includes Modelsim simulation examples, and users need to preinstall the Modelsim software by their own. After these preparations are done, double-click ips_sdi_dl_onboard_top_sim.bat to run the simulation.

The ModelSim simulation waveform is shown in Figure 2-19.

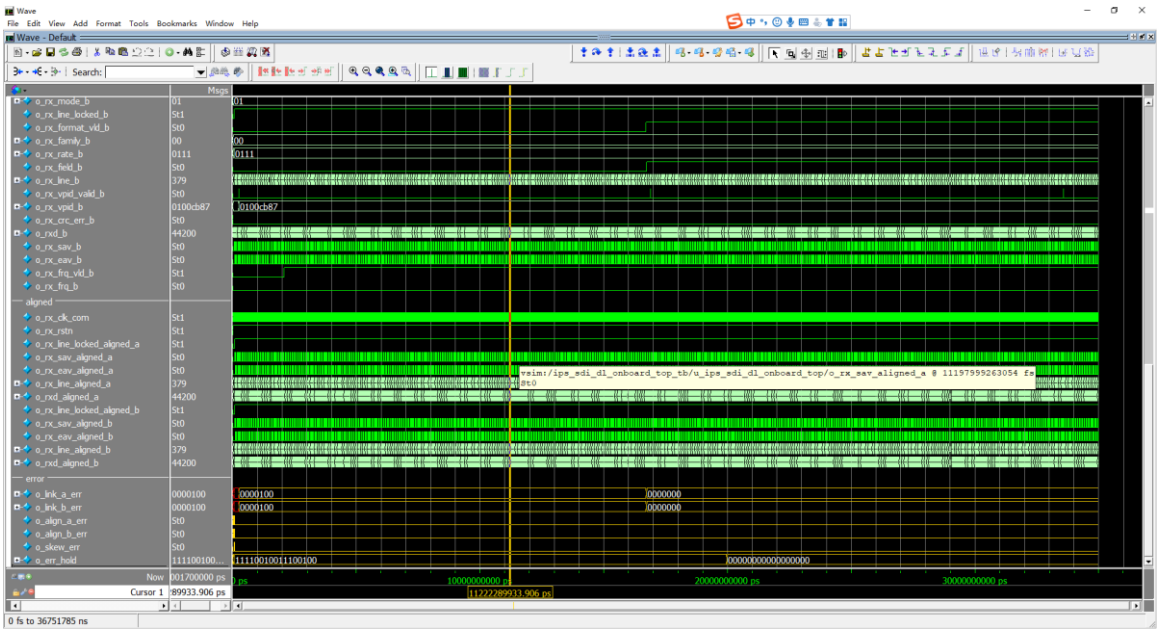

Figure 2-19 Dual Link HD Modelsim Simulation Waveform

2.8 Descriptions and Considerations

2.8.1 Clock Constraints

In the generated Example Design project constraint file ipsxe_sdi_onboard.fdc, the output clock of HSSTHP IP has been constrained to the global clock. Taking the Example Design project as an example:

create_clock -name {i_clk_27m} [get_ports {i_clk_27m}] -period {37} -waveform {0.000 18.500}

create_clock -name {tx_clk} [get_pins {U_IPS_SDI_TOP.U_HSSTLP_3GSDI.U_GTP_HSSTLP_WRAPPER.CHANNEL0_ENABLE.U_GTP_HSSTLP_LANE0/P_TCLK2FABRIC}] -period {6.7} -waveform {0.000 3.350}

create_clock -name {rx_clk} [get_pins {U_IPS_SDI_TOP.U_HSSTLP_3GSDI.U_GTP_HSSTLP_WRAPPER/P_RCLK2FABRIC_0}] -period {6.7} -waveform {0.000 3.350}

2.8.2 Physical Constraints

In application, it requires physical constraints on PLL and LANE of HSSTLP_3GSDI in the .fdc file through PDS based on the actual Single Board. The physical location can be constrained using

PDS software or by editing the physical location in the .fdc file. Taking the Example Design in this document as an example, the method of editing constraints in the .fdc file is as follows.

PLL0 and LANE0 Constraints for HSSTLP_3GSDI

define_attribute
{i:U_IPS_SDI_TOP.U_HSSTLP_3GSDI.U_GTP_HSSTLP_WRAPPER.PLL0_ENABLE.U_GTP_HSSTLP_PLL0} {PAP_LOC} {HSSTLP_364_918:U0_HSSTLP_PLL}

define_attribute
{i:U_IPS_SDI_TOP.U_HSSTLP_3GSDI.U_GTP_HSSTLP_WRAPPER.CHANNEL0_ENABLE.U_GTP_HSSTLP_LANE0} {PAP_LOC} {HSSTLP_364_918:U0_HSSTLP_LANE}

2.8.3 IP Clock Scheme

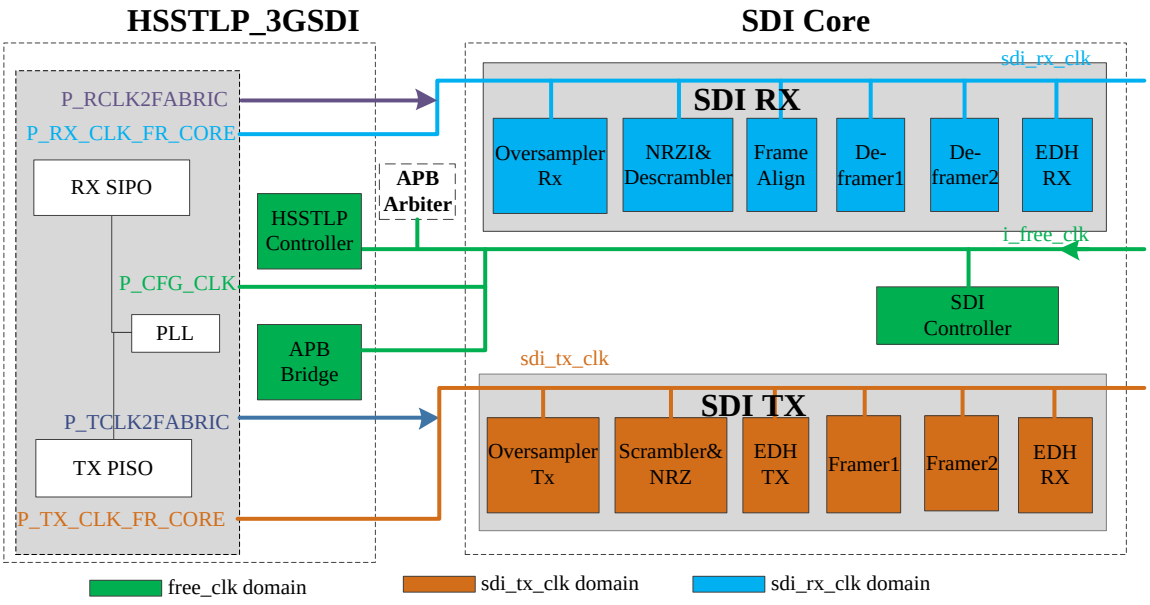

Figure 2-20 Clock Scheme Block Diagram

2.8.3.1 HSSTLP_3GSDI Clock Scheme

The HSSTLP_3GSDI clock scheme is determined by the working mode selected during the instantiation configuration of 3G-SDI IP.

Where:

TX data channel clock:

- From the local reference clock;

RX data channel clock:

- From the CDR recovered clock in HD-SDI and 3G-SDI modes;
- From the local reference clock in SD-SDI mode.

2.8.3.2 SDI Core Clock Scheme

SDI Core is divided into three clock domains, as is shown in Figure 2-20.

2.8.3.2.1 free_clk

This clock is provided by the user and used for APB port, register configuration and other basic control operations of 3G-SDI IP, requiring stability initially. The clock frequency is 27MHz.

2.8.3.2.2 sdi_tx_clk

This clock is output by the P_TCLK2FABRIC of HSSTLP_3GSDI. After routing to the clock tree, it serves as the drive clock for SDI Core TX logic and drives the P_TX_CLK_FR_CORE input pin of HSSTLP_3GSDI. The clock frequency is shown in Table 2-14.

Table 2-14 sdi_tx_clk Frequency in Different Modes

Reference clock frequency	**sdi_tx_clk Frequency (MHz)**		
	HD-SDI	**3G-SDI**[15]	**SD-SDI**[16]
REF_CLK	74.25	148.5	148.5
REF_CLK/1.001	74.25/1.001	148.5/1.001	148.5/1.001

15 sdi_tx_clk should be used in conjunction with the clock enable signal in 3G-SDI Level B mode; the same for sdi_rx_clk.

16 sdi_tx_clk should be used in conjunction with the clock enable signal in SD-SDI mode; the same for sdi_rx_clk.

2.8.3.2.3 sdi_rx_clk

This clock is output by the P_RCLK2FABRIC of HSSTLP_3GSDI. After routing to the clock tree, it serves as the drive clock for SDI Core RX logic and drives the P_RX_CLK_FR_CORE input pin of HSSTLP_3GSDI. The clock frequency is shown in Table 2-15.

Table 2-15 sdi_rx_clk Frequency in Different Modes

Reference clock frequency	**sdi_rx_clk Frequency (MHz)**		
	HD-SDI	**3G-SDI**	**SD-SDI**[17]
REF_CLK	HSSTLP_3GSDI RX differential interface/20		148.5
REF_CLK/1.001			148.5/1.001

2.8.4 IP Reset Scheme

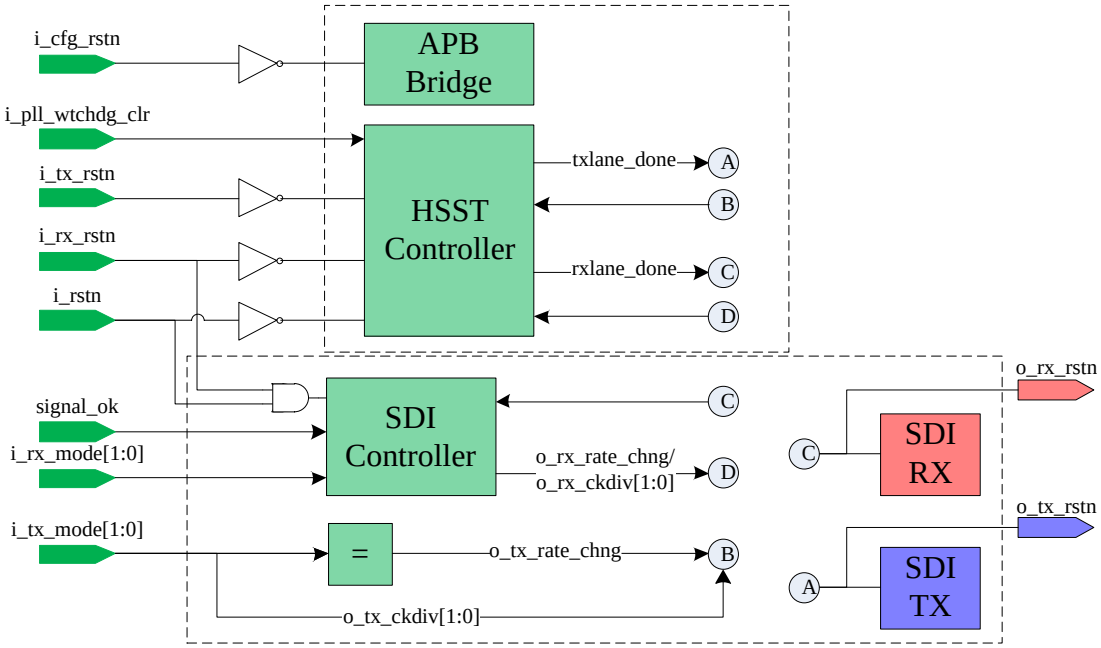

Figure 2-21 SDI Core Reset Scheme Block Diagram

The reset ports include configuration reset (i_cfg_rstn) port and logic reset (i_rstn, i_tx_rstn, and i_rx_rstn) port. The reset domains are described as follows.

17 As data inputs through the HSSTLP_3GSDI high-speed interface require oversampling, the SDI Controller module locks the RX output clock to the reference clock REF_CLK by configuring the registers of HSSTLP_3GSDI.

2.8.4.1 Configuration Reset

i_cfg_rstn controls the reset of the APB Bridge.

2.8.4.2 Logic Reset

2.8.4.2.1 SDI Core Reset

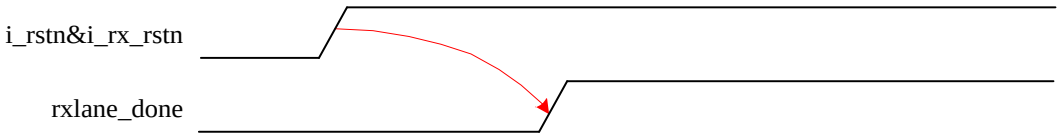

Figure 2-22 SDI Core RX Reset Timing Diagram

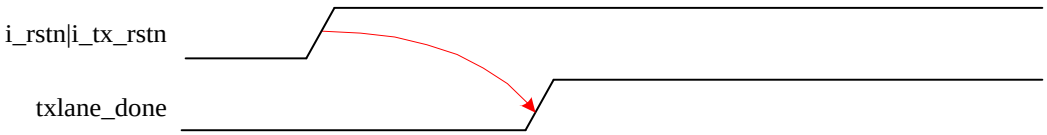

Figure 2-23 SDI Core TX Reset Timing Diagram

- i_rstn and i_rx_rstn control the SDI Controller. When both i_rstn and i_rx_rstn resets are released and signal_ok=1, the SDI Controller starts working[18].
- Upon completion of HSSTLP_3GSDI TX/RX reset, the txlane_done and rxlane_done are output, which can then be inverted to control the reset of the SDI Core TX and SDI Core RX respectively.

2.8.4.2.2 HSSTLP_3GSDI Reset

i_rstn, i_tx_rstn and i_rx_rstn serve as the overall logic reset, TX logic reset and RX logic reset respectively, allowing the HSSTLP Controller to reset the HSSTLP_3GSDI based on a valid reset sequence.

18 Due to the lack of specific details on the HSST RX error state during the automatic detection of HD-SDI and 3G-SDI modes, a simple free detection mechanism is employed.

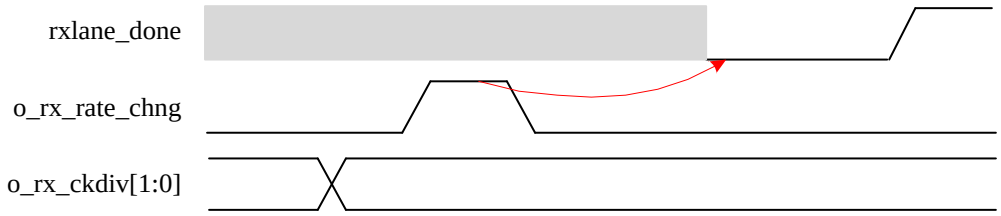

Figure 2-24 SDI Core RX Rate Switching Timing Diagram

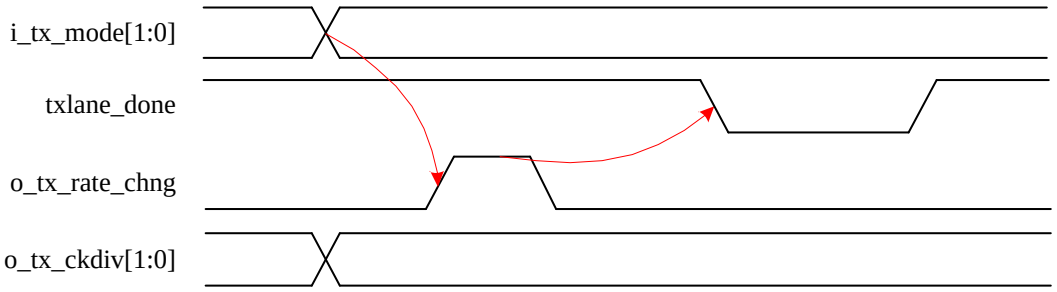

Figure 2-25 SDI Core TX Rate Switching Timing Diagram

- After the SDI Controller outputs o_rx_rate_chng/o_rx_ckdiv[1:0], the HSSTLP_3GSDI Controller performs rate switching operation on HSSTLP_3GSDI based on a valid rate switching sequence; after the rate switching is finished, rxlane_done is output to inform the SDI Controller of the completion of the operation.
- When txlane_done=1, the rate can be switched by dynamically changing the value of i_tx_mode. The SDI Core outputs tx_rate_chg_bus to trigger the rate switching operation for HSSTLP_3GSDI by the HSSTLP_3GSDI Controller, following a valid rate switching sequence; after the HSSTLP_3GSDI TX rate switching is finished, txlane_done is output to inform the SDI Controller of the completion of the operation.

2.8.5 SD Smoother Module

When the IP operates in SD-SDI mode, the serial data rate is low as 270Mbps. For direct reception of serial data by HSSTLP in FPGA, a 270Mbps rate is below the working range of the HSSTLP. Therefore, when receiving SD-SDI data with HSSTLP_3GSDI, the HSSTLP_3GSDI locks onto its reference clock. The clock frequency of p_clk2core_rx output by HSSTLP_3GSDI is tied to its reference clock frequency, with a standard value of 148.5 MHz. The serial data received by HSSTLP_3GSDI is 11x oversampled data, so at the receiver, the Oversampler RX module recovers

the 10-bit valid data from the 20-bit oversampled data rxd output by HSSTLP_3GSDI, and simultaneously outputs a data valid indication as the clock enable signal for SD-SDI data.

The frequency point of this clock enable signal is 27 MHz, which seems like an impulse signal alternately dividing the 148.5M clock by 6 and 5. However, due to oversampling operation, this clock enable signal is not a smooth signal. Therefore, a new clock enable signal needs to be regenerated to filter and attenuate the jitter and noise. Then, data operations across clock enable domains can be executed through a FIFO.

The 3G-SDI IP offers a reference module named SD Smoother, which functions to smooth the clock enable signal. Users can instantiate this module in their applications based on actual needs. Refer to Table 2-16 for interface connection.

The SD Smoother module comprises of 2 parts: the Clock Recovery Unit (CRU) and a synchronous FIFO with a depth of 64 and a width of 13. The CRU module is a second-order digital Phase Locked Loop. Within the CRU module, the jitter and noise of the clock enable signal output by the 3G-SDI IP are filtered and attenuated, which generates a new 27M clock signal output. The rising edge of the 27M clock signal will be output as the new clock enable signal sd_rx_ce.

Due to the synchronous FIFO in the SD_Smoother module, an uncertain delay will occur during the transfer of SD-SDI data stream through the FIFO. Therefore, the o_rx_sav, o_rx_eav, and o_rx_line_locked signals output by the 3G-SDI IP, along with o_rxd[19:10], should be written into the FIFO under the control of o_rx_ce, and then read out from the FIFO under the control of sd_rx_ce.

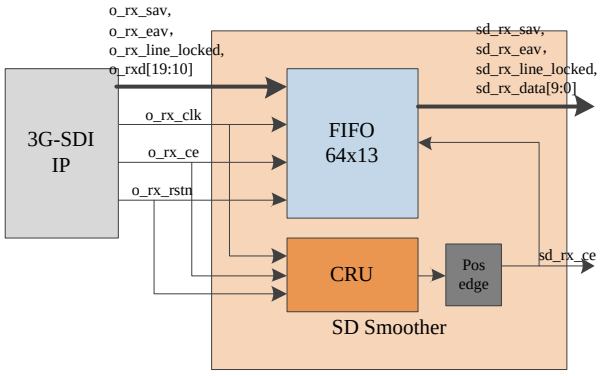

Figure 2-26 SD Smoother Module Functional Block Diagram

The interface description of the SD Smoother module is shown in Table 2-16.

Table 2-16SD Smoother Module Interface List

Signal Name	I/O	Description
3G-SDI IP-related Interfaces		
i_rx_clk	I	Input sampling clock (frequency 148.5 MHz, connected to o_rx_clk of 3G-SDI IP)
i_rx_rstn	I	Input reset signal (active low, connected to o_rx_rstn of 3G-SDI IP)
i_rx_ce	I	Input SD-SDI clock enable signal (connected to o_rx_ce of 3G-SDI IP)
i_rxd[12:0]	I	Input 13-bit data signal (connected to o_rxd[19:10], o_rx_line_locked, o_rx_eav and o_rx_sav of 3G-SDI IP)
o_rx_ce	O	Output smoothed SD-SDI clock enable signal
o_rxd[12:0]	O	Output smoothed 13-bit data signal (including sd_rx_data[9:0], sd_rx_line_locked, sd_rx_eav and sd_rx_sav)
Configuration and Debug Interface		
i_free_run	I	Enable NCO free oscillation within CRU (for debugging) 1: Enable NCO free oscillation within CRU 0: Normal Operation
i_coe_p[15:0]	I	Loop filter coefficient P within CRU (reference value: 16'd94)
i_coe_i[15:0]	I	Loop filter coefficient I within CRU (reference value: 16'd17).
i_noise_en	I	Noise insertion enable within CRU (for increasing SFDR and reducing SNR) 1: Enable noise insertion within CRU 0: Normal Operation
i_noise_pos[29:0]	I	Positive noise value inserted within CRU (valid only when i_noise_en=1, signed number, represented by binary complement)
i_noise_neg[29:0]	I	Negative noise value inserted within CRU (valid only when i_noise_en=1, signed number, represented by binary complement)
i_clr_stat	I	Performance statistics clear signal within module (for debugging) 1: Clear performance statistics within module 0: Normal function for performance statistics within module
o_fifo_full	O	"1" indicates FIFO full (for debugging)
o_fifo_empty	O	"1" indicates FIFO empty (for debugging)
o_locked	O	"1" indicates CRU locked
o_ph_err[12:0]	O	Output phase detection error (signed number, represented by binary complement, for debugging)
o_fcw[29:0]	O	Output frequency control word after loop filtering (for debugging)
o_max_diff[5:0]	O	Output historical maximum value of FIFO address difference (for debugging)
o_min_diff[5:0]	O	Output historical minimum value of FIFO address difference (for debugging)

2.9 IP Debugging Method

The 3G-SDI IP link status can be monitored through DebugCore. Refer to Table 2-10 for the DebugCore signal list.

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