FIR IP

User Guide

(UG052012, V1.5)

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Revisions History

Document Revisions

Version	Date of Release	Revisions	Applicable IP and Corresponding Versions
V1.5	24.04.2024	Initial release.	V1.5

IP Revisions

IP Version	Date of Release	Revisions
V1.5	24.04.2024	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
FIR	Finite Impulse Response
IPC	IP Compiler
PDS	Pango Design Suite

Related Documentation

The following documentation is related to this manual:

1. ***Pango_Design_Suite_Quick_Start_Tutorial***
2. ***Pango_Design_Suite_User_Guide***
3. ***IP_Compiler_User_Guide***
4. ***Simulation_User_Guide***
5. ***User_Constraint_Editor_User_Guide***
6. ***Physical_Constraint_Editor_User_Guide***
7. ***Route_Constraint_Editor_User_Guide***

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Chapter 1 Preface

This chapter describes the scope, structure, and writing standards of this manual to help users quickly find the information they need.

1.1 Introduction of the Manual

This manual serves as a user guide for the FIR (Finite Impulse Response) IP launched by Pango Microsystems, primarily including the IP user guide and related appendices. This manual helps users quickly understand the features and usage of FIR IP.

1.2 Writing Standards of the Manual

Table 1-1 Description of Writing Standards

Text	**Rules**
Attention	If users ignore the attention contents, they may suffer adverse consequences or fail to operate successfully due to incorrect actions.
Description	Instructions and tips provided for users.
Recommendation	Recommended settings and instructions for users.

Chapter 2 IP User Guide

This chapter provides a guide on the use of FIR IP, including an introduction to IP, IP block diagram, IP generation process, Example Design, IP interface description, IP register description, typical applications, instructions and considerations, and IP debugging methods. More details on the design process can be found in the following PDS help documentation.

- "***Pango_Design_Suite_Quick_Start_Tutorial***"
- "***Pango_Design_Suite_User_Guide***"
- "***IP_Compiler_User_Guide***"
- "***Simulation_User_Guide***"

2.1 IP Introduction

FIR IP is launched by Pango Microsystems to implement FIR filter computation. Users can configure and generate the IP module using the IPC (IP Compiler) tool within the PDS (Pango Design Suite).

2.1.1 Key Features[1]

- Single channel, with the sampling cycle and clock cycle being identical.
- Configurable filter types: Single Rate, Half Band, Decimator, and Interpolator.
- Configurable number of coefficients: 4-2048.
- Configurable input data width: signed, with the range of 2 Bit 49 Bit.
- Configurable filter coefficient bit width: signed, with the range of 2 Bit-35 Bit.
- Configurable rate conversion factor for polyphase decimator filters: integer, with the range of 2-1024.
- Configurable rate conversion factor for polyphase interpolator filters: integer, with the range of 2-1024.

1 The actual configuration range depends on the device resources and configuration parameter combinations.

- Configurable filter coefficient file source: direct input via UI, or selected file path via UI.
- Configurable filter coefficient structures: Asymmetric, Even Symmetric, Odd Symmetric, and Half Band.
- Configurable input data fractional bit width[2].
- Configurable output data width[3].
- Automatically calculates output data fractional bit width[4].
- Configurable output rounding modes: Full Precision and Truncate LSBs.
- Supports dynamic reloading of filter coefficients.
- Provides a bit-accurate C code model.

2.1.2 Applicable Devices and Packages

Table 2-1 Applicable Devices and Packages for FIR IP

Applicable Devices	**Supported Packages**
Logos2 Family	ALL
Titan2 Family	ALL
Kosmo2 Family	ALL

2 The minimum fractional data width for input data is 0 Bit, and the maximum is the input data width.

3 The output data width can only be configured when the output rounding mode is set to Truncate LSBs.

4 The output data fractional bit width matches the input data fractional bit width.

2.2 IP Block Diagram

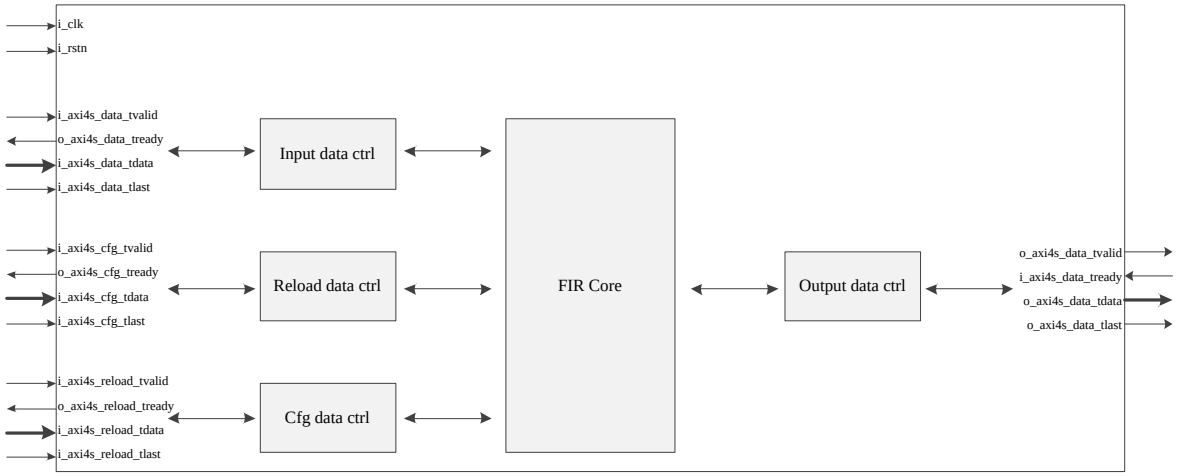

Figure 2-1 FIR IP System Block Diagram

The FIR IP system block diagram is shown in Figure 2-1, consisting of four data control modules and the FIR Core.

2.2.1 Data Interface Control Modules

Input data ctrl, Cfg data ctrl, Reload data ctrl, and Output data ctrl implement data interactions between the IP and external interfaces, including: input data interface, output data interface, reload data interface, configuration data interface. For interface descriptions, and Figure 2-11 for interface timing, please refer to Table 2-6 to Table 2-9.

2.2.2 FIR Core

It implements filter computations according to the FIR IP configurations, including single rate filters, half-band filters, polyphase decimator filters, and polyphase interpolator filters. Among them, single rate and polyphase decimator filters have three coefficient structures: asymmetric, even symmetric, and odd symmetric; polyphase interpolator filters only have asymmetric coefficient structures; half-band filters have asymmetric and half-band coefficient structures.

2.3 IP Generation Process

2.3.1 Module Instantiation

Users can customise the configuration of FIR IP through the IPC tool to instantiate the required IP modules. For detailed instructions on using the IPC tool, please refer to ***"IP_Compiler_User_Guide"***.

The main steps for instantiating the FIR IP module are described as follows.

2.3.1.1 Selecting IP

Open IPC and click File > Update in the main window to open the Update IP dialog box, where you add the corresponding version of the IP model.

After selecting the device type, the Catalog interface displays the loaded IP models. Select the corresponding version of FIR under the "System" directory. The IP selection path is shown in Figure 2-2. Then set the Pathname and Instance Name on the right side of the page. The project instantiation interface is shown in Figure 2-3.

Attention:

PG2L25H, PG2L50H, PG2L100H, PG2L200H, PG2T390H: The software version must be 2022.2-SP1 or above.

PG2L100HX, PG2T390HX: The software version must be 2023.1 or above.

PG2K400: For software versions, please contact FAE.

For devices uncovered above, please consult the FAE for software version requirements.

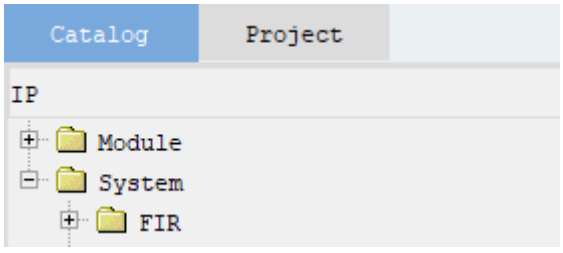

Figure 2-2 FIR IP Selection Path

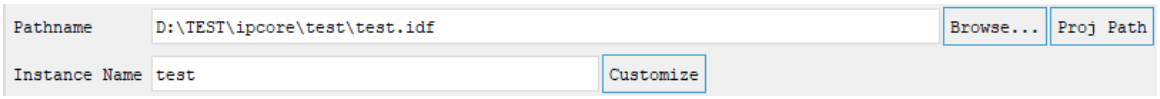

Figure 2-3 Project Instantiation Interface

2.3.1.2 IP Parameter Configuration

After selecting the IP, click <Customize> to enter the FIR IP parameter configuration interface. The left Symbol is the interface block diagram, as shown in Figure 2-4 and Figure 2-5; the Parameter Configuration window is shown on the right side, as shown in Figure 2-6. For configuration parameter descriptions, please refer to Table 2-2.

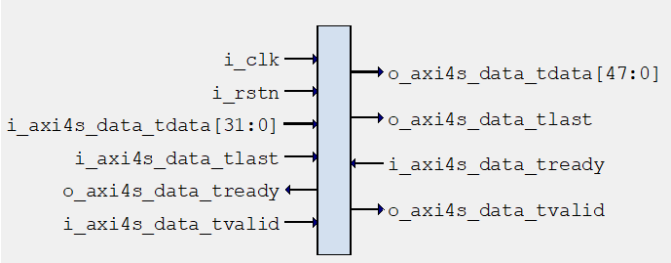

Figure 2-4 FIR IP Interface Block Diagram (Dynamic reload filter coefficients not enabled)

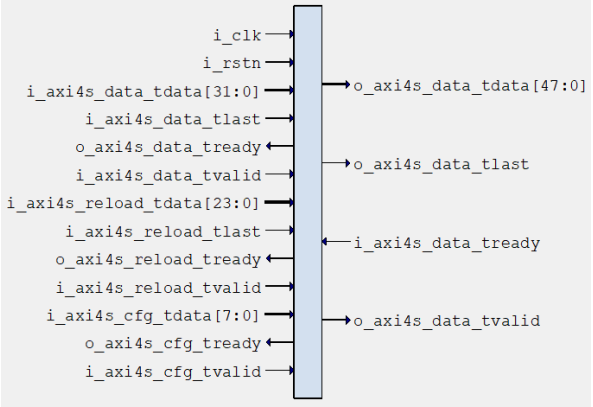

Figure 2-5 FIR IP Interface Block Diagram (Dynamic reload filter coefficients enabled)

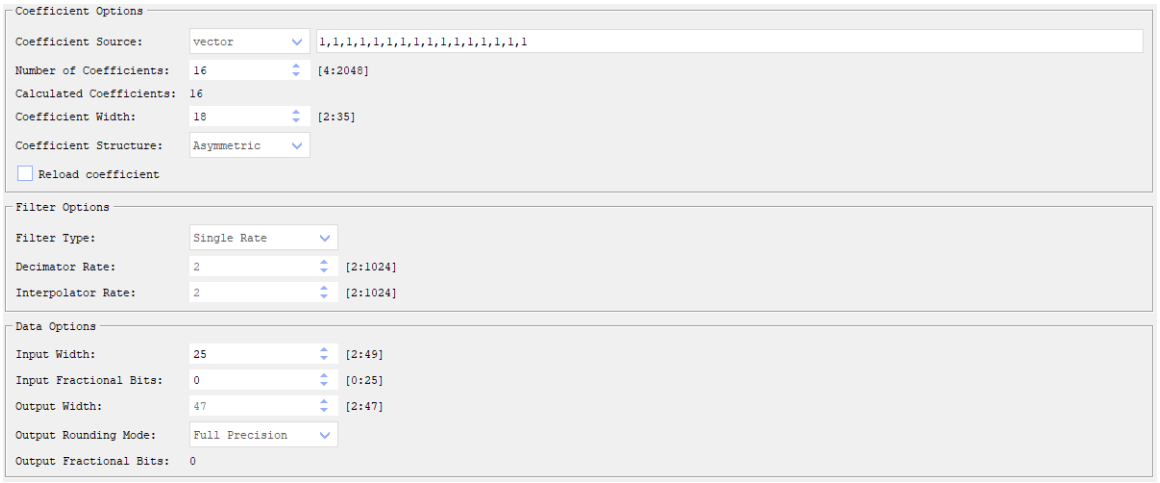

Figure 2-6 FIR IP Parameter Configuration Interface

Table 2-2 Configuration Parameter Description

Option Domain	**Parameter/Configuration Options**	**Parameter Description**	**Default Value**
Coefficient Options	Coefficient Source	Filter coefficient source selection: vector: Directly input filter coefficients in the interface coef file: Select the filter coefficient file in the interface to import coefficients	vector
	Number of Coefficients	Configure the number of filter coefficients: 4-2048	16
	Calculated Coefficients	Number of actual filter coefficients calculated based on the configuration	N/A
	Coefficient Width	Filter coefficient data width: 2-35	18
	Coefficient Structure	Filter coefficient structure: Asymmetric Even Symmetric Odd Symmetric Half Band	Asymmetric
	Reload coefficient	Configure whether to enable dynamic reload filter coefficient: Selected: Enabled Cleared: Disabled	Cleared
Filter Options	Filter Type	Configure filter structure: Single Rate Half Band Decimator Interpolator	Single Rate
	Decimator Rate	Configure the rate conversion factor in Decimator mode: 2-1024	2
	Interpolator Rate	Configure the rate conversion factor in Interpolator mode: 2-1024	2

Option Domain	Parameter/Configuration Options	Parameter Description	Default Value
Data Options	Input Width	Configure input data width: 2-49	25
	Input Fractional Bits	Configure input data fractional data width: 2-input data width	0
	Output Width	Configure output data width: 2-47	47
	Output Rounding Mode	Configure output data rounding method: Full Precision (no rounding) Truncate LSBs (truncate least significant bits)	Full Precision
	Output Fractional Bits	Display output data fractional bit width	N/A

Note: "N/A" indicates that the parameter is not configurable.

Attention:

When Coefficient Source is configured as "coef file", the selected file must exist and the file content format must match the coef_data_dat file in Table 2-3, and the coefficients in the file must be decimal integers;

When Coefficient Source is configured as "vector", the input values must be decimal integers;

The number of coefficients configured by Number of Coefficients must match the number of coefficients configured by Coefficient Source.

2.3.1.3 Generating IP

Upon completion of parameter configuration, click the <Generate> button in the top left corner to generate the FIR IP code according to the user-specific settings. The information report interface for IP generation is shown in Figure 2-7.

Figure 2-7 FIR IP Generation Report Interface

Upon successful IP generation, the files indicated in Figure 2-3 will be output to the Project path specified in the table below.

Table 2-3 Output Files after FIR IP Generation

Output File[5]	**Description**
$instname.v	The top-level .v file of the generated IP.
$instname.idf	The Configuration file of the generated IP.
/rtl/*	The RTL code file of the generated IP.
/example_design/*	The Test Bench, top-level files, and some module files used in the Example Design of the generated IP.
/pnr/*	The project files and pin constraint files for the Example Design of the generated IP.
/sim/*	The simulation directory for the generated IP.
/sim_lib/*	The directory of the encryption files for the IP.
/rev_1	The default output path for synthesis reports. (This folder is generated only after specifying the synthesis tool)
readme.txt	The readme file describes the structure of the generation directory after the IP is generated.
coef_data.dat	Reference file for importing coefficients by selecting file.

2.3.2 Constraint Configuration

For the specific configuration method of constraint files, please refer to the relevant help documents in the PDS installation path: "***User_Constraint_Editor_User_Guide***", "***Physical_Constraint_Editor_User_Guide***", "***Route_Constraint_Editor_User_Guide***".

2.3.3 Simulation Runs

The simulation of FIR IP is based on the Test Bench of the Example Design. For detailed information about Example Design, please refer to "2.4 Example Design".

For more details about the PDS simulation functions and third-party simulation tools, please consult the related help documents in the PDS installation path: "***Pango_Design_Suite_User Guide***", "***Simulation_User_Guide***".

In the Windows system, after IP generation, double-click the *.bat file under the "<project_path>/sim/modelsim" directory to run the simulation using ModelSim10.1a. After the simulation ends, specific simulation results will be saved in the vsim.log file, and the ModelSim

5 <$instname> is the instantiation name entered by the user; "*" is a wildcard character used to replace files of the same type.

simulation waveform is shown in Figure 2-8.

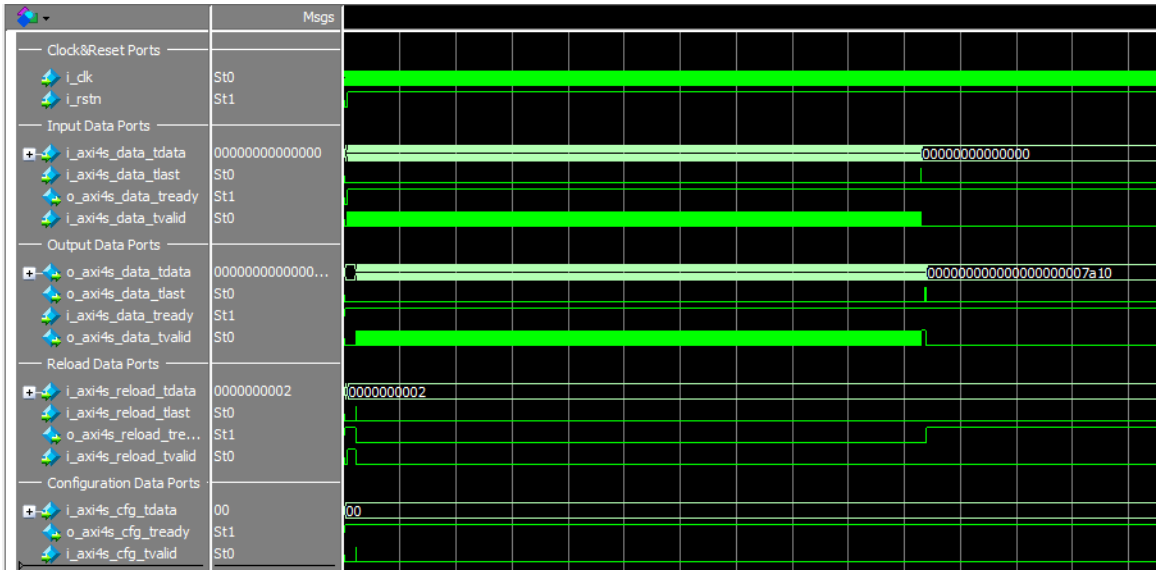

Figure 2-8 ModelSim Simulation Waveform

2.3.4 Synthesis and Placement/Routing

The specific usage of PDS synthesis tools and placement/routing tools can be found in the help documents within the PDS installation path.

Attention:

Example Design project files .pds and pin constraint files .fdc generated with the IP are located in the "/pnr/example_design" directory, and physical constraints need to be modified according to the actual devices and PCB trace routing. For details, please refer to "2.8 Descriptions and Considerations".

2.3.5 Resources Utilization

Resource utilization depends on the device and IP configuration. Resource utilization data for different devices with the same configuration may vary. Typical resource values for Titan2/Logos2/Kosmo2 family devices are shown in Table 2-4.

Table 2-4 Typical Resource Utilization Values for FIR IP Based on Applicable Devices

Device	Configuration Mode[6]		Typical Resource Utilization Values				
	FILTER_TYPE	COEF_SUM	LUT	FF	APM	Distributed RAM	USCM
PG2T390H/ PG2T390HX	Single Rate	32	295	371	131	144	1
	Half Band	31	277	331	71	144	1
	Decimator[7]	32	314	620	51	144	1
	Interpolator[8]	32	692	810	141	432	1
PG2L100H/ PG2L100HX	Single Rate	32	296	371	131	144	1
	Half Band	31	277	331	71	144	1
	Decimator[7]	32	313	620	51	144	1
	Interpolator[8]	32	687	810	141	432	1
PG2L25H	Single Rate	16	278	328	67	144	1
	Half Band	31	276	331	71	144	1
PG2L50H	Single Rate	16	276	328	67	144	1
	Half Band	31	277	331	71	144	1
PG2L200H	Single Rate	32	294	371	131	144	1
	Half Band	31	277	331	71	144	1
PG2K400	Single Rate	32	285	364	131	144	1
	Half Band	31	264	324	71	144	1
	Decimator[7]	32	301	613	51	144	1
	Interpolator[8]	32	681	803	141	432	1

Note:

For devices not listed in the above table, please refer to the typical resource utilization values in the table of the devices with similar configurations. Whether this configuration is supported depends on the overall resources of the device.

6 In configuration mode, INPUT_WIDTH is 49 bits, COEF_WIDTH is 35 bits, OUTPUT_ROUNDING_MODE is Full Precision, and RELOAD_COEF is 1.

7 In Decimator mode, the DECIMATOR_RATE is 3.

8 In Interpolator mode, the INTERPOLATOR_RATE is 3.

2.4 Example Design

This section mainly introduces the Example Design scheme based on FIR IP. The scheme generates several sets of input data, which undergo FIR IP calculation and verification before outputting error messages.

2.4.1 Design Block Diagram

The system block diagram of Example Design is shown in Figure 2-1, including three modules: Frame_Gen, FIR IP, and Frame_Chk. This scheme uses the P05V330RD05_A0_PCB single board for testing, and the pin constraints in Table 2-5 are for reference only.

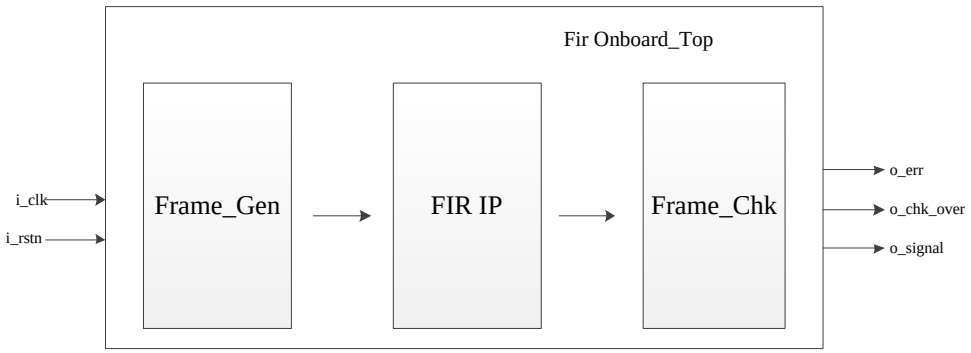

Figure 2-9 FIR IP Example Design Structural Diagram

2.4.2 Descriptions of Ports

Table 2-5 Example Design Interface List

Port	I/O	Bit width	Description	Pin constraints
i_clk	I	1	External input clock, with a maximum frequency of 150MHz	AB27
i_rstn	I	1	External input reset (active low)	AB30
o_chk_err	O	1	Test result indicator: 0: Test result correct 1: Test result incorrect	Y25
o_chk_over	O	1	Test completion indicator: 0: Test incomplete 1: Test completed	Y26
o_signal	O	1	Example Design does not check data. This signal prevents FIR IP internal logic from being optimised, and it has no practical significance.	AA26

2.4.3 Module Description

2.4.3.1 Frame_Gen

The test stimulus generation module, which starts generating a fixed amount of FIR IP input data after power-up reset.

2.4.3.2 FIR IP

Instantiated FIR IP.

2.4.3.3 Frame_Chk

The test data check module, which only checks whether the output data quantity of the FIR IP is correct, and outputs error indicator and test completion signal.

2.4.4 Test Method

After the bitstream of Example Design is loaded, test begins. When the o_chk_over signal is pulled high, it indicates the test is complete. At this moment, if the o_chk_err signal is pulled down, it indicates the test is correct, otherwise, the test has errors.

2.4.5 Instance Configuration

Example Design supports all IP configurations.

2.4.6 Instance Simulation

Under the Windows operating system, after the IP is generated, simulation can be run by double-clicking the "*.bat file" in the "<project_path>/sim/modelsim" directory[9].

9 For file path, please refer to Table 2-3.

2.5 Descriptions of IP Interfaces

This section provides descriptions of interfaces related to FIR IP and timings.

2.5.1 Descriptions of Ports

2.5.1.1 Clock and Reset Interface

Table 2-6 List of Clock and Reset Interface Signals

Port	I/O	Bit width	Description
i_clk	I	1	Clock signal of IP
i_rstn	I	1	Reset signal of IP, active low

2.5.1.2 Input Data Interface

Table 2-7 List of Input data Interface Signals

Port	I/O	Bit width	Description
i_axi4s_data_tvalid	I	1	valid signal, indicating that external input data is valid
o_axi4s_data_tready	O	1	ready signal, indicating that the IP can receive data
i_axi4s_data_tdata	I	2bit~49bit	External input data
i_axi4s_data_tlast	I	1	The tlast signal of AXI4 bus input data

2.5.1.3 Output Data Interface

Table 2-8 List of Output data Interface Signals

Port	I/O	Bit width	Description
o_axi4s_data_tvalid	O	1	valid signal, indicating that the IP output data is valid
i_axi4s_data_tready	I	1	ready signal, indicating that the external can receive data
o_axi4s_data_tdata	O	-[10]	Output data of IP
o_axi4s_data_tlast[11]	O	1	tlast signal, the signal delayed by the data processing time of the tlast signal from the input data

10 The output data width range dynamically changes according to the configuration of the FIR IP.

11 When the filter structure is a Decimator, o_axi4s_data_tlast is only significant during reloading coefficients.

2.5.1.4 reload Data Interface

Table 2-9 List of Reload Data Interface Signals

Port	I/O	Bit width	Description
i_axi4s_reload_tvalid	I	1	valid signal, indicating that external reload data is valid
o_axi4s_reload_tready	O	1	ready signal, indicating that the IP can receive reload data
i_axi4s_reload_tdata	I	2bit~35bit	External reload coefficient data
i_axi4s_reload_tlast	I	1	Indicates the last data of a frame of reload coefficient

2.5.1.5 Configuration Data Interface

Table 2-10 List of Configuration Data Interface Signals

Port	I/O	Bit width	Description
i_axi4s_cfg_tvalid	I	1	valid signal, indicating that external configuration input data is valid
o_axi4s_cfg_tready	O	1	ready signal, indicating that the IP can receive configuration input data
i_axi4s_cfg_tdata	I	8bit	Configuration input data, set to 0 during use

2.5.2 Interface Data Format

The data format of the FIR IP data interface[12] is consistent and needs to be extended to the byte boundary, as shown in Figure 2-10.

- For data input interface and data output interface: The data pad is the sign bit;
- For reload input interface and configuration input interface: The data pad is 0.

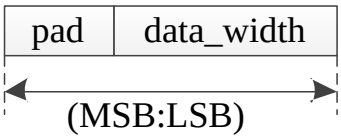

Figure 2-10 Data Format

12 They are the input data interface, output data interface, reload data interface, and configuration data interface, respectively. For interface descriptions, please refer to Table 2-6 to Table 2-9.

2.5.3 Descriptions of Interface Timings

2.5.3.1 Data Interface

The timing standards of the FIR IP data interface are consistent, as shown in Figure 2-11.

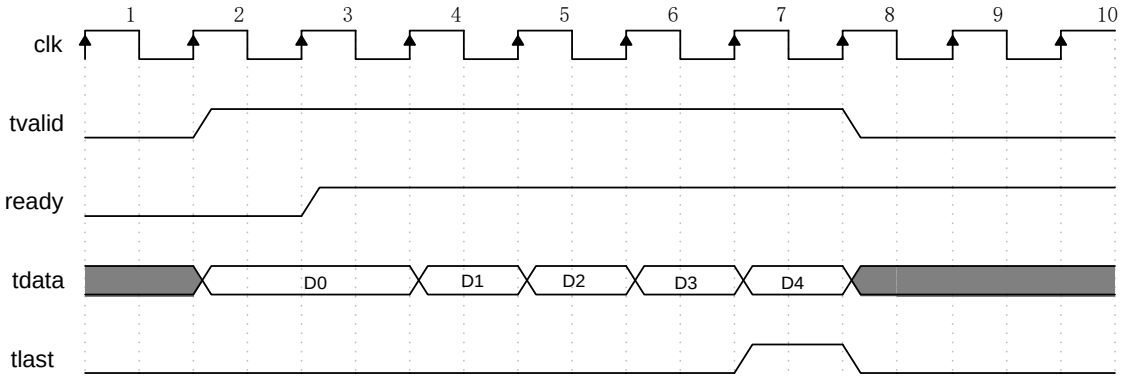

Figure 2-11 Interface Timing Diagram

2.5.3.2 Reload Filter Coefficients

The reload data interface and configuration data interface are used for reloading filter coefficients, with the timing as shown in Figure 2-12. After the reloaded data is received, you need to wait for the next configuration data to be received and then wait for an o_axi4s_data_tlast and then applying the reloaded coefficients in the data processing.

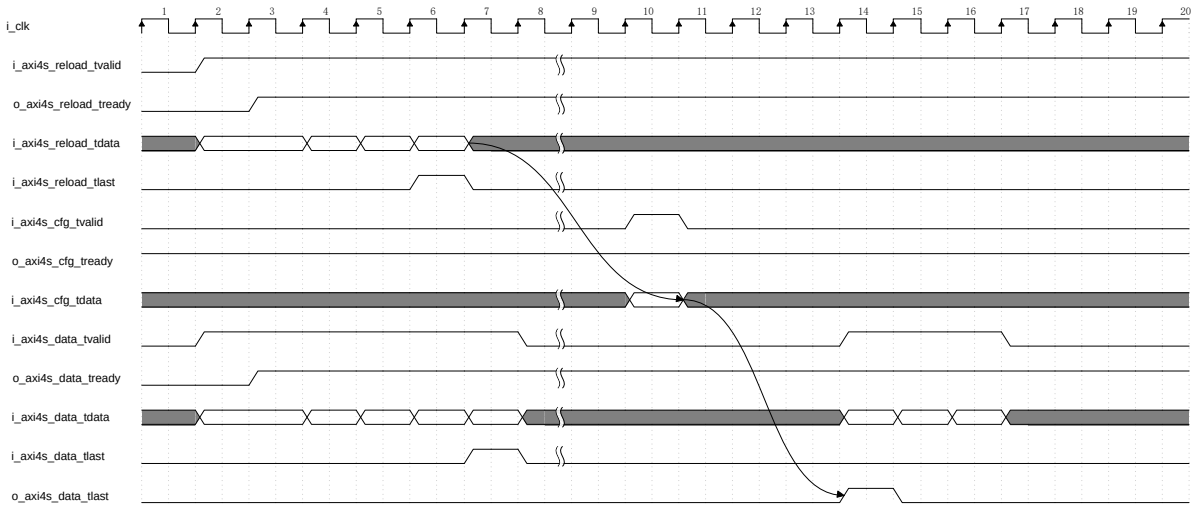

Figure 2-12 Timing of Reloading Filter Coefficients

2.6 Description of the IP Register

None.

2.7 Typical Applications

For typical applications of the FIR IP, please refer to "2.4 Example Design".

2.8 Descriptions and Considerations

2.8.1 Polyphase Filter Coefficient Padding

When applying a polyphase filter structure, it may be necessary to pad the coefficients with zero values to meet the implementation structure requirements. Coefficient padding will affect the data phase but not the data value. The number of coefficients after calculation will be displayed in the Calculated Coefficients interface, as shown in Table 2-2.

When the reload coefficient is enabled, the padded coefficients also need to be reloaded, i.e. the number of coefficients to be reloaded is the quantity displayed in Calculated Coefficients.

2.8.2 Coefficients Description

FIR IP supports four types of filter structures and four types of coefficient structures. The relationship between coefficient structures and filter structures is shown in Table 2-11. The diagram of coefficient structures is shown from Figure 2-13 to Figure 2-16.

Table 2-11 Optional Coefficient Structures

Filter Structure	**Coefficient Structure**
Half Band	Asymmetric, Half Band
Single Rate	Asymmetric, Even Symmetric, Odd Symmetric
Decimator	
Interpolator	Asymmetric

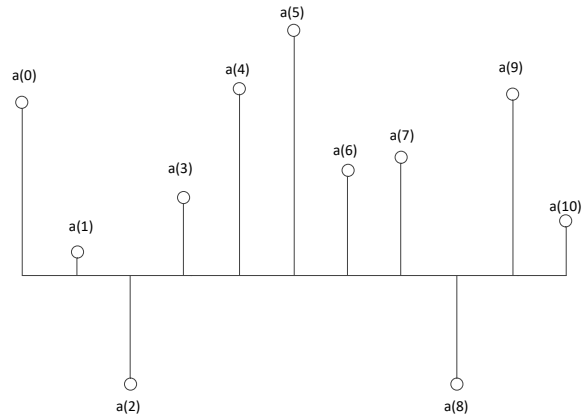

Figure 2-13 Asymmetric Coefficient Structure Diagram

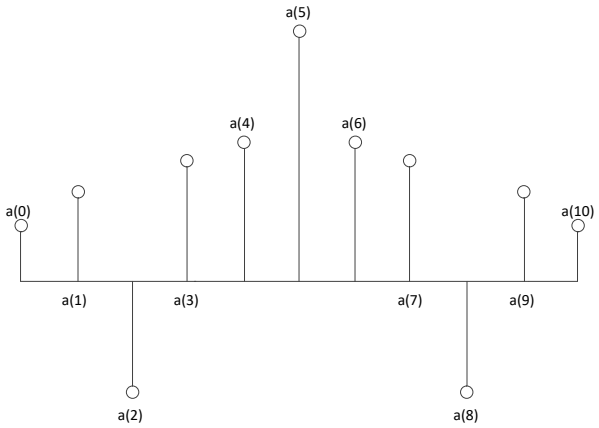

Figure 2-14 Even Symmetric Coefficient Structure Diagram

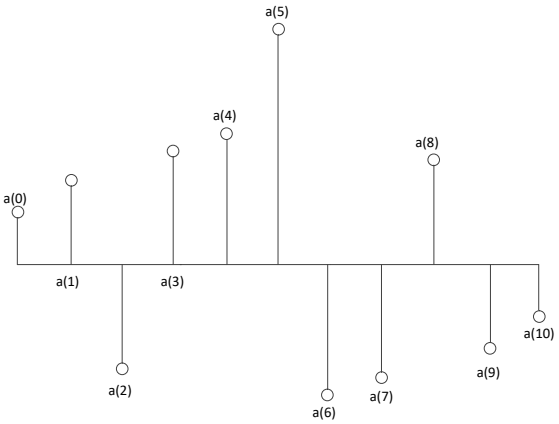

Figure 2-15 Odd Symmetric Coefficient Structure Diagram

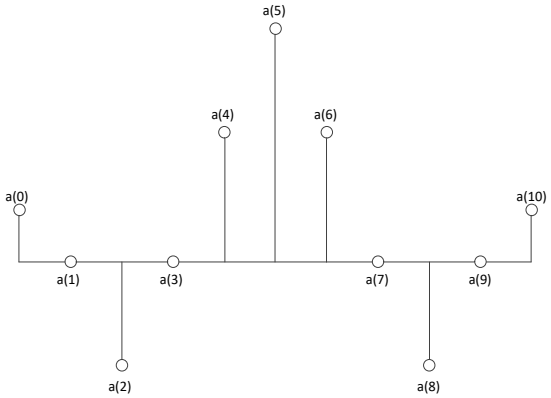

Figure 2-16 Half Band Coefficient Structure Diagram

Attention:

The coefficient structure configured to FIR IP via Coefficient Source must be consistent with the coefficient structure selected through Coefficient Structure;

According to the Half Band coefficient structure, when the IP is configured as a half-band filter structure, the number of coefficients required should be 4n+3 (n≥1).

2.8.3 Clock Constraints

FIR IP has only one clock. An example of constraints is as follows:

create_clock -name {i_clk} [get_ports {i_clk}] -period {10} -waveform {0.000 5.000}

2.8.4 C Model

FIR IP provides a bit-accurate C code model, which is provided as a dynamic link library. Additionally, C reference code is provided as an example to help users understand how to call the C model.

Attention:

The data type of the C model is double-precision floating point, and the maximum mantissa width may be less than the requirements for the calculation by FIR IP in certain configurations; therefore, there may be discrepancies between the C model calculations and RTL calculations.

Table 2-12 C Model File Description

File	Description
ipsxe_fir_def_v1_0.h	C model header file.
lib_ipsxe_fir_v1_0.so	Dynamic link library used for compiling in Linux system.
lib_ipsxe_fir_v1_0.lib	Dynamic link library used for compiling in Windows system.
ipsxe_fir_wrapper_tb.c	Top-level file for C model simulation.

The usage is as follows:

- On the Linux platform, run the compilation instruction to generate the executable program ipsxe_fir_wrapper_tb.
- gcc -o ipsxe_fir_wrapper_tb ipsxe_fir_wrapper_tb.c ./lib_ipsxe_fir_v1_0.so –lm
- On the Windows platform, run the compilation instruction to generate the executable program ipsxe_fir_wrapper_tb.exe.
- gcc -o ipsxe_fir_wrapper_tb ipsxe_fir_wrapper_tb.c ./lib_ipsxe_fir_v1_0.lib -lm

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