Compa Family CPLDs Device Power Consumption Control Application Guide

(AN03007, V1.2)

(28.10.2021)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.2	28.10.2021	Initial release

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
CPLD	Complex Programmable Logic Device
GTP	General Technology Primitive
POR	Power On Reset
PLL	Phase Lock Loop
bandgap	bandgap
SRB	Signal Relay Block

Related Documentation

The following documentation is related to this manual:

1. ***UG030004_Compa Family CPLD Configuration User Guide***

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Chapter 1 Overview

1.1 Introduction

This document serves as the application manual for the standby mode of the Compa Family CPLD devices launched by Shenzhen Pango Microsystems Co., Ltd. It allows users to control the devices to enter standby mode or wake up to resume normal operation as needed.

1.2 Main Functions

This document primarily introduces two standby mode application schemes:

2. Controlling the devices to enter standby mode using primitives such as GTP_POWERCTL;
3. Waking down the devices by pulling down the global signal.

The difference between the two schemes is: in scheme one, the register values of user logic do not change before and after wakeup, and the "done" in the status register remains unchanged as well. Scheme two achieves lower standby power consumption, but in standby mode, the register values of user logic are cleared, with "done" in the status register changing to 0 and then back to 1 upon wakeup.

1.3 Design Information

Table 1-1 Standby Mode Product Information

Standby Mode Product Information	
Supported Devices	Compa Family CPLD Devices
Supported User Interface	Custom
Provided Design Files	
Standby Mode Reference Design	Verilog file
Constraint File	fdc file
Development Tools	
Design Tools	Pango Design Suite 2019.3-PGC-beta4 and later versions

Chapter 2 Function Description

This document, taking the PGC4KL device as an example, introduces the application principles, implementation methods, operation procedures, and considerations for entering standby mode in both scheme one and scheme two.

2.1 Scheme One Function Description

2.1.1 Scheme One Power Consumption Control Design Architecture

In standby mode, all subsystems are shut down, such as the bandgap, on-die OSC, POR, PLL, output pins, and the majority of the core logic (including the clk tree), resulting in extremely low power consumption. Figure 2-1 is a diagram illustrating the standby mode application. After wakeup, the signal level from programmable logic to the interconnection line (SRB) maintains the pre-standby state, meaning the register values of user logic and "done" in the status register do not change before and after wakeup.

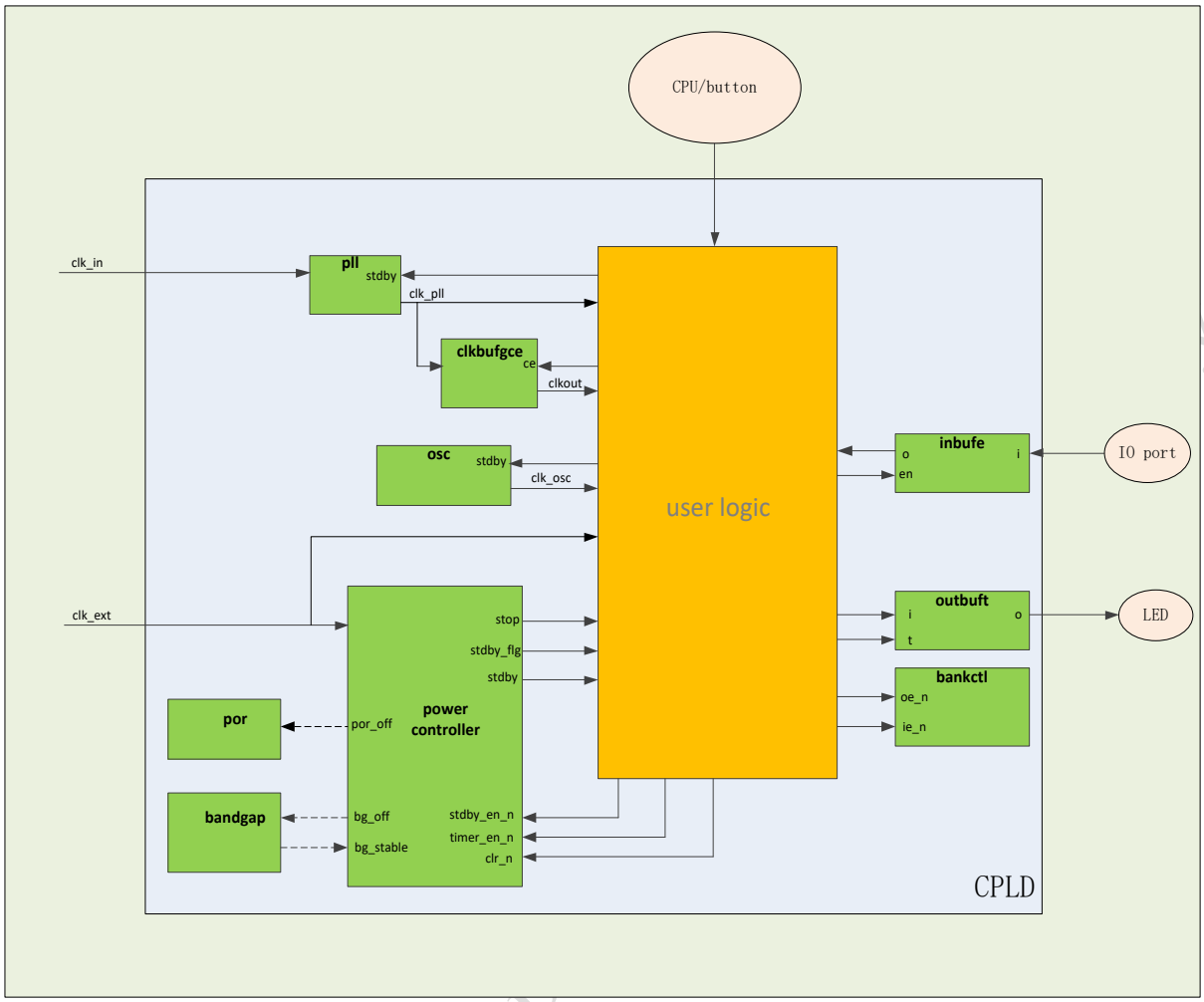

Figure 2-1 Standby Mode Application Diagram

Note:

1. The green box represents the hard core, and the orange box represents the FPGA logic implementation (which can be designed by users according to the application);
2. User logic can control POR and bandgap through the power controller, represented by hard connections (dashed lines in the diagram);
3. In both normal operating mode and standby mode, the external clock clk_ext is always working to facilitate device standby and wakeup.

In some applications, users can dynamically shut down some temporarily unused modules to save power, such as CLK TREE and IOB. Next, the document will introduce the primitives, such as GTP_POWERCTL, GTP_BANKCTL, GTP_OSC, GTP_INBUFE, GTP_OUTBUFT, GTP_CLKBUFGCE and other modules.

2.1.2 GTP_POWERCTL

2.1.2.1 Module Block Diagram

This GTP is used to control the circuit standby.

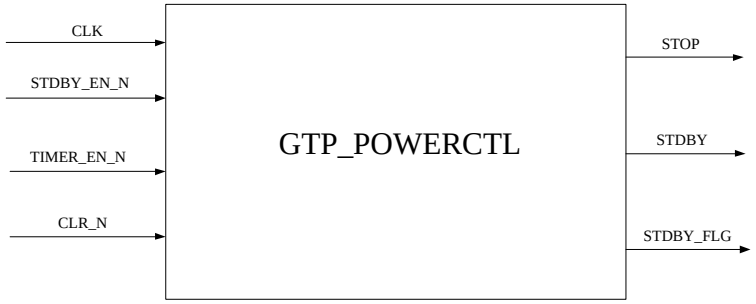

Figure 2-2 GTP_POWERCTL Module Block Diagram

2.1.3 Port List

Table 2-1 GTP_POWERCTL Interface List

Signal Name	Direction	Source/Purpose	Description
CLK	Input	SRB	External input clock, with a maximum frequency of 50MHz
STDBY_EN_N	Input	SRB	Standby enable, active low Enter the shutdown process from operating mode to standby mode, starting from the falling edge of standby enable. Enter the wake-up process from standby mode to operating mode, starting from the rising edge of standby enable
TIMER_EN_N	Input	SRB	Timer enable, active low Pulse signal, for starting the timer counting
CLR_N	Input	SRB	Standby complete, active low Pulse signal, for clearing the standby flag after wake-up
STOP	Output	SRB	Stop Used for standby preparation. User logic prepares for standby by shutting down signals such as the clock
STDBY	Output	SRB	Standby Global signal, output via SRB to user logic, IO PAD, and PLL. Used for controlling logic circuits to enter standby mode
STDBY_FLG	Output	SRB	Standby flag Indicates that the device is in standby mode

2.1.3.1 Mode Conversion

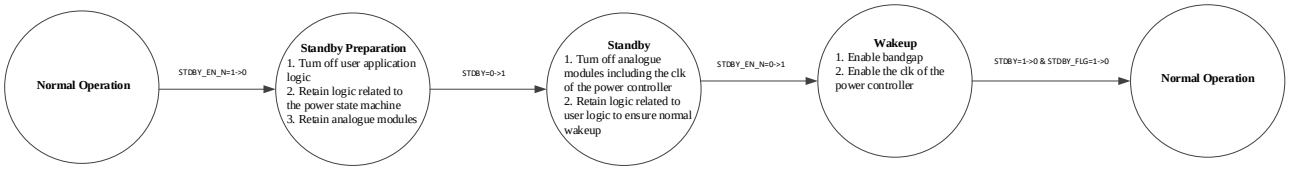

Figure 2-3 Entering and Exiting Standby Mode State Diagram

2.1.3.2 Interface Timing and Description

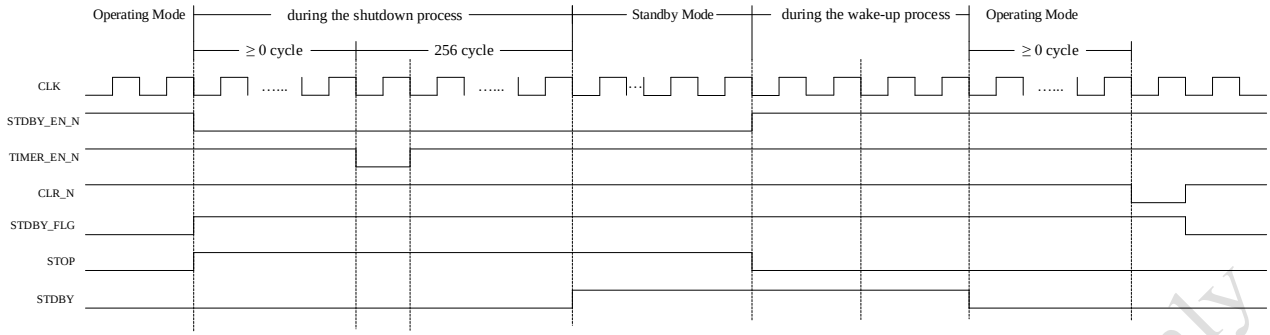

Figure 2-4 GTP_POWERCTL Interface Typical Timing

2.1.3.3 Shutdown Process

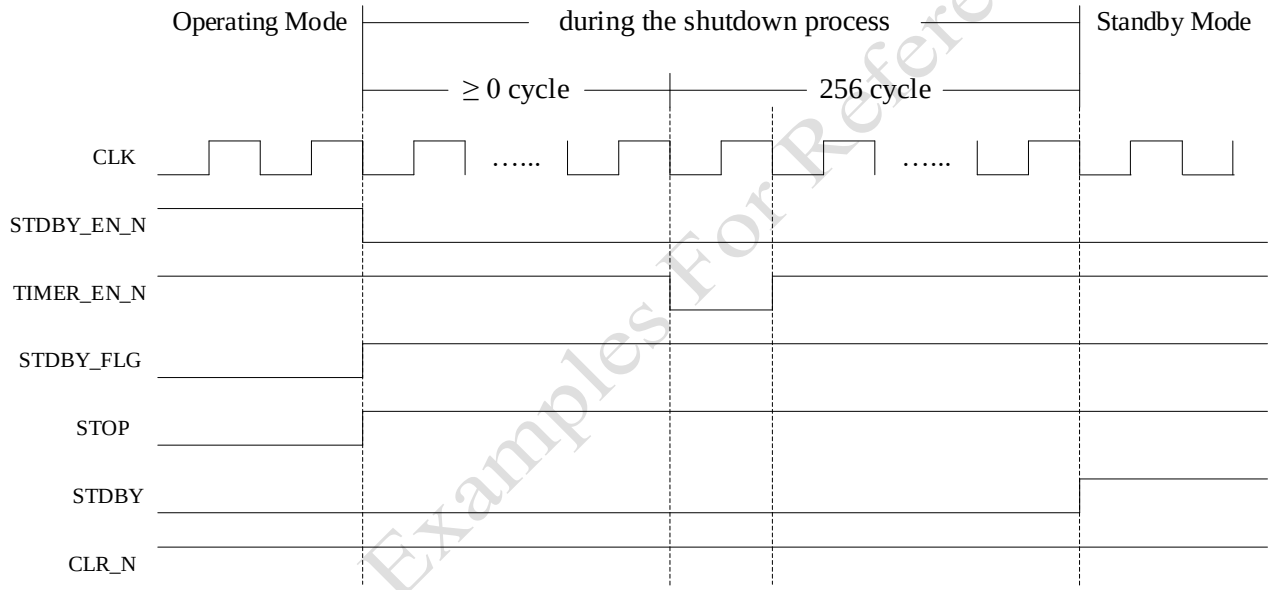

Figure 2-5Shutdown Process Timing Diagram

4. When the standby enable STDBY_EN_N changes to active from inactive, the power controller enters shutdown mode from operating mode:
   1) Generates a standby flag STDBY_FLG, indicating that the device is in standby mode.
   2) Generates a standby preparation STOP, where user logic prepares for standby through signals like shutdown clock.
5. The timer enable TIMER_EN_N pulse becomes active, starting the timer counting.
6. After counting 256 clock cycles by the timer:
   1) Generates a global standby signal which is outputted via SRB to user logic, IO PAD, OSC, and PLL for controlling logic circuits to enter standby mode.

2) Shuts down the band gap circuit and the power-up reset circuit. When the band gap circuit is shut down, the power-up reset circuit and analogue circuits (PLL, OSC) are also shut down.

Note: The 256 cycle shutdown process is implemented by internal circuits, with no need for user logic code.

2.1.3.4 Wakeup Process

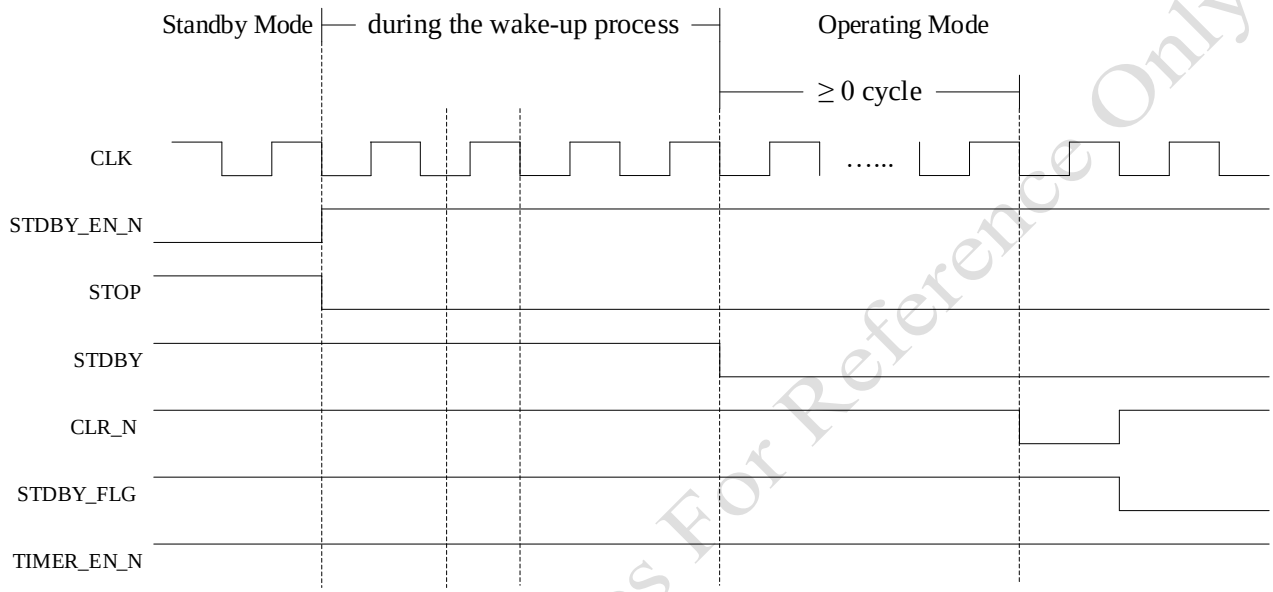

Figure 2-6 Wakeup Process Interface Timing

7. When the standby enable STDBY_EN_N changes from active to inactive, the power controller enters wake-up mode from standby mode:
   1) Clears standby preparation STOP.
   2) Turns on the band gap circuit.
8. After the band gap circuit stabilises, the global standby signal is cleared, and the power controller enters operating mode from wake-up mode.
9. After entering the operating mode, the user logic generates a standby end pulse:
   1) Turns on the power-up reset circuit.
   2) Clears the standby flag STDBY_FLG.

2.2 GTP_BANKCTL

GTP_BANKCTL supports dynamic enabling and disabling of true differential output in bank0 and differential input in banks 0~5 to save power when entering standby mode.

2.2.1.1 Module Block Diagram

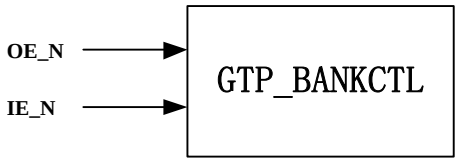

Figure 2-7 GTP_BANKCTL Module Block Diagram

2.2.1.2 Port List

Table 2-2 Port List

Port	Direction	Function Description
OE_N	Input	Disable or enable true differential output in bank0 from SRB. 0: Enable output; 1: Disable output
IE_N	Input	Disable or enable differential input in banks 0-5 from SRB. 0: Enable input; 1: Disable input

2.2.1.3 Port Design Rules

Controlled asynchronously by the user.

2.2.1.4 Parameter

Table 2-3 Parameter List

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
DIFFO_DYN_EN	string	“FALSE”,“TRUE”	“FALSE”	Differential output dynamic control. TRUE: Enable; FALSE: Disable
DIFFI_DYN_EN	string	“FALSE”,“TRUE”	“FALSE”	Differential input dynamic control. TRUE: Enable; FALSE: Disable
BANK_LOC	string	“BK0”, “BK1”, “BK2”, “BK3”, “BK4”, “BK5”	“BK0”	Specify bank location

2.2.1.5 Detailed Functions

- When parameter DIFFO_DYN_EN="TRUE", differential output is enabled for bank0 when signal OE_N=0 and disabled when OE_N=1.
- When parameter DIFFO_DYN_EN="FALSE", the dynamic control function for differential output is disabled.

- When parameter DIFFI_DYN_EN="TRUE", differential input is enabled for banks 0~5 when signal OE_N=0 and disabled when OE_N=1.
- When parameter DIFFI_DYN_EN="FALSE", the dynamic control function for differential input is disabled.

2.2.2 GTP_OSC

This GTP provides users with a configurable output clock.

2.2.2.1 Module Block Diagram

Figure 2-8 GTP_OSC Module Block Diagram

2.2.2.2 PORT Description

Figure 2-9 PORT Description

Port	Direction	Function Description
CLKOUT	Output	OSC clock output signal
CLKCRC	Output	CRC clock output signal
EN_N	Input	OSC shutdown signal, which turns off OSC when high and turns on OSC when low

2.2.2.3 Parameter

Table 2-4 Parameters

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
CLK_DIV	integer	0~127	0	Clock divider ratio configuration
USER_DIV_EN	string	“FALSE”,“TRUE”	“TRUE”	USER divider enable configuration

2.2.2.4 Detailed Functions

This GTP must be called when using the on-die oscillator of the CPLD. As shown in Table 8, the output clock frequency of the oscillator is configurable, with the configuration parameter CLK_DIV set to different values to output the corresponding division clock.

Note: When CLK_DIV is set to 0, a division by 128 is achieved; when set to 1, a division by 2 is achieved. For other values, the correspondence remains unchanged.

Table 2-5 Oscillator Output Frequency Configuration Table

CLK_DIV	**CLKOUT(MHz)**
0	266/128
1	266/2
2	266/2
3	266/3
…	…
125	266/125
126	266/126
127	266/127

2.2.3 GTP_INBUFE

GTP_INBUFE supports single-ended input driving function. Through this GTP, single-ended input IO can be shut down to reduce power consumption.

2.2.3.1 Module Block Diagram

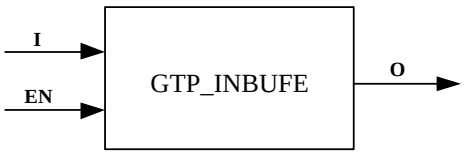

Figure 2-10 GTP_INBUFE Module Block Diagram

2.2.3.2 PORT Description

Table 2-6 Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	Output from input buffer to the chip
EN	Input	Input buffer is disabled when set to 0

2.2.3.3 Parameter

Table 2-7 Parameters

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
IOSTANDARD	string	LVTTL33 PCI33 LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12	DEFAULT =LVCMOS33	Input IO standard
TERM_DDR	string	None	“ON”	

2.2.4 GTP_OUTBUFT

GTP_OUTBUFT supports single-ended output driving function. Through this GTP, single-ended output IO can be shut down to reduce power consumption.

2.2.4.1 Module Block Diagram

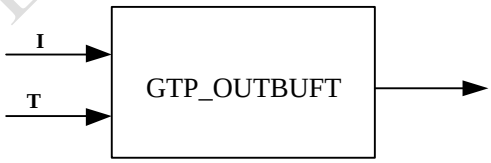

Figure 2-11 GTP_OUTBUFT Module Block Diagram

2.2.4.2 PORT Description

Table 2-8 Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	buffer output
T	Input	Enable signal, active when set to 0

2.2.4.3 Parameter

Table 2-9 Parameters

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
IOSTANDARD	string	LVTTL33 PCI33 LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12	DEFAULT =LVCMOS33	Input IO standard
SLEW_RATE	string	“SLOW”, “FAST”	“SLOW”	Slew rate
DRIVE_STRENGTH	string	"2", "4", "6", "8", "12", "16", "24"	"8"	Drive current strength

2.2.4.4 Detailed Functions

When T is active, the signal (I) from inside the chip is driven to the PAD; otherwise the output is tri-state.

2.2.5 GTP_CLKBUFGCE

This GTP provides a BUFFER with enable CE control for the GLOBAL CLOCK to shut down the global clock.

2.2.5.1 Module Block Diagram

Figure 2-12 GTP_CLKBUFGCE Module Block Diagram

2.2.5.2 PORT Description

Table 2-10 Port Description

Port	Direction	Function Description
CLKIN	Input	BUFFER input clock
CLKOUT	Output	BUFFER output clock
CE	Input	BUFFER enable end

2.2.5.3 Parameter

Table 2-11 Parameters

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
DEFAULT_VALUE	Character	1’b0, 1’b1	1’b0	When DEFAULT_VALUE=1'b0 and CE=0, the BUFFER outputs 1'b0; When DEFAULT_VALUE=1'b1 and CE=0, the BUFFER outputs 1'b1;

2.2.5.4 Detailed Functions

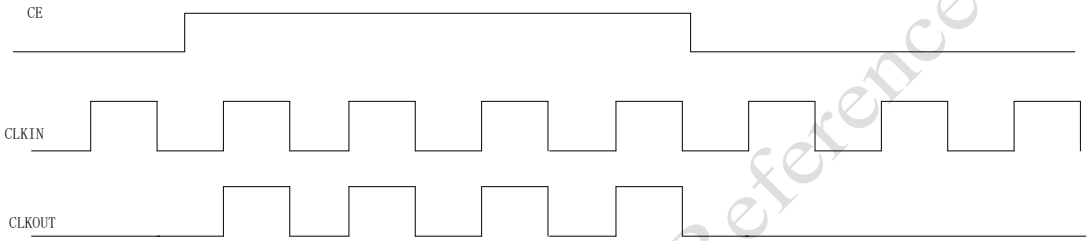

Figure 2-13 CE Control Diagram

2.3 Scheme Two Function Description

Devices are woken down by pulling down global signal. In standby mode, the register values of user logic are cleared, with "done" in the status register changing to 0 and then back to 1 upon wakeup. SRAM is not cleared upon wakeup, and there is no need to reconfigure the bitstream. Standby wakeup can be achieved through JTAG/SPI/I2C interfaces. The specific operation process is shown below:

2.3.1 JTAG Interface Operation Process

Table 2-12 JTAG Standby Process

Load CFGI instruction into instruction register IR
Enter the Run-Test/Idle state, to last for a minimum of 125 TCK cycles
Load JWAKEDOWN instruction into IR
Enter the Run-Test/Idle state, to last for a minimum of 30 TCK cycles (User clock wake-up, to last for a minimum of 30 UCLK cycles)
Load CFGI instruction into IR
Enter Shift-DR state:
Synchronization
Write GODOWN command to command register CMDR
Enter the Test Logic Reset state

For JTAG instruction set, refer to JTAG Instruction Set in Appendix; for related operations, refer to Chapters 7 and 8 in the "***UG030004_Compa Family CPLD Configuration User Guide***".

Table 2-13 JTAG Wakeup Process

Load CFGI instruction into IR
Enter the Run-Test/Idle state, to last for a minimum of 125 TCK cycles
Enter Shift-DR state:
Synchronization
Write "GUP" command to CMDR register
Write "SWAKEUP" command to CMDR register
Write a DESYNC instruction to CMDR register
Enter the Test Logic Reset state
Load CFGI instruction into IR
Enter the Run-Test/Idle state, to last for a minimum of 125 TCK cycles
Load JWAKEUP instruction into IR
Enter the Run-Test/Idle state, to last for a minimum of 30 TCK cycles (User clock wake-up, to last for a minimum of 30 UCLK cycles)
Enter the Test Logic Reset state

2.3.2 Slave SPI/Slave I2C Interface Operation Process

Table 2-14 Slave SPI/Slave I2C Standby Process

Write the "WREN" instruction
Write the CFG instruction, load:
1 padding word (32'hFFFFFFFF)
SYNC WORD
Write a SWAKEDOWN instruction to CMDR register
Write the RDSR instruction and read STATUSR register in a loop until wakedown_over is detected high
Write the CFG instruction, load:
Write "GODOWN" command to CMDR register
Write a DESYNC instruction to CMDR register
100 NOP
Write the "WRDIS" instruction

For slave SPI/Slave I2C instruction set, refer to Slave SPI/Slave I2C Instruction Set in Appendix; for related operations, refer to "Chapters 7 and 8" in the "***UG030004_Compa Family CPLD Configuration User Guide***".

Table 2-15 Slave SPI/Slave I2C Wakeup Process

Write the "WREN" instruction
Write the CFG instruction, load:
1 padding word (32'hFFFFFFFF)
SYNC WORD
Write "GUP" command to CMDR register
Write "SWAKEUP" command to CMDR register
Write a DESYNC instruction to CMDR register
100 NOP
Write the "WRDIS" instruction
Write the RDSR instruction and read STATUSR register in a loop until wakeup_over is detected high

Chapter 3 Reference Designs

3.1 Scheme One Reference Design

3.1.1 Scheme One Reference Function Design

This reference design uses GTP primitives and user logic to turn off on-die OSC, PLL, and differential IO. Button control can be used to enter standby mode or wake up from standby mode to enter normal operating mode.

3.1.2 Scheme One Reference Design Interface List

Table 3-1 Reference Design Interface List

Signal Name	I/O	Bit width	Signal Description
Global Signal			
clk_ext	input	1	GTP_POWERCTL module input clock, with a frequency of 20MHz
rstn_in	input	1	Global reset signal, active-low
Control Signals			
key_stdby_wakeup	input	1	Button to control the program to enter standby mode or wake up to enter normal operating mode
Read/write DRM signal			
led_drm_err	output	1	Read/write DRM error indicator; "on" indicates an error
Indicator			
led_lut_toggle	output	1	Logic toggle error indicator
led_flashing	output	1	For debugging; indicating device operating status
pin_bank3_test1	output	1	For debugging
pin_bank2_test1	output	1	For debugging
pin_bank0_test	output	2	For debugging

3.1.3 Scheme One Reference Design File Directory

```
PGC4KL_PWR_CTRL Design Instance Directory Structure Diagram
|  high_resource.pds                          // PDS Project File
├─doc                                         // Design Documentation
├─ipcore                                      //
|  └─pll0                                     //
|         pll0.idf                            // PLL IP
|         pll0.v                              //
└─source                                      //
    |  clk_rst.v                              //Clock Reset Module
    |  clm_4lut5_2ff.v                        //CLM's LUT FF Cascading Module
    |  drm_top.v                              //DRM Read/Write Module
    |  gtp_power_controller.v                 //Power Control Module
    |  high_resource.fdc                      //Location Constraints and Physical Constraints File
    |  lut_ff_cascade_top.v                   //LUT FF Cascading Module
    |  pgr_rst_debounce_v1.0.v                //Reset Debounce Module
    |  pgr_signal_debounce.v                  //Key Debounce Module
    |  power_controller_top.v                 //Power Control Module
    |  power_controller_top_tb.v              //Simulation File
    ├─high_resource                           //
    |      global_defines0.vh                 //Global Parameter Definition
    |      lut_2ff_cascade2.v                 //LUT FF Cascading Module
    |      lut_2ff_cascade3.v                 //LUT FF Cascading Module
    |      pgl22_5drm_cascade.v               //DRM Read/Write Module
    |      pgl22_drm_cascade.v                //DRM Read/Write Module
    |      toggle_rate_ctrl.v                 //Toggle Rate Control Module
    |      toggle_rate_ctrl2.v                //Toggle Rate Control Module
    └─sdpram01                                //
        |  sdpram01.idf                       //DRM IP
        |  sdpram01.v                         //
        └─rtl                                 //
              ipmc_sdpram_v1_3_sdpram01.v     //
```

Figure 3-1 Reference Design File Directory

3.1.4 Scheme One Reference Design On-board Verification

Download the bitstream to the test board, press the key_stdby_wakeup button to enter standby mode, and then press the key_stdby_wakeup button again to wake up and return to normal operating mode. Use DC power analyzer to power the board, record VCC current and VCCIO current in standby mode. Refer to Table 3-2.

Table 3-2 Standby Mode Power Consumption Test Table

Device	**VCC Current (mA)**	**VCCIO Current (mA)**	**Standby Power Consumption (mW)**
PGC4KL-UWG81	3.8	0.5	5.46

3.2 Scheme Two Reference Design

3.2.1 Scheme Two Reference Function Design

This reference design implements the wakeup process from standby mode through the Slave SPI interface to get the lowest standby power consumption.

3.2.2 Scheme Two Reference Design On-board Verification

Use MCU as the master device and PGC4KL as the slave device, and follow the Slave SPI Standby Wakeup Process to enter standby mode and return to normal operating mode without reloading the bitstream after wakeup. Power with a DC power analyzer, record VCC current and VCCIO current in standby mode.

Table 3-3 Standby Mode Power Consumption Test Table (Slave SPI)

Device	**VCC Current (mA)**	**VCCIO Current (mA)**	**Standby Power Consumption (mW)**
PGC4KL-UWG81	1.3	1	4. 86

Chapter 4 Appendix

Table 4-1 JTAG Instruction Set

Instruction	Types	Op Code	Description
BYPASS	1149.1 Non-test instruction	1111111111	Bypass instruction
SAMPLE/PRELOAD	1149.1 Non-test instruction	1010000000	Sample/preload instruction
EXTEST	1149.1 Test instruction	1010000001	External test instruction
INTEST	1149.1 Test instruction	1010000010	Internal test instruction
IDCODE	1149.1 Non-test instruction	1010000011	Identification instruction
HIGHZ	1149.1 Test instruction	1010000101	High-Z instruction
JRST	Only for design	1010001010	Reset instruction
CFGI	Only for design	1010001011	Configuration instruction
CFGO	Only for design	1010001100	Readback instruction
JWAKEUP	Only for design	1010001101	Wakeup instruction
JWAKEDOWN	Only for design	1010001110	Shutdown instruction
READ_UID	Only for design	0101001100	Read-UID instruction
RDSR	Only for design	0101011001	Read-Status-Register instruction
WADR	Only for design	0101011010	Write-Address instruction
HIGHZEN	Only for design	0101011011	High-Z enable instruction
HIGHZDIS	Only for design	0101011100	High-Z disable instruction
ERASE	Only for design	0101011101	Erase instruction
PROGRAM	Only for design	0101100000	Program instruction
PROGRAM_CTL	Only for design	0101100001	Program-Control instruction
READ	Only for design	0101100010	Read instruction
READ_CTL	Only for design	0101100011	Control-Read instruction
PROGRAM_LOCK	Only for design	0101100100	Embedded FLASH lock instruction
READ_LOCK	Only for design	0101100101	Embedded FLASH lock flag read instruction
EFLASH_SLEEP	Only for design	0101100110	Embedded FLASH sleep instruction
EFLASH_WAKEUP	Only for design	0101100111	Embedded FLASH wakeup instruction
PCTLR_WAKEUP	Only for design	0110000110	Power controller wakeup instruction
PCTLR_STDBY	Only for design	0110000111	Power controller standby instruction

Table 4-2 Slave SPI/Slave I2C Instruction Set

Instruction	Description	Op Code
NOP	No Operation	FF
READBACK	Readback Configuration Memory/Register	A0
RDID	Read Identification	A1
RDUSER	Read Usercode	A2
RDSR	Read Status Register	A3
RDUID	Read Unique Identification	A4
RDLOCK	Read Embedded FLASH Lock Information	A5
RDRDC	Read Read Check Bit	A6
CFG	Config Bitstream	50
WREN	Write Enable	51
WRDIS	Write Disable	52
ISC_ENABLE	ISC Enable After the "ISC_ENABLE" instruction is loaded, the device first samples the output value of the pins to the boundary scan register, then hands over control of the output pins to the boundary scan register	53
ISC_DISABLE	ISC Disable	54
RESET	Reset CPLD	60
ERASE	Erase Bulk	10
PROGRAM	Program Page	20
PROGRAM_UID	Program Unique ID	21
PROGRAM_CTL	Program Feature Control Page	22
READ	Read	30
READ_CTL	Read Feature Control Page	31
READ_TRIM	Read Trim Page	32
PROGRAM_LOCK	Lock Embedded FLASH	40
EFLASH_SLEEP	Embedded FLASH Sleep	70
EFLASH_WAKEUP	Embedded FLASH Wake Up	71
PCTLR_WAKEUP	Power Controller Wake Up	72
PCTLR_STDBY	Power Controller Standby	73

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