SGMII and QSGMII Flexible Mixed-use Design Application Guide

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.1	20.02.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
HSSTLP	High Speed Serial Transceiver Low Performance
PCS	Physical Code Sublayer
PM A	Physical Media Attachment
GM II	1Gigabit Media Independent Interface

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Chapter 1 Overview

1.1 Introduction

This document serves as the application manual for the Ethernet system interface product launched by Shenzhen Pango Microsystems Co., Ltd. This document primarily introduces the function list, design architecture, interface definition, interface timing, supported devices and reference designs of SGMII and QSGMII Flexible Mixed-use Design.

In the Logos2 family FPGA, HSSTLP has only two lpll, resulting in 4 lanes that cannot be freely used. In multi-lane applications, it cannot directly invoke multiple sgmii Ips and qsgmii Ips for mixed-use. This design provides users with SGMII And QSGMII IP flexible mixed-use implementation Scheme through parametrized settings.

1.2 Main Functions

It mainly realizes the flexible mixed-use of PCS from sgmii and qsgmii within one quad. The current version only supports the following four types of modes:

1. sgmii (lane0) + sgmii (lane1) + qsgmii (lane2) + qsgmii (lane3)
2. qsgmii (lane0) + qsgmii (lane1) + qsgmii (lane2) + qsgmii (lane3)
3. qsgmii (lane0) + qsgmii (lane1)
4. Sgmii (lane0) + sgmii (lane1) + sgmii (lane2)

1.3 Design Information

Table 1-1 SGMII and QSGMII Flexible Mixed-use Design Information

SGMII and QSGMII Flexible Mixed-use Design	
Supported Devices	PG2L50H family FPGA products
Supported User Interface	GMII Interface
Provided Design Files	
QSGMII and SGMII PCS Design Document	Encrypted file
SGMII and QSGMII Design Top-level and Reference Design	Verilog files
Constraint File	fdc file

Development Tools	
Design Tools	PDS Development Suite Pango Design Suite 2021 Supported. 1-SP2 versions
Simulation Tool	The third party tool

1.4 Resource Usage

Refer to SGMII and QSGMII IP resources to determine based on the actual number of IP calls.

Chapter 2 Function Description

SGMII and QSGMII Flexible Mixed-use Design primarily separate PCS and HSST from the SGMII IP and QSGMII IP respectively. The parameterized calls are implemented according to the user's configuration.

2.1 SGMII and QSGMII Flexible Mixed-use Ethernet System Design Architecture

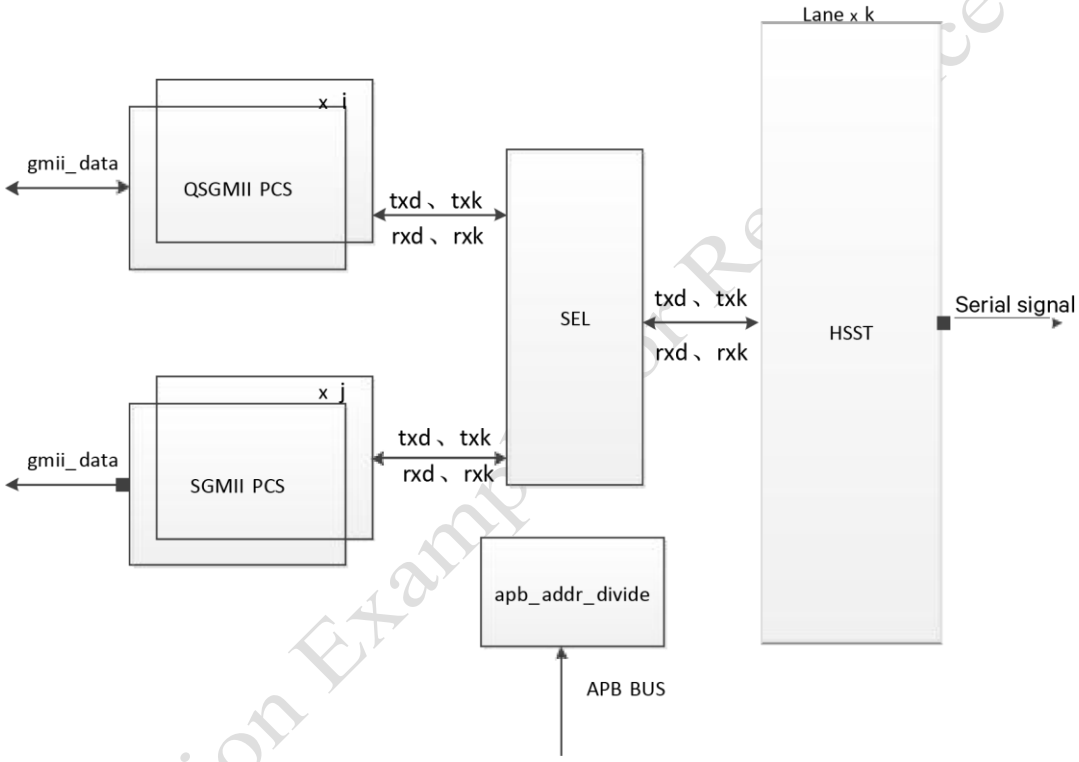

Figure 2-1 Block Diagram of Ethernet System Functions

The entire design consists of 5 parts: HSST, QSGMII PCS, SGMII PCS, Selection Logic and APB Address Partition Module.

HSST:

The number (k) of lanes used by HSST is determined by the user through configuration parameter LANE*_PROTOCOL. Configuration value is set to No. "DISABLE" indicates that the current lane is in use. The value of k is no more than 4, k = i + j.

QSGMII PCS:

QSGMII PCS is a PCS module stripped from the QSGMII IP. The number (i) of module calls is determined by the user through configuration parameter LANE*_PROTOCOL, with the value of "QSGMII", indicating that the current lane uses the QSGMII protocol. The value of i is no more than 4.

SGMII PCS:

SGMII PCS is a PCS module stripped from the SGMII IP. The number (j) of module calls is determined by the user through configuration parameter LANE*_PROTOCOL, with the value not set to "QSGMII" or "DISABLE", indicating that the current lane uses the SGMII or GE protocol. j is no more than 4.

Selection Logic:

Determine the selection of the clock, PLL, mode and data path based on user-configured parameters.

apb_addr_divide module:

Mainly to implement QSGMII PCS, SGMII PCS and APB address partition of HSST access space.

2.2 Interface List

Table 2-1 Interface List

Signal Name	Input/Output	Bit width	Description
Global signals			
external_rstn	Input	1	Global reset signal, active-low
free_clk	Input	1	Configuration clock, 10–100M
cfg_rstn	Output	1	Configuration reset signal output by SGMII Core, operating in the free_clk clock domain. 0: Reset; 1: Reset release.
HSST interfaces			
REFCK0N	Input	1	HSST Reference Clock 0. 125M or 156.25M
REFCK0P	Input	1	HSST Reference Clock 0. 125M or 156.25M
REFCK1N	Input	1	HSST Reference Clock 1. 125M or 156.25M
REFCK1P	Input	1	HSST Reference Clock 1. 125M or 156.25M
L0TXN	Output	1	LANE0 transmits differential signal, N side

Signal Name	Input/Output	Bit width	Description
L0TXP	Output	1	LANE0 transmits differential signal, P side
L0RXN	Input	1	LANE0 receives differential signal, N side
L0RXP	Input	1	LANE0 receives differential signal, P side
L1TXN	Output	1	LANE1 transmits differential signal, N side
L1TXP	Output	1	LANE1 transmits differential signal, P side
L1RXN	Input	1	LANE1 receives differential signal, N side
L1RXP	Input	1	LANE1 receives differential signal, P side
L2TXN	Output	1	LANE2 transmits differential signal, N side
L2TXP	Output	1	LANE2 transmits differential signal, P side
L2RXN	Input	1	LANE2 receives differential signal, N side
L2RXP	Input	1	LANE2 receives differential signal, P side
L3TXN	Output	1	LANE3 transmits differential signal, N side
L3TXP	Output	1	LANE3 transmits differential signal, P side
L3RXN	Input	1	LANE3 receives differential signal, N side
L3RXP	Input	1	LANE3 receives differential signal, P side
hsst_ch_ready	Output	4	HSSTLP IP Serdes RX channel reset completion flag, with bit3~bit0 corresponding to Lane3~Lane0, defaulting to Lane0. 0: HSSTLP IP Serdes RXchannel reset not completed; 1: HSSTLP IP Serdes RX channel reset completed. Note: The signal operates within the free_clk clock domain.
signal_loss	Output	4	Bit3~Bit0 correspond to Lane3~Lane0 respectively 0: Indicates a valid signal was detected from the port P_L*RXP/P_L*RXN; 1: Indicates no valid signal was detected from the port P_L*RXP/P_L*RXN Note: This is an asynchronous signal.
cdr_align	Output	4	Bit3~Bit0 correspond to Lane3~Lane0 respectively 0: Indicates CDR lock signal not established; 1: Indicates CDR lock signal successfully established. Note: This is an asynchronous signal.
tx_pll_lock	Output	2	Bit1~bit0 correspond to pll1 and pll0 0: PLL is not locked; 1: PLL is locked. Note: This is an asynchronous signal.
lsm_synced	Output	4	Bit3~Bit0 correspond to Lane3~Lane0 respectively 0: Word Align not successful; 1: Word Align successful. Note: This is an asynchronous signal.
txpll_sof_rst_n	Input	2	Bit1~bit0 correspond to pll1 and pll0 HSSTLP IP PLL soft reset. 0: Reset; 1: Reset release; Note: This signal is synchronized internally in HSSTLP IP to the free_clk clock domain.
hsst_cfg_soft_rstn	Input	4	Bit3~Bit0 correspond to Lane3~Lane0 respectively HSSTLP IP configuration module soft reset signal. 0: Reset; 1: Reset release;

Signal Name	Input/Output	Bit width	Description
			Note: This reset is located in the free_clk clock domain; Perform one external_rstn after enabling this reset.
txlane_sof_rst_n	Input	4	Bit3~Bit0 correspond to Lane3~Lane0 respectively HSSTLP IP Serdes TX channel soft reset. 0: Reset; 1: Reset release. Notes: This signal is synchronised internally in the HSSTLP IP to the free_clk clock domain, used only during debugging, and after the TX reset, the RX reset is required.
rxlane_sof_rst_n	Input	4	Bit3~Bit0 correspond to Lane3~Lane0 respectively HSSTLP IP Serdes RX channel soft reset, with bit3~bit0 corresponding to Lane3~Lane0 respectively, defaulting to Lane0. 0: Reset; 1: Reset release; Notes: This signal is synchronised internally in the HSSTLP IP to the free_clk clock domain, used only during debugging.
wtchdg_clr	Input	2	HSSTLP IP reset sequence watchdog clear signal, used during debugging. 0: Normal operation; 1: Watchdog counter cleared; Note: The signal is required to operate within the free_clk clock domain.
SGMII Interface			
The specific signal is the same as SGMII IP, supports up to 4 channels (CH0 to CH3), and CH0-CH3 don't correspond to Lane0-Lane3, and are configured by the user; when using one SGMII channel, use CH0; when using two SGMII channels, use CH0-CH1, and so on.			
QSGMII Interface			
The specific signal is the same as QGMII IP, supports up to 4 channels (CH0 to CH3), and CH0-CH3 don't correspond to Lane0-Lane3, and are configured by the user; when using one QGMII channel, use CH0; when using two QGMII channels, use CH0-CH1, and so on.			
Configuration signals			
apb_clk	Input	1	Configuration clock signal, with a frequency range of 10–100MHz
apb_penable	Input	1	Configuration access enable
apb_pwrite	Input	1	Read/write selection configuration signal, high for write, and low for read
apb_paddr	Input	19	Configuration address bus
apb_pwdata	Input	32	Configuration write data
apb_psel	Input	1	Configuration selection signal
apb_prdata	Output	32	Configuration read data
apb_pready	Output	1	Configure read/write ready output
Debug Signal			
pcs_nearend_loop	Input	4	Bit3~Bit0 correspond to Lane3~Lane0 respectively PCS parallel near-end loopback enable signal. 0: PCS parallel near-end loopback disabled. 1: PCS parallel near-end loopback enabled.
pcs_farend_loop	Input	4	Bit3~Bit0 correspond to Lane3~Lane0 respectively PCS parallel far-end loopback enable signal. 0: PCS parallel far-end loopback disabled; 1: PCS parallel far-end loopback enabled.

Signal Name	Input/Output	Bit width	Description
pma_nearend_ploop	Input	4	Bit3~Bit0 correspond to Lane3~Lane0 respectively PMA serial near-end loopback enable signal. 0: PMA serial near-end loopback disabled; 1: PMA serial near-end loopback enabled.
pma_nearend_sloop	Input	4	Bit3~Bit0 correspond to Lane3~Lane0 respectively PMA parallel near-end loopback enable signal. 0: PMA parallel near-end loopback enabled; 1: PMA parallel near-end loopback enabled.

2.3 Parameter Definitions

Table 2-2 Top-level Parameter Definitions

Parameter	Description
LANE0_PROTOCOL	Select the protocol type for LANE0, the selectable types are as follows: SGMII: SGMII mode, equivalent to the SGMII mode in SGMII IP. GE: GE mode, equivalent to the GE mode in SGMII IP. SGMII_GE: Compatible with SGMII and GE modes, equivalent to the BOTH mode in SGMII IP. QSGMII: QSGMII mode DISABLE: Disable this lane
LANE0_PLL	Select the PLL to be used by LANE0, equivalent to the pll selection of HSSTLP IP, and the optional values are: PLL0 and PLL1
LANE0_CLK_SOURCE	Select the reference clock source for LANE0, equivalent to the clock source selection of HSSTLP IP, and the optional values are: Diff_REFCK0 and Diff_REFCK1
LANE0_REF_CLK_FREQ	Select the reference clock frequency for LANE0, and the optional values are: 125.0 and 156.25
LANE0_BUFFER	Select whether to use the internal elastic buffer of SGMII or QSGMII IP, equivalent to the no buffer setting of SGMII or QSGMII IPinterface, and the optional values are: FALSE: Do not use internal buffer TRUE: Use internal buffer
LANE0_PHY_MODE	Select SGMII or QSGMII mode, and the optional values are: 0: PHY_MODE 1: MAC_MODE
LANE0_AUTO_NEGOTIATION	Select SGMII or QSGMII and enable auto-negotiation module, and the optional values are: TRUE: Auto-negotiation enabled FALSE: Auto-negotiation not enabled
LANE0_MDIO_ENABLE	Select whether to enable MDIO configuration interface, and the optional values are: TRUE: MDIO interface enabled FALSE: MDIO interface not enabled
LANE1_PROTOCOL	Select the protocol type for LANE1, the selectable types are as follows: SGMII: SGMII mode, equivalent to the SGMII mode in SGMII IP. GE: GE mode, equivalent to the GE mode in SGMII IP. SGMII_GE: Compatible with SGMII and GE modes, equivalent to the BOTH mode in SGMII IP. QSGMII: QSGMII mode DISABLE: Disable this lane
LANE1_PLL	Select the PLL to be used by LANE1, equivalent to the pll selection of HSSTLP IP, and the optional values are: PLL0 and PLL1
LANE1_CLK_SOURCE	Select the reference clock source for LANE1, equivalent to the clock source selection of HSSTLP IP, and the optional values are: Diff_REFCK0

Parameter	Description
	and Diff_REFCK1
LANE1_REF_CLK_FREQ	Select the reference clock frequency for LANE1, and the optional values are: 125.0 and 156.25
LANE1_BUFFER	Select whether to use the internal elastic buffer of SGMII or QSGMII IP, equivalent to the no buffer setting of SGMII or QSGMII IPinterface, and the optional values are: FALSE: Do not use internal buffer TRUE: Use internal buffer
LANE1_PHY_MODE	Select SGMII or QSGMII mode, and the optional values are: 0: PHY_MODE 1: MAC_MODE
LANE1_AUTO_NEGOTIATION	Select SGMII or QSGMII and enable auto-negotiation module, and the optional values are: TRUE: Auto-negotiation enabled FALSE: Auto-negotiation not enabled
LANE1_MDIO_ENABLE	Select whether to enable MDIO configuration interface, and the optional values are: TRUE: MDIO interface enabled FALSE: MDIO interface not enabled
LANE2_PROTOCOL	Select the protocol type for LANE2, the selectable types are as follows: SGMII: SGMII mode, equivalent to the SGMII mode in SGMII IP. GE: GE mode, equivalent to the GE mode in SGMII IP. SGMII_GE: Compatible with SGMII and GE modes, equivalent to the BOTH mode in SGMII IP. QSGMII: QSGMII mode DISABLE: Disable this lane
LANE2_PLL	Select the PLL to be used by LANE2, equivalent to the pll selection of HSSTLP IP, and the optional values are: PLL0 and PLL1
LANE2_CLK_SOURCE	Select the reference clock source for LANE2, equivalent to the clock source selection of HSSTLP IP, and the optional values are: Diff_REFCK0 and Diff_REFCK1
LANE2_REF_CLK_FREQ	Select the reference clock frequency for LANE2, and the optional values are: 125.0 and 156.25
LANE2_BUFFER	Select whether to use the internal elastic buffer of SGMII or QSGMII IP, equivalent to the no buffer setting of SGMII or QSGMII IPinterface, and the optional values are: FALSE: Do not use internal buffer TRUE: Use internal buffer
LANE2_PHY_MODE	Select SGMII or QSGMII mode, and the optional values are: 0: PHY_MODE 1: MAC_MODE
LANE2_AUTO_NEGOTIATION	Select SGMII or QSGMII and enable auto-negotiation module, and the optional values are: TRUE: Auto-negotiation enabled FALSE: Auto-negotiation not enabled
LANE2_MDIO_ENABLE	Select whether to enable MDIO configuration interface, and the optional values are: TRUE: MDIO interface enabled FALSE: MDIO interface not enabled

Parameter	Description
LANE3_PROTOCOL	Select the protocol type for LANE3, the selectable types are as follows: SGMII: SGMII mode, equivalent to the SGMII mode in SGMII IP. GE: GE mode, equivalent to the GE mode in SGMII IP. SGMII_GE: Compatible with SGMII and GE modes, equivalent to the BOTH mode in SGMII IP. QSGMII: QSGMII mode DISABLE: Disable this lane
LANE3_PLL	Select the PLL to be used by LANE3, equivalent to the pll selection of HSSTLP IP, and the optional values are: PLL0 and PLL1
LANE3_CLK_SOURCE	Select the reference clock source for LANE3, equivalent to the clock source selection of HSSTLP IP, and the optional values are: Diff_REFCK0 and Diff_REFCK1
LANE3_REF_CLK_FREQ	Select the reference clock frequency for LANE3, and the optional values are: 125.0 and 156.25
LANE3_BUFFER	Select whether to use the internal elastic buffer of SGMII or QSGMII IP, equivalent to the no buffer setting of SGMII or QSGMII IPinterface, and the optional values are: FALSE: Do not use internal buffer TRUE: Use internal buffer
LANE3_PHY_MODE	Select SGMII or QSGMII mode, and the optional values are: 0: PHY_MODE 1: MAC_MODE
LANE3_AUTO_NEGOTIATION	Select SGMII or QSGMII and enable auto-negotiation module, and the optional values are: TRUE: Auto-negotiation enabled FALSE: Auto-negotiation not enabled
LANE3_MDIO_ENABLE	Select whether to enable MDIO configuration interface, and the optional values are: TRUE: MDIO interface enabled FALSE: MDIO interface not enabled

2.4 Interface Timing

Refer to "***UG042007_Logos2_QSGMII_IP***" and "***UG042005_Logos2_SGMII_ 1GbE_IP***"

Chapter 3 Register Descriptions

HSST is accessed through APB interface. For the list of registers, refer to HSST manual "***UG040008_Logos2 Family FPGA***". High-Speed Serial Transceiver Low Performance (HSSTLP) User Guide

The PCS registers of QSGMII and SGMII can be accessed throughMDIO (LANE*_MDIO_ENABLE parameter configured to TRUE) or APB interface. MDIO access method is the same as IP. The address partition of PCS by APB access method can be implemented within the module. For PCS registers, refer to IP user documentation. Internal APB address partition is as follows, users can also allocate by themselves based on actual needs:

Table 3-1 Address Allocation

Addr [17] ==1'd0	HSST access space
Addr [17] == 1'd1 & Addr[16:12]=5'd0	First channel SGMII PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd1	Second channel SGMII PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd2	Third channel SGMII PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd3	Fourth channel SGMII PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd4	First channel QSGMII port0 PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd5	First channel QSGMII port1 PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd6	First channel QSGMII port2 PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd7	First channel QSGMII port3 PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd8	Second channel QSGMII port0 PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd9	Second channel QSGMII port1 PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd10	Second channel QSGMII port2 PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd11	Second channel QSGMII port3 PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd12	Third channel QSGMII port0 PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd13	Third channel QSGMII port1 PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd14	Third channel QSGMII port2 PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd15	Third channel QSGMII port3 PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd16	Fourth channel QSGMII port0 PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd17	Fourth channel QSGMII port1 PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd18	Fourth channel QSGMII port2 PCS access space
Addr [17] == 1'd1 & Addr[16:12]=5'd19	Fourth channel QSGMII port3 PCS access space

The address space allocation is fixed for 4 channels of SGMII and 4 channels of QSGMII respectively.

Chapter 4 Reference Design

4.1 Reference Function Design

The following figure shows the block diagram of the reference design provided. The 2.5G Ethernet system can verify the data transmitted and received through docking with third-party devices. The module functions are introduced as follows:

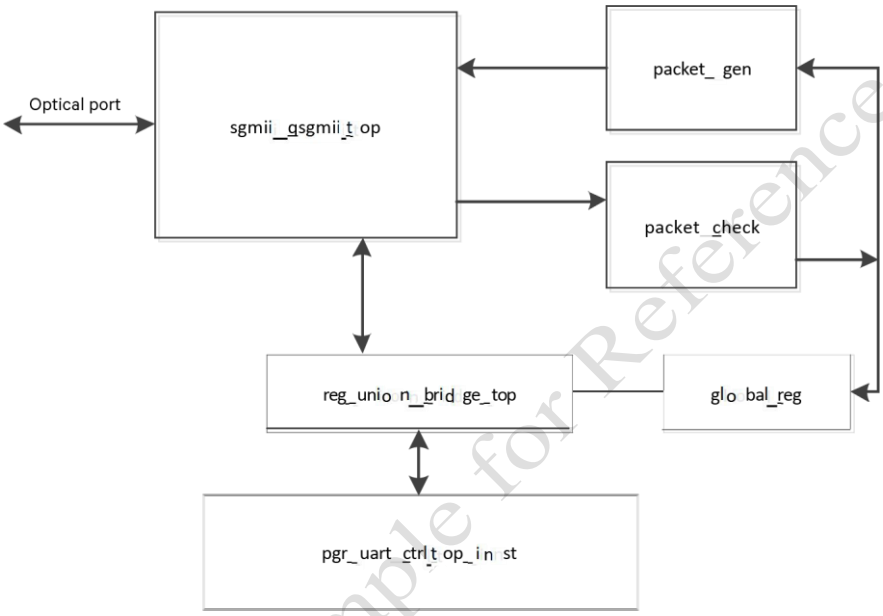

Figure 4-1 QSGMII and SGMII Mixed-use Design

packet_gen module

Generate data packets with random or fixed lengths based on configurations.

Sgmii_qsgmii_top module

QSGMII reference design

global_reg module

Global configuration register, configuring packet transmit modes, etc.

reg_union_bridge_top module

Register address space allocation

Table 4-1 Register Address Allocation

Addr[20]=1'b0	Access global register space
Addr[20]=1'b1	AccessHSST, SGMII PCS, QSGMII PCS register space

pgr_uart_ctrl_top_inst module

The serial port module, with a fixed baud rate of 115200, receives UART data and outputs data in the format required by the APB protocol during debugging. For read and write operations, the address width is 24 bits (higher 5 bits are 0), and the data width is 32 bits.

The format for read and write operations through UART is:

Read: 72 + address (byte-reversed)

Write: 77 + address (byte-reversed) + data (byte-reversed)

Example of serial port read and write:

Read the value of the configuration register at address 0x13 and change the value of this register to 1.

Read: 72130000

Write: 7713000001000000

The parameter configuration instructions for this reference design are illustrated by using the scenario of three instances of SGMII IP, with lane 0, lane 1 and lane 2 implemented The specific configuration parameters of SGMII mode are as follows:

```
sgmii_qsgmii_top #
(
.LANE0_PROTOCOL            ("SGMII"          ),  //SGMII、GE、 SGMII_GE、QSGMII、DISABLE
.LANE0_PLL                 ("PLL0"           ),  //PLL0、PLL1
.LANE0_CLK_SOURCE          ("Diff_REFCK0"    ),  //Diff_REFCK0  Diff_REFCK1
.LANE0_REF_CLK_FREQ        ("125.0"          ),  //125.0、156.25
.LANE0_BUFFER              ("TRUE"           ),  //"FALSE":DISABLE ELASTIC BUFFER "TRUE":ENABLE ELASTIC BUFFER
.LANE0_PHY_MODE            (1                ),  //1:PHY_MODE 0: MAC_MODE
.LANE0_AUTO_NEGOTIATION    ("TRUE"           ),  //"TRUE":AN ENABLE "FALSE": AN DISABLE
.LANE0_MDIO_ENABLE         ("FALSE"           ),  //"TRUE":MDIO ENABLE "FALSE": MDIO DISABLE
.LANE1_PROTOCOL            ("SGMII"          ),  //SGMII、GE、 SGMII_GE、QSGMII、DISABLE
.LANE1_PLL                 ("PLL0"           ),  //PLL0、PLL1
.LANE1_CLK_SOURCE          ("Diff_REFCK0"    ),  //Diff_REFCK0  Diff_REFCK1
.LANE1_REF_CLK_FREQ        ("125.0"          ),  //125.0、156.25
.LANE1_BUFFER              ("TRUE"           ),  //"FALSE":DISABLE ELASTIC BUFFER "TRUE":ENABLE ELASTIC BUFFER
.LANE1_PHY_MODE            (1                ),  //1:PHY_MODE 0: MAC_MODE
.LANE1_AUTO_NEGOTIATION    ("FALSE"           ),  //"TRUE":AN ENABLE "FALSE": AN DISABLE
.LANE1_MDIO_ENABLE         ("FALSE"           ),  //"TRUE":MDIO ENABLE "FALSE": MDIO DISABLE
.LANE2_PROTOCOL            ("SGMII"          ),  //SGMII、GE、 SGMII_GE、QSGMII、DISABLE
.LANE2_PLL                 ("PLL0"           ),  //PLL0、PLL1
.LANE2_CLK_SOURCE          ("Diff_REFCK0"    ),  //Diff_REFCK0  Diff_REFCK1
.LANE2_REF_CLK_FREQ        ("125.0"           ),  //125.0、156.25
.LANE2_BUFFER              ("TRUE"           ),  //"FALSE":DISABLE ELASTIC BUFFER "TRUE":ENABLE ELASTIC BUFFER
.LANE2_PHY_MODE            (1                ),  //1:PHY_MODE 0: MAC_MODE
.LANE2_AUTO_NEGOTIATION    ("TRUE"           ),  //"TRUE":AN ENABLE "FALSE": AN DISABLE
.LANE2_MDIO_ENABLE         ("FALSE"           ),  //"TRUE":MDIO ENABLE "FALSE": MDIO DISABLE
.LANE3_PROTOCOL            ("DISABLE"         ),  //SGMII、GE、 SGMII_GE、QSGMII、DISABLE
.LANE3_PLL                 ("PLL1"           ),  //PLL0、PLL1
.LANE3_CLK_SOURCE          ("Diff_REFCK1"    ),  //Diff_REFCK0  Diff_REFCK1
.LANE3_REF_CLK_FREQ        ("156.25"          ),  //125.0、156.25
.LANE3_BUFFER              ("TRUE"           ),  //"FALSE":DISABLE ELASTIC BUFFER "TRUE":ENABLE ELASTIC BUFFER
.LANE3_PHY_MODE            (0                ),  //1:PHY_MODE 0: MAC_MODE
.LANE3_AUTO_NEGOTIATION    ("TRUE"           ),  //"TRUE":AN ENABLE "FALSE": AN DISABLE
.LANE3_MDIO_ENABLE         ("FALSE"           )   //"TRUE":MDIO ENABLE "FALSE": MDIO DISABLE
)sgmii_qsgmii_top_inst
```

Figure 4-2 Examples of Parameter Configuration

4.2 Reference Design Interface List

Table 4-2 List of Interfaces

Signal Name	I/O	Bit width	Description
Global signals			
i_free_clk	Input	1	External clock input, with a frequency of 50MHz
sys_rst	Input	1	System reset interface, reset at a high level
HSSTHP-end signal			
ref_clk0_n	Input	1	HSSTHP differential reference clock negative end, 125 Mhz or 156M
ref_clk0_p	Input	1	HSSTHP differential reference clock positive end, 125 Mhz or 156M
ref_clk1_n	Input	1	HSSTHP differential reference clock negative end, 125 Mhz or 156M
ref_clk1_p	Input	1	HSSTHP differential reference clock positive end, 125 Mhz or 156M
rxn0	Input	1	HSSTHP differential data input negative end
rxp0	Input	1	HSSTHP differential data input positive end
txn0	Output	1	HSSTHP differential data output negative end
txp0	Output	1	HSSTHP differential data output positive end
rxn1	Input	1	HSSTHP differential data input negative end
rxp1	Input	1	HSSTHP differential data input positive end
txn1	Output	1	HSSTHP differential data output negative end
txp1	Output	1	HSSTHP differential data output positive end

Signal Name	I/O	Bit width	Description
rxn2	Input	1	HSSTHP differential data input negative end
rxp2	Input	1	HSSTHP differential data input positive end
txn2	Output	1	HSSTHP differential data output negative end
txp2	Output	1	HSSTHP differential data output positive end
rxn3	Input	1	HSSTHP differential data input negative end
rxp3	Input	1	HSSTHP differential data input positive end
txn3	Output	1	HSSTHP differential data output negative end
txp3	Output	1	HSSTHP differential data output positive end
Status signals			
led1	Output	1	Test signals
led2	Output	1	Test signals
SFP_TX_DISABLE	Output	4	Optical module enable signal
Serial port signals			
txd	Output	1	Serial port transmit
rxd	Input	1	Serial port receive

4.3 Reference Design File Directory

Design Example Directory Structure Diagram:

```
├─docs                          //Application guide
├─pnr                           //Project directory
|  ├─sgmii_qsgmii.fdc           //Constraint file
|  ├─sgmii_qsgmii_demo.pds      //Project file
├─source                        //Source file directory
|  ├─sgmii_qsgmii_top_demo.v    //Test project top level
|  ├─sgmii_qsgmii_top.v         //Reference design top-level
|  ├─global_reg.v               //Test project global register file
|  ├─reg_union_bridge_top.v     //Test project address allocation file
|  ├─apb_addr_divide.v          //Reference design register address allocation module
|  ├─clk_cal.v                  //Frequency test module
|  ├─ipm2l_hsstlp
|  |  ├─rtl                     //hsstlp IP folder (contains encrypted source code)
|  ├─qsgmii
|  |  ├─rtl                     //qsgmii IP folder (contains encrypted PCS source code)
|  ├─sgmii
|  |  ├─rtl                     //sgmii IP folder (contains encrypted PCS source code)
|  ├─uart_ctrl_32bit            //Serial port to APB interface code
|  ├─pkg_gen                    //Message generation and detection code
|  ├─sim_lib                    Simulation Library Files
├─sim                           // Simulation scripts
├─testbench                     Simulation Stimulus Files
```

Figure 4-3 File Directory

4.4 Reference Design Simulation

The current simulation file is configured with 3SGMII mode, i.e., Lane 0, Lane 1 and Lane2 are in SGMII mode. In each lane, HSST differential interface independent loopback is configured to 1000M mode.

After setting up the simulation environment, open the "sim" directory to run the "sim.bat" script. For detailed simulation steps, refer to sgmii ip or qsgmiiip simulation description.

4.5 Reference Design On-board Verification

On-board verification uses the P04I50KF01_A0board in conjunction with the 390H QSGMII IP and SGMII IP for interconnection testing, enabling two single boards to interconnect through optical fibre. The 50H demo board sends random or fixed packet lengths, 390H loopback is read to the 50H demo board. Send/receive MAC statistics to check for consistency and CRC errors.

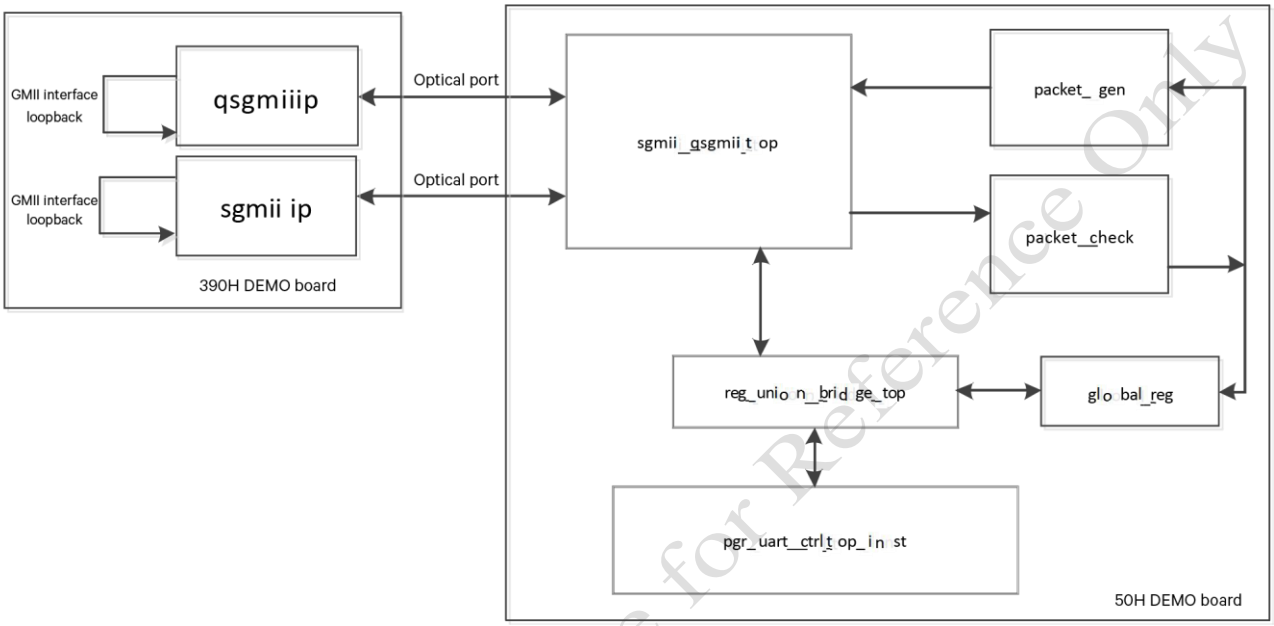

Figure 4-4 Reference Design On-board Verification

Chapter 5 Appendix

Table 5-1 Key Configuration Information for Common Modes

Mode	Key Parameter Configuration	GMII channel
2sgmii+2qsgmii	.LANE0_PROTOCOL ("SGMII"), .LANE0_PLL ("PLL0"), .LANE0_CLK_SOURCE .LANE0_REF_CLK_FREQ ("Diff_REFCK0"), ("125.0"), .LANE1_PROTOCOL ("SGMII"), .LANE1_PLL ("PLL0"), .LANE1_CLK_SOURCE .LANE1_REF_CLK_FREQ ("Diff_REFCK0"), ("125.0"), .LANE2_PROTOCOL ("QSGMII"), .LANE2_PLL ("PLL1"), .LANE2_CLK_SOURCE .LANE2_REF_CLK_FREQ ("Diff_REFCK1"), ("156.25"), .LANE3_PROTOCOL ("QSGMII"), .LANE3_PLL ("PLL1"), .LANE3_CLK_SOURCE ("Diff_REFCK1"), .LANE3_REF_CLK_FREQ ("156.25"),	SGMII: Using GMII data from CH0 and CH1 SGMII channels . QSGMII: Using GMII data from CH0 and CH1 QSGMII channels .
4qsgmii	.LANE0_PROTOCOL ("QSGMII"), .LANE0_PLL ("PLL0"), .LANE0_CLK_SOURCE .LANE0_REF_CLK_FREQ ("Diff_REFCK0"), ("156.25"), .LANE1_PROTOCOL ("QSGMII"), .LANE1_PLL ("PLL0"), .LANE1_CLK_SOURCE .LANE1_REF_CLK_FREQ ("Diff_REFCK0"), ("156.25"), .LANE2_PROTOCOL ("QSGMII"), .LANE2_PLL ("PLL0"), .LANE2_CLK_SOURCE .LANE2_REF_CLK_FREQ ("Diff_REFCK0"), ("156.25"), .LANE3_PROTOCOL ("QSGMII"), .LANE3_PLL ("PLL0"), .LANE3_CLK_SOURCE ("Diff_REFCK0"), .LANE3_REF_CLK_FREQ ("156.25"), Note: PLLcan also usePLL1 and CLK_SOURCE Diff_REFCK1	Using GMII data from CH0, CH1, CH2andCH3 QSGMII channels .
2qsgmii (Lane0 and Lane1)	LANE0_PROTOCOL ("QSGMII"), .LANE0_PLL ("PLL0"), .LANE0_CLK_SOURCE .LANE0_REF_CLK_FREQ ("Diff_REFCK0"), ("156.25"), .LANE1_PROTOCOL ("QSGMII"), .LANE1_PLL ("PLL0"), .LANE1_CLK_SOURCE ("Diff_REFCK0"), .LANE1_REF_CLK_FREQ ("156.25"), Note: PLLcan also usePLL1 and CLK_SOURCE Diff_REFCK1	Using GMII data from CH0 and CH1 QSGMII channels.

Mode	Key Parameter Configuration		GMII channel
3sgmii (Lane0 , Lane1 and Lane2)	.LANE0_PROTOCOL .LANE0_PLL .LANE0_CLK_SOURCE .LANE0_REF_CLK_FREQ .LANE1_PROTOCOL .LANE1_PLL .LANE1_CLK_SOURCE .LANE1_REF_CLK_FREQ .LANE2_PROTOCOL .LANE2_PLL .LANE2_CLK_SOURCE .LANE2_REF_CLK_FREQ	("SGMII"), ("PLL0"), ("Diff_REFCK0"), ("125.0"), ("SGMII"), ("PLL0"), ("Diff_REFCK0"), ("125.0"), ("SGMII"), ("PLL0"), ("Diff_REFCK0"), ("125.0"),	SGMII: Using GMII data from CH0, CH1 and CH2 SGMII channels.

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