Logos Family PCB Design

User Guide

(UG020012, V1.4)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.4	21.06.2022	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
PCB	Printed Circuit Board
BGA	Ball Grid Array
DDR	Double Data Rate
HSST	High Speed Serial Transceiver
LVDS	Low-Voltage Differential Signaling
PCIe	Peripheral Component Interconnect Express
SPI	Serial Peripheral Interface
JTAG	Joint Test Action Group
MIPI	Mobile Industry Processor Interface
C/A	Command/address

Related Documentation

The following documentation is related to this manual:

1. ***DS02001_Logos Family FPGAs Datasheet***
2. ***UG020005_Logos Family FPGAs Configuration User Guide***
3. ***UG020009_Logos Family FPGAs Analog-to-Digital Converter (ADC) User Guide***
4. ***UG020013_Logos Family FPGAs High-Speed Serial Transceiver (HSST) User Guide***
5. ***AN02023_PGL100H-FBG900 Configuration Multiplexing PIN Application Guide***

Table of Contents

Tables

Figures

Chapter 1 Overview

The Logos Family PCB Design User Guide is the instruction for recommended PCB design for Logos Family FPGA chips. After FPGA pins are assigned, it is recommended that users use PDS software to confirm pin assignments.

For details of product features, resource scale, packaging information, and number of user IOs for Logos Family FPGA, please refer to the "DS02001_Logos Family FPGAs Datasheet".

Chapter 2 Packaging and Fanout

The BGA pad diameter is generally designed to be the same as the FPGA ball diameter, and can be 20%-25% smaller than the FPGA ball diameter in special cases. Below is a reference diagram for Fanout.

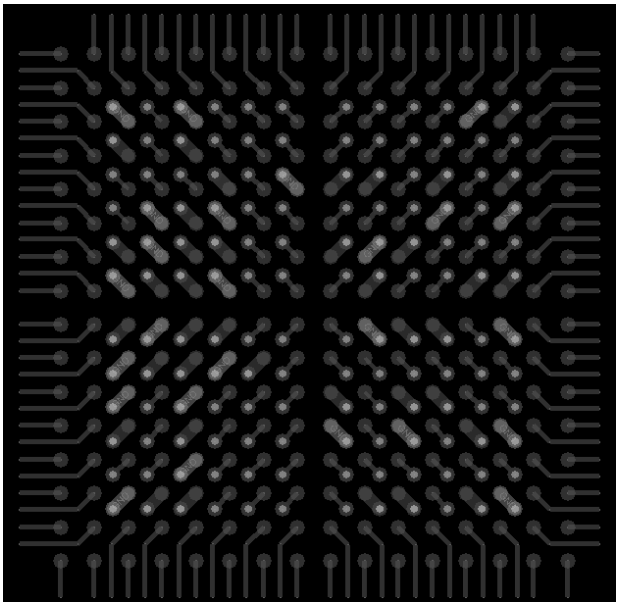


Figure 2-1 BGA Fanout Reference Diagram

As shown in Figure 2-1, the central "cross" divides the BGA into four equal regions, with the fanout trace in each region extending outward from the BGA. The position of the "cross" can be asymmetrically adjusted as required for fanout. The "cross" can be used in the middle layers for power trace and trace with larger trace spacing, and in the bottom layer for placing decoupling capacitors. The two outermost rows of pads can be routed directly from the chip soldering surface, while the inner rows of pads should be routed outward in a radial pattern after layer change through via. The power supply and ground signal traces should be widened as much as possible.
Avoid long traces between surface pads to prevent PCB processing defects and poor soldering, as shown in Figure 2-2.

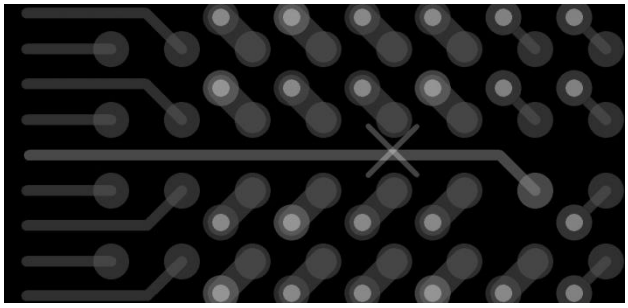


Figure 2-2 Diagram of Long Traces Between BGA Surface Pads

2.1 FBG

The Logos Family FPGAs currently have three types of FBG packaging: FBG256, FBG484, and FBG900. For specific packaging information, please refer to the packaging manuals.

The recommended pad, via sizes, and trace widths for FBG packaging are as follows:

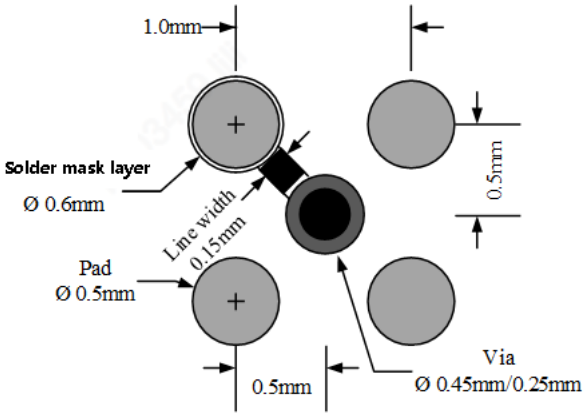


Figure 2-3 Diagram of FBG Packaging Pad and Via Sizes

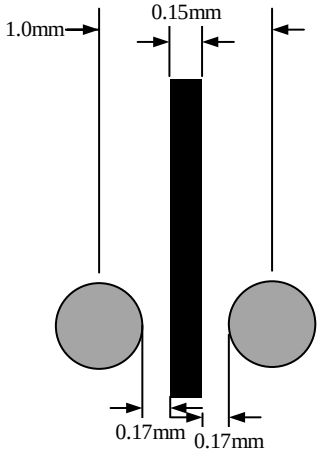


Figure 2-4 Diagram of Trace Sizes Between FBG Packaging Pads

2.2 MBG

The Logos Family FPGAs currently have one type of MBG packaging: MBG324. For specific packaging information, please refer to the packaging manual.

The recommended pad and via sizes, and trace widths for MBG packaging are as follows:

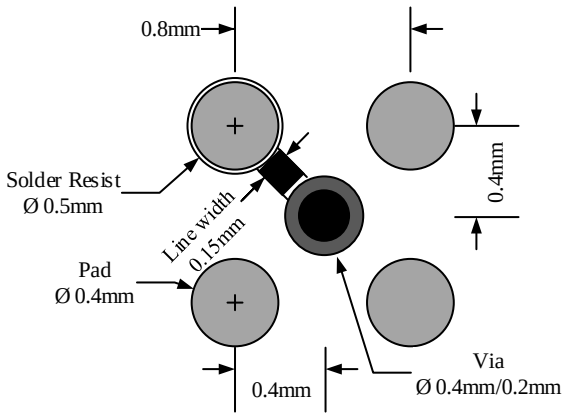


Figure 2-5 Diagram of MBG Packaging Pad and Via Sizes

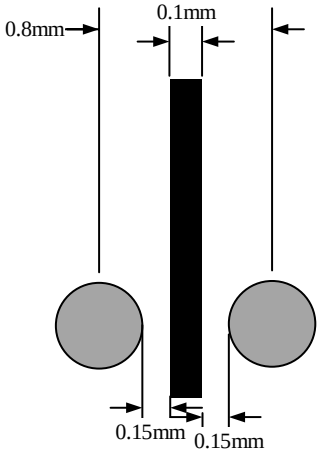


Figure 2-6 Diagram of Trace Sizes Between MBG Packaging Pads

2.3 LPG

The Logos Family FPGAs currently have two types of LPG packaging. For specific packaging information, please refer to the packaging manuals.

LPG packaging is in the form of Quad Flat Package (QFP), with PCB packaging and trace designed according to QFP requirements.

There is a EPAFD in the PGL22GS_LPG176 chip package with all VSS pins of the chip. PCB shall be designed in such a way that the EPAD is connected to GND over a large area.

Chapter 3 Configuration

The configuration modes supported by the Logos Family FPGAs are as shown in Table 3-1. For detailed configuration descriptions, please refer to the "***UG020005_Logos Family FPGAs Configuration User Guide***".

Table 3-1 Logos Family FPGAs Configuration Modes

S. No.	Configuration Mode	bit width	Support Information							CFG_CLK Direction
			PGL12G		PGL22G		PGL22GS	PGL25G/50G/50H	PGL100H	
			LPG144	FBG256	FBG256	MBG324	LPG176	ALL	ALL	
1	JTAG	1	√	√	√	√	√	√	√	Input (TCK)
2	Master SPI	1	√	√	√	√	√(1)	√	√	Output
		2								
		4								
		8						×	×	
3	Master BPI	8 (Asynchronous)	×	×	×	√	×	×	√	Output
		16 (Asynchronous)								
		16 (Synchronous)							×	
4	Slave SPI	1	√	√	√	√	×	×	×	Input
5	Slave Parallel	8	√	√	√	√	×	√	√	Input
		16	×							
		32			×			×	×	
6	Slave Serial	1	√	√	√	√	×	√	√	Input

Note: The master SPI mode of PGL22GS does not support serial daisy chain.

Please note that the requirements of configuration pin for PGL25G/PGL50G/PGL50H/PGL100H are different from those for PGL22G/PGL12G, and the differences of configuration pins are explained in the document UG020005.

For PGL25G/PGL50G/PGL50H/PGL100H chips, VCCAUX includes the configuration voltage. T The VCCAUX voltage of the PGL25G device supports only 3.3V, so the JTAG voltage can only be 3.3V. However, the VCCAUX voltage of PGL50G/PGL50H/PGL100H devices supports both 3.3V and 2.5V, so the JTAG voltage can be 3.3V and 2.5V.

For other configuration modes, refer to section "2 Configuration Mode Description" of document "***UG020005_Logos Family FPGAs Configuration User Guide***" for detailed information to configure the power domain of the configured interface.

When using configuration pins, ensure that the voltage of the BANK where the configuration interface signal is located matches the interface voltage of the configuration flash.

3.1 Description of Configuration Pin

For the description of configuration pins of the Logos Family FPGAs, please refer to the pin descriptions in the document "***UG020005_Logos Family FPGAs Configuration User Guide***" and the PK02xxx Package Manual. Note the differences in configuration pins between PGL12G/PGL22G devices and PGL25G/PGL50G/PGL50H/PGL100H devices, and verify them carefully during schematic design.

3.2 JTAG

JTAG configuration is one of the most universal basic configuration modes of FPGA. When applying JTAG daisy-chain configuration, the TCK and TMS signals connect to all devices on the configuration chain. At this moment, Signal bifurcation branch is equivalent to stub lines, and it is recommended to use a multiple drive buffer to ensure high-speed use of JTAG. In Figure 3-1, the resistance value of the series resistor R at driver side should be based on debugging, with 33Ω typically recommended.

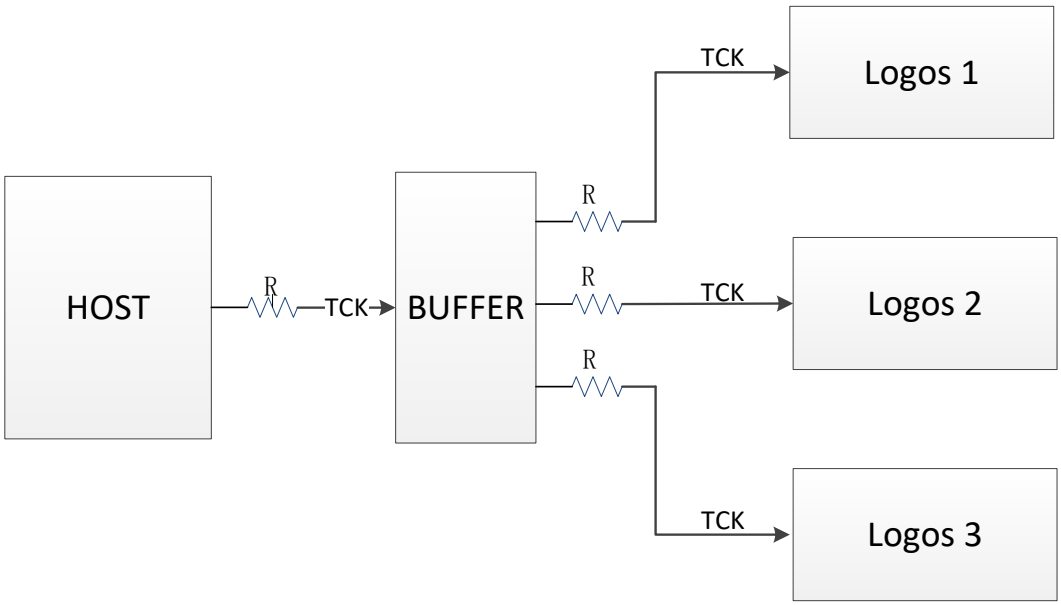


Figure 3-1 JTAG Cascading Application Diagram

3.3 SPI

When PGL12G/PGL22G devices use the Master SPI x8 configuration mode, two SPI FLASH chips

are needed to meet the bit width requirements. At this time, the CFG_CLK signal will drive both FLASH chips. To ensure the quality of the CFG_CLK signal, it is recommended to use a clock Buffer or to connect a small resistor in series at the clock branch point and shorten the branch length.

3.4 Configurable Multiplexed PIN

When using the configuration multiplexing pin as user IO for PGL25G/PGL50G/PGL50H/PGL100H devices, please refer to the "Configuration Multiplexing PIN Application Guide" for the corresponding device, such as "***AN02023_PGL100H-FBG900 Configuration Multiplexing PIN Application Guide***".

3.5 Other Configuration Pins

Other common configuration pins include MODE [2:0], RST_N, INIT_FLAG_N, and CFG_DONE, among others.

For PGL12G/PGL22G devices, the configuration mode is determined by the external pull-up or pull-down of the MODE [2:0] signal pins. For PGL25G/PGL50G/PGL50H/PGL100H devices, the configuration mode is determined by the external pull-up or pull-down of the MODE[1:0] signal pins.

RST_N is an active-low reset signal. There are generally three types of external connection circuits as shown in Figure 3-2, and users can select the appropriate circuit according to actual needs. In Figure 3-2 a, only an external pull-up resistor is connected, allowing the chip to reset automatically upon power-up. In Figure 3-2 b, a capacitor is added to form a power-up RC delay reset. In Figure 3-2 c, a button is added in the circuit to reset the chip when needed. Please refer to "2 Configuration Mode Description" in document UG020005 to determine the value of R, and calculate the value of C according to the required delay time.

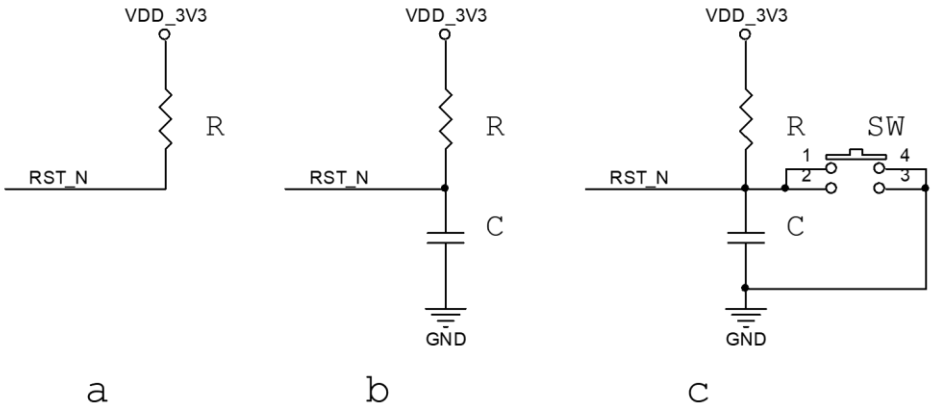


Figure 3-2 RST_N Circuit Diagram

Before sampling pins MODE [2:0], INIT_FLAG_N is an input, and configuration can be delayed by keeping it at a low level. After sampling the MODE [2:0] pins, INIT_FLAG_N is an open-drain output, indicating whether there is an error in the configuration process. When there is no need to indicate the configuration process, only one external pull-up resistor is connected to INIT_FLAG_N. When an LED is required to indicate the configuration process, it is recommended to design the circuit according to Figure 3-3, with diode D preventing the LED from pulling down the INIT_FLAG_N voltage. Please refer to "2 Configuration Mode Description" in document "***UG020005_Logos Family FPGAs Configuration User Guide***" to determine the value of R1 in the diagram, and calculate the value of R2 based on the LED's driving current.

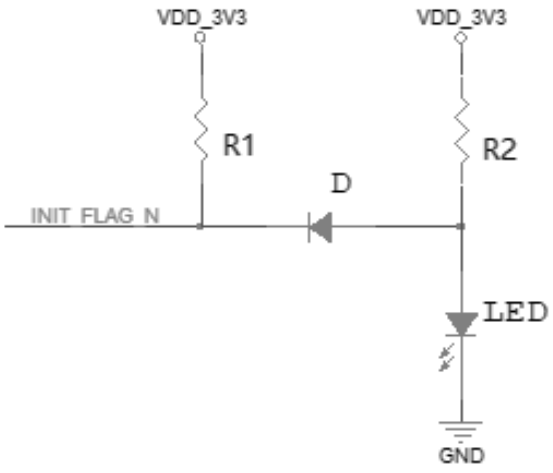


Figure 3-3 Circuit Diagram for INIT_FLAG_N Indicating the Configuration Process

CFG_DONE is used to indicate configuration completion. Refer to the above INIT_FLAG_N for external circuits.

When multiplexing pins are used as general IO, it is necessary to ensure that they are not affected by circuits other than the configuration circuit during power-up configuration, and it is recommended to use them only for low-speed signal output.

3.6 REXT Signal

REXT is a dedicated pin for external high-precision resistors unique to PGL12G and PGL22G; PGL25G/PGL50G/PGL50H/PGL100H do not have this pin. The REXT pin connects an external 10K resistor with 1% precision to ground. As shown in Figure 3-4, the chip is on the TOP side of the PCB, and the resistor is on the BOTTOM side. The resistor is placed near the REXT via to minimize the trace length between the two ends.

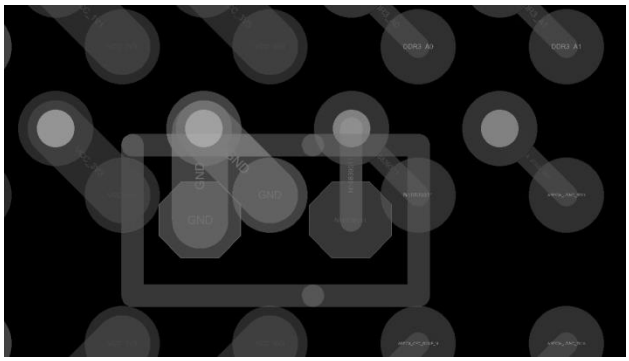


Figure 3-4 Schematic of REXT External Resistor

Chapter 4 Power

4.1 Voltage

For the operating conditions, absolute voltage limits, and recommended operating voltage of Logos Family devices, please refer to "***DS02001_Logos Family FPGAs Datasheet***".

In general applications, VCCAUX, VCCAUX_A, VCCEFUSE, VCCIOCFG, and the 3.3V VCCIO power supply are merged into a single 3.3V power supply for PGL12G/PGL22G devices.

For PGL25G/PGL50G/PGL50H/PGL100H devices, VCCAUX can be merged with other 3.3V VCCIO power supplies into a single 3.3V power supply.

PGL12G/PGL22G/PGL50G/PGL50H/PGL100H support the EFUSE function. During the EFUSE programming process, the VCCEFUSE pin must be connected to a 3.3V power supply; EFUSE programming shall be powered up in the recommended sequence. After EFUSE programming is complete, VCCEFUSE can maintain a 3.3V voltage or be grounded after powering down in the required sequence; it must not be left floating; if the user does not program EFUSE, the VCCEFUSE pin should be grounded.

4.2 Power-up/Power-down Sequence

For the recommended power-up and power-down sequence and power supply ramp rates, please refer to Section "2.5 Recommended Power-up/Power-down Sequence" in the "***DS02001_Logos Family FPGAs Datasheet***".

4.3 Power-Rail Current

Users can estimate the chip's power consumption based on the actual operating junction temperature and resource utilization using the power estimation tool (Pango Power Planner) in the PDS development environment, and design with a certain margin based on the estimation.

4.4 Recommended Number and Parameters of Decoupling Capacitors

The recommended number of capacitors and reference parameters for medium-scale devices such as PGL50G/PGL50H/PGL100H are as follows. Users can adjust the number and parameters of capacitors according to actual conditions and, if necessary, evaluate through PI simulation. For PGL12G/PGL22G/PGL25G devices, users should evaluate based on resource and IO utilization. For the number of decoupling capacitors for HSST, please refer to the HSST section.

Table4-1 Number of Decoupling Capacitors for PGL50G/PGL50H_FBG484

Power Supply	**100uF**	**4.7uF**	**470nF**	**Description**
VCC	1	1	2	Core logic power supply
VCCAUX	1	2	4	Auxiliary power supply
VCCIO	1	1	4	Bank power supply

Table4-2 Number of Decoupling Capacitors for PGL100H_FBG900

Power Supply	**100uF**	**4.7uF**	**470nF**	**Description**
VCC	1	2	4	Core logic power supply
VCCAUX	2	3	6	Auxiliary power supply
VCCIO	1	1	4	Bank power supply

Table4-3 Recommended Capacitor Parameters

Parameter	**100uF**	**4.7uF**	**470nF**
Package	1210	0805	0402
Tolerance	6.3	6.3	6.3
ESL	5nH	2nH	1.5nH
ESR	10 mΩ<ESR<60 mΩ	10 mΩ<ESR<60 mΩ	10 mΩ<ESR<60 mΩ
Type	MLCC (X7R)	MLCC (X7R)	MLCC (X7R)

4.5 Power Trace

Power cord and ground wires should be short and thick; it is recommended to connect the power supply in a plane to reduce the inductance of the power path.

4.6 Decoupling Capacitor Placement Recommendation

For large packages including 1210, D-type and 7343-type, due to their large size, they cannot be placed close to the FPGA pins. However, the low-frequency decoupling provided by the large-capacity capacitors is not sensitive to their location. They can be located farther away but still as close to the FPGA as possible. It is recommended to use a large area of copper foil for connections and increase the number of vias to reduce loop inductance. Capacitors in 0805, 0603, and smaller packages are used for mid-to-high frequency decoupling, which is sensitive to their location. It is recommended to place them as close as possible to the FPGA power pins. Wide and short leads can be connected to power supply and ground vias in any way of the figures (2), (3), or (4) as shown in Figure 4-1. Avoid using long or thin leads as shown in figure (1), as this would increase parasitic inductance and impair decoupling capability.

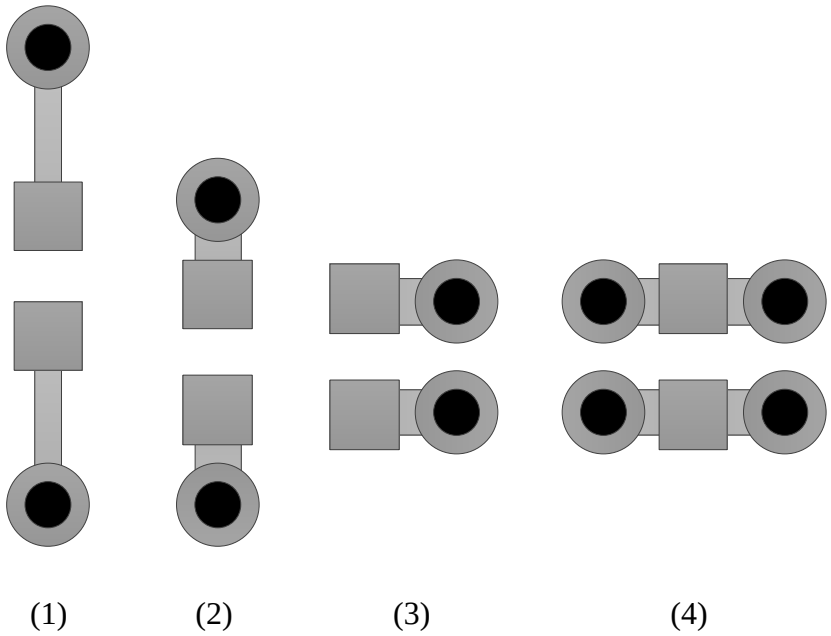


Figure 4-1 Decoupling Capacitor Placement Diagram

Chapter 5 ADC

PGL22G and PGL12G contain an ADC module inside, while
PGL25G/PGL50G/PGL50H/PGL100H do not contain.

VA0 and VA1 are dedicated analog input pins and cannot be used as GPIO. When not using the chip's ADC, these two pins should be left floating.

The ADC requires a 2.5V reference voltage, which can be provided internally by the chip or externally through the chip's VREF_EXT pin. It is recommended to use an external reference voltage with an LDO power supply. When using the internal reference voltage or not using the chip's ADC, the VREF_EXT pin should be left floating.

The specific use of the ADC is detailed in the "***UG020009_Logos Family FPGAs Analog-to-Digital Converter (ADC) User Guide***".

Chapter 6 DDR3

6.1 DDR3 Interface Signal Description

Table6-1 DDR3 Interface Signal Description

Signal Name	Description
Clock Signal	
CLK_P, CLK_N	DDR differential clock signal
Address and Command Signals	
DDR_A[15:0]	Address signal
BA[2:0]	Bank address signal
RAS_n	Row address strobe
CAS_n	Column address strobe
WE_n	Write enable
Control Signals	
CKE	Clock enable
CS	Chip select signal
ODT	On-chip terminal enable signal
REST_n	Reset signal
Data Signals	
DQ	Data Signals
DQS_P, DQS_N	Differential data strobe
DM	Data mask
Other Signals	
ZQ	External calibration resistor, connect 240ohm resistor to ground

6.2 Schematic Design Guide for DDR3 Application of PGL22G Device

The PGL22G-FBG256 and PGL22G-MBG324 packaged FPGA chips have two HMEMCs (One is on the left side of the chip and the other is on the right side of the chip). For the connection between DDR memory and FPGA, DQ pins can be swapped within each group (8 bits form a group, such as DQ0-DQ7 as a group), while other pins must strictly correspond to the "Memory byte Group" column in the "Ball name list" of the corresponding Packaging_and_Pinout User Guide.

After routing DQSU_GATE_OUT outside the chip, it connects to DQSU_GATE_IN, and the routing length should be approximately equal to the sum of the CK trace length and the DQS trace length. DQSL_GATE_OUT and DQSL_GATE_IN should be treated similarly. (Not required; the device can be used with these four pins left floating).

Add weak pull-down resistors to the FPGA pins DQSU_P and DQSL_P, and weak pull-up resistors to the FPGA pins DQSU_N and DQSL_N, with resistance values between 500-1000ohm. The voltage applied to the pull-up resistors should match the voltage of the DDR memory, for example, 1.5V for DDR3. (Not required, used to improve signal quality).

6.3 PGL12G Device DDR3 Application Device Schematic Design Guide

The PGL12G_FBG256 chip has 4 Banks: L0, L1, R0, and R1, with each containing external memory interface pins and being divided into 3 groups. For example, DQ0_L0 belongs to group0 of Bank L0, and can be connected to the DQ signal pins of external DDR3; DQS0_L0 and DQS0#_L0 also belong to group0 of Bank L0, and can be connected to DQS/DQS# signal pins of external DDR3. When a group is used for address command signal pin assignment, the "DQ, DQS, DQS#" within the group are allocated as pins for address command signals. There are FPGA configuration signals on Bank L0; if L0 is connected to external DDR3, pay attention to the signal levels. For detailed grouping information, please refer to ***"PK0203_PGL12G_FBG256"***.

Table6-2 represents the DDR3 control signal grouping and its correspondence with groups; signals within the same group can be swapped, but signals from different groups cannot be swapped.

The reference clock needs to be connected to the BANK used for DDR pin assignment.

Table6-2 DDR3 C/A Signal Grouping and Its Correspondence with Group

Group	**Signals**
Group0	A0~A7
Group1	A8~A14, CKE
Group2	BA0~BA2, CS_N, WE_N, RAS_N, ODT, CAS_N, CK, CK_N

For the Bank connecting to external DDR3 data, the VREF pins require an externally connected reference voltage. Every 8 bits of data, the corresponding DM and DQS/DQS# are within one group; DQ and DM within the same group can be swapped, but DQS/DQS# cannot be swapped.

6.4 PGL25G/PGL50G/PGL50H/PGL100H Application Schematic Design Guide

To meet the DDR3 interface I/O standards, a VREF reference voltage input is provided to the used DDR interface Bank, with the VREF voltage standard being 0.5 times the VCCIO. The VREF power can be generated using a dedicated chip or through resistor voltage division; it is recommended to use a dedicated chip. When adopting resistor voltage division, pay attention to power filtering, resistor precision, and resistance value, and it is suggested to use a 1K resistor with

a precision of 1%. For the PGL100H device, each IO Bank has multiple VREF pins, and when used for DDR pin assignment, all VREF pins within the Bank need a reference voltage input.

The PGL25G/PGL50G/PGL50H/PGL100H chip supports up to 32-bit width DDR3 for a single Bank and does not support cross-Bank DDR3 pin assignment. Banks that support DDR3 interface have multiple byte groups, each with a pair of dedicated DQS signal pins. For pin numbers and byte groupings, please refer to the Pin name list in the packaging Manual. Pins with a blank DQS grouping column in the Pin name list cannot be used for DDR3 interface signals.

DQS signals must be connected to the designated DQS pins, and DQ and DM must be connected to the corresponding byte group pins. Command/address signals must be connected to pins that are not used for data grouping. The DDR3 CLK signal must be connected to the P-N pair pins of a command/address byte group. RESET_N can be connected to any pin, preferably constrained to the Bank where the DDR interface is located. No termination is required but it must be pulled down to GND through a 4.7K ohm resistor. Reserve a 1nF capacitance to ground. Signals within the DQ byte group can be freely swapped (except for specific DQS pins), and byte groups within the Bank can be swapped as a whole.

The reference clock input pins for the DDR system must be selected from the Bank where the DDR interface is located or an adjacent Bank, and a global clock input pin must be used. Cross-Bank inputs result in longer internal routing and can introduce additional jitter. When the system clock selects a differential signal and does not match the Bank voltage, please use the circuit in form of AC coupling + DC bias, and the bias voltage should match the I/O Standard constrained by the clock pins.

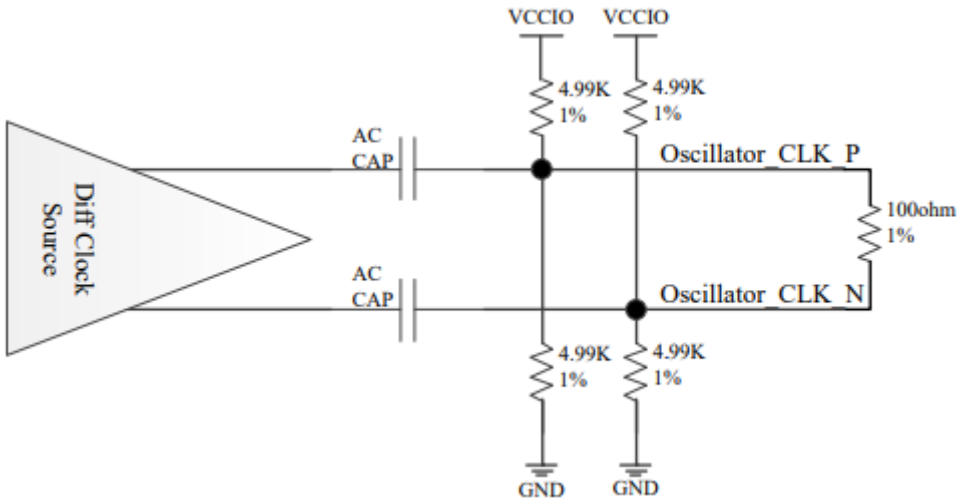


Figure 6-1 Reference clock input pins for the DDR

6.5 DDR3 PCB Design Requirements for PGL12G/PGL22G Devices

Each Hard Core or Soft Core of the Logos Family PGL12G and PGL22G devices supports a maximum of one 16-bit DDR3 chip, therefore multi-chip topology is not considered here.

Strictly controlling the equal length of DDR3 signal traces ensures sufficient setup and hold time for the signals. The following points should be noted:

- Signals can be divided into two categories: data (DQ, DQS, DM) and other command/address signals (command, address, control, CK);
- Data is divided into two groups: lower 8 bits and upper 8 bits, with intra-group equal length error constrained within 20mil, where DQS_P and DQS_N have an equal length error within 5mil, and the signal length difference between groups is within 100mil;
- Use the CK as a reference for address and control signals, with error constrained within 100mil, and the equal length error between CK differential pairs within 5mil;
- The trace length of CK should be slightly greater than that of DQS to ensure that the time difference between the arrival of the CK and DQS signals at the DDR memory is within one clock cycle. The difference in trace length between the CK and DQS should be within 250mil to ensure longer setup and hold time;
- Pin delay information of the FPGA chip must be added during delay tuning;
- Signals in the same group should be routed on the same layer to avoid signal skew being affected by changing layers. If layer change is necessary, maintain equal length before and after the change, try to avoid surface layer trace, and limit to no more than 2 vias per signal;
- For the delay tuning trace, route single ended trace at 3W spacing (where W is the wire width) and differential trace at 5W spacing. Ensure that the spacing within each signal group is not less than 3H (where H is the distance from the trace to the main reference plane), the spacing between groups is not less than 5H spacing, and the distance from DQS and CK to other signals is greater than 5H spacing;
- All signal traces must have a complete reference ground plane.
- Another key aspect of DDR3 trace design is power supply. DDR3 has three types of power supplies: VDD, VTT, and VREF:
- The VDD is the core power supply for DDR3 chips, with scattered pins, requiring a dedicated area in the power plane and a certain number of capacitors. 0.1μF capacitors shall be placed close to the chip pins, and use the smallest possible package;
- The VTT power supply has high precision requirements and significant instantaneous current, necessitating the use of numerous decoupling capacitors. The width of the VTT power supply copper connecting the termination resistor should be greater than 120mil;

- The VREF power supply requires high precision, but carries a small current, so it does not need very wide traces, and needs less decoupling capacitors. VREF needs to be kept away from sources of interference.

6.6 DDR3 PCB Design Requirements of PGL25G/PGL50G/PGL50H/PGL100H Device

The Logos Family FPGA PGL25G, PGL50G, PGL50H, and PGL100H devices support a DDR Soft Core with up to 32-bit width. Take the typical Flyby topology as an example below.

- During PCB design, it is necessary to include Pin Delay information and activate it during routing, as well as the via delay.
- For Flyby topology, the CK trace length should not be shorter than the DQS trace of the first group, and the trace delay difference should not exceed 1/4 CK cycle. For topologies other than Flyby, the CLK trace delay from the FPGA to each DRAM die must be greater than the DQS trace delay, and the delay difference should be less than 1/4 CK cycle;
- The CK differential pair's P-N Skew should be less than 5mil, with a control impedance difference of 100ohm ±10%. A complete reference GND layer is required, with minimized layer changes, and symmetric accompanying GND vias should be added where vias are used to change layers.
- In Flyby topology, the delay of the command/address signal from each DDR3 chip to the FPGA relative to the CK signal is constrained, with the CK trunk trace (FPGA to frist DDR chip) less than 2000mil, and branch trace (Flyby to DDR chip) less than 120mil.
- Use the CK as a reference for address and control signals, with error constrained within 200mil.
- Command/address signals require a complete reference layer, with GND accompanying vias for ODT, CS, CKE vias, and at least one GND via next to every 3-6 signal vias for other signals.
- The DQS differential pair's P-N Skew should be less than 5mil, with a control impedance difference of 100ohm. A complete reference GND layer is required with no more than twice layer changes, and symmetric accompanying GND vias should be added where vias are used to change layers.
- DQ signals require a complete reference layer, with at least one GND via accompanying every 2-4 signal vias.
- Within the same DQS byte group, the DQ trace length difference is constrained to be less than 50mil based on DQS, with a total length constrained within 1500mil.
- Traces for different DQS byte groups can be designed in unequal lengths of 200-300mil to reduce SSN impact; for example, groups 0 and 2 are of standard length, while groups 1 and 3 are 200mil longer in trace.

- Signals in the same group should be routed on the same layer to avoid signal skew being affected by changing layers. If layer changes are necessary, ensure the traces before and after the change are equal in length and try to avoid surface layer trace;
- For the delay tuning trace, route single ended trace at 3W spacing (where W is the wire width) and differential trace at 5W spacing. Ensure that the spacing within each signal group is not less than 3H spacing (where H is the distance from the trace to the main reference plane), the spacing between groups is not less than 5H spacing, and the distance from DQS and CK to other signals is greater than 5H spacing;
- The power supply should have a complete power plane, with a target impedance constrained within 0.01ohm@100M.
- Decoupling capacitors should be placed as close as possible beneath the BGA Ball, ensuring that there is at least one filtering capacitor beneath each power pin is connected to ground.
- The VTT power supply has high precision requirements and significant instantaneous current, necessitating the use of sufficient decoupling capacitors. The width of the VTT power supply copper connecting the termination resistor should be greater than 120mil;
- The VREF power supply requires high precision, but carries a small current, thus requiring less decoupling capacitors. VREF needs to be kept away from sources of interference;
- 240ohm resistors with 1% precision are used as ZQ calibration resistors and should be placed close to the pins use, with widened traces and trace lengths less than 100mil.

Chapter 7 HSST

The Logos Family FPGAs' PGL50H and PGL100H devices support the high-speed serial transceiver (HSST).

7.1 HSST Pin Description

The HSST pins of the PGL50H FBG484 product are described in the table below.

Table7-1 PGL50H FBG484 HSST Pin Description

PIN name	PIN type	I/O	PIN description
VCCA_LANE	Dedicated	POWER	1.2V HSST Lane Power Supply: (1) The peak-to-peak noise must be less than 10mV; (2) Leave floating when HSST is not in use; (3) Recommended number of capacitors: 2 capacitors of 4.7μF and 6 capacitors of 0.22μF.
VCCA_PLL_0	Dedicated	POWER	1.2V HSST PLL0 Power Supply: (1) The peak-to-peak noise must be less than 10mV; (2) Leave floating when HSST is not in use; (3) Recommended number of capacitors: 1 capacitor of 4.7μF and 1 capacitor of 0.22μF.
VCCA_PLL_1	Dedicated	POWER	1.2V HSST PLL1 Power Supply: (1) The peak-to-peak noise must be less than 10mV; (2) Leave floating when HSST is not in use; (3) Recommended number of capacitors: 1 capacitor of 4.7μF and 1 capacitor of 0.22μF.
PAD_PLL_TEST_0	Dedicated	Input	HSST Precise Reference Resistor: (1) Requires an external 2KΩ pull-down resistor with a precision of ±1%; (2) The total resistance of the trace across the resistor must be less than 1Ω.
PAD_REFCLK[P,N]_[0,1]	Dedicated	Input	HSST PLL Reference Clock Differential Input: (1) Requires an external AC coupling (100nF capacitors recommended), left floating when not in use.
PAD_TX_SD[P,N][0,1,2,3]	Dedicated	Output	HSST Channel Differential Output: Each HSST has 4 pairs, with AC coupling recommended between them and RX, left floating when not in use.
PAD_RX_SD[P,N][0,1,2,3]	Dedicated	Input	HSST Channel Differential Input: Each HSST has 4 pairs, with AC coupling recommended between them and TX, and idle channels grounded.

The HSST pins of the PGL100H FBG900 product are described in the table below.

Table7-2 PGL100H FBG900 HSST Pin Description

PIN name	PIN type	I/O	PIN description
VCCA_LANE[_T,_B]	Dedicated	POWER	1.2V HSST Lane Power Supply: (1) The peak-to-peak noise must be less than 10mV; (2) Leave floating when HSST is not in use; (3) Recommended number of capacitors: 1 capacitor of 4.7μF and 6 capacitors of 0.22μF.
VCCA_PLL_0[_T,_B]	Dedicated	POWER	1.2V HSST PLL0 Power Supply: (1) The peak-to-peak noise must be less than 10mV; (2) Leave floating when HSST is not in use; (3) Recommended number of capacitors: 1 capacitor of 4.7μF, 2 capacitors of 0.22μF.
VCCA_PLL_1[_T,_B]	Dedicated	POWER	1.2V HSST PLL1 Power Supply: (1) The peak-to-peak noise must be less than 10mV; (2) Leave floating when HSST is not in use; (3) Recommended number of capacitors: 1 capacitor of 4.7μF, 2 capacitors of 0.22μF.
PAD_PLL_TEST_0	Dedicated	Input	HSST Precise Reference Resistor: (1) Requires an external 2KΩ pull-down resistor with a precision of ±1%; (2) The total resistance of the trace across the resistor must be less than 1Ω.
PAD_REFCLK[P,N] _[0,1] [_T,_B]	Dedicated	Input	HSST PLL Reference Clock Differential Input: (1) Requires an external AC coupling (100nF capacitors recommended), left floating when not in use.
PAD_TX_SD[P,N] [0,1,2,3][_T,_B]	Dedicated	Output	HSST Channel Differential Output: Each HSST has 4 pairs, with AC coupling recommended between them and RX, left floating when not in use.
PAD_RX_SD[P,N] [0,1,2,3][_T,_B]	Dedicated	Input	HSST Channel Differential Input: Each HSST has 4 pairs, with AC coupling recommended between them and TX, and idle channels grounded.

7.2 HSST Power Supply Design Guide

- The ripple voltage of VCCA_LANE, VCCA_PLL_0, and VCCA_PLL_1 power supply should be less than 10mv. Please optimize power supply ripple voltage during circuit design to ensure optimal performance.
- All power pins must be powered when using HSST; when HSST is not in use, leave HSST power pins floating and reserve a ground resistor, ground RX pins, and leave other pins floating.
- The requirements of filtering capacitors for HSST Power Supply are as follows:

Table7-3 PGL50H HSST Power Supply Decoupling Capacitor Requirements

Power Supply	4.7uF (X7R/10%)	0.22uF (X7R/10%)
VCCA_LANE	2	6

Power Supply	4.7uF (X7R/10%)	0.22uF (X7R/10%)
VCCA_PLL_0	1	1
VCCA_PLL_1	1	1

Table7-4 PGL100H HSST Power Supply Decoupling Capacitor Requirements

Power Supply	4.7uF (X7R/10%)	0.22uF (X7R/10%)
VCCA_LANE_B(T)	1	6
VCCA_PLL_0_B(T)	1	2
VCCA_PLL_1_B(T)	1	2

Note: Users may adjust the capacitors as needed based on actual conditions.

7.3 HSST Reference Clock Design Guide

- The PAD_REFCLK input pin integrates an internal termination matching resistor, eliminating the need for additional external termination resistor during circuit design.
- For the allowable input range of the reference clock, refer to the "HSST Hard Core DC Characteristics Parameters" section in the ***"DS02001_Logos Family FPGAs Datasheet"***.
- HSSTREFCLK reference clock input is designed with AC coupling, with 100nF capacitors recommended for AC coupling.

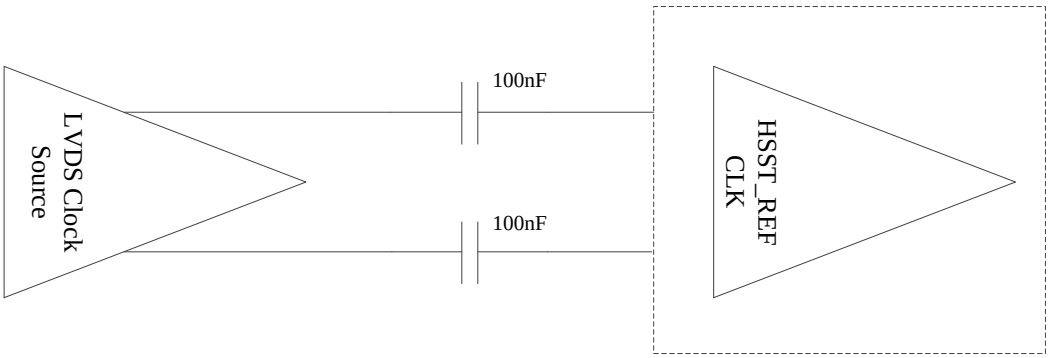


Figure 7-1 HSSTREFCLK Input Diagram for LVDS Level Standard

7.4 Other Considerations

- PLL0 can provide a reference clock for Lane0/1/2/3; PLL1 can provide a clock for Lane2/3;
- For detailed usage of HSST, please refer to the ***"UG020013_Logos Family FPGAs High-Speed Serial Transceiver (HSST) User Guide"***.

7.5 PCIe Hard Core Application Connection Instructions

Table7-5 Recommended PCIe Connection Methods

PCIe Lane	**x1**	**x2**	**x4**
Lane 0	PAD_[TX/RX]_SD 0	PAD_[TX/RX]_SD 0	PAD_[TX/RX]_SD 0
Lane 1	-	PAD_[TX/RX]_SD 1	PAD_[TX/RX]_SD 1
Lane 2	-	-	PAD_[TX/RX]_SD 2
Lane 3	-	-	PAD_[TX/RX]_SD 3

Note:

1. "-" indicates that there is no description for the item.

2. For PGL100H, PAD_SDP_T is preferred to be used as the HSST for PCIe.

Table7-6 Supported PCIe Connection Methods

PCIe Lane	**x1**	**x1[A]**	**x2**	**x2[B]**
Lane 0	PAD_[TX/RX]_SD 0	PAD_[TX/RX]_SD 1/2/3	PAD_[TX/RX]_SD 0	PAD_[TX/RX]_SD 1
Lane 1	-	-	PAD_[TX/RX]_SD 1	PAD_[TX/RX]_SD 0
Lane 2	-	-	-	-
Lane 3	-	-	-	-
PCIe Lane	**x2[A]**	**x2[A]**	**x4**	**x4[B]**
Lane 0	PAD_[TX/RX]_SD 2	PAD_[TX/RX]_SD 3	PAD_[TX/RX]_SD 0	PAD_[TX/RX]_SD 3
Lane 1	PAD_[TX/RX]_SD 3	PAD_[TX/RX]_SD 2	PAD_[TX/RX]_SD 1	PAD_[TX/RX]_SD 2
Lane 2	-	-	PAD_[TX/RX]_SD 2	PAD_[TX/RX]_SD 1
Lane 3	-	-	PAD_[TX/RX]_SD 3	PAD_[TX/RX]_SD 0

Note:

1. IP code shall be changed manually to implement this connection method.

2. IP's Lane Reversal function shall be enabled to implement this connection method.

3. For PGL100H, PAD_SDP_T is recommended to use as the HSST for PCIe.

7.6 HSST PCB Design Guide

7.6.1 Routing Rules

- In an HSST differential pair, the equal length error of P and N shall be constrained within 5mil (total error after adding Pin delay). The space between differential wires and other wires shall be greater than 3W, and differential impedance shall be constrained at 100Ω±10%;
- The optimal location for wire-wrapping to ensure equal length of a differential pair is where the length mismatch between P and N occurs; in principle, tuning delay at the location of the deviation.
- HSST differential signal routing requires a complete reference ground plane, and discontinuities in the ground plane as shown in Figure 7-2 are prohibited;

- Each differential wire should pass no more than two vias, with symmetrical accompanying ground vias set beside the vias for layer change. For high-speed transceiver, minimize the number of vias, shorten via length, and remove via stubs; therefore, the following two methods can be adopted:
  - Route close to the Bottom layer, and shorten the via stub length to the maximum extent possible without using back-drilling technology.
  - Route close to the TOP layer, combined with back-drilling technology, to greatly reduce the via length.

It is recommended that designers choose the appropriate routing method according to the actual PCB stack-up and simulation results, to achieve the balance between performance and cost as much as possible.

- Optimized design of SMT pads for FPGA transceivers, backplane connectors, and coupled series devices can reduce impedance discontinuities in the HSST channel.
- It is recommended to route HSST signal wires between two vias beneath the BGA in the Neck mode, and ensure that the routing impedance of Neck mode is consistent with that of normal mode.

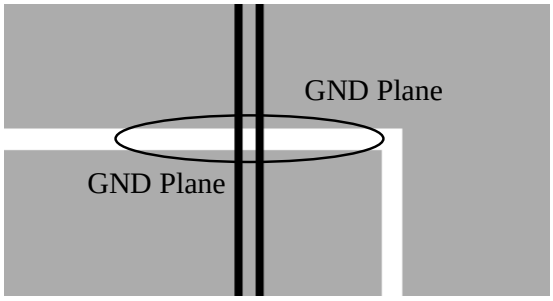


Figure 7-2 Discontinuous Ground Plane

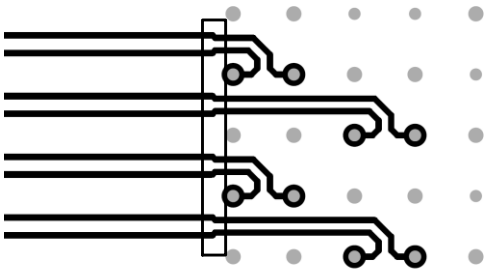
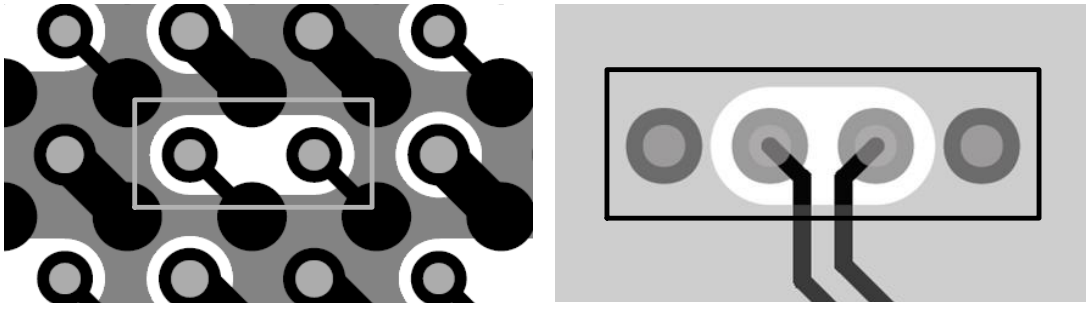


Figure 7-3 Neck Mode Routing Beneath BGA

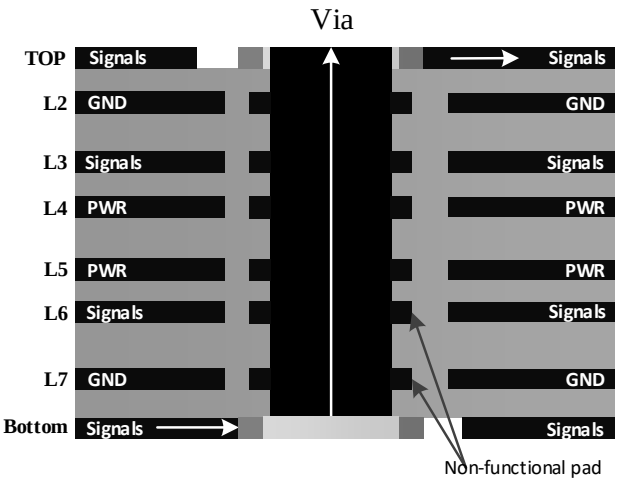
7.6.2 Optimized Design of High-Speed Signal Via

- As shown in Figure 7-4 (1), HSST signal via is designed with an appropriate elongated oval anti-pad to reduce the edge-coupled parasitic capacitance between the via and inner layers; the size of the anti-pad should be evaluated by the designer based on actual via and spacing simulations;
- As shown in Figure 7-4 (2), a symmetrical accompanying ground via needs to be set beside the via for HSST signal layer change, to provide a return path for the signal, thus reducing signal path inductance, and the requirement for symmetry in the accompanying via is to control the symmetry of the PN pair's return path;
- Figure 7-5 illustrates three types of via structures; structure (1) is the most common form and is the default structure in general PCB design software, structure (2) removes the non-functional pads on the inner layers that are not connected, which is beneficial for reducing via parasitic parameters, and structure (3) uses back-drilling technology to remove the via stubs on the basis of structure (2), resulting in excellent performance when routing close to the TOP layer.

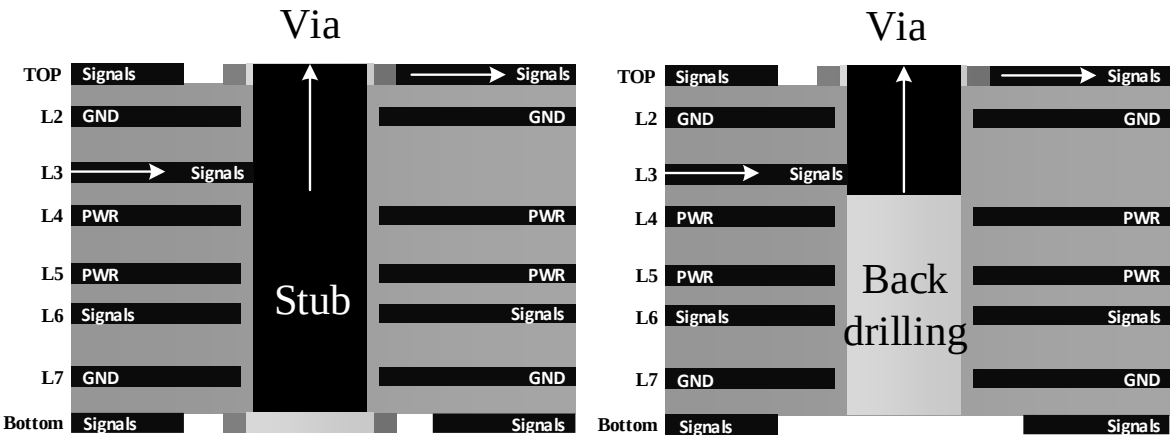


(1) High-Speed Signal Via Anti-Pad Design (2) High-Speed Differential Signal Via Design for Layer Change

Figure 7-4 High-Speed Signal Via Design Examples



(1) Via Structure 1



(1) Via Structure 2 (2) Via Structure 3

Figure 7-5 Via Structure Design Examples

7.6.3 SMT Pad Optimization

SMT pads are inevitable during routing HSST signal wires, such as connecting the gold fingers and their Tx channel AC capacitors. Typically, the SMT pads are much wider than the signal traces. If a 4.6mil trace with a 50Ω characteristic impedance is connected to a 28mil standard PCIe gold finger, the characteristic impedance of gold finger pad with the same reference plane will be much lower than 50Ω, leading to severe impedance discontinuity. To maintain consistent impedance of SMT pads with the transmission impedance, it is recommended to remove the ground plane beneath the SMT pads. As PCBs differ in stack-up, it is not possible to specify the exact size of the area to be removed. Designers can determine the size of the area to be removed through simulation based on the actual stack-up.

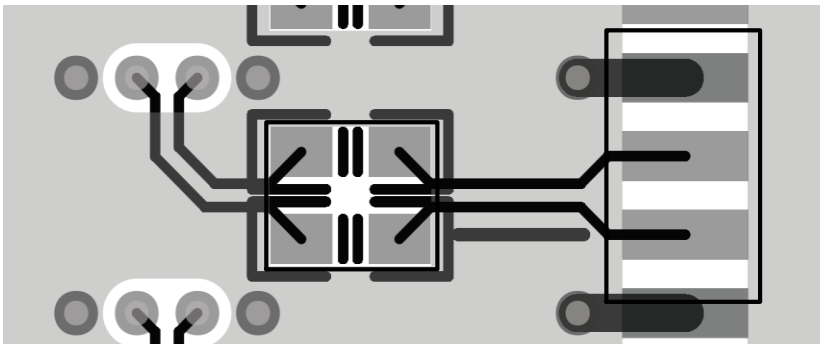


Figure 7-6 High-Speed Signal SMT Pad Design

Chapter 8 LVDS

8.1 Chip Pin Selection Requirements

When using the LVDS interface for Logos Family FPGAs, the corresponding Bank voltage is 2.5V. Therefore, it is preferred to select Banks that do not include FPGA configuration pins. LVDS clock input signals should be connected to the global differential clock input pins of the FPGA chip.

All I/O pairs of PGL22G support true differential input and output.

All I/O pairs of PGL12G support true differential input, but only the right-side I/Os support true differential output.

For PGL25G, PGL50G, PGL50H, and PGL100H, only BANK0 and BANK2 support true differential output.

8.2 LVDS Routing Recommendation

- The transmitter chip should be as close to the receiver chip as possible to minimize the length of the LVDS trace, with 45 °or arc trace corner;
- Differential trace impedance should be constrained at 100ohm ±10%, with the termination matching resistor close to the receiver, minimizing the distance to the receiver pins, and internal matching resistors at the receiver are preferred;
- Minimize the number of vias, with a recommendation of no more than two vias per trace;
- Traces should have a complete reference ground plane;
- When changing signal layers, if the reference plane is also changed, the reference plane requires a via for layer change, and it should be adjacent to the signal via;
- The spacing between different differential pair traces should be greater than 3W, or greater than 5W if conditions permit. The spacing between differential wires and other signal wires should be more than 5W, and the spacing between TX and RX differential pairs should be greater than 5W;
- The two wires within a differential pair should be strictly equal in length, with a length mismatch not exceeding 5mil; differential pairs within the same group should be equal in length, with a mismatch not exceeding 20mil; the principle for length compensation is to compensate where the mismatch occurs;

Chapter 9 MIPI

9.1 Chip Pin Selection Requirements

In the Logos Family PGL22G, the TX and RX ends differ when using the MIPI interface. TX data and clock both use 2-wire scheme, and the Bank voltage is 1.2V. RX data Lane0 uses 4-wire scheme as shown in Figure 9-1, while other Lanes use 2-wire scheme, with both high-speed and low-speed data Banks at 1.2V voltage. The MIPI signal pins first select the bank that does not contain configuration pins. Note that RX and TX pins cannot be allocated in the same Bank. MIPI clock input signals should be connected to the global differential clock input pins of the FPGA chip.

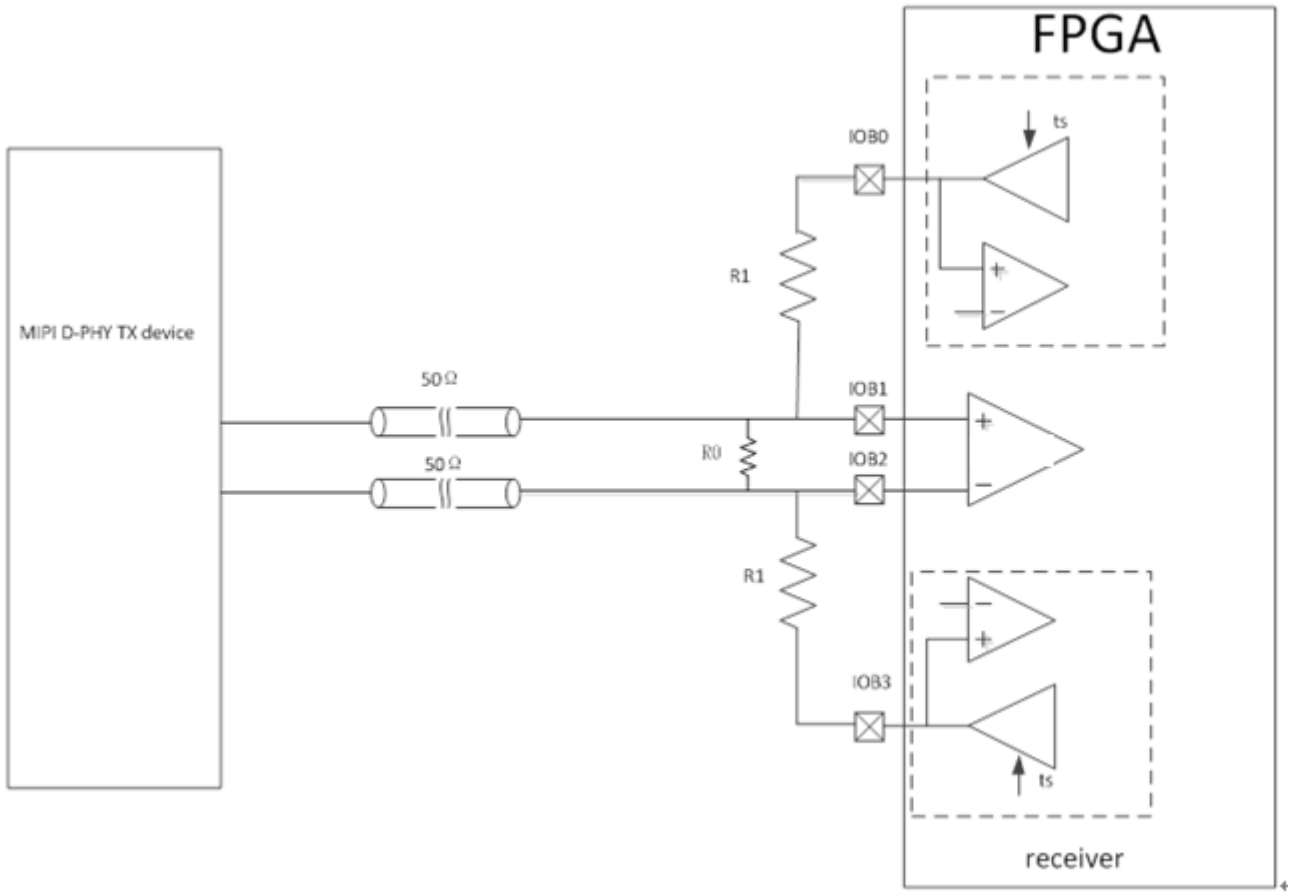


Figure 9-1 Schematic of 4-Wire Scheme for Lane0

In the schematic of the 4-wire scheme for RX data Lane0, IOB0 and IOB3 correspond to low-speed signals, while IOB1 and IOB2 correspond to high-speed signals. The resistance of R0 is 100Ω, and R1 is 50Ω. For other RX lanes signals, external termination matching resistors or internal termination matching resistors of the FPGA chip can be used.

In the Logos Family PGL12G, when using the MIPI interface, both TX and RX ends use 2-wire scheme, with the Bank voltage being 1.2V. Banks that do not include FPGA configuration pins are preferred for MIPI signal pins. Note that RX and TX pins cannot be allocated in the same Bank. MIPI clock input signals should be connected to the global differential clock input pins of the FPGA chip.

For other models in the Logos Family, the MIPI signal TX and RX use two-wire scheme, and a Bank that supports full differential input and output shall be used for the pins, with a VCCIO voltage of 1.2V.

9.2 MIPI PCB Design Requirements

PCB trace shall be designed to ensure that R1 in Figure 9-1 has minimal impact on the differential wires, and route the low-speed signal trace in the 4-wire scheme as general signal traces. Other requirements are the same as those for LVDS trace.

Chapter 10 Clock

10.1 Clock Pin

For the Logos Family FPGAs, each Bank has a certain number of global clock input pins and PLL clock input pins, and some pins are shared between global clock input and PLL clock input. The input of oscillator clock and the synchronous clock will be connected into these pins.

The FPGA output clock can be connected to general I/O.

10.2 Clock Trace

- The oscillator power supply adopts a combination of beads and capacitors of various sizes for filtering.
- The clock circuit should be placed away from the edge of the board, with trace kept distant from signal wires to avoid running parallel with other signal wires.
- When the clock wire is shielded with a ground net, vias shall be set on the ground plane at regular intervals for the shield wire.
- Clock trace should have a complete reference ground plane with minimized layer changes.
- There should be ground vias next to clock vias, and a complete reference ground plane should be present after changing layers.
- Clock trace should maintain continuous impedance and avoid cross splits.
- Reserve a position for a series resistor at the source end of the clock wire.

Chapter 11 Reflow Requirements

The recommended reflow conditions are as follows:

Preheat time t_s (Tsmin 150 ℃ to Tsmax 200 ℃): 60-120s;

Rate of temperature rise (T_L to T_P): ≤ 3 ℃/s;

Holding period of temperature T_L (217 ℃): 60-150s;

Peak temperature T_P of package body: 250 ℃+5 ℃/-0 ℃;

Time (tp)* within 5 ℃ of the specified classification temperature T_P: t_p ≤ 30s;

Rate of temperature fall (T_P to T_L): ≤ 6°C/s;

Time for temperature rising from 25 ℃ to peak temperature (25 ℃ to T_P): ≤ 8min.

Please refer to the J-STD-020E standard for specific packaging.

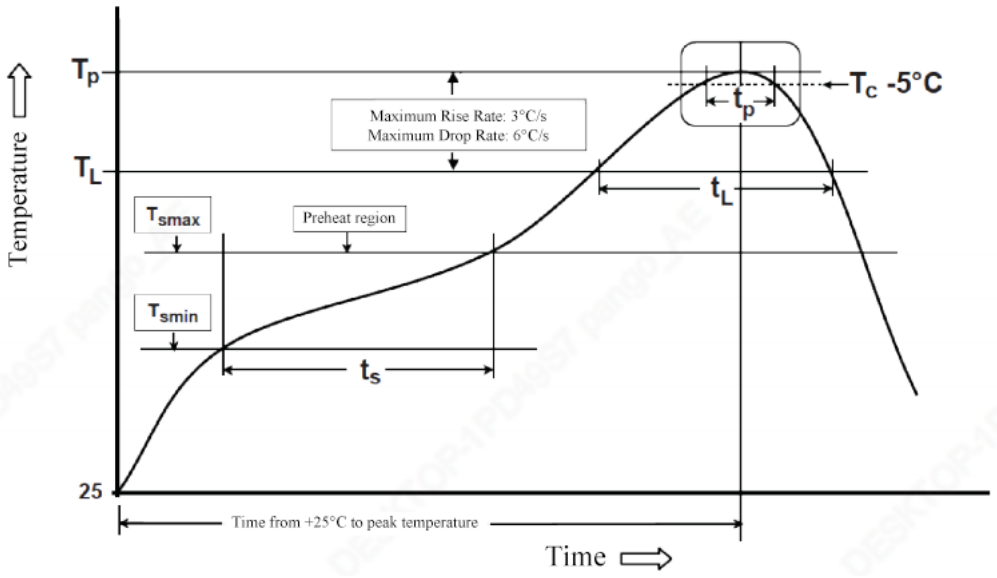


Figure 11-1 Oven Temperature Profile

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