PK04004_PG2L25H_MBG325

(PK04004, V1.1)

(25.03.2022)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.1	25. 03.2022	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
POD	Package Outline Drawing

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Chapter 1 Introduction to Packaging

PG2L25H_MBG325 uses a Wire-Bond BGA type of packaging. Package size: 15x15mm; Number of balls: 324; Ball pitch: 0.8mm; Maximum package thickness: 1.45mm.

Chapter 2 Package Dimension and Pin Definitions

2.1 Package Dimension

Table 2-1 Dimensional Values

Unit: Millimeter

Dimension Symbol	Value			Dimension Symbol	Value		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	1.15	1.30	1.45	c	0.22	0.26	0.30
A1	0.29	0.34	0.39	e	-	0.8	-
A2	0.91	0.96	1.01	b	0.40	0.45	0.50
D	14.9	15.0	15.1	aaa	-	-	0.15
E	14.9	15.0	15.1	ccc	-	-	0.15
D1	-	13.6	-	ddd	-	-	0.15
E1	-	13.6	-	eee	-	-	0.15

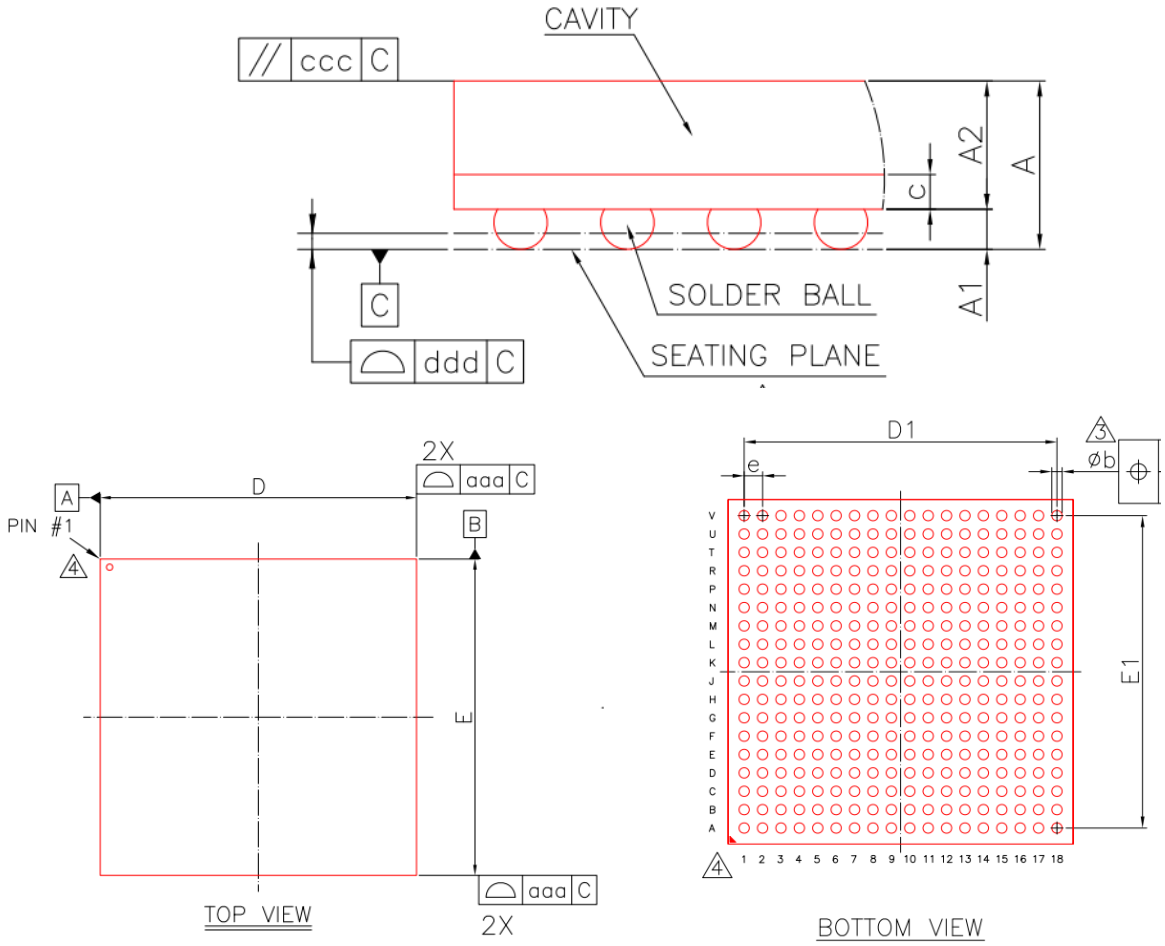

Figure 2-1 Package Outline Dimension (POD)

Note: Pin #1 is the pin 1 position of the chip.

2.2 Pin Definitions

PG2L25H _ MBG325 has 150 user IOs.

Table 2-2 Product Pin Definitions

PIN Name	PIN Type	PIN Direction	PIN Description
General PIN			
DIFFIO_XX_GY _NN[P,N]	General	Input/Output	General pin: (1) "DIFFIO" indicates the pin supports differential input/output and can be used for transmitting and receiving LVDS signals; (2) " XX " indicates bank numbers, which can be L4, L5, R5; (3) "G " indicates belonging to a memory group; (4) "Y " indicates the group number in a bank, each of which contains four groups; (5) "NN" indicates the sequence number of programmable IO pairs in a bank, increasing from 0, a bank contains 24 difference pairs; (6) In "[N,P]", "P" indicates the positive end of the differential pair and "N" indicates the negative end; During initialization (clear configuration memory), all general pins remain in Tri-state, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors. During configuration, all general pins remain in Tri-state except those need to be used for the multiplexed configuration IOs, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors.
SIO_XX_NN	General	Input/Output	General pin: (1) "SIO " indicates the pin only supports single ended input/output; (2) "XX " indicates bank numbers, which can be L4, L5, R5; (3) "NN" indicates the sequence number of programmable IO in a bank, increasing from 0, a bank contains 2 single ended IOs; During initialization (clear configuration memory), all general pins remain in Tri-state, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors. During configuration, all general pins remain in Tri- state except those need to be used for the multiplexed configuration IOs, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors.
Configuration PIN			
INIT_FLAG_N	Dedicated	Bidirectional (open-drain)	Initialization and configuration status dedicated pin: When it is low, it indicates that the FPGA is being initialized (clear configuration memory) or a configuration error has occurred. The pin has an internal weak pull-up resistor

PIN Name	PIN Type	PIN Direction	PIN Description
			that is enabled during configuration; When the FPGA powers up completion, the pin is driven to low level. Once the FPGA completes initialization, the pin is released. During the power up and initialization process, this pin can accept an external low level input to delay the configuration process. When the FPGA detects high level input on this pin after initialization, the FPGA starts the configuration process. During configuration, this pin serves as an output for the configuration error indication state, low level indicates that an error occurred. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 4.7K. After the configuration is complete, user can configure weak pull-up or float state for this pin.
CFG_DONE	Dedicated	Bidirectional (open-drain)	Dedicated configuration status pin, built in weak pull-up resistor about 10K. Output as the configuration completion indicator, high level indicates that the configuration is complete. This pin is an open-drain output. When the FPGA powers up completion, the pin is driven to low level before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released. After the configuration is complete, the pin can be driven externally to low level, Once the internal start-up timing finds that the external DONE pin is low, the internal start-up circuit stops until the external pin is high. After the configuration is complete, user can configure weak pull-up or float state for this pin.
RSTN	Dedicated	Input	Dedicated configuration reset pin, built in weak pull-up resistor and always effective. For restarting configuration logic and configuration memory, active-low. When this pin is low, the FPGA configuration memory is emptied and a new configuration process begins. The configuration logic reset begins with the falling edge of the pin, and the configuration process begins with the rising edge of the pin. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 4.7K. Keeping this pin low during power up does not put the FPGA configuration logic in a reset state. After the configuration is complete, user can configure weak pull-up or float state for this

PIN Name	PIN Type	PIN Direction	PIN Description
			pin.
CFG_CLK	Dedicated	Input/Output	Configuration clock pin. Except for the JTAG configuration mode, the configuration process of the FPGA is synchronize by this clock in other modes. In the slave SPI, slave serial and slave parallel configuration modes, the pin serves as a clock input to obtain configuration data from external sources. In the master SPI configuration mode, the pin serves as a clock output to obtain configuration data from external sources and an external pull-up resistor of 1K is required. When the clock is not needed (such as in the JTAG mode), this pin is in the High-Z state. After the configuration is complete, user can configure weak pull-up or float state for this pin.
TCK	Dedicated	Input	Test clock input pin compliant with IEEE STD 1149.1 and provides a clock for the JTAG chain of the FPGA. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TMS	Dedicated	Input	Dedicated JTAG test mode selection input pin. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TDI	Dedicated	Input	Dedicated JTAG test data input pin. Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TDO	Dedicated	Output	Dedicated JTAG test data output pin Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
MODE_2	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
MODE_1	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
MODE_0	Dedicated	Input	Dedicated configuration pin, used for selecting configuration modes, built in weak pull-up resistor. This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
SCBV	Dedicated	Input	The pin is always effective on BANKCFG, but only on BANK which the multiplexing

PIN Name	PIN Type	PIN Direction	PIN Description
			configuration pins are located during configuration. When the voltage of VCCIOCFG is 2.5V or 3.3V, the pin must be connected to high level and can be connected directly to the VCCIOCFG. When the voltage of VCCIOCFG is 1.8V or lower, the pin must be connected to low level and can be connected directly to the ground. If the multiplexing configuration pin is used, the VCCIO of the BANK which the pin is located must be consistent with VCCIOCFG.
FCS_N	Multiplexed	Output	Multi-function configuration pin, used for the Master SPI configuration mode. (1) In the Master SPI X1, X2 and X4 modes, this pin outputs a chip select signal to external flash, active-low. And should be connected to VCCIO via an external pull-up resistor of no more than 4.7K. (2) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin serves as a general pin.
MOSI_D0	Multiplexed	Input/Output	Multi-function configuration data pin. (1) “MOSI”, in the master SPI X1 mode, this pin used for serial data output and connects to the data input pin of the external SPI flash (such as DQ0, D, SI, IO0, etc). After the command and address are sent to the external SPI flash, the pin output high-Z or weak pull-up, depending on the state of the IO_STATUS_C pin. (2) In the master SPI X2, X4 and X8 modes, the pin is bidirectional data port, as command and address output to the external SPI flash. Receive the lowest bit data from the external SPI flash. The pin connects to the bidirectional data pin of the external SPI flash (such as DQ0, D, SI, IO0, etc). (3) “ D0” in the slave parallel mode, this pin serves as the D[0] bit of the data bus. (4) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state. (5) After the configuration is complete, the pin serves as a general pin.
MISO_D1_DI	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X1 mode, “ MISO” serves as data input and connects to the data output pin of the external SPI flash (such as DQ1, Q, SO, IO1, etc). (2) In the master SPI X2, X4 and X8 modes, “D1” connects to the second serial data output pin of the external SPI flash (such as DQ1, Q, SO, IO1, etc). (3) In the slave parallel mode, this pin serves

PIN Name	PIN Type	PIN Direction	PIN Description
			as the D[1] bit of the data bus. (4) In the slave serial mode, “D1” serves as data input pin. (5) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state. In the other configuration modes(such as JTAG), the state on the pin is ignored (6) After the configuration is complete, the pin serves as a general pin.
D[2, 3]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X4 and X8 modes, serve as data input and connects to the data output pin of the external SPI flash. “ D2” connects to the third bit data output pin of the external SPI flash(such as DQ2, W#, WP#, IO2, etc). “ D3” connects to the fourth bit data output pin of the external SPI flash(such as DQ3, HOLD#, IO3, etc). These pins should be connected to VCCIO via an external weak pull-up resistor of 4.7K. (2) In the slave parallel mode, these pins serve as the D[3:2] bits of the data bus. (3) In the other configuration modes or in initialization process, these pins act as general pins in a high-Z or weak pull-up state. (4) After the configuration is complete, these pins serve as general pins.
D[4, 5, 6, 7]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X8 mode, connect to the second flash in the same way as D[3:0]. (2) In the slave parallel mode, these pins serve as the D[7:4] bits of the data bus. (3) In the other configuration modes or in initialization process, these pins act as general pins in a high-Z or weak pull-up state. (4) After the configuration is complete, these pins serve as general pins.
D[8,…,15]	Multiplexed	Input/Output	Multi-function configuration data pin. (1)In the slave parallel mode, serve as the D[15:8] bits of the data bus. (2) In the other configuration modes, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (3) After the configuration is complete, these pins serve as general pins.
D[16,…,31]_A[0,…,15]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the slave parallel X32 mode, serve as the D[31:16] bits of the data bus. (2) In the other configuration modes, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (3) After the configuration is complete, these pins serve as general pins.
A[16,…,28]	Multiplexed	Output	Multi-function configuration data pin.

PIN Name	PIN Type	PIN Direction	PIN Description
			After the configuration is complete, these pins serve as general pins.
CS_N	Multiplexed	Input	Multi-function configuration pin. For chip select input. Active low. (1) When it is low level, this pin enables the slave parallel mode configuration interface. In the slave parallel configuration mode, the external controller can select the slave parallel bus of the FPGA by controlling this pin. Or this pin connected to the previous FPGA CSO_DOUT pin in the slave parallel configuration chain. (2) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin serves as a general pin.
RWSEL	Multiplexed	Input	Multi-function configuration pin. For selecting the read/write input in the slave parallel configuration mode (high for read and low for write). (1) When it is high level, the slave parallel configuration mode reads data from the data bus. (2) When it is low level, the slave parallel configuration mode writes data to the data bus. (3) Read and write can be switched only when CS_N is high level. (4) After the configuration is complete, the pin serves as a general pin. (5) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state.
CSO_DOUT	Multiplexed	Output(OD)/Output	Multi-function configuration pin. Needed for cascade. (1) In the master SPI X1 mode, this pin serves as cascaded data output. In the other configuration modes, during initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (2) In the slave serial configuration mode, this pin serves as cascaded data output. In the other configuration modes, during initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (3) In the slave parallel cascade configuration mode, this pin serves as a chip select signal open-drain output, connects to downstream chip CS_N pin and should be connected to VCCIO via an external pull-up resistor of 330Ω. (4) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state.
VS[0, 1]	Multiplexed	Output	Multi-function configuration pin.

PIN Name	PIN Type	PIN Direction	PIN Description
			After the configuration is complete, these pins as general pins.
IO_STATUS_C	Multiplexed	Input	Multi-function configuration pin, used for controlling whether the weak pull-up resistors for all general pins are enabled during the configuration process. (1) When it is set to "0", the internal pull-up resistors for all general pins are enabled. (2) When it is set to "1", the internal pull-up resistors for all general pins are disabled. (3)It is recommended that the pin connects to VCCIO via an external weak pull-up resistor. (4)The pin can connect to VCCIO or VSS, either directly or via an external resistor of no more than 1K. (5) This pin must not be left floating before or during configuration.
ECCLKIN	Multiplexed	Input	The external clock input for the Master configuration mode, which is an optional external clock input to the configuration logic. (1) In the master SPI mode, the FPGA can select this clock input as the configuration clock for the configuration logic. This clock can be divided (Depends on the settings in the bitstream) and output from the CFG_CLK pin. (2) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state.
BFOE_N	Multiplexed	Output	Multi-function configuration pin. After the configuration is complete, the pin as a general pin.
BFWE_FCS2_N	Multiplexed	Output	Multi-function configuration pin, used for the master SPI X8 configuration mode. (1) In the Master SPI X8 mode, this pin outputs a chip select signal to external flash, active-low. And should be connected to VCCIO via an external pull-up resistor of no more than 4.7K. (2) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin as a general pin.
BADRVO_N	Multiplexed	Output	Multi-function configuration pin. After the configuration is complete, the pin as a general pin.
Clock PIN			
GMCLK	Multiplexed	Input	Multiplexing global multi-regional clock input pins. These pins can directly drive the regional clock buffer, IO clock buffer, global clock buffer, GPLL, PPLL, and also drive the multi-regional clock buffer. When not used as clock input, these pins serve as general pins, and when the differential pair is connected to a single ended clock source, only the positive

PIN Name	PIN Type	PIN Direction	PIN Description
			end of the differential pair needs to be connected. When these pins serve as single regional clock sources, they are able to drive all the IO clock buffers and regional clock buffers of the BANK.
GSCLK	Multiplexed	Input	Multiplexing global single regional clock input pins. These pins can directly drive the regional clock buffer, IO clock buffer, global clock buffer, GPLL and PPLL. When not used as clock input, these pins serve as general pins, and when the differential pair is connected to a single ended clock source, only the positive end of the differential pair needs to be connected. They are able to drive all the IO clock buffers and regional clock buffers of the BANK.
Memory Interface PIN			
DQS	Multiplexed	N/A	DDR DQS PIN, each memory group contains two pins.
Reference PIN			
VREF	Multiplexed	N/A	Input reference voltage pins,. When not used as external reference voltage pins, these pins serve as general pins,
Power/ Ground PIN			
VCC	Dedicated	Power	Core logic power, 1.0V. Power supply for core logic.
VCC_DRM	Dedicated	Power	DRM power, 1.0V. Dedicated power supply for DRM. If the voltage is the same as VCC, it can be connected to VCC at the board.
VCCA	Dedicated	Power	Analog power, 1.8V. Power supply for internal analog circuit.
VCCIO[L4, L5, R5, CFG]	Dedicated	Power	IO BANK power.
VCCB	Dedicated	Power	Key memory backup battery power supply voltage, 1.0V~1.9V. When the key function is not used, the pin needs to be connected to the VCCA or ground.
VSS	Dedicated	Ground	GND relative to all VCC, VCC_DRM, VCCA, VCCIOx.
ADC PIN			
VCCADC	Dedicated	Power	ADC analog power, 1.8V. Power supply for ADC analog circuit.
VSSADC	Dedicated	Ground	GND relative to VCCADC
VAADC_P	Dedicated	Input	ADC dedicated analog differential input (Positive).
VAADC_N	Dedicated	Input	ADC dedicated analog differential input (Negative).
VREFADC_P	Dedicated	N/A	1.255V ADC reference voltage pin.
VREFADC_N	Dedicated	N/A	ADC reference voltage ground.
VAA[0,..,15]P,VAA[0,..,15]N	Multiplexed	Input	ADC differential analog input signals.
TSDP	Dedicated	N/A	Positive pin of the temperature sensor diode. When not used temperature diode, the pin needs to be connected to the VSS. When

PIN Name	PIN Type	PIN Direction	PIN Description
			temperature sensor diode is to be used, then appropriate external temperature monitoring chip is required.
TSDN	Dedicated	N/A	Negative pin of the temperature sensor diode.
HSST PIN			
HSSTAVCC_QR4	Dedicated	Power	1.0V analog power pins, power supply for HSST internal transmit and receive circuit.
HSSTAVCCPLL_QR4	Dedicated	Power	1.2V analog power pin, power supply for HSST internal PLL.
HSSTRREF_QR4	Dedicated	Input	Calibration resistance input pin of the terminal resistance calibration circuit.
HSSTREFCLK[0,1]P_QR4	Dedicated	Input	Positive end of differential clock input pin, provide a reference clock to HSST.
HSSTREFCLK[0,1]N_QR4	Dedicated	Input	Negative end of differential clock input pin, provide a reference clock to HSST.
HSSTTX[0,1,2,3][P,N]_QR4	Dedicated	Output	Channel differential outputs of HSST. Each HSST has 4 pairs.
HSSTRX[0,1,2,3][P,N]_QR4	Dedicated	Input	Channel differential inputs of HSST. Each HSST has 4 pairs.

2.2.1 Pin Name List

Table 2-3 Pin Name List

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L4	SIO_L4_00	D10		78.0377	
L4	DIFFIO_L4_G0_00P_VAA1P	D8	IO_1_P	96.8587	L4_G0
L4	DIFFIO_L4_G0_00N_VAA1N	C8	IO_1_N	96.1465	L4_G0
L4	DIFFIO_L4_G0_01P_VAA2P	D9	IO_2_P	97.2852	L4_G0
L4	DIFFIO_L4_G0_01N_VAA2N	C9	IO_2_N	86.0388	L4_G0
L4	DIFFIO_L4_G0_02P_DQS_VAA3P	B9	IO_3_P	101.51	L4_G0_DQS
L4	DIFFIO_L4_G0_02N_DQS_VAA3N	A9	IO_3_N	107.237	L4_G0_DQS
L4	DIFFIO_L4_G0_03P	C11	IO_4_P	75.9215	L4_G0
L4	DIFFIO_L4_G0_03N	B11	IO_4_N	79.6203	L4_G0
L4	DIFFIO_L4_G0_04P_VAA5P	B10	IO_5_P	107.228	L4_G0
L4	DIFFIO_L4_G0_04N_VAA5N	A10	IO_5_N	109.021	L4_G0
L4	DIFFIO_L4_G0_05P	D11	IO_6_P	71.0179	L4_G0
L4	DIFFIO_L4_G0_05N_VREF	C12	IO_6_N	70.5254	L4_G0
L4	DIFFIO_L4_G1_06P_VAA7P	B12	IO_7_P	109.944	L4_G1
L4	DIFFIO_L4_G1_06N_VAA7N	A12	IO_7_N	109.723	L4_G1
L4	DIFFIO_L4_G1_07P_VAA8P	A13	IO_8_P	82.0582	L4_G1
L4	DIFFIO_L4_G1_07N_VAA8N	A14	IO_8_N	82.4037	L4_G1
L4	DIFFIO_L4_G1_08P_DQS_VAA9P	C14	IO_9_P	94.611	L4_G1_DQS
L4	DIFFIO_L4_G1_08N_DQS_VAA9N	B15	IO_9_N	93.5507	L4_G1_DQS

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L4	DIFFIO_L4_G1_09P_VAA10P	B14	IO_10_P	77.4111	L4_G1
L4	DIFFIO_L4_G1_09N_VAA10N	A15	IO_10_N	79.7115	L4_G1
L4	DIFFIO_L4_G1_10P_GSCLK	D13	IO_11_P	82.0078	L4_G1
L4	DIFFIO_L4_G1_10N_GSCLK	C13	IO_11_N	86.2281	L4_G1
L4	DIFFIO_L4_G1_11P_GMCLK	E13	IO_12_P	60.521	L4_G1
L4	DIFFIO_L4_G1_11N_GMCLK	D14	IO_12_N	60.8072	L4_G1
L4	DIFFIO_L4_G2_12P_GMCLK	E15	IO_13_P	57.7455	L4_G2
L4	DIFFIO_L4_G2_12N_GMCLK	D15	IO_13_N	65.2042	L4_G2
L4	DIFFIO_L4_G2_13P_GSCLK	E16	IO_14_P	59.5873	L4_G2
L4	DIFFIO_L4_G2_13N_GSCLK	D16	IO_14_N	57.4247	L4_G2
L4	DIFFIO_L4_G2_14P_DQS	B16	IO_15_P	92.2214	L4_G2_DQS
L4	DIFFIO_L4_G2_14N_DQS_BADRVO_N	A17	IO_15_N	96.9937	L4_G2_DQS
L4	DIFFIO_L4_G2_15P_A28	C16	IO_16_P	77.7218	L4_G2
L4	DIFFIO_L4_G2_15N_A27	B17	IO_16_N	84.383	L4_G2
L4	DIFFIO_L4_G2_16P_A26	E17	IO_17_P	73.0632	L4_G2
L4	DIFFIO_L4_G2_16N_A25	D18	IO_17_N	76.0136	L4_G2
L4	DIFFIO_L4_G2_17P_A24	C17	IO_18_P	78.8331	L4_G2
L4	DIFFIO_L4_G2_17N_A23	C18	IO_18_N	78.675	L4_G2
L4	DIFFIO_L4_G3_18P_A22	G17	IO_19_P	61.9522	L4_G3
L4	DIFFIO_L4_G3_18N_VREF_A21	F18	IO_19_N	63.9991	L4_G3
L4	DIFFIO_L4_G3_19P_A20	H16	IO_20_P	42.8034	L4_G3
L4	DIFFIO_L4_G3_19N_A19	G16	IO_20_N	50.4908	L4_G3
L4	DIFFIO_L4_G3_20P_DQS	G15	IO_21_P	71.8595	L4_G3_DQS
L4	DIFFIO_L4_G3_20N_DQS_A18	F15	IO_21_N	71.4449	L4_G3_DQS
L4	DIFFIO_L4_G3_21P_A17	G14	IO_22_P	58.777	L4_G3
L4	DIFFIO_L4_G3_21N_A16	F14	IO_22_N	59.7006	L4_G3
L4	DIFFIO_L4_G3_22P_BFOE_N	H17	IO_23_P	60.9335	L4_G3
L4	DIFFIO_L4_G3_22N_BFWE_FCS2_N	H18	IO_23_N	60.7952	L4_G3
L4	DIFFIO_L4_G3_23P_VS1	F17	IO_24_P	76.6272	L4_G3
L4	DIFFIO_L4_G3_23N_VS0	E18	IO_24_N	75.1761	L4_G3
L4	SIO_L4_01	H14		45.6958	
L5	SIO_L5_00	L14		45.9236	
L5	DIFFIO_L5_G0_00P_MOSI_D0	K16	IO_25_P	59.0079	L5_G0
L5	DIFFIO_L5_G0_00N_MISO_D1_DI	L17	IO_25_N	58.4858	L5_G0
L5	DIFFIO_L5_G0_01P_D2	J15	IO_26_P	45.7486	L5_G0
L5	DIFFIO_L5_G0_01N_D3	J16	IO_26_N	43.3017	L5_G0
L5	DIFFIO_L5_G0_02P_DQS_IO_STATUS_C	J18	IO_27_P	57.5346	L5_G0_DQS
L5	DIFFIO_L5_G0_02N_DQS_ECCLKIN	K18	IO_27_N	61.4672	L5_G0_DQS
L5	DIFFIO_L5_G0_03P_D4	K17	IO_28_P	44.8192	L5_G0

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L5	DIFFIO_L5_G0_03N_D5	L18	IO_28_N	47.8471	L5_G0
L5	DIFFIO_L5_G0_04P_D6	J14	IO_29_P	67.2373	L5_G0
L5	DIFFIO_L5_G0_04N_D7	K15	IO_29_N	66.0463	L5_G0
L5	DIFFIO_L5_G0_05P_FCS_N	L15	IO_30_P	53.3311	L5_G0
L5	DIFFIO_L5_G0_05N_VREF_D8	M15	IO_30_N	51.9001	L5_G0
L5	DIFFIO_L5_G1_06P_D9	M16	IO_31_P	65.977	L5_G1
L5	DIFFIO_L5_G1_06N_D10	M17	IO_31_N	63.0933	L5_G1
L5	DIFFIO_L5_G1_07P_D11	M14	IO_32_P	52.6933	L5_G1
L5	DIFFIO_L5_G1_07N_D12	N14	IO_32_N	52.652	L5_G1
L5	DIFFIO_L5_G1_08P_DQS	N16	IO_33_P	53.6854	L5_G1_DQS
L5	DIFFIO_L5_G1_08N_DQS_D13	N17	IO_33_N	56.3349	L5_G1_DQS
L5	DIFFIO_L5_G1_09P_D14	N18	IO_34_P	59.0042	L5_G1
L5	DIFFIO_L5_G1_09N_D15	P18	IO_34_N	59.9072	L5_G1
L5	DIFFIO_L5_G1_10P_GSCLK	P15	IO_35_P	73.8428	L5_G1
L5	DIFFIO_L5_G1_10N_GSCLK	P16	IO_35_N	73.7692	L5_G1
L5	DIFFIO_L5_G1_11P_GMCLK	P14	IO_36_P	58.7556	L5_G1
L5	DIFFIO_L5_G1_11N_GMCLK	R15	IO_36_N	60.9397	L5_G1
L5	DIFFIO_L5_G2_12P_GMCLK	T14	IO_37_P	96.367	L5_G2
L5	DIFFIO_L5_G2_12N_GMCLK	T15	IO_37_N	93.4302	L5_G2
L5	DIFFIO_L5_G2_13P_GSCLK	R16	IO_38_P	59.732	L5_G2
L5	DIFFIO_L5_G2_13N_GSCLK	R17	IO_38_N	57.5649	L5_G2
L5	DIFFIO_L5_G2_14P_DQS_RWSEL	R18	IO_39_P	66.8627	L5_G2_DQS
L5	DIFFIO_L5_G2_14N_DQS_CSO_DOUT	T18	IO_39_N	69.625	L5_G2_DQS
L5	DIFFIO_L5_G2_15P_CS_N	T17	IO_40_P	65.9314	L5_G2
L5	DIFFIO_L5_G2_15N_D31_A15	U17	IO_40_N	68.5718	L5_G2
L5	DIFFIO_L5_G2_16P_D30_A14	U15	IO_41_P	88.7743	L5_G2
L5	DIFFIO_L5_G2_16N_D29_A13	U16	IO_41_N	78.5296	L5_G2
L5	DIFFIO_L5_G2_17P_D28_A12	V16	IO_42_P	74.3576	L5_G2
L5	DIFFIO_L5_G2_17N_D27_A11	V17	IO_42_N	67.9359	L5_G2
L5	DIFFIO_L5_G3_18P_D26_A10	R13	IO_43_P	59.117	L5_G3
L5	DIFFIO_L5_G3_18N_VREF_D25_A9	T13	IO_43_N	60.3086	L5_G3
L5	DIFFIO_L5_G3_19P_D24_A8	U14	IO_44_P	78.1287	L5_G3
L5	DIFFIO_L5_G3_19N_D23_A7	V14	IO_44_N	76.8307	L5_G3
L5	DIFFIO_L5_G3_20P_DQS	V12	IO_45_P	86.4022	L5_G3_DQS
L5	DIFFIO_L5_G3_20N_DQS_D22_A6	V13	IO_45_N	80.6386	L5_G3_DQS
L5	DIFFIO_L5_G3_21P_D21_A5	T12	IO_46_P	71.7798	L5_G3
L5	DIFFIO_L5_G3_21N_D20_A4	U12	IO_46_N	68.3203	L5_G3
L5	DIFFIO_L5_G3_22P_D19_A3	U11	IO_47_P	80.7828	L5_G3
L5	DIFFIO_L5_G3_22N_D18_A2	V11	IO_47_N	79.8612	L5_G3

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L5	DIFFIO_L5_G3_23P_D17_A1	U9	IO_48_P	81.4647	L5_G3
L5	DIFFIO_L5_G3_23N_D16_A0	V9	IO_48_N	83.9042	L5_G3
L5	SIO_L5_01	U10		65.8443	
R5	SIO_R5_00	J6		23.7553	
R5	DIFFIO_R5_G0_00P	K6	IO_49_P	78.2306	R5_G0
R5	DIFFIO_R5_G0_00N	K5	IO_49_N	78.3389	R5_G0
R5	DIFFIO_R5_G0_01P	J5	IO_50_P	53.533	R5_G0
R5	DIFFIO_R5_G0_01N	J4	IO_50_N	50.3386	R5_G0
R5	DIFFIO_R5_G0_02P_DQS	K2	IO_51_P	51.2631	R5_G0_DQS
R5	DIFFIO_R5_G0_02N_DQS	K1	IO_51_N	53.3679	R5_G0_DQS
R5	DIFFIO_R5_G0_03P	K3	IO_52_P	46.5149	R5_G0
R5	DIFFIO_R5_G0_03N	L2	IO_52_N	48.1942	R5_G0
R5	DIFFIO_R5_G0_04P	L4	IO_53_P	53.557	R5_G0
R5	DIFFIO_R5_G0_04N	L3	IO_53_N	58.8186	R5_G0
R5	DIFFIO_R5_G0_05P	L5	IO_54_P	57.3442	R5_G0
R5	DIFFIO_R5_G0_05N_VREF	M5	IO_54_N	59.1956	R5_G0
R5	DIFFIO_R5_G1_06P	M2	IO_55_P	62.9143	R5_G1
R5	DIFFIO_R5_G1_06N	M1	IO_55_N	64.237	R5_G1
R5	DIFFIO_R5_G1_07P	M6	IO_56_P	70.8653	R5_G1
R5	DIFFIO_R5_G1_07N	N6	IO_56_N	69.858	R5_G1
R5	DIFFIO_R5_G1_08P_DQS	N1	IO_57_P	67.4522	R5_G1_DQS
R5	DIFFIO_R5_G1_08N_DQS	P1	IO_57_N	69.3455	R5_G1_DQS
R5	DIFFIO_R5_G1_09P	M4	IO_58_P	50.9774	R5_G1
R5	DIFFIO_R5_G1_09N	N4	IO_58_N	58.6709	R5_G1
R5	DIFFIO_R5_G1_10P_GSCLK	N3	IO_59_P	58.4611	R5_G1
R5	DIFFIO_R5_G1_10N_GSCLK	N2	IO_59_N	57.3309	R5_G1
R5	DIFFIO_R5_G1_11P_GMCLK	P4	IO_60_P	56.1906	R5_G1
R5	DIFFIO_R5_G1_11N_GMCLK	P3	IO_60_N	52.776	R5_G1
R5	DIFFIO_R5_G2_12P_GMCLK	R2	IO_61_P	70.23	R5_G2
R5	DIFFIO_R5_G2_12N_GMCLK	R1	IO_61_N	68.6529	R5_G2
R5	DIFFIO_R5_G2_13P_GSCLK	R3	IO_62_P	72.9871	R5_G2
R5	DIFFIO_R5_G2_13N_GSCLK	T2	IO_62_N	66.569	R5_G2
R5	DIFFIO_R5_G2_14P_DQS	U2	IO_63_P	75.6878	R5_G2_DQS
R5	DIFFIO_R5_G2_14N_DQS	U1	IO_63_N	73.7211	R5_G2_DQS
R5	DIFFIO_R5_G2_15P	V3	IO_64_P	81.0033	R5_G2
R5	DIFFIO_R5_G2_15N	V2	IO_64_N	76.1516	R5_G2

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R5	DIFFIO_R5_G2_16P	T4	IO_65_P	74.9114	R5_G2
R5	DIFFIO_R5_G2_16N	T3	IO_65_N	70.5782	R5_G2
R5	DIFFIO_R5_G2_17P	U4	IO_66_P	74.5556	R5_G2
R5	DIFFIO_R5_G2_17N	V4	IO_66_N	72.4676	R5_G2
R5	DIFFIO_R5_G3_18P	P6	IO_67_P	70.6987	R5_G3
R5	DIFFIO_R5_G3_18N_VREF	P5	IO_67_N	65.1374	R5_G3
R5	DIFFIO_R5_G3_19P	U6	IO_68_P	75.7368	R5_G3
R5	DIFFIO_R5_G3_19N	U5	IO_68_N	68.619	R5_G3
R5	DIFFIO_R5_G3_20P_DQS	R5	IO_69_P	62.5627	R5_G3_DQS
R5	DIFFIO_R5_G3_20N_DQS	T5	IO_69_N	66.6075	R5_G3_DQS
R5	DIFFIO_R5_G3_21P	R7	IO_70_P	66.5461	R5_G3
R5	DIFFIO_R5_G3_21N	T7	IO_70_N	66.6965	R5_G3
R5	DIFFIO_R5_G3_22P	U7	IO_71_P	56.758	R5_G3
R5	DIFFIO_R5_G3_22N	V6	IO_71_N	53.1491	R5_G3
R5	DIFFIO_R5_G3_23P	V8	IO_72_P	62.8032	R5_G3
R5	DIFFIO_R5_G3_23N	V7	IO_72_N	60.4554	R5_G3
R5	SIO_R5_01	R6		32.671	
	HSSTRX3N_QR4	E3	IO_73_N	41.0186	
	HSSTRX3P_QR4	E4	IO_73_P	41.6938	
	HSSTRX1N_QR4	C3	IO_74_N	48.4802	
	HSSTRX1P_QR4	C4	IO_74_P	45.7103	
	HSSTRX2N_QR4	A3	IO_75_N	65.4003	
	HSSTRX2P_QR4	A4	IO_75_P	64.3954	
	HSSTRX0N_QR4	G3	IO_76_N	34.1468	
	HSSTRX0P_QR4	G4	IO_76_P	30.4415	
	HSSTTX0N_QR4	B1	IO_77_N	73.9438	
	HSSTTX0P_QR4	B2	IO_77_P	71.5102	
	HSSTTX1N_QR4	D1	IO_78_N	63.492	
	HSSTTX1P_QR4	D2	IO_78_P	61.6092	
	HSSTTX2N_QR4	F1	IO_79_N	55.1799	
	HSSTTX2P_QR4	F2	IO_79_P	53.7882	
	HSSTTX3N_QR4	H1	IO_80_N	51.2552	
	HSSTTX3P_QR4	H2	IO_80_P	49.522	
	HSSTREFCLK0N_QR4	B5	IO_81_N	63.0209	
	HSSTREFCLK0P_QR4	B6	IO_81_P	63.8958	
	HSSTREFCLK1N_QR4	D5	IO_82_N	44.9734	
	HSSTREFCLK1P_QR4	D6	IO_82_P	50.3469	
	HSSTRREF_QR4	A6		65.8251	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	CFG_CLK	E8		27.6217	
	CFG_DONE	F12		70.0035	
	INIT_FLAG_N	T10		41.5214	
	MODE_0	R12		51.6864	
	MODE_1	R11		52.977	
	MODE_2	F13		76.5249	
	RSTN	P10		27.0045	
	SCBV	E12		79.6255	
	TCK	F8		50.9062	
	TDI	T9		83.5087	
	TDO	T8		87.2785	
	TMS	R8		86.2375	
	TSDN	M9	IO_83_N	75.3533	
	TSDP	M10	IO_83_P	68.7302	
	VAADC_N	L9	IO_84_N	57.0579	
	VAADC_P	K10	IO_84_P	55.2397	
	VREFADC_N	K9	IO_85_N	64.7262	
	VREFADC_P	L10	IO_85_P	62.7944	
	HSSTAVCCPLL_QR4	A2		79.3182	
	HSSTAVCCPLL_QR4	C1		79.3182	
	HSSTAVCCPLL_QR4	E1		79.3182	
	HSSTAVCCPLL_QR4	F3		79.3182	
	HSSTAVCCPLL_QR4	G2		79.3182	
	HSSTAVCC_QR4	F5		159.145	
	HSSTAVCC_QR4	B4		159.145	
	HSSTAVCC_QR4	C5		159.145	
	HSSTAVCC_QR4	E5		159.145	
	VCC	F7			
	VCC	F9			
	VCC	G8			
	VCC	H7			
	VCC	H9			
	VCC	J8			
	VCC	J12			
	VCC	K7			
	VCC	K11			
	VCC	L8			
	VCC	L12			
	VCC	M7			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VCC	M11			
	VCC	N8			
	VCC	N10			
	VCC	N12			
	VCC	P9			
	VCC	P11			
	VCCA	G12			
	VCCA	H13			
	VCCA	K13			
	VCCA	M13			
	VCCA	P13			
	VCCADC	J10			
	VCCB	E11			
	VCC_DRM	F11			
	VCC_DRM	G10			
	VCC_DRM	H11			
	VCCIOCFG	E10			
	VCCIOCFG	R10			
	VCCIOL4	A16			
	VCCIOL4	B13			
	VCCIOL4	C10			
	VCCIOL4	D17			
	VCCIOL4	E14			
	VCCIOL4	G18			
	VCCIOL4	H15			
	VCCIOL5	L16			
	VCCIOL5	P17			
	VCCIOL5	R14			
	VCCIOL5	T11			
	VCCIOL5	U8			
	VCCIOL5	U18			
	VCCIOL5	V15			
	VCCIOR5	L6			
	VCCIOR5	M3			
	VCCIOR5	P7			
	VCCIOR5	R4			
	VCCIOR5	T1			
	VCCIOR5	V5			
	VSSADC	J9			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	A1			
	VSS	A5			
	VSS	A7			
	VSS	A8			
	VSS	A11			
	VSS	A18			
	VSS	B3			
	VSS	B7			
	VSS	B8			
	VSS	B18			
	VSS	C2			
	VSS	C6			
	VSS	C7			
	VSS	C15			
	VSS	D3			
	VSS	D4			
	VSS	D7			
	VSS	D12			
	VSS	E2			
	VSS	E6			
	VSS	E7			
	VSS	E9			
	VSS	F4			
	VSS	F6			
	VSS	F10			
	VSS	F16			
	VSS	G1			
	VSS	G5			
	VSS	G6			
	VSS	G7			
	VSS	G9			
	VSS	G11			
	VSS	G13			
	VSS	H3			
	VSS	H4			
	VSS	H5			
	VSS	H6			
	VSS	H8			
	VSS	H10			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	H12			
	VSS	J1			
	VSS	J2			
	VSS	J3			
	VSS	J7			
	VSS	J11			
	VSS	J13			
	VSS	J17			
	VSS	K4			
	VSS	K8			
	VSS	K12			
	VSS	K14			
	VSS	L1			
	VSS	L7			
	VSS	L11			
	VSS	L13			
	VSS	M8			
	VSS	M12			
	VSS	M18			
	VSS	N5			
	VSS	N7			
	VSS	N9			
	VSS	N11			
	VSS	N13			
	VSS	N15			
	VSS	P2			
	VSS	P8			
	VSS	P12			
	VSS	R9			
	VSS	T6			
	VSS	T16			
	VSS	U3			
	VSS	U13			
	VSS	V1			
	VSS	V10			
	VSS	V18			

Chapter 3 Thermal Resistance

Table 3-1 Thermal Resistance

θJA(℃/W) (Flow: 0m/s)	**θJB(℃/W)**	**θJC(℃/W)**	**θJA(℃/W) (Flow: 1m/s)**	**θJA(℃/W) (Flow: 2m/s)**
21.2	13.4	7.1	18.5	16.7

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