PG2L100H Full-resource Test Project Description

(V1.4)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.4		Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
CLM	Configurable Logic Module
DRM	Dedicated RAM Module
PLL	Phase Locked Loop
APM	Arithmetic Process Module

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Chapter 1 Overview

This document mainly introduces the methods for testing the main core resources of PG2L100H, including 133,200 FFs, 66,600 LUTs (for instantiating 19,900 distributed RAMs), 155 DRMs, 240 APMs, and 12 PLLs (6 GPLLs and 6 PPLLs). The full-resource test project includes three sub-projects, covering tests for all the logic resources mentioned above. The resources covered in the tests of each project are as follows.

Project I: Covers CLMA units with smaller vertical coordinates in the Logic Tile, and tests all LUTs, main registers, and additional registers in the units covered. The logic units to be tested account for 50% of the total logic resources. Additionally, 4 GPLL modules are covered in Project I, which VCO frequency reaches the upper limit of 1200MHz.

Project II: Covers CLMA units or CLMS units with larger vertical coordinates in the Logic Tile, and tests all LUTs, main registers, and additional registers in the units covered. The logic units to be tested account for 50% of the total logic resources (the other 50% of units are tested in Project I). Additionally, 4 PPLL modules are covered in Project II, which VCO frequency reaches the upper limit of 2125MHz (near the upper limit).

Project III: Covers all CLMS units which work as distributed RAMs, all APM units, all DRM units, 2 GPLL modules and 2 PPLL modules, which GPLL's VCO frequency reaches the lower limit of 600MHz, and the PPLL's VCO Frequency reaches lower limit of 1350MHz.

Chapter 2 Project I

2.1 System Planning

This project is divided into two submodules, namely CLM_LUT_FF (testing the LUTs and registers in CLM) and gpll_top (testing the GPLLs). The top-level module mainly performs signal synchronisation and debounce. There are a total of 6 top-level signals, as shown in Table 2-1.

Table 2-1 Top-level Signals and Descriptions of Project I

No.	Signal Name	Input/Output	Signal Description
1	clk	Input	System clock, 25MHz
2	rst_n	Input	Asynchronous reset signal, active-low
3	error_in	Input	Error injection signal, active-high
4	clm_led	Output	LUT6_DFF test state indicator. Low indicates pass, and high indicates fail.
5	gpll_lock_led	Output	GPLL output frequency lock signal. High indicates pass, and low indicates fail.
6	gpll_led	Output	GPLL output frequency test signal, Low indicates pass, and high indicates fail.

2.2 Functional Module Design

2.2.1 CLM_LUT_FF Module

Based on the SSA failure model, build LUT6_DFF pair, traverse the input combinations through the counter signal, and perform an XOR comparison on the outputs and chain the results in series. The test circuit structure is shown in Figure 2-1.

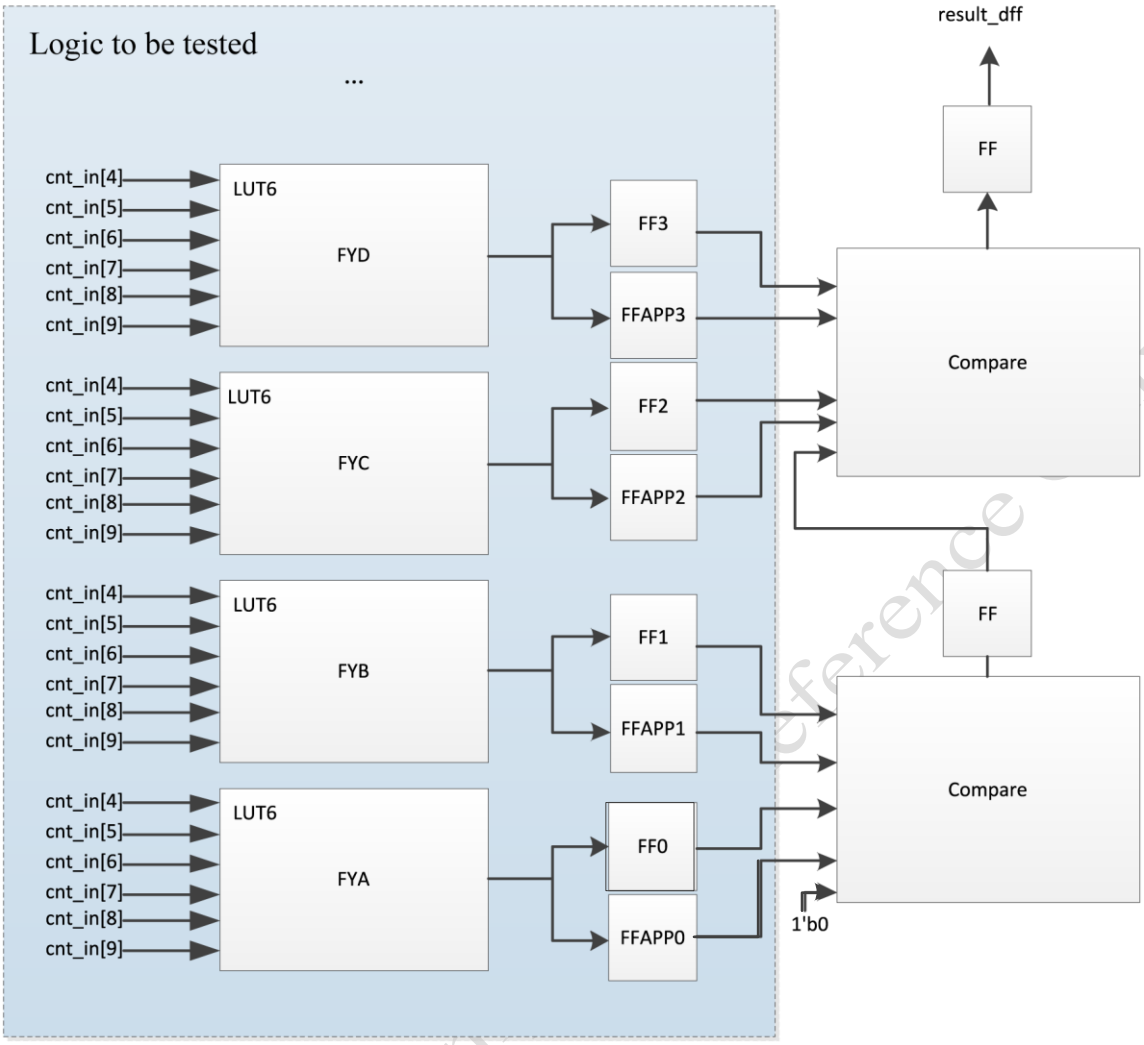

Figure 2-1 LUT6_DFF Test Circuit Structure

Error injection is supported. When the error injection signal is valid, if the highest-bit input of the first-stage LUT differs from the other LUTs, the XOR comparison logic

outputs high, indicating a testing error.

The resource instantiation is shown in Figure 2-2.

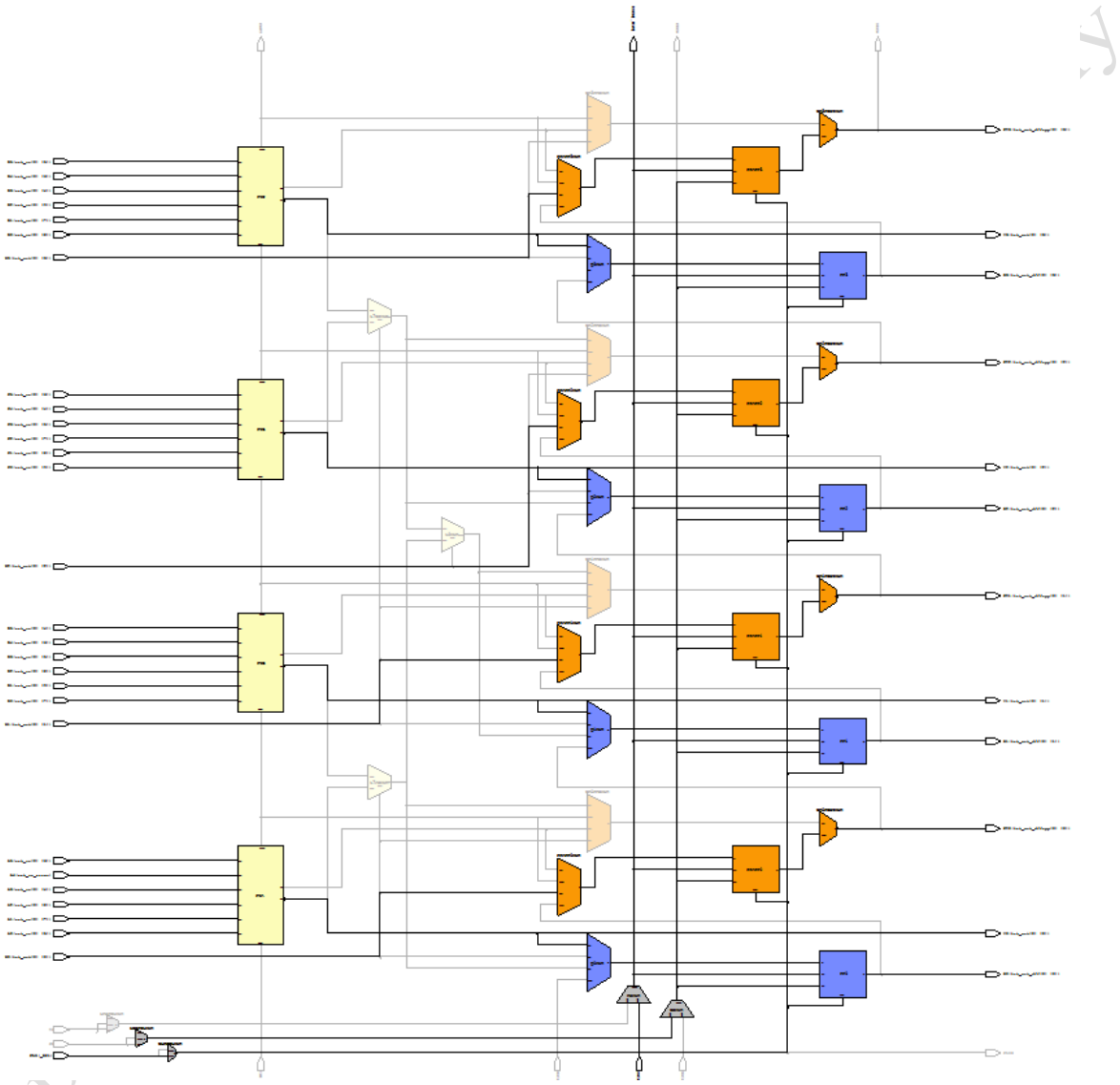

Figure 2-2 LUT_DFF Resource Instantiation

2.2.2 gpll_top Module

Test objective: This module instantiates 4 GPLL modules, which VCO frequency reaches the upper limit of 1200MHz, for testing the output frequency and lock signals.

Test method: Count the input reference clock and output clock separately, and test the output clock

frequency based on its multiplication relationship with the input reference clock.

If the output frequency deviation exceeds the expected frequency by ±5%, the testing result is fail.

In the design, the calculation method for the GPLL output clock count range is as follows: Suppose the input reference clock cycle is tref, and the pll output clock clkout cycle is t0, then cnt_min = (10000 * tref / t0) * 0.95 and cnt_max = (10000 * tref / t0) *1.05.

When the error injection signal is valid, the PLL is reset, the GPLL will not be locked, and the output clock counter will also be reset, indicating a clock frequency test failure.

The GPLL module test circuit is as shown in the figure below.

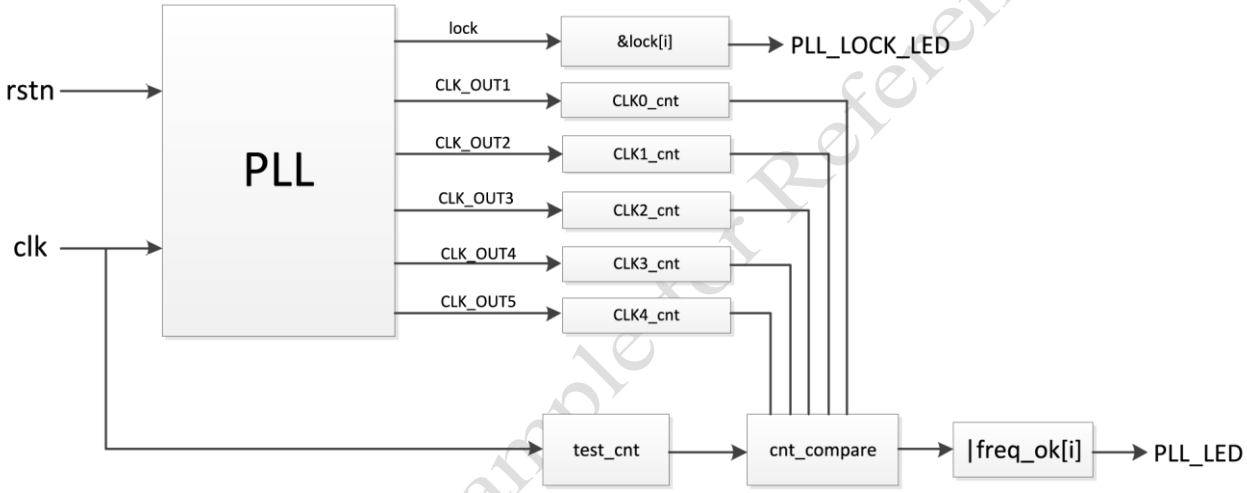

Figure 2-3 GPLL Test Circuit Structure

2.3 PDS Compilation Results

In Project I, the resource usage rate after placement and routing based on PDS2021.1-SP2.1 compilation is shown in the figure below.

Logic Utilization	Used	Available	Utilization(%)
Use of ADC	0	1	0
Use of ANALOG	0	1	0
Use of APM	0	240	0
Use of BKCL	3	6	50
Use of CCS	1	1	100
Use of CLMA	11623	11675	100
FF	75165	93400	81
LUT	41861	46700	90
LUT-FF pairs	41734	46700	90
Use of CLMS	4874	4975	98
FF	11959	39800	31
LUT	12206	19900	62
LUT-FF pairs	11838	19900	60
Distributed RAM	0	19900	0
Use of DDRPHY_CPD	0	12	0
Use of DDRPHY_IOCLK_DIV	0	6	0
Use of DDR_PHY	0	24	0
Use of DRM	0	155	0
Use of GPLL	4	6	67
Use of GSEB	0	218	0
Use of HARD0	1239	10550	12
Use of HCKB	14	96	15
Use of HCKMUX_TEST	0	8	0
Use of HSSTLP	0	2	0
Use of IO	6	300	2
Use of IOCKB	0	24	0
Use of IOCKMUX_TEST	0	6	0

Figure 2-4 Resource Usage Rate of Project I

The timing report is shown in the figure below.

	Clock	Fmax	Requested Frequency	Slack
1	clk	72.480MHz	50.000MHz	6.203
2	clk|u_gpll_top/GPLL[0].u_GPLL/u_gpll/CLKOUT0_Inferred	372.162MHz	40.000MHz	22.313
3	clk|u_gpll_top/GPLL[0].u_GPLL/u_gpll/CLKOUT1_Inferred	313.578MHz	80.000MHz	9.311
4	clk|u_gpll_top/GPLL[0].u_GPLL/u_gpll/CLKOUT2_Inferred	444.444MHz	150.015MHz	4.416
5	clk|u_gpll_top/GPLL[0].u_GPLL/u_gpll/CLKOUT3_Inferred	471.476MHz	240.038MHz	2.045
6	clk|u_gpll_top/GPLL[0].u_GPLL/u_gpll/CLKOUT4_Inferred	492.368MHz	240.038MHz	2.135
7	clk|u_gpll_top/GPLL[1].u_GPLL/u_gpll/CLKOUT0_Inferred	347.222MHz	40.000MHz	22.120
8	clk|u_gpll_top/GPLL[1].u_GPLL/u_gpll/CLKOUT1_Inferred	384.763MHz	80.000MHz	9.901
9	clk|u_gpll_top/GPLL[1].u_GPLL/u_gpll/CLKOUT2_Inferred	467.508MHz	150.015MHz	4.527
10	clk|u_gpll_top/GPLL[1].u_GPLL/u_gpll/CLKOUT3_Inferred	492.368MHz	240.038MHz	2.135
11	clk|u_gpll_top/GPLL[1].u_GPLL/u_gpll/CLKOUT4_Inferred	504.032MHz	240.038MHz	2.182
12	clk|u_gpll_top/GPLL[2].u_GPLL/u_gpll/CLKOUT0_Inferred	338.181MHz	40.000MHz	22.043
13	clk|u_gpll_top/GPLL[2].u_GPLL/u_gpll/CLKOUT1_Inferred	456.204MHz	80.000MHz	10.308
14	clk|u_gpll_top/GPLL[2].u_GPLL/u_gpll/CLKOUT2_Inferred	512.033MHz	150.015MHz	4.713
15	clk|u_gpll_top/GPLL[2].u_GPLL/u_gpll/CLKOUT3_Inferred	480.769MHz	240.038MHz	2.086
16	clk|u_gpll_top/GPLL[2].u_GPLL/u_gpll/CLKOUT4_Inferred	478.240MHz	240.038MHz	2.075
17	clk|u_gpll_top/GPLL[3].u_GPLL/u_gpll/CLKOUT0_Inferred	447.427MHz	40.000MHz	22.765
18	clk|u_gpll_top/GPLL[3].u_GPLL/u_gpll/CLKOUT1_Inferred	492.611MHz	80.000MHz	10.470
19	clk|u_gpll_top/GPLL[3].u_GPLL/u_gpll/CLKOUT2_Inferred	500.250MHz	150.015MHz	4.667
20	clk|u_gpll_top/GPLL[3].u_GPLL/u_gpll/CLKOUT3_Inferred	522.193MHz	240.038MHz	2.251
21	clk|u_gpll_top/GPLL[3].u_GPLL/u_gpll/CLKOUT4_Inferred	513.084MHz	240.038MHz	2.217

Figure 2-5 Timing Report of Project I

2.4 Simulation Results

The simulation results of Project I are shown in the figure below.

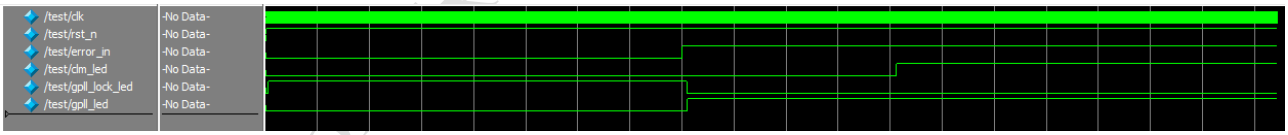

Figure 2-6 Simulation Results of Project I

2.5 On-board Test

1. Configure the bitstream, and repeatedly perform reset and un-reset tests for 1000 cycles, pass.
2. Repeatedly configure the bitstream without power-down and test for 1000 cycles, pass.
3. Configure the bitstream upon power-up, test and then power down, repeatedly test for 1000 cycles, pass.

2.6 Warning Descriptions

1. LUT and FF are merged by the tool into LUT-FF pairs. This warning can be ignored;
2. IO has no timing constraints, and users can make modifications as needed. This warning can be ignored;
3. Registers with floating output are optimized. This warning can be ignored;
4. If constraints are applied using fdc, the previously generated pcf in the project will be overridden. This warning can be ignored.

Chapter 3 Project II

3.1 System Planning

This project is divided into two submodules, namely CLM_LUT_FF (testing the LUTs and registers in CLM) and ppll_top (testing the PPLLs). The top-level module mainly performs signal synchronisation and debounce. There are a total of 6 top-level signals, as shown in Table 3-1.

Table 3-1 Top-level Signals and Descriptions of Project II

No.	Signal Name	Input/Output	Description
1	clk	Input	System clock, 25MHz
2	rst_n	Input	Asynchronous reset signal, active-low
3	error_in	Input	Error injection signal, active-high
4	clm_led	Output	LUT6_DFF test state indicator. Low indicates pass, and high indicates fail.
5	ppll_lock_led	Output	PPLL output frequency lock signal. High indicates pass, and low indicates fail.
6	ppll_led	Output	PPLL output frequency test signal. High indicates pass, and low indicates fail.

3.2 Functional Module Design

3.2.1 CLM_LUT_FF Module

Test objective: This module tests the LUT6_DFF pairs in CLMs, testing 50% of the resources by each of Project I and Project II.

Test method: Same as Project I.

3.2.2 ppll_top Module

Test objective: This module instantiates 4 PPLL modules, which VCO frequency reaches the upper limit of 2125MHz, for testing the output frequency and the lock signal.

Test method: Count the input reference clock and output clock separately, and test the output clock frequency based on its multiplication relationship with the input reference clock.

If the output frequency deviation exceeds the expected frequency by ±5%, the testing result is fail.

In the design, the PPLL output clock count range is calculated as follows: Suppose the input reference clock cycle is tref, and the pll output clock clkout cycle is t0, then cnt_min = (10000 * tref / t0) * 0.95, and cnt_max = (10000 * tref / t0) *1.05.

When the error injection signal is valid, the PPLL is reset, the PPLL will not be locked, and the output clock counter will also be reset, indicating a clock frequency test failure.

The PPLL module test circuit is the same as GPLL.

3.3 PDS Compilation Results

In Project II, the resource usage rate after placement and routing based on PDS2021.1-SP2.1 compilation is shown in the figure below.

Logic Utilization	Used	Available	Utilization(%)
Use of ADC	0	1	0
Use of ANALOG	0	1	0
Use of APM	0	240	0
Use of BKCL	3	6	50
Use of CCS	1	1	100
Use of CLMA	9529	11675	82
FF	47324	93400	51
LUT	34127	46700	74
LUT-FF pairs	33701	46700	73
Use of CLMS	4975	4975	100
FF	39800	39800	100
LUT	19900	19900	100
LUT-FF pairs	19900	19900	100
Distributed RAM	0	19900	0
Use of DDRPHY_CPD	0	12	0
Use of DDRPHY_IOCLK_DIV	0	6	0
Use of DDR_PHY	0	24	0
Use of DRM	0	155	0
Use of GPLL	0	6	0
Use of GSEB	0	218	0
Use of HARD0	1214	10550	12
Use of HCKB	12	96	13
Use of HCKMUX_TEST	0	8	0
Use of HSSTLP	0	2	0
Use of IO	6	300	2
IOBD	3	144	3
IOBS	3	156	2

Logic Utilization	Used	Available	Utilization(%)
IOBD	3	144	3
IOBS	3	156	2
Use of IOCKB	0	24	0
Use of IOCKMUX_TEST	0	6	0
Use of IOLHR	6	300	2
Use of KEYRAM	0	1	0
Use of MFG_TEST	0	1	0
Use of MRCKB	0	12	0
Use of MRCKMUX_TEST	0	6	0
Use of MRPOSTMUX_TEST	0	6	0
Use of PCIE	0	1	0
Use of PCKMUX_TEST	0	12	0
Use of PLLMRMUX_TEST	0	6	0
Use of PLLREFMUX_TEST	0	6	0
Use of PPLL	4	6	67
Use of PREGMUXC_TEST	0	4	0
Use of PREGMUXLR_TEST	0	6	0
Use of RCKB	16	24	67
Use of RCKMUX_TEST	0	6	0
Use of SCANCHAIN	0	1	0
Use of SCKMUX_TEST	0	12	0
Use of SFB	0	2225	0
Use of SPAD	0	8	0
Use of TSERDES	0	48	0
Use of USCM	5	32	16
Use of USCMMUX_TEST	0	32	0

Figure 3-1 Resource Usage Rate of Project II

The timing report of Project II is shown in the figure below.

	Clock	Fmax	Requested Frequency	Slack
1	clk	75.177MHz	50.000MHz	6.698
2	clk|u_ppll_top/PPLL[0].u_PPLL/u_ppll/CLKOUT0_Inferred	450.045MHz	40.095MHz	22.719
3	clk|u_ppll_top/PPLL[0].u_PPLL/u_ppll/CLKOUT1_Inferred	440.141MHz	78.709MHz	10.433
4	clk|u_ppll_top/PPLL[0].u_PPLL/u_ppll/CLKOUT2_Inferred	410.678MHz	163.479MHz	3.682
5	clk|u_ppll_top/PPLL[0].u_PPLL/u_ppll/CLKOUT3_Inferred	524.109MHz	265.675MHz	1.856
6	clk|u_ppll_top/PPLL[0].u_PPLL/u_ppll/CLKOUT4_Inferred	483.793MHz	265.675MHz	1.697
7	clk|u_ppll_top/PPLL[1].u_PPLL/u_ppll/CLKOUT0_Inferred	265.745MHz	40.095MHz	21.178
8	clk|u_ppll_top/PPLL[1].u_PPLL/u_ppll/CLKOUT1_Inferred	426.076MHz	78.709MHz	10.358
9	clk|u_ppll_top/PPLL[1].u_PPLL/u_ppll/CLKOUT2_Inferred	330.251MHz	163.479MHz	3.089
10	clk|u_ppll_top/PPLL[1].u_PPLL/u_ppll/CLKOUT3_Inferred	499.750MHz	265.675MHz	1.763
11	clk|u_ppll_top/PPLL[1].u_PPLL/u_ppll/CLKOUT4_Inferred	504.286MHz	265.675MHz	1.781
12	clk|u_ppll_top/PPLL[2].u_PPLL/u_ppll/CLKOUT0_Inferred	358.551MHz	40.095MHz	22.152
13	clk|u_ppll_top/PPLL[2].u_PPLL/u_ppll/CLKOUT1_Inferred	399.521MHz	78.709MHz	10.202
14	clk|u_ppll_top/PPLL[2].u_PPLL/u_ppll/CLKOUT2_Inferred	424.628MHz	163.479MHz	3.762
15	clk|u_ppll_top/PPLL[2].u_PPLL/u_ppll/CLKOUT3_Inferred	502.008MHz	265.675MHz	1.772
16	clk|u_ppll_top/PPLL[2].u_PPLL/u_ppll/CLKOUT4_Inferred	533.333MHz	265.675MHz	1.889
17	clk|u_ppll_top/PPLL[3].u_PPLL/u_ppll/CLKOUT0_Inferred	351.247MHz	40.095MHz	22.094
18	clk|u_ppll_top/PPLL[3].u_PPLL/u_ppll/CLKOUT1_Inferred	360.750MHz	78.709MHz	9.933
19	clk|u_ppll_top/PPLL[3].u_PPLL/u_ppll/CLKOUT2_Inferred	455.166MHz	163.479MHz	3.920
20	clk|u_ppll_top/PPLL[3].u_PPLL/u_ppll/CLKOUT3_Inferred	490.918MHz	265.675MHz	1.727
21	clk|u_ppll_top/PPLL[3].u_PPLL/u_ppll/CLKOUT4_Inferred	490.436MHz	265.675MHz	1.725

Figure 3-2 Timing Report of Project II

3.4 Simulation Results

The top-level signal simulation results of Project II are shown in the figure below.

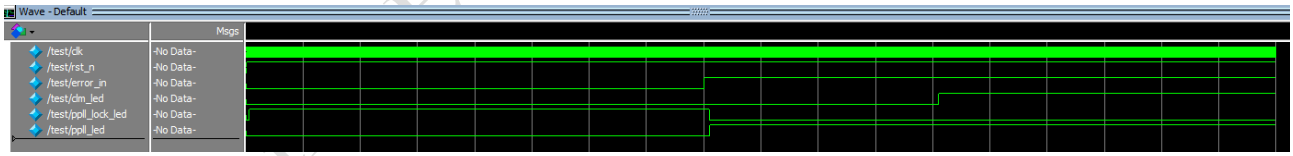

Figure 3-3 Simulation Results of Project II

3.5 On-board Test

1. Configure the bitstream, and repeatedly perform reset and un-reset tests for 1000 cycles, pass.
2. Repeatedly configure the bitstream without power-down and test for 1000 cycles, pass.
3. Configure the bitstream upon power-up, test and then power down, repeatedly test for 1000 cycles, pass.

3.6 Warning Descriptions

1. LUT and FF are merged by the tool into LUT-FF pairs. This warning can be ignored;
2. IO has no timing constraints, and users can make modifications as needed. This warning can be ignored;
3. Registers with floating output are optimized. This warning can be ignored;
4. If constraints are applied using fdc, the previously generated pcf in the project will be overridden. This warning can be ignored.

Chapter 4 Project III

4.1 System Planning

This project is divided into 5 submodules, namely drm_top (testing all DRMs), gpll_top (the VCO reaches the lower limit of 600MHz), ppll_top (the VCO reaches the lower limit of 1350MHz), dram_top (testing distributed RAMs), and apm_top (testing all APMs). The top-level module mainly performs signal synchronisation and debounce, There are a total of 10 top-level signals, as shown in the table below.

Table 4-1 Top-level Signals and Descriptions of Project III

No.	Signal Name	Input/Output	Signal Description
1	clk	Input	System clock, 25MHz
2	rst_n	Input	Asynchronous reset signal, active-low
3	error_in	Input	Error injection signal, active-high
4	drm_led	Output	DRM test state indicator. Low indicates pass, and high indicates fail.
5	apm_led	Output	APM test state indicator. Low indicates pass, and high indicates fail.
6	dram_led	Output	Distributed RAM test state indicator. Low indicates pass, and high indicates fail.
7	gpll_lock_led	Output	GPLL output frequency lock signal. High indicates pass, and low indicates fail.
8	gpll_ led	Output	GPLL output frequency test indicator. Low indicates pass, and high indicates fail.
9	ppll_lock_led	Output	PPLL output frequency lock signal. High indicates pass, and low indicates fail.
10	ppll_ led	Output	PPLL output frequency test indicator. Low indicates pass, and high indicates fail.

4.2 Functional Module Design

4.2.1 drm_top Module

Test objective: This module tests all core DRMs in the PG2L100H chip.

Test method: Instantiate GTP_DRM36K_E1, and configure the DRMs to true dual-port mode. Controlled by the reset signal, all DRMs are divided into 4 regions, tested serially; sequentially perform read-write verification on port A/B using the MARCH IC algorithm.

Error injection is supported. When the error injection signal is valid, if the expected readout value of the DRM does not match the write-in value, a verification error occurs.

4.2.2 gpll_top Module

Test objective: This module instantiates 2 GPLL modules, which VCO frequency reaches the lower limit of 600MHz, for testing the output frequency and lock signals.

Test method: Count the input reference clock and output clock separately, and test the output clock frequency based on its multiplication relationship with the input reference clock.

If the output frequency deviation exceeds the expected frequency by ±5%, the testing result is fail.

In the design, the GPLL output clock count range is calculated as follows: Suppose the input reference clock cycle is tref, and the pll output clock clkout cycle is t0, then cnt_min = (10000 * tref / t0) * 0.95, and cnt_max = (10000 * tref / t0) *1.05.

When the error injection signal is valid, the PLL is reset, the GPLL will not be locked, and the output clock counter will also be reset, indicating a clock frequency test failure.

The GPLL module test circuit is the same as in Figure 2-3.

4.2.3 ppll_top Module

Test objective: This module instantiates 2 PPLL modules, which VCO frequency reaches the lower limit of 1350MHz, for testing the output frequency and the lock signal.

Test method: Count the input reference clock and output clock separately, and test the output clock frequency based on its multiplication relationship with the input reference clock.

If the output frequency deviation exceeds the expected frequency by ±5%, the testing result is fail.

In the design, the PPLL output clock count range is calculated as follows: Suppose the input reference clock cycle is tref, and the pll output clock clkout cycle is t0, then cnt_min = (10000 * tref / t0) * 0.95, and cnt_max = (10000 * tref / t0) *1.05.

When the error injection signal is valid, the PPLL is reset, the PPLL will not be locked, and the output clock counter will also be reset, indicating a clock frequency test failure.

The PPLL module test circuit is the same as in Figure 2-3.

4.2.4 dram_test Module

Test objective: This module tests all distributed RAMs constructed by CLMS in the PG2L100H chip.

Test method: Instantiate GTP_RAM256X1SP, configure the distributed RAMs to single-port mode, with the same DIN for all distributed RAMs, and compare their outputs for consistency. The distributed RAMs use a method of writing to one address and reading from another. The compared register's reset port is valid before writing to the current address and is released after writing, so as to prevent the register from not sampling glitches.

Error injection is supported. When the error injection signal is valid, if the value written to the first distributed RAM is different from those of others,verification fails.

This test circuit structure is shown in the figure below.

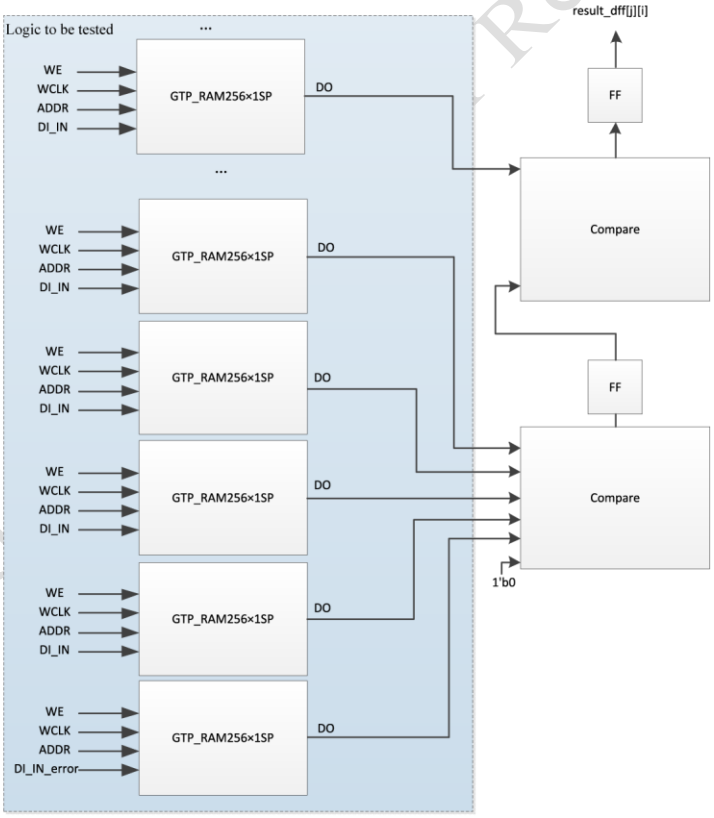

Figure 4-1 Structure Diagram of Distributed RAM Test Circuit

Resource instantiation is shown in the following figure.

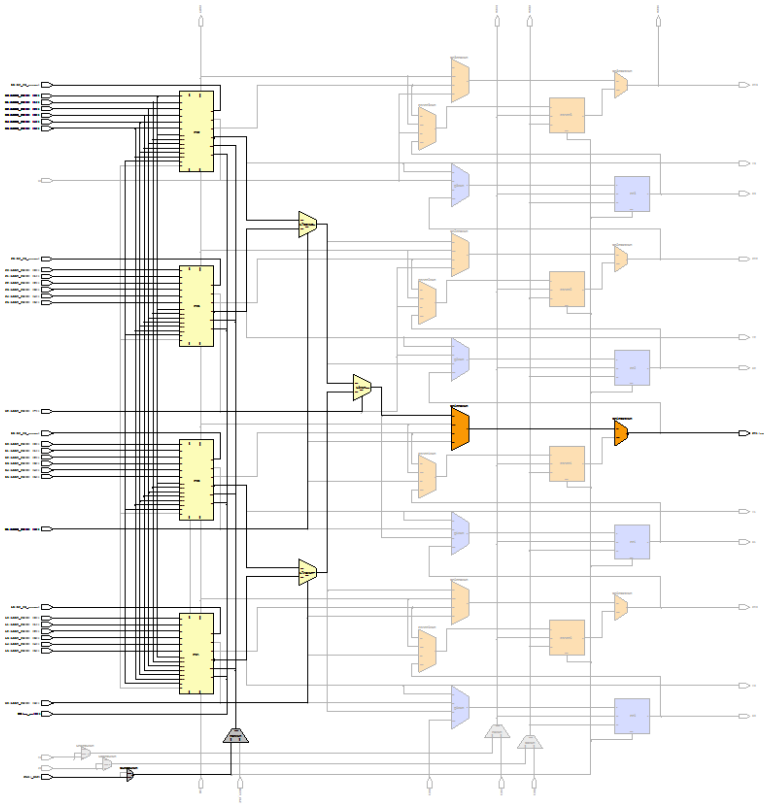

Figure 4-2 Resource Instantiation of Distributed RAMs

4.2.5 apm_top Module

Test objective: This module tests all core dedicated APMs in the PG2L100H chip.

Test method: Instantiate GTP_APM_E2, configure APMs to multiply-accumulate mode, and compare APM output values with the expected value computed by ordinary logic using XOR, with APM input data the same as ordinary logic input data.

Error injection is supported. When the error injection signal is valid, if the expected APM output value changes, verification fails.

4.3 PDS Compilation Results

In Project III, the resource usage rate after placement and routing based on PDS2021.1-SP2.1 compilation is shown in the figure below.

Logic Utilization	Used	Available	Utilization(%)
Use of ADC	0	1	0
Use of ANALOG	0	1	0
Use of APM	240	240	100
Use of BKCL	5	6	84
Use of CCS	1	1	100
Use of CLMA	4243	11675	37
FF	3458	93400	4
LUT	10742	46700	24
LUT-FF pairs	3104	46700	7
Use of CLMS	4975	4975	100
FF	3	39800	1
LUT	19900	19900	100
LUT-FF pairs	0	19900	0
Distributed RAM	19900	19900	100
Use of DDRPHY_CPD	0	12	0
Use of DDRPHY_IOCLK_DIV	0	6	0
Use of DDR_PHY	0	24	0
Use of DRM	155	155	100
Use of GPLL	2	6	34
Use of GSEB	0	218	0
Use of HARD0	1609	10550	16
Use of HCKB	15	96	16
Use of HCKMUX_TEST	0	8	0
Use of HSSTLP	0	2	0
Use of IO	10	300	4
IOBD	5	144	4
IOBS	5	156	4

Logic Utilization	Used	Available	Utilization(%)
IOBD	5	144	4
IOBS	5	156	4
Use of IOCKB	0	24	0
Use of IOCKMUX_TEST	0	6	0
Use of IOLHR	10	300	4
Use of KEYRAM	0	1	0
Use of MFG_TEST	0	1	0
Use of MRCKB	0	12	0
Use of MRCKMUX_TEST	0	6	0
Use of MRPOSTMUX_TEST	0	6	0
Use of PCIE	0	1	0
Use of PCKMUX_TEST	0	12	0
Use of PLLMRMUX_TEST	0	6	0
Use of PLLREFMUX_TEST	0	6	0
Use of PPLL	2	6	34
Use of PREGMUXC_TEST	0	4	0
Use of PREGMUXLR_TEST	0	6	0
Use of RCKB	17	24	71
Use of RCKMUX_TEST	0	6	0
Use of SCANCHAIN	0	1	0
Use of SCKMUX_TEST	0	12	0
Use of SFB	0	2225	0
Use of SPAD	0	8	0
Use of TSERDES	0	48	0
Use of USCM	6	32	19
Use of USCMMUX_TEST	0	32	0

Figure 4-3 Resource Usage Rate of Project III

The timing report of Project III is shown in the figure below.

	Clock	Fmax	Requested Frequency	Slack
1	clk	100.010MHz	50.000MHz	10.001
2	clk|u_gpll_top/GPLL[0].u_GPLL/u_gpll/CLKOUT0_Inferred	513.347MHz	40.000MHz	23.052
3	clk|u_gpll_top/GPLL[0].u_GPLL/u_gpll/CLKOUT1_Inferred	393.082MHz	75.002MHz	10.789
4	clk|u_gpll_top/GPLL[0].u_GPLL/u_gpll/CLKOUT2_Inferred	430.478MHz	150.015MHz	4.343
5	clk|u_gpll_top/GPLL[0].u_GPLL/u_gpll/CLKOUT3_Inferred	556.793MHz	300.030MHz	1.537
6	clk|u_gpll_top/GPLL[0].u_GPLL/u_gpll/CLKOUT4_Inferred	574.053MHz	300.030MHz	1.591
7	clk|u_gpll_top/GPLL[1].u_GPLL/u_gpll/CLKOUT0_Inferred	468.604MHz	40.000MHz	22.866
8	clk|u_gpll_top/GPLL[1].u_GPLL/u_gpll/CLKOUT1_Inferred	372.995MHz	75.002MHz	10.652
9	clk|u_gpll_top/GPLL[1].u_GPLL/u_gpll/CLKOUT2_Inferred	562.746MHz	150.015MHz	4.889
10	clk|u_gpll_top/GPLL[1].u_GPLL/u_gpll/CLKOUT3_Inferred	573.723MHz	300.030MHz	1.590
11	clk|u_gpll_top/GPLL[1].u_GPLL/u_gpll/CLKOUT4_Inferred	517.331MHz	300.030MHz	1.400
12	clk|u_ppll_top/PPLL[0].u_PPLL/u_ppll/CLKOUT0_Inferred	436.681MHz	45.000MHz	19.932
13	clk|u_ppll_top/PPLL[0].u_PPLL/u_ppll/CLKOUT1_Inferred	474.383MHz	90.001MHz	9.003
14	clk|u_ppll_top/PPLL[0].u_PPLL/u_ppll/CLKOUT2_Inferred	452.284MHz	135.007MHz	5.196
15	clk|u_ppll_top/PPLL[0].u_PPLL/u_ppll/CLKOUT3_Inferred	568.828MHz	270.051MHz	1.945
16	clk|u_ppll_top/PPLL[0].u_PPLL/u_ppll/CLKOUT4_Inferred	554.631MHz	270.051MHz	1.900
17	clk|u_ppll_top/PPLL[1].u_PPLL/u_ppll/CLKOUT0_Inferred	456.204MHz	45.000MHz	20.030
18	clk|u_ppll_top/PPLL[1].u_PPLL/u_ppll/CLKOUT1_Inferred	451.264MHz	90.001MHz	8.895
19	clk|u_ppll_top/PPLL[1].u_PPLL/u_ppll/CLKOUT2_Inferred	440.917MHz	135.007MHz	5.139
20	clk|u_ppll_top/PPLL[1].u_PPLL/u_ppll/CLKOUT3_Inferred	515.730MHz	270.051MHz	1.764
21	clk|u_ppll_top/PPLL[1].u_PPLL/u_ppll/CLKOUT4_Inferred	474.608MHz	270.051MHz	1.596

Figure 4-4 Timing Report of Project III

4.4 Simulation Results

The top-level signal simulation results of Project III are shown in the figure below.

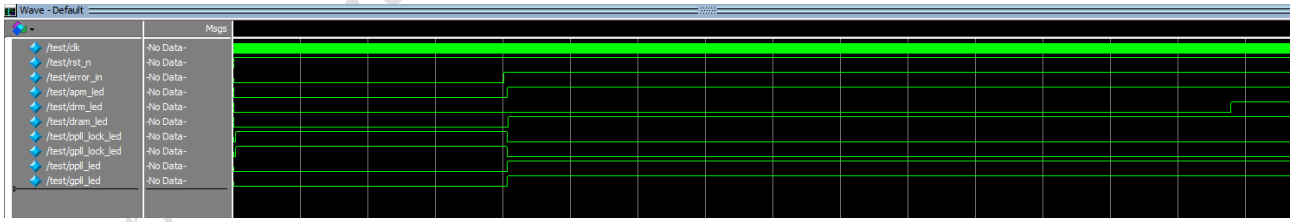

Figure 4-5 Simulation Results of Project III

4.5 On-board Test

1. Configure the bitstream, and repeatedly perform reset and un-reset tests for 1000 cycles, pass.
2. Repeatedly configure the bitstream without power-down and test for 1000 cycles, pass.
3. Configure the bitstream upon power-up, test and then power down, repeatedly test for 1000 cycles, pass.

4.6 Warning Descriptions

1. Warning for GTP can be ignored;
2. Floating signals in drm_top and apm_top modules are optimized. This warning can be ignored;
3. IO has no timing constraints, and users can make modifications as needed. This warning can be ignored;
4. If constraints are applied using fdc, the previously generated pcf in the project will be overridden. This warning can be ignored.

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