PK03023_PGC4KL_UWG81

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.2	11.04.2021	Initial release

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
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Chapter 1 Introduction to Packaging

The PGC4KL_UWG81 device is packaged with WLCSP wafer-level chip. Its package size is 3.866x3.643mm, with 81 solder balls, a pitch of 0.4mm between the balls and a maximum package thickness of 0.576mm.

Chapter 2 Package Dimension and Pins

2.1 Package Outline Dimension

Table 2-1 Dimensional Data

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
D	3.623	3.643	3.663	A	0.510	0.543	0.576
D1	–	3.20	–	A1	0.157	0.175	0.193
E	3.846	3.866	3.886	A2	0.343	0.368	0.393
E1	–	3.20	–	e	–	0.4	–
b	0.207	0.23	0.253				

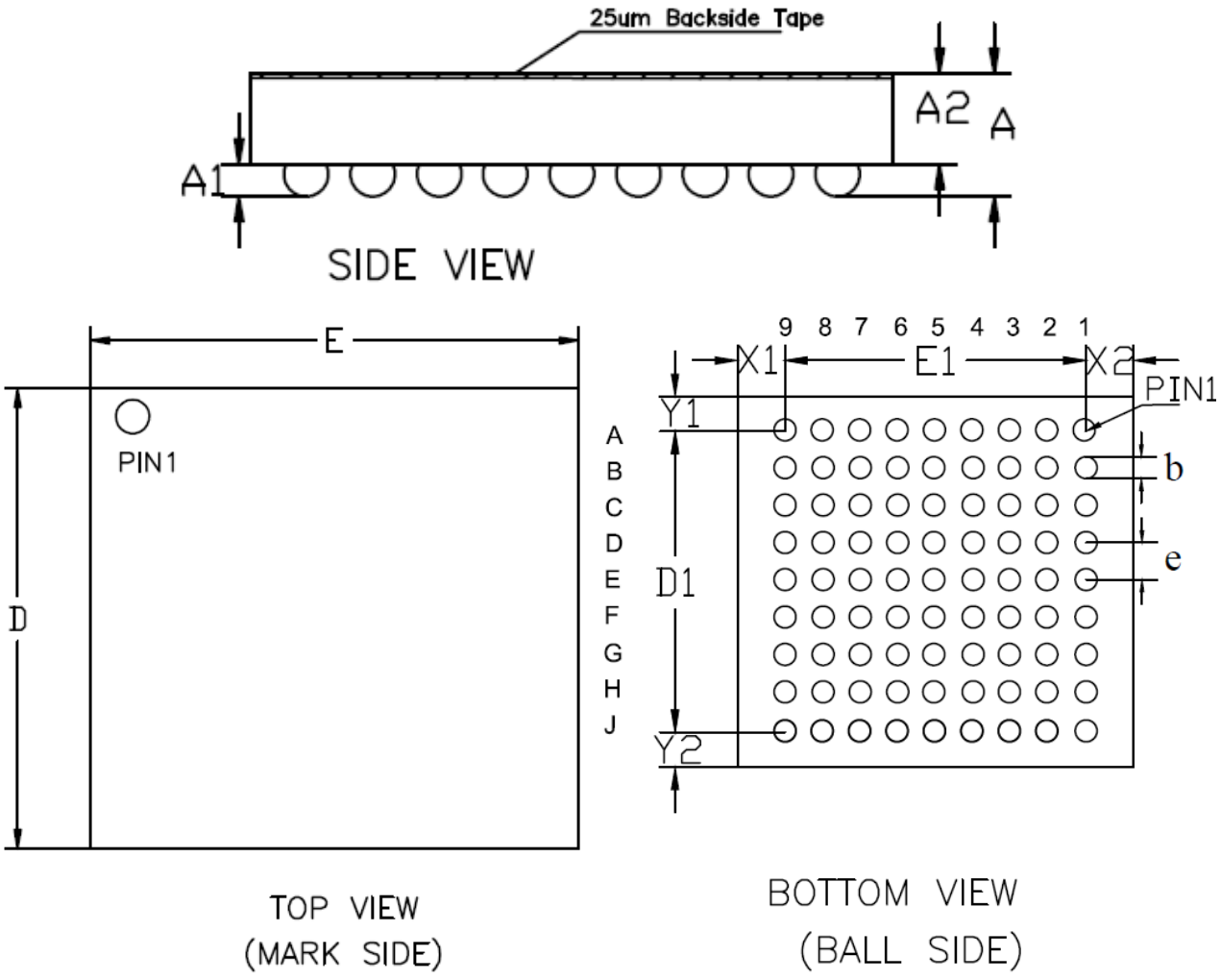

Figure 2-1 Package Outline Dimension (POD)

2.2 Pin Description

The PGC4KL_UWG81 device has 64 user I/Os.

Table 2-2 Device Pin Definitions

Pin Name	Pin Type	Direction	Pin Description
User I/O Pin			
DIFF[I,IO]_XX_NN[P,N]	User pin	Input/Output	User I/O. (1) DIFFI indicates support for differential signal input and pseudo-differential output; DIFFIO indicates support for differential signal input and true differential output, which can be used for transmitting and receiving LVDS signals; (2) “XX” denotes the Bank number, with possible values being B0, B1, B2, B3, B4, and B5; (3) “NN” denotes the sequence number of the programmable I/O group within the Bank, starting from 0 and increasing incrementally; (4) [P,N]: “P” denotes the positive side of the differential pair, and “N” denotes the negative side; During power-up, the user I/O is at a low voltage; After power-up is complete but before configuration, the general user I/O is at pull-down status; During configuration, the user I/O is at pull-down status;
Configuration[1]			
INIT_FLAG_N	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, with an internal weak pull-up resistor. When used as a configuration pin: During power-up, it is at a low voltage; After power-up is complete before configuration, it is open-drain at weak pull-up status; During configuration, it is open-drain at weak pull-up status; During initialization, the pin can be driven to a low voltage by an external input to indicate an error or to delay configuration. During configuration, the pin serves as an indicator output for configuration errors, where a low voltage indicates an error has occurred;
CFG_DONE	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, with an internal weak pull-up resistor. When it is used as configuration pin, it serves as an indicator output for configuration completion, where a high voltage indicates configuration is complete; Before or during configuration, the pin is driven to a low voltage; after configuration is complete, the pin can continue to be driven to a low voltage by an external source. If the internal start-up timing detects CFG_DONE at a low voltage, the internal start-up circuitry maintains its state until CFG_DONE goes high to continue the start-up process;
RSTN	Multi-function pin	Input	Configurable multiplexed reset pin, with an internal weak pull-up resistor. When it is used as a reset pin, it serves to restart the configuration process, active low. At this situation, it must be pulled up with an external resistor (internal weak pull-up resistor typically has a value of over 20kOhms, with a relatively weak pull-up strength); when the pin is at a low voltage, the CPLD enters reset state, with all I/Os in a weak pull-down status;

Pin Name	Pin Type	Direction	Pin Description
CFG_CLK	Multi-function pin	Input/Output	Configurable multiplexed clock pin, with an internal weak pull-up resistor. When it is used as a configuration pin: In slave SPI configuration mode, the pin serves as a clock input to acquire configuration data from an external source; In master SPI configuration mode, the pin serves as a clock output to acquire configuration data from an external source; in this mode, a 1kOhms pull-up resistor is needed; Master SPI mode and slave SPI mode are allowed to be enabled simultaneously, but using them at the same time is not permitted;
TCK	Multi-function pin	Input	Multiplexed JTAG test clock input pin; requires an external 4.7kOhms pull-down resistor;
TMS	Multi-function pin	Input	Multiplexed JTAG test mode select input pin; with an internal weak pull-up resistor, pulled up to VCCIO0;
TDI	Multi-function pin	Input	Multiplexed JTAG test data input pin; with an internal weak pull-up resistor, pulled up to VCCIO0;
TDO	Multi-function pin	Output	Multiplexed JTAG test data output pin; with an internal weak pull-up resistor, pulled up to VCCIO0.
JTAGEN	Multi-function pin	Input	Optional JTAG port behaviour control pin, usually used in user mode, when JTAG pins are configured as configuration I/Os, this pin is user I/O, with the state controlled by the user; when JTAG pins serve as user I/Os, JTAGEN serves as a dedicated input used to control the availability of JTAG pins; the default state is weak pull-down; when JTAGEN is configured as a dedicated I/O: (1) When at a low voltage, the JTAG pins function as user I/Os; (2) When at a high voltage, the JTAG pins function as JTAG configuration port.
FCS_N	Multi-function pin	Output	Configurable multiplexed pin, used for master SPI configuration mode, (1) In master SPI mode, outputs an active-low chip select signal to an external Flash; (2) After configuration is completed, it can be used as a user I/O.
MISO_SO	Multi-function pin	Input/Output	Configurable multiplexed pin; (1) MISO, serial data input in master SPI mode; (2) SO, serial data output in slave SPI mode; Master and slave SPI modes are allowed to be enabled simultaneously, but using them at the same time is not permitted.
MOSI_SI	Multi-function pin	Input/Output	Configurable multiplexed pin; (1) MOSI, serial data output in master SPI mode; (2) SI, serial data input in slave SPI mode; Master and slave SPI modes are allowed to be enabled simultaneously, but using them at the same time is not permitted.
FCSI_N	Multi-function pin	Input	Configurable multiplexed pin, with an internal weak pull-up resistor; In slave SPI mode, active-low chip select input.
SCL	Multi-function pin	Input (Open-dra	Configurable multiplexed pin, clock input in slave I2C mode; requires an external weak pull-up resistor.

Pin Name	Pin Type	Direction	Pin Description
		in)	
SDA	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, data input/output in I2C mode; requires an external weak pull-up resistor.
SPAL_CLK	Multi-function pin	Input	Clock input in slave parallel X16 configuration mode.
SPAL_CS_N	Multi-function pin	Input	Chip select input in slave parallel X16 configuration mode. Active-low
SPAL_RDWR_N	Multi-function pin	Input	Read/write control input in slave parallel X16 configuration mode; 1: read; 0: write.
SPAL_BUSY	Multi-function pin	Output	Busy indicator in slave parallel X16 configuration mode; During readback, if the data is not ready, SPAL_BUSY changes to high voltage.
SPAL_D15~SPAL_D0	Multi-function pin	Input/Output	Data bus in slave parallel X16 configuration mode.
Clock, PLL			
CLK[0,1,2][P,N]_[B0,…,B5]	Multi-function pin	Input	Global clock input pin; can also be used as user I/O; (1) [0,1,2]: clock pin numbers; (2) [P,N]: positive and negative sides of the differential clock pins; (3) [B0,B1,…,B5]: bank numbers.
PLL[0,1]_CLKIN_[P,N]	Multi-function pin	Input	PLL input. PLL can choose to directly input a clock from these pins; they can also be used as user I/Os; (1) [0,1]: corresponds to PLL0 and PLL1; (2) [P,N]: positive and negative sides of the differential clock pins.
PLL[0,1]_CLKFB_[P,N]	Multi-function pin	Input	Optional PLL feedback clock input. PLL can select to feedback clock externally from these pins; they can also be used as user I/Os; (1) [0,1]: corresponds to PLL0 and PLL1; (2) [P,N]: positive and negative sides of the differential clock pins.
Power			
VCC		Power	External power supply of 1.2V, providing power to the core logic.
VCCIO[0,2,3,5]		Power	I/O Bank power.
VSS		Ground	Ground associated with VCC;
MIPI_CTRL	Dedicated		MIPI high-performance application control pin; when connected to 2.5V or 3.3V, the device supports high-performance MIPI transmission functions; when connected to VSS or left floating, the device does not support the high-performance MIPI transmission capabilities.

Note:

1. When the configured multi-function pin is used as a user I/O, its status is the same as the user I/O pin.

2.2.1 Pin Name list

Table 2-3 Pin Name List

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B0	DIFFI_B0_0N/CFG_DONE	B1	IO_1_N	9.30398
B0	DIFFI_B0_0P/INIT_FLAG_N	C1	IO_1_P	8.53257
B0	DIFFIO_B0_3N/SPAL_RDWR_N	B2	IO_4_N	6.19289
B0	DIFFIO_B0_3P/SPAL_BUSY	A2	IO_4_P	4.63408
B0	DIFFIO_B0_7N/SPAL_D13	E1	IO_8_N	16.1449
B0	DIFFIO_B0_7P/SPAL_D12	F1	IO_8_P	16.4335
B0	DIFFIO_B0_9N/SPAL_D9	A3	IO_10_N	4.7683
B0	DIFFIO_B0_9P/SPAL_D8	B3	IO_10_P	6.1913
B0	DIFFI_B0_10N/RSTN	C2	IO_11_N	10.3087
B0	DIFFI_B0_10P/JTAGEN	D2	IO_11_P	11.384
B0	DIFFIO_B0_13N/SPAL_D5	E2	IO_14_N	16.3487
B0	DIFFIO_B0_13P/SPAL_D4	F2	IO_14_P	16.7424
B0	DIFFIO_B0_15N/SPAL_D3	B4	IO_16_N	10.3392
B0	DIFFIO_B0_15P/SPAL_D2	C3	IO_16_P	11.657
B0	DIFFI_B0_16N/SDA/CLK0N_B0	B5	IO_17_N	7.61531
B0	DIFFI_B0_16P/SCL/CLK0P_B0	A5	IO_17_P	6.89111
B0	DIFFIO_B0_19N	D3	IO_20_N	16.3852
B0	DIFFIO_B0_19P	E3	IO_20_P	18.4603
B0	DIFFIO_B0_21N/CLK1N_B0	B6	IO_22_N	7.69101
B0	DIFFIO_B0_21P/CLK1P_B0	A6	IO_22_P	6.92237
B0	DIFFI_B0_22N/TMS	D4	IO_23_N	15.6366
B0	DIFFI_B0_22P/TCK	E4	IO_23_P	13.1346
B0	DIFFI_B0_26N/TDI	A7	IO_27_N	5.84008
B0	DIFFI_B0_26P/TDO	B7	IO_27_P	8.88168
B0	DIFFIO_B0_31N	B8	IO_32_N	7.29111
B0	DIFFIO_B0_31P	A8	IO_32_P	5.37862
B0	DIFFIO_B0_33N	C6	IO_34_N	15.8104
B0	DIFFIO_B0_33P	D5	IO_34_P	15.1907
B0	DIFFIO_B0_35N	D6	IO_36_N	12.9297
B0	DIFFIO_B0_35P	D7	IO_36_P	10.5629
B2	DIFFI_B2_1N/MOSI_SI	H1	IO_86_N	10.2663
B2	DIFFI_B2_1P/FCSI_N	G1	IO_86_P	10.0235
B2	DIFFI_B2_5N	J2	IO_90_N	5.59938
B2	DIFFI_B2_5P	H2	IO_90_P	6.70158
B2	DIFFI_B2_9N	J3	IO_94_N	4.50244
B2	DIFFI_B2_9P	H3	IO_94_P	5.39665

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B2	DIFFI_B2_11N	G2	IO_96_N	10.1114
B2	DIFFI_B2_11P	G3	IO_96_P	8.2004
B2	DIFFI_B2_15N/CLK1N_B2	H4	IO_100_N	8.01432
B2	DIFFI_B2_15P/CLK1P_B2	G4	IO_100_P	8.22285
B2	DIFFI_B2_19N	J5	IO_104_N	6.3703
B2	DIFFI_B2_19P	H5	IO_104_P	6.47003
B2	DIFFI_B2_21N/CLK0N_B2	H6	IO_106_N	6.76784
B2	DIFFI_B2_21P/CLK0P_B2	J6	IO_106_P	4.84766
B2	DIFFI_B2_27N/MISO_SO	J7	IO_112_N	4.43218
B2	DIFFI_B2_27P/CFG_CLK	H7	IO_112_P	5.87413
B2	DIFFI_B2_29N	G7	IO_114_N	10.1997
B2	DIFFI_B2_29P	H8	IO_114_P	8.44955
B2	DIFFI_B2_33N	J8	IO_118_N	6.68513
B2	DIFFI_B2_33P/FCS_N	H9	IO_118_P	6.66941
B3	DIFFI_B3_0P	F8	IO_127_P	9.75961
B3	DIFFI_B3_0N	F7	IO_127_N	9.96959
B3	DIFFI_B3_2P	F6	IO_129_P	11.9933
B3	DIFFI_B3_4P/CLK0P_B3	G9	IO_131_P	4.79835
B3	DIFFI_B3_4N/CLK0N_B3	G8	IO_131_N	5.79225
B3	DIFFI_B3_6P	F5	IO_133_P	15.828
B3	DIFFI_B3_6N	F4	IO_133_N	17.4965
B5	DIFFI_B5_4P/PLL0_CLKIN_P	B9	IO_157_P	8.95874
B5	DIFFI_B5_4N/PLL0_CLKIN_N	C8	IO_157_N	7.97998
B5	DIFFI_B5_6P	D8	IO_159_P	10.2505
B5	DIFFI_B5_10P	E6	IO_163_P	12.1941
B5	DIFFI_B5_10N	E7	IO_163_N	10.6025
B5	DIFFI_B5_13P	D9	IO_166_P	5.78377
B5	DIFFI_B5_13N	E8	IO_166_N	8.04644
	MIPI_CTRL	A9		4.47123
	VCC	C4		
	VCC	D1		
	VCC	E9		
	VCC	F3		
	VCCIO0	A4		
	VCCIO0	C5		
	VCCIO0	C7		
	VCCIO2	G6		
	VCCIO2	J4		
	VCCIO3	F9		

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
	VCCIO5	C9		
	VSS	A1		
	VSS	E5		
	VSS	G5		
	VSS	J1		
	VSS	J9		

2.3 Soldering Temperature Profile

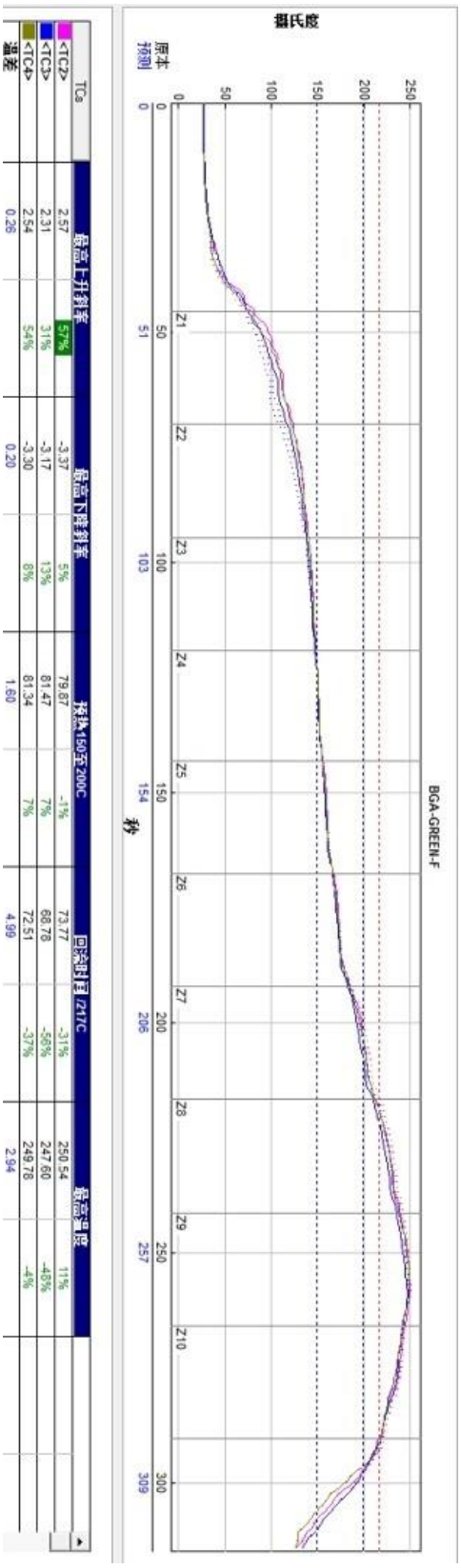

Figure 2-2 Soldering Temperature Profile

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