Logos Family PGL25G Device Configurable Multi-function PINs Application Guide

(AN02018, V1.1)

(17.11.2022)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.1	17.11.2022	Initial release.

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Chapter 1 Overview

A configurable multi-function PIN can be used as a configuration interface during the configuration, and after the completion of the configuration, it can be used as a standard IO for the user in user mode. Some considerations on using a configurable Multi-function PIN as a user IO shall be taken into account in the single board design. The configurable multi-function PINs are all on Bank0, Bank1, or Bank2. See details in Table 2-1 and Table 2-2. So there is no need to consider the application of configurable multi-function IOs in other banks.

Configurable multi-function PINs must be used according to the special notes to avoid the following problem scenario: When reconfiguring the FPGA by resetting it in user mode and using a configurable multi-function PIN as an output for user logic, then after resetting, the multi-function PIN output will be in a non-high impedance state for a short term period (less than 100ns) (some PINs at a high level and some at a low level) and not controlled by IO_STATUS_C.

The process is shown in the following figure:

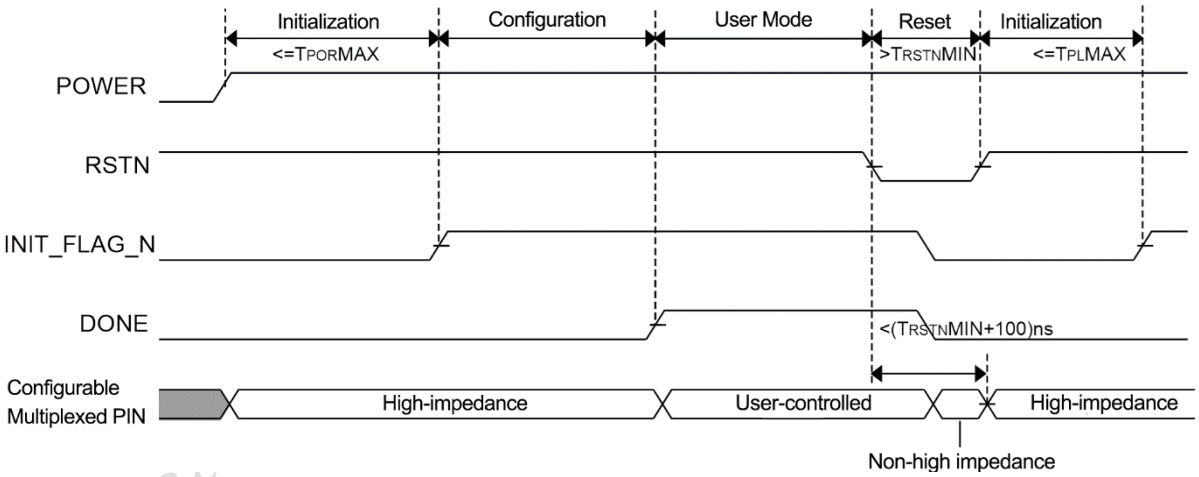

Figure 1-1 Non-High Impedance Process Diagram

For parameters in Figure 1-1, see "***DS02001_Logos Family FPGA Device Datasheet***" under the Chapter "Power-up Timing Characteristics".

This scenario mainly affects applications that require IO to maintain a fixed level during the reconfiguration process. For example, a configurable multi-function PIN is used as the enable or reset signal for other devices, and an external pull-up (or pull-down) of the FPGA is applied to keep the signal level stable during the configuration. In this case, it is expected that after the FPGA is reset, the configurable multi-function PIN output will be in a high impedance state, but the existence of the non-high impedance process may cause changes to the enable or reset signal, affecting the operation of other devices.

The possible triggers include:

1. Resetting FPGA in user mode
2. When resetting the FPGA, a configurable multi-function PIN is used as a user output. The following solutions are provided for single board design for this scenario.

Chapter 2 Requirements for Single Board Design

The design requirements are the following:

1. If a configurable multi-function PIN is used as an input in user mode, it will not affect the design.
2. If a configurable multi-function PIN is used as an output in user mode, the following notes must be observed.
   1) Pin IO_STATUS_C requires an external pull-up.
   2) If the configurable multi-function PIN used needs to be maintained at a fixed level during the configuration, select pins using the following method: For a fixed high level, choose pins from Table 2-1 and apply an external pull-up (A pull-up resistor of 4.7K is recommended); for a fixed low level, choose pins from Table 2-2 and apply an external pull-down (A pull-down resistor of 4.7K is recommended). If the rules of Table 2-1 and Table 2-2 are not followed, the configurable multi-function PIN output may be abnormal.

      For example: When using PGL25G-FBG256, if a signal needs to remain at a high level during the reconfiguration, users can choose pins such as M15 (BFCE_N) and M16 (BFOE_N), and connect an external pull-up resistor; if a signal needs to remain at a low level during the reconfiguration, users can choose E13 (ADR25), E12 (ADR24), etc., and apply an external pull-down.

      If there is no need for the FPGA to maintain a fixed level during the reconfiguration, no action is required.

Table 2-1 Configurable Multi-function PINs that Can Remain at a High Level during Configuration

Bank Name	Pin Name (Function name)	Pin Number		
		FBG256	MBG324	FBG484
B0	DIFFIO_B0_0P/IO_STATUS_C	C4	D4	A3
B1	DIFFI_B1_25P/BFCE_N	M15	L17	M21
B1	DIFFI_B1_25N/BFOE_N	M16	L18	M22
B1	DIFFI_B1_26P/BFWE_N	L14	M16	N20
B1	DIFFI_B1_28P/BHDC	P15	N17	P21
B2	DIFFIO_B2_0N/CSO_N	T3	V3	T5
B2	DIFFIO_B2_12N/RWSEL/VREF_B2	T5	T5	AB7
B2	DIFFIO_B2_23N/GCLK0/ECCLK/PLL2_CLK4/PLL3_CLK4	T8	V10	AB13
B2	DIFFIO_B2_33P/MODE_1	N11	N12	U15
B2	DIFFIO_B2_39N/MODE_0	T11	T15	AA22
B2	DIFFIO_B2_39P/CFG_CLK	R11	R15	Y21

Table 2-2 Configurable Multi-function PINs that Can Remain at a Low Level during Configuration

Bank Name	Pin Name (Function name)	Pin Number		
		FBG256	MBG324	FBG484
B1	DIFFI_B1_0P/ADR25	E13	F15	C19
B1	DIFFI_B1_0N/ADR24/VREF_B1	E12	F16	B20
B1	DIFFI_B1_7P/ADR23	B15	C17	D19
B1	DIFFI_B1_7N/ADR22	B16	C18	D20
B1	DIFFI_B1_8P/ADR21	F12	F14	F18
B1	DIFFI_B1_8N/ADR20	G11	G14	F19
B1	DIFFI_B1_9P/ADR19	D14	D17	D21
B1	DIFFI_B1_9N/ADR18	D16	D18	D22
B1	DIFFI_B1_10P/ADR17	F13	H12	C20
B1	DIFFI_B1_10N/ADR16	F14	G13	C22
B1	DIFFI_B1_11P/ADR15	C15	E16	G19
B1	DIFFI_B1_11N/ADR14	C16	E18	F20
B1	DIFFI_B1_12P/ADR13	E15	K12	H19
B1	DIFFI_B1_12N/ADR12	E16	K13	H18
B1	DIFFI_B1_13P/ADR11	F15	F17	E20
B1	DIFFI_B1_13N/ADR10	F16	F18	E22
B1	DIFFI_B1_14P/ADR9	G14	H13	J17
B1	DIFFI_B1_14N/ADR8	G16	H14	K17
B1	DIFFI_B1_15P/ADR7	H15	H15	F21
B1	DIFFI_B1_15N/ADR6	H16	H16	F22
B1	DIFFI_B1_16P/ADR5	G12	G16	H20
B1	DIFFI_B1_16N/ADR4	H11	G18	J19
B1	DIFFI_B1_23P/ADR3	K15	J16	K21
B1	DIFFI_B1_23N/ADR2	K16	J18	K22
B1	DIFFI_B1_24P/ADR1	N14	K17	L20
B1	DIFFI_B1_24N/ADR0	N16	K18	L22
B1	DIFFI_B1_26N/BLDC	L16	M18	N22
B1	DIFFI_B1_39N/DOUT_BUSY	M14	P16	T20
B2	DIFFIO_B2_0P/INIT_FLAG_N	R3	U3	T6
B2	DIFFIO_B2_1N/D9	N6	P6	AB2
B2	DIFFIO_B2_1P/D8	M6	N5	AA2
B2	DIFFIO_B2_3N/D6	L7	T3	Y4
B2	DIFFIO_B2_3P/D5	L8	R3	W4
B2	DIFFIO_B2_11N/D4	P5	V5	AB6
B2	DIFFIO_B2_11P/D3	N5	U5	AA6
B2	DIFFIO_B2_12P/D7	R5	R5	Y7
B2	DIFFIO_B2_22N/GCLK30/D15/PLL2_CLK2/PLL3_CLK2	M7	T8	AB12

Bank Name	Pin Name (Function name)	Pin Number		
		FBG256	MBG324	FBG484
B2	DIFFIO_B2_22P/GCLK31/D14/PLL2_CLK3/PLL3_CLK3	P7	R8	AA12
B2	DIFFIO_B2_23P/GCLK1/D13/PLL2_CLK5/PLL3_CLK5	P8	U10	Y13
B2	DIFFIO_B2_32N/D12	P9	V13	AB18
B2	DIFFIO_B2_32P/D11	N9	U13	AA18
B2	DIFFIO_B2_33N/D10	P11	P12	V15
B2	DIFFIO_B2_34N/D2	P12	V14	U13
B2	DIFFIO_B2_34P/D1	N12	T14	U14
B2	DIFFIO_B2_37N/CS_N	T10	T13	AB20
B2	DIFFIO_B2_37P/D0	P10	R13	AA20

Users must verify based on the application to ensure that the pin meets application requirements at each stage.

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