ADC IP

User Guide

(UG041005, V1.7)

(28.04.2024)

Revisions History

Document Revisions

Version	Date of Release	Revisions	Applicable IP and Corresponding Versions
V1.7	28.04.2024	Initial release.	V1.7

IP Revisions

IP Version	Date of Release	Revisions
V1.7	28.04.2024	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
ADC	Analog-to-Digital Converter
IPC	IP Compiler
PDS	Pango Design Suite

Related Documentation

The following documentation is related to this manual:

1. ***Pango_Design_Suite_Quick_Start_Tutorial***
2. ***Pango_Design_Suite_User_Guide***
3. ***IP_Compiler_User_Guide***
4. ***Simulation_User_Guide***
5. ***User_Constraint_Editor_User_Guide***
6. ***Physical_Constraint_Editor_User_Guide***
7. ***Route_Constraint_Editor_User_Guide***
8. ***UG040009_Logos2 Family FPGAs Analog-to-Digital Conversion (ADC) Module User Guide***
9. ***UG050009_Titan2 Family FPGAs Analog-to-Digital Conversion (ADC) Module User Guide***
10. ***UG100009_Kosmo2 Family SOPC Analog-to-Digital Conversion (ADC) Module User Guide***

Table of Contents

Tables

Figures

Chapter 1 Preface

This chapter describes the scope, structure, and writing standards of this manual to help users quickly find the information they need.

1.1 Introduction of the Manual

This manual serves as a user guide for the ADC IP launched by Pango Microsystems, primarily including the IP user guide and related information. The manual helps users quickly understand the features and usage of ADC IP.

1.2 Writing Standards of the Manual

Table 1-1 Description of Writing Standards

Text	**Rules**
Attention	If users ignore the attention contents, they may suffer adverse consequences or fail to operate successfully due to incorrect actions.
Description	Instructions and tips provided for users.
Recommendation	Recommended settings and instructions for users.

Chapter 2 IP User Guide

This chapter provides a guide on the use of ADC IP, including an introduction to IP, IP block diagram, IP generation process, Example Design, IP interface description, IP register description, typical applications, instructions and considerations, and IP debugging methods. More details on the design process can be found in the following PDS help documentation.

- "***Pango_Design_Suite_Quick_Start_Tutorial***"
- "***Pango_Design_Suite_User_Guide***"
- "***IP_Compiler_User_Guide***"
- "***Simulation_User_Guide***"

2.1 IP Introduction

ADC IP is an IP designed by Pango Microsystems based on ADC hardware resources that can achieve relevant control and status by on-chip ADC modules. Users can configure and generate the IP module using the IPC (IP Compiler) tool within the PDS (Pango Design Suite).

2.1.1 Key Features

- Supports operating mode options: Power Up Mode, Scan Sequence Mode;
- Supports sampling mode options: Event_drive, Continuous;
- Supports voltage reference source options: On-chip, External;
- Supports sampling clock, sampling frequency configuration;
- Supports calibration control configuration: NONE, Offset Correction Only, Offset and Gain Correction;
- Supports ADC power-down configuration: NONE, ADCB Power Down Only, ADCA and ADCB Power Down;
- Supports sampling averaging times configuration: NONE, 16, 64, 256;
- Supports dedicated channel scan configuration: ADCA, ADCB;
- Supports configuration for channel enable;

- Supports external channel mode configuration: Unipolar, Bipolar[1];
- Supports temperature/voltage monitoring alarm configuration.

2.1.2 Applicable Devices and Packages

Table 2-1 ADC IP Applicable Devices and Packages

Applicable Devices	**Supported Packages**
PG2L25H	ALL
PG2L50H	ALL
PG2L100H	ALL
PG2L100HX	ALL
PG2L200H	ALL
PG2T390H	ALL
PG2T390HX	ALL
PG2K400	ALL

1 PG2L100H does not support switching input mode configuration during multiple-channel scaning.

2.2 IP Block Diagram

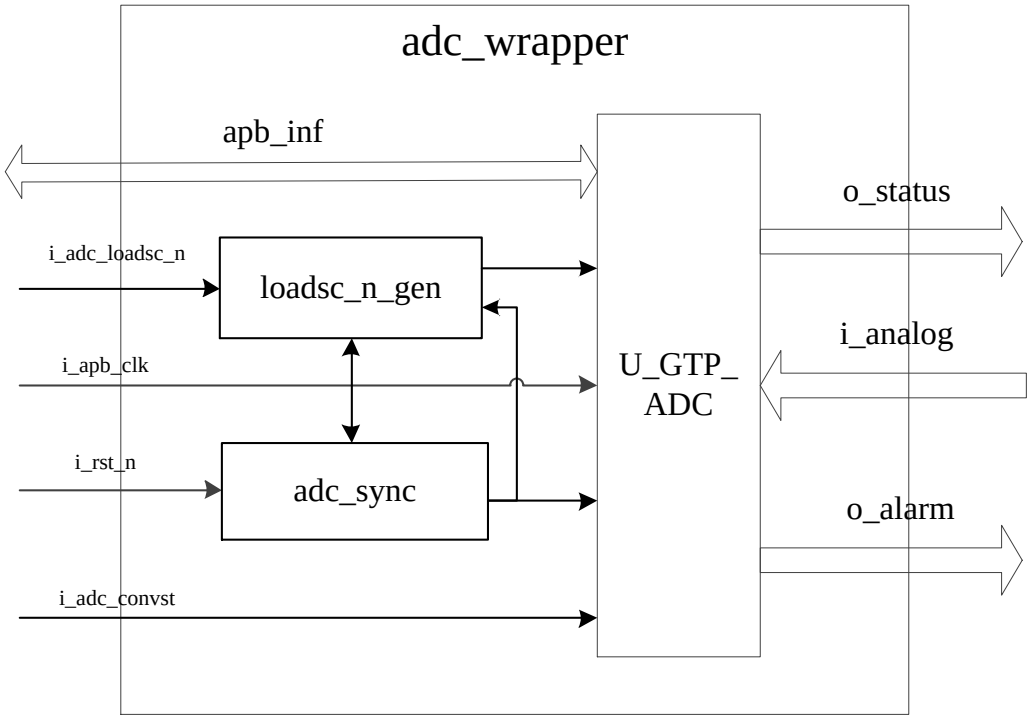

Figure 2-1 ADC IP System Block Diagram

The ADC IP system block diagram is shown in Figure 2-1, and it consists of three parts: U_GTP_ADC, loadsc_n_gen, and adc_sync.

- U_GTP_ADC is an ADC hard core module that provides ADC hard core resources and related interfaces.
- The loadsc_n_gen module processes i_adc_loadsc_n and sends it to the ADC hard core module.
- The adc_sync module synchronises the reset signal input by the user, serving as the reset signal for the ADC IP.

2.3 IP Generation Process

2.3.1 Module Instantiation

Users can customise the configuration of ADC IP through the IPC tool to instantiate the required IP modules. For detailed instructions on using the IPC tool, please refer to "***IP_Compiler_User_Guide***".

The main steps for instantiating the ADC IP module are described as follows.

2.3.1.1 Selecting IP

Open IPC and click File > Update in the main window to open the Update IP dialog box, where you add the corresponding version of the IP model.

After selecting the device type, the Catalog interface displays the loaded IP models. Select the corresponding ADC IP version under the "System/ADC" directory. The IP selection path interface is shown in Figure 2-2 Then set the Pathname and Instance Name on the right side of the page. The project instantiation interface is shown in Figure 2-3

Attention:

PG2L25H, PG2L50H: The software version must be 2022.1 or above.

PG2L100H, PG2T390H: The software version must be 2021.4-SP2, 2022.1 or above.

PG2L100HX, PG2T390HX: The software version must be 2023.1 or above.

PG2L200H: The software version must be 2022.2 or above.

PG2K400: The software version must be 2023.2 or above.

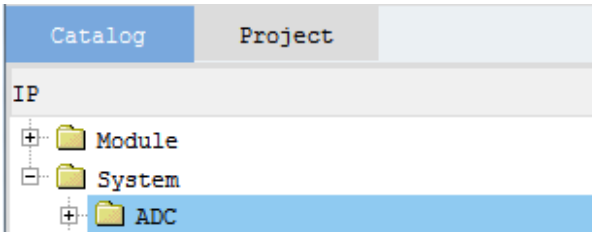

Figure 2-2 ADC IP Selection Path

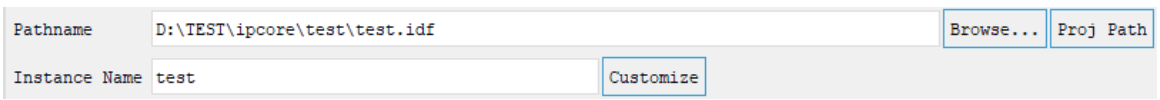

Figure 2-3 Project Instantiation Interface

2.3.1.2 IP Parameter Configuration

After selecting the IP, click <Customize> to enter the ADC IP parameter configuration interface. The left Symbol is the interface block diagram, as shown in Figure 2-4; the Parameter Configuration window is shown on the right side, as shown in Figure 2-5.

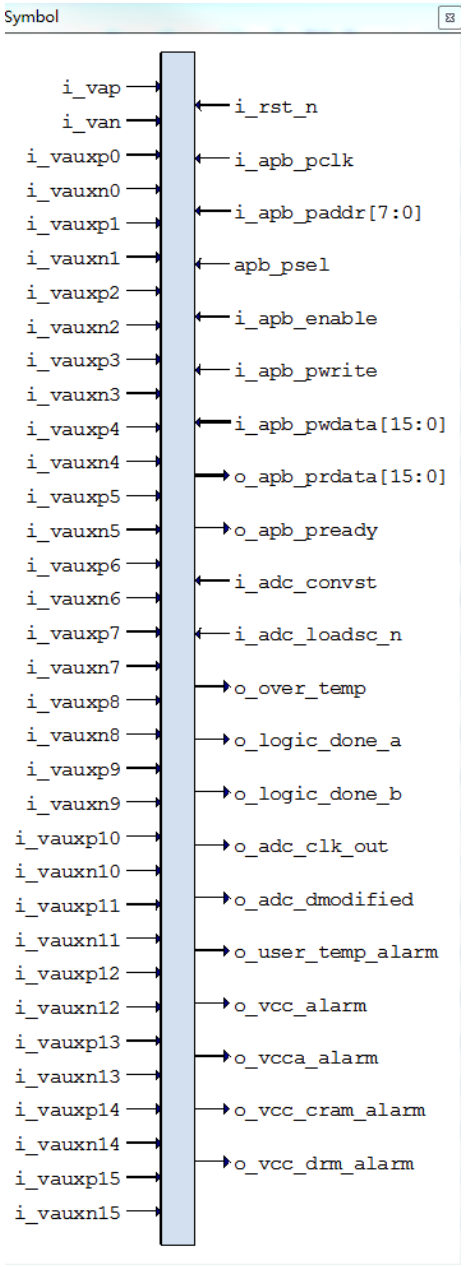

Figure 2-4 Block Diagram of the ADC IP Interfaces

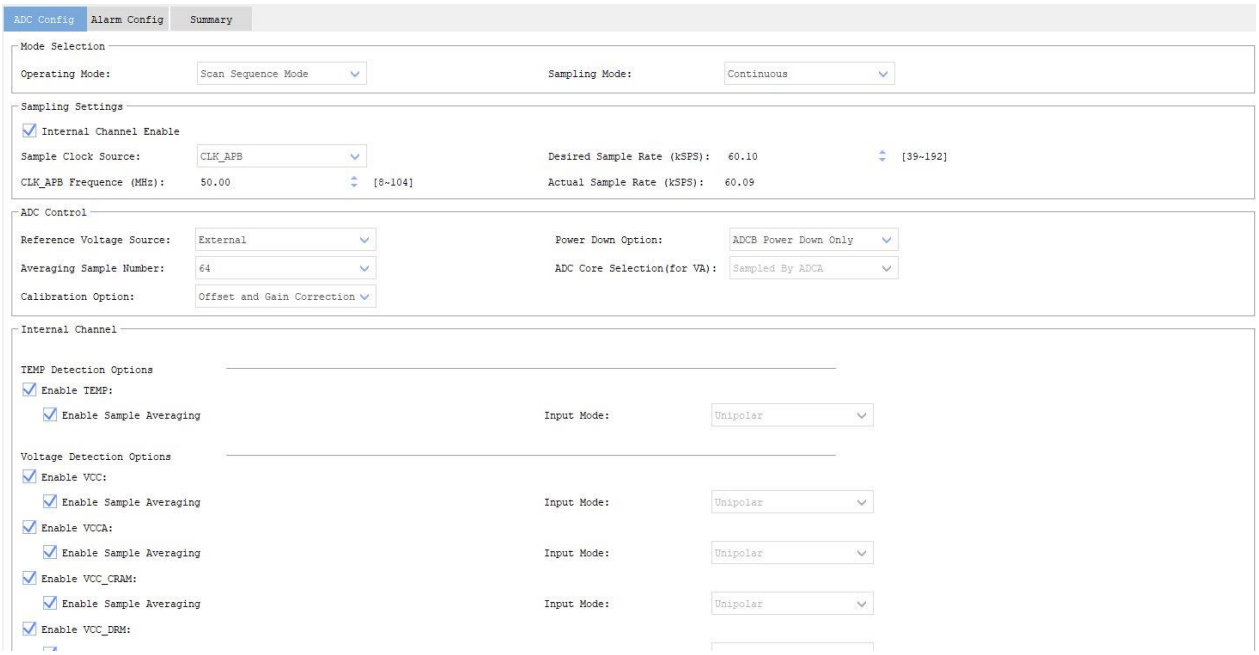

Figure 2-5 ADC IP Parameter Configuration Interface

The ADC IP parameter configuration is divided into three pages: ADC Config, Alarm Config, and Summary. The configuration parameters for each page are described as follows.

2.3.1.2.1 ADC Config

ADC Config is the configuration page for the ADC parameters, as shown in Figure 2-6. Refer to Table 2-2 for detailed parameters.

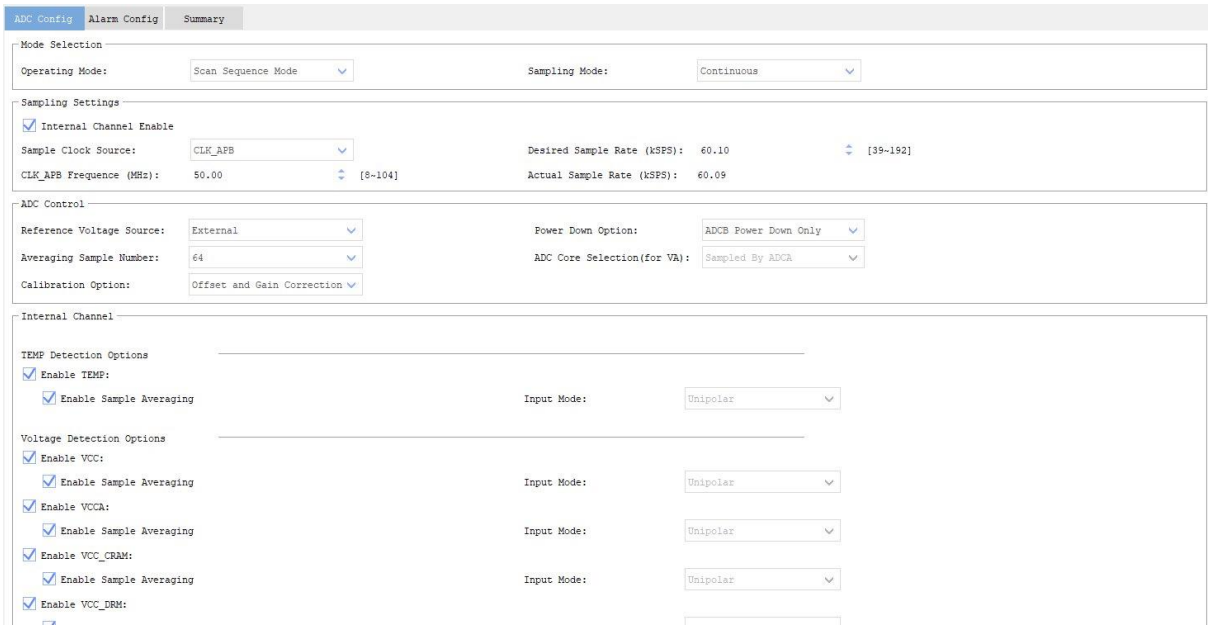

Figure 2-6 ADC Config Page

Table 2-2 Descriptions of Configuration Parameters on the ADC Config Page

Option Domain	**Parameter/Configuration Options**	**Parameter Description**	**Default Value**
Mode Selection	Operating Mode	ADC Operating Mode Selection Power Up Mode: ADC default configuration Scan Sequence Mode: User defined channel scanning Please refer to "2.8.3 Operating Modes" for details.	Scan Sequence Mode
	Sampling Mode	ADC Sampling Mode Selection Continuous: Continuous sampling Event_drive: Active control sampling Please refer to "2.8.9 Sampling Mode Descriptions" for details.	Continuous

Option Domain	Parameter/Configuration Options	Parameter Description	Default Value
Sampling Settings	Internal Channel Enable	Internal channel enable control Selected: Configurable internal channel enable Cleared: All internal channels disabled	Selected
	Sample Clock Source	Sampling clock selection CLK_OSC: Internal OSC clock CLK_APB: APB clock	CLK_APB
	Desired Sample Rate (kSPS)	User-expected sampling rate setting[2]	60.10
	CLK_APB Frequency (MHz)	Frequency setting of APB clock	50.00
	Actual Sample Rate (kSPS)	Display of the actual ADC sampling frequency	-
ADC Control	Reference Voltage Source	ADC voltage reference source setting On-chip: on-chip External: external	External
	Power Down Option	ADC power-down mode setting NONE: None power-down ADCB Power Down Only: ADCB power-down ADCA and ADCB Power Down: Both power-down	ADCB Power Down Only
	Averaging Sample Number	Setting the averaging times of ADC channel NONE: Not averaging 16: 16 times of averaging 64: 64 times of averaging 256: 256 times of averaging	64
	ADC Core Selection (for VA)	VA scan configuration for dedicated channel Sampled By ADCA: ADCA scan Sampled By ADCB: ADCB scan	Sampled By ADCA
	Calibration Option	ADC calibration mode configuration NONE: No calibration Offset Correction Only: Offset correction only Offset and Gain Correction: Offset and gain correction	Offset and Gain Correction
Input Mode Setting[3]	ADCA	Input mode selection for ADCA sampling channel Available input modes: Unipolar, Bipolar	Unipolar
	ADCB	Input mode selection for ADCB sampling channel Available input modes: Unipolar, Bipolar	Unipolar

2 The sampling frequency range is related to the configuration mode. For details, please refer to "2.8.4 Description of Sampling Frequency".

3 Only valid for PG2L100H, indicating the input mode of the channels sampled by ADCA and ADCB.

Option Domain	Parameter/Configuration Options	Parameter Description	Default Value
Internal Channel	Enable TEMP	ADC on-chip temperature detection channel enable Selected: Enabled Cleared: Disabled	Selected
	Enable VCC	Enable ADC on-chip VCC detection channel Selected: Enabled Cleared: Disabled	Selected
	Enable VCCA	Enable ADC on-chip VCCA detection channel Selected: Enabled Cleared: Disabled	Selected
	Enable VCC_CRAM	Enable ADC on-chip VCC_CRAM detection channel Selected: Enabled Cleared: Disabled	Selected
	Enable VCC_DRM	Enable ADC on-chip VCC_DRM detection channel Selected: Enabled Cleared: Disabled	Selected
	Enable VCC_PU[4]	Enable ADC on-chip VCC_PU detection channel Selected: Enabled Cleared: Disabled	Selected
	Enable VCCA_PU[4]	Enable ADC on-chip VCCA_PU detection channel Selected: Enabled Cleared: Disabled	Selected
	Enable VCCIO_DDR[4]	Enable ADC on-chip VCCIO_DDR detection channel Selected: Enabled Cleared: Disabled	Selected
	Enable Sample Averaging	Enable ADC channel averaging times Selected: Enable corresponding channels averaging Cleared: Disable corresponding channels averaging	Selected
	Input Mode	Selection of ADC channel input mode Fixed to Unipolar	Unipolar
External Channel	Enable VA	Enable ADC dedicated channel Selected: Enabled Cleared: Disabled	Cleared
	Enable VAUXn[5]	Enable ADC multiplexed channel Selected: Enable corresponding channel Cleared: Disable corresponding channel Note: For explanation of multiplexed channels, please refer to Table 2-3	Cleared

4 Only valid for PG2K400, indicating the ADC on-chip detection channel enabling mode.

5 "n" indicates the multiplexed channel number.

Option Domain	Parameter/Configuration Options	Parameter Description	Default Value
	Enable Sample Averaging	Enable ADC channel averaging times Selected: Enable corresponding channels averaging Cleared: Disable corresponding channels averaging	Selected
	Input Mode	Input mode selection for corresponding enabled channel Available input modes: Unipolar, Bipolar	Unipolar

Note: "-" indicates that there is no default value for this parameter on the IP configuration interface.

Table 2-3 ADC IP Multiplexed Channel Description

Applicable Devices	Package Type(s)	Number of Multiplexed Channels (n)	Description
PG2L25H	MBG325	8	The IP interface only allows configuration of available multiplexed channels
PG2L50H	FBG484	16	All multiplexed channels can be configured
PG2L100H	FBG676	16	All multiplexed channels can be configured
PG2L100HX	FBG676	16	All multiplexed channels can be configured
PG2L200H	FFBG1156	16	All multiplexed channels can be configured
PG2T390H	FFBG900	11	The number of multiplexed channels corresponds to the 11 available channels in ***"UG050009_Titan2 Family FPGA Analog-to-Digital Conversion (ADC) Module User Guide"*** in ascending order, and the available channels correspond to the device pin numbers in ascending order.
PG2T390HX	FFBG900	11	The number of multiplexed channels corresponds to the 11 available channels in ***"UG050009_Titan2 Family FPGA Analog-to-Digital Conversion (ADC) Module User Guide"*** in ascending order, and the available channels correspond to the device pin numbers in ascending order.
PG2K400	FFBG676	16	All multiplexed channels can be configured

Note: For other package types of applicable devices, the user must confirm the actually available multiplexed channels with AE before use.

2.3.1.2.2 Alarm Config

Alarm Config is the configuration page for temperature/voltage monitoring alarms. The interface is shown in Figure 2-7. For detailed parameters, please refer to Table 2-4. For alarm threshold configuration, please refer to "2.8.5 Temperature and Voltage Monitoring".

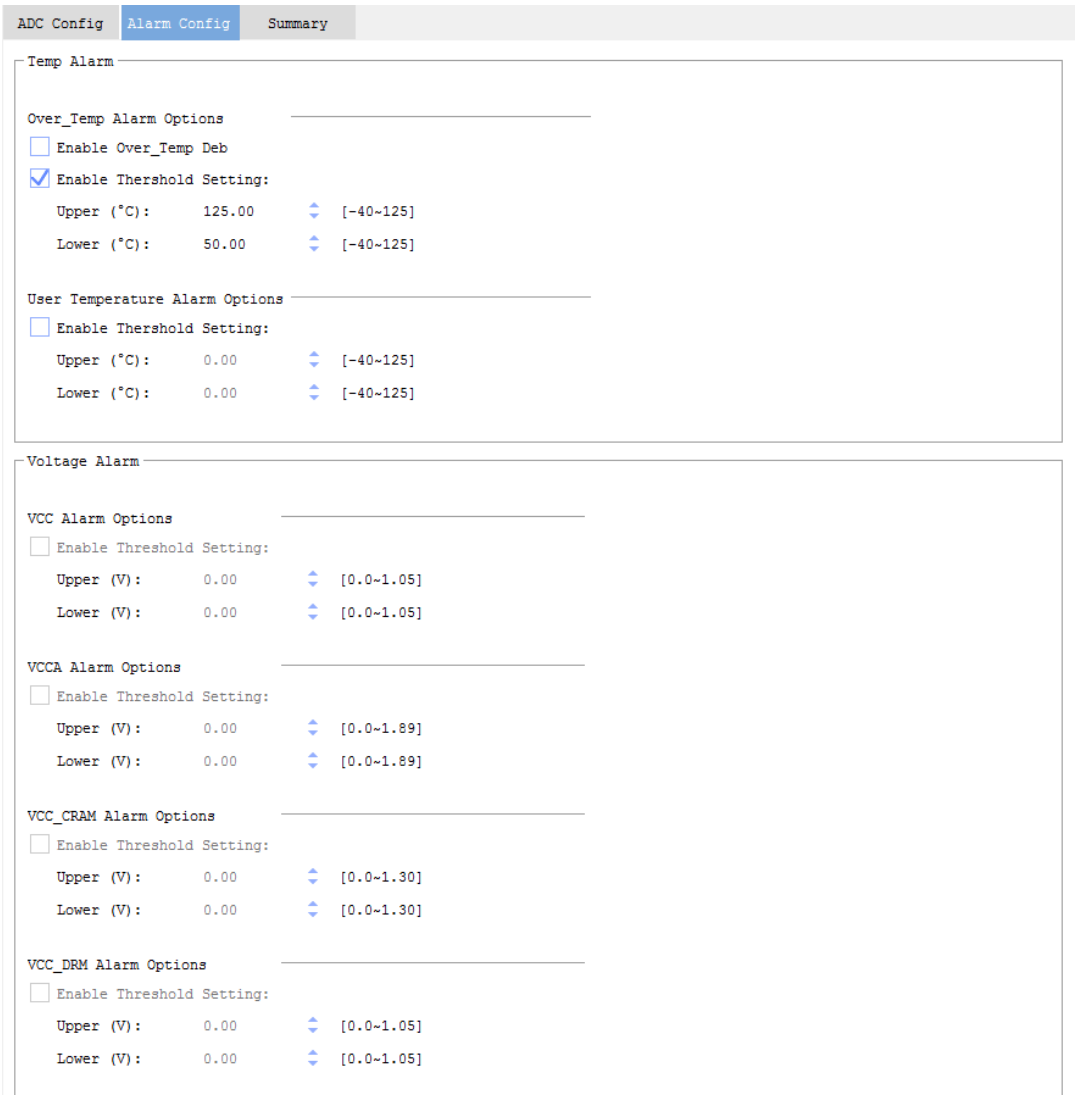

Figure 2-7 Alarm Config Page

Table 2-4 Descriptions of Configuration Parameters on the Alarm Config Page

Option Domain	Parameter/Configuration Options	Parameter Description	Default Value
Temp Alarm	Over_Temp Alarm Options	Enable Over_Temp Deb: Enable Over_Temp Debounce Selected: Enabled Cleared: Disabled	Cleared
		Enable Threshold Setting: Enable Over_Temp Alarm Threshold Setting Selected: Enabled Cleared: Not enabled (threshold cannot be configured) Upper: Setting upper limit for Over_Temp threshold Lower: Setting lower limit for Over_Temp threshold	Selected Upper: 125.00 Lower: 50.00

Option Domain	Parameter/Configuration Options	Parameter Description	Default Value
	User Temperature Alarm Options	Enable Threshold Setting: Enable User_Temp Alarm Threshold Setting Selected: Enabled Cleared: Not enabled (threshold cannot be configured) Upper: Setting upper limit for User_Temp threshold Lower: Setting lower limit for User_Temp threshold	Cleared Upper: 0.00 Lower: 0.00
Voltage Alarm	VCC Alarm Options	Enable Threshold Setting: Enable VCC Alarm Threshold Setting Selected: Enabled Cleared: Not enabled (threshold cannot be configured) Upper: Setting upper limit for VCC threshold Lower: Setting lower limit for VCC threshold	Cleared Upper: 0.00 Lower: 0.00
	VCCA Alarm Options	Enable Threshold Setting: Enable VCCA Alarm Threshold Setting Selected: Enabled Cleared: Not enabled (threshold cannot be configured) Upper: Setting upper limit for VCCA threshold Lower: Setting lower limit for VCCA threshold	Cleared Upper: 0.00 Lower: 0.00
	VCC_CRAM Alarm Options	Enable Threshold Setting: Enable VCC_CRAM Alarm Threshold Setting Selected: Enabled Cleared: Not enabled (threshold cannot be configured) Upper: Setting upper limit for VCC_CRAM threshold Lower: Setting lower limit for VCC_CRAM threshold	Cleared Upper: 0.00 Lower: 0.00
	VCC_DRM Alarm Options	Enable Threshold Setting: Enable VCC_DRM Alarm Threshold Setting Selected: Enabled Cleared: Not enabled (threshold cannot be configured) Upper: Setting upper limit for VCC_DRM threshold Lower: Setting lower limit for VCC_DRM threshold	Cleared Upper: 0.00 Lower: 0.00

Option Domain	Parameter/Configuration Options	Parameter Description	Default Value
	VCC_PU Alarm Options[6]	Enable Threshold Setting: Enable VCC_PU Alarm Threshold Setting Selected: Enabled Cleared: Not enabled (threshold cannot be configured) Upper: Setting upper limit for VCC_PU threshold Lower: Setting lower limit for VCC_PU threshold	Cleared Upper: 0.00 Lower: 0.00
	VCCA_PU Alarm Options[6]	Enable Threshold Setting: Enable VCCA_PU Alarm Threshold Setting Selected: Enabled Cleared: Not enabled (threshold cannot be configured) Upper: Setting upper limit for VCCA_PU threshold Lower: Setting lower limit for VCCA_PU threshold	Cleared Upper: 0.00 Lower: 0.00
	VCCIO_DDR Alarm Options[6]	Enable Threshold Setting: Enable VCCIO_DDR Alarm Threshold Setting Selected: Enabled Cleared: Not enabled (threshold cannot be configured) Upper: Setting upper limit for VCCIO_DDR threshold Lower: Setting lower limit for VCCIO_DDR threshold	Cleared Upper: 0.00 Lower: 0.00

2.3.1.2.3 Summary

The Summary page is used to print the current configuration information without configuration required, as shown in Figure 2-8.

Figure 2-8 Summary Page

6 Only valid for PG2K400, indicating ADC alarm threshold mode.

2.3.1.3 Generating IP

After configuring the parameters, click the <Generate> button in the top-left corner to generate the ADC IP code corresponding to the user-specific settings. The information report interface for IP generation is shown in Figure 2-9.

Figure 2-9 ADC IP Report Generation Interface

Upon successful IP generation, the files indicated in Figure 2-3 will be output to the Project path specified in the table below.

Table 2-5 Output Files After ADC IP Generation

Output File[7]	**Description**
$instname.v	The top-level .v file of the generated IP.
$instname.idf	The Configuration file of the generated IP.
/rtl/*	The plaintext RTL code files of the generated IP.
/example_design/*	The Test Bench, top-level files, and some module files used in the Example Design of the generated IP.
/pnr/core_only/*	The project files and pin constraint files for the generated IP core.
/pnr/example_design/*	The project files and pin constraint files for the Example Design of the generated IP.
/sim/modelsim/*	The simulation directory of the generated IP and the related files used for simulation.
/rev_1	The default output path for synthesis reports. (This folder is generated only after specifying the synthesis tool)
readme.txt	The readme file describes the structure of the generation directory after the IP is generated.

2.3.2 Constraint Configuration

For the specific configuration method of constraint files, please refer to the relevant help documents in the PDS installation path: "***User_Constraint_Editor_User_Guide***", "***Physical_Constraint_Editor_User_Guide***", "***Route_Constraint_Editor_User_Guide***".

7 <$instname> is the instantiation name entered by the user; "*" is a wildcard character used to replace files of the same type.

2.3.3 Simulation Runs

ADC IP performs simulation based on the IP core's Test Bench. Double-click the sim.bat file under the "<project_path>/sim/modelsim/" path to conduct simulation.

Attention:

When building their own simulation project, users need to place the design.txt file from the original simulation directory into this directory and use the macro definition "FOR_GTP_ADC_E2_SIM" to load the simulation input file design.txt required for simulation.

For more detailed information about the PDS simulation functions and third-party simulation tools, please consult the relevant help documents in the PDS installation path: "***Pango_Design_Suite_User Guide***", "***Simulation_User_Guide***".

2.3.4 Synthesis and Placement/Routing

The specific usage of PDS synthesis tools and placement/routing tools can be found in the help documents within the PDS installation path.

Attention:

Example Design project files .pds and pin constraint files .fdc generated with the IP are located in the "/pnr/example_design" directory, and the physical constraints need to be modified according to the actual devices and PCB trace routing. For details, please refer to "2.8 Descriptions and Considerations".

2.3.5 Bitstream Loading

After the ADC bitstream is downloaded, a reset is required to load the static configuration values into the ADC control register. Resetting time shall be at least one APB clock cycle. For a detailed introduction to the reset signal, please refer to "i_rst_n".

When using the signal "i_adc_loadsc_n" to reload the static configuration values, it needs to meet certain timing requirements. For detailed information, please refer to Table 2-6.

Table 2-6 i_adc_loadsc_n Timing Requirements for Reloading Static Configuration

Sampling Clock Source	Timing Requirements
CLK_OSC	Pull down for at least 80ns
CLK_APB	Pull down for at least one APB clock cycle

2.3.6 Resources Utilization

Table 2-7 Typical Resource Utilization Values for ADC IP Based on Applicable Devices

Device	Typical Resource Utilization Values			
	LUT	FF	USCM	ADC
PG2L25H	7	15	1	1
PG2L50H	7	15	1	1
PG2L100H	7	15	1	1
PG2T100HX	8	15	1	1
PG2L200H	7	15	1	1
PG2T390H	8	15	1	1
PG2T390HX	8	15	1	1
PG2K400	8	15	1	1

2.4 Example Design

This section mainly introduces the ADC IP Example Design scheme based on PG2T390H. This solution receives the analogue signal through the differential input port, collects the analogue signal according to the configured ADC working/sampling mode, and compares the measured value with the actual value to determine whether the ADC conversion is correct.

2.4.1 Design Block Diagram

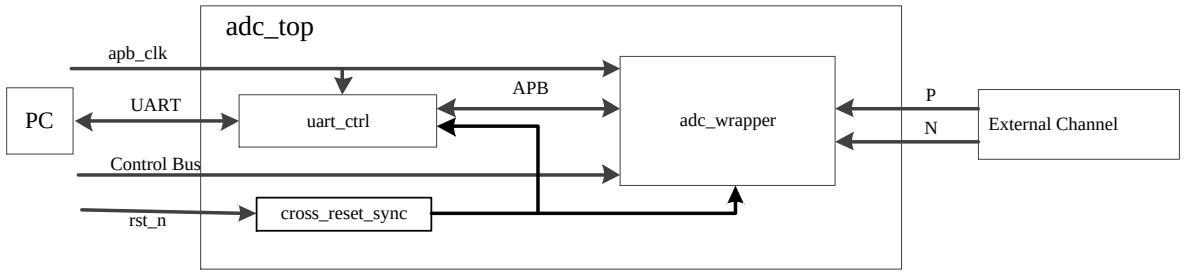

Figure 2-10 Example Design Block Diagram

The system block diagram of the Example Design is shown in Figure 2-10 mainly including the uart_ctrl, cross_reset_sync and adc_wrapper functional modules.

- The uart_ctrl module is used to read the conversion values from the ADC status register or to change the operating mode of ADC by modifying the ADC's control register;
- The cross_reset_sync module is used to debounce the reset signal.
- The adc_wrapper module is the top-level module of the IP, which processes ADC parameters and sorts ADC signals based on user configuration.

2.4.2 Descriptions of Ports

Table 2-8 Example Design Interface List

Port	I/O	Bit width	Description
Analog Input			
i_van	I	1	Dedicated analog input port N side
i_vap	I	1	Dedicated analog input port P side
i_vauxn0	I	1	Multiplex analog input port 0 N side
i_vauxp0	I	1	Multiplex analog input port 0 P side
i_vauxn1	I	1	Multiplex analog input port 1 N side
i_vauxp1	I	1	Multiplex analog input port 1 P side
i_vauxn2	I	1	Multiplex analog input port 2 N side
i_vauxp2	I	1	Multiplex analog input port 2 P side
i_vauxn3	I	1	Multiplex analog input port 3 N side
i_vauxp3	I	1	Multiplex analog input port 3 P side
i_vauxn4	I	1	Multiplex analog input port 4 N side
i_vauxp4	I	1	Multiplex analog input port 4 P side
i_vauxn5	I	1	Multiplex analog input port 5 N side
i_vauxp5	I	1	Multiplex analog input port 5 P side
i_vauxn6	I	1	Multiplex analog input port 6 N side
i_vauxp6	I	1	Multiplex analog input port 6 P side
i_vauxn7	I	1	Multiplex analog input port 7 N side
i_vauxp7	I	1	Multiplex analog input port 7 P side
i_vauxn8	I	1	Multiplex analog input port 8 N side
i_vauxp8	I	1	Multiplex analog input port 8 P side
i_vauxn9	I	1	Multiplex analog input port 9 N side
i_vauxp9	I	1	Multiplex analog input port 9 P side
i_vauxn10	I	1	Multiplex analog input port 10 N side
i_vauxp10	I	1	Multiplex analog input port 10 P side

Port	I/O	Bit width	Description
Clock and reset			
rst_n	I	1	System reset signal 0: Reset 1: Reset release
apb_pclk	I	1	APB clock Frequency: 8MHz - 104MHz
ADC control and status interface			
convst	I	1	Active sampling control signal, triggered at high pulse
adc_loadsc_n	I	1	Control register loading static configuration enable signal 0: Enabled 1: Disabled
over_temp	O	1	Over temperature indicator signal 0: Normal 1: Over_temp
user_temp_alarm	O	1	Temperature alarm indicator 0: Normal 1: Alarm
vcc_alarm	O	1	VCC voltage alarm indicator 0: Normal 1: Alarm
vcca_alarm	O	1	VCCA voltage alarm indicator 0: Normal 1: Alarm
vcc_cram_alarm	O	1	VCC_CRAM voltage alarm indicator 0: Normal 1: Alarm
vcc_drm_alarm	O	1	VCC_DRM voltage alarm indicator 0: Normal 1: Alarm
vcc_pu_alarm[8]	O	1	VCC_PU voltage alarm indicator 0: Normal 1: Alarm
vcca_pu_alarm[8]	O	1	VCCA_PU voltage alarm indicator 0: Normal 1: Alarm
vccio_ddr_alarm[8]	O	1	VCCIO_DDR voltage alarm indicator 0: Normal 1: Alarm
logic_done_a	O	1	ADCA status register update signal 0: Not updated 1: Updated
logic_done_b	O	1	ADCB status register update signal 0: Not updated 1: Updated
adc_clk_out	O	1	ADC working clock transmitted to SRB (this clock is not recommended for user logic)

8 Only valid for PG2K400, indicating ADC voltage alarm signal.

Port	I/O	Bit width	Description
UART interface			
cfg_uart_txd	O	1	Local port for sending data to the host computer
cfg_uart_rxd	I	1	Local port for receiving data from the host computer

2.4.3 Module Description

2.4.3.1 uart_ctrl

This is a serial port module used for debugging. It receives data from the UART and outputs data in the format required by the APB protocol, achieving data conversion between the serial port and the APB interface. The baud rate of the serial port is fixed at 115200, the read/write operation address is 8 bits, and the data is 16 bits.

- Read operation format: "0x72" + "address";
- Write operation format: "0x77" + "address" + "data".

For related read and write operation examples, please refer to "2.8.7 Read and Write Operation Examples of the uart_ctrl Module".

2.4.3.2 cross_reset_sync

Asynchronous signal synchronisation module, used for synchronising and debouncing externally input asynchronous signals.

2.4.3.3 adc_wrapper

For ADC IP layer, please refer to Table 2-9 for related interfaces.

2.4.4 Test Method

By instantiating the ADC IP of the corresponding mode[9], the Example Design project[10] of IP is used to generate a bitstream and program it onto the corresponding test board[11]. A differential voltage is used as the input to the external channel of the ADC, the status register of the corresponding enabled channel is read through the serial port, the read value is calculated to obtain the measurement result, and the measured value is compared with the input value to determine whether the ADC is converted correctly or not.

2.4.5 Instance Configuration

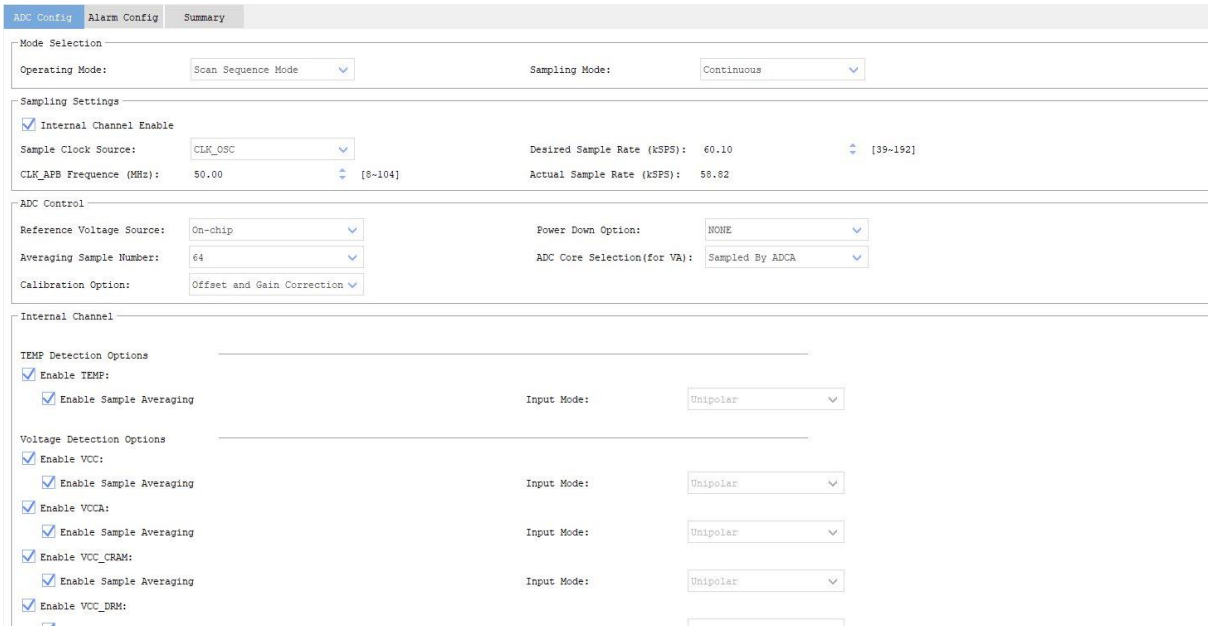

Figure 2-11 Block Diagram a of Example Design Instance Configuration

9 For details, please refer to "2.4.5 Instance Configuration" and "2.3.1 Module Instantiation".

10 For the Example Design project path, please refer to Table 2-5.

11 The model of the PG2T390H test board is P05V330RD04_A0.

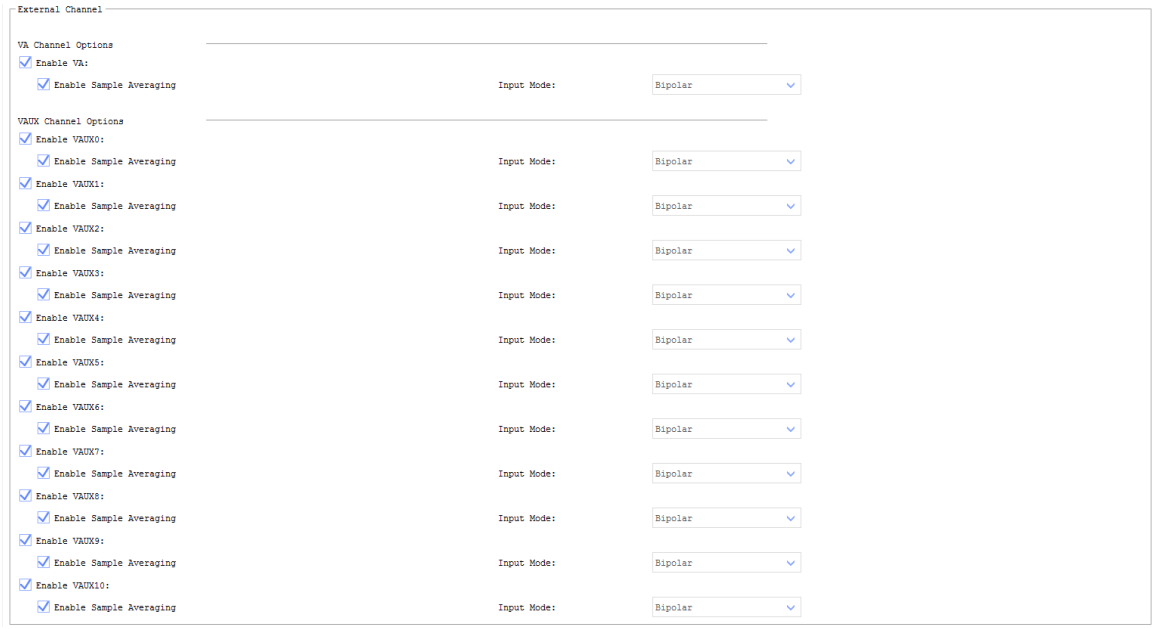

Figure 2-12 Block Diagram b of Example Design Instance Configuration

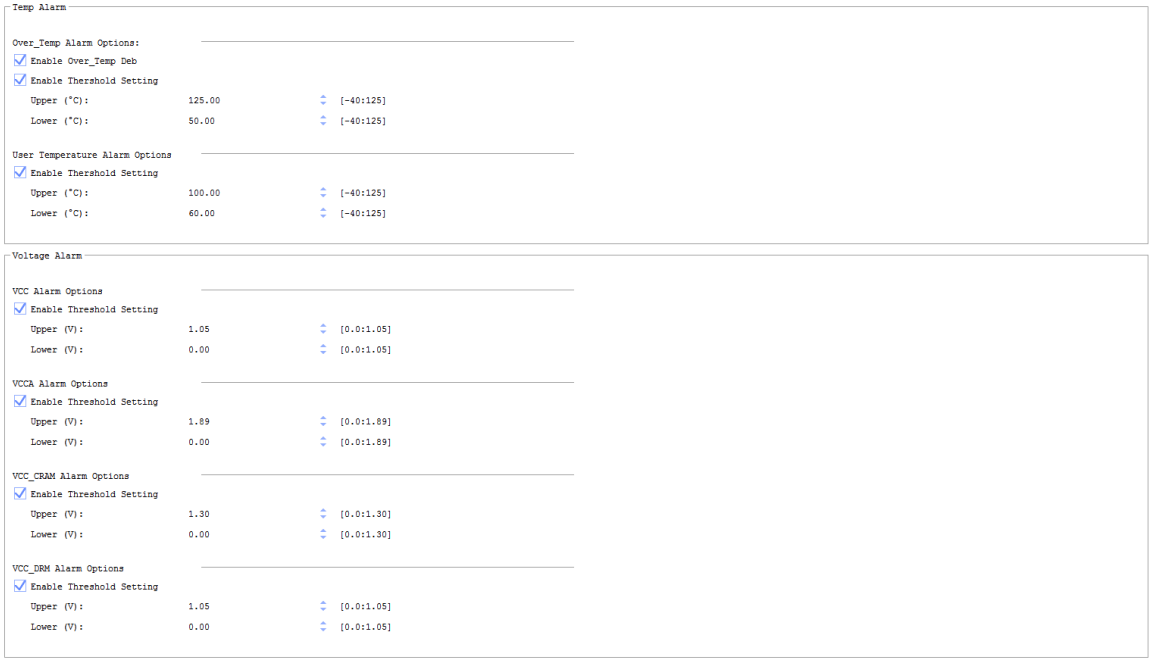

Figure 2-13 Block Diagram c of Example Design Instance Configuration

2.4.6 Instance Simulation

In the Windows system, after IP generation, double-click the *.bat file [12] under the "<project_path>/sim/modelsim" path to run simulation.

Attention:

Do not directly use the Example Design generated by the IP for Flow on-board testing; Modify physical constraints according to the devices and the PCB traces used, then proceed with Flow on-board testing. For details, please refer to "2.8 Descriptions and Considerations".

2.5 Descriptions of IP Interfaces

This section provides the ADC IP related to interface instructions and timing descriptions.

2.5.1 Descriptions of Ports

Table 2-9 List of ADC IP Interfaces

Port	I/O	Bit width	Description
Analog Input[13]			
i_vap	I	1	Dedicated analog input port P side
i_van	I	1	Dedicated analog input port N side
i_vauxp0	I	1	Multiplex analog input port 0 P side
i_vauxn0	I	1	Multiplex analog input port 0 N side
i_vauxp1	I	1	Multiplex analog input port 1 P side
i_vauxn1	I	1	Multiplex analog input port 1 N side
i_vauxp2	I	1	Multiplex analog input port 2 P side
i_vauxn2	I	1	Multiplex analog input port 2 N side
i_vauxp3	I	1	Multiplex analog input port 3 P side
i_vauxn3	I	1	Multiplex analog input port 3 N side

12 For the output files after IP generation, please refer to Table 2-5.

13 For the number of multiplexed channels on different devices, please refer to Table 2-3; multiplexed channels need to be constrained to the 1.8V level standard.

Port	I/O	Bit width	Description
i_vauxp4	I	1	Multiplex analog input port 4 P side
i_vauxn4	I	1	Multiplex analog input port 4 N side
i_vauxp5	I	1	Multiplex analog input port 5 P side
i_vauxn5	I	1	Multiplex analog input port 5 N side
i_vauxp6	I	1	Multiplex analog input port 6 P side
i_vauxn6	I	1	Multiplex analog input port 6 N side
i_vauxp7	I	1	Multiplex analog input port 7 P side
i_vauxn7	I	1	Multiplex analog input port 7 N side
i_vauxp8	I	1	Multiplex analog input port 8 P side
i_vauxn8	I	1	Multiplex analog input port 8 N side
i_vauxp9	I	1	Multiplex analog input port 9 P side
i_vauxn9	I	1	Multiplex analog input port 9 N side
i_vauxp10	I	1	Multiplex analog input port 10 P side
i_vauxn10	I	1	Multiplex analog input port 10 N side
i_vauxp11	I	1	Multiplex analog input port 11 P side
i_vauxn11	I	1	Multiplex analog input port 11 N side
i_vauxp12	I	1	Multiplex analog input port 12 P side
i_vauxn12	I	1	Multiplex analog input port 12 N side
i_vauxp13	I	1	Multiplex analog input port 13 P side
i_vauxn13	I	1	Multiplex analog input port 13 N side
i_vauxp14	I	1	Multiplex analog input port 14 P side
i_vauxn14	I	1	Multiplex analog input port 14 N side
i_vauxp15	I	1	Multiplex analog input port 15 P side
i_vauxn15	I	1	Multiplex analog input port 15 N side
Clock and reset			
i_rst_n	I	1	ADC IP reset signal An active reset must be performed after the bitstream is downloaded 0: Reset (maintaining for at least one APB clock cycle) 1: Reset release
i_apb_pclk	I	1	APB clock Frequency: 8MHz-100MHz (Logos2 Family) 8MHz-104MHz (Titan2/Kosmo2 family)
APB interface			
i_apb_paddr[7:0]	I	8	APB interface read/write address bus
i_apb_psel	I	1	APB interface Chip Select signal 0: Cleared 1: Selected
i_apb_enable	I	1	APB interface access enable 0: Not enabled 1: Enabled
i_apb_pwrite	I	1	Write operation enable signal 0: Read data 1: Write data

Port	I/O	Bit width	Description
i_apb_pwdata[15:0]	I	16	APB interface write data bus
i_apb_prdata[15:0]	O	16	APB interface read data bus
o_apb_pready	O	1	APB interface read/write Ready signal Write Operation 0: Data has not been successfully written to the register 1: Data has been successfully written to the register Read Operation 0: Read data is not yet ready 1: Read data is now ready
ADC control and status interface			
i_adc_convst	I	1	Active sampling control signal, active at high pulse
i_adc_loadsc_n	I	1	Control register loading static configuration enable signal 0: Enabled 1: Disabled
o_over_temp	O	1	Over Temperature indicator 0: Normal 1: Over_temp
o_logic_done_a	O	1	ADCA status register update indicator 0: Not updated 1: Updated
o_logic_done_b	O	1	ADCB status register update indicator 0: Not updated 1: Updated
o_adc_clk_out	O	1	ADC working clock transmitted to SRB (this clock is not recommended for user logic)
o_adc_dmodified	O	1	Control register modification flag signal 0: APB has already operated the control register 1: After Jtag-APB writes, APB operation has not been operated
o_user_temp_alarm	O	1	Temperature alarm indicator: 0: Normal 1: Alarm
o_vcc_alarm	O	1	VCC voltage alarm indicator: 0: Normal 1: Alarm
o_vcca_alarm	O	1	VCCA voltage alarm indicator: 0: Normal 1: Alarm
o_vcc_drm_alarm	O	1	VCC_DRM voltage alarm indicator: 0: Normal 1: Alarm
o_vcc_cram_alarm	O	1	VCC_CRAM voltage alarm indicator: 0: Normal 1: Alarm
o_vcc_pu_alarm[14]	O	1	VCC_PU voltage alarm indicator: 0: Normal 1: Alarm

14 Used only for PG2K400 to indicate voltage alarm signal.

Port	I/O	Bit width	Description
o_vcca_pu_alarm[14]	O	1	VCCA_PU voltage alarm indicator: 0: Normal 1: Alarm
o_vccio_ddr_alarm[14]	O	1	VCCIO_DDR voltage alarm indicator: 0: Normal 1: Alarm

2.5.2 Descriptions of Timings

2.5.2.1 APB Write Timing

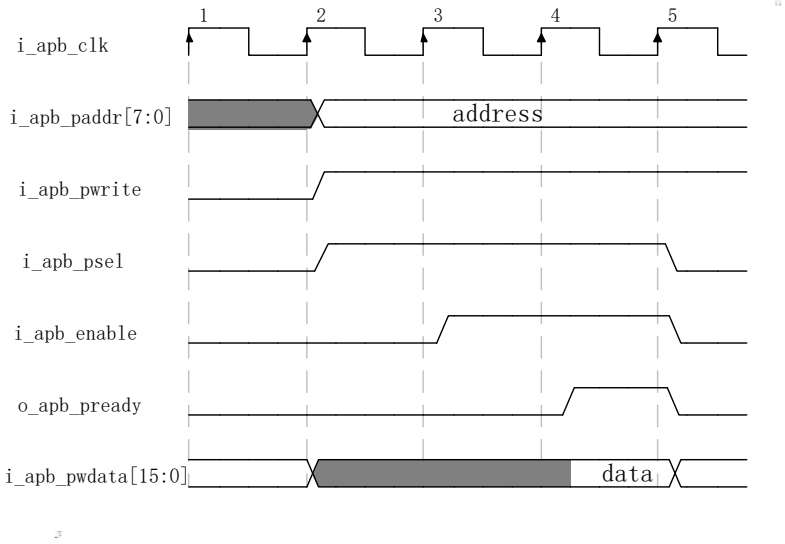

Figure 2-14 APB Write Timing

2.5.2.2 APB Read Timing

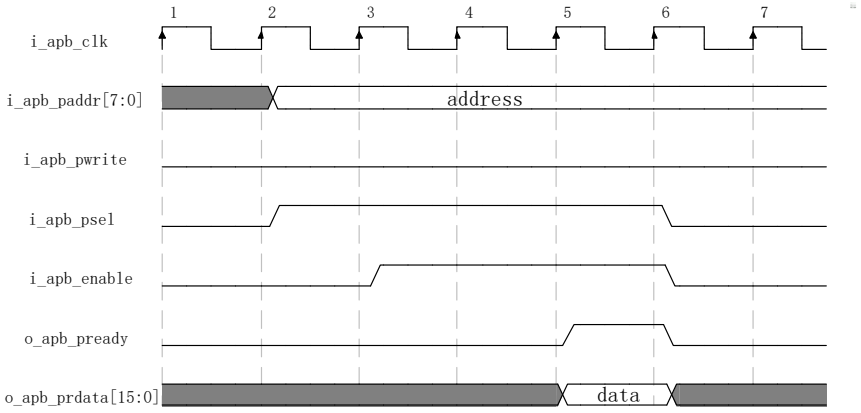

Figure 2-15 APB Read Timing

2.6 Description of the IP Register

For information on ADC module registers, please refer to "***UG040009_Logos2 Family FPGA Analog-to-Digital Conversion (ADC) Module User Guide***", "***UG050009_Titan2 Family FPGA Analog-to-Digital Conversion (ADC) Module User Guide***", and "***UG100009_Kosmo2 Family SOPC Analog-to-Digital Conversion (ADC) Module User Guide***".

2.7 Typical Applications

For typical applications of ADC IP, please refer to "2.4 Example Design".

2.8 Descriptions and Considerations

2.8.1 Clock Constraints

In the generated Example Design project constraint file ipmxb_vt_snsr_onboard_top.fdc, the APB clock of ADC has been constrained to the clock pin. Taking the Example Design project as an example:

```
define_attribute {p:apb_clk} {PAP_IO_DIRECTION} {INPUT}
define_attribute {p:apb_clk} {PAP_IO_LOC} {AG10}
define_attribute {p:apb_clk} {PAP_IO_VCCIO} {1.8}
define_attribute {p:apb_clk} {PAP_IO_STANDARD} {LVCMOS18}
define_attribute {p:apb_clk} {PAP_IO_UNUSED} {TRUE}
```

Users can modify the constraints according to the actual situation of the single board to meet practical usage requirements.

2.8.2 Physical Location Constraints

In the application, the PDS software will automatically constrain the ADC to the relevant position, and in the generated Example Design project constraint file ipmxe_adc_top.fdc, the relevant constraints have been made on the enabled multiplexed analog channels, and the user can modify it according to the actual situation of the single board to adapt to the actual needs.

The dedicated analogue channel of the ADC is a fixed pin, which will be automatically constrained by PDS software.

2.8.3 Operating Modes

2.8.3.1 Power Up Mode

The main function of Power Up Mode is to detect internal voltage signals and temperature through on-chip detectors. The fixed configuration for this mode is described as follows:

- Scan Mode: Fixed to Unipolar mode;
- ADC Input Reference Source: Fixed to On-chip;
- Number of Data Averages: Fixed to 16 times;
- Sampling Mode: Fixed to Continuous.
- Sampling Channels: Fixed to internal voltage and temperature channels.

2.8.3.2 Scan Sequence Mode

The main function of Scan Sequence Mode is to perform configured scans on selected channels according to the respective settings, executing either a single scan or cycled scans.

Scan Sequence Mode has following three scan configurations:

- Standalone ADCA Scan, in which ADCA performs scans according to the settings in the control register. It is possible to scan a single channel or scan multiple channels at once.
- ADCA and ADCB scan different external channels[15] in pairs, and both ADCs select the same number of external channels and operate independently of each other. At this time, ADCA can still choose to scan internal temperature and voltage channels. When ADCA scans temperature and voltage, ADCB remains in an idle state.

15 In this mode, the IP interface can only configure the external channels scanned by ADCA, and the channels paired with ADCB will be automatically enabled; at this time, the channel averaging enabling and input mode can still be configured separately (except for PG2L100H).

- ADCA performs Power Up Mode while ADCB scans external channels. Both ADCs scan relatively independently.

Attention:

When using ADCA/ADCB separately, if configured in 2-channel mode and 2 division, the AVG setting of 1 is not supported; otherwise, the corresponding sampling rate will be incorrect.

PG2L100H does not support switching channel input modes during the scan process, and all channel input modes scanned by ADCA/ADCB must be the same.

Table 2-10 Scan Sequence Mode Scan Configuration Description

Scanning Mode	**Corresponding Configuration**
Standalone ADCA Scan	Power Down Option: ADCB Power Down Only ADC Core Selection (for VA): Sampled By ADCA
ADCA and ADCB scan different external channels in pair	Power Down Option: NONE ADC Core Selection (for VA): Sampled By ADCA
ADCA performs Power Up Mode while ADCB scans external channels	Power Down Option: NONE ADC Core Selection (for VA): Sampled By ADCB

2.8.4 Description of Sampling Frequency

2.8.4.1 CLK_OSC as the Sampling Clock Source

Table 2-11 Description of Sampling Frequency Range Under CLK_OSC

Operating Modes	**Sampling Frequency Range**
Power Up Mode	39~192kSPS
Scan Sequence Mode	39~1000kSPS

2.8.4.2 CLK_APB as the Sampling Clock Source

Table 2-12 Description of Sampling Frequency Range Under CLK_APB

Operating Modes	**Sampling Frequency Range**[16]
Power Up Mode	39~192kSPS
Scan Sequence Mode	39~350kSPS (CLK_APB frequency < 36.4MHz) 39~1000kSPS (CLK_APB frequency ≥ 36.4MHz)

2.8.4.3 Actual Sampling Frequency Calculation Method

The actual sampling frequency is calculated based on the user's input of the desired sampling frequency, resulting in the closest sampling frequency within the sampling frequency range. The detailed calculation formulas are as follows:

$$div = \frac{clk}{rate(desired) * 26}$$

$$div(act) = \begin{cases} int(div)；\ (int(div)\ Even\ number） \\ int(div) + 1；（int(div)\ Odd\ number） \end{cases}$$

$$rate(act) = \frac{clk}{div(act) * 26}$$

Among them, clk is the clock frequency of the sampling clock source; div is the clock division value directly calculated based on the user's desired sampling frequency, int(div) is the rounded value of div, div(act) is the actual written clock division value, and rate(act) is the calculated actual sampling frequency.

If the calculated actual sampling frequency is greater than the sampling frequency range, *div(act)* will be automatically increased by 2 to recalculate the actual sampling frequency; if the calculated actual sampling frequency is less than the sampling frequency range, *div(act)* will be automatically decreased by 2 to recalculate the actual sampling frequency.

16 The sampling frequency is related to the APB read time. For details, please refer to "***UG040009_Logos2 Family FPGA Analog-to-Digital Conversion (ADC) Module User Guide***", "***UG050009_Titan2 Family FPGA Analog-to-Digital Conversion (ADC) Module User Guide***", and "***UG100009_Kosmo2 Family SOPC Analog-to-Digital Conversion (ADC) Module User Guide***".

2.8.5 Temperature and Voltage Monitoring

2.8.5.1 Temperature

After enabling the temperature scan channel, the temperature alarm threshold can be configured in the Alarm interface. The formula for converting user-set thresholds to ADC Code is:

$$Code = \frac{D_{in} + 273.15}{0.1219}$$

$$T_{up} = int(Code)$$

$$T_{below} = int(Code) + 1$$

Among them, D_{in} is the user interface configured threshold, *Code* is the write value of the converted register, *int(Code)* is the rounded operation on *Code*, T_{up} is the upper limit of the actual written register threshold, and T_{below} is lower limit of the actual written register threshold.

2.8.5.2 Voltage

After enabling the voltage scan channel, the voltage alarm threshold for the corresponding channel can be configured in the Alarm interface. The formula for converting user-set thresholds to ADC Code is:

$$Code = \frac{4096 * D_{in}}{3}$$

$$V_{up} = int(code)$$

$$V_{below} = int(code) + 1$$

Among them, D_{in} is the user interface configured threshold, *Code* is the write value of the converted register, *int(Code)* is the rounded operation on *Code*, V_{up} is the upper limit of the actual written register threshold, and V_{below} is the lower limit of the actual written register threshold.

2.8.6 Dynamically Modify IP Configuration

After modifying the ADC internal registers through the APB interface, the IP will operate under the corresponding configuration.

Recommendation:

It is recommended to configure the required ADC IP through IPC instantiation.

2.8.7 Read and Write Operation Examples of the uart_ctrl Module

2.8.7.1 Read Operation

Read data from address 0x01: "0x72" + "0x01", resulting in 0x7201.

2.8.7.2 Write Operation

Write 0x01 to address 0x02: "0x77"+"0x01"+"0x0002", resulting in 0x77010200.

2.8.8 IP Invocation Method

Users can directly add the IP by adding the idf of the ADC IP generated by the IPC instantiation through PDS.

2.8.9 Sampling Mode Descriptions

If it requires to switch the sampling mode from active sampling mode to continuous sampling mode, the mode switch needs to be achieved by configuring the address 0x00 or 0x01 register and triggering a soft reset.

2.9 IP Debugging Method

The UART in Example Design can read the control register and status register within the IP to determine the IP operating mode. For UART module usage, please refer to "2.4.3.1 uart_ctrl".

For more information on IP debugging, please refer to "***UG040009_Logos2 Family FPGA Analog-to-Digital Conversion (ADC) Module User Guide***", "***UG050009_Titan2 Family FPGA Analog-to-Digital Conversion (ADC) Module User Guide***", and "***UG100009_Kosmo2 Family SOPC Analog-to-Digital Conversion (ADC) Module User Guide***".

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