SGMII over LVDS IP

User Guide

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Revisions History

Document Revisions

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V1.4	25.04.2024	Initial release.	V1.4

IP Revisions

IP Version	Date of Release	Revisions
V1.4	25.04.2024	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
APB	Advanced Peripheral Bus
GMII	Gigabit Media Independent Interface
LH	Latching High
LL	Latching Low
LVDS	Low Voltage Differential Signal
MDIO	Management Data Input/Output
PCS	Physical Code Sublayer
PLL	Phase Lock Loop
PMA	Physical Media Attachment
SGMII	Serial Gigabit Media Independent Interface
IPC	IP Compiler
PDS	Pango Design Suite

Related Documentation

The following documentation is related to this manual:

1. ***Pango_Design_Suite_Quick_Start_Tutorial***
2. ***Pango_Design_Suite_User_Guide***
3. ***IP_Compiler_User_Guide***
4. ***Simulation_User_Guide***
5. ***User_Constraint_Editor_User_Guide***
6. ***Physical_Constraint_Editor_User_Guide***
7. ***Route_Constraint_Editor_User_Guide***
8. ***IEEE 802.3-2012 Specification***
9. ***Serial-GMII Specification-rev1.8***
10. ***UG040006_Logos2 Family FPGAs Input/Output Interface (IO) User Guide***
11. ***UG040004_Logos2 Family FPGAs Clock Resources (Clock) User Guide***
12. ***UG050006_Titan2 Family FPGA Input/Output Interface (IO) User Guide***

13. UG050004_Titan2 Family FPGA Clock Resources (Clock) User Guide

14. UG100004_Kosmo2 Family SoPC Clock Resource (Clock) User Guide

15. UG100006_Kosmo2 Family SoPC Input/Output Interface (IO) User Guide

Table of Contents

Revisions History **1**
About this Manual **2**
Table of Contents **4**
Tables **6**
Figures **7**
Chapter 1 Preface **8**
1.1 Introduction of the Manual 8
1.2 Writing Standards of the Manual 8
Chapter 2 IP User Guide **9**
2.1 IP Introduction 9
2.1.1 Key Features 9
2.1.2 Applicable Devices and Packages 10
2.2 IP Block Diagram 10
2.3 IP Generation Process 11
2.3.1 Module Instantiation 11
2.3.2 Constraint Configuration 15
2.3.3 Simulation Runs 16
2.3.4 Synthesis and Placement/Routing 16
2.3.5 Resources Utilization 17
2.4 Example Design 17
2.4.1 Design Block Diagram 18
2.4.2 Module Description 18
2.4.3 Descriptions of Ports 21
2.4.4 Test Method 22
2.4.5 Instance Configuration 22
2.4.6 Instance Simulation 23
2.5 Descriptions of IP Interfaces 23
2.5.1 IP Interface Description 23
2.5.2 Configuration Management Interface 28
2.5.3 Fast Configuration Interface 29
2.5.4 GMII Interface 30
2.6 Description of the IP Register 31
2.6.1 Register Description 31
2.7 Typical Applications 37
2.7.1 Single Lane Typical Applications 37
2.7.2 Multi Lane Typical Applications 37

2.8 Descriptions and Considerations 38
2.8.1 Clock Signal 38
2.8.2 Reset signal 39
2.8.3 Physical Constraints 39
2.8.4 LVDS Transceiver Module 40
2.8.5 Loopback Mode 41
2.8.6 IP Clock Scheme 43
2.8.7 Example of read and write operations for the uart_ctrl_top module 43
2.9 IP Debugging Method 44
Disclaimer 45

Tables

Table 1-1 Description of Writing Standards 8
Table 2-1 SGMII over LVDS IP Applicable Devices and Packages 10
Table 2-2 SGMII over LVDS IP Configuration Parameter Description 14
Table 2-3 Output Files After SGMII over LVDS IP Generation 14
Table 2-4 Typical Resource Utilization Values for SGMII over LVDS IP Based on Applicable Devices 17
Table 2-5 uart_ctrl Module Address Description 19
Table 2-6 sgmii_lvds_reg_slave Register Description 20
Table 2-7 List of Example Design Interface Signals 21
Table 2-8 SGMII over LVDS IP Interface Signal List 23
Table 2-9 Register Definitions When Auto-Negotiation is Enabled 31
Table 2-10 Register Definitions When Auto-Negotiation is Disabled 32
Table 2-11 Control Register (Register 0) 33
Table 2-12 Status Register (Register 1) 33
Table 2-13 PHY Identifier Register (Register 2 & 3) 34
Table 2-14 Auto-Negotiation Advertisement PHY Mode (Register 4) 34
Table 2-15 Auto-Negotiation Advertisement MAC Mode (Register 4) 35
Table 2-16 Auto-Negotiation Link Partner Ability Register (Register 5) 35
Table 2-17 Auto-Negotiation Expansion Register (Register 6) 36
Table 2-18 Extended Status Register (Register 15) 36
Table 2-19 Vender_spc Register (Register 16) 36
Table 2-20 Vendor_Spec_1 Register (Register 17) 37
Table 2-21 clk_gen Interface Signal List 38
Table 2-22 PCS Core Loopback Port Configuration 41
Table 2-23 PCS Core Loopback Port Configuration 41
Table 2-24 Transceiver Near-End Loopback Port Configuration 42
Table 2-25 Transceiver Near-End Loopback Register Configuration 42
Table 2-26 Transceiver Far-End Loopback Port Configuration 42
Table 2-27 Transceiver Far-End Loopback Register Configuration 42
Table 2-28 Debug Ports and Their Description 44

Figures

Figure 2-1 SGMII over LVDS IP System Block Diagram 10
Figure 2-2 SGMII over LVDS IP Selection Path 12
Figure 2-3 Project Instantiation Interface 12
Figure 2-4 SGMII over LVDS IP Interface Block Diagram 13
Figure 2-5 Configuration Interface for SGMII over LVDS IP Parameters 13
Figure 2-6 SGMII over LVDS IP Generation Report Interface 14
Figure 2-7 Example Design Block Diagram 18
Figure 2-8 MAC Side Configuration Diagram 22
Figure 2-9 PHY Side Configuration Diagram 23
Figure 2-10 Basic APB Write Timing 28
Figure 2-11 Basic APB Read Timing 29
Figure 2-12 MDIO Write Timing 29
Figure 2-13 MDIO Write Timing 29
Figure 2-14 GMII Transmit Timing at a Rate of 100Mbps 30
Diagram 2-15 GMII Receive Timing at a Rate of 100Mbps 31
Figure 2-16 Multi Lane Scheme Diagram 38
Figure 2-17 LVDS Transceiver Function Diagram 40
Figure 2-18 IP Clock Network Diagram 43

Chapter 1 Preface

This chapter describes the scope, structure, and writing standards of this manual to help users quickly find the information they need.

1.1 Introduction of the Manual

This manual is a user guide for the SGMII over LVDS IP launched by Pango Microsystems. The content of this manual primarily includes the IP user guide and related information. This manual helps users quickly understand the features and usage of the IP.

1.2 Writing Standards of the Manual

Table 1-1 Description of Writing Standards

Text	**Rules**
Attention	If users ignore the attention contents, they may suffer adverse consequences or fail to operate successfully due to incorrect actions.
Description	Instructions and tips provided for users.
Recommendation	Recommended settings and instructions for users.

Chapter 2 IP User Guide

This chapter provides a guide on the use of SGMII over LVDS IP, including an introduction to IP, block diagram, IP generation process, Example Design, IP interface description, IP register description, typical applications, instructions and considerations, and IP debugging methods. More details on the design process can be found in the following PDS help documentation.

- "***Pango_Design_Suite_Quick_Start_Tutorial***"
- "***Pango_Design_Suite_User_Guide***"
- "***IP_Compiler_User_Guide***"
- "***Simulation_User_Guide***"

2.1 IP Introduction

SGMII over LVDS IP is developed by Pango Microsystems based on General Purpose IO (GPIO) to achieve the Ethernet SGMII interface. This IP uses the LVDS interface as a transceiver and provides a cost-effective solution that facilitates multiple channel expansions. Users can configure and generate the IP module using the IPC (IP Compiler) tool within the PDS (Pango Design Suite).

2.1.1 Key Features

SGMII over LVDS IP is compliant with "***IEEE 802.3-2012 Specification***" and "***Serial-GMII Specification-rev1.8***" standards. It has the following main features.

- Supports clock synchronization SGMII interface;[1]
- Supports mode selection: PHY mode and MAC mode;
- Supports rate switching: 10/100/1000Mbps;
- Supports auto-negotiation function;
- Supports configuration management interface: APB and MDIO interfaces;

1 Clock synchronization means there is no frequency offset between the local end and the Link Partner.

- Supports fast configuration through ports;
- Supports interface timing calibration: automatic calibration and user-defined calibration;
- Supports loopback function;
- Supports LVDS25 and LVDS18[2] level standard transmission.

2.1.2 Applicable Devices and Packages

Table 2-1 SGMII over LVDS IP Applicable Devices and Packages

Applicable Devices	**Supported Packages**
PG2L25H	ALL
PG2L50H	ALL
PG2L100HX	ALL
PG2L200H	ALL
PG2T70H	ALL
PG2T160H	ALL
PG2T390HX	ALL
PG2K400	ALL

2.2 IP Block Diagram

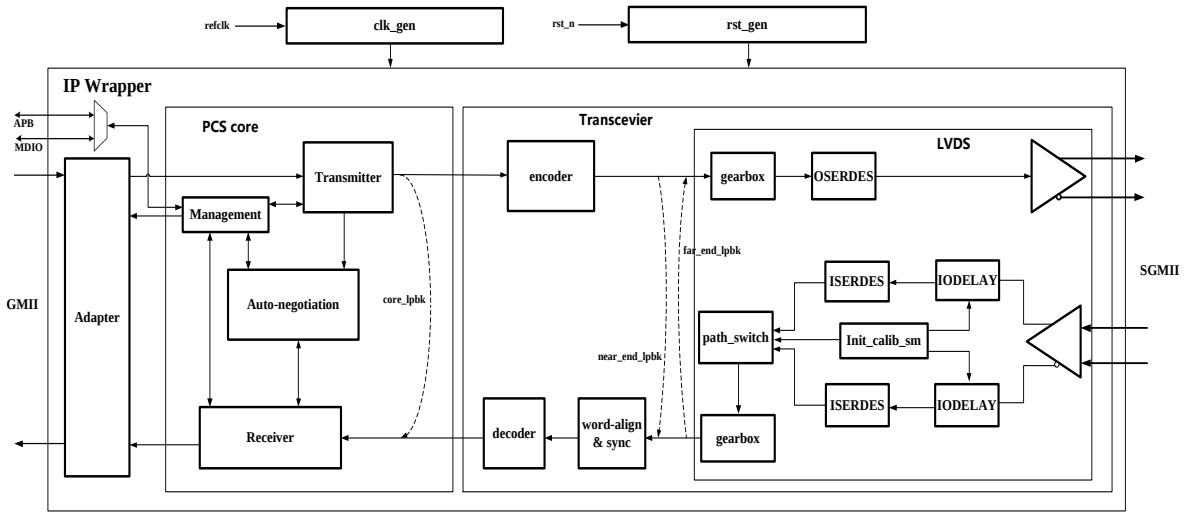

Figure 2-1 SGMII over LVDS IP System Block Diagram

2 PG2T and PG2K family devices are supported.

The SGMII over LVDS IP system block diagram is shown in Figure 2-1. The SGMII over LVDS IP consists of four parts: PCS core, Transceiver, clk_gen, and rst_gen. The dashed lines in the diagram indicate the data stream during loopback; for loopback configuration, please refer to "2.8.5 Loopback Mode".

- The PCS core module implements data transmission, reception, auto-negotiation, and interface management functions as specified in the 1000BASE-X protocol layer;
- The Transceiver module is primarily responsible for data encoding/decoding, synchronization, and PMA serialization/deserialization. For details, please refer to "2.8.4 LVDS Transceiver Module";
- The clk_gen and rst_gen modules generate clock and reset signals for the interface, respectively, and are independent of the IP top module. When implementing multiple interfaces, the clk_gen and rst_gen modules can be shared. For multi-lane applications, please refer to "2.7.2 Multi Lane Typical Applications".

2.3 IP Generation Process

2.3.1 Module Instantiation

Configurations of SGMII over LVDS IP can be customized through the IPC tool, instantiating the required IP modules. For specific usage of the IPC tool, please refer to *"**IP_Compiler_User_Guide**"*.

The main steps for instantiating the SGMII over LVDS IP module are described below.

2.3.1.1 Selecting IP

Open IPC and click File > Update in the main window to open the Update IP dialog box, where you add the corresponding version of the IP model.

After selecting the FPGAs device type, the Catalog interface displays the loaded IP models. Select the corresponding version of SGMII over LVDS under the "System/Ethernet" directory. The IP selection path is shown in Figure 2-2. Then set the Pathname and Instance Name on the right side of the page. The project instantiation interface is shown in Figure 2-3.

Attention:

PG2L25H: The software version must be 2023.2 or above.

PG2L50H: The software version must be 2022.2 or above.

PG2L200H: The software version must be 2022.2 or above.

PG2T390HX: The software version must be 2023.1 or above.

PG2K400: The software version must be 2023.2 or above;

PG2L100HX: The software version must be 2023.1 or above;

PG2T70H: The software version must be 2023.2 or above;

PG2T160H: The software version must be 2024.1 or above.

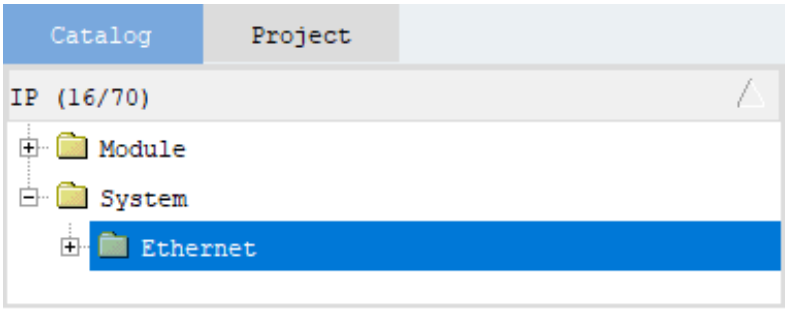

Figure 2-2 SGMII over LVDS IP Selection Path

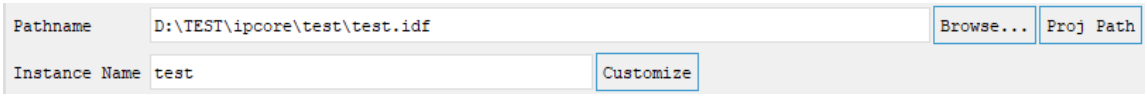

Figure 2-3 Project Instantiation Interface

2.3.1.2 IP Parameter Configuration

After selecting the IP, click <Customize> to enter the SGMII over LVDS IP parameter configuration graphic interface. The left Symbol is the interface block diagram, as shown in Figure 2-4; the Parameter Configuration window is shown on the right side, as shown in Figure 2-5.

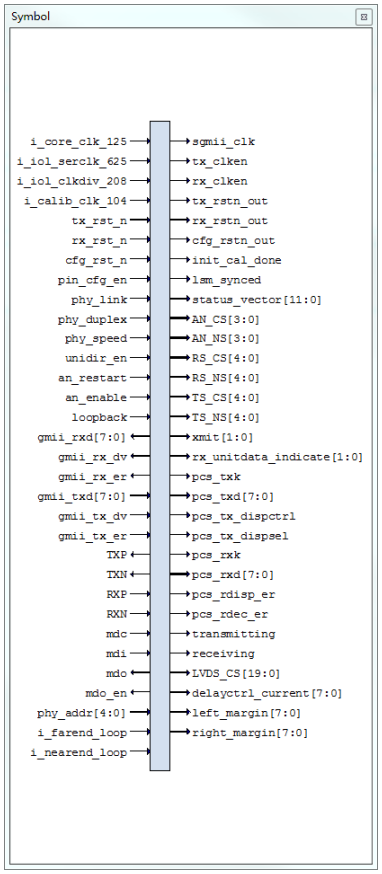

Figure 2-4 SGMII over LVDS IP Interface Block Diagram

Figure 2-5 Configuration Interface for SGMII over LVDS IP Parameters

Table 2-2 SGMII over LVDS IP Configuration Parameter Description

Option Domain	Option Name/Parameter Name	Parameter Description	Default Value
Management Options	Enable Auto Negotiation	Select whether to enable auto-negotiation Selected: Enabled Cleared: Disabled	Enabled
	Enable MDIO	Select whether to enable MDIO. Selected: Enabled (the MDIO configuration management register is used) Cleared: Disabled (the APB configuration management register is used)	Enabled
Operation Mode	SGMII PHY Mode	Select the SGMII working mode Selected: IP operates in PHY mode Cleared: IP operates in MAC mode	PHY
IO Bank Select	HP IO Bank[3]	The interface uses HPIO resources to transmit serial data with LVDS18 level standards.	HR IO Bank
	HR IO Bank	The interface uses HRIO resources to transmit serial data with LVDS25 level standards.	

2.3.1.3 Generating IP

Upon completion of parameter configuration, click the <Generate> button in the top left corner to generate the SGMII over LVDS IP code according to the user-specific settings. The information report interface for IP generation is shown in Figure 2-6.

Figure 2-6 SGMII over LVDS IP Generation Report Interface

Upon successful IP generation, the files indicated in Figure 2-3 will be output to the Project path specified in the table below.

Table 2-3 Output Files After SGMII over LVDS IP Generation

Output File[4]	Description
$instname.v	The top-level .v file of the generated IP.
$instname.idf	The Configuration file of the generated IP.

3 PG2T and PG2K family devices support "HP IO Bank" Configuration.

4 <$instname> is the instantiation name entered by the user; "*" is a wildcard character used to replace files of the same type.

Output File[4]	Description
/rtl/*	The plaintext RTL files of the generated IP.
/rtl/common/*.v	The plaintext RTL files of the generated IP to store some common modules.
/rtl/lvds /*.v	This folder contains plaintext RTL files of the LVDS transceiver.
/rtl/synplify/*.vp	The nonplaintext RTL files of the generated IP, used for synthesis.
/example_design/bench/ *.v	The simulation stimulus files for the Example Design.
/example_design/rtl/*.v	The top-level file of the Example Design and some module files used in the design.
/pnr/core_only/*.pds	The project file of the generated IP core.
/pnr/core_only/*.fdc	The constraint file of the generated IP core.
/pnr/example_design/*.pds	The project file of the Example Design.
/pnr/example_design/*.fdc	The constraint file of the generated Example Design.
/sim/modelsim/*.f	List of .v files required for Questasim simulation of the generated Example Design in the Windows environment.
/sim/modelsim/*.do	do script files and do waveform files for Questasim simulation of the generated Example Design in the Windows environment.
/sim/modelsim/*.bat	Scripts for Questasim simulation of the generated Example Design in the Windows environment.
/sim/modelsim/makefile	Scripts for Questasim simulation in the Linux environment.
/sim_lib/modelsim/*.vp	The nonplaintext RTL files of the generated IP, which can be used for ModelSim or VCS simulation.
readme.txt	The readme file describes the directory structure of the generated files after the IP is generated.

2.3.2 Constraint Configuration

Attention:

The .fdc constraint files generated with the IP are for reference only; please modify the pin constraints according to the package and pin connections before using.

For specific configuration of the constraint file, please refer to the relevant help documents under the PDS installation path: "***User_Constraint_Editor_User_Guide***", "***Physical_Constraint_Editor_User_Guide***", and "***Route_Constraint_Editor_User_Guide***".

2.3.3 Simulation Runs

Attention:

When users perform a system-level simulation with the generated IP design, the Local end and Link Partner must use a same source clock or source synchronous clock, otherwise the simulation will fail due to frequency offset.

Under the Windows operating system, after the IP is generated, Questasim simulation can be run by double-clicking the sim.bat file in the "<project_path>/sim/modelsim" path.

Under the Linux system, after the IP is generated, Questasim simulation can be run by entering "make all" in the [Terminal] at the "<project_path>/sim/modelsim" path.

The simulation of SGMII over LVDS IP is based on the Test Bench of the Example Design. For detailed information about Example Design, please refer to "2.4 Example Design".

For more detailed information on PDS simulation functions and third-party simulation tools, please refer to the relevant help documents under the PDS installation path: "***Pango_Design_Suite_User_Guide***", "***Simulation_User_Guide***".

2.3.4 Synthesis and Placement/Routing

The specific usage of PDS synthesis tools and placement/routing tools can be found in the help documents within the PDS installation path.

Attention:

Example Design project files .pds and pin constraint files .fdc generated with the IP are located in the "/pnr/example_design" directory, and physical constraints need to be modified according to the actual devices, packages, and PCB trace routing. For details, please refer to "2.8 Descriptions and Considerations".

2.3.5 Resources Utilization

Table 2-4 Typical Resource Utilization Values for SGMII over LVDS IP Based on Applicable Devices

Device	Configuration Mode	Typical Resource Utilization Values				
		LUT	FF	PPLL[5]	BUFR[5]	IOCLKBUF[5]
PG2L25H	Enable auto-negotiation and MDIO	1126	1312	1	3	1
	Disable auto-negotiation and MDIO	879	972	1	3	1
PG2L50H	Enable auto-negotiation and MDIO	1156	1237	1	3	1
	Disable auto-negotiation and MDIO	921	961	1	3	1
PG2L100HX	Enable auto-negotiation and MDIO	1089	1313	1	3	1
	Disable auto-negotiation and MDIO	853	961	1	3	1
PG2L200H	Enable auto-negotiation and MDIO	1174	1315	1	3	1
	Disable auto-negotiation and MDIO	907	962	1	3	1
PG2T70H	Enable auto-negotiation and MDIO	1094	1313	1	3	1
	Disable auto-negotiation and MDIO	856	961	1	3	1
PG2T160H	Enable auto-negotiation and MDIO	1126	1312	1	3	1
	Disable auto-negotiation and MDIO	885	972	1	3	1
PG2T390HX	Enable auto-negotiation and MDIO	1125	1237	1	3	1
	Disable auto-negotiation and MDIO	901	954	1	3	1
PG2K400	Enable auto-negotiation and MDIO	1165	1315	1	3	1
	Disable auto-negotiation and MDIO	900	962	1	3	1

2.4 Example Design

This section mainly introduces the Example Design scheme based on SGMII over LVDS IP. This scheme involves instantiating a MAC Side SGMII IP and a PHY Side SGMII IP that interface with each other to perform auto-negotiation, followed by data transmission, and using CRC to verify the

5 FPGA clock resources. For detailed functions, please refer to *"**UG040004_Logos2 Family FPGAs Clock Resources (Clock) User Guide**"*, *"**UG050004_Titan2 Family FPGA Clock Resources (Clock) User Guide**"*, and *"**UG100004_Kosmo2 Family SoPC Clock Resource (Clock) User Guide**"*.

accuracy of the data at the receiver. The scheme performs read and write register operations on the SGMII Core via the MDIO interface.

2.4.1 Design Block Diagram

The system block diagram of the Example Design is as shown in Figure 2-7.

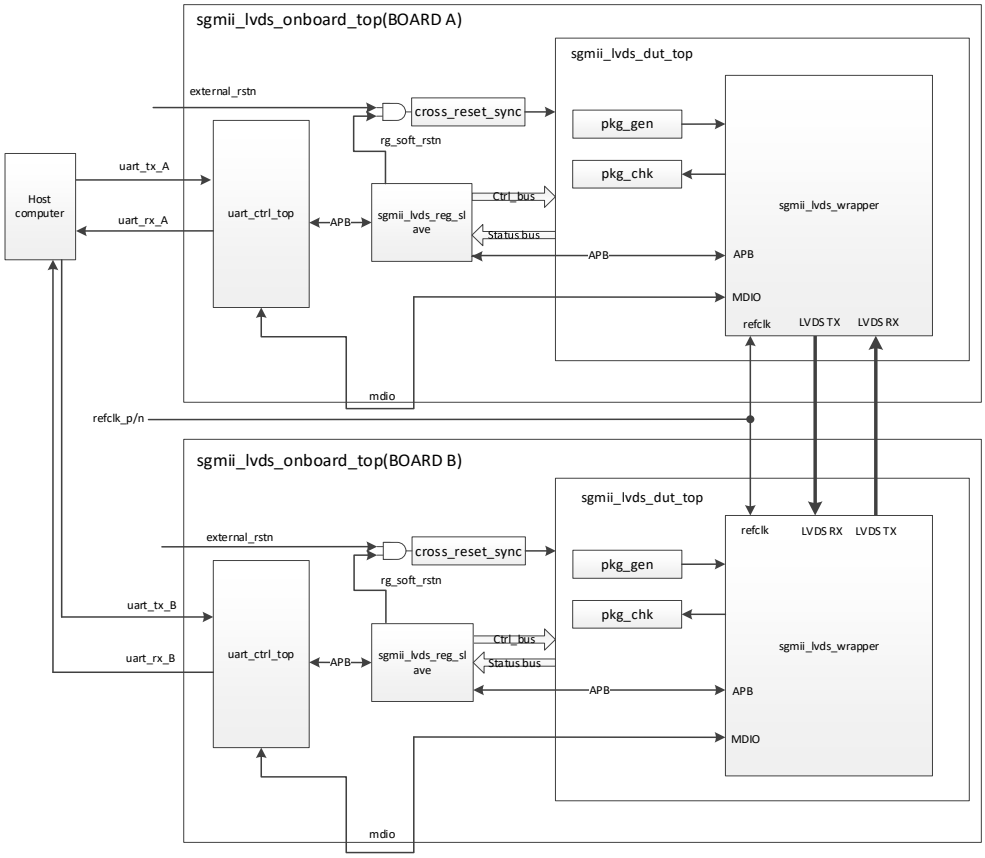

Figure 2-7 Example Design Block Diagram

2.4.2 Module Description

2.4.2.1 uart_ctrl_top

A serial port module used for debugging, for receiving UART data with a fixed baud rate of 115200, outputting in data formats required by APB or MDIO protocols. For read and write operations, the address is 24 bits, and the data is 32 bits.

2.4.2.1.1 Read and Write Operation Description

- Read operation format: "0x72" + "address";
- Write operation format: "0x77" + "address" + "data".

For the read and write operation examples, please refer to "2.8.7 Example of read and write operations for the uart_ctrl_top module".

2.4.2.1.2 Address description

For information about the address for accessing registers through the uart_ctrl_top module, please refer to Table 2-5.

Table 2-5 uart_ctrl Module Address Description

Address bits	Description
Access the IP register via APB[6]/ sgmii_lvds_reg_slave register[7]	
23:21	Reserved and set to "0".
20	Set to 0 when accessing registers through the APB interface; Set to 1 when accessing registers through the MDIO interface; Here, it should be set to "0".
19:9	Reserved and set to "0".
8	1'b0: Access the IP register through the APB interface; 1'b1: Access the register of sgmii_lvds_reg_slave module through the APB interface.
6:0	Access the IP Register: [6:2] corresponds to the IP register address [4:0]; Access sgmii_lvds_reg_slave: [6:0] corresponds to the sgmii_lvds_reg_slave address [6:0]. For the sgmii_lvds_reg_slave register, please refer to Table 2-6.
Access the IP register via MDIO[6]	
23:21	Reserved and set to "0".
20	Set to 0 when accessing registers through the APB interface; Set to 1 when accessing registers through the MDIO interface. Here, it should be set to "1".
19:18	MDIO ST (start of frame), MDIO frame start bit, set to 01.
17:16	MDIO OP(operation code) 2'b10: Read; 2'b01: Write.
15:13	Reserved and set to "0".

6 For the IP register, please refer to "2.6 Description of the IP Register".

7 For the sgmii_lvds_reg_slave register, please refer to "2.4.2.2 sgmii_lvds_reg_slave".

Address bits	Description
12:8	MDIO PHY Address[4:0].
7:5	Reserved and set to "0".
4:0	For Management Register Address [4:0], please refer to "2.6.1 Register Description".

2.4.2.2 sgmii_lvds_reg_slave

For the custom register module used for debugging, please refer to Table 2-6 for relevant register descriptions.

Table 2-6 sgmii_lvds_reg_slave Register Description

Register address (7bit)	R/W	Description	Default value (32 bits)
0x00	R/W	bit 28: pin_cfg_en port configuration enabled. 1'b 0: port configuration is invalid (default); 1'b 1: port configuration enabled. bit24: phy_duplex. (Defaults to 1'b1, Full Duplex) bit20: phy_link. (Defaults to 1'b1, Link Up) bit[17:16]: phy_speed 2'b11: reserved; 2'b10:SGMII 1000Mbps (default); 2'b01:SGMII 100Mbps; 2'b00:SGMII 10Mbps. bit12: unidir_en, unidirectional mode 1'b1: Undirectional mode enabled; 1'b0: Undirectional mode not enabled (default). bit8: loopback, pcs core loopback configuration 1'b1: pcs core loopback enabled; 1'b0: pcs core loopback not enabled (default). bit4: an_enable, auto-negotiation enable. 1'b 0: auto-negotiation not enabled; 1'b 1: auto-negotiation not enabled. (Default) bit0: an_restart, restart auto-negotiation. 1'b 0: auto-negotiation restart not enabled (default); 1'b 1: auto-negotiation restart enabled. Undefined bit positions: Reserved.	0x01_12_00_10
0x02	R/W	bit0: start_test. 1'b 0: packet transmission stop (default) 1'b1: packet transmission start. bit[31:1]: Reserved.	0x0
0x06	R	bit[31:0]: pkg_gen_cnt Number of transmitted data packets.	0x0
0x07	R	bit[31:0]: crc_ok_cnt Number of correct data packets received.	0x0
0x08	R	bit[31:0]: crc_err_cnt Number of error data packets received.	0x0

2.4.2.3 cross_reset_sync

Signal synchronisation module, used for synchronising and debouncing externally input asynchronous signals.

2.4.2.4 pkg_gen

Frame generation module, used for producing transmission data.

2.4.2.5 pkg_chk

Frame detection module, used for CRC verification of received data.

2.4.2.6 sgmii_lvds_wrapper

SGMII over LVDS IP top module.

2.4.3 Descriptions of Ports

Table 2-7 List of Example Design Interface Signals

Port	I/O	Bit width	Description
free_clk	I	1	External reference clock Frequency: 50MHz
ext_rstn	I	1	System reset signal 1: Reset release 0: Reset
cfg_rstn	I	1	Serial Port reset signal. 1: Reset release 0: Reset
ok_led	O	1	Packet reception verification correct indicator 0: Light off (verification error) 1: Light on (verification correct)
pll_ready	O	1	PLL lock indicator of the interface 0: Unlocked 1: Locked
lvds_phy_ready	O	1	Interface initialization and synchronization complete indicator 0: Interface initialization or synchronization not completed 1: Interface initialization complete and synchronization completed
an_status	O	1	SGMII link status indicator 0: link issue 1: link normal

Port	I/O	Bit width	Description
refclk_p	I	1	Interface differential reference clock input P side Frequency: 125MHz, global clock port
refclk_n	I	1	Interface differential reference clock input N side Frequency: 125MHz, global clock port
TXP	O	1	SGMII TX data P side
TXN	O	1	SGMII TX data N side
RXP	I	1	SGMII RX data P side
RXN	I	1	SGMII RX data N side
master_mdc_o	O	1	MDIO output clock (generated by the serial port module)
master_mdio	IO	1	MDIO data signal
slave_mdc	I	1	MDIO input clock (connected to master_mdc_o)
slave_mdio	IO	1	MDIO data signal (connected to master_mdio)
uart_txd	O	1	Serial port for sending data from the local side to the host computer
uart_rxd	I	1	Serial port for receiving data from the host computer to the local side

2.4.4 Test Method

Instantiate the customized IP and generate the bitstream using the IP's own Example Design project. Use two test boards for link tests; one with the MAC Side bitstream programmed, and the other with the PHY Side bitstream programmed; evaluate the test results based on the link indicators and CRC verification.

2.4.5 Instance Configuration

2.4.5.1 MAC Side

Figure 2-8 MAC Side Configuration Diagram

2.4.5.2 PHY Side

Figure 2-9 PHY Side Configuration Diagram

2.4.6 Instance Simulation

For instance simulation, please refer to "2.3.3 Simulation Runs".

2.5 Descriptions of IP Interfaces

This section provides the SGMII over LVDS IP related ports instructions and timing descriptions.

2.5.1 IP Interface Description

Table 2-8 SGMII over LVDS IP Interface Signal List

Port	I/O	Bit width	Description
Clock Signal			
i_core_clk_125	I	1	125MHz clock (regional clock network)
i_iol_serclk_625	I	1	625MHz clock (IO clock network)
i_iol_clkdiv_208	I	1	208.333MHz clock (regional clock network)
i_calib_clk_104	I	1	104.167MHz clock (regional clock network)
Reset signal			
tx_rst_n	I	1	TX reset 0: Reset 1: Reset release
rx_rst_n	I	1	RX reset 0: Reset 1: Reset release
cfg_rst_n	I	1	Configuration module reset 0: Reset 1: Reset release

Port	I/O	Bit width	Description
MDIO Signals[8]			
mdc	I	1	Management Data Clock, used for the MDIO interface clock This port must have a clock input when the MDIO interface is enabled Frequency: 2.5MHz
mdi	I	1	Management Data In
mdo	O	1	Management Data Out
mdo_en	O	1	Output enable control signal 1: mdo valid 0: mdo invalid
phy_addr	I	5	Input MDIO PHY address[9]
APB Signals[10]			
pclk	I	1	APB interface clock
paddr	I	7	APB address signal
pwrite	I	1	APB write enable signal (active high)
psel	I	1	APB selection signal (active high)
penable	I	1	APB enable signal (active high)
pwdata	I	32	APB write data signal
prdata	O	32	APB read data signal
pready	O	1	APB interface read/write Ready signal
Fast Configuration Ports			
pin_cfg_en	1	1	Fast configuration port enable[11] 1: The fast configuration port is valid (directly written to the configuration register). 0: The fast configuration port is invalid (written to the configuration register through the CPU configuration interface)
phy_link	I	1	PHY Link status (meaningful in PHY mode) 1:Link Up 0:Link Down Corresponding to register Reg4.15
phy_duplex	I	1	PHY duplex status (meaningful in PHY mode) 1: Full duplex 0: Non-full duplex Corresponding to register Reg4.12

8 Valid when configuring the management interface as MDIO, please refer to "2.3.1.2 IP Parameter Configuration".

9 MDIO read/write operations are valid if they match the PHY address on mdi; if not, invalid.

10 Valid when configuring the management interface not as MDIO, please refer to "2.3.1.2 IP Parameter Configuration".

11 Fast configuration of registers only affects Reg0 and Reg4, and does not affect other registers. For details, please refer to "2.5.3 Fast Configuration Interface".

Port	I/O	Bit width	Description
phy_speed	I	2	PHY operational speed (meaningful in PHY mode) 11: Reserved 10: 1000 Mbps 01: 100 Mbps 00: 10 Mbps In PHY mode Corresponding to registers Reg4.11:10 when auto-negotiation is enabled Corresponding to registers Reg0.6 and Reg0.13 when auto-negotiation is disabled In MAC mode Meaningless when auto-negotiation is enabled Corresponding to registers Reg0.6 and Reg0.13 when auto-negotiation is disabled
unidir_en	I	1	Unidirectional mode enable 1: Enabled 0: Not enabled Corresponding to register Reg0.5
an_restart	I	1	Auto-negotiation restart control 1: Restart auto-negotiation 0: Normal operation Corresponding to register Reg0.9
an_enable	I	1	Auto-negotiation enable control 1: Enabled 0: Not enabled Corresponding to register Reg0.12
loopback	I	1	PCS Core internal loopback control 1: Loopback enabled 0: Loopback not enabled Corresponding to register Reg0.14
MISC			
sgmii_clk	O	1	SGMII operating clock (125MHz, regional clock network)
tx_clken	O	1	Clock enable for TX rate matching (active high), related to PHY Device Speed Speed=11: Reserved Speed=10: SGMII 1000 Mbps (always asserted) Speed =10: SGMII 100 Mbps (assert one clock period every 10 clock cycles) Speed =00: SGMII 10 Mbps (assert one clock period every 100 clock cycles)
rx_clken	O	1	Clock enable for RX rate matching (active high), related to PHY Device Speed Speed=11: Reserved Speed=10: SGMII 1000 Mbps (Always asserted) Speed =10: SGMII 100 Mbps (Assert one clock period every 10 clock cycles) Speed =00: SGMII 10 Mbps (Assert one clock period every 100 clock cycles)
tx_rstn_out	O	1	Reset signal provided by the IP to the user-side TX logic (active low)
rx_rstn_out	O	1	Reset signal provided by the IP to the user-side RX logic (active low)
cfg_rstn_out	O	1	Configuration reset output (active low)

Port	I/O	Bit width	Description
SGMII Interface			
TXP	O	1	SGMII TX data P side
TXN	O	1	SGMII TX data N side
RXP	I	1	SGMII RX data P side
RXN	I	1	SGMII RX data N side
GMII Interface			
gmii_rxd	O	8	GMII RXD[7:0] signal
gmii_rx_dv	O	1	GMII RX_DV signal
gmii_rx_er	O	1	GMII RX_ER signal
gmii_txd	I	8	GMII TXD[7:0] signal
gmii_tx_en	I	1	GMII TX_EN signal
gmii_tx_er	I	1	GMII TX_ER signal
Status Indicator			
status_vector	O	12	PCS Core output status indicators. The field definitions are as follows: Bit[11]: resolve_priority Controls the Invocation of the Priority Resolution Function. This signal is asserted during the auto-negotiation IDLE_DETECT and LINK_OK states, and desserted in other states Bit[10]: an_complete Auto-negotiation completion indication: Bit[9]: an_page_rx New configuration data received during auto-negotiation Bit[8]: rxdisp_er 10B/8B decoding polarity error Bit[7]: rxdec_er 10B/8B decoding data error Bit[6]: remote_fault_encode Received link status from Link Partner during auto-negotiation In SGMII MAC mode: 1: Link down 0: Link up In SGMII PHY mode: Fixed to 0: Bit[5]: Duplex 1: Full Duplex 0: Half Duplex Bit[4:3]: speed[1:0] 11: Reserved 10: 100Mbps 01: 100Mbps 00: 10Mbps Bit[2:1]: rx_unitdata_indicate[1:0] 01: Invalid, an error occurred while receiving C-code or I-code; 10: /C/, receiving C-code 11: /I/, receiving I-code Bit[0]: link_status When auto-negotiation is enabled: 1: Synchronization successful and auto-negotiation completed 0: Synchronization failed and auto-negotiation not completed

Port	I/O	Bit width	Description
			When auto-negotiation is disabled: 1: Synchronization successful 0: Synchronization failed
init_cal_done	O	1	Indicator signal for LVDS interface initialization 1: Interface initialization completed 0: Interface initialization not completed
lsm_synced	O	1	Synchronization status 1: Synchronous 0: synchronization not completed
AN_CS	O	4	Current state of the PCS Core auto-negotiation state machine
AN_NS	O	4	Next state of the PCS Core auto-negotiation state machine
RS_CS	O	5	Current state of the PCS Core receive state machine
RS_NS	O	5	Next state of the PCS Core receive state machine
TS_CS	O	5	Current state of the PCS Core transmit state machine
TS_NS	O	5	Next state of the PCS Core transmit state machine
xmit	O	2	xmit signal output by the auto-negotiation state machine 00: Reserved 01: CONFIGURATION 10: DATA 11: IDLE
rx_unitdata_indicate	O	2	Signal to indicate type of data, received from PCS 00: Reserved 01: Invalid 10: /C/ 11: /I/
pcs_txk	I	1	Indicates current PCS data type
pcs_tx_dispctrl	I	1	8B/10B encoding forced polarity control signal {tx_dispctrl ,tx_dispsel} 00: Default 01: I2 replaced with I1 10: Disparity forced to be negative 11: Disparity forced to be positive
pcs_tx_dispsel	I	1	Please refer to pcs_tx_dispctrl signal description
pcs_txd	I	8	Data signal transmitted by PCS
pcs_rxk	I	1	Indicates the current data type received by the PCS
pcs_rdisp_er	O	1	10B/8B decoding polarity error indicator signal 1: Decoding polarity error 0: Decoding polarity normal
pcs_rdec_er	O	1	10B/8B decoding status indicator 1: Invalid codes found in data decoding 0: Data decoding normal
pcs_rxd	O	8	Data signal received by PCS rx_sm
transmitting	O	1	PCS transmit status indicator 1. PCS is in transmit status 0: PCS is not in transmit status
receiving	O	1	PCS receive status indicator 1. PCS is in receive status 0: PCS is not in receive status
delayctrl_current	O	8	IODELAY delay steps in the main data path in auto Training mode (Debug signal)

Port	I/O	Bit width	Description
left_margin	O	8	Delay steps corresponding to left boundary of the data window (Debug signal)
right_margin	O	8	Delay steps corresponding to right boundary of the data window (Debug signal)
LVDS_CS	O	20	Current State of the Re-timing state machine for the LVDS interface (Debug signal)
Loopback Interface			
i_farend_loop	I	1	Control port to enable LVDS transceiver far-end loopback 1: Enabled 0: Not enabled
i_nearend_loop	I	1	Control port to enable LVDS transceiver near-end loopback 1: Enabled 0: Not enabled

2.5.2 Configuration Management Interface

SGMII over LVDS IP provides two types of configuration management interfaces - APB and MDIO interfaces. Users can enable/disable the MDIO interface by configuring the MDIO Enable graphic option. For detailed descriptions, please refer to "2.3.1.2 IP Parameter Configuration".

- When the MDIO interface is not enabled, SGMII over LVDS IP operates the PCS Core management registers via the APB interface.
- When the MDIO interface is enabled, SGMII over LVDS IP operates the PCS Core management registers via the MDIO interface.

2.5.2.1 APB Interface Timing

2.5.2.1.1 APB Write Timing

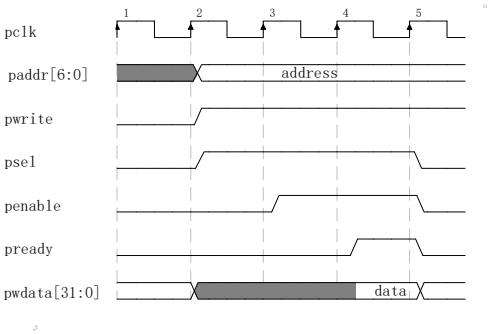

Figure 2-10 Basic APB Write Timing

2.5.2.1.2 APB Read Timing

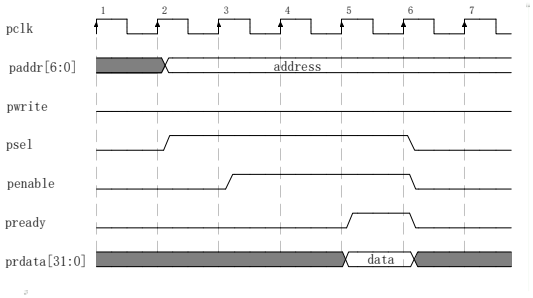

Figure 2-11 Basic APB Read Timing

2.5.2.2 MDIO Interface Timing

2.5.2.2.1 MDIO Write Timing

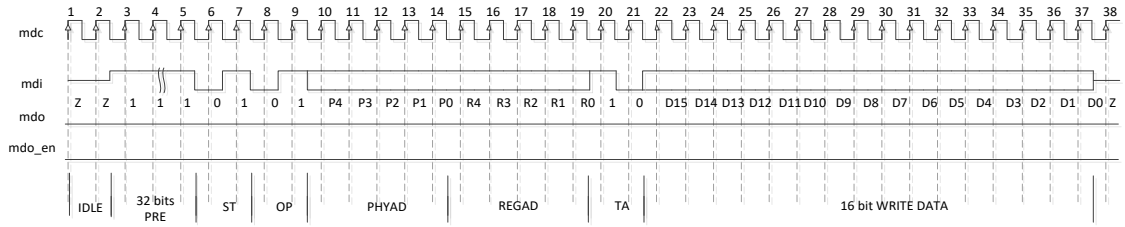

Figure 2-12 MDIO Write Timing

2.5.2.2.2 MDIO Write Timing

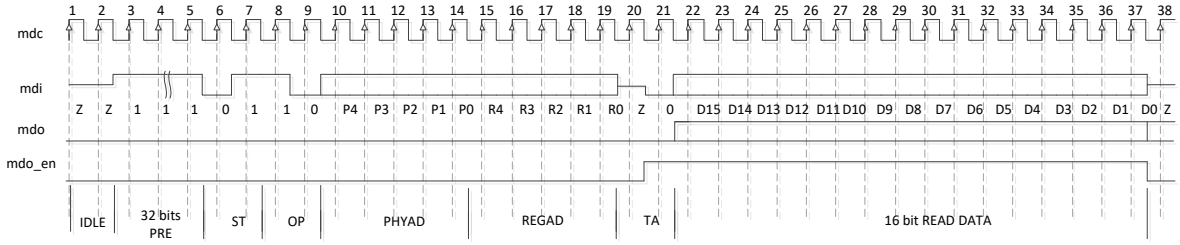

Figure 2-13 MDIO Write Timing

2.5.3 Fast Configuration Interface

The fast configuration interface allows for quick configuration of registers Reg0 and Reg4. When the fast configuration enable signal is active, the configuration information can be written directly to the corresponding configuration registers. Timing requirements are as follows:

- The fast configuration enable signal must be kept high for at least one cycle relative to configuration management interface clock;
- The configuration value must remain stable for at least one cycle relative to configuration management interface clock.

When the fast configuration enable signal is valid, registers other than Reg0 and Reg4 are written via the configuration management interface, and all registers are read via the configuration management interface; when the fast configuration interface enable signal is not valid, all registers are read and written via the configuration management interface.

2.5.4 GMII Interface

2.5.4.1 GMII Transmit Timing

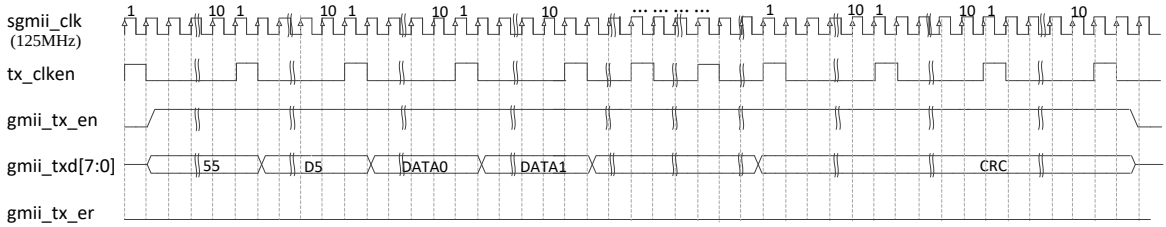

Figure 2-14 GMII Transmit Timing at a Rate of 100Mbps

Attention:

At a rate of 10Mbps, tx_clken is pulled high every 100 cycles of the 125MHz clock, with each data lasting for 100 cycles of the 125MHz clock;

At a rate of 100Mbps, tx_clken is pulled high every 10 cycles of the 125MHz clock, with each data lasting for 10 cycles of the 125MHz clock;

At a rate of 1000Mbps, tx_clken is high throughout, with each data lasting for 1 cycle of the 125MHz clock.

2.5.4.2 GMII Receive Timing

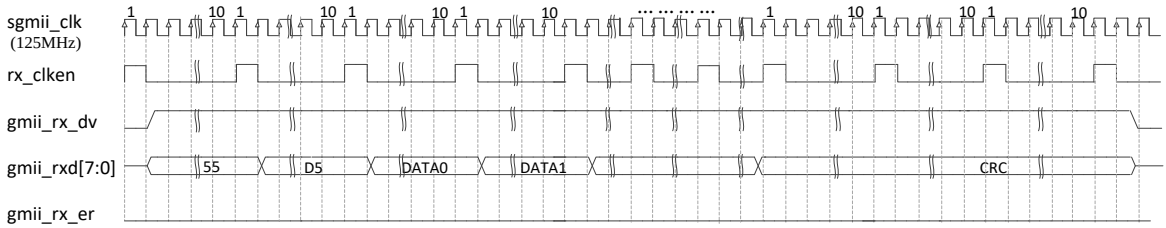

Diagram 2-15 GMII Receive Timing at a Rate of 100Mbps

Attention:

At a rate of 10Mbps, rx_clken is pulled high every 100 cycles of the 125MHz clock, with each data lasting for 100 cycles of the 125MHz clock;

At a rate of 100Mbps, rx_clken is pulled high every 10 cycles of the 125MHz clock, with each data lasting for 10 cycles of the 125MHz clock;

At a rate of 1000Mbps, rx_clken is high throughout, with each data lasting for 1 cycle of the 125MHz clock.

2.6 Description of the IP Register

SGMII over LVDS IP Registers can be configured through the configuration management interface (MDIO or APB interface)[12] or via ports directly[13].

2.6.1 Register Description

2.6.1.1 Register Definition

Table 2-9 Register Definitions When Auto-Negotiation is Enabled

Address (5 bits)	Register	Description
0x00	Control Register (Register 0)	Configure parameters for the SGMII module function.
0x01	Status Register (Register 1)	SGMII module status parameters.

12 Refer to "MDIO Signal" and "APB Signal" in Table 2-8.

13 Refer to the "Fast Configuration Ports" in Table 2-8.

Address (5 bits)	Register	Description
0x02	PHY Identifier Register2 (Register 2)	PHY ID.
0x03	PHY Identifier Register3 (Register 3)	PHY ID.
0x04	Auto-Negotiation Advertisement (Register 4)	Auto-negotiation capability values of the local device.
0x05	Auto-Negotiation Link Partner Ability Base (Register 5)	Auto-negotiation capability values of the remote device.
0x06	Auto-Negotiation Expansion Register (Register 6)	Auto-negotiation expansion register.
0x0f	Extended Status Register (Register 15)	Extended status register.
0x10	Vender_spc Register (Register 16)	Transceiver delay/path control register.
0x11	Vender_spc_1 Register (Register 17)	Loopback control registers.

Table 2-10 Register Definitions When Auto-Negotiation is Disabled

Address (5 bits)	Register	Description
0x00	Control Register (Register 0)	Configure parameters for the SGMII module function.
0x01	Status Register (Register 1)	SGMII module status parameters.
0x02	PHY Identifier Register2 (Register 2)	PHY ID.
0x03	PHY Identifier Registe3 (Register 3)	PHY ID.
0x0f	Extended Status Register (Register 15)	Extended status register.
0x10	Vender_spc Register (Register 16)	Transceiver delay/path control register.
0x11	Vender_spc_1 Register (Register 17)	Loopback control registers.

2.6.1.2 Register List

Attention:

Reset will set all registers to default values.

The register with "self-clearing" property, which, after being configured via the register management interface, will automatically reset to zero after one clock cycle of the configuration interface. When configuring self-clearing registers via the port, the self-clear function does not operate, default value should be written to clear.

The register with "read-to-clear" property, which immediately reset to zero after their value is read through the management configuration interface.

2.6.1.2.1 Register 0

Table 2-11 Control Register (Register 0)

Bit	Register	Description	Property	Defaults
0.15	Reset	1: Core reset 0: Normal Operation	Read /Write/Self-cleaning	1'b0
0.14	Loopback	1: Core loopback enabled 0: Core loopback not enabled During loopback, TX still sends data to the remote side;	Read/Write	1'b0
0.13	Speed Selection(LSB)	0.6:0.13 11 = Reserved 10 = 1000 Mb/s 01 = 100 Mb/s 00 = 10 Mb/s	Read/Write	1'b0
0.12	Auto-Negotiation Enable	Auto-negotiation enable register 1: Enable auto-negotiation 0: Diable auto-negotiation	Read /Write	1'b1
0.11	Reserved	Reserved	Read	1'b0
0.10	Reserved	Reserved	Read	1'b1
0.9	Restart Auto-Negotiation	Auto-negotiation restart Register 1: Restart auto-negotiation 0: Normal operation	Read /Write/Self-cleaning	1'b0
0.8	Duplex Mode	1: Full duplex 0: Half duplex The IP does not support half duplex	Read	1'b1
0.7	Reserved	Reserved	Read	1'b0
0.6	Speed Selection(MSB)	0.6:0.13 11 = Reserved 10 = 1000 Mb/s 01 = 100 Mb/s 00 = 10 Mb/s	Read/Write	1'b1
0.5	Unidirectional enable	Unidirectional mode enable register 1: Enabled. The status in the RX direction does not affect the operation in the TX direction. 0: Not enabled. Transmission is enabled only after Link up;	Read/Write	1'b0
0.4:0	Reserved	Reserved	Read	5'b00000

2.6.1.2.2 Register 1

Table 2-12 Status Register (Register 1)

Bit	Register	Description	Property	Defaults
1.15:9	Reserved	Reserved	Read	7'b0000000
1.8	Extended Status	AN_Extened Status Register(reg15) supported status	Read	1'b1

Bit	Register	Description	Property	Defaults
1.7	Unidirectional ability	States Supported by Unidirectional Mode	Read	1'b1
1.6	Reserved	Reserved	Read	1'b0
1.5	Auto-Negotiation Complete	Auto-negotiation completion indication: 1: Auto-negotiation completed 0: Auto-negotiation not completed	Read	1'b0
1.4	Remote Fault	MAC Side: 1: PHY Link Status received as 0 0: PHY Link Status received as 1 PHY Side: Constantly 0	Read/Read-to-Clear/LH	mac mode: 1'b1; phy mode: 1'b0;
1.3	Auto-Negotiation Ability	States supported by auto-negotiation capability	Read	1'b1
1.2	Link Status	When auto-negotiation is enabled: 1: Synchronous and auto-negotiation completed 0: Synchronization or auto-negotiation not completed When auto-negotiation is disabled: 1: Synchronized 0: Synchronization failed	Read/Read-to-Clear/LL	1'b0
1.1:0	Reserved	Reserved	Read	1'b0

2.6.1.2.3 Register2 & 3

Table 2-13 PHY Identifier Register (Register 2 & 3)

Bit	Register	Description	Property	Defaults
Reg2[15:0]	Organizationally Unique Identifier	Organizationally Unique Identifier[3:18]	Read/Write	16'h0000
Reg3[15:10]	Organizationally Unique Identifier	Organizationally Unique Identifier[19:24]	Read/Write	6'b000000
Reg3[9:4]	Manufacturer's Model Number	Manufacturer's Model Number	Read/Write	6'b000000
Reg3[3:0]	Revision Number	Revision Number	Read/Write	4'b0000

2.6.1.2.4 Register4

Table 2-14 Auto-Negotiation Advertisement PHY Mode (Register 4)

Bit	Register	Description	Property	Defaults
4.15	PHY Link Status	phy_link control: 1: Link up 0: Link down	Read/Write	1'b0
4.14	Acknowledge	Local side response bit	Read Only	1'b0
4.13	reserved	Reserved	Read Only	1'b0

Bit	Register	Description	Property	Defaults
4.12	duplex mode	phy_duplex control 1: full duplex 0: half duplex The IP does not support half-duplex, but this register can transmit upper layer configurations to the remote side through auto-negotiation;	Read/Write	1'b0
4.11:10	speed	phy_speed control 11 = Reserved 10: 1000Mb/s 01: 100Mb/s 00: 10Mb/s	Read/Write	2'b00
4.9:1	reserved	Reserved	Read Only	9'h000
4.0	reserved	Reserved	Read Only	1'b1

Table 2-15 Auto-Negotiation Advertisement MAC Mode (Register 4)

Bit	Register	Description	Property	Defaults
4.15:0	Fixed value	Fixed value	Read	16'h4001

Attention:

SGMII MAC Side speed uses the speed of the remote side, with the default speed being 1000Mbps.

2.6.1.2.5 Register5

Table 2-16 Auto-Negotiation Link Partner Ability Register (Register 5)

Bit	Register	Description	Property	Defaults
5.15	PHY Link Status	phy_link control 1: Link up 0: Link down	Read Only	1'b0
5.14	Acknowledge	1: Acknowledged, indicating the remote side received the message 0: Not acknowledged, indicating the remote side did not receive the message	Read Only	1'b0
5.13	reserved	Reserved	Read Only	1'b0
5.12	duplex mode	1: Full duplex 0: Half duplex	Read Only	1'b0
5.11:10	speed	The speed of the remote side 11 = Reserved 10: 1000Mb/s 01: 100Mb/s 00: 10Mb/s	Read Only	2'b10
5.9:0	reserved	Reserved	Read Only	10'b0

2.6.1.2.6 Register6

Table 2-17 Auto-Negotiation Expansion Register (Register 6)

Bit	Register	Description	Property	Defaults
6.15:2	Reserved	Reserved	Read Only	14'd0
6.1	Page Received	1: A new Page message received 0: No new Page message received	Read Only	1'b0
6.0	reserved	Reserved	Read Only	1'b0

2.6.1.2.7 Register15

Table 2-18 Extended Status Register (Register 15)

Bit	Register	Description	Property	Defaults
15.15	1000BASE-X Full Duplex	1000BASE-X Full Duplex (Supported)	Read	1'b1
15.14	1000BASE-X Half Duplex	1000BASE-X Half Duplex (Not Supported)	Read	1'b0
15.13	1000BASE-T Full Duplex	1000BASE-T Full Duplex (Not Supported)	Read	1'b0
15.12	1000BASE-T Half Duplex	1000BASE-T Half Duplex (Not Supported)	Read	1'b0
15.11:0	Reserved	Reserved	Read	12'h000

2.6.1.2.8 Register16

Table 2-19 Vender_spc Register (Register 16)

Bit	Register	Description	Property	Defaults
16.15:8	mr_delayctrl_mannual	IODELAY delay steps for changing delay manually in the data path	Read/Write	8'h00
16.7:2	reserved	Reserved	Read	6'b000000
16.1	mr_path_force	1: Slave path forced to be the actual data path 0: Master path forced to be the actual data path	Read/Write	1'b0
16.0	mr_mannual_ctrl_vld	1: Manual control enable 0: Auto Training	Read/Write	1'b0

2.6.1.2.9 Register17

Table 2-20 Vendor_Spec_1 Register (Register 17)

Bit	Register	Description	Property	Defaults
17.15:2	reserved	Reserved	Read	14'h000
17.1	mr_farend_lpbk	1: Far-end loopback enabled 0: Far-end loopback disabled	Read/Write	1'b0
17.0	mr_nearend_lpbk	1: Near-end loopback enabled 0: Near-end loopback disabled	Read/Write	1'b0

2.7 Typical Applications

2.7.1 Single Lane Typical Applications

For typical applications of SGMII over LVDS IP in a single lane, please refer to "2.4 Example Design".

2.7.2 Multi Lane Typical Applications

This section introduces expansion schemes on the SGMII over LVDS Multi Lane interface. That is, it describes how to build a Multi Lane project with multiple channels based on the single Lane SGMII over LVDS IP by modifications. Users can refer to this Multi Lane scheme to modify the designs to meet actual needs.

The Multi Lane scheme diagram is shown in Figure 2-16.

- Clock and reset modules of channels in the same clock region (CLK Region) are shared;
- Clock and reset modules of channels in different clock regions (CLK Region) cannot be reused; external reference clock and reset sharing are supported.
- Independent reset signals of each channel are controlled by the global reset of the reset module.

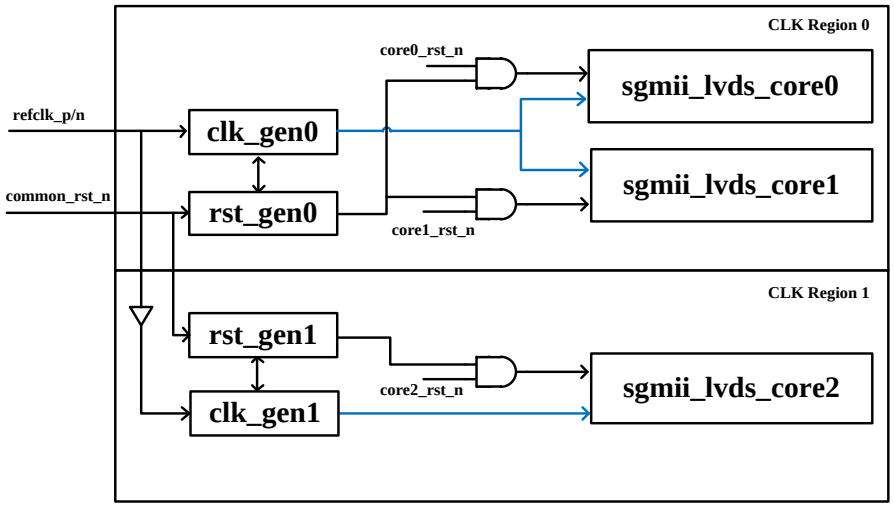

Figure 2-16 Multi Lane Scheme Diagram

Attention:

In Multi Lane application scenarios, users should determine the permitted number of extension channels based on the resource usage of the Clock Region.

The configuration interface of each channel can be achieved by adding additional chip selection signals or extended configuration addresses.

2.8 Descriptions and Considerations

2.8.1 Clock Signal

The multiple clocks required by the IP are generated by the clock module located at ".\example_design\rtl\clk_reset", with each clock in the clk_gen module assigned a clock buffer for clock propagation. The port descriptions are as shown in Table 2-21.

Table 2-21 clk_gen Interface Signal List

Port	I/O	Bit width	Description
refclk_p	I	1	Input reference clock P side, with a frequency of 125MHz
refclk_n	I	1	Input reference clock N side, with a frequency of 125MHz
pll_rst_n	I	1	PPLL reset signal: 0: PPLL reset 1: PPLL reset release
pll_lock	O	1	PPLL lock status indicator signal
iol_serclk_625	O	1	625MHz output clock, with the domain of the high-speed IO clock network

Port	I/O	Bit width	Description
iol_clkdiv_208	O	1	208.333MHz output clock, with the domain of the regional clock network
core_clk_125	O	1	125MHz output clock, with the domain of the regional clock network
calib_clk_104	O	1	104.167MHz output clock, with the domain of the regional clock network
clk_125_bufg	O	1	125MHz output clock, with the domain of the global clock

2.8.2 Reset signal

IP reset is generated by the reset module located at ".\example_design\rtl\clk_reset" and can implement PPLL, TX, RX, and configuration reset.

2.8.3 Physical Constraints

- The PPLL and the fabric resources used by the IP must be located in the same CLK Region. It is recommended to constrain the PPLL position.
- If the receiver has no external differential impedance, the internal impedance of the IO needs to be enabled. The following is an example of a constraint:

```
define_attribute {p:RXP} {PAP_IO_DIFF_IN_TERM_MODE} {ON}
define_attribute {p:RXN} {PAP_IO_DIFF_IN_TERM_MODE} {ON}
```

- Do not constrain the pin location of the interface receiver to the dedicated global clock pins.

2.8.4 LVDS Transceiver Module

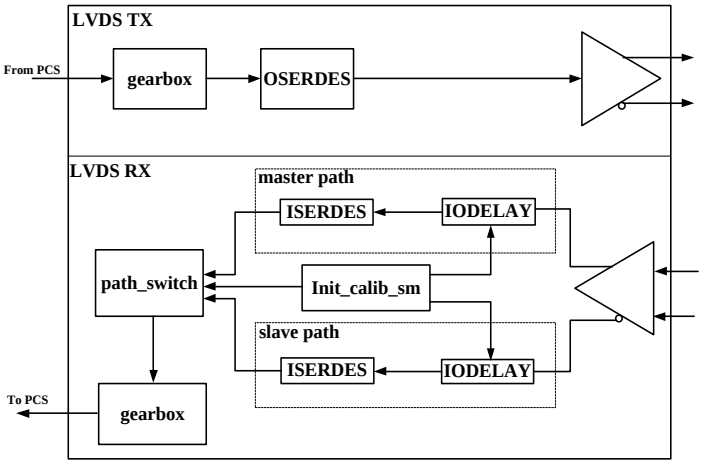

Figure 2-17 LVDS Transceiver Function Diagram

An LVDS transceiver is implemented using FPGA IO logic resources, primarily to accomplish the functions of serialization, deserialization, and data synchronization corresponding to the PMA. It supports the transmission of differential signals using LVDS25 or LVDS18 I/O standards. The functional diagram of the LVDS transceiver is shown in Figure 2-17. For related IO logic hardware primitives, please refer to "***UG040006_Logos2 Family FPGAs Input/Output Interface (IO) User Guide***", "***UG050006_Titan2 Family FPGA Input/Output Interface (IO) User Guide***", and "***UG100006_Kosmo2 Family SoPC Input/Output Interface (IO) User Guide***".

The parallel data transmitted by the PCS is converted to serial via OSERDES and then driven as a serial output at LVDS levels. The incoming serial data can be received via two paths as shown in Figure 2-17, namely the master path and the slave path. Sampling and serial-to-parallel conversion are performed in each path independently. One of the paths is then selected to convey the parallel data to the PCS.

The receiver of the transceiver enable automatic timing training by default. By adjusting the step of IODELAY in the path, stable sampling of RX serial data is achieved. Users can also manually control the selection of the master path and slave path, as well as the timing of serial data sampling, by accessing Register 16 of the IP Core and forcibly modifying the data path and the step of IODELAY.

Attention:

Manual adjustments are usually for interface debugging only.

If re-entering the automatic timing training mode is required after manual adjustments, RX must be reset.

2.8.5 Loopback Mode

The SGMII over LVDS IP supports three loopback modes, as shown in Figure 2-1:

- PCS core Loopback
- Transceiver near-end parallel loopback
- Transceiver far-end parallel loopback

2.8.5.1 PCS core Loopback

This loopback mode supports two types of configuration: port configuration and register configuration.

Table 2-22 PCS Core Loopback Port Configuration

Configuration Item	**Configuration Descriptions**
Port enable	pin_cfg_en=1, the port configuration is enabled
Loopback configuration	loopback=1
Non-Loopback configuration	loopback=0

Table 2-23 PCS Core Loopback Port Configuration

Configuration Item	**Configuration Descriptions**
Register enable	Pin_cfg_en=0, register configuration is enabled.
Loopback configuration	Reg0.14 Loopback=1'b1
Non-Loopback configuration	Reg0.14 Loopback=1'b0

2.8.5.2 Transceiver near-end parallel loopback

This loopback mode supports two types of configuration: port configuration and register configuration.

Table 2-24 Transceiver Near-End Loopback Port Configuration

Configuration Item	Configuration Descriptions
Loopback configuration	i_nearend_loop =1
Non-Loopback configuration	i_nearend_loop =0

Table 2-25 Transceiver Near-End Loopback Register Configuration

Configuration Item	Configuration Descriptions
Loopback configuration	Reg17.0 mr_nearend_lpbk =1'b1
Non-Loopback configuration	Reg17.0 mr_nearend_lpbk =1'b0

2.8.5.3 Transceiver far-end parallel loopback

This loopback mode supports two types of configuration: port configuration and register configuration.

Table 2-26 Transceiver Far-End Loopback Port Configuration

Configuration Item	Configuration Descriptions
Loopback configuration	i_farend_loop =1
Non-Loopback configuration	i_farend_loop =0

Table 2-27 Transceiver Far-End Loopback Register Configuration

Configuration Item	Configuration Descriptions
Loopback configuration	Reg17.1 mr_farend_lpbk =1'b1
Non-Loopback configuration	Reg17.1 mr_farend_lpbk =1'b0

2.8.6 IP Clock Scheme

The IP clock scheme is shown in Figure 2-18. For the related functions of clock buffers BUFR, BUFG, and IOCLKBUF in the figure, please refer to "***UG040004_Logos2 Family FPGAs Clock Resources (Clock) User Guide***", "***UG050004_Titan2 Family FPGA Clock Resources (Clock) User Guide***" and "***UG100004_Kosmo2 Family SoPC Clock Resource (Clock) User Guide***".

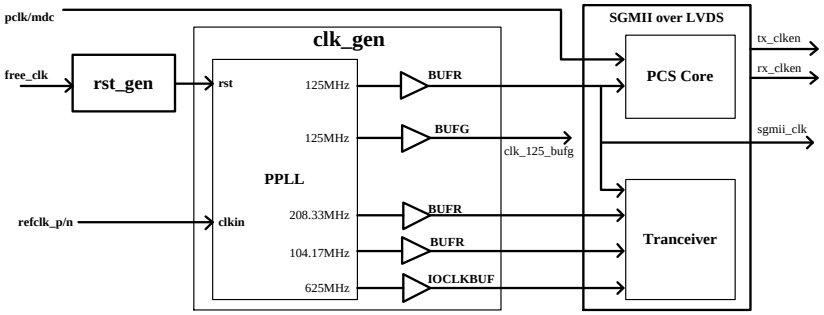

Figure 2-18 IP Clock Network Diagram

Attention:

Pay attention to the domain of each clock and the corresponding clock buffer;

The clk_gen module of the IP provides a 125MHz global lock (clk_125_bufg). Users can use this clock to synchronise GMII interface signals from the regional clock domain (sgmii_clk) to the global clock domain.

2.8.7 Example of read and write operations for the uart_ctrl_top module

2.8.7.1 Read Operation

Reading data from address 0x000001: "0x72"+"0x000001", which is 0x72000001.

2.8.7.2 Write Operation

Write 0x02 to address 0x000001: "0x77"+"0x000001"+"0x00000002", results in 0x7700000100000002.

2.9 IP Debugging Method

The IP provides several ports for monitoring the interface's working state. The port list is shown in Table 2-28.

Table 2-28 Debug Ports and Their Description

Port	**Port Description**
status_vector	PCS Core status indicator
init_cal_done	Training completion flag for LVDS interface initialization
lsm_synced	Interface synchronisation status, 1: synchronised; 0: not synchronised;
delayctrl_current	In automatic training mode, the final setting of IODELAY steps in the main data path (Debug signal)
left_margin	Delay steps corresponding to left boundary of the data window (Debug signal)
right_margin	Delay steps corresponding to right boundary of the data window (Debug signal)
LVDS_CS	The current state of the LVDS interface timing training state machine (Debug signal)

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