Logos Family PGL50H Device Configurable Multi-function PINs Application Guide

(AN02027, V1.1)

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Chapter 1 Overview

A configurable multi-function PIN can be used as a configuration interface during the configuration, and after the completion of the configuration, it can be used as a standard IO for the user in user mode. Some considerations on using a configurable multi-function PIN as a user IO shall be taken into account in the single board design. The configurable multi-function PINs are all on Bank0, Bank1, or Bank2. See details in Table 2-1 and Table 2-2. So there is no need to consider the application of configurable multi-function IOs in other banks.

Configurable multi-function PINs must be used with the considerations in mind to avoid the following problem scenario: When reconfiguring the FPGA by resetting it in user mode and using a configurable multi-function PIN as an output for user logic, then after resetting, the multi-function PIN output will be in a non-high impedance state for a brief period (less than 100ns) (some PINs at a high level and some at a low level) and not controlled by IO_STATUS_C.

The process is shown in the following figure:

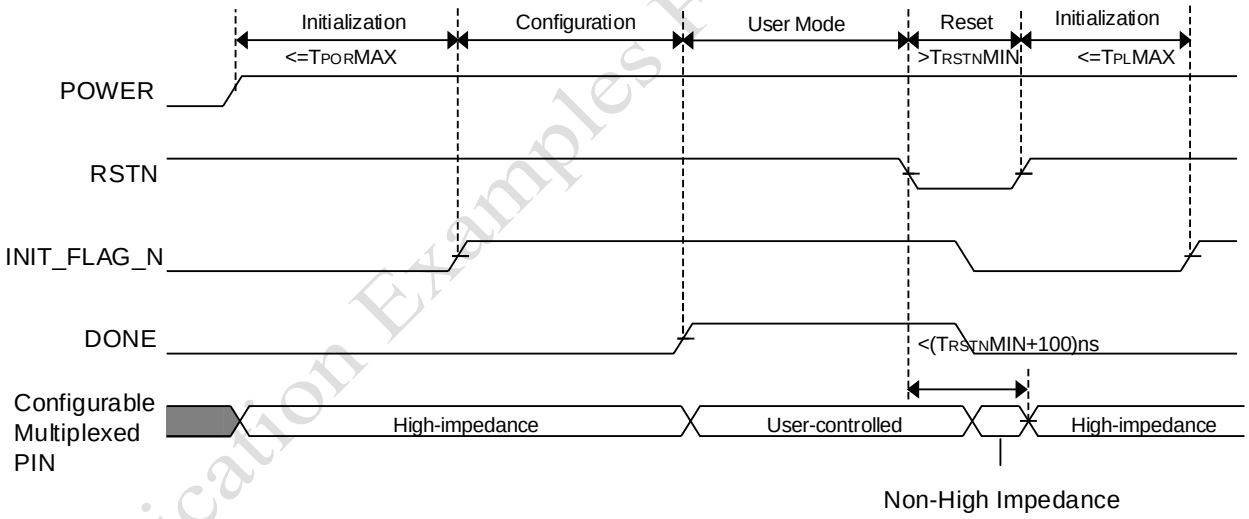

Figure 1-1 Non-High Impedance Process Diagram

For parameters in Figure 1-1, see the "DS02001_Logos Family FPGA Device Datasheet" under the Chapter "Power-up Timing Characteristics".

This scenario mainly affects applications that require an IO to maintain at a fixed level during the reconfiguration process. For example, a configurable multi-function PIN is used as the enable or reset signal for other devices, and an external pull-up (or pull-down) of the FPGA is applied to keep the signal at a fixed level during the configuration. In this case, it is expected that after the FPGA is reset, the multi-function PIN output will be in a high impedance state, but the existence of the

non-high impedance process may cause changes to the enable or reset signal, affecting the operation of other devices.

The possible triggers include:

1. Resetting FPGA in user mode
2. When resetting FPGA, a configurable multi-function PIN is used as a user output.

The following solutions are provided for single board design for this scenario.

Chapter 2 Requirements for Single Board Design

The design requirements are the following:

1. If a configurable multi-function PIN is used as an input in user mode, it will not affect the design.
2. If a Configurable Multi-function PIN is used as an output in user mode, the following considerations shall be observed.
    1) Pin IO_STATUS_C requires an external pull-up.
    2) If the configurable multi-function PIN used needs to be maintained at a fixed level during the configuration, select a pin using the following method: For a fixed high level, choose a pin from Table 2-1 and apply an external pull-up (A pull-up resistor of 4.7K is recommended); for a fixed low level, choose one from Table 2-2 and apply an external pull-down (A pull-down resistor of 4.7K is recommended). If the rules of Table 2-1 and Table 2-2 are not followed, the configurable multi-function PIN output may be abnormal.
    For example: If a signal needs to remain at a high level during the configuration, users can choose pins such as P21(BFCE_N) and P22(BFOE_N) and apply an external pull-up; if a signal needs to remain at a low level during the configuration, users can choose F18 (ADR25), F19(ADR24), etc. and apply an external pull-down.
    If there is no need to maintain at a fixed level, no action is required.

Table 2-1 Configurable Multi-function PINs that Can Remain at a High Level during Configuration

Bank Name	Pin Name (Function name)	Pin Number
B1	DIFFI_B1_31P/BFCE_N	P21
B1	DIFFI_B1_31N/BFOE_N	P22
B1	DIFFI_B1_32P/BFWE_N	R20
B1	DIFFI_B1_32N/BLDC	R22
B1	DIFFI_B1_33P/BHDC	T21
B2	DIFFIO_B2_1N/CSO_N	AA3
B2	DIFFIO_B2_15N/RWSEL/VREF_B2	Y8
B2	DIFFIO_B2_26N/GCLK0/PLL4_CLK8/PLL5_CLK8/ECCLK	AB13
B2	DIFFIO_B2_38P/MODE_1	Y19
B2	DIFFIO_B2_54N/MODE_0	AA21
B2	DIFFIO_B2_54P/CFG_CLK	Y20

Table 2-2 Configurable Multi-function PINs that Can Remain at a Low Level During Configuration

Bank Name	Pin Name (Function name)	Pin Number
B1	DIFFI_B1_0P/ADR25	F18
B1	DIFFI_B1_0N/ADR24/VREF_B1	F19
B1	DIFFI_B1_14P/ADR23	G19
B1	DIFFI_B1_14N/ADR22	F20
B1	DIFFI_B1_15P/ADR21	H18
B1	DIFFI_B1_15N/ADR20	H19
B1	DIFFI_B1_16P/ADR19	F21
B1	DIFFI_B1_16N/ADR18	F22
B1	DIFFI_B1_17P/ADR17	E20
B1	DIFFI_B1_17N/ADR16	E22
B1	DIFFI_B1_18P/ADR15	J19
B1	DIFFI_B1_18N/ADR14	H20
B1	DIFFI_B1_19P/ADR13	K19
B1	DIFFI_B1_19N/ADR12	K18
B1	DIFFI_B1_20P/ADR11	G20
B1	DIFFI_B1_20N/ADR10	G22
B1	DIFFI_B1_21P/ADR9	K17
B1	DIFFI_B1_21N/ADR8	L17
B1	DIFFI_B1_22P/ADR7	H21
B1	DIFFI_B1_22N/ADR6	H22
B1	DIFFI_B1_23P/ADR5	K20
B1	DIFFI_B1_23N/ADR4	L19
B1	DIFFI_B1_29P/ADR3	M21
B1	DIFFI_B1_29N/ADR2	M22
B1	DIFFI_B1_30P/ADR1	N20
B1	DIFFI_B1_30N/ADR0	N22
B1	DIFFI_B1_55N/DOUT_BUSY	V20
B2	DIFFIO_B2_1P/INIT_FLAG_N	Y4
B2	DIFFIO_B2_2N/D9	U6
B2	DIFFIO_B2_2P/D8	T7
B2	DIFFIO_B2_4N/D6	AB5
B2	DIFFIO_B2_4P/D5	Y5
B2	DIFFIO_B2_14N/D4	AB6
B2	DIFFIO_B2_14P/D3	AA6
B2	DIFFIO_B2_15P/D7	W9
B2	DIFFIO_B2_25N/GCLK30/PLL4_CLK6/PLL5_CLK6/D15	AB12
B2	DIFFIO_B2_25P/GCLK31/PLL4_CLK7/PLL5_CLK7/D14	AA12
B2	DIFFIO_B2_26P/GCLK1/PLL4_CLK9/PLL5_CLK9/D13	Y13

Bank Name	Pin Name (Function name)	Pin Number
B2	DIFFIO_B2_37N/D12	AB18
B2	DIFFIO_B2_37P/D11	AA18
B2	DIFFIO_B2_38N/D10	AB19
B2	DIFFIO_B2_39N/D2	T14
B2	DIFFIO_B2_39P/D1	R13
B2	DIFFIO_B2_52N/CS_N	AB20
B2	DIFFIO_B2_52P/D0	AA20

Users must verify based on the application to ensure that the pin meets application requirements at each stage.

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