SEU IP

User Guide

(UG042001, V1.12)

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Revisions History

Document Revisions

Version	Date of Release	Revisions	Applicable IP and Corresponding Versions
V1.12	30.04.2024	Initial release.	V1.12

IP Revisions

IP Version	Date of Release	Revisions
V1.12	30.04.2024	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
CCS	Configuration Controller System
CRAM	Configuration Random Access Memory
DRM	Dedicated RAM Module
IPAL	Internal Slave Parallel Interface
RAM	Random Access Memory
SEU	Single Event Upsets
TLR	Test Logic Reset
IPC	IP Compiler
PDS	Pango Design Suite

Related Documentation

The following documentation is related to this manual:

1. ***Pango_Design_Suite_Quick_Start_Tutorial***
2. ***Pango_Design_Suite_User_Guide***
3. ***IP_Compiler_User_Guide***
4. ***Simulation_User_Guide***
5. ***User_Constraint_Editor_User_Guide***
6. ***Physical_Constraint_Editor_User_Guide***
7. ***Route_Constraint_Editor_User_Guide***

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Chapter 1 Preface

This chapter describes the scope, structure, and writing standards of this manual to help users quickly find the information they need.

1.1 Background Introduction

When high-energy subatomic particles pass through the silicon in large-scale circuit storage units (flip-flops, register units, or RAM units), free charges are generated. These charges accumulate at the circuit nodes in an extremely short time interval. If the charge accumulation exceeds a certain level, the stored data will change, leading to system errors. As the damage it causes to the circuit is not permanent, this phenomenon is called a soft failure.

In FPGA devices, there are four types of storage involved: configuration storage units, DRM storage units, distributed RAM, and flip-flops. That is, soft failures may occur in all of these four types of storage units. The SEU IP is designed based on the error detection circuit in CCS of the device, targeted at addressing the soft failures of configuration storage units to help users mitigate system soft failures.

1.2 Introduction of the Manual

This manual is a user guide for the SEU IP launched by Pango Microsystems. The IP is based on the CCS resources of FPGA products. The content of this manual primarily includes the IP user guide and related information. This manual helps users quickly understand the features and usage of SEU IP.

1.3 Writing Standards of the Manual

Table 1-1 Description of Writing Standards

Text	**Rules**
Attention	If users ignore the attention contents, they may suffer adverse consequences or fail to operate successfully due to incorrect actions.
Description	Instructions and tips provided for users.
Recommendation	Recommended settings and instructions for users.

Chapter 2 IP User Guide

This chapter provides a guide on the use of SEU IP, including an introduction to IP, IP block diagram, IP generation process, Example Design, IP interface description, instructions and considerations, and IP debugging methods. More details on the design process can be found in the following PDS help documentation.

- "***Pango_Design_Suite_Quick_Start_Tutorial***"
- "***Pango_Design_Suite_User_Guide***"
- "***IP_Compiler_User_Guide*** "
- "***Simulation_User_Guide*** "

2.1 IP Introduction

The SEU IP launched by Pango Microsystems is used to address the soft failure issues of CRAM, and implement error detection, error correction, command input, and state output for CRAM based on the CCS resources of FPGA products. It can be configured and generated through the IP Compiler (IPC) tool in the Pango Design Suite (PDS).

2.1.1 Key Features

Table 2-1 Main Features of SEU IP

Features	**Feature Description**
Supports function initialization	Initialisation of the CRC value for the scanning frames.
Supports ECC function	Single-bit ECC.
	Multi-bit ECC.
Supports optional scanning of masked regions	PG2T390H/PG2T390HX: Optional scanning of LVDS masked regions
	PG2T390H/PG2T390HX: Optional scanning of different partitions in DDR masked regions.
	PG2L100H/PG2L100HX: Optional scanning of full-frame mask region.
Supports CRC enable configuration	Configurable to enable/disable.
Supports CRC error detection granularity configuration	Single frame/double frame/full CRAM.
Supports error correction enable configuration	Configurable to enable/disable.

Features	Feature Description
Supports error correction mode configuration	Repair mode: single-bit error correction.
	Replace mode: single-bit error, multiple-bit error, and CRC error (not full CRAM) corrections.
Supports heartbeat function	An impulse signal is generated every 100 clock cycles.
Supports error injection	Error injection via the Control and Monitor Interface and the Error Inject Interface.
Supports error report	Print error reports from the control and monitor interface.
Supports error statistics	Statistics of correctable and uncorrectable errors.

2.1.2 Applicable Devices and Packages

Table 2-2 SEU IP Applicable Devices and Package

Applicable Devices	Supported Packages
PG2L25H	ALL
PG2L50H	ALL
PG2L100H	ALL
PG2L100HX	ALL
PG2L200H	ALL
PG2T390H	ALL
PG2T390HX	ALL
PG2K400	ALL
PG2T70H	ALL
PG2T160H	ALL

2.1.3 IP Performance

2.1.3.1 Maximum Clock Frequency

The i_seu_clk frequency must not exceed the specified maximum frequency under any circumstances.

Table 2-3 Maximum Clock Frequency

Device	Maximum Frequency of i_seu_clk
PG2L25H	10MHz
PG2L50H	
PG2L100H	
PG2L100HX	
PG2L200H	
PG2T390H	
PG2T390HX	
PG2K400	
PG2T70H	
PG2T160H	

2.1.3.2 Time Consumption

Refer to Table 2-4 for operation times; the time consumption is given in clock cycles, and the specific duration needs to be calculated based on the clock frequency.

Table 2-4 Description of Operation Times

Device Name	Operation Type	Time Consumption[1]	Description
PG2L25H	Initialization	376,201 clock cycles	The time it takes for the IP to perform the initialization operation.
	Error detection	376,201 clock cycles	The time it takes to check the entire CRAM once when no errors are detected.
	Error injection	980 clock cycles	The time it takes to perform an error injection operation once.
	Error Repair	605 clock cycles	The time it takes to correct a single frame of data when a single-bit error is detected.
	Error Replace	605 clock cycles + "external memory readback time"	Time of reading back external memory depends on the external memory read back method, clock frequency, and other conditions. The correction times for single-bit errors, multi-bit errors, and CRC Only errors are the same.
PG2L50H	Initialization	576,409 clock cycles	The time it takes for the IP to perform the initialization operation.
	Error detection	576,409 clock cycles	The time it takes to check the entire CRAM once when no errors are detected.
	Error injection	980 clock cycles	The time it takes to perform an error injection operation once.

1 This time consumption does not include the time needed to send commands through the interface.

Device Name	Operation Type		Time Consumption[1]	Description
	Error Repair		605 clock cycles	The time it takes to correct a single frame of data when a single-bit error is detected.
	Error Replace		605 clock cycles + "external memory readback time"	Time of reading back external memory depends on the external memory read back method, clock frequency, and other conditions. The correction times for single-bit errors, multi-bit errors, and CRC Only errors are the same.
PG2L100H /PG2L100HX	Initialization	Disable Full Scan	1,072,457 clock cycles	The time it takes for the IP to perform the initialization operation with risk regions masked.
		Enable Full Scan	1,260,969 clock cycles	The time it takes for the IP to perform the initialization operation with risk regions unmasked.
	Error detection	Disable Full Scan	1,072,457 clock cycles	The time it takes to check the entire CRAM once (with risk regions masked) when no errors are detected.
		Enable Full Scan	1,260,969 clock cycles	The time it takes to check the entire CRAM once (with risk regions unmasked) when no errors are detected.
	Error injection		980 clock cycles	The time it takes to perform an error injection operation once.
	Error Repair		605 clock cycles	The time it takes to correct a single frame of data when a single-bit error is detected.
	Error Replace		605 clock cycles + "external memory readback time"	Time of reading back external memory depends on the external memory read back method, clock frequency, and other conditions. The correction times for single-bit errors, multi-bit errors, and CRC Only errors are the same.
PG2L200H	Initialization		3,911,145 clock cycles	The time it takes for the IP to perform the initialization operation.
	Error detection		3,911,145 clock cycles	The time it takes to check the entire CRAM once when no errors are detected.
	Error injection		980 clock cycles	The time it takes to perform an error injection operation once.
	Error Repair		605 clock cycles	The time it takes to correct a single frame of data when a single-bit error is detected.
	Error Replace		605 clock cycles + "external memory readback time"	Time of reading back external memory depends on the external memory read back method, clock frequency, and other conditions. The correction times for single-bit errors, multi-bit errors, and CRC Only errors are the same.

Device Name	Operation Type		Time Consumption[1]	Description
PG2T390H	Initialization	Enable LVDS	4,260,649 clock cycles	The time it takes for the IP to perform initialization operation with the LVDS regions unmasked and the DDR regions masked
		Disable LVDS	4,226,249 clock cycles	The time it takes for the IP to perform initialization operation with LVDS and DDR regions masked.
	Error detection	Enable LVDS	4,260,649 clock cycles	The time it takes to check the entire CRAM once (with the LVDS regions unmasked and the DDR regions masked) when no errors are detected.
		Disable LVDS	4,226,249 clock cycles	The time it takes to check the entire CRAM once (with the LVDS and DDR region masked) when no errors are detected.
	Error injection		980 clock cycles	The time it takes to perform an error injection operation once.
	Error Repair		605 clock cycles	The time it takes to correct a single frame of data when a single-bit error is detected.
	Error Replace	Type 1	605 clock cycles + "external memory readback time"	Time of reading back external memory depends on the external memory read back method, clock frequency, and other conditions. The correction times for single-bit errors, multi-bit errors, and CRC Only errors with single-frame granularity are the same.
		Type 2	1,210 clock cycles + "external memory readback time for 2 frames of data"	Time of reading back external memory depends on the external memory read back method, clock frequency, and other conditions. The correction time for CRC Only errors with double-frame granularity.
PG2T390HX	Initialization	Enable LVDS	4,285,417 clock cycles	The time it takes for the IP to perform initialization operation with the LVDS regions unmasked and the DDR regions masked
		Disable LVDS	4,251,017 clock cycles	The time it takes for the IP to perform initialization operation with LVDS and DDR regions masked.
	Error detection	Enable LVDS	4,285,417 clock cycles	The time it takes to check the entire CRAM once (with the LVDS regions unmasked and the DDR regions masked) when no errors are detected.
		Disable LVDS	4,251,017 clock cycles	The time it takes to check the entire CRAM once (with the LVDS and DDR region masked) when no errors are detected.
	Error injection		980 clock cycles	The time it takes to perform an error injection operation once.
	Error Repair		605 clock cycles	The time it takes to correct a single frame of data when a single-bit error is detected.
	Error Replace	Type 1	605 clock cycles + "external memory readback time"	Time of reading back external memory depends on the external memory read back method, clock frequency, and other conditions. The correction times for single-bit errors, multi-bit errors, and CRC Only errors with single-frame granularity are the same.

Device Name	Operation Type		Time Consumption[1]	Description
		Type 2	1,210 clock cycles + "external memory readback time for 2 frames of data"	Time of reading back external memory depends on the external memory read back method, clock frequency, and other conditions. The correction time for CRC Only errors with double-frame granularity.
PG2K400	Initialization	Enable LVDS	3,957,241 clock cycles	The time it takes for the IP to perform the initialization operation with LVDS unmasked.
		Disable LVDS	3,602,233 clock cycles	The time it takes for the IP to perform the initialization operation with LVDS masked.
	Error detection	Enable LVDS	3,957,241 clock cycles	The time it takes to check the entire CRAM once (with LVDS unmasked) when no errors are detected.
		Disable LVDS	3,602,233 clock cycles	The time it takes to check the entire CRAM once (with LVDS masked) when no errors are detected.
	Error injection		980 clock cycles	The time it takes to perform an error injection operation once.
	Error Repair		605 clock cycles	The time it takes to correct a single frame of data when a single-bit error is detected.
	Error Replace	Type 1	605 clock cycles + "external memory readback time"	Time of reading back external memory depends on the external memory read back method, clock frequency, and other conditions. The correction times for single-bit errors, multi-bit errors, and CRC Only errors with single-frame granularity are the same.
		Type 2	1,210 clock cycles + "external memory readback time for 2 frames of data"	Time of reading back external memory depends on the external memory read back method, clock frequency, and other conditions. The correction time for CRC Only errors with double-frame granularity.
PG2T70H	Initialization		797,257 clock cycles	The time it takes for the IP to perform the initialization operation.
	Error detection		797,257 clock cycles	The time it takes to check the entire CRAM once when no errors are detected.
	Error injection		980 clock cycles	The time it takes to perform an error injection operation once.
	Error Repair		605 clock cycles	The time it takes to correct a single frame of data when a single-bit error is detected.
	Error Replace		605 clock cycles + "external memory readback time"	Time of reading back external memory depends on the external memory read back method, clock frequency, and other conditions. The correction times for single-bit errors, multi-bit errors, and CRC Only errors are the same.

Device Name	Operation Type	Time Consumption[1]	Description
PG2T160H	Initialization	1,975,113 clock cycles	The time it takes for the IP to perform the initialization operation.
	Error detection	1,975,113 clock cycles	The time it takes to check the entire CRAM once when no errors are detected.
	Error injection	980 clock cycles	The time it takes to perform an error injection operation once.
	Error Repair	605 clock cycles	The time it takes to correct a single frame of data when a single-bit error is detected.
	Error Replace	605 clock cycles + "external memory readback time"	Time of reading back external memory depends on the external memory read back method, clock frequency, and other conditions. The correction times for single-bit errors, multi-bit errors, and CRC Only errors are the same.

2.1.3.3 CRAM Frame Readback Check

For CRAM frames in device risk regions, the SEU IP will not perform readback checks, in order to reduce the impact on signals in risk regions. For detailed information, please refer to Table 2-5.

Table 2-5 CRAM Frame Readback Verification Details

Device	Proportion of frames without readback verification[2]	Corresponding Default Configuration of SEU IP
PG2L25H	0%	No frames are excluded.
PG2L50H	17.78%	Frames corresponding to risk regions will be excluded.
PG2L100H	14.96%	Frames corresponding to risk regions will be excluded.
PG2L100HX	14.96%	Frames corresponding to risk regions will be excluded.
PG2L200H	0%	No frames are excluded.
PG2T390H	4.18%	Frames corresponding to risk regions will be excluded.
PG2T390HX	3.62%	Frames corresponding to risk regions will be excluded.
PG2K400	11.30%	Frames corresponding to risk regions will be excluded.
PG2T70H	10.79%	Frames corresponding to risk regions will be excluded.
PG2T160H	4.78%	Frames corresponding to risk regions will be excluded.

2 The proportion of active bits in CRAM frames without readback verification, relative to the total chip configuration data, with all risk regions excluded by default.

2.2 IP Block Diagram

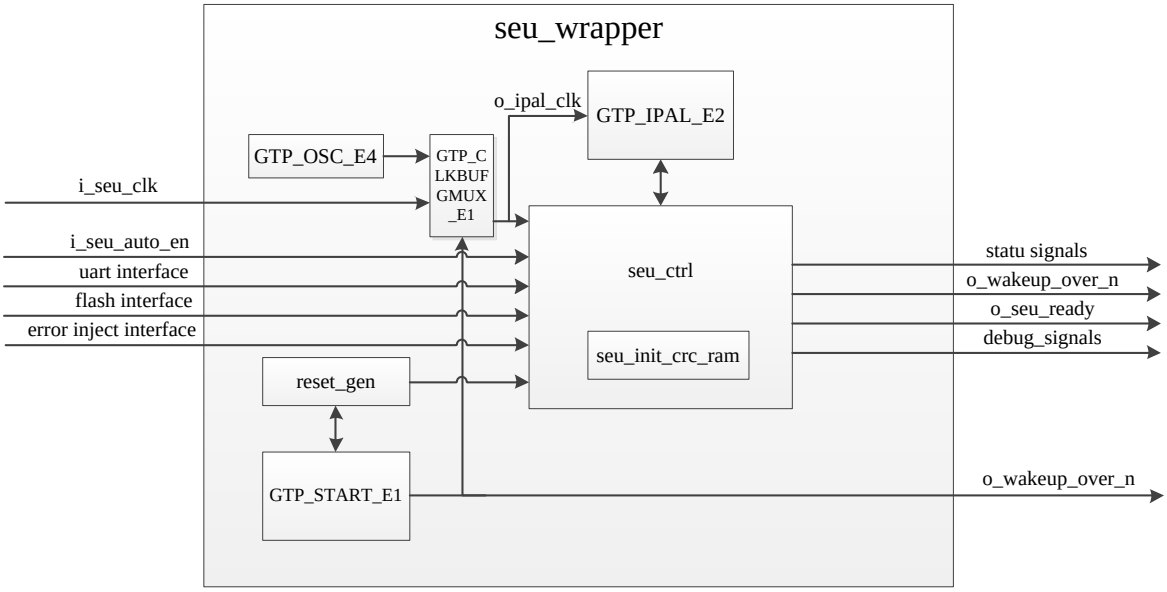

Figure 2-1 SEU IP System Block Diagram

The SEU IP system block diagram is shown in Figure 2-1, which primarily consists of the following modules:

- seu_ctrl: The SEU controller, which receives user control commands, performs error injection, SEU error detection and correction, state reporting, and generates corresponding state signals etc.
- seu_init_crc_ram: Stores the initial CRC values in RAM during the initialization process.
- GTP_IPAL_E2: Internal slave parallel interface for controlling FPGA CRAM.
- GTP_START_E1: Generates the FPGA wakeup indicator signal.
- reset_gen: The module to generate reset signal.
- GTP_OSC_E4: Generates osc_clk clock signal.
- GTP_CLKBUFGMUX_E1: Clock selection module.

2.3 IP Generation Process

2.3.1 Module Instantiation

The configuration of SEU IP can be customised by the IPC tool to instantiate the required IP modules. For detailed instructions on using the IPC tool, please refer to "***IP_Compiler_User_Guide***".

The main steps for instantiating the SEU IP module are described as follows.

2.3.1.1 Selecting IP

Open IPC and click File > Update in the main window to open the Update IP dialog box, where you add the corresponding version of the IP model.

After selecting the FPGAs device type, the Catalog interface displays the loaded IP models. Select the corresponding IP version under the "System/SEU" directory. The IP selection path interface is shown in Figure 2-2. Then set the Pathname and Instance Name on the right side of the page. The project instantiation interface is shown in Figure 2-3.

Attention:

PG2L25H, PG2L50H: The software version must be 2022.1 or above.

PG2L100H, PG2T390H: The software version must be 2021.1-SP6.5 or above.

PG2L200H: The software version must be 2022.2 or above.

PG2L100HX, PG2T390HX: The software version must be 2023.1 or above.

PG2K400: The software version must be 2023.2 or above.

PG2T70H: The software version must be 2023.2 or above.

PG2T160H: The software version must be 2024.1 or above.

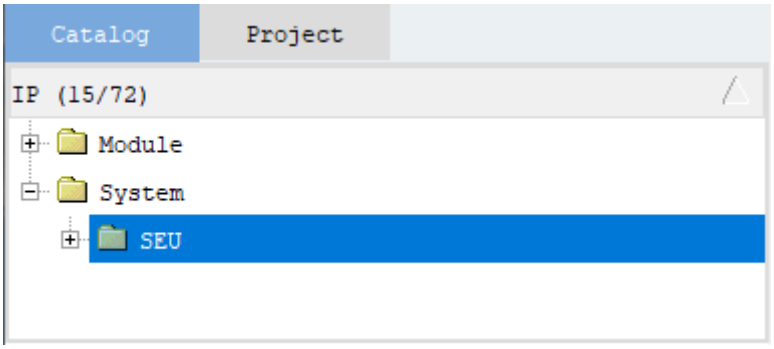

Figure 2-2 SEU IP Selection Path Interface

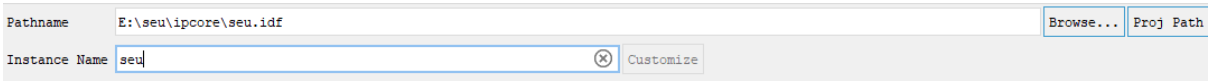

Figure 2-3 Project Instantiation Interface

2.3.1.2 Configure IP

After selecting the IP, click <Customize> to enter the SEU IP configuration interface. The left Symbol is the interface block diagram, as shown in Figure 2-4; the configuration window is shown on the right side, as shown in Figure 2-5.

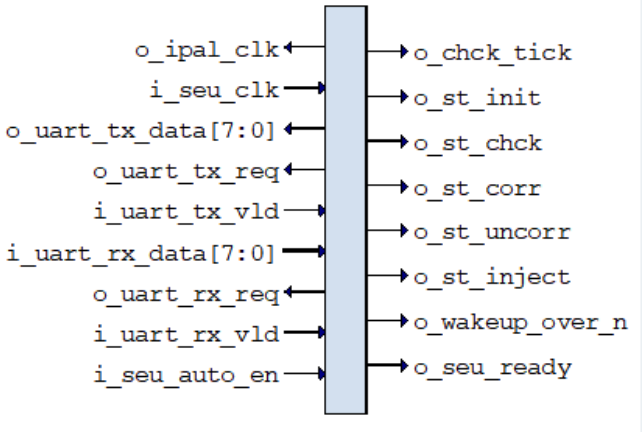

Figure 2-4 SEU IP Interface Block Diagram

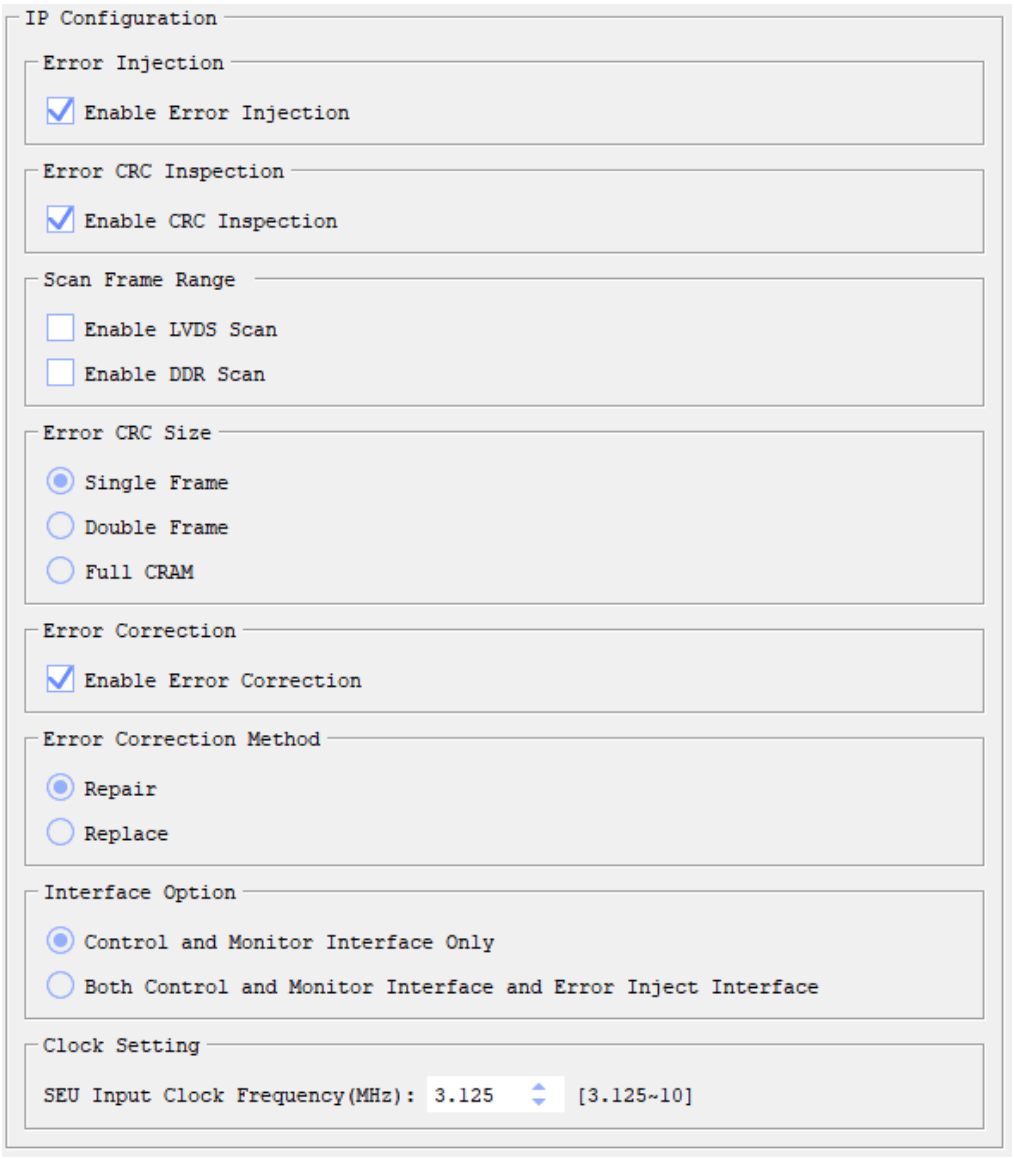

Figure 2-5 SEU IP Parameter Configuration Interface

For SEU IP configuration parameter description, please refer to Table 2-6.

Table 2-6 Configuration Parameter Description

Option Domain	Option Name/Parameter Name		Parameter Description	Default Value
Error Injection	Enable Error Injection		Enable the error injection function to inject errors into CRAM.	Enabled
Error CRC Inspection	Enable CRC Inspection[3]		Enable CRC verification.	Enabled
Scan Frame Range	Enable Full Scan		Enable scanning of the full-frame region[4].	Disabled
	Enable LVDS Scan		Enable scanning of the LVDS region[5].	Disabled
	Enable DDR Scan	Enable DDR BANKL1 Scan	Enable scanning of the DDR BANKL1 region[6].	Disabled
		Enable DDR BANKL2 Scan	Enable scanning of the DDR BANKL2 region[6].	Disabled
		Enable DDR BANKL3 Scan	Enable scanning of the DDR BANKL3 region[6].	Disabled
		Enable DDR BANKL4 Scan	Enable scanning of the DDR BANKL4 region[6].	Disabled
		Enable DDR BANKL5 Scan	Enable scanning of the DDR BANKL5 region[6].	Disabled
		Enable DDR BANKL6 Scan	Enable scanning of the DDR BANKL6 region[6].	Disabled
		Enable DDR BANKL7 Scan	Enable scanning of the DDR BANKL7 region[6].	Disabled
		Enable DDR BANKR5 Scan	Enable scanning of the DDR BANKR5 region[6].	Disabled
		Enable DDR BANKR6 Scan	Enable scanning of the DDR BANKR6 region[6].	Disabled
		Enable DDR BANKR7 Scan	Enable scanning of the DDR BANKR7 region[6].	Disabled
Error CRC Size[7]	Single Frame		Enable CRC with a detection granularity of 1, using a single frame as a CRC inspection unit.	Selected
	Double Frame		Enable CRC with a detection granularity of 2, using a double frame as a CRC inspection unit.	Cleared
	Full CRAM		Enable CRC with a full-CRAM detection granularity, using the full CRAM as a CRC inspection unit.	Cleared

3 Saves resources when the CRC verification function is disabled.

4 Only applicable to PG2L100H/PG2L100HX.

5 Only applicable to PG2T390H/PG2T390HX/PG2K400.

6 Only applicable to PG2T390H/PG2T390HX.

7 CRC error detection granularity configuration.

Option Domain	Option Name/Parameter Name	Parameter Description	Default Value
Error Correction	Enable Error Correction[8]	Enable error correction.	Enabled
Error Correction Method[9]	Repair	For Repair error correction mode, please refer to "2.8.6.1 Repair Mode" for details.	Selected
	Replace	For Replace error correction mode, please refer to "2.8.6.2 Replace Mode" for details.	Cleared
Interface Option[10]	Control and Monitor Interface Only	Instantiates only the "Control and Monitor Interface", please refer to "2.5.1.3 Control and Monitor Interface" for detailed interface description.	Selected
	Both Control and Monitor Interface and Error Inject Interface	Instantiates both "Control and Monitor Interface" and "Error Inject Interface". Please refer to "2.5.1.2 Error Inject Interface" and "2.5.1.3 Control and Monitor Interface" for detailed interface description.	Cleared
Clock Setting	SEU Input Clock Frequency(MHz)	SEU input clock frequency settings, effective clock frequency range: 3.125~10 MHz.	3.125

2.3.1.3 Generating IP

Upon completion of parameter configuration, click the <Generate> button in the top left corner to generate the SEU IP and the IP code according to user-specific settings. The information report interface for IP generation is shown in Figure 2-6.

Figure 2-6 SEU IP Generation Report Interface

8 When error correction is disabled, only error detection is performed without error correction.

9 Error correction mode configuration.

10 Top-level interface instantiation configuration.

Upon successful IP generation, the files indicated in Table 2-7 will be output to the Project path specified in Figure 2-3.

Table 2-7 Output Files after IP Generation

Output File[11]	**Description**
$instname.v	Top-level .v file of the generated IP.
$instname.idf	The Configuration file of the generated IP.
/rtl/*	The RTL code file of the generated IP.
/example_design/*	The Test Bench and the corresponding Memory Simulation Model files used by the Example Design of the generated IP.
/pnr/*	The project files .pds and pin constraint files .fdc for the Example Design of the generated IP.
/sim/*	The simulation directory for the generated IP. sim.tcl is a ModelSim simulation script, makefile is a VCS simulation script, and sim_file_list.f is a list of simulation files.
/sim_lib/	The directory for the simulation library files required by the IP.
/rev_1	The default output path for synthesis reports. (This folder is generated only after specifying the synthesis tool)
readme.txt	The readme file describes the structure of the generation directory after the IP is generated.
pg2l25h_cram_addr.txt	Description of the CRAM address structure for PG2L25H devices.
pg2l50h_cram_addr.txt	Description of the CRAM address structure for PG2L50H devices.
pg2l100h_cram_addr.txt	Description of the CRAM address structure for PG2L100H/PG2L100HX devices.
pg2l200h_cram_addr.txt	Description of the CRAM address structure for PG2L200H devices.
pg2t390h_cram_addr.txt	Description of the CRAM address structure for PG2T390H/PG2T390HX devices.
pg2k400_cram_addr.txt	Description of the CRAM address structure for PG2K400 devices.
pg2t70h_cram_addr.txt	Description of the CRAM address structure for PG2T70H devices.
pg2t160h_cram_addr.txt	Description of the CRAM address structure for PG2T160H devices.
pg2l50h_grid.seu	SEU mask region coordinate file for PG2L50H devices. (This file is only generated when PG2L50H devices are selected)
pg2l100h_grid.seu	SEU mask region coordinate file for PG2L100H devices. (This file is only generated when PG2L100H devices are selected)
pg2l100hx_grid.seu	SEU mask region coordinate file for PG2L100HX devices. (This file is only generated when the PG2L100HX devices are selected)
pg2t390h_grid.seu	SEU mask region coordinate file for PG2T390H devices. (This file is only generated when PG2T390H devices are selected)
pg2t390hx_grid.seu	SEU mask region coordinate file for PG2T390HX devices. (This file is only generated when PG2T390HX devices are selected)
pg2k400_grid.seu	SEU mask region coordinate file for PG2K400 devices. (This file is only generated when PG2K400 devices are selected)
pg2t70h_grid.seu	SEU mask region coordinate file for PG2T70H devices. (This file is only generated when PG2T70H devices are selected)
pg2t160h_grid.seu	SEU mask region coordinate file for PG2T160H devices. (This file is only generated when PG2T160H devices are selected)

11 <$instname> is the instantiation name entered by the user; "*" is a wildcard character used to replace files of the same type.

2.3.2 Constraint Configuration

For the specific configuration method of constraint files, please refer to the relevant help documents in the PDS installation path: "***User_Constraint_Editor_User_Guide***", "***Physical_Constraint_Editor_User_Guide***", "***Route_Constraint_Editor_User_Guide***".

2.3.3 Simulation Runs

The simulation of SEU IP is based on the Test Bench of the Example Design. For detailed information about Example Design, please refer to "2.4 Example Design".

For more details about the PDS simulation functions and third-party simulation tools, please consult the related help documents in the PDS installation path: "***Pango_Design_Suite_User Guide***", "***Simulation_User_Guide***".

ModelSim simulation steps: Open cmd.exe, switch the current directory to "/sim/modelsim" under the IP generation directory via command line, run ips2l_seu_top_sim.ba, and open ModelSim simulation software, as shown in Figure 2-7. Scripts can be run within the ModelSim simulation software for simulation.

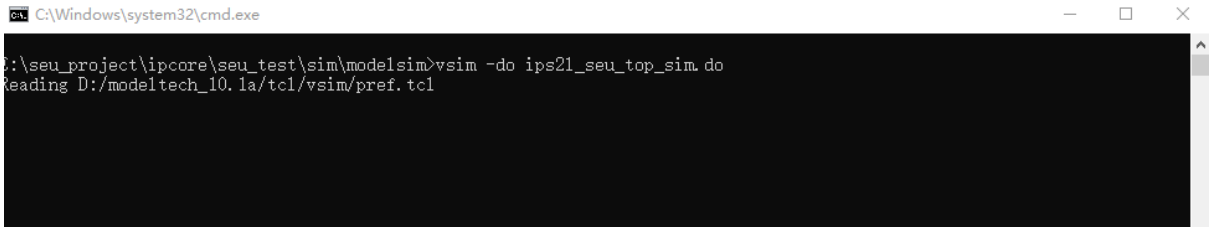

Figure 2-7 Open ModelSim Instruction

Descirption:

For related instructions on Replace function simulation, please refer to "2.8.11 External Memory Simulation File Description".

2.3.4 Synthesis and Placement/Routing

The specific usage of PDS synthesis tools and placement/routing tools can be found in the help documents within the PDS installation path.

Attention:

The "Example Design" project files .pds and the pin constraint files .fdc generated with the IP are located in the "/pnr/example_design" directory. When in use, the physical constraints need to be modified according to the actual device and PCB board trace; for details, please refer to "2.8 Descriptions and Considerations".

Table 2-8 Typical Resource Utilization Values for SEU IP Based on Applicable Device

Device Name	Configuration Mode			Typical Resource Utilization Values					
	Error Correction	CRC Verification	CRC Granularity	LUT	FF	Distributed RAM	DRM	IPAL	USCM
PG2L25H	Repair	On	Single	729	435	64	4	1	1
		On	Full	716	456	64	0	1	1
		Off	-	536	347	64	0	1	1
	Replace	On	Single	765	470	64	4	1	1
		On	Full	737	467	64	0	1	1
		Off	-	568	357	64	0	1	1
PG2L50H	Repair	On	Single	730	435	64	4	1	1
		On	Full	712	456	64	0	1	1
		Off	-	535	347	64	0	1	1
	Replace	On	Single	761	470	64	4	1	1
		On	Full	742	467	64	0	1	1
		Off	-	567	357	64	0	1	1
PG2L100H/ PG2L100HX	Repair	On	Single	765	455	64	8	1	1
		On	Full	748	475	64	0	1	1
		Off	-	575	366	64	0	1	1
	Replace	On	Single	884	481	64	8	1	1
		On	Full	870	487	64	0	1	1
		Off	-	687	368	64	0	1	1

Device Name	Configuration Mode			Typical Resource Utilization Values					
	Error Correction	CRC Verification	CRC Granularity	LUT	FF	Distributed RAM	DRM	IPAL	USCM
PG2L200H	Repair	On	Single	713	438	64	32	1	1
		On	Full	693	456	64	0	1	1
		Off	-	515	347	64	0	1	1
	Replace	On	Single	752	473	64	32	1	1
		On	Full	737	470	64	0	1	1
		Off	-	553	360	64	0	1	1
PG2T390H	Repair	On	Single	784	457	64	32	1	1
		On	Double	777	459	64	16	1	1
		On	Full	768	476	64	0	1	1
		Off	-	588	366	64	0	1	1
	Replace	On	Single	852	483	64	32	1	1
		On	Double	877	472	64	16	1	1
		On	Full	879	513	64	0	1	1
		Off	-	653	370	64	0	1	1
PG2T390HX	Repair	On	Single	755	459	64	32	1	1
		On	Double	758	461	64	16	1	1
		On	Full	752	477	64	0	1	1
		Off	-	568	366	64	0	1	1
	Replace	On	Single	773	485	64	32	1	1
		On	Double	827	474	64	16	1	1
		On	Full	795	499	64	0	1	1
		Off	-	564	355	64	0	1	1
PG2K400	Repair	On	Single	732	449	64	32	1	1
		On	Double	730	451	64	16	1	1
		On	Full	715	467	64	0	1	1
		Off	-	542	356	64	0	1	1
	Replace	On	Single	791	484	64	32	1	1
		On	Double	814	473	64	16	1	1
		On	Full	813	504	64	0	1	1
		Off	-	598	369	64	0	1	1
PG2T70H	Repair	On	Single	736	457	64	8	1	1
		On	Full	720	477	64	0	1	1
		Off	-	546	366	64	0	1	1
	Replace	On	Single	755	483	64	8	1	1
		On	Full	730	476	64	0	1	1
		Off	-	540	355	64	0	1	1

Device Name	Configuration Mode			Typical Resource Utilization Values					
	Error Correction	CRC Verification	CRC Granularity	LUT	FF	Distributed RAM	DRM	IPAL	USCM
PG2T160H	Repair	On	Single	733	458	64	16	1	1
		On	Double	730	460	64	8	1	1
		On	Full	719	477	64	0	1	1
		Off	-	540	366	64	0	1	1
	Replace	On	Single	757	484	64	16	1	1
		On	Double	763	473	64	8	1	1
		On	Full	761	499	64	0	1	1
		Off	-	545	355	64	0	1	1

Note: The "-" indicates that there is no description for the configuration item.

2.4 Example Design

This section mainly introduces the Example Design scheme based on SEU IP. In this scheme, user logic controls the SEU IP via USB-to-Serial Port conversion, where the serial port supports 115200bps by default. User logic writes instructions to the SEU via the Error Inject Interface or the Monitoring Interface and judges the correctness of the SEU logic by receiving the returned state report and the illumination of the indicator lights.

- seu_top_tb and lower levels can be used for simulation, where the GTP path in Example Design needs to be set according to the actual PDS installation path.
- seu_top and lower levels can be used for on-board debugging. The pin constraints in the Example Design are based on the P05I330RD04-A0 and PG2L100RD01-A0_SCH board designs. For other boards, pin configurations should be adjusted according to actual circumstances.

Attention:

Example Design generated by IP may not directly be usable for Flow on-board testing; pin constraints need to be based on the actual pin connections of the single board before Flow on-board testing can be performed.

2.4.1 Design Block Diagram

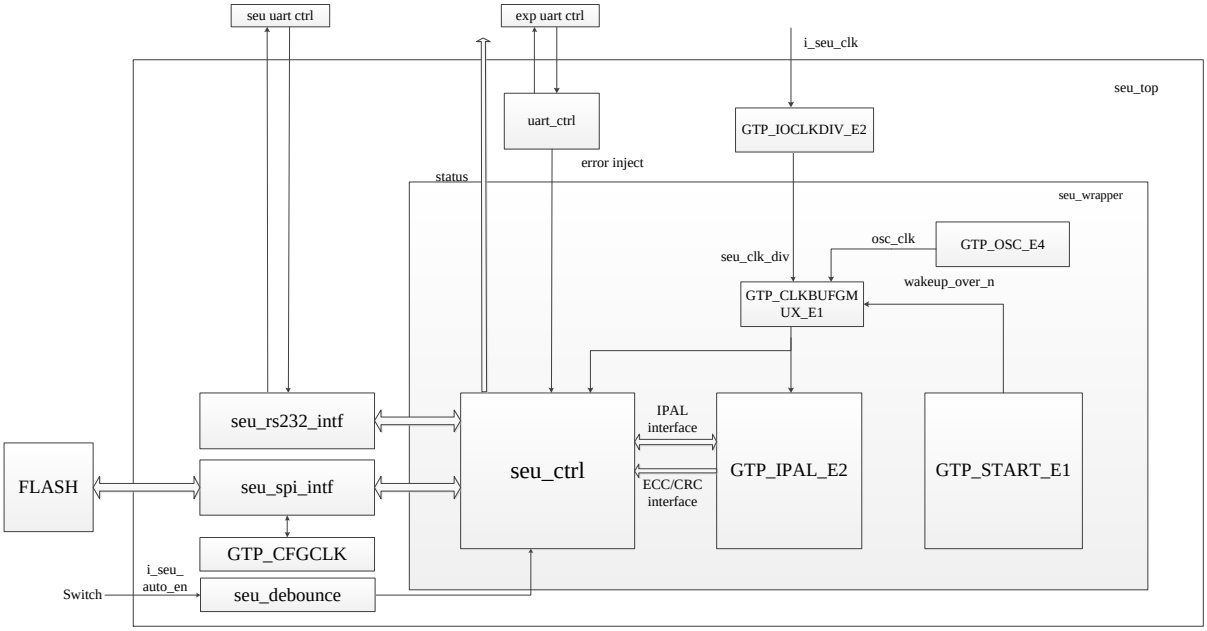

Figure 2-8 Example Design System Block Diagram

The system block diagram of Example Design is shown in Figure 2-8, where the User logic writes instructions to the SEU via the Error Inject Interface or the Monitoring Interface and judges the correctness of the SEU logic by receiving the returned state report and the illumination of the indicator lights. Additionally, in the seu_top_tb.v code used for simulation, the i_seu_auto_en input port is fixed to 1'b1, allowing the SEU to automatically enter the IDLE state and return to the error detection state based on the JTAG interface status.

2.4.2 Module Description

2.4.2.1 seu_uart_ctrl module

Module for motivating simulation, which generates input data and accepts output data for the SEU control and monitor interface.

2.4.2.2 exp_uart_ctrl module

Module for motivating simulation, which generates input data for the SEU error inject interface.

2.4.2.3 uart_ctrl module

Module for converting serial port data, which generates error inject interface control data.

2.4.2.4 seu_rs232_intf module

Module for converting between control and monitor interface and serial port, which implements data interaction between the Control and Monitor Interface and the seu_uart_ctrl module. For information on serial port configuration, please refer to "2.8.10 UART Interface Description".

2.4.2.5 seu_spi_intf module

Module for controling FLASH data read, which implements data exchange between the control and monitor interface and external FLASH via the SPI interface.

2.4.2.6 seu_debounce module

Module for processing debounce, which filters the jitter of the input signal i_seu_auto_en. In the simulation, by using the macro definition IPS_SEU_SPEEDUP_SIM, this module can be bypassed to speed up the simulation.

2.4.2.7 GTP_CFGCLK module

It controls external memory clock, generates spi_sck, and outputs it via SRB to the FLASH clock pin of the CCS device.

2.4.2.8 GTP_IOCLKDIV_E2 module

Clock division module, which divides the input clock.

Attention:

The seu_spi_intf module has only been tested on-board for the MICRON N25Q256 device. If using other FLASH devices, please modify this module as necessary.

2.4.3 Directory Description

Table 2-9 Example Design Directory Description List

Directories	Subdirectories and Files	Lower-Level Subdirectories and Files	Functional Description
--/example_design	-	-	Files included in Example Design.
-	-- /bench	-	Code files for top-level and testbench.
-	-	-- ips2l_seu_core_only_top.v	The top-level files for SEU IP Core Only, including the SEU IP module.
-	-	-- ips2l_seu_top.v	SEU IP Example Design top-level file, containing the SEU IP and other peripheral modules.
-	-	-- ips2l_seu_top_tb.v	SEU IP Example Design top-level simulation file, providing clock propagation and configuration for the SEU IP Example Design top-level file.
-	-- /rtl	-	Code files for the commonly used modules.
-	-	-- /led	LED module RTL folder, which provides the functionality to light up LED using a clock signal.
-	-	-- /uart_ctrl_32bit	Error Inject Interface to Serial Port conversion module.
-	-	-- /ips2l_seu_rs232_intf	Control and Monitor Interface to Serial Port conversion module.
-	-	-- ips2l_seu_spi_intf.v	FLASH data read control module. This module has only been on-board tested for MICRON N25Q256 device, if using other FLASH devices, please modify this module as necessary.

Directories	Subdirectories and Files	Lower-Level Subdirectories and Files	Functional Description
		-- ips2l_seu_debounce.v	Functional module for debouncing external input signals.
--/pnr	-	-	Synthesis placement and routing project.
	--/example_design	-	Synthesis placement and routing project files and constraint files for the Example Design.
-	-	-- ips2l_seu_top.pds	SEU IP Example Design PDS project files.
-	-	-- ips2l_seu_top.fdc	SEU IP Example Design PDS constraint files. The constraints generated by the IP are based on the P05I330RD04_A0 or PG2L100RD01_A0 boards, users need to modify them according to their actual applications.
-	-- /core_only	-	SEU IP synthesis placement and routing project files and constraint files.
-	-	-- ips2l_seu_core_only_top.pds	SEU IP PDS project files.
-	-	-- ips2l_seu_core_only_top.fdc	SEU IP PDS constraint files.
--/rtl	-	-	Design codes included in the SEU IP.
-	-- xxx_xxx.v	-	SEU IP code, usable for synthesis or simulation.
-	-- /common	-	Common modules, such as FIFO and RAM, called by SEU Core.
--/sim	-	-	Simulation directory.
-	-- /modelsim	-	.bat files for simulation run and filelist
-	-	/task	Task file directory for simulation.
-	-	/testcase	Testcase file directory for simulation.
-	-	cmem_data.txt	CRAM test data for simulation.
-	-	flash.txt	Flash test data for simulation. (to be prepared by the user)
-	-	--ips2l_seu_top_filelist.f	Filelist for simulation, called by seu_sim.do.
-	-	--ips2l_seu_top_sim.do	Backend program for simulation.
-	-	--ips2l_seu_top_sim_wave.do	Waveform load file for simulation.
-	-	--ips2l_seu_top_sim.bat	Batch file for simulation.
--/sim_lib	-	-	Simulation model directory.

Directories	Subdirectories and Files	Lower-Level Subdirectories and Files	Functional Description
-	-- /flash_model	-	Simulation model of external Flash. (to be prepared by the user and placed here)

Note: "-" indicates that there is no content for the item.

2.5 Descriptions of IP Interfaces

This section provides descriptions of interfaces related to SEU IP.

2.5.1 Top-Level Interface Description

2.5.1.1 Global Interface

Table 2-10 Global Interface

Port	I/O	Bit width	Valid Values	Description
i_seu_clk	I	1	-	Input clock interface provided by the user.
o_ipal_clk	O	1	-	Output clock interface provided by the SEU.
i_seu_auto_en	I	1	-	Automatic status switching enable signal. When the enable signal is active, the SEU automatically enters the IDLE state or returns to the error detection state based on the JTAG interface status: When the JTAG interface is detected to start transmitting instructions: the SEU automatically enters and remains in the IDLE state, rendering instructions input through the IP interface invalid; When the JTAG interface is detected to finish transmitting instructions, the SEU automatically returns to the detection state. 1: Enabled; 0: Disabled.

Note: "-" indicates that the parameter does not exist.

Attention:

For the use of i_seu_auto_en signal:

First, interference signals must be avoided on the JTAG port. If interference signals persist, this will not only affect the SEU but also pose risks to other chip functionalities;

Ensure the JTAG enters the TLR state after performing daisy chain operations on other chips;

If it is impossible to avoid interference signals on the JTAG port, the user can dynamically switch the value of i_seu_auto_en to prevent the SEU from automatically entering the IDLE state.

2.5.1.2 Error Inject Interface

Table 2-11 Error Inject Interface

Port	I/O	Bit width	Valid Values	Description
i_err_inject_req	I	1	High	IPS2L_SEU IP error inject interface, which controls IP operation by sending commands. Active-high pulse, the pulse width is one i_seu_clk clock cycle, one pulse represents one command.
i_err_inject_addr	I	34	-	IPS2L_SEU IP error injection address. bit[33]: Command identification. 1: Enter control command, used in conjunction with bit[32:28], bit[27:0] is irrelevant at this time; 0: Enter error injection command, where bit [32:0] represents the error injection address. bit[32:28]: Command encoding or region addr. When bit [33]=1, bit [32:28] represents the command encoding; When bit [33]=0, bit [32:28] represents the region addr. Command encodings are as follows: 5'h00: Enter the error detection mode; 5'h01: Enter the idle state. 5'h02: Soft reset. bit[27:20]: column addr. bit[19:12]: frame addr. bit[11:0]: error bit in frame addr.

Note: "-" indicates that the parameter does not exist.

Attention:

The error injection address must be a valid address; otherwise, it may cause the device to malfunction.

2.5.1.3 Control and Monitor Interface

Table 2-12 Control and Monitor Interface

Port	I/O	Bit width	Valid Values	Description
o_uart_txdata	O	8	-	UART sends data.
o_uart_txreq	O	1	High	UART sends request 1: Request to send 0: Do not request to send
i_uart_txvld	I	1	High	Allow to send data flag. 1: UART interface FIFO is not full, sending request is allowed; 0: UART interface FIFO is full, sending request is not allowed.
i_uart_rxdata	I	8	-	UART receives data.
o_uart_rxreq	O	1	High	UART receives request. 1: Request to receive; 0: Do not request to receive.
i_uart_rxvld	I	1	High	Allow to receive data flag. 1: Receiving request is allowed 0: Receiving request is not allowed

Note: "-" indicates that the parameter does not exist.

2.5.1.4 External Memory Interface

Table 2-13 External Memory Interface

Port	I/O	Bit width	Valid Values	Description
o_spi_txdata	O	32	-	SPI sends data.
o_spi_txreq	O	1	High	SPI sends request. 1: Request to send 0: Do not request to send
i_spi_txvld	I	1	High	Allow to send SPI data flag. 1: Sending request is allowed 0: Sending request is not allowed
i_spi_rxdata	I	32	-	SPI receives data.
o_spi_rxreq	O	1	High	SPI receives request. 1: Request to receive; 0: Do not request to receive.
i_spi_rxvld	I	1	High	Allow receiving SPI data flag. 1: SPI interface FIFO is not empty, reception request is allowed; 0: SPI interface FIFO is empty, reception request is not allowed.

Note: "-" indicates that the parameter does not exist.

2.5.1.5 Status Interface

Table 2-14 State Interface

Port	I/O	Bit width	Valid Values	Description
o_wakeup_over_n	O	1	High	Wakeup complete flag. 0: Wakeup completed; 1: Wakeup not completed.
o_seu_ready	O	1	High	SEU IP is ready and can start operation upon receiving external commands. 0: Not ready; 1: Ready.
o_chck_tick	O	1	High	Heartbeat indicator signal. It is effective only during SEU error detection, generating a high-level pulse for one clock cycle every 100 i_seu_clk clock cycles.
o_st_init	O	1	High	Initialization process indicator signal. 0: SEU IP is not in initialization state; 1: SEU IP is initializing.
o_st_chck	O	1	High	SEU error detection process indicator signal. 0: SEU IP is not in error detection state; 1: SEU IP is performing error detection.
o_st_corr	O	1	High	Error correction process indicator signal. 0: SEU IP is not in error correction state; 1: SEU IP is performing error correction.
o_st_inject	O	1	High	Error injection process indicator signal. 0: SEU IP is not in error injection state; 1: SEU IP is performing an error injection operation.
o_st_uncorr	O	1	High	Error correction state indicator signal. 0: Errors are correctable; 1: Errors are uncorrectable. At the end of the error detection process, the signal state changes according to the actual situation.
o_seu_err_enable_repair	O	1	High	When a correctable error is detected, a pulse lasting one clock cycle in the o_ipal_clk clock domain will be generated. Only valid in Repair mode. 1: Indicates that correctable errors are detected.
o_seu_err_unable_repair	O	1	High	When an uncorrectable error is detected, a pulse lasting one clock cycle in the o_ipal_clk clock domain will be generated. Only valid in Repair mode. 1: Indicates that uncorrectable errors are detected.

Note: "-" indicates that the parameter does not exist.

2.5.1.6 Debug Interface

Table 2-15 Debug Interface

Port	I/O	Bit width	Valid Values	Description
o_seu_valid	O	1	High	SEU information valid flag, pulse signal. 0: o_seu_serr, o_seu_derr, and o_seu_index are invalid; 1: o_seu_serr, o_seu_derr, and o_seu_index are valid.
o_seu_index	O	12	-	Position of single-bit error within the frame.
o_seu_serr	O	1	High	Single-bit error flag. 0: No single-bit error; 1: Single-bit error present.
o_seu_derr	O	1	High	Double-bit error flag. 0: No double-bit error; 1: Double-bit error present.
o_seu_crc_err	O	1	High	CRC error flag. 0: No CRC error; 1: CRC error present.
o_seu_corr_cnt	O	8	-	Correctable error count statistics, which is cleared to zero after a soft reset and remain unchanged when full.
o_seu_uncorr_cnt	O	8	-	Uncorrectable error count statistics, which is cleared to zero after a soft reset and remain unchanged when full.
o_seu_frame_addr	O	8	-	Frame address of the current frame.
o_seu_column_addr	O	8	-	Column address of the current frame.
o_seu_region_addr	O	5	-	Region address of the current frame.
o_fsm_debug	O	32	-	bit[31:29]: seu_cs, current SEU state. 3'd0: E_SEU_WAKEUP 3'd1: E_SEU_IDLE 3'd2: E_SEU_START 3'd3: E_SEU_RB_FM 3'd4: E_SEU_RD_EXT 3'd5: E_SEU_CORRECT 3'd6: E_SEU_DYN_RECFG 3'd7: E_SEU_END bit[28:26]: seu_ns, next SEU state. bit[25:21]: ipal_st, the count of instructions sent by the ipal interface. bit[20:9]: cmd_cnt, the clock cycle count used by the ipal interface for sending each instruction. bit[8]: fifo_rd_en, FIFO read enable. 0: Do not read; 1: Read FIFO. bit[7]: fifo_empty, FIFO empty flag. 0: FIFO is not empty; 1: FIFO is empty, cannot be read. bit[6]: fifo_wr_en, FIFO write enable. 0: Do not write; 1: Write FIFO. bit[5]: fifo_full, FIFO full flag. 0: FIFO is not full; 1: FIFO is full, cannot be written. bit[4]: crc_ram_wr_en, CRC RAM write enable.

Port	I/O	Bit width	Valid Values	Description
				0: Do not write CRC RAM; 1: Write CRC RAM. bit[3]: seu_serr_lck, single-bit error hold. 0: No single-bit error; 1: Single-bit error present. bit[2]: seu_derr_lck, multi-bit error hold. 0: No multi-bit error; 1: Multi-bit error present. bit[1]: seu_crc_err_lck, CRC error hold. 0: No CRC error; 1: CRC error present. bit[0]: drcfg_err_lck, dynamic reconfiguration error flag. 0: Dynamic reconfiguration successful; 1: Dynamic reconfiguration error.

Note: "-" indicates that the parameter does not exist.

2.5.2 Top-Level Interface Description

2.5.2.1 Error Inject Interface

2.5.2.1.1 Descriptions of Timings

The Error Inject Interface can control SEU IP operation by sending commands, the typical timing is shown in Figure 2-9.

- i_err_inject_addr is valid when i_err_inject_req is high;
- i_err_inject_req holds for one i_ipal_clk clock cycle.

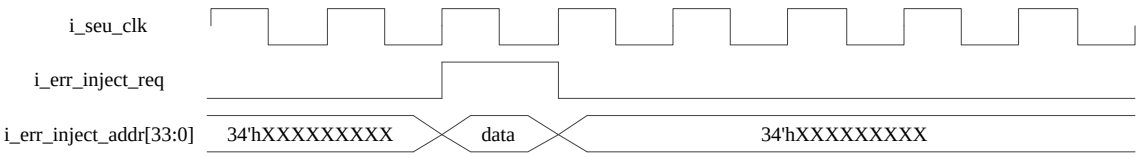

Figure 2-9 Typical Timing for the Error Inject Interface

Attention:

If the i_err_inject_req signal remains high for multiple clock cycles, it may cause command collisions.

2.5.2.1.2 Command Description

For the description of the commands supported by the error inject interface, please refer to Table 2-16.

Table 2-16 Descriptions of Commands Related to The Error Inject Interface

Command Type	**Applicable Scenarios**[12]	**Command Interpreting**	**Command Format Description**[13]				
			bit[33]	**bit[32:28]**	**bit[27:20]**	**bit[19:12]**	**bit[11:0]**
Command to enter error detection state	IDLE State	Exit IDLE state to enter error detection state, perform error detection and correction.	1'b1	5'b00000	8'bxxxxxxxx	8'bxxxxxxxx	12'bxxxxxxxxxxxx
Soft Reset Command	IDLE State	Perform a reset on the state machine part of the SEU IP and re-initiate IP initialization. After execution of the "Soft reset command", the system automatically enters the error detection state.	1'b1	5'b00010	8'bxxxxxxxx	8'bxxxxxxxx	12'bxxxxxxxxxxxx

12 This command is only applicable in the corresponding state scenario; sending it in other states is ineffective.

13 region address: CRAM region address; column address: CRAM column address; frame address: CRAM frame address; bit address: bit position address within CRAM frame. For examples of error injection instruction addresses, please refer to "2.8.8 Example of Error Injection Command Address". For description of the CRAM address range, please refer to "2.8.9 CRAM Address Range Description".

Command Type	Applicable Scenarios[12]	Command Interpreting	Command Format Description[13]				
			bit[33]	bit[32:28]	bit[27:20]	bit[19:12]	bit[11:0]
Error injection Command	IDLE State	Inject a single-bit error into CRAM; to inject multi-bit errors, repeat this command. After execution of the "Error injection command", the system automatically returns to the IDLE state.	1'b0	region address	column address	frame address	bit address
Command to enter IDLE state	Error detection or error correction state	Enter IDLE state after the current frame error detection or correction is completed.	1'b1	5'b00001	8'bxxxxxxxx	8'bxxxxxxxx	12'bxxxxxxxxxxxx

Note: "x" indicates that the value of the bit is irrelevant.

2.5.2.2 Control and Monitor Interface

2.5.2.2.1 Descriptions of Timings

The Control and Monitor Interface can control SEU IP by sending commands, the typical timing is shown in Figure 2-10.

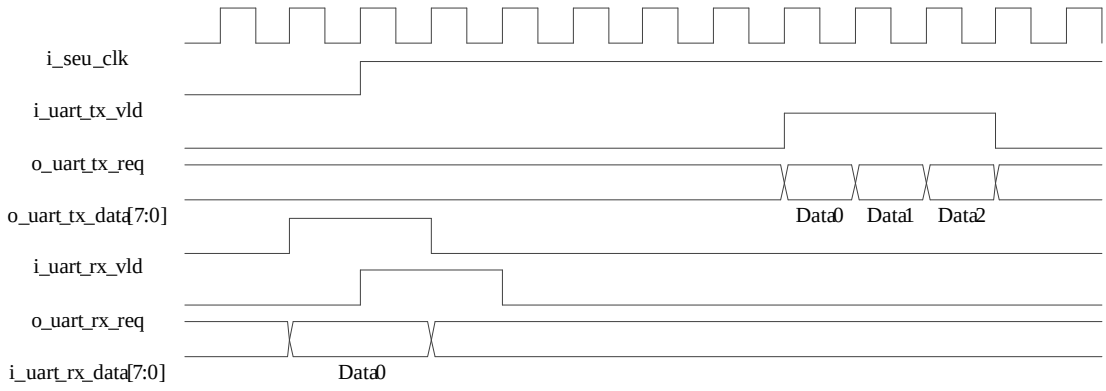

Figure 2-10 Timing of Control and Monitor Interface

- i_uart_tx_vld high level indicates allowing to transmit data;
- o_uart_tx_req high level indicates data is being transmitted;

- When o_uart_tx_req is at high level, o_uart_tx_data transmits one byte of valid data per clock cycle.
- i_uart_rx_vld high level indicates data is available to read in the receiving direction; low level indicates no data to read;
- o_uart_rx_req high level indicates data is being read;
- When both i_uart_rx_vld and o_uart_rx_req are high, one byte of data is read from i_uart_rx_data every clock cycle.

2.5.2.2.2 Command Description

For descriptions of supported commands by the Control and Monitor Interface, please refer to Table 2-17.

Descirption:

All the following command contents are in ASCII format unless otherwise specified.

Table 2-17 Descriptions of Commands Related to Control and Monitor Interface

Command Type	Applicable Scenarios[14]	Command Interpreting	Command Format
Command to enter error detection state	IDLE state	Exit IDLE state to enter error detection state, perform error detection and correction.	"D"
Soft reset command	IDLE state	Perform a reset on the state machine part of the SEU IP, and reinitialize the IP. After execution of the "Soft reset command", the system automatically enters the error detection state.	"R"
Error injection command	IDLE state	Inject a single-bit error into CRAM; to inject multi-bit errors, repeat this command. After execution of the "Error injection command", the system automatically returns to the IDLE state.	"E" + "Error injection address"[15]

14 This command is only applicable in the corresponding state scenario; sending it in other states is ineffective.

15 Error injection address consists of 10 hexadecimal digits (40bit binary data), not in ASCII format; for format, please refer to Table 2-18.

Command Type	Applicable Scenarios[14]	Command Interpreting	Command Format
Command to enter IDLE state	Error detection or correction state	Enter IDLE state after the current frame error detection and correction is completed.	"I"
State report commands	Any state	Trigger the SEU IP to report its current state via the Control and Monitor Interface.	"S"

Table 2-18 Error Injection Address Format[16]

bit[39: 33]	bit[32:28]	bit[27:20]	bit[19:12]	bit[11:0]
7'b0	region address	column address	frame address	bit address

2.5.2.2.3 Output Reports

Descirption:

All the following reports are in ASCII format.

The Control and Monitor Interface can monitor the working state of SEU IP by receiving reported output reports. The SEU IP supports three types of output reports: initialization state report, error detection report, and state report. As specifically described below.

- Initialization State Report

After initialization, the SEU IP will generate an initialization status report. For the report description, please refer to Table 2-19.

16 region address: CRAM region address; column address: CRAM column address; frame address: CRAM frame address; bit address: bit position address within CRAM frame. For description of the CRAM address range, please refer to "2.8.9 CRAM Address Range Description".

Table 2-19 Initialization State Report Description

Content of Report[17]	Generation Scenario	Content Interpreting
"LOGOS2_SEU_"+"Vx_x"+"CR"+"LF"	After the SEU IP starts initialization.	SEU IP version number.

Note: "Vx_x" corresponds to the current SEU IP version.

➢ Error Detection Report

If the SEU IP detects a CRAM error during initialization or error detection it generates an error detection report; for report description, please refer to Table 2-20. For error address field description, please refer to Table 2-21.

Table 2-20 Error Detection Report Description

Content of Report[18]	Repair Mode	Verification Mode		Content Interpreting
"SER" + "Space" + "AD" + "Error Address" + "CR" + "LF"	Off	ECC	Single-bit ECC	A single-bit error is detected at the bit corresponding to the current error address.
"DER" + "Space" + "AD" + "Error Address" + "CR" + "LF"			Multi-bit ECC	Multi-bit error is detected[19].
"CRC" + "Space" + "AD" + "Error Address" + "CR" + "LF"		CRC	Single frame	Detected CRC Only error in the current error address frame[19].
			Double frame	Detected CRC Only errors in both the current error address frame and the previous frame[19].
			Full CRAM	CRC error detected in the bitstream[20].

17 CR represents "Carriage Return", LF represents "Line Feed".

18 SER represents single-bit error, DER represents multiple-bit errors, CRC represents CRC Only error, REP represents correctable error, UNR represents uncorrectable error, CR represents "Carriage Return", LF represents "Line Feed". The error address consists of 9 hexadecimal digits (36bit binary data), which have been converted into ASCII format before report upload, with each hexadecimal digit converted into one ASCII character, totalling 9 ASCII characters.

19 The bit address field in the error address field makes on sense.

20 The error address indicated in the error detection report makes no sense.

Content of Report[18]	Repair Mode	Verification Mode		Content Interpreting
"REP" + "Space" + "AD" + "Error Address" + "CR" + "LF"	On	ECC	Single-bit ECC	A single-bit correctable error is detected in the Bit corresponding to the current incorrect address.
"UNR" + "Space" + "AD" + "Error Address" + "CR" + "LF"			Multi-bit ECC	An uncorrectable error is detected in the current error address frame[19].
		CRC	Single frame	An uncorrectable error is detected in the current error address frame[19].
			Double frame	Uncorrectable errors are detected in both the current error address frame and the previous frame[19].
			Full CRAM	An uncorrectable error is detected in the bitstream[20].

Table 2-21 Error Address Field Description[21]

bit[36:33]	bit[32:28]	bit[27:20]	bit[19:12]	bit[11:0]
4'b0	region address	column address	frame address	bit address

- State Report

SEU IP generates a state report in the following scenarios; for report description, please refer to Table 2-22; for state code description, please refer to Table 2-23.

21 region address: CRAM region address; column address: CRAM column address; frame address: CRAM frame address; bit address: bit position address within CRAM frame. For description of the CRAM address range, please refer to "2.8.9 CRAM Address Range Description".

Table 2-22 State Report Description

Content of Report[22]	Type of State Report	Generation Scenario	Content Interpreting
"ST" + "Space" + "State Code" + "CR" + "LF"	Current State Report	Received "State report command".	Reflect current state.
	Error detection State Report	Automatically jumps to error detection state after initialization.	Indicates that the system has entered the error detection state.
		Jumps to error detection state upon receiving the "Command to enter error detection state".	Indicates that the system has entered the error detection state.
	IDLE State Report	Jumps to IDLE state upon receiving the "Command to enter IDLE state".	Indicates that the system has entered the IDLE state.
		Automatically jumps to IDLE state upon completion of error injection execution.	Indicates that the system has entered the IDLE state.
	Error injection State Report	Jumps to error injection state upon receiving the "Error injection command".	Indicates that the system has entered the error injection state.

Table 2-23 State Description Corresponding to the Status Code

State Code[22]	State Description
00	Wakeup state
01	Initialization state
02	Error detection state
03	Error correction state
04	IDLE state
05	Error injection state

2.5.2.3 External Memory Interface

External memory interface is used for accessing external registers during CRAM dynamic reconfiguration. In the Example Design, the attached FLASH is accessed through the SPI interface; for details, please refer to "2.4 Example Design".

22 The state code is a 2-digit hexadecimal number (8-bit binary data).

2.5.2.3.1 Process Description

When the SEU IP error correction mode is set to "Replace", if an error is detected, it is necessary to read the CRAM data of the erroneous frame from the external memory and perform a partial dynamic reconfiguration of the CRAM. The brief process description is as follows:

When performing SEU detection, it begins counting data frames from CRAM. If a frame is found to be erroneous and requires correction, it sends the current frame count. The FLASH data reading control module calculates the starting address for reading the FLASH based on the current frame count, then reads a frame of data into the FIFO. Once a frame of data is read, the SEU controller reads out the frame data from the FIFO and performs CRAM dynamic reconfiguration. When the CRC granularity is set to 2 and a CRC error is detected, the SEU will repeat the above operations twice, reading the current and previous frame data from the flash each time, to replace the current and previous frame data in the CRAM.

2.5.2.3.2 Descriptions of Timings

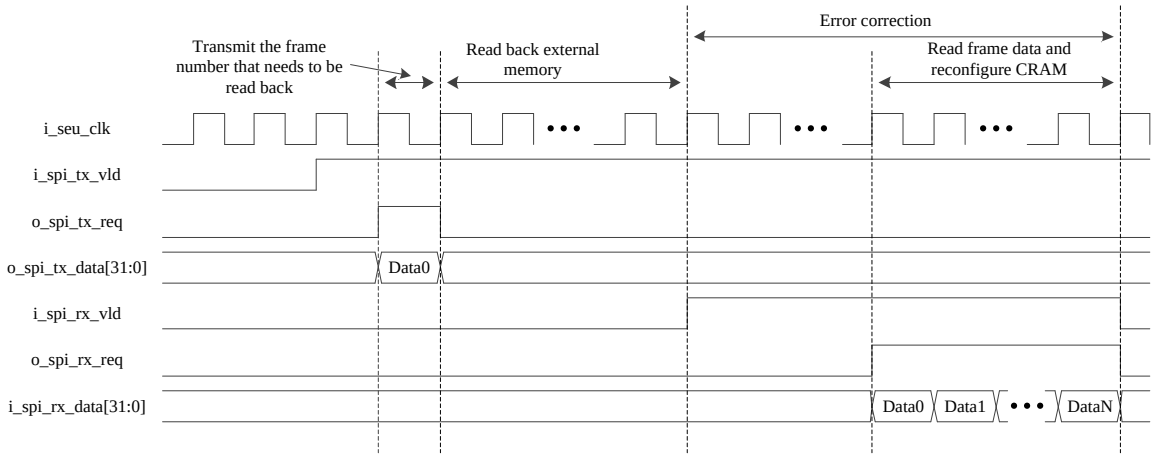

Figure 2-11 External Memory Interface Timing Diagram

- Data is allowed to be sent when i_spi_tx_vld is high;
- o_spi_tx_req being high indicates that data is being sent, with only one clock cycle of data sent at a time;
- o_spi_tx_data is for sending data, where o_spi_tx_data [11:0] is the count value for the current frame and o_spi_tx_data [15:12] is fixed at 0;
- i_spi_rx_vld indicates that the readback of the external memory is complete;

- o_spi_rx_req represents the reading of data from FIFO;
- During the high level of o_spi_rx_req, 16bit data is read every clock cycle until a frame of data is completely read.

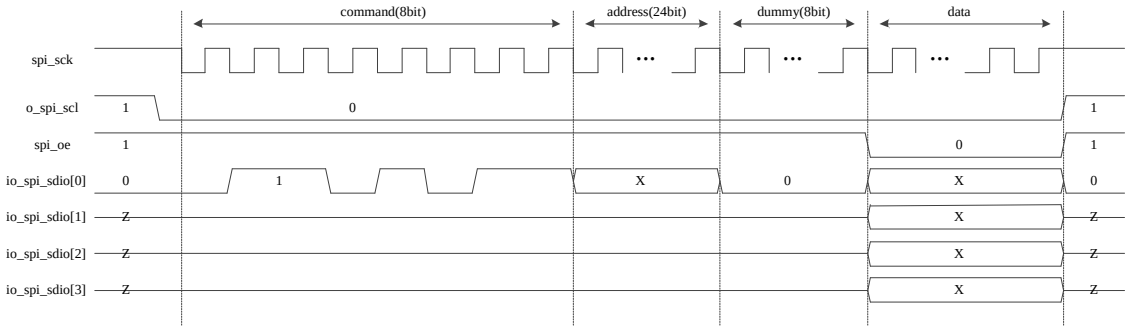

Figure 2-12 SPI Interface Timing Diagram

2.6 Description of the IP Register

None.

2.7 Typical Applications

For typical applications of the SEU IP, please refer to "2.4 Example Design".

2.8 Descriptions and Considerations

2.8.1 Configure Parameters

Parameters within the SEU IP are not open to users and should not be arbitrarily modified.

2.8.2 Bitstream Generation

Before generating the bitstream file, ensure that the "Project Setting > Generate Bitstream > Readback > Enable Mask Variable Memory In Read Back" option is selected, which is usually selected by default in the PDS version.

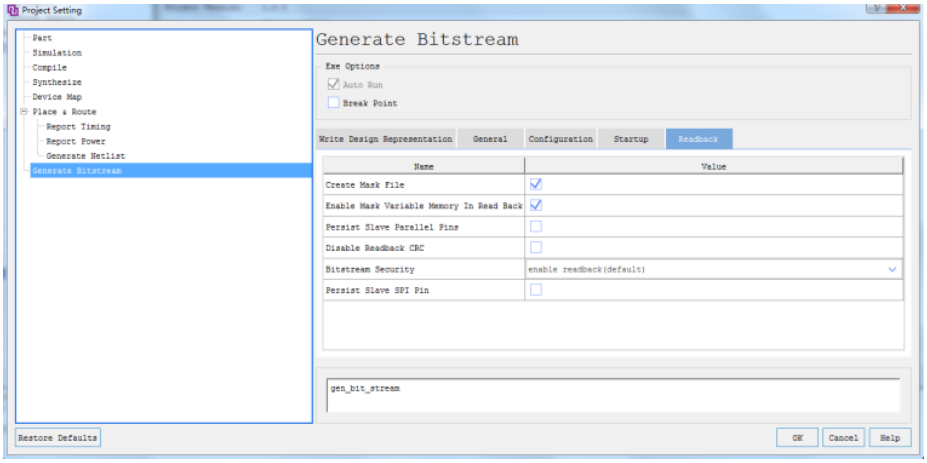

Figure 2-13 Bitstream Generation Settings Interface

2.8.3 IO Constraints

The IP provides an .fdc file compatible with Example Design, suitable only for specific packages and boards of PG2L100H and PG2T390H devices. For other chip packages and boards, it needs to be written according to specific circumstances.

2.8.4 Placement and Routing Constraints

The .fdc that comes with Example Design includes constraints on the placement and routing positions, which can limit the placement and routing of SEU IP to specific regions.

2.8.5 Working State

The working state of SEU IP and the conditions for transitioning between states are shown in Figure 2-14. For relevant interface command information, please refer to "2.5.2 Top-Level Interface Description".

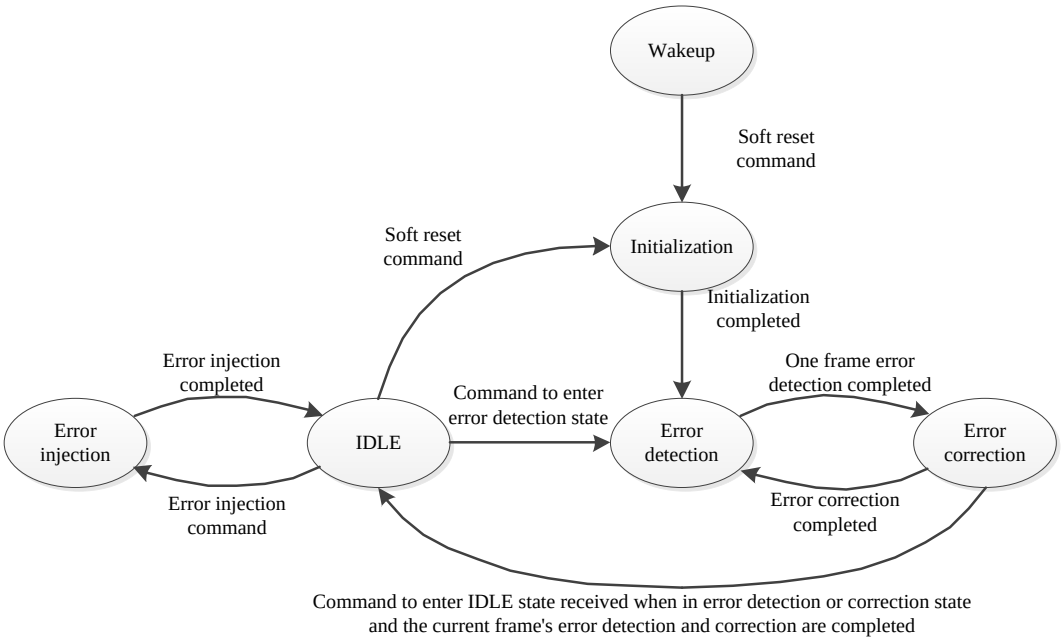

Figure 2-14 SEU IP Working State Transition Diagram

2.8.5.1 Wake-up State

After power-up, the SEU IP is in the wake-up state.

- In the wake-up state, the SEU IP needs to wait for the o_seu_ready signal to be pulled high before it can start working.
- After the o_seu_ready is pulled high, the SEU IP receives the "Soft reset command" to enter the initialization state.

2.8.5.2 Initialization State

After receiving the "Soft reset command", the SEU IP enters the initialization state.

- In the initialization state, the o_st_init signal is pulled high.
- In the initialization state, the SEU IP reads all frames of the CRAM once[23]. If CRC is enabled, the SEU IP will calculate and store the CRC value according to the check granularity as the initial CRC value, which will be used for CRC comparison during error detection processes. For CRC calculation description, please refer to Table 2-24.
- After initialization is complete, SEU IP automatically enters the error detection state and starts working properly.

Table 2-24 CRC Value Calculation Description

CRC Granularity	**CRC Value Calculation Unit**	**Storage Location of the Calculation Results**
1	Single frame	ips2l_seu_init_crc_ram
2	Double frame	
Full CRAM	Full bitstream	Register

Attention:

SEU detection is also performed during the initialization process. If single-bit or multi-bit errors are detected during the initialization process through the state interface signals or control and monitor interface, users need to identify and rectify the cause of the errors and then re-execute the initialization operation.

If cyclic redundancy check (CRC) is enabled, the CRC value will be calculated and stored normally during initialization even if single-bit or multi-bit errors are detected, but this initial CRC value will be incorrect. Under these circumstances, after completion of the initialization and entering the error detection state, the SEU IP will continuously detect CRC errors even after the correction of single-bit or multi-bit errors.

23 To reduce the impact on risk region signals when the SEU IP is turned on, readback check is not performed on the CRAM frames within the region during the initialization process. For detailed information, please refer to "2.1.3.3 CRAM Frame Readback Check".

2.8.5.3 Error detection state

After completing the initialization, or upon receiving the "Command to enter error detection state" in the IDLE state, the SEU IP will enter the error detection state.

- In the error detection state, the o_st_chck signal is pulled high.
- The SEU IP performs frame-by-frame error detection on CRAM data in the error detection state, and enters the error correction state upon completion of each frame, regardless of whether an error is detected or not.
- The SEU IP can receive a "Command to enter IDLE state" during the error detection state. If this command is received, the SEU IP enters the IDLE state after completing error detection and correction for the current frame.

Note:

During the error detection process, if CRC is enabled, the SEU IP calculates a CRC value for every frame, every two frames, or the entire CRAM depending on the CRC granularity settings. The result is compared with the initial CRC value, and if inconsistent, a CRC error is detected.

When there are errors of 3 bits or more, the ECC error detection results are inaccurate, which may result in three scenarios: no ECC error reported, single-bit ECC error reported, or double-bit ECC error reported. Since the ECC error detection priority in the IP's internal error detection algorithm is higher than that of the CRC error detection:

In Repair mode, when there are errors of 3 bits or more, if the ECC algorithm incorrectly reports a double-bit error, the IP will stop the error detection process and enter the IDLE state. Because a double-bit error is uncorrectable, a CRC error will not be reported. If ECC incorrectly reports a single-bit error, the IP will correct the reported bit error and then start a new round of error detection; if ECC does not detect any error, CRC error indication will be reported normally.

In Replace mode, when there are errors of 3 bits or more, if the ECC algorithm incorrectly reports a 1-bit or 2-bit error, the IP will reconfigure the reported error frame and start a new round of error detection; if the ECC algorithm does not detect any error, the IP will report CRC error normally.

2.8.5.4 error correction state

When the SEU IP performs error detection for each frame of CRAM data in the error detection state, it enters the error correction state.

- In the error correction state, the o_st_corr signal is pulled high.
- The operations performed by the SEU IP in the error correction state depend on the error detection results and error correction function configuration, please refer to Table 2-25.
- The SEU IP can receive a "Command to enter IDLE state" in the error correction state. If this command is received, the SEU IP enters the IDLE state after correcting the current frame.

Table 2-25 SEU IP Error Correction Operation Description

Error Correction Function[24]	**Error Detection Results**	**SEU IP Operation Description**
Disabled	-	Do not perform error correction, jump directly to the error detection state.
Enabled	Correctable errors are detected	Enter the error detection state after completing error correction.
	Uncorrectable errors are detected	Jump to IDLE state and pull high the o_st_uncorr signal.
	No errors are detected	Directly jump to the error detection state.

Note: "-" indicates that this content is irrelevant.

Descirption:

After entering the normal working state, if the SEU IP has not detected any uncorrectable errors, has not received a "Command to enter IDLE state", and encounters no other anomalies, it will continuously switch between the error detection and error correction states, cyclically detecting and correcting errors in CRAM data frames.

24 For the corresponding "Enable Error Correction" parameters, please refer to "2.3.1.2 Configure IP".

2.8.5.5 IDLE state

The SEU IP enters IDLE state upon receiving a "Command to enter IDLE state" during error detection or error correction, or after completing error injection in the error injection state.

- In IDLE state, the state indicators o_st_init, o_st_chck, o_st_corr, and o_st_inject are all low.
- In IDLE state, the SEU IP can perform relevant operations by receiving commands, please refer to Table 2-26.

Table 2-26 Commands and Operations in IDLE State

Receivable Commands	**SEU IP Operation Description**
Error injection command	Inject a single-bit error into CRAM; to inject multi-bit errors, repeat this command. After execution of the "Error injection command", the system automatically returns to the IDLE state.
Soft reset command	Perform a reset on the state machine part of the SEU IP and re-initiate IP initialization. After execution of the "Soft reset command", the system automatically enters the error detection state.
Command to enter error detection state	Exit IDLE state to enter the error detection state.

2.8.5.6 Error injection state

The SEU IP enters the error injection state upon receiving an "Error injection command" in the IDLE state.

- In the error injection state, the o_st_inject signal is pulled high.
- The operations performed by the SEU IP in the error injection state depend on the error injection function configuration, please refer to Table 2-27.
- After error injection is complete, return to the IDLE state.

Table 2-27 Description of Operations in Error Injection State

Error Injection Function[25]	**SEU IP Operation Description**
Enabled	The SEU IP introduces a single-bit error at a designated location in the CRAM. Error injection method: First read back the data frame where the error needs to be injected, invert the bit to be subjected to error injection, and then dynamically reconfigure the CRAM.
Disabled	Only read back the specified data frame without performing dynamic reconfiguration.

25 For the corresponding "Enable Error Injection" parameters, please refer to "2.3.1.2 Configure IP" for details.

Attention:

The SEU IP can only receive the "Error injection command" in IDLE state; the command is invalid in other states.

2.8.6 Error Correction

The SEU IP supports error correction, with two configurable correction modes according to the error correction capability[26]: Repair mode and Replace mode. For error correction methods under different correction modes, see Table 2-28.

2.8.6.1 Repair Mode

Repair mode only supports the correction of single-bit errors. If multiple-bit errors or CRC Only errors[27] are detected, it is considered an uncorrectable error, and the SEU IP exits the error detection and correction state and enters the IDLE state.

26 For the corresponding "Error Correction Method" parameters, please refer to "2.3.1.2 Configure IP".

27 This indicates that only CRC errors have been detected, without detecting any single-bit or multiple-bit errors.

2.8.6.2 Replace Mode

Replace mode can correct single-bit errors, multiple-bit errors, and CRC Only errors (not full CRAM).

Table 2-28 SEU IP Error Correction Method Description

Error Correction	**Verification Mode**		**Error Correction Method**
Repair	ECC	Single-bit ECC	Invert the erroneous Bit of the current frame, then dynamically reconfigure the CRAM.
		Multi-bit ECC	Uncorrectable error, the SEU IP exits the error detection and correction states and enters the IDLE state.
	CRC	Single frame	
		Double frame	
		Full CRAM	
Replace	ECC	Single-bit ECC	Read the erroneous frame data from the external memory, then dynamically reconfigure the CRAM.
		Multi-bit ECC	
	CRC	Single frame	Retrieve a frame of erroneous data from the external memory, then dynamically reconfigure the CRAM.
		Double frame	Retrieve two frames of erroneous data from the external memory, then dynamically reconfigure the CRAM.
		Full CRAM	The SEU IP enters the IDLE state, waiting for the user to manually reconfigure the CRAM.

Descirption:

Replace mode requires an external memory.

2.8.7 Operation Flow

2.8.7.1 Error Detection and Correction Flow

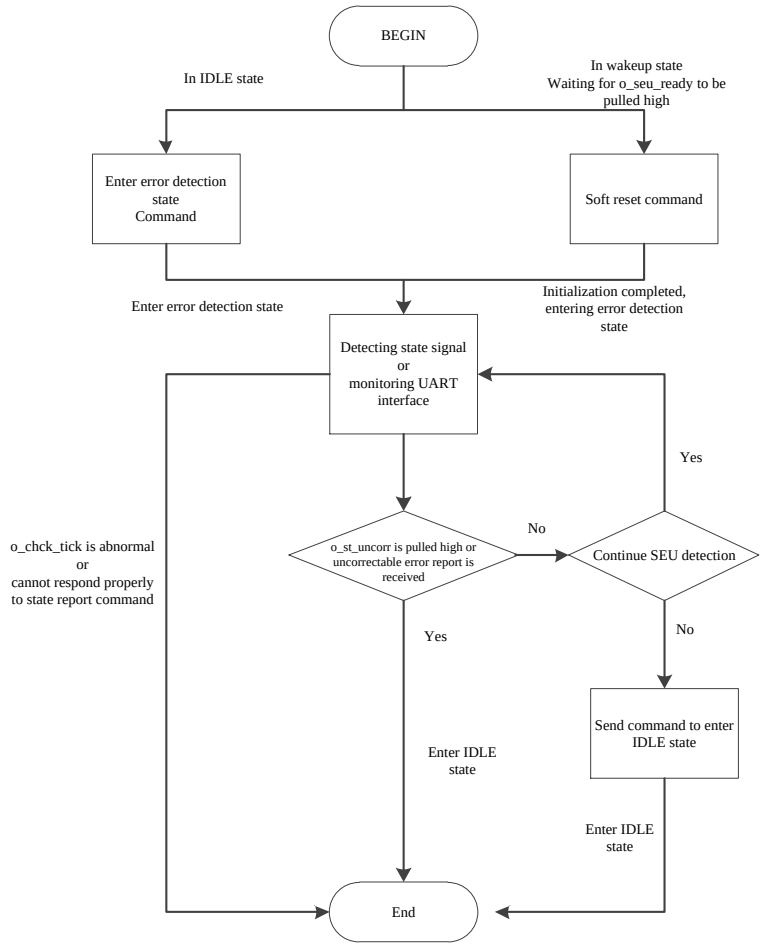

Figure 2-15 SEU Error Detection and Correction Flowchart

2.8.7.1.1 Start Error Detection and Correction

There are two ways to start the error detection and correction process, depending on the working state of the SEU IP:

- In the wake-up state, it is necessary to wait for o_seu_ready to be pulled high, then send a "Soft reset command", after which the SEU IP will automatically enter the error detection and correction process upon completion of initialization.
- In IDLE state, send the "Command to enter error detection state" directly, and the SEU IP will move into the error detection and correction process.

2.8.7.1.2 Uncorrectable errors are detected

If the SEU IP detects an uncorrectable error[28], it will automatically stop the error detection and correction and enter the IDLE state.

2.8.7.1.3 Stop Error Detection and Correction

Sending the "Command to enter IDLE state" can abort the SEU error checking process, and the SEU IP enters the IDLE state after completing the error detection and correction of the current frame.

2.8.7.1.4 Resolve SEU IP Fault

If the o_chck_tick state signal is abnormal, or the expected state report is not received after sending a "State report command," then it may indicate a fault in the SEU IP itself, preventing it from operating properly. Users need to take corrective operations to resolve the fault. For information on IP debugging, please refer to "2.9 IP Debugging Method".

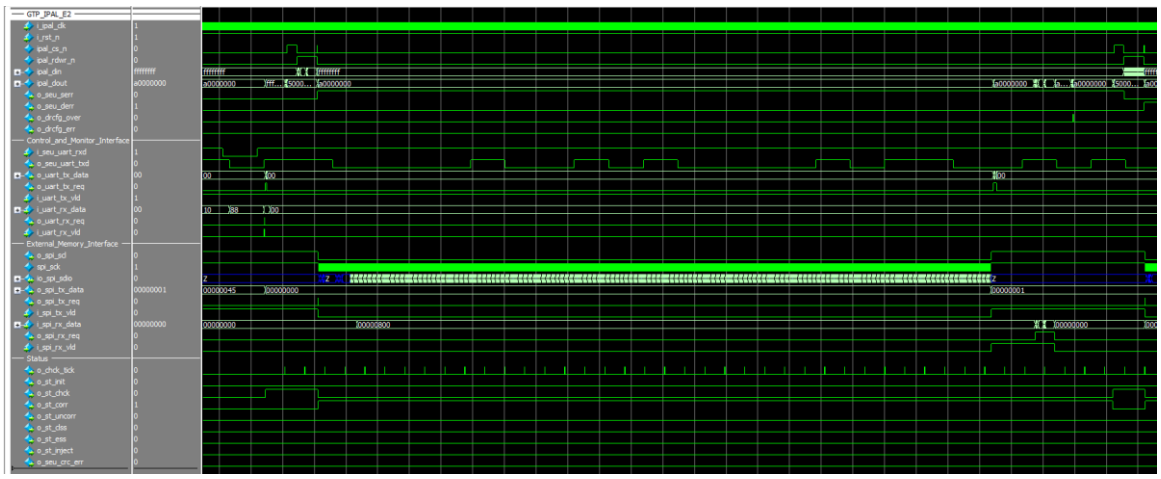

Figure 2-16 SEU Error Detection and Correction Waveform Diagram

28 An uncorrectable error refers to an error that cannot be corrected in the current correction mode, for example, if the current error correction function is enabled and it is in Repair mode, then multiple-bit errors are uncorrectable, and SEU will send an UNR error report. For specific information, please refer to "2.8.12 Explanation of Correctable and Uncorrectable Errors".

2.8.7.2 Error Injection Flow

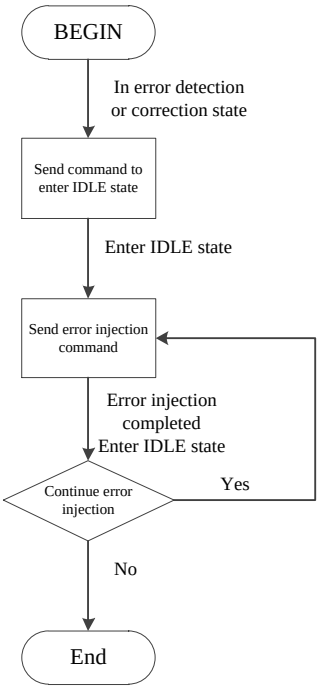

Figure 2-17 SEU Error Injection Process Flowchart

The error injection function is mainly used for debugging, and allows a single-bit error to be injected into any Bit of any frame in the CRAM. If multi-bit errors need to be injected, the error injection operation should be repeated multiple times.

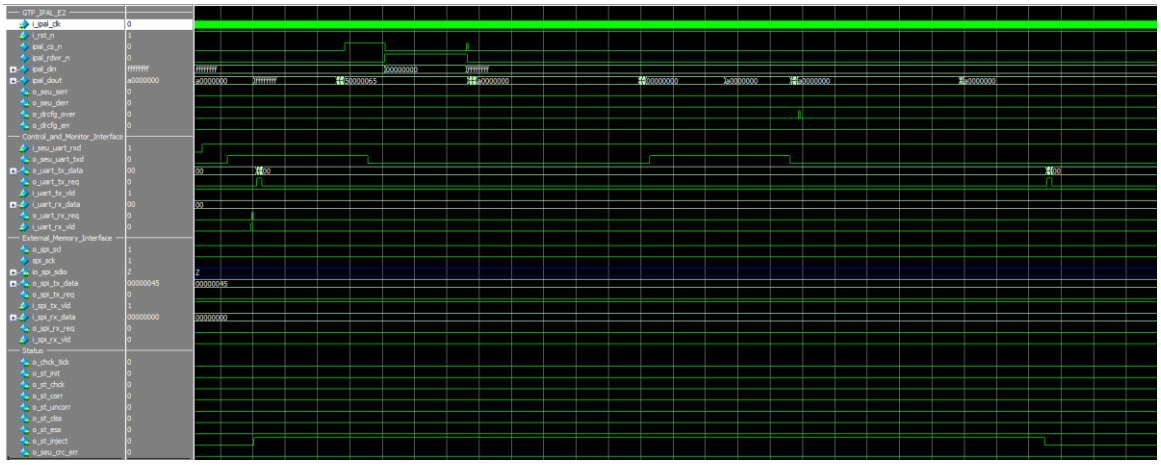

Figure 2-18 SEU Error Injection Waveform Diagram

Attention:

Error injection may cause the project to stop working properly.

2.8.8 Example of Error Injection Command Address

For example, there are 7 Regions in PG2T390H, each Region contains several Columns (the number of Columns may differ between different Regions), and each Column contains several Frames (the number of Frames may differ between different Columns), with each Frame containing 3,232 bits of data.

If we were to inject an error into bit 273 of frame 17, column 16, region 2, the error injection instruction address would be as follows:

region address = 5'b00010;

column address = 8'b00010000;

frame address = 8'b00010001;

bit address = 12'b000100010001.

2.8.9 CRAM Address Range Description

- When generating the SEU IP, there are txt files in the IP generation folder that describe the corresponding CRAM address space of the device. For file names and related content, please refer to Table 2-29. Do not inject errors into addresses beyond the specified range.
- Injecting errors into wrong addresses will change the bit value of the CRAM, which, if related to user logic functions, can affect both the IP itself and the user's logic functions.
- If only verifying IP functionality, non-functional bits can be used. Non-functional bits are described in two txt files and do not affect user logic, facilitating users to debug their control logic.

Table 2-29 CRAM Address Space Description File Description

File Name	Content Description
pg2l25h_cram_addr.txt	Provides the complete CRAM address space for PG2L25H.
pg2l50h_cram_addr.txt	Provides the complete CRAM address space for PG2L50H.
pg2l100h_cram_addr.txt	Provides the complete CRAM address space for PG2L100H/PG2L100HX.

File Name	Content Description
pg2l200h_cram_addr.txt	Provides the complete CRAM address space for PG2L200H.
pg2t390h_cram_addr.txt	Provides the complete CRAM address space for PG2T390H/PG2T390HX.
pg2k400_cram_addr.txt	Provides the complete CRAM address space for PG2K400.
pg2t70h_cram_addr.txt	Provides the complete CRAM address space for PG2T70H.
pg2t160h_cram_addr.txt	Provides the complete CRAM address space for PG2T160H.

2.8.10 UART Interface Description

In the Example Design, the Control and Monitor Interface is connected to the host computer via a 2-wire UART interface. Users can modify the design according to actual needs to meet their requirements.

2.8.10.1 UART Interface Configuration

The UART interface in the Example Design complies with the RS232 standard, with the supported configuration as follows:

- Baud Rate: 115200bps;
- Start bit: 1bit;
- Data bit: 8bit;
- Stop bit: 1bit;
- Checksum bit: Not supported;
- Flow control: Not supported.

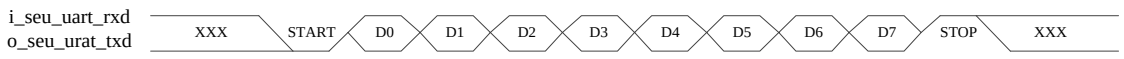

Figure 2-19 Typical Timing of UART Interface

2.8.10.2 Change Baud Rate

Customers can change the baud rate as needed, by modifying the CLK_DIV_P parameter in the ips2l_seu_rs232_intf.v module. The method for calculating the value of CLK_DIV_P is as follows:

$$\text{CLK\_DIV\_P} = \text{round}[\frac{\text{i\_seu\_clk frequency}}{6 \times \text{baud rate}}]$$

Here, round denotes rounding, which means the calculation will be rounded off to the nearest integer.

For example, if the i_seu_clk frequency is 50M and the baud rate is 115,200bps, then the calculation for CLK_DIV_P is as follows:

$$\text{CLK\_DIV\_P} = \text{round}\left[\frac{50000000}{6 \times 115200}\right] = 72$$

Descirption:

If customers need to change UART interface configurations other than the baud rate, they may do so by modifying the ips2l_seu_rs232_intf.v module.

2.8.11 External Memory Simulation File Description

When using the Replace function for simulation, the user needs to prepare the Flash model and place it in the following path: "\sim_lib\flash_model".

Attention:

This IP does not provide third-party Flash simulation models; users need to adapt the interface timing for simulation.

2.8.12 Explanation of Correctable and Uncorrectable Errors

The classification of correctable and uncorrectable errors is effective only when the error correction function is enabled and the error correction mode is set to Repair. The classification is based on the current error state indicator.

The working process of SEU IP in error detection mode is described as follows:

- After SEU IP starts working in error detection mode, it will scan CRAM frame by frame until it exits to IDLE state;
- If an error is detected, the scanning will pause and the corresponding error correction operation will be performed;
- After the error correction operation is complete, the scanning of CRAM will continue frame by frame.

The starting position for continuing the frame-by-frame scanning of CRAM after error correction depends on the settings of the error correction mode and the verification mode. For detailed information, please refer to Table 2-29. For more information about error correction operations, please refer to "2.8.5.4 error correction state", "2.8.6 Error Correction".

Table 2-30 Description of Starting Positions for Continuing Frame-by-Frame Scanning of CRAM

Error Correction	**Verification Mode**		**Starting Position for Continuing Frame-by-Frame Scanning of CRAM After Error Correction**
Repair	ECC	Single-bit ECC	The next frame from the current error frame.
		Multi-bit ECC	In this error correction mode and verification mode, if the detected error is uncorrectable, the frame-by-frame scanning will not continue, the SEU IP will exit the error detection and correction state and enter the IDLE state.
	CRC	Single frame	
		Double frame	
		Full CRAM	
Replace	ECC	Single-bit ECC	The next frame from the current error frame.
		Multi-bit ECC	
	CRC	Single frame	The next verification unit from the current verification unit.
		Double frame	
		Full CRAM	In this error correction and verification mode, frame-by-frame scanning will not continue. The SEU IP enters the IDLE state, waiting for the user to manually reconfigure the CRAM.

2.8.13 Usage Instructions for SEU IP Masked Frame

For different devices, the scanning of masked regions is controlled by parameters in the UI or IP code. For specific cases, please refer to Table 2-31.

Table 2-31 Usage Instructions for Masked Frame Scanning

Device Name	Masked Frame Scanning Control Variables	Control Range	Methods for Scanning Masked Frames
PG2L50H	The "FULL_SCAN_50H" parameter in the $instname.v file in the IP generation directory	All masked regions	Change the parameter value to "TRUE"
PG2L100H /PG2L100HX	"Enable Full Scan" parameter in the UI	All masked regions	Check this option
PG2T390H /PG2T390HX	"Enable LVDS Scan" parameter in the UI	LVDS-related mask regions	Check this option
	"Enable DDR Scan" parameter in the UI interface and 10 sub-option parameters	DDR-related mask regions	Check the corresponding region option
	"FULL_SCAN_390H"/"FULL_SCAN_390HX" parameters in the $instname.v file in the IP generation directory	All masked regions	Change the parameter value to "TRUE"
PG2T70H	"FULL_SCAN_70H" parameter in the $instname.v file in the IP generation directory	All masked regions	Change the parameter value to "TRUE"
PG2K400	"Enable LVDS Scan" parameter in the UI	LVDS-related mask regions	Check this option
	"FULL_SCAN_400" parameter in the $instname.v file in the IP generation directory	All masked regions	Change the parameter value to "TRUE"
PG2T160H	"FULL_SCAN_160H" parameter in the $instname.v file in the IP generation directory	All masked regions	Change the parameter value to "TRUE"

2.9 IP Debugging Method

2.9.1 Key Indicator Signal

For some key information during SEU operation, single-bit indicator signal is created for easy observation, which can be connected to external LEDs or monitored in other ways to quickly determine the operating state of the SEU. For descriptions of key indicator signal, please refer to Table 2-32.

Table 2-32 Key Indicator Signal

Port	I/O	Bit width	Valid Values	Description
o_chck_tick	O	1	High	Heartbeat indicator signal. It is effective only during SEU error detection, generating a high-level pulse for one clock cycle every 100 i_seu_clk clock cycles.
o_st_init	O	1	High	Initialization process indicator signal. 0: SEU IP is not in initialization state; 1: SEU IP is initializing.
o_st_chck	O	1	High	SEU error detection process indicator signal. 0: SEU IP is not in error detection state; 1: SEU IP is performing error detection.

Port	I/O	Bit width	Valid Values	Description
o_st_corr	O	1	High	Error correction process indicator signal. 0: SEU IP is not in error correction state; 1: SEU IP is performing error correction.
o_st_inject	O	1	High	Error injection process indicator signal. 0: SEU IP is not in error injection state; 1: SEU IP is performing an error injection operation.
o_st_uncorr	O	1	High	Error correction state indicator signal. 0: Errors are correctable; 1: Errors are uncorrectable. At the end of the error detection process, the signal state changes according to the actual situation.

2.9.2 Debug Signal

For other internal states needed for debugging, the relevant Debug signal can be captured through the Debug Core to monitor the working state of the SEU. For Debug interface signal, please refer to Table 2-15.

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