PK03026_PGC10KD_MBG484

(V1.0)

(28.02.2020)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.0	28.02.2020	Initial release

About this Manual

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Chapter 1 Introduction to Packaging

The PGC10KD_MBG484 divice is packaged with a Wire Bond BGA. Its package size is 19mmx19mm, with 484 solder balls, a pitch of 0.8mm and a maximum package thickness of 1.56mm.

Chapter 2 Package Dimension and Pins

2.1 Package Outline Dimension

Table 2-1 Dimensional Data

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	1.26	1.41	1.56	c	0.32	0.36	0.40
A1	0.30	0.35	0.40	e	-	0.8	-
A2	1.01	1.06	1.11	b	0.40	0.45	0.50
D	18.9	19.0	19.1	aaa	-	-	0.15
E	18.9	19.0	19.1	bbb	-	-	0.20
D1	-	16.8	-	ddd	-	-	0.20
E1	-	16.8	-	eee	-	-	0.15

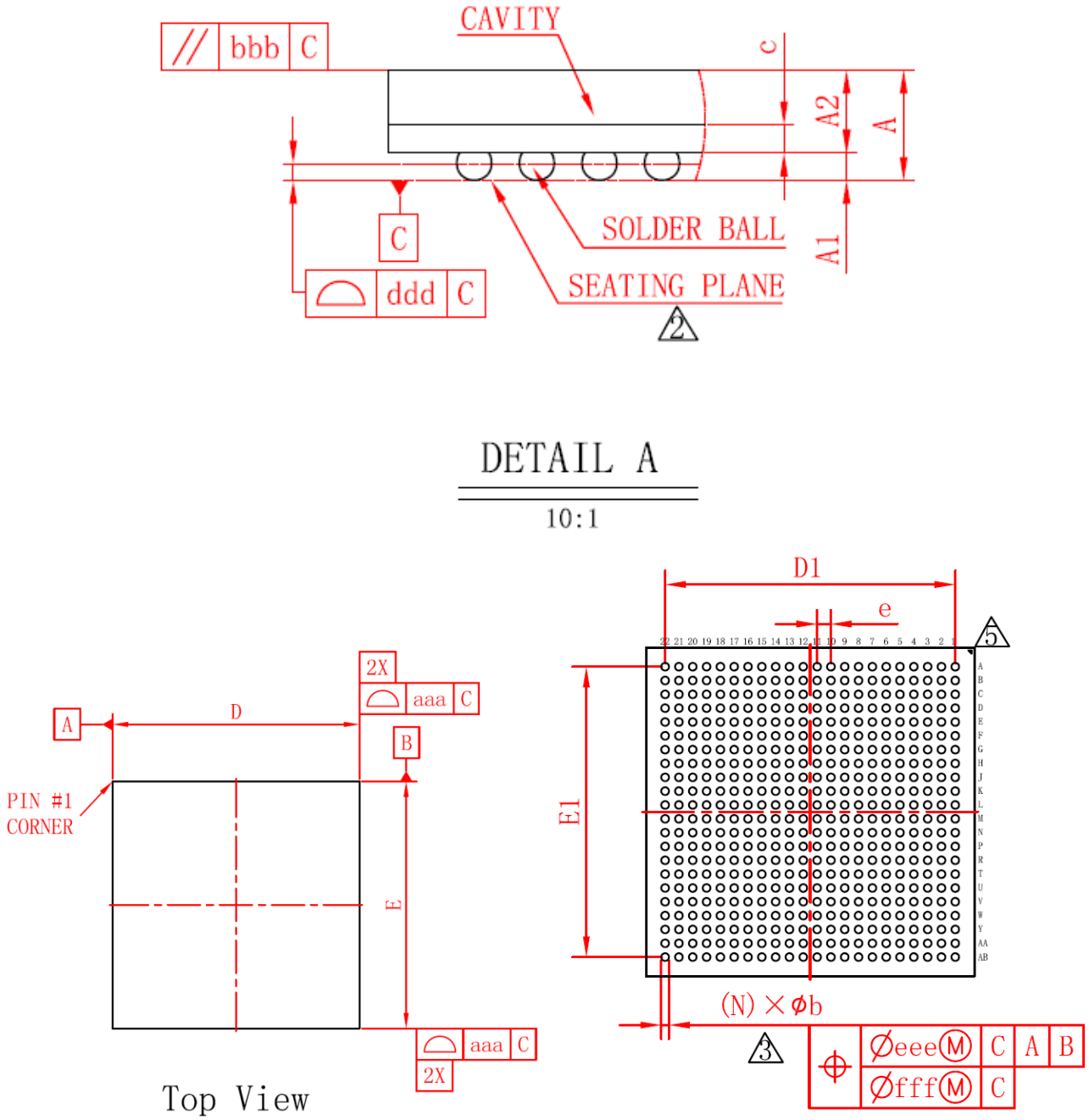

Figure 2-1 Package Outline Dimension (POD)

2.2 Pin Description

The PGC10KD_MBG484 device has 384 user I/Os.

Table 2-2 Device Pin Definitions

Pin Name	Pin Type	Direction	Pin Description
User I/O Pin			
DIFF[I,IO]_XX_NN[P,N]	User pin	Input/Output	User I/O. (1) DIFFI indicates support for differential signal input and pseudo-differential output; DIFFIO indicates support for differential signal input and true differential output, which can be used for transmitting and receiving LVDS

Pin Name	Pin Type	Direction	Pin Description
			signals; (2) “XX” denotes the Bank number, with possible values being B0, B1, B2, B3, B4, and B5; (3) “NN” denotes the sequence number of the programmable I/O group within the Bank, starting from 0 and increasing incrementally; (4) [P,N]: “P” denotes the positive side of the differential pair, and “N” denotes the negative side; During power-up, the user I/O is at a low voltage; After power-up is complete but before configuration, the general user I/O is at pull-down status; During configuration, the user I/O is at pull-down status;
Configuration[1]			
INIT_FLAG_N	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, with an internal weak pull-up resistor. When used as a configuration pin: During power-up, it is at a low voltage; After power-up is complete before configuration, it is open-drain at weak pull-up status; During configuration, it is open-drain at weak pull-up status; During initialization, the pin can be driven to a low voltage by an external input to indicate an error or to delay configuration. During configuration, the pin serves as an indicator output for configuration errors, where a low voltage indicates an error has occurred;
CFG_DONE	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, with an internal weak pull-up resistor. When it is used as configuration pin, it serves as an indicator output for configuration completion, where a high voltage indicates configuration is complete; Before or during configuration, the pin is driven to a low voltage; after configuration is complete, the pin can continue to be driven to a low voltage by an external source. If the internal start-up timing detects CFG_DONE at a low voltage, the internal start-up circuitry maintains its state until CFG_DONE goes high to continue the start-up process;
RSTN	Multi-function pin	Input	Configurable multiplexed reset pin, with an internal weak pull-up resistor. When it is used as a reset pin, it serves to restart the configuration process, active low. At this situation, it must be pulled up with an external resistor (internal weak pull-up resistor typically has a value of over 20kOhms, with a relatively weak pull-up strength); when the pin is at a low voltage, the CPLD enters reset state, with all I/Os in a weak pull-down status;
CFG_CLK	Multi-function pin	Input/Output	Configurable multiplexed clock pin, with an internal weak pull-up resistor. When it is used as a configuration pin: In slave SPI configuration mode, the pin serves as a clock input to acquire configuration data from an external source; In master SPI configuration mode, the pin serves as a clock output to acquire configuration data from an external source; in this mode, a 1kOhms pull-up resistor is needed; Master SPI mode and slave SPI mode are allowed to be enabled simultaneously, but using them at the same time

Pin Name	Pin Type	Direction	Pin Description
			is not permitted;
TCK	Multi-function pin	Input	Multiplexed JTAG test clock input pin; requires an external 4.7kOhms pull-down resistor;
TMS	Multi-function pin	Input	Multiplexed JTAG test mode select input pin; with an internal weak pull-up resistor, pulled up to VCCIO0;
TDI	Multi-function pin	Input	Multiplexed JTAG test data input pin; with an internal weak pull-up resistor, pulled up to VCCIO0;
TDO	Multi-function pin	Output	Multiplexed JTAG test data output pin; with an internal weak pull-up resistor, pulled up to VCCIO0.
JTAGEN	Multi-function pin	Input	Optional JTAG port behaviour control pin, usually used in user mode, when JTAG pins are configured as configuration I/Os, this pin is user I/O, with the state controlled by the user; when JTAG pins serve as user I/Os, JTAGEN serves as a dedicated input used to control the availability of JTAG pins; the default state is weak pull-down; when JTAGEN is configured as a dedicated I/O: (1) When at a low voltage, the JTAG pins function as user I/Os; (2) When at a high voltage, the JTAG pins function as JTAG configuration port.
FCS_N	Multi-function pin	Output	Configurable multiplexed pin, used for master SPI configuration mode, (1) In master SPI mode, outputs an active-low chip select signal to an external Flash; (2) After configuration is completed, it can be used as a user I/O.
MISO_SO	Multi-function pin	Input/Output	Configurable multiplexed pin; (1) MISO, serial data input in master SPI mode; (2) SO, serial data output in slave SPI mode; Master and slave SPI modes are allowed to be enabled simultaneously, but using them at the same time is not permitted.
MOSI_SI	Multi-function pin	Input/Output	Configurable multiplexed pin; (1) MOSI, serial data output in master SPI mode; (2) SI, serial data input in slave SPI mode; Master and slave SPI modes are allowed to be enabled simultaneously, but using them at the same time is not permitted.
FCSI_N	Multi-function pin	Input	Configurable multiplexed pin, with an internal weak pull-up resistor; In slave SPI mode, active-low chip select input.
SCL	Multi-function pin	Input (Open-drain)	Configurable multiplexed pin, clock input in slave I2C mode; requires an external weak pull-up resistor.
SDA	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, data input/output in I2C mode; requires an external weak pull-up resistor.
SPAL_CLK	Multi-function pin	Input	Clock input in slave parallel X16 configuration mode.
SPAL_CS_N	Multi-function pin	Input	Chip select input in slave parallel X16 configuration mode. Active-low
SPAL_RDWR_N	Multi-function pin	Input	Read/write control input in slave parallel X16 configuration mode; 1: read; 0: write.

Pin Name	Pin Type	Direction	Pin Description
SPAL_BUSY	Multi-function pin	Output	Busy indicator in slave parallel X16 configuration mode; During readback, if the data is not ready, SPAL_BUSY changes to high voltage.
SPAL_D15~SPAL_D0	Multi-function pin	Input/Output	Data bus in slave parallel X16 configuration mode.
Clock, PLL			
CLK[0,1,2][P,N]_[B0,B1,…,B5]	Multi-function pin	Input	Global clock input pin; can also be used as user I/O; (1) [0,1,2]: clock pin numbers; (2) [P,N]: positive and negative sides of the differential clock pins; (3) [B0,B1,…,B5]: bank numbers.
PLL[0,1]_CLKIN_[P,N]	Multi-function pin	Input	PLL input. PLL can choose to directly input a clock from these pins; they can also be used as user I/Os; (1) [0,1]: corresponds to PLL0 and PLL1; (2) [P,N]: positive and negative sides of the differential clock pins.
PLL[0,1]_CLKFB_[P,N]	Multi-function pin	Input	Optional PLL feedback clock input. PLL can select to feedback clock externally from these pins; they can also be used as user I/Os; (1) [0,1]: corresponds to PLL0 and PLL1; (2) [P,N]: positive and negative sides of the differential clock pins.
Power			
VCC		Power	External power supply of 2.5V or 3.3V, providing power to the core logic.
VCCIO[0,1,2,3,4,5]		Power	I/O Bank power.
VSS		Ground	Ground associated with VCC;

Note:

1. When the configured multi-function pin is used as a user I/O, its status is the same as the user I/O pin.

2.2.1 Pin Name list

Table 2-3 Pin Name List

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B0	DIFFI_B0_0N/CFG_DONE	E17	IO_1_N	44.1581
B0	DIFFI_B0_0P/INIT_FLAG_N	F16	IO_1_P	42.0152
B0	DIFFIO_B0_1N/SPAL_CLK	B22	IO_2_N	101.216
B0	DIFFIO_B0_1P/SPAL_CS_N	A21	IO_2_P	104.353
B0	DIFFI_B0_2N	C20	IO_3_N	85.5383
B0	DIFFI_B0_2P	C19	IO_3_P	85.1321
B0	DIFFIO_B0_3N/SPAL_RDWR_N	B21	IO_4_N	100.449
B0	DIFFIO_B0_3P/SPAL_BUSY	A20	IO_4_P	102.981
B0	DIFFI_B0_4N	G15	IO_5_N	39.8378
B0	DIFFI_B0_4P	F15	IO_5_P	39.3893
B0	DIFFIO_B0_5N/SPAL_D15	B20	IO_6_N	93.2942
B0	DIFFIO_B0_5P/SPAL_D14	A19	IO_6_P	89.9384

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B0	DIFFI_B0_6N	D18	IO_7_N	67.1366
B0	DIFFI_B0_6P	C18	IO_7_P	67.7956
B0	DIFFIO_B0_7N/SPAL_D13	B19	IO_8_N	85.7801
B0	DIFFIO_B0_7P/SPAL_D12	A18	IO_8_P	90.1877
B0	DIFFI_B0_8N	D17	IO_9_N	67.3182
B0	DIFFI_B0_8P	E16	IO_9_P	66.2487
B0	DIFFIO_B0_9N	B18	IO_10_N	84.5092
B0	DIFFIO_B0_9P	A17	IO_10_P	86.7343
B0	DIFFI_B0_10N	D16	IO_11_N	75.2853
B0	DIFFI_B0_10P	C17	IO_11_P	78.7071
B0	DIFFIO_B0_11N/SPAL_D11	B17	IO_12_N	78.5486
B0	DIFFIO_B0_11P/SPAL_D10	A16	IO_12_P	79.1132
B0	DIFFI_B0_12N	D15	IO_13_N	74.4274
B0	DIFFI_B0_12P	C15	IO_13_P	71.4521
B0	DIFFIO_B0_13N/SPAL_D9	B15	IO_14_N	72.6405
B0	DIFFIO_B0_13P/SPAL_D8	A15	IO_14_P	72.8634
B0	DIFFI_B0_14N/RSTN	E15	IO_15_N	61.1299
B0	DIFFI_B0_14P/JTAGEN	E14	IO_15_P	61.0793
B0	DIFFIO_B0_15N/SPAL_D7	F14	IO_16_N	45.3164
B0	DIFFIO_B0_15P/SPAL_D6	G14	IO_16_P	50.2379
B0	DIFFI_B0_16N	D14	IO_17_N	73.2282
B0	DIFFI_B0_16P	C14	IO_17_P	73.8331
B0	DIFFIO_B0_17N	B14	IO_18_N	73.9777
B0	DIFFIO_B0_17P	A14	IO_18_P	75.1891
B0	DIFFI_B0_18N	D13	IO_19_N	72.0087
B0	DIFFI_B0_18P	C13	IO_19_P	72.8192
B0	DIFFIO_B0_19N/SPAL_D5	B13	IO_20_N	73.0862
B0	DIFFIO_B0_19P/SPAL_D4	A13	IO_20_P	73.1679
B0	DIFFI_B0_20N	F13	IO_21_N	55.2923
B0	DIFFI_B0_20P	E13	IO_21_P	53.9639
B0	DIFFIO_B0_21N/SPAL_D3	F12	IO_22_N	33.8271
B0	DIFFIO_B0_21P/SPAL_D2	G12	IO_22_P	37.0243
B0	DIFFI_B0_22N/SDA/CLK0N_B0	A12	IO_23_N	72.3473
B0	DIFFI_B0_22P/SCL/CLK0P_B0	B12	IO_23_P	69.2241
B0	DIFFIO_B0_23N/SPAL_D1	E12	IO_24_N	69.5664
B0	DIFFIO_B0_23P/SPAL_D0	D12	IO_24_P	65.9319
B0	DIFFI_B0_24N	D11	IO_25_N	73.1602
B0	DIFFI_B0_24P	E11	IO_25_P	75.0894
B0	DIFFIO_B0_25N	A11	IO_26_N	75.8003

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B0	DIFFIO_B0_25P	B11	IO_26_P	74.9829
B0	DIFFI_B0_26N	F11	IO_27_N	49.6474
B0	DIFFI_B0_26P	G11	IO_27_P	44.7229
B0	DIFFIO_B0_27N/CLK1N_B0	A10	IO_28_N	74.521
B0	DIFFIO_B0_27P/CLK1P_B0	B10	IO_28_P	70.2853
B0	DIFFI_B0_28N/TMS	C10	IO_29_N	52.1171
B0	DIFFI_B0_28P/TCK	D10	IO_29_P	54.148
B0	DIFFIO_B0_29N	E10	IO_30_N	47.6422
B0	DIFFIO_B0_29P	F10	IO_30_P	45.8557
B0	DIFFI_B0_30N	G9	IO_31_N	54.3918
B0	DIFFI_B0_30P	F9	IO_31_P	54.0195
B0	DIFFIO_B0_31N	A9	IO_32_N	75.6996
B0	DIFFIO_B0_31P	B9	IO_32_P	75.4379
B0	DIFFI_B0_32N	D9	IO_33_N	67.8894
B0	DIFFI_B0_32P	C9	IO_33_P	67.6541
B0	DIFFIO_B0_33N	A8	IO_34_N	79.344
B0	DIFFIO_B0_33P	B8	IO_34_P	77.1311
B0	DIFFI_B0_34N/TDI	E9	IO_35_N	51.5134
B0	DIFFI_B0_34P/TDO	E8	IO_35_P	52.9525
B0	DIFFIO_B0_35N	D8	IO_36_N	67.0354
B0	DIFFIO_B0_35P	C8	IO_36_P	67.5202
B0	DIFFI_B0_36N	D7	IO_37_N	72.4184
B0	DIFFI_B0_36P	C6	IO_37_P	76.626
B0	DIFFIO_B0_37N	A7	IO_38_N	80.195
B0	DIFFIO_B0_37P	B6	IO_38_P	78.7494
B0	DIFFI_B0_38N	E7	IO_39_N	66.8826
B0	DIFFI_B0_38P	D6	IO_39_P	66.492
B0	DIFFIO_B0_39N	A6	IO_40_N	84.4271
B0	DIFFIO_B0_39P	B5	IO_40_P	85.0596
B0	DIFFI_B0_40N	C5	IO_41_N	83.0635
B0	DIFFI_B0_40P	D5	IO_41_P	86.6597
B0	DIFFIO_B0_41N	A5	IO_42_N	94.2278
B0	DIFFIO_B0_41P	B4	IO_42_P	92.2764
B0	DIFFI_B0_42N	G8	IO_43_N	43.5107
B0	DIFFI_B0_42P	F8	IO_43_P	42.6144
B0	DIFFIO_B0_43N	A4	IO_44_N	91.0147
B0	DIFFIO_B0_43P	B3	IO_44_P	91.9089
B0	DIFFI_B0_44N	C4	IO_45_N	87.1625
B0	DIFFI_B0_44P	C3	IO_45_P	83.58

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B0	DIFFIO_B0_45N	A3	IO_46_N	98.6528
B0	DIFFIO_B0_45P	B2	IO_46_P	95.0752
B0	DIFFI_B0_46N	F7	IO_47_N	48.1724
B0	DIFFI_B0_46P	E6	IO_47_P	45.3045
B0	DIFFIO_B0_47N	A2	IO_48_N	95.9587
B0	DIFFIO_B0_47P	B1	IO_48_P	93.6699
B1	DIFFI_B1_0P/PLL1_CLKFB_P	C21	IO_49_P	89.9321
B1	DIFFI_B1_0N/PLL1_CLKFB_N	C22	IO_49_N	94.3844
B1	DIFFI_B1_1P	F17	IO_50_P	52.3197
B1	DIFFI_B1_1N	G16	IO_50_N	49.3508
B1	DIFFI_B1_2P/PLL1_CLKIN_P	D22	IO_51_P	91.211
B1	DIFFI_B1_2N/PLL1_CLKIN_N	D21	IO_51_N	90.0786
B1	DIFFI_B1_3P	D19	IO_52_P	70.2504
B1	DIFFI_B1_3N	D20	IO_52_N	73.8623
B1	DIFFI_B1_4P	E22	IO_53_P	86.7367
B1	DIFFI_B1_4N	E21	IO_53_N	82.125
B1	DIFFI_B1_5P	E19	IO_54_P	74.6153
B1	DIFFI_B1_5N	E20	IO_54_N	74.4973
B1	DIFFI_B1_6P	F22	IO_55_P	81.8354
B1	DIFFI_B1_6N	G22	IO_55_N	82.2989
B1	DIFFI_B1_7P	F18	IO_56_P	70.6776
B1	DIFFI_B1_7N	F19	IO_56_N	69.3433
B1	DIFFI_B1_8P	G21	IO_57_P	68.3835
B1	DIFFI_B1_8N	G20	IO_57_N	63.5184
B1	DIFFI_B1_9P	G19	IO_58_P	54.6895
B1	DIFFI_B1_9N	G18	IO_58_N	58.9007
B1	DIFFI_B1_10P	H22	IO_59_P	81.832
B1	DIFFI_B1_10N	H21	IO_59_N	81.5461
B1	DIFFI_B1_11P	G17	IO_60_P	58.1466
B1	DIFFI_B1_11N	H20	IO_60_N	59.2817
B1	DIFFI_B1_12P	H19	IO_61_P	73.7222
B1	DIFFI_B1_12N	H18	IO_61_N	71.8708
B1	DIFFI_B1_13P	H17	IO_62_P	52.819
B1	DIFFI_B1_13N	H16	IO_62_N	49.0877
B1	DIFFI_B1_14P	J16	IO_63_P	44.58
B1	DIFFI_B1_14N	J17	IO_63_N	44.5929
B1	DIFFI_B1_15P	J18	IO_64_P	48.4
B1	DIFFI_B1_15N	J19	IO_64_N	46.7977
B1	DIFFI_B1_16P	J21	IO_65_P	71.065

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B1	DIFFI_B1_16N	J22	IO_65_N	71.6907
B1	DIFFI_B1_17P	J20	IO_66_P	65.1153
B1	DIFFI_B1_17N	K20	IO_66_N	64.2489
B1	DIFFI_B1_18P	K19	IO_67_P	58.8176
B1	DIFFI_B1_18N	K18	IO_67_N	56.8342
B1	DIFFI_B1_19P	K17	IO_68_P	46.3118
B1	DIFFI_B1_19N	K16	IO_68_N	45.2361
B1	DIFFI_B1_20P	L17	IO_69_P	40.7479
B1	DIFFI_B1_20N	L16	IO_69_N	41.1085
B1	DIFFI_B1_21P	L19	IO_70_P	66.2622
B1	DIFFI_B1_21N	L20	IO_70_N	63.3123
B1	DIFFI_B1_22P	K22	IO_71_P	75.3544
B1	DIFFI_B1_22N	L21	IO_71_N	72.9509
B1	DIFFI_B1_23P	L22	IO_72_P	68.7188
B1	DIFFI_B1_23N	M17	IO_72_N	45.9583
B1	DIFFI_B1_24P/CLK0P_B1	M22	IO_73_P	70.3073
B1	DIFFI_B1_24N/CLK0N_B1	M21	IO_73_N	65.3649
B1	DIFFI_B1_25P	M20	IO_74_P	43.577
B1	DIFFI_B1_25N	M19	IO_74_N	44.8727
B1	DIFFI_B1_26P	M16	IO_75_P	42.1563
B1	DIFFI_B1_26N	N16	IO_75_N	45.2161
B1	DIFFI_B1_27P	N17	IO_76_P	56.7145
B1	DIFFI_B1_27N	N18	IO_76_N	54.6691
B1	DIFFI_B1_28P	N22	IO_77_P	74.8236
B1	DIFFI_B1_28N	P21	IO_77_N	75.5036
B1	DIFFI_B1_29P	N20	IO_78_P	49.7305
B1	DIFFI_B1_29N	N19	IO_78_N	46.371
B1	DIFFI_B1_30P	R22	IO_79_P	85.9783
B1	DIFFI_B1_30N	R21	IO_79_N	84.6443
B1	DIFFI_B1_31P	P22	IO_80_P	70.0627
B1	DIFFI_B1_31N	P20	IO_80_N	62.4159
B1	DIFFI_B1_32P	T22	IO_81_P	78.832
B1	DIFFI_B1_32N	T21	IO_81_N	77.3419
B1	DIFFI_B1_33P	P19	IO_82_P	40.8222
B1	DIFFI_B1_33N	P18	IO_82_N	40.6157
B1	DIFFI_B1_34P	P17	IO_83_P	43.8143
B1	DIFFI_B1_34N	P16	IO_83_N	43.7784
B1	DIFFI_B1_35P	U22	IO_84_P	88.27
B1	DIFFI_B1_35N	U21	IO_84_N	82.7969

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B1	DIFFI_B1_36P	V22	IO_85_P	101.937
B1	DIFFI_B1_36N	W22	IO_85_N	104.571
B1	DIFFI_B1_37P	R20	IO_86_P	49.6223
B1	DIFFI_B1_37N	R19	IO_86_N	50.3799
B1	DIFFI_B1_38P	R18	IO_87_P	36.0522
B1	DIFFI_B1_38N	R17	IO_87_N	38.7864
B1	DIFFI_B1_39P	R16	IO_88_P	61.1324
B1	DIFFI_B1_39N	T20	IO_88_N	54.5495
B1	DIFFI_B1_40P	T19	IO_89_P	65.0708
B1	DIFFI_B1_40N	T18	IO_89_N	67.3031
B1	DIFFI_B1_41P	T17	IO_90_P	48.0656
B1	DIFFI_B1_41N	U20	IO_90_N	59.4103
B1	DIFFI_B1_42P	Y22	IO_91_P	94.0507
B1	DIFFI_B1_42N	W21	IO_91_N	91.2273
B1	DIFFI_B1_43P	U19	IO_92_P	51.763
B1	DIFFI_B1_43N	U18	IO_92_N	50.7642
B1	DIFFI_B1_44P	AA22	IO_93_P	96.3853
B1	DIFFI_B1_44N	Y21	IO_93_N	95.8991
B1	DIFFI_B1_45P	U17	IO_94_P	60.2247
B1	DIFFI_B1_45N	V19	IO_94_N	61.8253
B1	DIFFI_B1_46P	V18	IO_95_P	68.8343
B1	DIFFI_B1_46N	W20	IO_95_N	70.0462
B1	DIFFI_B1_47P	W19	IO_96_P	74.7152
B1	DIFFI_B1_47N	Y20	IO_96_N	71.1242
B2	DIFFI_B2_0N	T16	IO_97_N	61.121
B2	DIFFI_B2_0P	V17	IO_97_P	59.2232
B2	DIFFI_B2_1N/MOSI_SI	AA21	IO_98_N	90.2607
B2	DIFFI_B2_1P/FCSI_N	AB21	IO_98_P	93.021
B2	DIFFI_B2_2N	W18	IO_99_N	68.7143
B2	DIFFI_B2_2P	Y19	IO_99_P	67.8765
B2	DIFFI_B2_3N	AA20	IO_100_N	86.3805
B2	DIFFI_B2_3P	AB20	IO_100_P	87.5764
B2	DIFFI_B2_4N	U16	IO_101_N	55.2471
B2	DIFFI_B2_4P	T15	IO_101_P	56.8704
B2	DIFFI_B2_5N	AA19	IO_102_N	85.4742
B2	DIFFI_B2_5P	AB19	IO_102_P	84.944
B2	DIFFI_B2_6N	W17	IO_103_N	61.7192
B2	DIFFI_B2_6P	Y18	IO_103_P	67.3839
B2	DIFFI_B2_7N	AA18	IO_104_N	78.6055

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B2	DIFFI_B2_7P	AB18	IO_104_P	82.0492
B2	DIFFI_B2_8N	V16	IO_105_N	64.3751
B2	DIFFI_B2_8P	Y17	IO_105_P	63.2469
B2	DIFFI_B2_9N	AA17	IO_106_N	74.6345
B2	DIFFI_B2_9P	AB17	IO_106_P	76.7311
B2	DIFFI_B2_10N	U15	IO_107_N	51.0028
B2	DIFFI_B2_10P	V15	IO_107_P	49.6474
B2	DIFFI_B2_11N	AA16	IO_108_N	72.3823
B2	DIFFI_B2_11P	AB16	IO_108_P	75.6033
B2	DIFFI_B2_12N	W15	IO_109_N	51.9499
B2	DIFFI_B2_12P	Y15	IO_109_P	50.4865
B2	DIFFI_B2_13N	AA15	IO_110_N	73.3916
B2	DIFFI_B2_13P	AB15	IO_110_P	73.5913
B2	DIFFI_B2_14N	W14	IO_111_N	67.1713
B2	DIFFI_B2_14P	Y14	IO_111_P	68.0743
B2	DIFFI_B2_15N	AA14	IO_112_N	76.0411
B2	DIFFI_B2_15P	AB14	IO_112_P	79.388
B2	DIFFI_B2_16N	V14	IO_113_N	49.6666
B2	DIFFI_B2_16P	U14	IO_113_P	50.11
B2	DIFFI_B2_17N	T14	IO_114_N	39.1316
B2	DIFFI_B2_17P	T13	IO_114_P	38.6175
B2	DIFFI_B2_18N	W13	IO_115_N	47.3463
B2	DIFFI_B2_18P	Y13	IO_115_P	50.599
B2	DIFFI_B2_19N	AA13	IO_116_N	70.1005
B2	DIFFI_B2_19P	AB13	IO_116_P	72.2288
B2	DIFFI_B2_20N	U13	IO_117_N	61.0868
B2	DIFFI_B2_20P	V13	IO_117_P	62.2712
B2	DIFFI_B2_21N/CLK1N_B2	AA12	IO_118_N	68.3461
B2	DIFFI_B2_21P/CLK1P_B2	AB12	IO_118_P	68.2548
B2	DIFFI_B2_22N	V12	IO_119_N	52.1019
B2	DIFFI_B2_22P	U12	IO_119_P	50.6727
B2	DIFFI_B2_23N	T12	IO_120_N	37.872
B2	DIFFI_B2_23P	Y12	IO_120_P	53.1803
B2	DIFFI_B2_24N	Y11	IO_121_N	55.0224
B2	DIFFI_B2_24P	V11	IO_121_P	50.5843
B2	DIFFI_B2_25N	AB11	IO_122_N	72.0645
B2	DIFFI_B2_25P	AA11	IO_122_P	69.7233
B2	DIFFI_B2_26N	U11	IO_123_N	48.5421
B2	DIFFI_B2_26P	T11	IO_123_P	51.2628

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B2	DIFFI_B2_27N/CLK0N_B2	AB10	IO_124_N	74.1521
B2	DIFFI_B2_27P/CLK0P_B2	AA10	IO_124_P	72.7547
B2	DIFFI_B2_28N	Y10	IO_125_N	65.892
B2	DIFFI_B2_28P	Y9	IO_125_P	65.4287
B2	DIFFI_B2_29N	W10	IO_126_N	45.5179
B2	DIFFI_B2_29P	V10	IO_126_P	44.3046
B2	DIFFI_B2_30N	U10	IO_127_N	72.6741
B2	DIFFI_B2_30P	T10	IO_127_P	73.0586
B2	DIFFI_B2_31N	AB9	IO_128_N	72.3052
B2	DIFFI_B2_31P	AA9	IO_128_P	72.9187
B2	DIFFI_B2_32N	W9	IO_129_N	67.7401
B2	DIFFI_B2_32P	Y8	IO_129_P	66.9953
B2	DIFFI_B2_33N	AB8	IO_130_N	75.1821
B2	DIFFI_B2_33P	AA8	IO_130_P	73.6929
B2	DIFFI_B2_34N	W8	IO_131_N	48.2719
B2	DIFFI_B2_34P	V9	IO_131_P	50.1957
B2	DIFFI_B2_35N/MISO_SO	U9	IO_132_N	41.4993
B2	DIFFI_B2_35P/CFG_CLK	T9	IO_132_P	42.242
B2	DIFFI_B2_36N	U8	IO_133_N	53.9324
B2	DIFFI_B2_36P	V8	IO_133_P	51.2126
B2	DIFFI_B2_37N	AB7	IO_134_N	76.9426
B2	DIFFI_B2_37P	AA7	IO_134_P	74.8264
B2	DIFFI_B2_38N	V7	IO_135_N	67.4861
B2	DIFFI_B2_38P	W6	IO_135_P	66.5191
B2	DIFFI_B2_39N	AB6	IO_136_N	76.0223
B2	DIFFI_B2_39P	AA6	IO_136_P	76.5035
B2	DIFFI_B2_40N	Y6	IO_137_N	70.5842
B2	DIFFI_B2_40P	Y5	IO_137_P	70.1176
B2	DIFFI_B2_41N	AB5	IO_138_N	83.7488
B2	DIFFI_B2_41P	AA5	IO_138_P	81.9767
B2	DIFFI_B2_42N	T8	IO_139_N	59.2843
B2	DIFFI_B2_42P	U7	IO_139_P	59.2563
B2	DIFFI_B2_43N	AB4	IO_140_N	85.1267
B2	DIFFI_B2_43P	AA4	IO_140_P	82.7867
B2	DIFFI_B2_44N	W5	IO_141_N	68.9687
B2	DIFFI_B2_44P	Y4	IO_141_P	68.2746
B2	DIFFI_B2_45N	AB3	IO_142_N	88.7414
B2	DIFFI_B2_45P/FCS_N	AA3	IO_142_P	89.5246
B2	DIFFI_B2_46N	U6	IO_143_N	47.4914

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B2	DIFFI_B2_46P	V6	IO_143_P	49.9104
B2	DIFFI_B2_47N	AB2	IO_144_N	94.6521
B2	DIFFI_B2_47P	AA2	IO_144_P	94.5417
B3	DIFFI_B3_0P	P4	IO_145_P	46.7842
B3	DIFFI_B3_0N	N5	IO_145_N	43.4722
B3	DIFFI_B3_1P	N6	IO_146_P	44.9567
B3	DIFFI_B3_1N	N7	IO_146_N	46.2748
B3	DIFFI_B3_2P	R2	IO_147_P	75.8239
B3	DIFFI_B3_2N	T1	IO_147_N	79.4494
B3	DIFFI_B3_3P	P5	IO_148_P	62.5801
B3	DIFFI_B3_3N	P6	IO_148_N	62.435
B3	DIFFI_B3_4P	R3	IO_149_P	52.4087
B3	DIFFI_B3_4N	R4	IO_149_N	53.5132
B3	DIFFI_B3_5P	R5	IO_150_P	57.799
B3	DIFFI_B3_5N	P7	IO_150_N	53.0073
B3	DIFFI_B3_6P	T2	IO_151_P	74.3572
B3	DIFFI_B3_6N	U1	IO_151_N	76.9209
B3	DIFFI_B3_7P	R6	IO_152_P	49.9551
B3	DIFFI_B3_7N	R7	IO_152_N	48.2151
B3	DIFFI_B3_8P	T3	IO_153_P	74.7175
B3	DIFFI_B3_8N	T4	IO_153_N	77.0327
B3	DIFFI_B3_9P	T5	IO_154_P	59.0191
B3	DIFFI_B3_9N	T6	IO_154_N	56.4829
B3	DIFFI_B3_10P/CLK0P_B3	U2	IO_155_P	84.5506
B3	DIFFI_B3_10N/CLK0N_B3	V1	IO_155_N	85.9559
B3	DIFFI_B3_11P	U3	IO_156_P	60.9337
B3	DIFFI_B3_11N	U4	IO_156_N	63.5072
B3	DIFFI_B3_12P	W1	IO_157_P	88.3699
B3	DIFFI_B3_12N	W2	IO_157_N	86.0624
B3	DIFFI_B3_13P	V4	IO_158_P	65.6674
B3	DIFFI_B3_13N	U5	IO_158_N	60.6316
B3	DIFFI_B3_14P	Y1	IO_159_P	93.9386
B3	DIFFI_B3_14N	AA1	IO_159_N	94.7535
B3	DIFFI_B3_15P	W3	IO_160_P	82.1783
B3	DIFFI_B3_15N	Y2	IO_160_N	79.4457
B3	DIFFI_B3_16P	Y3	IO_161_P	78.7893
B3	DIFFI_B3_16N	W4	IO_161_N	74.6288
B3	DIFFI_B3_17P	V5	IO_162_P	54.7152
B3	DIFFI_B3_17N	T7	IO_162_N	44.7298

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B4	DIFFI_B4_0P	L7	IO_163_P	34.7226
B4	DIFFI_B4_0N	K5	IO_163_N	37.3783
B4	DIFFI_B4_1P	K4	IO_164_P	52.4748
B4	DIFFI_B4_1N	K3	IO_164_N	51.6084
B4	DIFFI_B4_2P	K2	IO_165_P	70.4106
B4	DIFFI_B4_2N	K1	IO_165_N	72.5388
B4	DIFFI_B4_3P	L6	IO_166_P	53.5227
B4	DIFFI_B4_3N	L5	IO_166_N	53.9813
B4	DIFFI_B4_4P/CLK0P_B4	L1	IO_167_P	72.8229
B4	DIFFI_B4_4N/CLK0N_B4	M2	IO_167_N	72.3549
B4	DIFFI_B4_5P	L3	IO_168_P	79.3173
B4	DIFFI_B4_5N	L4	IO_168_N	79.8032
B4	DIFFI_B4_6P	M1	IO_169_P	80.1619
B4	DIFFI_B4_6N	N1	IO_169_N	84.6552
B4	DIFFI_B4_7P	M6	IO_170_P	78.5928
B4	DIFFI_B4_7N	M5	IO_170_N	78.3527
B4	DIFFI_B4_8P	N2	IO_171_P	77.9479
B4	DIFFI_B4_8N	P1	IO_171_N	79.0874
B4	DIFFI_B4_9P	N3	IO_172_P	69.7
B4	DIFFI_B4_9N	N4	IO_172_N	71.8529
B4	DIFFI_B4_10P	P2	IO_173_P	74.4074
B4	DIFFI_B4_10N	R1	IO_173_N	77.337
B4	DIFFI_B4_11P	P3	IO_174_P	51.5676
B4	DIFFI_B4_11N	M7	IO_174_N	49.1565
B5	DIFFI_B5_0P	D3	IO_175_P	75.06
B5	DIFFI_B5_0N	D4	IO_175_N	71.5331
B5	DIFFI_B5_1P	F6	IO_176_P	51.8809
B5	DIFFI_B5_1N	G7	IO_176_N	53.3994
B5	DIFFI_B5_2P/PLL0_CLKFB_P	E4	IO_177_P	56.5293
B5	DIFFI_B5_2N/PLL0_CLKFB_N	F5	IO_177_N	52.1851
B5	DIFFI_B5_3P	G6	IO_178_P	73.5069
B5	DIFFI_B5_3N	H7	IO_178_N	73.3
B5	DIFFI_B5_4P/PLL0_CLKIN_P	C1	IO_179_P	87.6586
B5	DIFFI_B5_4N/PLL0_CLKIN_N	D2	IO_179_N	86.4717
B5	DIFFI_B5_5P	G5	IO_180_P	50.1828
B5	DIFFI_B5_5N	H6	IO_180_N	49.0769
B5	DIFFI_B5_6P	D1	IO_181_P	94.031
B5	DIFFI_B5_6N	E2	IO_181_N	95.8008
B5	DIFFI_B5_7P	E3	IO_182_P	75.0581

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B5	DIFFI_B5_7N	F4	IO_182_N	76.7714
B5	DIFFI_B5_8P	E1	IO_183_P	90.0466
B5	DIFFI_B5_8N	F1	IO_183_N	88.9151
B5	DIFFI_B5_9P	G3	IO_184_P	56.5792
B5	DIFFI_B5_9N	G4	IO_184_N	56.0662
B5	DIFFI_B5_10P/CLK0P_B5	G2	IO_185_P	74.4221
B5	DIFFI_B5_10N/CLK0N_B5	G1	IO_185_N	75.0408
B5	DIFFI_B5_11P	H4	IO_186_P	70.7352
B5	DIFFI_B5_11N	H3	IO_186_N	70.0401
B5	DIFFI_B5_12P	H2	IO_187_P	72.1844
B5	DIFFI_B5_12N	H1	IO_187_N	72.956
B5	DIFFI_B5_13P	J7	IO_188_P	59.6711
B5	DIFFI_B5_13N	J6	IO_188_N	61.2986
B5	DIFFI_B5_14P	H5	IO_189_P	78.1215
B5	DIFFI_B5_14N	J5	IO_189_N	79.6212
B5	DIFFI_B5_15P	J4	IO_190_P	49.5885
B5	DIFFI_B5_15N	J3	IO_190_N	52.2541
B5	DIFFI_B5_16P	J2	IO_191_P	74.3228
B5	DIFFI_B5_16N	J1	IO_191_N	73.1967
B5	DIFFI_B5_17P	K7	IO_192_P	59.9661
B5	DIFFI_B5_17N	K6	IO_192_N	60.208
	VSS	A1		
	VCC	K10		
	VCC	K11		
	VCC	K12		
	VCC	K13		
	VCC	L11		
	VCC	L12		
	VCC	M11		
	VCC	M12		
	VCC	N10		
	VCC	N11		
	VCC	N12		
	VCC	N13		
	VCCIO0	C7		
	VCCIO0	C12		
	VCCIO0	C16		
	VCCIO0	G10		
	VCCIO0	G13		

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
	VCCIO0	H9		
	VCCIO0	H11		
	VCCIO0	H12		
	VCCIO0	H14		
	VCCIO1	F20		
	VCCIO1	J15		
	VCCIO1	K15		
	VCCIO1	L15		
	VCCIO1	M15		
	VCCIO1	M18		
	VCCIO1	N15		
	VCCIO1	P15		
	VCCIO1	V20		
	VCCIO2	R9		
	VCCIO2	R10		
	VCCIO2	R11		
	VCCIO2	R12		
	VCCIO2	R13		
	VCCIO2	R14		
	VCCIO2	W7		
	VCCIO2	W11		
	VCCIO2	W16		
	VCCIO3	N8		
	VCCIO3	P8		
	VCCIO3	V3		
	VCCIO4	L8		
	VCCIO4	M3		
	VCCIO4	M8		
	VCCIO5	F3		
	VCCIO5	J8		
	VCCIO5	K8		
	VSS	A22		
	VSS	B7		
	VSS	B16		
	VSS	C2		
	VSS	C11		
	VSS	E5		
	VSS	E18		
	VSS	F2		

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
	VSS	F21		
	VSS	H8		
	VSS	H10		
	VSS	H13		
	VSS	H15		
	VSS	J9		
	VSS	J10		
	VSS	J11		
	VSS	J12		
	VSS	J13		
	VSS	J14		
	VSS	K9		
	VSS	K14		
	VSS	K21		
	VSS	L2		
	VSS	L9		
	VSS	L10		
	VSS	L13		
	VSS	L14		
	VSS	L18		
	VSS	M4		
	VSS	M9		
	VSS	M10		
	VSS	M13		
	VSS	M14		
	VSS	N9		
	VSS	N14		
	VSS	N21		
	VSS	P9		
	VSS	P10		
	VSS	P11		
	VSS	P12		
	VSS	P13		
	VSS	P14		
	VSS	R8		
	VSS	R15		
	VSS	V2		
	VSS	V21		
	VSS	W12		

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
	VSS	Y7		
	VSS	Y16		
	VSS	AB1		
	VSS	AB22		

2.2.2 Thermal Resistance

Table 2-4 Thermal Resistance Data

θJA(°C/W) (Flow: 0m/s)	θJB (°C/W)	θJC (°C/W)	θJA(°C/W) (Flow: 1m/s)	θJA(°C/W) (Flow: 2m/s)
19.6	11.5	8.9	16.1	15.0

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