Logos Family PGL100H-FBG900 Configurable Multi-function PINs Application Guide

(AN02023, V1.0)

(24.08.2021)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.0	24.08.2021	Initial release

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Chapter 1 Overview

A configurable multiplexed PIN can be used as a configuration interface during the configuration, and after the completion of the configuration, it can be used as a standard IO for the user in user mode. Reconfiguration when power on refers to the FPGA not powering down in user mode; the reconfiguration is triggered by resetting the device. In reconfiguration when power on mode, some considerations on using a configurable multi-function PIN as a user IO shall be taken into account in the PCB design or logic design. The configurable multi-function PINs are all on Bank0, Bank1, and Bank2. There is no need to consider the application of configurable multiplexed IOs in other banks.

The configurable multi-function PINs must be used with the considerations in mind to avoid the following problem scenario: Reconfiguration when power on in user mode FPGA, and if the user logic uses the configurable multi-function PIN as an output, then after reset, this multi-function PIN be in a non-high impedance state for a brief period (less than 100ns) (some IOs at a high level and some at a low level). The process is shown in the following figure:

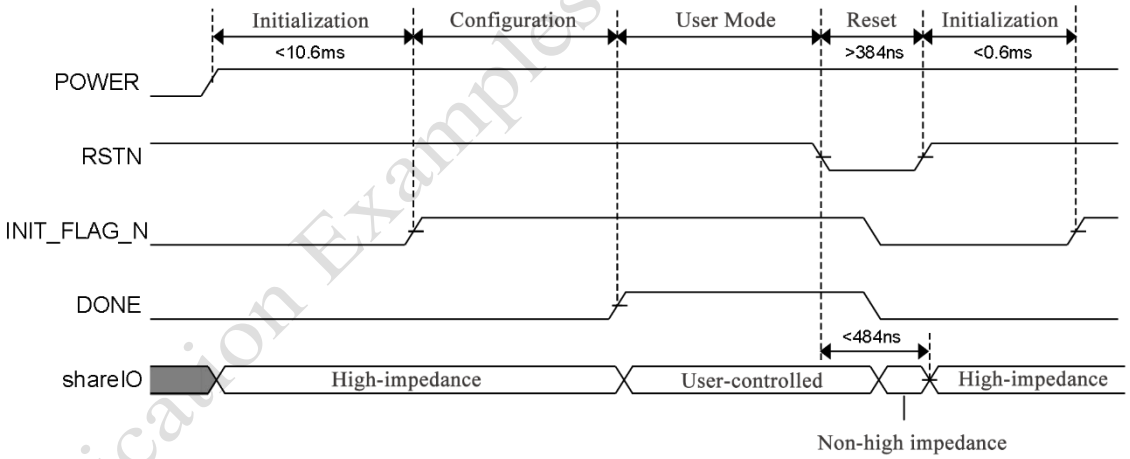

Figure 1-1 Non-High Impedance Process Diagram

This scenario mainly affects applications that require IO to maintain a fixed level during the reconfiguration process. For example, a configurable multi-function PIN is used as the enable or reset signal for other devices, and an external pull-up (or pull-down) of the FPGA is applied to keep the signal level stable during the configuration. In this case, it is expected that after the FPGA is reset, the multi-function PIN output would be in a high impedance state, but the existence of the non-high impedance process may cause changes to the enable or reset signal. If the counterpart device cares about the state of this signal during reconfiguration, and if the user system does not

have a mechanism to prevent abnormal signals under abnormal operation of the FPGA, it could affect the operation of other devices.

The possible triggers are: Reconfiguration when power on the FPGA and use the configurable multi-function PIN as user output.

Chapter 2 PCB Design Considerations

Design considerations are as follows:

1. If a configurable multi-function PIN is used as an input in user mode, it will not affect the design
2. If a configurable multi-function PIN is used as an output in user mode, the following considerations shall be observed:
    1) Pin IO_STATUS_C requires an external pull-up
    2) If the configurable multi-function PIN used needs to be maintained at a fixed level during the configuration, select a pin using the following method:
    For a fixed high level, choose a pin from Table 2-1 and apply an external pull-up (A pull-up resistor of 4.7K is recommended);
    For a fixed low level, choose one from Table 2-2 and apply an external pull-down (A pull-down resistor of 4.7K is recommended).
    For example:
    If a signal needs to remain at a high level during the configuration, users can choose pins such as BFCE_N, BFOE_N and apply an external pull-up;
    If a signal needs to remain at a low level during the configuration, users can choose ADR25, ADR24 etc., and apply an external pull-down;
    If there is no need to maintain at a fixed level, no action is required.

Table 2-1 Configurable Multi-function PINs that Can Remain at a High-Level During Configuration

Bank Name	Pin Name (Function name)	Pin Number
B1	DIFFI_B1_18P/BFCE_N	AA27
B1	DIFFI_B1_18N/BFOE_N	AA28
B1	DIFFI_B1_19P/BFWE_N	Y26
B1	DIFFI_B1_19N/BLDC	Y27
B1	DIFFI_B1_20P/BHDC	AD28
B2	DIFFIO_B2_0N/CSO_N	AK6
B2	DIFFIO_B2_11N/RWSEL/VREF_B2	AC13
B2	DIFFIO_B2_23N/GCLK0/PLL8_CLK8/ECCLK	AG16
B2	DIFFIO_B2_33P/MODE_1	AG24
B2	DIFFIO_B2_45N/MODE_0	AK26
B2	DIFFIO_B2_45P/CFG_CLK	AJ26

Table 2-2 Configurable Multi-function PINs that Can Remain at a Low-Level During Configuration

Bank Name	Pin Name (Function name)	Pin Number
B5	DIFFI_B5_0P/ADR25	G25
B5	DIFFI_B5_0N/ADR24/VREF_B5	F25
B1	DIFFI_B1_1P/ADR23	N29
B1	DIFFI_B1_1N/ADR22	N30
B1	DIFFI_B1_2P/ADR21	N27
B1	DIFFI_B1_2N/ADR20	N28
B1	DIFFI_B1_3P/ADR19	P28
B1	DIFFI_B1_3N/ADR18	P30
B1	DIFFI_B1_4P/ADR17	P26
B1	DIFFI_B1_4N/ADR16	P27
B1	DIFFI_B1_5P/ADR15	R29
B1	DIFFI_B1_5N/ADR14	R30
B1	DIFFI_B1_6P/ADR13	R27
B1	DIFFI_B1_6N/ADR12	R28
B1	DIFFI_B1_7P/ADR11	T26
B1	DIFFI_B1_7N/ADR10	T27
B1	DIFFI_B1_8P/ADR9	T28
B1	DIFFI_B1_8N/ADR8	T30
B1	DIFFI_B1_9P/ADR7	U29
B1	DIFFI_B1_9N/ADR6	U30
B1	DIFFI_B1_10P/ADR5	U27
B1	DIFFI_B1_10N/ADR4	U28
B1	DIFFI_B1_16P/ADR3	Y28
B1	DIFFI_B1_16N/ADR2	Y30
B1	DIFFI_B1_17P/ADR1	AA29
B1	DIFFI_B1_17N/ADR0	AA30
B1	DIFFI_B1_46N/DOUT_BUSY	AA25
B2	DIFFIO_B2_0P/INIT_FLAG_N	AJ6
B2	DIFFIO_B2_1N/D9	AH6
B2	DIFFIO_B2_1P/D8	AG6
B2	DIFFIO_B2_3N/D6	AK7
B2	DIFFIO_B2_3P/D5	AH7
B2	DIFFIO_B2_10N/D4	AF11
B2	DIFFIO_B2_10P/D3	AE11
B2	DIFFIO_B2_11P/D7	AB13
B2	DIFFIO_B2_22N/GCLK30/PLL8_CLK6/D15	AK16
B2	DIFFIO_B2_22P/GCLK31/PLL8_CLK7/D14	AH16
B2	DIFFIO_B2_23P/GCLK1/PLL8_CLK9/D13	AF16

Bank Name	Pin Name (Function name)	Pin Number
B2	DIFFIO_B2_32N/D12	AD19
B2	DIFFIO_B2_32P/D11	AC19
B2	DIFFIO_B2_33N/D10	AH24
B2	DIFFIO_B2_34N/D2	AC20
B2	DIFFIO_B2_34P/D1	AB20
B2	DIFFIO_B2_43N/CS_N	AK25
B2	DIFFIO_B2_43P/D0	AJ25

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