Logos2 Family Products Low-Power Design Application Guide

(AN04026, V1.0)

(14.11.2023)

Shenzhen Pango Microsystems Co., Ltd.

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.0	14.11.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
DRM	Dedicated RAM Module
T_{jmax}	Maximum Junction Temperature
θ_{JA}	Junction to Ambient Thermal Resistance
DE	Design Editor
HSST	High Speed Serial Transceiver
PPP	Pango Power Planner
PPC	Pango Power Calculator
CLM	Configurable Logic Module
GTP	Generic Technology Primitive

Table of Contents

Tables

Figures

Chapter 1 Overview

This document mainly introduces the composition of FPGA power and common methods to reduce FPGA power from a design perspective.

Chapter 2 Composition of FPGA Power

FPGA power generally consists of 3 parts: Static power of the chip, static power of the design, and dynamic power of the design.

- Static power of the chip:
  It is mainly caused by leakage current. After the chip is powered up, leakage current always exists, regardless of whether the chip is working or idle
- Static power of the design:
  After the FPGA configuration is completed, before the design is started, it is necessary to maintain the quiescent current of I/O, clock management, and other circuits.
- Dynamic power of the design:
  It refers to the power of the design after the design in the FPGA is started normally. Its amount mainly depends on the internal logic of the FPGA and the occupation of routing resources.

Dynamic power is mainly caused by capacitor charging and discharging, and it is related to 3 parameters: Node capacitance, operating frequency, and core voltage. They are proportional to power. Larger node capacitance results in higher operating frequency, greater core voltage, and increased dynamic power In FPGAs, dynamic power mainly includes the power consumed by the memory, internal logic, clocks, and I/O.

Chapter 3 How to Reduce Power

Static power depends on the FPGA chip and hardware design, so it cannot be significantly reduced. It is relatively easier to reduce the dynamic power of the design, which plays a key role in reducing the entire system's power.

3.1 System-level Power Reduction Techniques

- Select low-voltage devices
- Use low-ripple power supplies
- Choose devices with larger packages within the same family of chips
- Select smaller devices that meet performance requirements
- Lower the ambient temperature
- Install heat sinks
- Increase airflow

3.2 Design-level Power Reduction Techniques

3.2.1 Static Power Reduction Design Guide

To reduce the static power of the design, all input connections must be given to avoid dangling input pins.

In many applications, pull-up or pull-down resistors are used to determine the I/O level status. To reduce power, the IO pin connected to pull-up/down resistor should be: either set to high-impedance or consistent with the pull-up/down level state.

Excessive power is usually caused by the contrary between the I/O output drive level and the state of the external pull-up/down resistor. Proper connections of FPGA IO pins help reduce power, while improper connections will result in unnecessary power. For example, with an interface voltage of 3.3V and a 10kΩ pull-up resistor, if the output is low, then the power consumption of a single pin can exceed 1mW. Therefore, to reduce power, it is recommended to connect as Table 3-1.

Table 3-1 Relationship between IO Pin Configuration and Power

Pin Type	**IO Configuration**	**Resistor Connection Condition**	**Low-power Scenarios**	**Situations to Avoid (Higher Power)**
Used pins	Output (output drive, bidirectional I/O enable output)	None	High/low output drive	Bus contention (a high driver vs a low driver)
		External pull-up resistor	High-impedance state or high output	Continuous low output
		External pull-down resistor	High-z state or low output	Continuous high output
	Input	None	Stable high/low level	or indefinite input state; slowly changing input
		Internal or external pull-up resistor	High-z state or high input	Low input
		Internal or external pull-down resistor	High-z state or low input	High input
Unused pins	Unused pins	Internal or external pull-up resistor	High-z state or high input	Low input
		Internal or external pull-down resistor	High-z state or low input	High input

3.2.2 Dynamic Power Reduction Design Guide

Apply low-power design techniques in FPGA designs to reduce FPGA power. The table below lists several common low-power design techniques.

Table 3-2 Low-Power Design Techniques

No.	**Low-Power Design Technique**
1	Reduce clock network power
2	Reduce DRM power
3	Pipelining and Retiming
4	State machine encoding
5	Reduce control sets and asynchronous control signals
6	Reduce routing power
7	Architecture optimisation
8	I/O power optimisation
9	Reduce Bank usage
10	Reduce HSSTLP power
11	Reduce DDR power
12	Reduce PLL power
13	Set Preserve to disable the column clocks of CKEBs
14	ADC power

1. Reduce Clock Network Power

In synchronous clock circuit design, most of the power comes from the clock network. This is because the clock signal usually drives a tree-structured clock network, which has a long path and a high toggle rate. Taking the PG2L100H device as an example, when the clock is not needed, use the dedicated PLL's Clock Gate function as well as the GTP_CLKBUFGCE and GTP_CLKBUFGMUX to gate the clockto reduce clock power. It is not recommended to use the CLM logic to control the clock, as this may generate glitchsignals. For high-speed IO CLK, use GTP_IOCLKBUF to enable/disable IO CLK.

For example, GTP_CLKBUFGCE is a clock BUFFER with the Clock Gate function, and it can be used by directly instantiating

GTP in RTL as follows:

```
GTP_CLKBUFGCE
#(
DEFAULT_VALUE (1'b0)      //"TRUE"; "FALSE"
) I_GTP_CLKBUFGCE (
CLKOUT              (Clkout),
CLKIN          (Clkin),
CE                  (ce)      //gate control, CLKOUT outputs default value when low
);
```

For IO CLK, GTP_IOCLKBUF is a clock BUFFER with the Clock Gate function, and it can be used by directly instantiating

GTP in RTL as follows:

```
GTP_IOCLKBUF
#(
GATE_EN ("TRUE")      //"TRUE"; "FALSE"
```

```
) I_GTP_IOCLKBUF (

CLKOUT          (Clkout),

CLKIN           (Clkin),

DI              (Di)        //gate control, CLKOUT outputs none when low

);
```

Use the GTP_CLKBUFGMUX module to control clock selection and thus reduce clock power.

Switch to a lower-frequency clock as needed to reduce power.

In addition, avoid using multiple clock networks in FPGA design. Merge clocks to minimize the number of clocks and optimize clock network design, effectively reducing clock power.

2. Reduce DRM Power

In typical FPGA applications, DRM power accounts for about 20% of the FPGA's core power. When the DRM is working, it performs read and write operations internally according to the timing logic. To reduce DRM power, the key lies in reducing clock inversion events in the memory.Users can control the clock network for clock gating, or use the clock enable port of the DRM.When using the IP Compiler tool to generate DRM IP, users can check "Enable clk_en Signal" to enable the clock enable port, as shown in Figure 3-1.

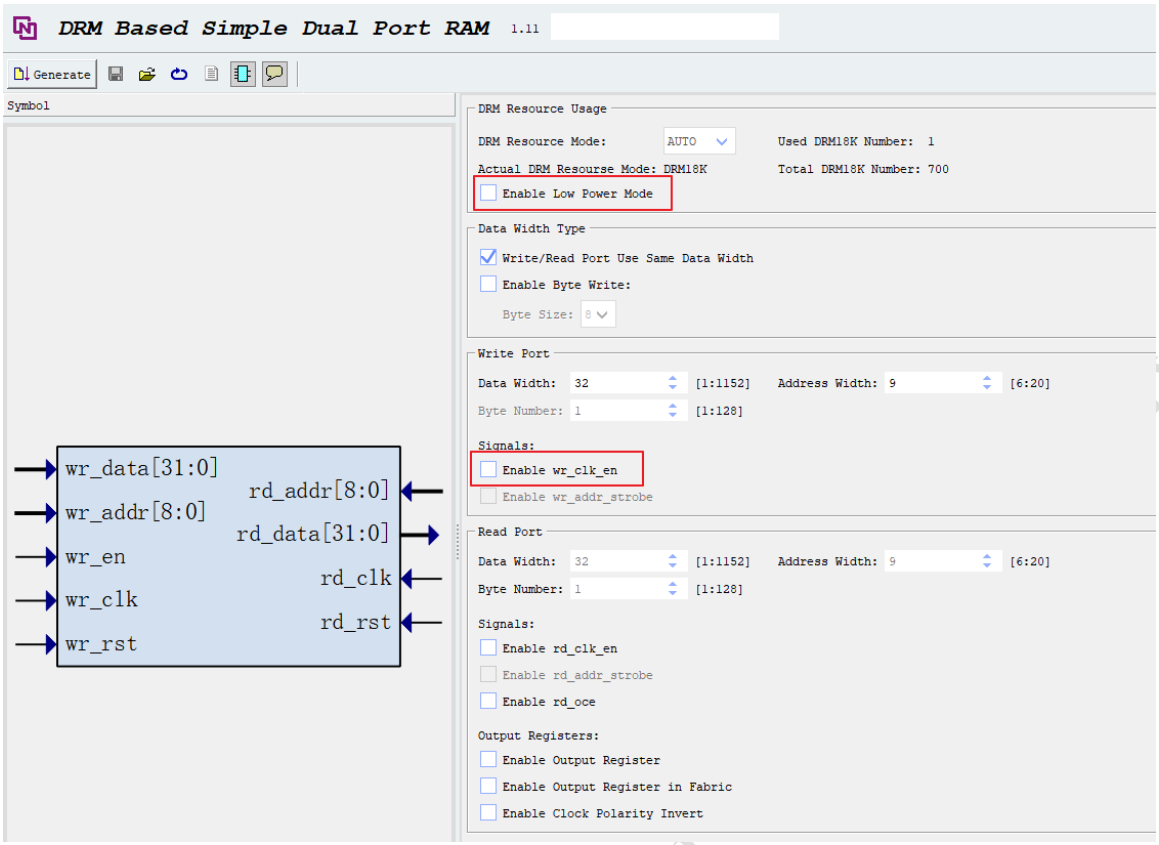

Figure 3-1 Clock Enable Port Option

Avoiding read/write conflicts reduces power consumption.

When a large amount of memory is used in the design, multiple DRMs need to be spliced together. Use a "deep stacking" structure to avoid simultaneous read and write operations on multiple DRMs, thereby reducing power. In other words, check "Enable Low Power Mode" as shown in Figure 3-1. However, the "deep stacking" structure requires additional data selection logic, increasing the logic layers and area, which reduces power while degrading performance.

If the output remains unchanged during write operations, it is recommended to use NormalWrite mode to reduce power.

Choose between distributed RAM and DRM according to the storage scale. When the address depth is less than 64,adopt distributed RAM to optimise power and timing. When the address depth is no less than 64, it is recommended to use DRM.

3. Pipelining and Retiming

In FPGA design, when signal delays differ due to unaligned logical input signals or there are

multiple levels of combinatorial logic between the flip-flops due to many asynchronous operations in design circuits (such as CRC verification circuits, arithmetic circuits), glitches may occur. Glitch signals can cause unnecessary or unexpected logic toggles in the combinatorial logic output. Glitch signals toggle faster than normal logic, resulting in additional power.

Pipelining and Retiming mean inserting flip-flops or adjusting the positions of flip-flops to the middle of long-path combinatorial logic. Since flip-flops can block the propagation of glitches, the circuit will be free of glitch signals after pipelining. Although pipelining increases circuit delays, it also brings an additional advantage, which enables the circuit to operate at a higher clock frequency.

Pipelining effectively removes glitches from combinatorial logic, thereby reducing the power of combinatorial logic. However, for designs that are not prone to glitches, do not add pipelining flip-flops as they will increase power and occupy more resources.

4. State Machine Encoding

Table 3-3 State Machine Encoding Methods

State	**Binary Code**	**One-hot Code**	**Grey Code**
S0	000	00000001	000
S1	001	00000010	001
S2	010	00000100	011
S3	011	00001000	010
S4	100	00010000	110
S5	101	00100000	111
S6	110	01000000	101
S7	111	10000000	100
Total number of transitions	11	16	8
Max. number of transitions per clock cycle	3	2	1
Clock load	3	8	3

Use grey code to reduce signal transitions, eliminate glitches, reduce clock load, and decrease power. Users can change the encoding method in the Project Settings of PDS, as shown in Table 3-3, For descriptions of these encoding methods, refer to "***ADS_Synthesis_User_Guide***" in the PDS software installation directory.

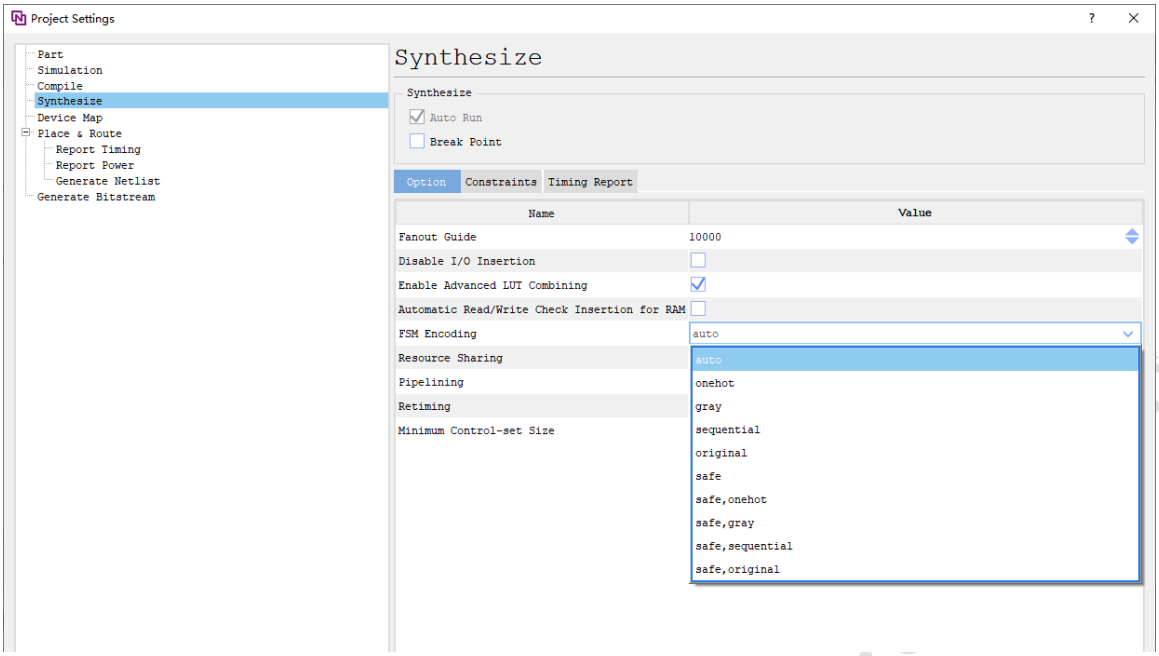

Figure 3-2 State Machine Encoding

5. Reduce Control Sets and Asynchronous Control Signals

Control sets include clock (CLK), clock enable (CE), local reset/set (RS), and distributed RAM write enable (WE). Different control sets cannot be placed into the same CLM. When there are too many control sets in the project, it will prevent the placement of related logic nearby,which will increase routing arcs, thereby increasing power.

Additionally, please think twice before performing reset operations; for example, control path logic may require a reset to ensure proper operation, while data path logic typically does not need a reset in order to reduce fanout and routing resources, facilitate timing closure, and reduce power.

6. Reduce Routing Power

There are two ways to reduce routing power:

1) Use multi-thread routing to reduce Routing Arc Length.

The software with a version of PDS_2023.1 and above supports multi-thread routing for PG2L100H. The multi-thread routing function is enabled by default and does not need additional operations by users. Search "Used SRB routingarc" in "./place_route/run_route_optimize.log" to find "Routing Arc Length".

2) Use routing multiplexed parameters.

Increase the routing multiplexed parameter to increase the multiplexing rate of the routing arc, reduce the routing arc, and thus reduce power, at the expense of timing deterioration. Usage method: In the same directory as the *.pds file, create a new testparam.txt file, and write parameter rt_delay_estimate_coef_double with a default value of 2.0 and a parameter range of [1.0, 5.0], as shown in Figure 3-3. Too large or small parameter values will increase the software runtime. Software version requirement: PDS_2022.2 and above.

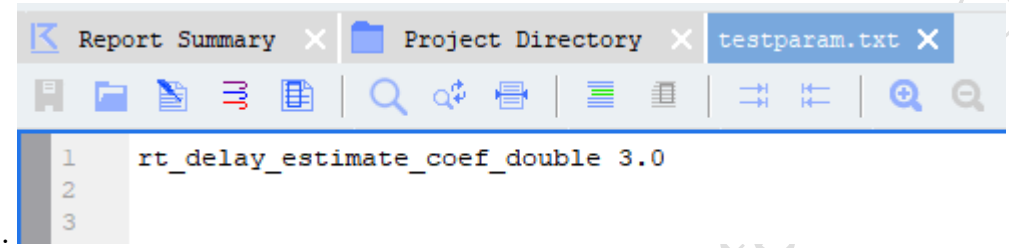

Figure 3-3 Example of The testparam Parameter

7. Architecture Optimisation

When designing, utilise the structural features of FPGA devices to optimise the design's power. These devices include DRM (Dedicated RAM Module) and APM (Arithmetic Process Module). DRM provides abundant on-chip RAM resources for the Logos2 family products, and APM provides efficient digital signal processing capabilities for Logos2 family products. Compared to CLM logic units, these specific structural modules can reduce power.

8. I/O Power Optimisation

For IO standard interfaces like LVTTL and LVCMOS that have no termination matching resistor, the voltage difference between the high level and low level of the output logic is equal to the supply voltage value of VCCIO. The static power of such IO standard interfaces is very low, while the dynamic power driven by the IO interface can be calculated as per the following formula: $P = 0.5 \times f \times c \times VCCIO^2$, where f is the signal output frequency, c is the load capacitance during level conversion, and VCCIO is the IO supply voltage. Since power P is related to VCCIO by a square relationship, the IO standard interfaces with lower levels have significantly lower dynamic power. The above formula shows that the power of LVCMOS and LVTTL IO interfaces mainly depends on load capacitance, frequency, and voltage. Choose the minimum slew/standard/drive that meets the rate and waveform requirements to minimize power.

For IO standard interfaces like SSTL and HSTL with termination matching resistors, the voltage swing of the output signal is very small based on the bias point. Similarly, the formula is: $P = 0.5 \times f \times c \times V^2$, where V is the output signal voltage swing value. Compared to IO standard interfaces without termination matching resistors, the V value is much smaller than the VCCIO value, which means significantly lower dynamic power. However, IO standard interfaces with termination matching resistors consume higher static power, as there is a continuous current passing through the matching resistor in IO.

It can be seen from the above that for high-frequency signals, the IO standard interfaces with termination matching resistors have lower dynamic power. When using IO standard interfaces with termination matching resistors, choose the minimum IO drive settings that meet the rate and waveform requirements can minimize the power of the IO interfaces.

9. Reduce Bank Usage

Reducing the use of FPGA Banks can lower power. Except for the Banks where the multiplexed configuration signals exist, the VCCIO pins of unused Banks can be left floating. When the Banks that contain multiplexed configuration signals are not in use, apply an appropriate voltage to their VCCIO. Refer to "***UG040012_Logos2 Board Hardware Design User Guide***" for details.

10. Reduce HSSTLP Power

When the HSSTLP module is not in use, handle the HSSTLP power supply in accordance with "***UG040012_Logos2 Board Hardware Design User Guide***" for details.

When the Channel is not in use, it can be disabled in the IPC interface, as shown in Figure 3-4.

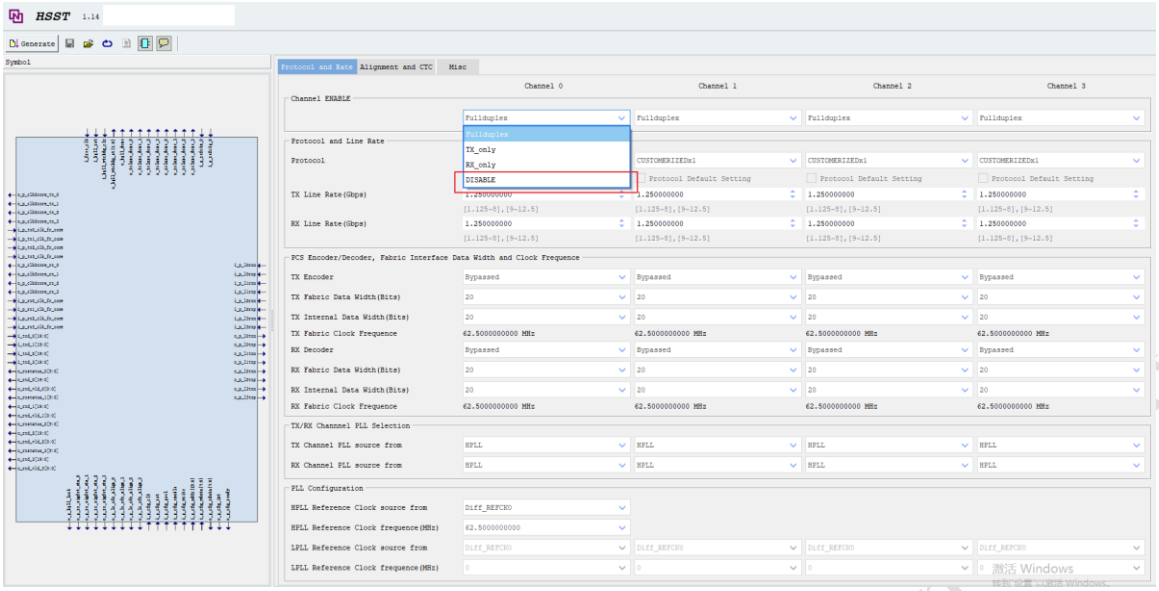

Figure 3-4 Disable Channel

By reducing the TX Swing, power can be reduced at the cost of weakened drive strength. It is recommended to estimate power with PPP. It is recommended to control the TX output swing through configuring registers. For details, refer to "***AN04004_Logos2 Family FPGAs HSSTLP Common Functions Application Guide***".

11. Reduce DDR Power

Configure registers through the APB interface to switch DDR3 SDRAM between Power Down, Self-Refresh, MRS, and Normal states, as shown in Figure 3-5. For the definitions and addresses of registers, refer to "***UG042003_Logos2_HMIC_S IP User Guide***".

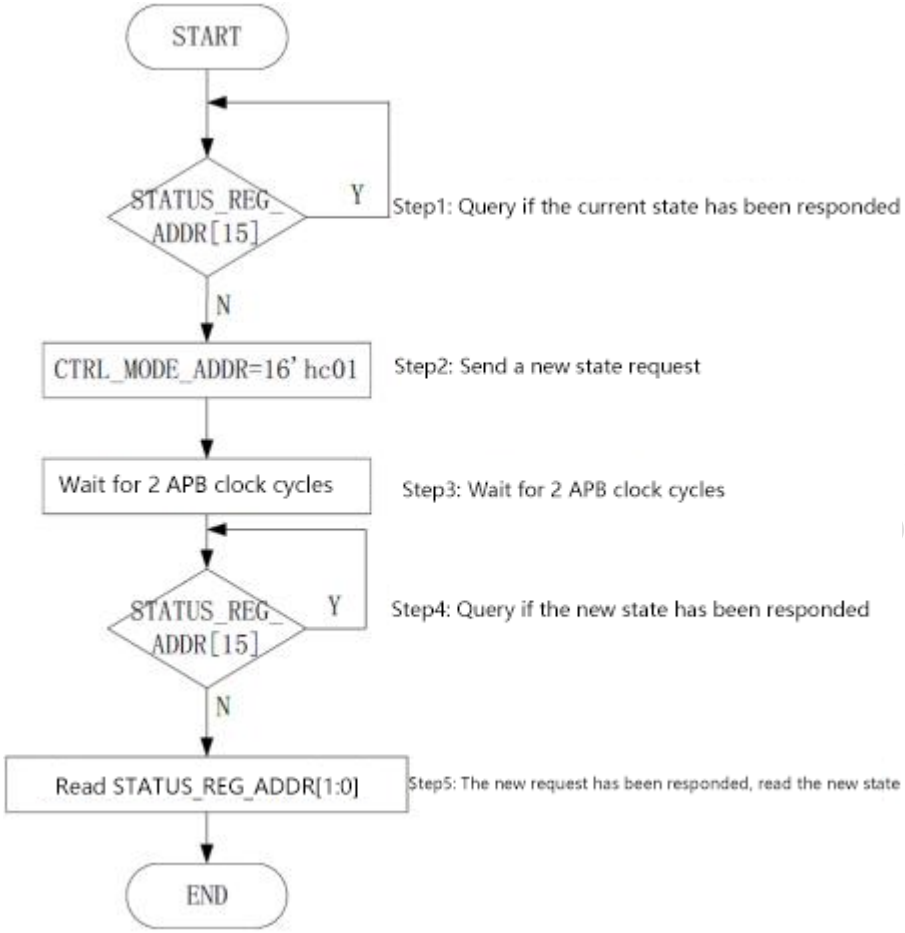

Figure 3-5 Status Switching Request Flowchart

Use Bus-Invert encoding to reduce the number of toggles, lowering power. Additionally, under the premise of meeting system performance requirements, reducing the DDR data rate can also reduce power.

12. Reduce PLL Power

The VCO power accounts for 80%–90% of PLL power, while the number of output clocks has little impact on the PLL power. Therefore, the key to reducing PLL power lies in merging clocks to reduce the number of PLLs and lower the VCO frequency.

The following example illustrates different PLL power values under similar frequencies but different VCO frequencies.

Taking the PG2L100H device's GPLL as an example:

gpll0 u_gpll0 (// VCO = 650M

```
clkout0(clk_ 100m),

clkout1(clk_65m),

lock( ),

clkin1(clk_25m)

);

gpll2    u_gpll2 (      // VCO = 1187.5M

clkout0(clk_ 100m),

clkout1(clk_66m),

lock( ),

clkin1(clk_25m)

);
```

Use the Power Planner to estimate the dynamic power of gpll0 and gpll2, which are 0.051W and 0.085W respectively. According to the PG2L100H device datasheet, the VCO range of GPLL is 600M–1200M. The output frequencies are similar, but the power difference is 0.034W.

Considering the power differences due to VCO frequencies, users need to reasonably plan the clock frequencies based on VCO frequencies.

The VCO frequencies are shown under "Show Internal Settings of PLL" in the IPC interface, as shown in Figure 3-6.

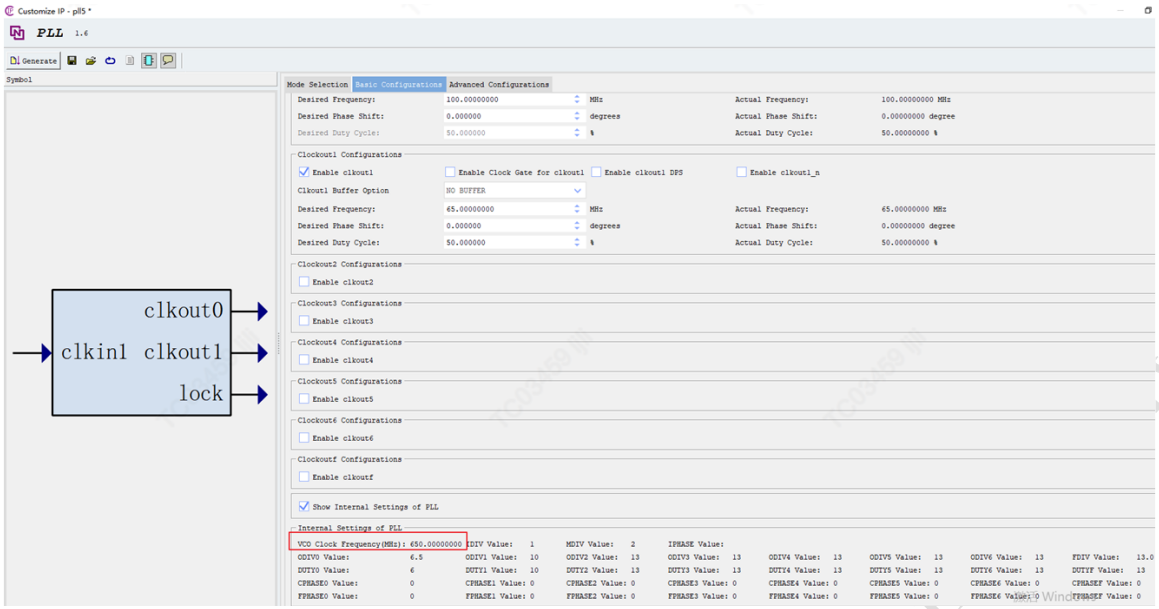

Figure 3-6 PLL VCO Frequency

13. Set Preserve to Disable the Column Clocks of CKEBs

In the PG2L100H clock architecture, CKEBs provide clocks for two columns of logic (CLM/DRM/APM, etc.).

The column logic driven by CKEBs does not use all resources, and the unused FFs also consume power, which is consistent with competitive products. Therefore, to reduce power, reduce the power of the additional unused FFs driven by the column logic of CKEBs. Through reasonable Preserve settings, users can shut down some CKEBs, and improve the utilization of the column logic driven by other CKEBs to reduce the power of additional unused FFs driven by the column logic of CKEBs.

Currently, a device (CLM/DRM/APM, etc.) is placed within the driving range of any CKEB, and the software will enable this CKEB. If no device is placed within the driving range of a CKEB, the software will shut down that CKEB.

Preserve constraint example:

define_global_attribute {PAP_SITE_PRESERVE} {region2;region1;region3;region4;}

define_global_attribute {PAP_REGION} {region1(4,63,175,199)[CLMA,CLMS,DRM,APM];region2(4,63,0,24)[CLMA,CLMS,DRM,APM];region3(4,25,100,149)[DRM,APM,CLMA,CLMS];region4(66,107,175,199)[DRM,APM,CLMA,

CLMS];}

The settings of Preserve regions are related to the user's project IO, DRM, and data streams. Set Preserve for the top left, middle left, and bottom left parts to reduce the phenomenon that only a few designs exist within the driving range of a single CKEB, and perform iteration adjustment according to the routing arc length, as shown in Figure 3-7.

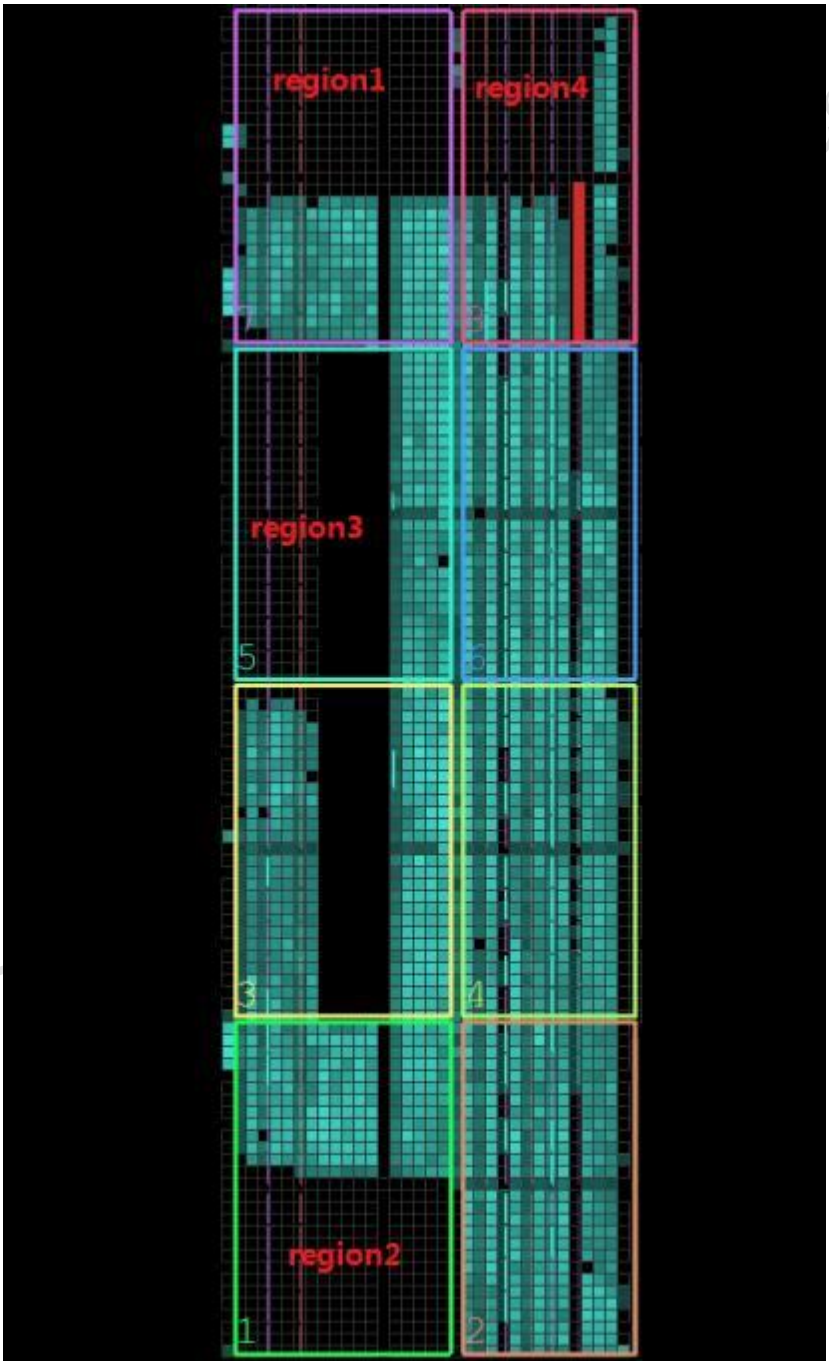

Figure 3-7 DE after Preserve Settings

14. ADC Power

In typical application scenarios, the ADC consumes little power.

If the ADC is not used, for the VCCADC power supply handling method during designing board, refer to "***UG040009_Logos2 Family FPGAs Analog-to-Digital Converter (ADC) Module User Guide***".

Disclaimer

Copyright Notice

Disclaimer

1. This document only provides information in stages and may be updated at any time based on the actual situation of the products without further notice. The Company assumes no legal responsibility for any direct or indirect losses caused by improper use of this document.
2. This document is provided "as is" without any warranties, including but not limited to warranties of merchantability, fitness for a particular purpose, non-infringement, or any other warranties mentioned in proposals, specifications, or samples. This document does not grant any explicit or implied intellectual property usage license, whether by estoppel or otherwise.
3. The Company reserves the right to modify any documents related to its series products at any time without prior notice.
4. The information contained in this document is intended to assist users in resolving application-related issues. While we strive for accuracy, we cannot guarantee that the document is entirely free from flaws. Should any functional abnormalities and performance degradation arise due to deviation from the prescribed procedures outlined herein, our company will neither be held liable nor concede that such issues stem from product deficiencies. The solutions presented in this document are just one of the feasible options and cannot cover all application scenarios. Consequently, if users encounter functional abnormalities or performance degradation despite adhering to the prescribed procedures outlined herein, we cannot assure that such issues are indicative of product deficiencies.