

Logos2 Family Product GTPs User Guide

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.2	19.07.2023	Initial release.

Note: LOGOS2 currently does not support HPIO. The newly added GTPs for the HPIO parameter are only for compatibility with other families of devices, and the HPIO parameter can only be set in other devices that support HPIO.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
GTP	Generic Technology Primitive
FPGA	Field Programmable Gate Array
DRM	Dedicated RAM Module
HSST	High Speed Serial Transceiver
APM	Arithmetic Process Module
SRB	Signal Relay Block
ADC	Analog to Digital Converter
HRIO	High range IO
HPIO	High performance IO

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Chapter 1 GTP Classification

GTP (Generic Technology Primitive) refer to the names of a series of general modules developed based on the features of our company's devices. They serve as the basic units on the chip, representing the actual hardware logic elements that the FPGA possesses, such as LUT, DFF, DRAM and more.

In this section, the GTP primitives described in this article are classified into nine categories according to their functions: flip-flops, latches, LUT-related GTPs, ROM and RAM-related GTPs, IO-related GTPs, clock-related GTPs, configuration-related GTPs, DDR-related GTPs, and others. See the table below for the specific classification.

The support status, ports, parameters, instantiation templates, and other information of GTP primitives should be based on the corresponding version of the PDS software.

Table 1-1 Logos2 Family GTP Classification

GTP Name	GTP Description
Flip-flop	
GTP_DFF	Flip-flop
GTP_DFF_C	Asynchronous clear flip-flop
GTP_DFF_E	Flip-flop with enable
GTP_DFF_CE	Asynchronous clear flip-flop with enable
GTP_DFF_P	Asynchronous set flip-flop
GTP_DFF_PE	Asynchronous set flip-flop with enable
GTP_DFF_R	Synchronous clear flip-flop
GTP_DFF_RE	Synchronous clear flip-flop with enable
GTP_DFF_S	Synchronous set flip-flop
GTP_DFF_SE	Synchronous set flip-flop with enable
Latch	
GTP_DLATCH	Latch
GTP_DLATCH_E	Latch with enable
GTP_DLATCH_C	Asynchronous clear latch
GTP_DLATCH_CE	Asynchronous clear latch with enable
GTP_DLATCH_P	Asynchronous set latch
GTP_DLATCH_PE	Asynchronous set latch with enable
LUT-related	
GTP_ONE	GTP_ONE outputs a high level signal
GTP_ZERO	GTP_ZERO outputs a low level signal
GTP_BUF	General-purpose 1bit BUF

GTP Name	GTP Description
GTP_INV	Inverter
GTP_LUT1	1-input LUT
GTP_LUT2	2-input LUT
GTP_LUT3	3-input LUT
GTP_LUT4	4-input LUT
GTP_LUT5	5-input LUT
GTP_LUT6	6-input LUT
GTP_LUT7	7-input LUT
GTP_LUT8	8-input LUT
GTP_LUT6CARRY	6-input LUT with carry chain
GTP_LUT6D	6-input LUT with 2 output ports
GTP_MUX2LUT7	GTP_LUT7 dedicated 2-input selector
GTP_MUX2LUT8	GTP_LUT8 dedicated 2-input selector
ROM and RAM-related	
GTP_ROM32X1	ROM with a 32-bit address depth and 1-bit data
GTP_ROM32X2	ROM with a 32-bit address depth and 2-bit data
GTP_ROM64X1	ROM with a 64-bit address depth and 1-bit data
GTP_ROM128X1	ROM with a 128-bit address depth and 1-bit data
GTP_ROM256X1	ROM with a 256-bit address depth and 1-bit data
GTP_RAM32X1SP	Single-port RAM with a 32-bit address depth and 1-bit data
GTP_RAM32X1DP	Simple dual-port RAM with a 32-bit address depth and 1-bit data
GTP_RAM32X2SP	Single-port RAM with a 32-bit address depth and 2-bit data
GTP_RAM32X2DP	Simple dual-port RAM with a 32-bit address depth and 2-bit data
GTP_RAM64X1SP	Single-port RAM with a 64-bit address depth and 1-bit data
GTP_RAM64X1DP	Simple dual-port RAM with a 64-bit address depth and 1-bit data
GTP_RAM128X1SP	Single port RAM with a 128-bit address depth and 1-bit data
GTP_RAM128X1DP	Simple dual-port RAM with a 128-bit address depth and 1-bit data
GTP_RAM256X1SP	Single-port RAM with a 256-bit address depth and 1-bit data
GTP_DRM36K_E1	36K bits dedicated RAM module (DRM)
GTP_DRM18K_E1	18K bits dedicated RAM module (DRM)
GTP_FIFO36K_E1	36K bits FIFO
GTP_FIFO18K_E1	18K bits FIFO
IO-related	
GTP_INBUF	Single-ended input BUFFER
GTP_INBUFG	Single-ended input clock BUFFER
GTP_INBUFDS	Differential input BUFFER
GTP_INBUFGDS	Differential input clock BUFFER
GTP_INBUFE	Single-ended input BUFFER with enable end
GTP_INBUFEDS	Differential input BUFFER with enable end

GTP Name	GTP Description
GTP_OUTBUF	Single-ended output BUFFER
GTP_OUTBUFT	Tri-state output BUFFER
GTP_OUTBUFDS	True differential output BUFFER
GTP_OUTBUFTDS	Tri-state true differential output BUFFER
GTP_OUTBUFCO	Pseudo-differential output BUFFER
GTP_OUTBUFTCO	Tri-state pseudo-differential output BUFFER
GTP_Iobuf	Bidirectional BUFFER
GTP_Iobufco	Bidirectional pseudo-differential BUFFER
GTP_Iobufds	Bidirectional true differential BUFFER
GTP_Iobufe	Bidirectional BUFFER with enable end
GTP_Iobufeco	Bidirectional pseudo-differential BUFFER with enable end
GTP_Iobufeds	Bidirectional true differential BUFFER with enable end
GTP_ISERDES_E2	Input data processing module
GTP_OSERDES_E2	Data output conversion module
GTP_Iodelay_E2	Data delay unit, supporting dynamic or static delay control
GTP_ZeroHoldDelay	Data delay unit, supporting static delay control
GTP_Iobufco_E1	Bidirectional pseudo-differential BUFFER
GTP_OUTBUFCO_E1	Pseudo-differential output BUFFER
GTP_OUTBUFTCO_E1	Tri-state pseudo-differential output BUFFER
GTP_INBUFDS_E1	Differential input BUFFER
GTP_INBUFEDS_E1	Differential input BUFFER with enable end
Clock-related	
GTP_CLKBUFG	Global clock BUFFER
GTP_CLKBUFGCE	Global clock BUFFER with port enabled
GTP_CLKBUFGMUX	Support switching between two global clock inputs
GTP_CLKBUFR	Regional clock BUFFER
GTP_IOCLKBUF	IO clock BUFFER
GTP_Ioclkdiv_E2	Clock divide GTP
GTP_CLKBUFMCE	Multi-region (vertical) clock buffer with enable end
GTP_CLKBUFM	Multi-region (vertical) clock buffer
GTP_CLKBUFXCE	Multi-region (horizontal) clock buffer with enable end
GTP_CLKBUFX	Multi-region (horizontal) clock buffer
GTP_DLL	Phase locked loop primitive
GTP_PPLL	Phase locked loop primitive
GTP_DLL_E2	Dynamically lock the frequency of the input reference clock and output an equivalent number of delay steps
GTP_OSC_E4	Output a fixed 50MHz clock to CCS as the system clock
Configuration-related	
GTP_EFUSECODE	This GTP is used to read EFUSECODE and outputs 32-bit data stored in efuse to the user in parallel
GTP_IPAL_E2	Used for CRC checking or SEU checking of readback data

GTP Name	GTP Description
GTP_SCANCHAIN_E1	Read the values of user data registers through the JTAG interface
GTP_UDID	This GTP is used to read UDID CODE values
GTP_JTAGIF	Enable JTAG Interface function for users
GTP_KEYRAM	Clear internal memory
GTP_CFGCLK	This GTP enables the FLASH clock sent to CCS by SRB
DDR-related	
GTP_IOCLKDIV_E3	Divide the clock input from the PLL IOCLK clock tree to generate the system clock for DDRPHY
GTP_CLKPD	Detect the phase difference between the MEMORY CONTROLLER soft core clock and the DDR_PHY system clock, and output the FLAG_PD signal to SRB
GTP_DDC_E2	Generate the write clock for DDR memory
GTP_IDDR_E1	Data deserializer
GTP_ODDR_E1	Parallel-to-serial data processing module
Other	
GTP_APM_E2	Arithmetic logic unit
GTP_GRS	This GTP is used to control the global reset signal
GTP_START_E1	This GTP describes the process of releasing the global signal for the wake-up operation
GTP_ADC_E2	Used to implement ADC functions
GTP_PCIEGEN2	High-speed serial interface module compatible with PCIE2.1 protocol
GTP_HSSTLP_LANE	1-4 full-duplex transmit and receive LANEs supported by each HSSTLP (High-Speed Serial Transceiver)
GTP_HSSTLP_PLL	GTP_HSSTLP_PLL is the dedicated pll module for HSSTLP (High-Speed Serial Transceiver)

Chapter 2 Usage Instructions for Trigger GTPs

2.1 GTP_DFF

2.1.1 Supported Devices

Table 2-1 GTP_DFF-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

2.1.2 Description of Functionality

GTP_DFF is a D flip-flop with a data input D and a data output Q. It is triggered on the rising edge of the clock, transferring the input signal to the output.

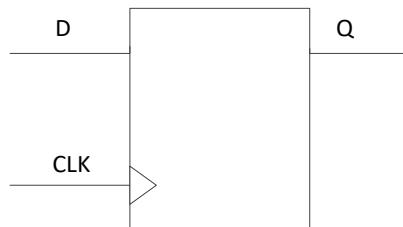


Figure 2-1 GTP_DFF

2.1.3 Port Description

Table 2-2 GTP_DFF Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger

2.1.4 Parameter Description

Table 2-3 GTP_DFF Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	"TRUE", "FALSE"	"TRUE"	Global reset signal enable
INIT	<binary>	1'b0, 1'b1	1'b0	Initial value, asynchronously triggered by the global reset signal when GRS_EN = "TRUE"

2.1.5 Instantiation Template

```
GTP_DFF #(
    .GRS_EN("TRUE"),
    .INIT(1'b0)
) GTP_DFF_inst (
    .Q  (qout),
    .CLK(clk),
    .D  (d)
);
```

2.2 GTP_DFF_C

2.2.1 Supported Devices

Table 2-4 GTP_DFF_C-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

2.2.2 Description of Functionality

GTP_DFF_C is a D flip-flop with a data input D and a data output Q. It is triggered on the rising edge of the clock, transferring the input signal to the output. Asynchronous clear.

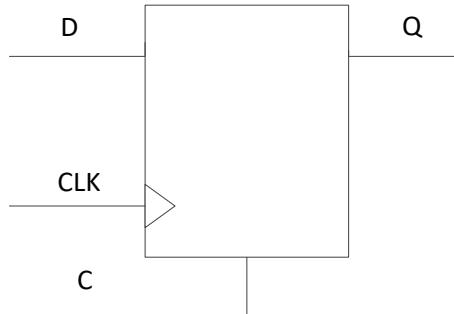


Figure 2-2 GTP_DFF_C

2.2.3 Port Description

Table 2-5 GTP_DFF_C Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger
C	Input	Asynchronous clear signal

2.2.4 Parameter Description

Table 2-6 GTP_DFF_C Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	"TRUE", "FALSE"	"TRUE"	Global reset signal enable
INIT	<binary>	1'b0, 1'b1	1'b0	Initial value, asynchronously triggered by the global reset signal when GRS_EN = "TRUE"

2.2.5 Instantiation Template

```
GTP_DFF_C #(  
    .GRS_EN("TRUE"),  
    .INIT(1'b0)  
) GTP_DFF_C_inst (  
    .Q(qout),  
    .C(clear),  
    .CLK(clk),  
    .D(d)  
);
```

2.3 GTP_DFF_E

2.3.1 Supported Devices

Table 2-7 GTP_DFF_E-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

2.3.2 Description of Functionality

GTP_DFF_E is a D flip-flop with a data input D and a data output Q. It is triggered on the rising edge of the clock, transferring the input signal to the output when CE is high.

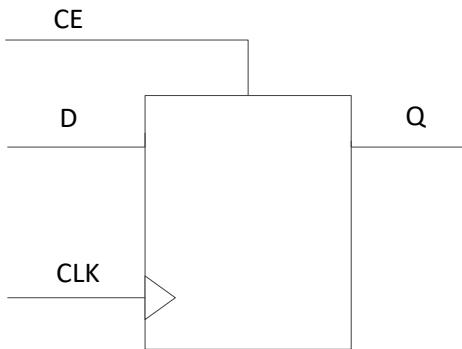


Figure 2-3 GTP_DFF_E

2.3.3 Port Description

Table 2-8 GTP_DFF_E Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger
CE	Input	Active-high enable signal

2.3.4 Parameter Description

Table 2-9 GTP_DFF_E Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	"TRUE", "FALSE"	"TRUE"	Global reset signal enable
INIT	<binary>	1'b0, 1'b1	1'b0	Initial value, asynchronously triggered by the global reset signal when GRS_EN = "TRUE"

2.3.5 Instantiation Template

```
GTP_DFF_E #(
    .GRS_EN("TRUE"),
    .INIT(1'b0),
    ) GTP_DFF_E_inst (
        .Q(q),
        .CE(ce),
        .CLK(clk),
        .D(d)
    );
```

2.4 GTP_DFF_CE

2.4.1 Supported Devices

Table 2-10 GTP_DFF_CE-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

2.4.2 Description of Functionality

GTP_DFF_CE is a D flip-flop with a data input D and a data output Q. It is triggered on the rising edge of the clock, transferring the input signal to the output when CE is high. Asynchronous clear.

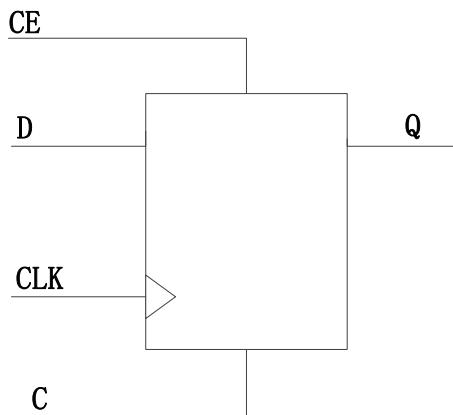


Figure 2-4 GTP_DFF_CE

2.4.3 Port Description

Table 2-11 GTP_DFF_CE Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger
C	Input	Asynchronous clear signal
CE	Input	Active-high enable signal

2.4.4 Parameter Description

Table 2-12 GTP_DFF_CE Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	"TRUE", "FALSE"	"TRUE"	Global reset signal enable
INIT	<binary>	1'b0, 1'b1	1'b0	Initial value, asynchronously triggered by the global reset signal when GRS_EN = "TRUE"

2.4.5 Instantiation Template

```
GTP_DFF_CE #(
    .GRS_EN("TRUE"),
    .INIT(1'b0)
) GTP_DFF_CE_inst (
    .Q      (q  ),
    .C      (c  ),
    .CE     (ce ),
    .CLK    (clk),
    .D      (d  )
);
```

2.5 GTP_DFF_P

2.5.1 Supported Devices

Table 2-13 GTP_DFF_P-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

2.5.2 Description of Functionality

GTP_DFF_P is a D flip-flop with a data input D and a data output Q. It is triggered on the rising edge of the clock, transferring the input signal to the output. It is asynchronously set.

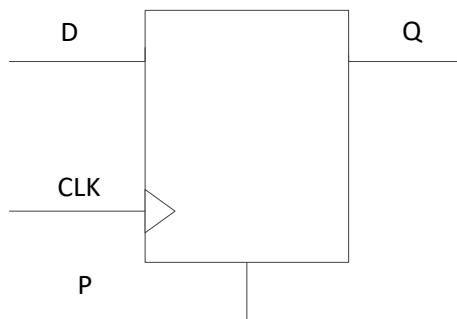


Figure 2-5 GTP_DFF_P

2.5.3 Port Description

Table 2-14 GTP_DFF_P Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger
P	Input	Asynchronous set signal

2.5.4 Parameter Description

Table 2-15 GTP_DFF_P Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	"TRUE", "FALSE"	"TRUE"	Global reset signal enable
INIT	<binary>	1'b0, 1'b1	1'b1	Initial value, asynchronously triggered by the global reset signal when GRS_EN = "TRUE"

2.5.5 Instantiation Template

```
GTP_DFF_P #(
    .GRS_EN("TRUE"),
    .INIT(1'b1),
    ) GTP_DFF_P_inst (
        .Q(q),
        .CLK(clk),
        .D(d),
        .P(p)
    );
```

2.6 GTP_DFF_PE

2.6.1 Supported Devices

Table 2-16 GTP_DFF_PE-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

2.6.2 Description of Functionality

GTP_DFF_PE is a D flip-flop with a data input D and a data output Q. It is triggered on the rising edge of the clock when the CE is high, transferring the input signal to the output. It is asynchronously set.

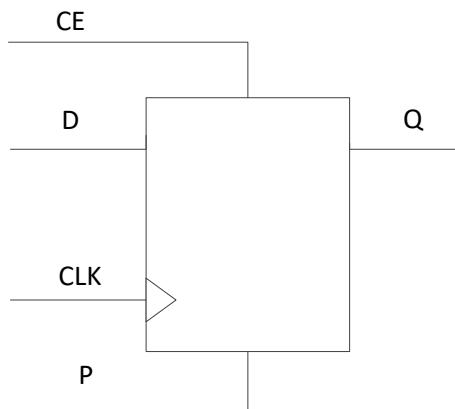


Figure 2-6 GTP_DFF_PE

2.6.3 Port Description

Table 2-17 GTP_DFF_PE Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger
P	Input	Asynchronous set signal
CE	Input	Active-high enable signal

2.6.4 Parameter Description

Table 2-18 GTP_DFF_PE Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	"TRUE", "FALSE"	"TRUE"	Global reset signal enable
INIT	<binary>	1'b0, 1'b1	1'b1	Initial value, asynchronously triggered by the global reset signal when GRS_EN = "TRUE"

2.6.5 Instantiation Template

```
GTP_DFF_PE #(
    .GRS_EN("TRUE"),
    .INIT(1'b1)
) GTP_DFF_PE_inst (
    .Q(q),
    .CE(ce),
    .CLK(clk),
    .D(d),
    .P(p)
);
```

2.7 GTP_DFF_R

2.7.1 Supported Devices

Table 2-19 GTP_DFF_R-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

2.7.2 Description of Functionality

GTP_DFF_R is a D flip-flop with a data input D and a data output Q. It is triggered on the rising edge of the clock, transferring the input signal to the output. Synchronous clear.

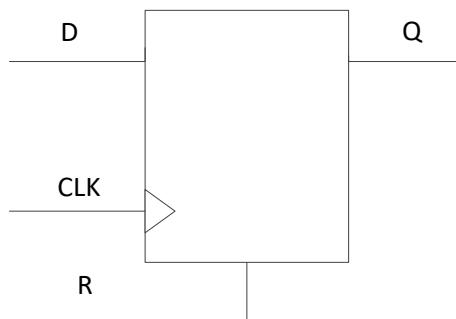


Figure 2-7 GTP_DFF_R

2.7.3 Port Description

Table 2-20 GTP_DFF_R Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger
R	Input	Synchronization clear signal

2.7.4 Parameter Description

Table 2-21 GTP_DFF_R Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	"TRUE", "FALSE"	"TRUE"	Global reset signal enable
INIT	<binary>	1'b0, 1'b1	1'b0	Initial value, asynchronously triggered by the global reset signal when GRS_EN = "TRUE"

2.7.5 Instantiation Template

```
GTP_DFF_R #(
    .GRS_EN("TRUE"),
    .INIT(1'b0)
) GTP_DFF_R_inst (
    .Q(q),
    .CLK(clk),
    .D(d),
    .R(r)
);
```

2.8 GTP_DFF_RE

2.8.1 Supported Devices

Table 2-22 GTP_DFF_RE-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

2.8.2 Description of Functionality

GTP_DFF_RE is a D flip-flop with a data input D and a data output Q. It is triggered on the rising edge of the clock when the CE is high, transferring the input signal to the output. Synchronous clear.

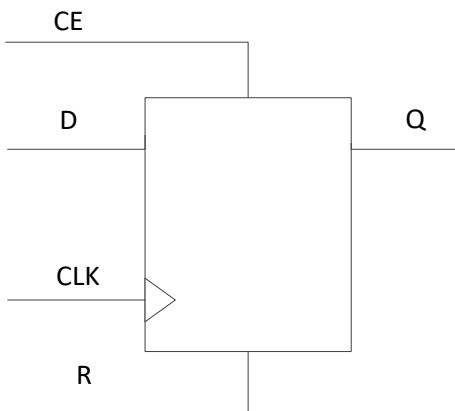


Figure 2-8 GTP_DFF_RE

2.8.3 Port Description

Table 2-23 GTP_DFF_RE Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger
R	Input	Synchronization clear signal
CE	Input	Active-high enable signal

2.8.4 Parameter Description

Table 2-24 GTP_DFF_RE Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	"TRUE", "FALSE"	"TRUE"	Global reset signal enable
INIT	<binary>	1'b0, 1'b1	1'b0	Initial value, asynchronously triggered by the global reset signal when GRS_EN = "TRUE"

2.8.5 Instantiation Template

```
GTP_DFF_RE #(  
    .GRS_EN("TRUE"),  
    .INIT(1'b0)  
) GTP_DFF_RE_inst (  
    .Q(q),  
    .CE(ce),  
    .CLK(clk),  
    .D(d),  
    .R(r)  
);
```

2.9 GTP_DFF_S

2.9.1 Supported Devices

Table 2-25 GTP_DFF_S-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

2.9.2 Description of Functionality

GTP_DFF_S is a D flip-flop with a data input D and a data output Q. It is triggered on the rising edge of the clock, transferring the input signal to the output. Synchronously set.

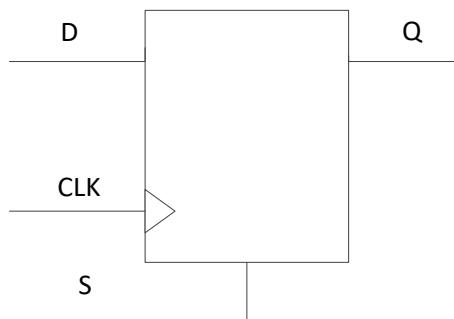


Figure 2-9 GTP_DFF_S

2.9.3 Port Description

Table 2-26 GTP_DFF_S Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger
S	Input	Synchronization set signal

2.9.4 Parameter Description

Table 2-27 GTP_DFF_S Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	"TRUE", "FALSE"	"TRUE"	Global reset signal enable
INIT	<binary>	1'b0, 1'b1	1'b1	Initial value, asynchronously triggered by the global reset signal when GRS_EN = "TRUE"

2.9.5 Instantiation Template

```
GTP_DFF_S #(
    .GRS_EN("TRUE"),
    .INIT(1'b1),
    ) GTP_DFF_S_inst (
        .Q(q),
        .CLK(clk),
        .D(d),
        .S(s)
    );
```

2.10 GTP_DFF_SE

2.10.1 Supported Devices

Table 2-28 GTP_DFF_SE-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

2.10.2 Description of Functionality

GTP_DFF_SE is a D flip-flop with a data input D and a data output Q. It is triggered on the rising edge of the clock, transferring the input signal to the output when CE is high. Synchronously set.

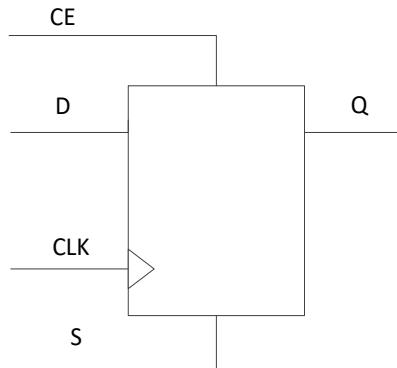


Figure 2-10 GTP_DFF_SE

2.10.3 Port Description

Table 2-29 GTP_DFF_SE Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger
S	Input	Synchronization set signal
CE	Input	Active-high enable signal

2.10.4 Parameter Description

Table 2-30 GTP_DFF_SE Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	"TRUE", "FALSE"	"TRUE"	Global reset signal enable
INIT	<binary>	1'b0, 1'b1	1'b1	Initial value, asynchronously triggered by the global reset signal when GRS_EN = "TRUE"

2.10.5 Instantiation Template

```
GTP_DFF_SE #(  
    .GRS_EN("TRUE"),  
    .INIT(1'b1)  
) GTP_DFF_SE_inst (  
    .Q(q),  
    .CE(ce),  
    .CLK(clk),  
    .D(d),  
    .S(s)  
);
```

Chapter 3 Usage Instructions for Latch GTPs

3.1 GTP_DLATCH

3.1.1 Supported Devices

Table 3-1 GTP_DLATCH-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

3.1.2 Description of Functionality

GTP_DLATCH is a latch with D as data input and Q as data output. It can send the input signal to the output when G is high.

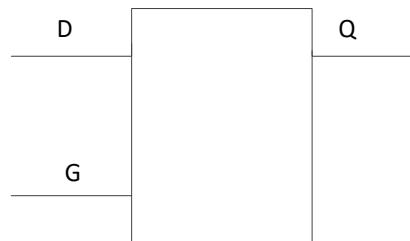


Figure 3-1 GTP_DLATCH Diagram

3.1.3 Port Description

Table 3-2 GTP_DLATCH Port List

Port	Direction	Function Description
G	Input	Level input
D	Input	Latch input signal
Q	Output	Latch output signal

3.1.4 Parameter Description

Table 3-3 GTP_DLATCH Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	"TRUE", "FALSE"	"TRUE"	Global reset signal enable
INIT	<binary>	1'b0, 1'b1	1'b0	Initial value, asynchronously triggered by the global reset signal when GRS_EN = "TRUE"

3.1.5 Instantiation Template

```
GTP_DLATCH#(
    .INIT(1'b0),
    .GRS_EN("TURE")//"TURE"; "FALSE"
)
GTP_DLATCH_inst (
    .Q(q),
    .D(d),
    .G(g)
);
```

3.2 GTP_DLATCH_E

3.2.1 Supported Devices

Table 3-4 GTP_DLATCH_E-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

3.2.2 Description of Functionality

GTP_DLATCH_E is a latch with a data input D and a data output Q, transmitting the input signal to the output when G and GE are both high.

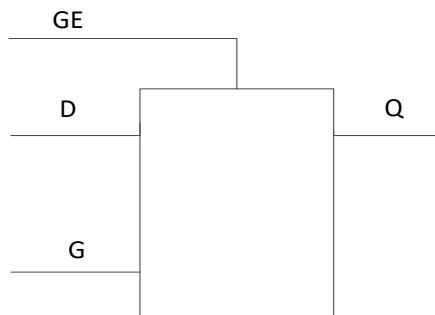


Figure 3-2 GTP_DLATCH_E Diagram

3.2.3 Port Description

Table 3-5 GTP_DLATCH_E Port List

Port	Direction	Function Description
G	Input	Input level
D	Input	Latch input signal
Q	Output	Latch output signal
GE	Input	Active-high enable signal

3.2.4 Parameter Description

Table 3-6 GTP_DLATCH_E Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	"TRUE", "FALSE"	"TRUE"	Global reset signal enable
INIT	<binary>	1'b0, 1'b1	1'b0	Initial value, asynchronously triggered by the global reset signal when GRS_EN = "TRUE"

3.2.5 Instantiation Template

```
GTP_DLATCH_E#(
    .INIT (1'b0),
    .GRS_EN("TURE")// "TURE"; "FALSE"
)
GTP_DLATCH_E_inst (
    .Q (q),
    .D (d),
    .G (g),
    .GE (en)
);
```

3.3 GTP_DLATCH_C

3.3.1 Supported Devices

Table 3-7 GTP_DLATCH_C-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

3.3.2 Description of Functionality

GTP_DLATCH_C is a latch with a data input D and a data output Q, transmitting the input signal to the output when G is high. Asynchronous clear.

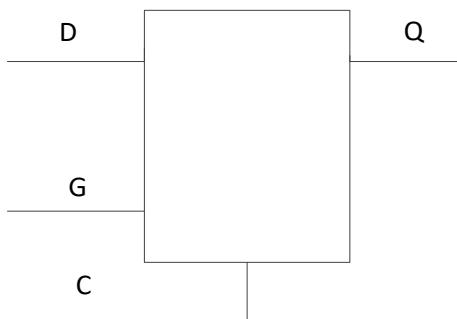


Figure 3-3 GTP_DLATCH_C Diagram

3.3.3 Port Description

Table 3-8 GTP_DLATCH_C Port List

Port	Direction	Function Description
G	Input	Input level
D	Input	Latch input signal
Q	Output	Latch output signal
C	Input	Asynchronous clear signal

3.3.4 Parameter Description

Table 3-9 GTP_DLATCH_C Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	"TRUE", "FALSE"	"TRUE"	Global reset signal enable
INIT	<binary>	1'b0, 1'b1	1'b0	Initial value, asynchronously triggered by the global reset signal when GRS_EN = "TRUE"

3.3.5 Instantiation Template

```

GTP_DLATCH_C#(
    .INIT(1'b0),
    .GRS_EN("TURE")//"TURE"; "FALSE"
)
GTP_DLATCH_C_inst (
    .Q (q),
    .D (d),
    .G (g),
    .C (c)
);

```

3.4 GTP_DLATCH_CE

3.4.1 Supported Devices

Table 3-10 GTP_DLATCH_CE-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

3.4.2 Description of Functionality

GTP_DLATCH_CE is a latch with a data input D and a data output Q, transmitting the input signal to the output when G and GE are both high. Asynchronous clear.

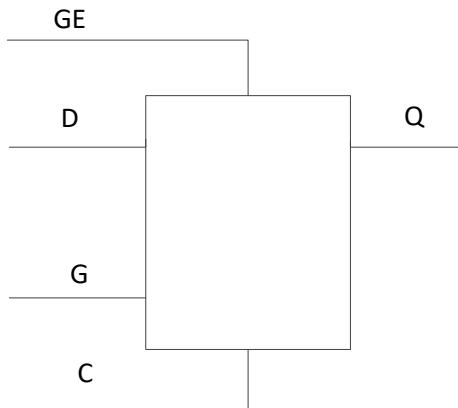


Figure 3-4 GTP_DLATCH_CE Diagram

3.4.3 Port Description

Table 3-11 GTP_DLATCH_CE Port List

Port	Direction	Function Description
G	Input	Input level
D	Input	Latch input signal
Q	Output	Latch output signal
C	Input	Asynchronous clear signal
GE	Input	Active-high enable signal

3.4.4 Parameter Description

Table 3-12 GTP_DLATCH_CE Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	"TRUE", "FALSE"	"TRUE"	Global reset signal enable
INIT	<binary>	1'b0, 1'b1	1'b0	Initial value, asynchronously triggered by the global reset signal when GRS_EN = "TRUE"

3.4.5 Instantiation Template

```
GTP_DLATCH_CE#(
    .INIT(1'b0),
    .GRS_EN("TURE")// "TURE"; "FALSE"
)
GTP_DLATCH_CE_inst (
    .Q (q),
    .D (d),
    .G (g),
    .C (c),
    .GE (ge)
);
```

3.5 GTP_DLATCH_P

3.5.1 Supported Devices

Table 3-13 GTP_DLATCH_P-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

3.5.2 Description of Functionality

GTP_DLATCH_P is a latch with a data input D and a data output Q, transmitting the input signal to the output when G is high. It is asynchronously set.

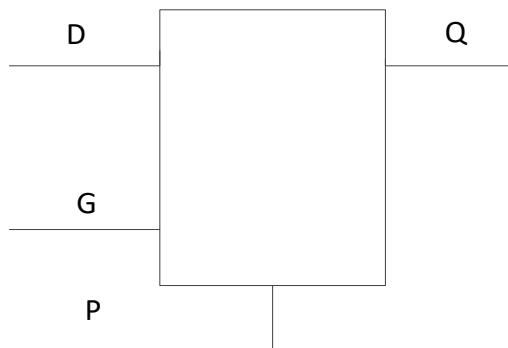


Figure 3-5 GTP_DLATCH_P Diagram

3.5.3 Port Description

Table 3-14 GTP_DLATCH_P Port List

Port	Direction	Function Description
G	Input	Input level
D	Input	Latch input signal
Q	Output	Latch output signal
P	Input	Asynchronous set signal

3.5.4 Parameter Description

Table 3-15 GTP_DLATCH_P Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	"TRUE", "FALSE"	"TRUE"	Global reset signal enable
INIT	<binary>	1'b0, 1'b1	1'b1	Initial value, asynchronously triggered by the global reset signal when GRS_EN = "TRUE"

3.5.5 Instantiation Template

```

GTP_DLATCH_P#(
    .INIT(1'b1),
    .GRS_EN("TURE")//"TURE"; "FALSE"
)
GTP_DLATCH_P_inst (
    .Q (q),
    .D (d),
    .G (g),
    .P (p)
);

```

3.6 GTP_DLATCH_PE

3.6.1 Supported Devices

Table 3-16 GTP_DLATCH_PE-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

3.6.2 Description of Functionality

GTP_DLATCH_PE is a latch with a data input D and a data output Q, transmitting the input signal to the output when G and GE are both high. It is asynchronously set.

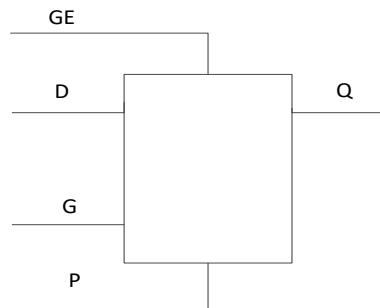


Figure 3-6 GTP_DLATCH_PE Diagram

3.6.3 Port Description

Table 3-17 GTP_DLATCH_PE Port List

Port	Direction	Function Description
G	Input	Input level
D	Input	Latch input signal
Q	Output	Latch output signal
P	Input	Asynchronous set signal
GE	Input	Active-high enable signal

3.6.4 Parameter Description

Table 3-18 GTP_DLATCH_PE Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	"TRUE", "FALSE"	"TRUE"	Global reset signal enable
INIT	<binary>	1'b0, 1'b1	1'b1	Initial value, asynchronously triggered by the global reset signal when GRS_EN = "TRUE"

3.6.5 Instantiation Template

```
GTP_DLATCH_PE#(
    .INIT(1'b1),
    .GRS_EN("TURE")// "TURE"; "FALSE"
)
GTP_DLATCH_PE_inst (
    .Q (q),
    .D (d),
    .G (g),
    .P (p),
    .GE (en)
);
```

Chapter 4 Usage Instructions for LUT-related GTPs

4.1 GTP_ONE

4.1.1 Supported Devices

Table 4-1 GTP_ONE-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

4.1.2 Description of Functionality

GTP_ONE outputs a high level signal. This is shown in the following figure:

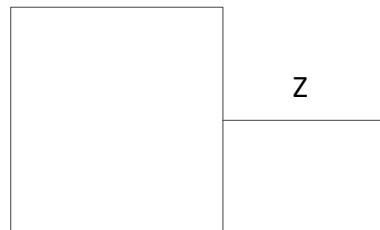


Figure 4-1 GTP_ONE Structure Diagram

4.1.3 Port Description

Table 4-2 GTP_ONE Port List

Port	Direction	Function Description
Z	Output	High-level output

4.1.4 Instantiation Template

```
GTP_ONE GTP_ONE_inst (
    .Z_ (Z)
);
```

4.2 GTP_ZERO

4.2.1 Supported Devices

Table 4-3 GTP_ZERO-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

4.2.2 Description of Functionality

GTP_ZERO outputs a low level signal. The structure is shown below:

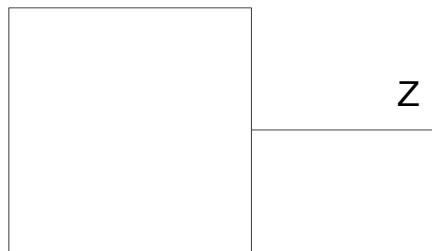


Figure 4-2 GTP_ZERO Structure Diagram

4.2.3 Port Description

Table 4-4 GTP_ZERO Port List

Port	Direction	Function Description
Z	Output	Low-level output

4.2.4 Instantiation Template

```

GTP_ZERO GTP_ZERO_inst (
    .Z_ (z)
);
  
```

4.3 GTP_BUF

4.3.1 Supported Devices

Table 4-5 GTP_BUF-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

4.3.2 Description of Functionality

GTP_BUF is a general 1-bit BUFFER, and its structure is shown as follows:

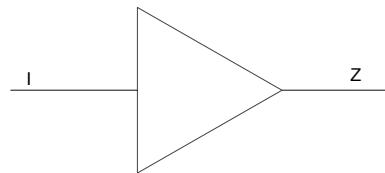


Figure 4-3 GTP_BUF Structure Diagram

4.3.3 Port Description

Table 4-6 GTP_BUF Port List

Port	Direction	Function Description
Z	Output	Output signal
I	Input	Input Signal

4.3.4 Instantiation Template

```
GTP_BUF GTP_BUF_inst (
    .I    (I),
    .Z    (Z)
);
```

4.4 GTP_INV

4.4.1 Supported Devices

Table 4-7 GTP_INV-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

4.4.2 Description of Functionality

GTP_INV is an inverter. The structure is shown below:

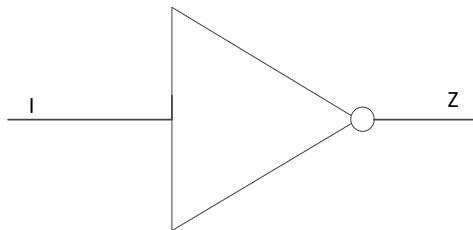


Figure 4-4 GTP_INV Structure Diagram

4.4.3 Port Description

Table 4-8 GTP_INV Port List

Port	Direction	Function Description
Z	Output	Inverted output signal
I	Input	Input Signal

4.4.4 Instantiation Template

```

GTP_INV  GTP_INV_inst (
    .I  (i),
    .Z  (z)
);
  
```

4.5 GTP_LUT1

4.5.1 Supported Devices

Table 4-9 GTP_LUT1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

4.5.2 Description of Functionality

GTP_LUT1 is a lookup table with 1-bit input and 1-bit output. The structure block diagram is shown below:

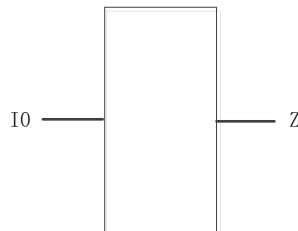


Figure 4-5 GTP_LUT1 Structure Diagram

4.5.3 Port Description

Table 4-10 GTP_LUT1 Port List

Port	Direction	Function Description
Z	Output	Output signal
I0	Input	Input Signal

Truth Table:

Table 4-11 GTP_LUT1 Truth Table

Input	Output
I0	Z
0	INIT[0]
1	INIT[1]

4.5.4 Parameter Description

Table 4-12 GTP_LUT1 Parameter List

Parameter Name	Description	Defaults	Valid Values
INIT	Output Configuration Parameter	2'h0	0~3

4.5.5 Instantiation Template

GTP_LUT1

```
#(
    .INIT  (2'h0)
  )GTP_LUT1_inst (
    .Z      (z),
    .I0     (i0)
);
```

4.6 GTP_LUT2

4.6.1 Supported Devices

Table 4-13 GTP_LUT2-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

4.6.2 Description of Functionality

GTP_LUT2 is a dual-input lookup table, with different INIT parameter values corresponding to different functions of LUT2; the corresponding INIT parameter must be specified when used. The structure block diagram is shown below:

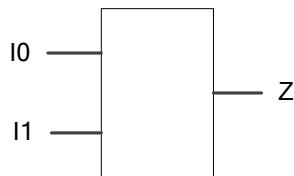


Figure 4-6 GTP_LUT2 Structure Diagram

4.6.3 Port Description

Table 4-14 GTP_LUT2 Port List

Port	Direction	Function Description
Z	Output	Output signal
I0	Input	Input Signal
I1	Input	Input Signal

Truth Table:

Table 4-15 GTP_LUT2 Truth Table

Input		Output
I1	I0	Z
0	0	INIT[0]
0	1	INIT[1]
1	0	INIT[2]
1	1	INIT[3]

4.6.4 Paramater Description

Table 4-16 GTP_LUT2 Parameter List

Parameter Name	Description	Defaults	Valid Values
INIT	Output Configuration Parameter	4'h0	0~15

4.6.5 Instantiation Template

```
GTP_LUT2
#(
    .INIT    (4'h0)
    )GTP_LUT2_inst (
        .Z      (z),
        .I0     (i0),
        .I1     (i1)
    );
```

4.7 GTP_LUT3

4.7.1 Supported Devices

Table 4-17 GTP_LUT3-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

4.7.2 Description of Functionality

GTP_LUT3 is a triple-input lookup table, with different INIT parameter values corresponding to different functions of LUT3; the corresponding INIT parameter must be specified when used. The structure block diagram is shown below:

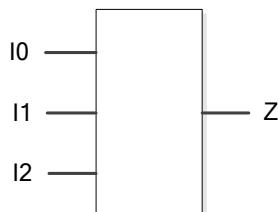


Figure 4-7 GTP_LUT3 Structure Diagram

4.7.3 Port Description

Table 4-18 GTP_LUT3 Port List

Port	Direction	Function Description
Z	Output	Output signal
I0	Input	Input Signal
I1	Input	Input Signal
I2	Input	Input Signal

Truth Table:

Table 4-19 GTP_LUT3 Truth Table

Input			Output
I2	I1	I0	Z
0	0	0	INIT[0]
0	0	1	INIT[1]
0	1	0	INIT[2]
0	1	1	INIT[3]
1	0	0	INIT[4]
1	0	1	INIT[5]
1	1	0	INIT[6]
1	1	1	INIT[7]

4.7.4 Parameter Description

Table 4-20 GTP_LUT3 Parameter List

Parameter Name	Description	Defaults	Valid Values
INIT	Output Configuration Parameter	8'h00	0~255

4.7.5 Instantiation Template

```
GTP_LUT3
#(
    .INIT      (8'h00)
  )GTP_LUT3_inst (
    .Z        (z),
    .I0       (i0),
    .I1       (i1),
    .I2       (i2)
);
```

4.8 GTP_LUT4

4.8.1 Supported Devices

Table 4-21 GTP_LUT4-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

4.8.2 Description of Functionality

GTP_LUT4 is a 4-input lookup table, with different INIT parameter values corresponding to different functions of LUT4; the corresponding INIT parameter must be specified when used. The structure block diagram is shown below:

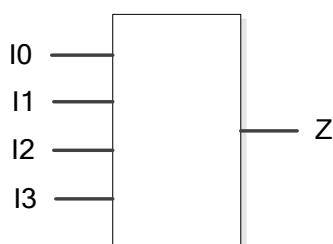


Figure 4-8 GTP_LUT4 Structure Diagram

4.8.3 Port Description

Table 4-22 GTP_LUT4 Port List

Port	Direction	Function Description
Z	Output	Output signal
I0	Input	Input Signal
I1	Input	Input Signal
I2	Input	Input Signal
I3	Input	Input Signal

Truth Table:

Table 4-23 GTP_LUT4 Truth Table

Input				Output
I3	I2	I1	I0	Z
0	0	0	0	INIT[0]
0	0	0	1	INIT[1]
0	0	1	0	INIT[2]
0	0	1	1	INIT[3]
0	1	0	0	INIT[4]
0	1	0	1	INIT[5]
0	1	1	0	INIT[6]
0	1	1	1	INIT[7]
1	0	0	0	INIT[8]
1	0	0	1	INIT[9]
1	0	1	0	INIT[10]
1	0	1	1	INIT[11]
1	1	0	0	INIT[12]
1	1	0	1	INIT[13]
1	1	1	0	INIT[14]
1	1	1	1	INIT[15]

4.8.4 Parameter Description

Table 4-24 GTP_LUT4 Parameter List

Parameter Name	Description	Defaults	Valid Values
INIT	Output Configuration Parameter	16'h0000	0~2^16-1

4.8.5 Instantiation Template

GTP_LUT4

```
#(
    .INIT  (16'h0000)
)GTP_LUT4_inst (
    .Z      (z),
    .I0     (i0),
    .I1     (i1),
    .I2     (i2),
    .I3     (i3)
);
```

4.9 GTP_LUT5

4.9.1 Supported Devices

Table 4-25 GTP_LUT5-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

4.9.2 Description of Functionality

GTP_LUT5 is a 5-input lookup table, with different INIT parameter values corresponding to different features of LUT5; the corresponding INIT parameter must be specified when used. The structure block diagram is shown below:

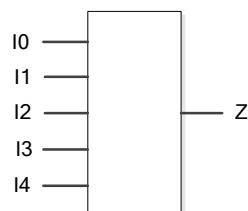


Figure 4-9 GTP_LUT5 Structure Diagram

4.9.3 Port Description

Table 4-26 GTP_LUT5 Port List

Port	Direction	Function Description
Z	Output	Output signal
I0	Input	Input Signal
I1	Input	Input Signal
I2	Input	Input Signal
I3	Input	Input Signal
I4	Input	Input Signal

Truth Table:

Table 4-27 GTP_LUT5 Truth Table

Input					Output
I4	I3	I2	I1	I0	Z
0	0	0	0	0	INIT[0]
0	0	0	0	1	INIT[1]
0	0	0	1	0	INIT[2]
0	0	0	1	1	INIT[3]
0	0	1	0	0	INIT[4]
0	0	1	0	1	INIT[5]
0	0	1	1	0	INIT[6]
0	0	1	1	1	INIT[7]
0	1	0	0	0	INIT[8]
0	1	0	0	1	INIT[9]
0	1	0	1	0	INIT[10]
0	1	0	1	1	INIT[11]
0	1	1	0	0	INIT[12]
0	1	1	0	1	INIT[13]
0	1	1	1	0	INIT[14]
0	1	1	1	1	INIT[15]
1	0	0	0	0	INIT[16]
1	0	0	0	1	INIT[17]
1	0	0	1	0	INIT[18]
1	0	0	1	1	INIT[19]
1	0	1	0	0	INIT[20]
1	0	1	0	1	INIT[21]
1	0	1	1	0	INIT[22]
1	0	1	1	1	INIT[23]
1	1	0	0	0	INIT[24]

Input					Output
I4	I3	I2	I1	I0	Z
1	1	0	0	1	INIT[25]
1	1	0	1	0	INIT[26]
1	1	0	1	1	INIT[27]
1	1	1	0	0	INIT[28]
1	1	1	0	1	INIT[29]
1	1	1	1	0	INIT[30]
1	1	1	1	1	INIT[31]

4.9.4 Paramater Description

Table 4-28 GTP_LUT5 Parameters

Parameter	Description	Defaults	Setting Value
INIT	Output Configuration Parameter	32'h0000_0000	0 ~ 2^32-1

4.9.5 Instantiation Template

```
GTP_LUT5
#(
    .INIT    (32'h0000_0000)
    )GTP_LUT5_inst (
        .Z      (z),
        .I0     (i0),
        .I1     (i1),
        .I2     (i2),
        .I3     (i3),
        .I4     (i4)
    );
```

4.10 GTP_LUT6

4.10.1 Supported Devices

Table 4-29 GTP_LUT6-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

4.10.2 Description of Functionality

GTP_LUT6 is a 6-input lookup table, with different INIT parameter values corresponding to different functions of LUT6. The corresponding INIT parameter must be specified when used. The structure block diagram is shown below:

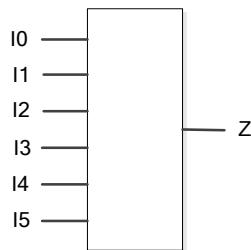


Figure 4-10 GTP_LUT6 Structure Diagram

4.10.3 Port Description

Table 4-30 GTP_LUT6 Ports

Port	Direction	Function Description
Z	Output	Output signal
I0	Input	Input Signal
I1	Input	Input Signal
I2	Input	Input Signal
I3	Input	Input Signal
I4	Input	Input Signal
I5	Input	Input Signal

Truth Table:

Table 4-31 GTP_LUT6 Truth Table

Input						Output
I5	I4	I3	I2	I1	I0	Z
0	0	0	0	0	0	INIT[0]
0	0	0	0	0	1	INIT[1]
0	0	0	0	1	0	INIT[2]
0	0	0	0	1	1	INIT[3]
0	0	0	1	0	0	INIT[4]
0	0	0	1	0	1	INIT[5]
0	0	0	1	1	0	INIT[6]
0	0	0	1	1	1	INIT[7]
0	0	1	0	0	0	INIT[8]
0	0	1	0	0	1	INIT[9]

Input						Output
I5	I4	I3	I2	I1	I0	Z
0	0	1	0	1	0	INIT[10]
0	0	1	0	1	1	INIT[11]
0	0	1	1	0	0	INIT[12]
0	0	1	1	0	1	INIT[13]
0	0	1	1	1	0	INIT[14]
0	0	1	1	1	1	INIT[15]
0	1	0	0	0	0	INIT[16]
0	1	0	0	0	1	INIT[17]
0	1	0	0	1	0	INIT[18]
0	1	0	0	1	1	INIT[19]
0	1	0	1	0	0	INIT[20]
0	1	0	1	0	1	INIT[21]
0	1	0	1	1	0	INIT[22]
0	1	0	1	1	1	INIT[23]
0	1	1	0	0	0	INIT[24]
0	1	1	0	0	1	INIT[25]
0	1	1	0	1	0	INIT[26]
0	1	1	0	1	1	INIT[27]
0	1	1	1	0	0	INIT[28]
0	1	1	1	0	1	INIT[29]
0	1	1	1	1	0	INIT[30]
0	1	1	1	1	1	INIT[31]
1	0	0	0	0	0	INIT[32]
1	0	0	0	0	1	INIT[33]
1	0	0	0	1	0	INIT[34]
1	0	0	0	1	1	INIT[35]
1	0	0	1	0	0	INIT[36]
1	0	0	1	0	1	INIT[37]
1	0	0	1	1	0	INIT[38]
1	0	0	1	1	1	INIT[39]
1	0	1	0	0	0	INIT[40]
1	0	1	0	0	1	INIT[41]
1	0	1	0	1	0	INIT[42]
1	0	1	0	1	1	INIT[43]
1	0	1	1	0	0	INIT[44]
1	0	1	1	0	1	INIT[45]
1	0	1	1	1	0	INIT[46]
1	0	1	1	1	1	INIT[47]

Input						Output
I5	I4	I3	I2	I1	I0	Z
1	1	0	0	0	0	INIT[48]
1	1	0	0	0	1	INIT[49]
1	1	0	0	1	0	INIT[50]
1	1	0	0	1	1	INIT[51]
1	1	0	1	0	0	INIT[52]
1	1	0	1	0	1	INIT[53]
1	1	0	1	1	0	INIT[54]
1	1	0	1	1	1	INIT[55]
1	1	1	0	0	0	INIT[56]
1	1	1	0	0	1	INIT[57]
1	1	1	0	1	0	INIT[58]
1	1	1	0	1	1	INIT[59]
1	1	1	1	0	0	INIT[60]
1	1	1	1	0	1	INIT[61]
1	1	1	1	1	0	INIT[62]
1	1	1	1	1	1	INIT[63]

4.10.4 Paramater Description

Table 4-32 GTP_LUT6 Parameters

Parameter	Description	Defaults	Setting Value
INIT	Output Configuration Parameter	64'h0000_0000_0000_0000	0 ~ 2^64-1

4.10.5 Instantiation Template

```
GTP_LUT6
#(
    .INIT  (64'h0000_0000_0000_0000)
)GTP_LUT6_inst (
    .Z      (z),
    .I0     (i0),
    .I1     (i1),
    .I2     (i2),
    .I3     (i3),
    .I4     (i4),
    .I5     (i5)
);
```

4.11 GTP_LUT7

4.11.1 Supported Devices

Table 4-33 GTP_LUT7-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

4.11.2 Description of Functionality

GTP_LUT7 is a 7-input lookup table, with different INIT parameter values corresponding to different functions of LUT7; the corresponding INIT parameter must be specified when used. The structure block diagram is shown below:

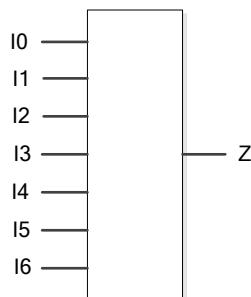


Figure 4-11 GTP_LUT7 Structure Diagram

4.11.3 Port Description

Table 4-34 GTP_LUT7 Ports

Port	Direction	Function Description
Z	Output	Output signal
I0	Input	Input Signal
I1	Input	Input Signal
I2	Input	Input Signal
I3	Input	Input Signal
I4	Input	Input Signal
I5	Input	Input Signal
I6	Input	Input Signal

Truth Table:

Table 4-35 GTP_LUT7 Truth Table

Input							Output
I6	I5	I4	I3	I2	I1	I0	Z
0	0	0	0	0	0	0	INIT[0]
0	0	0	0	0	0	1	INIT[1]
0	0	0	0	0	1	0	INIT[2]
0	0	0	0	0	1	1	INIT[3]
0	0	0	0	1	0	0	INIT[4]
0	0	0	0	1	0	1	INIT[5]
0	0	0	0	1	1	0	INIT[6]
0	0	0	0	1	1	1	INIT[7]
0	0	0	1	0	0	0	INIT[8]
0	0	0	1	0	0	1	INIT[9]
0	0	0	1	0	1	0	INIT[10]
0	0	0	1	0	1	1	INIT[11]
0	0	0	1	1	0	0	INIT[12]
0	0	0	1	1	0	1	INIT[13]
0	0	0	1	1	1	0	INIT[14]
0	0	0	1	1	1	1	INIT[15]
0	0	1	0	0	0	0	INIT[16]
0	0	1	0	0	0	1	INIT[17]
0	0	1	0	0	1	0	INIT[18]
0	0	1	0	0	1	1	INIT[19]
0	0	1	0	1	0	0	INIT[20]
0	0	1	0	1	0	1	INIT[21]
0	0	1	0	1	1	0	INIT[22]

Input							Output
I6	I5	I4	I3	I2	I1	I0	Z
0	0	1	0	1	1	1	INIT[23]
0	0	1	1	0	0	0	INIT[24]
0	0	1	1	0	0	1	INIT[25]
0	0	1	1	0	1	0	INIT[26]
0	0	1	1	0	1	1	INIT[27]
0	0	1	1	1	0	0	INIT[28]
0	0	1	1	1	0	1	INIT[29]
0	0	1	1	1	1	0	INIT[30]
0	0	1	1	1	1	1	INIT[31]
0	1	0	0	0	0	0	INIT[32]
0	1	0	0	0	0	1	INIT[33]
0	1	0	0	0	1	0	INIT[34]
0	1	0	0	0	1	1	INIT[35]
0	1	0	0	1	0	0	INIT[36]
0	1	0	0	1	0	1	INIT[37]
0	1	0	0	1	1	0	INIT[38]
0	1	0	0	1	1	1	INIT[39]
0	1	0	1	0	0	0	INIT[40]
0	1	0	1	0	0	1	INIT[41]
0	1	0	1	0	1	0	INIT[42]
0	1	0	1	0	1	1	INIT[43]
0	1	0	1	1	0	0	INIT[44]
0	1	0	1	1	0	1	INIT[45]
0	1	0	1	1	1	0	INIT[46]
0	1	0	1	1	1	1	INIT[47]
0	1	1	0	0	0	0	INIT[48]
0	1	1	0	0	0	1	INIT[49]
0	1	1	0	0	1	0	INIT[50]
0	1	1	0	0	1	1	INIT[51]
0	1	1	0	1	0	0	INIT[52]
0	1	1	0	1	0	1	INIT[53]
0	1	1	0	1	1	0	INIT[54]
0	1	1	0	1	1	1	INIT[55]
0	1	1	1	0	0	0	INIT[56]
0	1	1	1	0	0	1	INIT[57]
0	1	1	1	0	1	0	INIT[58]
0	1	1	1	0	1	1	INIT[59]
0	1	1	1	1	0	0	INIT[60]

Input							Output
I6	I5	I4	I3	I2	I1	I0	Z
0	1	1	1	1	0	1	INIT[61]
0	1	1	1	1	1	0	INIT[62]
0	1	1	1	1	1	1	INIT[63]
1	0	0	0	0	0	0	INIT[64]
1	0	0	0	0	0	1	INIT[65]
1	0	0	0	0	1	0	INIT[66]
1	0	0	0	0	1	1	INIT[67]
1	0	0	0	1	0	0	INIT[68]
1	0	0	0	1	0	1	INIT[69]
1	0	0	0	1	1	0	INIT[70]
1	0	0	0	1	1	1	INIT[71]
1	0	0	1	0	0	0	INIT[72]
1	0	0	1	0	0	1	INIT[73]
1	0	0	1	0	1	0	INIT[74]
1	0	0	1	1	0	0	INIT[75]
1	0	0	1	1	0	1	INIT[76]
1	0	0	1	1	0	1	INIT[77]
1	0	0	1	1	1	0	INIT[78]
1	0	0	1	1	1	1	INIT[79]
1	0	1	0	0	0	0	INIT[80]
1	0	1	0	0	0	1	INIT[81]
1	0	1	0	0	1	0	INIT[82]
1	0	1	0	0	1	1	INIT[83]
1	0	1	0	1	0	0	INIT[84]
1	0	1	0	1	0	1	INIT[85]
1	0	1	0	1	1	0	INIT[86]
1	0	1	0	1	1	1	INIT[87]
1	0	1	1	0	0	0	INIT[88]
1	0	1	1	0	0	1	INIT[89]
1	0	1	1	0	1	0	INIT[90]
1	0	1	1	0	1	1	INIT[91]
1	0	1	1	1	0	0	INIT[92]
1	0	1	1	1	0	1	INIT[93]
1	0	1	1	1	1	0	INIT[94]
1	0	1	1	1	1	1	INIT[95]
1	1	0	0	0	0	0	INIT[96]
1	1	0	0	0	0	1	INIT[97]
1	1	0	0	0	1	0	INIT[98]

Input							Output
I6	I5	I4	I3	I2	I1	I0	Z
1	1	0	0	0	1	1	INIT[99]
1	1	0	0	1	0	0	INIT[100]
1	1	0	0	1	0	1	INIT[101]
1	1	0	0	1	1	0	INIT[102]
1	1	0	0	1	1	1	INIT[103]
1	1	0	1	0	0	0	INIT[104]
1	1	0	1	0	0	1	INIT[105]
1	1	0	1	0	1	0	INIT[106]
1	1	0	1	0	1	1	INIT[107]
1	1	0	1	1	0	0	INIT[108]
1	1	0	1	1	0	1	INIT[109]
1	1	0	1	1	1	0	INIT[110]
1	1	0	1	1	1	1	INIT[111]
1	1	1	0	0	0	0	INIT[112]
1	1	1	0	0	0	1	INIT[113]
1	1	1	0	0	1	0	INIT[114]
1	1	1	0	0	1	1	INIT[115]
1	1	1	0	1	0	0	INIT[116]
1	1	1	0	1	0	1	INIT[117]
1	1	1	0	1	1	0	INIT[118]
1	1	1	0	1	1	1	INIT[119]
1	1	1	1	0	0	0	INIT[120]
1	1	1	1	0	0	1	INIT[121]
1	1	1	1	0	1	0	INIT[122]
1	1	1	1	0	1	1	INIT[123]
1	1	1	1	1	0	0	INIT[124]
1	1	1	1	1	0	1	INIT[125]
1	1	1	1	1	1	0	INIT[126]
1	1	1	1	1	1	1	INIT[127]

4.11.4 Parameter Description

Table 4-36 GTP_LUT7 Parameters

Parameter	Description	Defaults	Setting Value
INIT	Output Configuration Parameter	128'h00000000_00000000_00000000_00000000	0 ~ 2^128-1

4.11.5 Instantiation Template

```
GTP_LUT7
#(
    .INIT  (128'h00000000_00000000_00000000_00000000)
)GTP_LUT7_inst (
    .Z      (z),
    .I0     (i0),
    .I1     (i1),
    .I2     (i2),
    .I3     (i3),
    .I4     (i4),
    .I5     (i5),
    .I6     (i6)
);
```

4.12 GTP_LUT8

4.12.1 Supported Devices

Table 4-37 GTP_LUT8-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

4.12.2 Description of Functionality

GTP_LUT8 is an 8-input lookup table, with different INIT parameter values corresponding to different functions of LUT8; the corresponding INIT parameter must be specified when used. The structure block diagram is shown below:

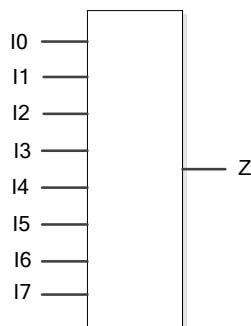


Figure 4-12 GTP_LUT8 Structure Diagram

4.12.3 Port Description

Table 4-38 GTP_LUT8 Ports

Port	Direction	Function Description
Z	Output	Output signal
I0	Input	Input Signal
I1	Input	Input Signal
I2	Input	Input Signal
I3	Input	Input Signal
I4	Input	Input Signal
I5	Input	Input Signal
I6	Input	Input Signal
I7	Input	Input Signal

Truth Table:

Table 4-39 GTP_LUT8 Truth Table

Input								Output
I7	I6	I5	I4	I3	I2	I1	I0	Z
0	0	0	0	0	0	0	0	INIT[0]
0	0	0	0	0	0	0	1	INIT[1]
0	0	0	0	0	0	1	0	INIT[2]
0	0	0	0	0	0	1	1	INIT[3]
0	0	0	0	0	1	0	0	INIT[4]
0	0	0	0	0	1	0	1	INIT[5]
0	0	0	0	0	1	1	0	INIT[6]
0	0	0	0	0	1	1	1	INIT[7]
0	0	0	0	1	0	0	0	INIT[8]
0	0	0	0	1	0	0	1	INIT[9]
0	0	0	0	1	0	1	0	INIT[10]
0	0	0	0	1	0	1	1	INIT[11]
0	0	0	0	1	1	0	0	INIT[12]
0	0	0	0	1	1	0	1	INIT[13]
0	0	0	0	1	1	1	0	INIT[14]
0	0	0	0	1	1	1	1	INIT[15]
0	0	0	1	0	0	0	0	INIT[16]
0	0	0	1	0	0	0	1	INIT[17]
0	0	0	1	0	0	1	0	INIT[18]
0	0	0	1	0	0	1	1	INIT[19]
0	0	0	1	0	1	0	0	INIT[20]
0	0	0	1	0	1	0	1	INIT[21]

Input								Output
I7	I6	I5	I4	I3	I2	I1	I0	Z
0	0	0	1	0	1	1	0	INIT[22]
0	0	0	1	0	1	1	1	INIT[23]
0	0	0	1	1	0	0	0	INIT[24]
0	0	0	1	1	0	0	1	INIT[25]
0	0	0	1	1	0	1	0	INIT[26]
0	0	0	1	1	0	1	1	INIT[27]
0	0	0	1	1	1	0	0	INIT[28]
0	0	0	1	1	1	0	1	INIT[29]
0	0	0	1	1	1	1	0	INIT[30]
0	0	0	1	1	1	1	1	INIT[31]
0	0	1	0	0	0	0	0	INIT[32]
0	0	1	0	0	0	0	1	INIT[33]
0	0	1	0	0	0	1	0	INIT[34]
0	0	1	0	0	0	1	1	INIT[35]
0	0	1	0	0	1	0	0	INIT[36]
0	0	1	0	0	1	0	1	INIT[37]
0	0	1	0	0	1	1	0	INIT[38]
0	0	1	0	0	1	1	1	INIT[39]
0	0	1	0	1	0	0	0	INIT[40]
0	0	1	0	1	0	0	1	INIT[41]
0	0	1	0	1	0	1	0	INIT[42]
0	0	1	0	1	0	1	1	INIT[43]
0	0	1	0	1	1	0	0	INIT[44]
0	0	1	0	1	1	0	1	INIT[45]
0	0	1	0	1	1	1	0	INIT[46]
0	0	1	0	1	1	1	1	INIT[47]
0	0	1	1	0	0	0	0	INIT[48]
0	0	1	1	0	0	0	1	INIT[49]
0	0	1	1	0	0	1	0	INIT[50]
0	0	1	1	0	0	1	1	INIT[51]
0	0	1	1	0	1	0	0	INIT[52]
0	0	1	1	0	1	0	1	INIT[53]
0	0	1	1	0	1	1	0	INIT[54]
0	0	1	1	0	1	1	1	INIT[55]
0	0	1	1	1	0	0	0	INIT[56]
0	0	1	1	1	0	0	1	INIT[57]
0	0	1	1	1	0	1	0	INIT[58]
0	0	1	1	1	0	1	1	INIT[59]

Input								Output
I7	I6	I5	I4	I3	I2	I1	I0	Z
0	0	1	1	1	1	0	0	INIT[60]
0	0	1	1	1	1	0	1	INIT[61]
0	0	1	1	1	1	1	0	INIT[62]
0	0	1	1	1	1	1	1	INIT[63]
0	1	0	0	0	0	0	0	INIT[64]
0	1	0	0	0	0	0	1	INIT[65]
0	1	0	0	0	0	1	0	INIT[66]
0	1	0	0	0	0	1	1	INIT[67]
0	1	0	0	0	1	0	0	INIT[68]
0	1	0	0	0	1	0	1	INIT[69]
0	1	0	0	0	1	1	0	INIT[70]
0	1	0	0	0	1	1	1	INIT[71]
0	1	0	0	1	0	0	0	INIT[72]
0	1	0	0	1	0	0	1	INIT[73]
0	1	0	0	1	0	1	0	INIT[74]
0	1	0	0	1	0	1	1	INIT[75]
0	1	0	0	1	1	0	0	INIT[76]
0	1	0	0	1	1	0	1	INIT[77]
0	1	0	0	1	1	1	0	INIT[78]
0	1	0	0	1	1	1	1	INIT[79]
0	1	0	1	0	0	0	0	INIT[80]
0	1	0	1	0	0	0	1	INIT[81]
0	1	0	1	0	0	1	0	INIT[82]
0	1	0	1	0	0	1	1	INIT[83]
0	1	0	1	0	1	0	0	INIT[84]
0	1	0	1	0	1	0	1	INIT[85]
0	1	0	1	0	1	1	0	INIT[86]
0	1	0	1	0	1	1	1	INIT[87]
0	1	0	1	1	0	0	0	INIT[88]
0	1	0	1	1	0	0	1	INIT[89]
0	1	0	1	1	0	1	0	INIT[90]
0	1	0	1	1	0	1	1	INIT[91]
0	1	0	1	1	1	0	0	INIT[92]
0	1	0	1	1	1	0	1	INIT[93]
0	1	0	1	1	1	1	0	INIT[94]
0	1	0	1	1	1	1	1	INIT[95]
0	1	1	0	0	0	0	0	INIT[96]
0	1	1	0	0	0	0	1	INIT[97]

Input								Output
I7	I6	I5	I4	I3	I2	I1	I0	Z
0	1	1	0	0	0	1	0	INIT[98]
0	1	1	0	0	0	1	1	INIT[99]
0	1	1	0	0	1	0	0	INIT[100]
0	1	1	0	0	1	0	1	INIT[101]
0	1	1	0	0	1	1	0	INIT[102]
0	1	1	0	0	1	1	1	INIT[103]
0	1	1	0	1	0	0	0	INIT[104]
0	1	1	0	1	0	0	1	INIT[105]
0	1	1	0	1	0	1	0	INIT[106]
0	1	1	0	1	0	1	1	INIT[107]
0	1	1	0	1	1	0	0	INIT[108]
0	1	1	0	1	1	0	1	INIT[109]
0	1	1	0	1	1	1	0	INIT[110]
0	1	1	0	1	1	1	1	INIT[111]
0	1	1	1	0	0	0	0	INIT[112]
0	1	1	1	0	0	0	1	INIT[113]
0	1	1	1	0	0	1	0	INIT[114]
0	1	1	1	0	0	1	1	INIT[115]
0	1	1	1	0	1	0	0	INIT[116]
0	1	1	1	0	1	0	1	INIT[117]
0	1	1	1	0	1	1	0	INIT[118]
0	1	1	1	0	1	1	1	INIT[119]
0	1	1	1	1	0	0	0	INIT[120]
0	1	1	1	1	0	0	1	INIT[121]
0	1	1	1	1	0	1	0	INIT[122]
0	1	1	1	1	0	1	1	INIT[123]
0	1	1	1	1	1	0	0	INIT[124]
0	1	1	1	1	1	0	1	INIT[125]
0	1	1	1	1	1	1	0	INIT[126]
0	1	1	1	1	1	1	1	INIT[127]
1	0	0	0	0	0	0	0	INIT[128]
1	0	0	0	0	0	0	1	INIT[129]
1	0	0	0	0	0	1	0	INIT[130]
1	0	0	0	0	0	1	1	INIT[131]
1	0	0	0	0	1	0	0	INIT[132]
1	0	0	0	0	1	0	1	INIT[133]
1	0	0	0	0	1	1	0	INIT[134]
1	0	0	0	0	1	1	1	INIT[135]

Input								Output
I7	I6	I5	I4	I3	I2	I1	I0	Z
1	0	0	0	1	0	0	0	INIT[136]
1	0	0	0	1	0	0	1	INIT[137]
1	0	0	0	1	0	1	0	INIT[138]
1	0	0	0	1	0	1	1	INIT[139]
1	0	0	0	1	1	0	0	INIT[140]
1	0	0	0	1	1	0	1	INIT[141]
1	0	0	0	1	1	1	0	INIT[142]
1	0	0	0	1	1	1	1	INIT[143]
1	0	0	1	0	0	0	0	INIT[144]
1	0	0	1	0	0	0	1	INIT[145]
1	0	0	1	0	0	1	0	INIT[146]
1	0	0	1	0	0	1	1	INIT[147]
1	0	0	1	0	1	0	0	INIT[148]
1	0	0	1	0	1	0	1	INIT[149]
1	0	0	1	1	0	1	0	INIT[150]
1	0	0	1	0	1	1	1	INIT[151]
1	0	0	1	1	0	0	0	INIT[152]
1	0	0	1	1	0	0	1	INIT[153]
1	0	0	1	1	0	1	0	INIT[154]
1	0	0	1	1	0	1	1	INIT[155]
1	0	0	1	1	1	0	0	INIT[156]
1	0	0	1	1	1	0	1	INIT[157]
1	0	0	1	1	1	1	0	INIT[158]
1	0	0	1	1	1	1	1	INIT[159]
1	0	1	0	0	0	0	0	INIT[160]
1	0	1	0	0	0	0	1	INIT[161]
1	0	1	0	0	0	1	0	INIT[162]
1	0	1	0	0	0	1	1	INIT[163]
1	0	1	0	0	1	0	0	INIT[164]
1	0	1	0	0	1	0	1	INIT[165]
1	0	1	0	0	1	1	0	INIT[166]
1	0	1	0	0	1	1	1	INIT[167]
1	0	1	0	1	0	0	0	INIT[168]
1	0	1	0	1	0	0	1	INIT[169]
1	0	1	0	1	0	1	0	INIT[170]
1	0	1	0	1	0	1	1	INIT[171]
1	0	1	0	1	1	0	0	INIT[172]
1	0	1	0	1	1	0	1	INIT[173]

Input								Output
I7	I6	I5	I4	I3	I2	I1	I0	Z
1	0	1	0	1	1	1	0	INIT[174]
1	0	1	0	1	1	1	1	INIT[175]
1	0	1	1	0	0	0	0	INIT[176]
1	0	1	1	0	0	0	1	INIT[177]
1	0	1	1	0	0	1	0	INIT[178]
1	0	1	1	0	0	1	1	INIT[179]
1	0	1	1	0	1	0	0	INIT[180]
1	0	1	1	0	1	0	1	INIT[181]
1	0	1	1	0	1	1	0	INIT[182]
1	0	1	1	0	1	1	1	INIT[183]
1	0	1	1	1	0	0	0	INIT[184]
1	0	1	1	1	0	0	1	INIT[185]
1	0	1	1	1	0	1	0	INIT[186]
1	0	1	1	1	0	1	1	INIT[187]
1	0	1	1	1	1	0	0	INIT[188]
1	0	1	1	1	1	0	1	INIT[189]
1	0	1	1	1	1	1	0	INIT[190]
1	0	1	1	1	1	1	1	INIT[191]
1	1	0	0	0	0	0	0	INIT[192]
1	1	0	0	0	0	0	1	INIT[193]
1	1	0	0	0	0	1	0	INIT[194]
1	1	0	0	0	0	1	1	INIT[195]
1	1	0	0	0	1	0	0	INIT[196]
1	1	0	0	0	1	0	1	INIT[197]
1	1	0	0	0	1	1	0	INIT[198]
1	1	0	0	0	1	1	1	INIT[199]
1	1	0	0	1	0	0	0	INIT[200]
1	1	0	0	1	0	0	1	INIT[201]
1	1	0	0	1	0	1	0	INIT[202]
1	1	0	0	1	0	1	1	INIT[203]
1	1	0	0	1	1	0	0	INIT[204]
1	1	0	0	1	1	0	1	INIT[205]
1	1	0	0	1	1	1	0	INIT[206]
1	1	0	0	1	1	1	1	INIT[207]
1	1	0	1	0	0	0	0	INIT[208]
1	1	0	1	0	0	0	1	INIT[209]
1	1	0	1	0	0	1	0	INIT[210]
1	1	0	1	0	0	1	1	INIT[211]

Input								Output
I7	I6	I5	I4	I3	I2	I1	I0	Z
1	1	0	1	0	1	0	0	INIT[212]
1	1	0	1	0	1	0	1	INIT[213]
1	1	0	1	0	1	1	0	INIT[214]
1	1	0	1	0	1	1	1	INIT[215]
1	1	0	1	1	0	0	0	INIT[216]
1	1	0	1	1	0	0	1	INIT[217]
1	1	0	1	1	0	1	0	INIT[218]
1	1	0	1	1	0	1	1	INIT[219]
1	1	0	1	1	1	0	0	INIT[220]
1	1	0	1	1	1	0	1	INIT[221]
1	1	0	1	1	1	1	0	INIT[222]
1	1	0	1	1	1	1	1	INIT[223]
1	1	1	0	0	0	0	0	INIT[224]
1	1	1	0	0	0	0	1	INIT[225]
1	1	1	0	0	0	1	0	INIT[226]
1	1	1	0	0	0	1	1	INIT[227]
1	1	1	0	0	1	0	0	INIT[228]
1	1	1	0	0	1	0	1	INIT[229]
1	1	1	0	0	1	1	0	INIT[230]
1	1	1	0	0	1	1	1	INIT[231]
1	1	1	0	1	0	0	0	INIT[232]
1	1	1	0	1	0	0	1	INIT[233]
1	1	1	0	1	0	1	0	INIT[234]
1	1	1	0	1	0	1	1	INIT[235]
1	1	1	0	1	1	0	0	INIT[236]
1	1	1	0	1	1	0	1	INIT[237]
1	1	1	0	1	1	1	0	INIT[238]
1	1	1	0	1	1	1	1	INIT[239]
1	1	1	1	0	0	0	0	INIT[240]
1	1	1	1	0	0	0	1	INIT[241]
1	1	1	1	0	0	1	0	INIT[242]
1	1	1	1	0	0	1	1	INIT[243]
1	1	1	1	0	1	0	0	INIT[244]
1	1	1	1	0	1	0	1	INIT[245]
1	1	1	1	0	1	1	0	INIT[246]
1	1	1	1	0	1	1	1	INIT[247]
1	1	1	1	1	0	0	0	INIT[248]
1	1	1	1	1	0	0	1	INIT[249]

Input								Output
I7	I6	I5	I4	I3	I2	I1	I0	Z
1	1	1	1	1	0	1	0	INIT[250]
1	1	1	1	1	0	1	1	INIT[251]
1	1	1	1	1	1	0	0	INIT[252]
1	1	1	1	1	1	0	1	INIT[253]
1	1	1	1	1	1	1	0	INIT[254]
1	1	1	1	1	1	1	1	INIT[255]

4.12.4 Paramater Description

Table 4-40 GTP_LUT8 Parameters

Parameter	Description	Defaults	Setting Value
INIT	Output Configuration Parameter	256'h0000000000000000_0000000000000000_0000000000000000_0000000000000000	0 ~ 2^256-1

4.12.5 Instantiation Template

GTP_LUT8

```
#(
    .INIT  (256'h0000000000000000_0000000000000000_0000000000000000_0000000000000000)
    )GTP_LUT8_inst (
        .Z      (z),
        .I0     (i0),
        .I1     (i1),
        .I2     (i2),
        .I3     (i3),
        .I4     (i4),
        .I5     (i5),
        .I6     (i6),
        .I7     (i7)
    );
```

4.13 GTP_LUT6CARRY

4.13.1 Supported Devices

Table 4-41 GTP_LUT6CARRY-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

4.13.2 Description of Functionality

GTP_LUT6CARRY is a fast carry logic, typically used for addition and subtraction operations, settable counter counting, one out of four data selector MUX41, data comparator, address logic, priority encoder and other applications. The Structure Diagram is shown below:

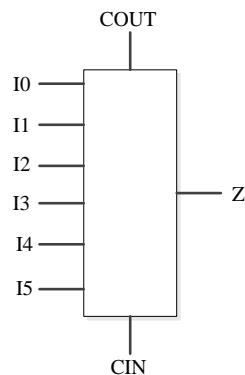


Figure 4-13 GTP_LUT6CARRY Structure Diagram

4.13.3 Port Description

Table 4-42 GTP_LUT6CARRY Ports

Port	Direction	Function Description
I0	Input	Input Signal
I1	Input	Input Signal
I2	Input	Input Signal
I3	Input	Input Signal
I4	Input	Input Signal
I5	Input	Input Signal
CIN	Input	Input signal, cascade input
COUT	Output	Cascade output
Z	Output	Output signal

4.13.4 Parameter Description

Table 4-43 GTP_LUT6CARRY Parameters

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
INIT	<binary>	0~2^64-1	64'h0000_0000_0000_0000	Output Configuration Parameter
I5_TO_CARRY	<string>	"TRUE" or "FALSE"	"TRUE"	Select parameters of I5 and LUT5B
I5_TO_LUT	<string>	"TRUE" or "FALSE"	"FALSE"	Select parameters of I5 and CIN

4.13.5 Instantiation Template

```
GTP_LUT6CARRY #(
    .INIT(64'h0000_0000_0000_0000),
    .I5_TO_CARRY("TRUE"),
    .I5_TO_LUT("FALSE")
) GTP_LUT6CARRY_inst (
    .COUT(cout),
    .Z(z),
    .CIN(cin),
    .I0(i0),
    .I1(i1),
    .I2(i2),
    .I3(i3),
    .I4(i4),
    .I5(i5)
);
```

4.14 GTP_LUT6D

4.14.1 Supported Devices

Table 4-44 GTP_LUT6D-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

4.14.2 Description of Functionality

GTP_LUT6D consists of a 6-input lookup table with 2 output ports. Different INIT parameter values correspond to different functions of LUT6D. The corresponding INIT parameter must be specified when used. Depending on the input values of I5, I4, I3, I2, I1 and I0, Z can output each bit of INIT, while Z5 can only output the 32 lower bits of INIT.

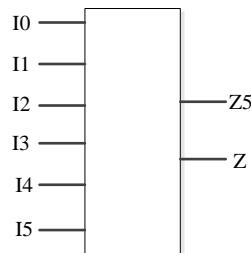


Figure 4-14 GTP_LUT 6D Structure Diagram

4.14.3 Port Description

Table 4-45 GTP_LUT6D Ports

Port	Direction	Function Description
I0	Input	Input Signal
I1	Input	Input Signal
I2	Input	Input Signal
I3	Input	Input Signal
I4	Input	Input Signal
I5	Input	Input Signal
Z5	Output	Output signal
Z	Output	Output signal

4.14.4 Parameter Description

Table 4-46 GTP_LUT6D Parameters

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
INIT	<binary>	0~2^64-1	64'h0000_0000_0000_0000	Output Configuration Parameter

Table 4-47 GTP_LUT6D Parameter Truth Table

Input						Output	
I5	I4	I3	I2	I1	I0	Z	Z5
0	0	0	0	0	0	INIT[0]	INIT[0]
0	0	0	0	0	1	INIT[1]	INIT[1]
0	0	0	0	1	0	INIT[2]	INIT[2]
0	0	0	0	1	1	INIT[3]	INIT[3]
0	0	0	1	0	0	INIT[4]	INIT[4]
0	0	0	1	0	1	INIT[5]	INIT[5]
0	0	0	1	1	0	INIT[6]	INIT[6]
0	0	0	1	1	1	INIT[7]	INIT[7]
0	0	1	0	0	0	INIT[8]	INIT[8]
0	0	1	0	0	1	INIT[9]	INIT[9]
0	0	1	0	1	0	INIT[10]	INIT[10]
0	0	1	0	1	1	INIT[11]	INIT[11]
0	0	1	1	0	0	INIT[12]	INIT[12]
0	0	1	1	0	1	INIT[13]	INIT[13]
0	0	1	1	1	0	INIT[14]	INIT[14]
0	0	1	1	1	1	INIT[15]	INIT[15]
0	1	0	0	0	0	INIT[16]	INIT[16]
0	1	0	0	0	1	INIT[17]	INIT[17]
0	1	0	0	1	0	INIT[18]	INIT[18]
0	1	0	0	1	1	INIT[19]	INIT[19]
0	1	0	1	0	0	INIT[20]	INIT[20]
0	1	0	1	0	1	INIT[21]	INIT[21]
0	1	0	1	1	0	INIT[22]	INIT[22]
0	1	0	1	1	1	INIT[23]	INIT[23]
0	1	1	0	0	0	INIT[24]	INIT[24]
0	1	1	0	0	1	INIT[25]	INIT[25]
0	1	1	0	1	0	INIT[26]	INIT[26]
0	1	1	0	1	1	INIT[27]	INIT[27]
0	1	1	1	0	0	INIT[28]	INIT[28]
0	1	1	1	0	1	INIT[29]	INIT[29]
0	1	1	1	1	0	INIT[30]	INIT[30]
0	1	1	1	1	1	INIT[31]	INIT[31]
1	0	0	0	0	0	INIT[32]	INIT[0]
1	0	0	0	0	1	INIT[33]	INIT[1]
1	0	0	0	1	0	INIT[34]	INIT[2]
1	0	0	0	1	1	INIT[35]	INIT[3]
1	0	0	1	0	0	INIT[36]	INIT[4]

Input						Output	
I5	I4	I3	I2	I1	I0	Z	Z5
1	0	0	1	0	1	INIT[37]	INIT[5]
1	0	0	1	1	0	INIT[38]	INIT[6]
1	0	0	1	1	1	INIT[39]	INIT[7]
1	0	1	0	0	0	INIT[40]	INIT[8]
1	0	1	0	0	1	INIT[41]	INIT[9]
1	0	1	0	1	0	INIT[42]	INIT[10]
1	0	1	0	1	1	INIT[43]	INIT[11]
1	0	1	1	0	0	INIT[44]	INIT[12]
1	0	1	1	0	1	INIT[45]	INIT[13]
1	0	1	1	1	0	INIT[46]	INIT[14]
1	0	1	1	1	1	INIT[47]	INIT[15]
1	1	0	0	0	0	INIT[48]	INIT[16]
1	1	0	0	0	1	INIT[49]	INIT[17]
1	1	0	0	1	0	INIT[50]	INIT[18]
1	1	0	0	1	1	INIT[51]	INIT[19]
1	1	0	1	0	0	INIT[52]	INIT[20]
1	1	0	1	0	1	INIT[53]	INIT[21]
1	1	0	1	1	0	INIT[54]	INIT[22]
1	1	0	1	1	1	INIT[55]	INIT[23]
1	1	1	0	0	0	INIT[56]	INIT[24]
1	1	1	0	0	1	INIT[57]	INIT[25]
1	1	1	0	1	0	INIT[58]	INIT[26]
1	1	1	0	1	1	INIT[59]	INIT[27]
1	1	1	1	0	0	INIT[60]	INIT[28]
1	1	1	1	0	1	INIT[61]	INIT[29]
1	1	1	1	1	0	INIT[62]	INIT[30]
1	1	1	1	1	1	INIT[63]	INIT[31]

4.14.5 Instantiation Template

```
GTP_LUT6D #(
    .INIT(64'h0000_0000_0000_0000)
) GTP_LUT6D_inst (
    .Z(z),
    .Z5(z5),
    .I0(i0),
    .I1(i1),
    .I2(i2),
    .I3(i3),
    .I4(i4),
    .I5(i5)
);
```

4.15 GTP_MUX2LUT7

4.15.1 Supported Devices

Table 4-48 GTP_MUX2LUT7-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

4.15.2 Description of Functionality

GTP_MUX2LUT7 is a dual-input selector dedicated to GTP_LUT7, where I0 and I1 are data inputs, and S is the selection signal. It outputs I0 when S is 1'b0 and I1 when S is 1'b1. The Structure Block Diagram is shown below. GTP_MUX2LUT7 is used to select the outputs of two LUT6s to form a single LUT7, thus it must be used in conjunction with LUT6.

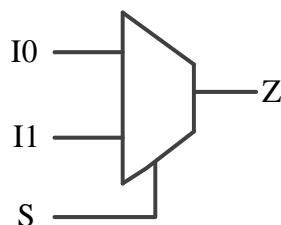


Figure 4-15 GTP_MUX2LUT7 Structure Diagram

4.15.3 Port Description

Table 4-49 GTP_MUX2LUT7 Ports

Port	Direction	Function Description
I0	Input	Input Signal
I1	Input	Input Signal
S	Input	Selection signal
Z	Output	Output signal

4.15.4 Instantiation Template

```
GTP_MUX2LUT7 GTP_MUX2LUT7_inst (
    .Z(lut7_out),
    .I0(lut6a_out),
    .I1(lut6b_out),
    .S(i6)
);
```

4.16 GTP_MUX2LUT8

4.16.1 Supported Devices

Table 4-50 GTP_MUX2LUT8-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

4.16.2 Description of Functionality

GTP_MUX2LUT8 is a dual-input selector dedicated to GTP_LUT8, where I0 and I1 are data inputs, and S is the selection signal. It outputs I0 when S is 1'b0 and I1 when S is 1'b1. The Structure Block Diagram is shown below. GTP_MUX2LUT8 is used to select the outputs of two LUT7s to form a single LUT8, thus it must be used in conjunction with LUT7.

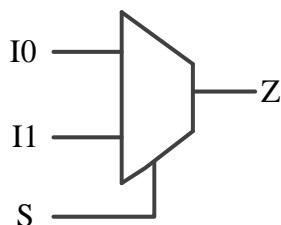


Figure 4-16 GTP_MUX2LUT8 Structure Diagram

4.16.3 Port Description

Table 4-51 GTP_MUX2LUT8 Ports

Port	Direction	Function Description
I0	Input	Input Signal
I1	Input	Input Signal
S	Input	Selection signal
Z	Output	Output signal

4.16.4 Instantiation Template

```
GTP_MUX2LUT8 GTP_MUX2LUT8_inst (
    .Z(lut8_out),
    .I0(lut7ab_out),
    .I1(lut7cd_out),
    .S(i7)
);
```

Chapter 5 Usage Instructions for ROM and RAM Related GTPs

5.1 GTP_ROM32X1

5.1.1 Supported Devices

Table 5-1 GTP_ROM32X1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.1.2 Description of Functionality

GTP_ROM32X1 is a storage ROM with an address depth of 32 bits and a data width of 1 bit. The Structure Block Diagram is shown below.

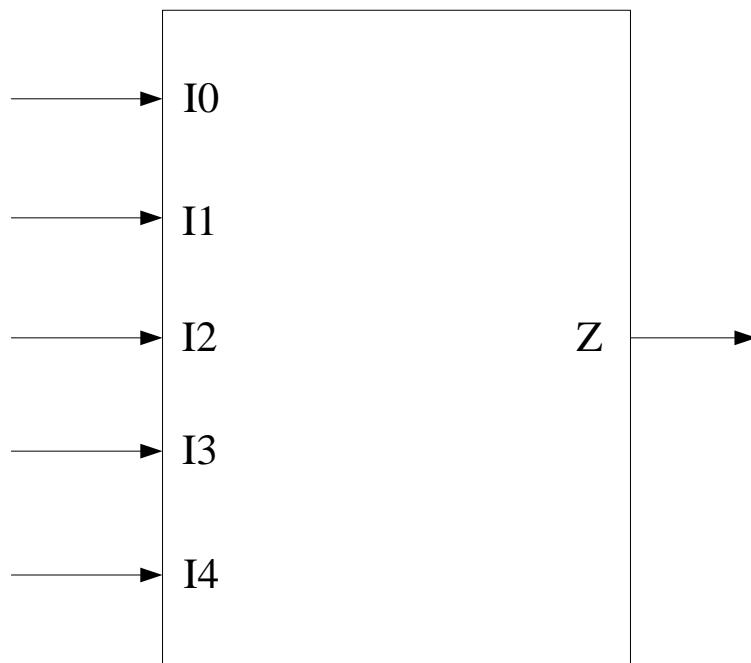


Figure 5-1 GTP_ROM32X1 Structure Block Diagram

5.1.3 Port Description

Table 5-2 GTP_ROM32X1 Port List

Port	Direction	Function Description
I0	Input	ROM read address addr[0]
I1	Input	ROM read address addr[1]
I2	Input	ROM read address addr[2]
I3	Input	ROM read address addr[3]
I4	Input	ROM read address addr[4]
Z	Output	Read data

5.1.4 Paramater Description

Table 5-3 GTP_ROM32X1 Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Description
INIT	<binary>	32'h00000000~32'hffffffffff	32'h00000000	ROM Initialization Configuration Parameters

5.1.5 Instantiation Template

```
GTP_ROM32X1 #(  
    .INIT      (32'h00000000)  
);  
  
GTP_ROM32X1_inst(  
    .I0      (i0),  
    .I1      (ii),  
    .I2      (i2),  
    .I3      (i3),  
    .I4      (i4),  
    .Z       (z )  
);
```

5.1.6 Detailed Functional Description

This GTP implements the ROM storage function. Inputs I4~I0 form the address for reading the value of the specified bit of the ROM's Initialization Configuration Parameters.

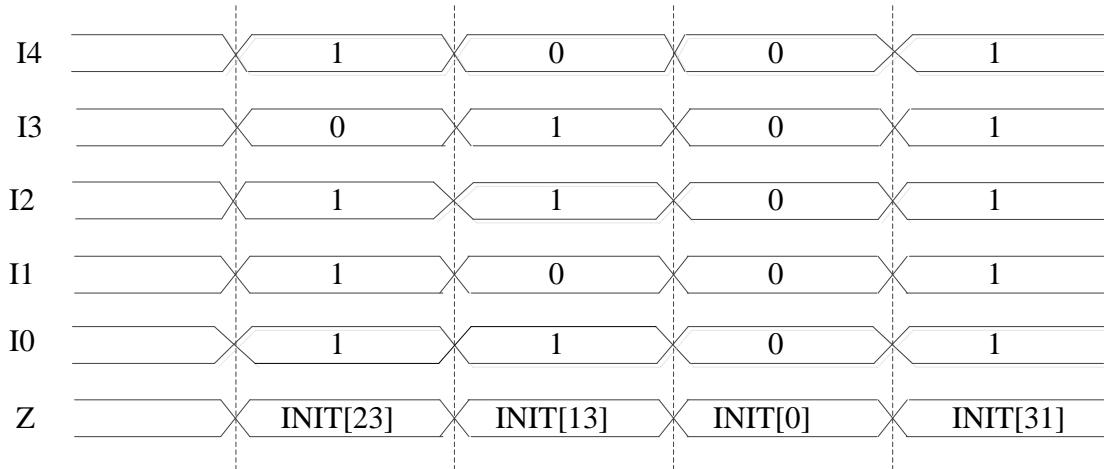


Figure 5-2 GTP_ROM32X1 Waveform Diagram

5.2 GTP_ROM32X2

5.2.1 Supported Devices

Table 5-4 GTP_ROM32X2-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.2.2 Description of Functionality

GTP_ROM32X2 is a storage ROM with an address depth of 32 bits and a data width of 2 bits. The Structure Block Diagram is shown as below:

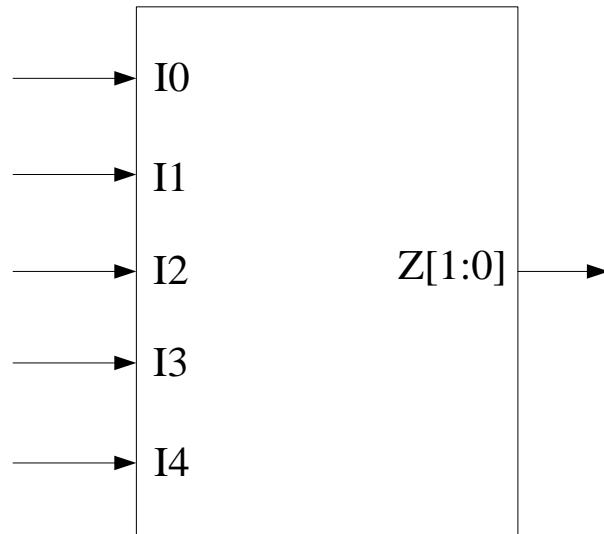


Figure 5-3 GTP_ROM32X2 Structure Block Diagram

5.2.3 Port Description

Table 5-5 GTP_ROM32X2 Port List

Port	Direction	Function Description
I0	Input	ROM read address addr[0]
I1	Input	ROM read address addr[1]
I2	Input	ROM read address addr[2]
I3	Input	ROM read address addr[3]
I4	Input	ROM read address addr[4]
Z	Output	Read data

5.2.4 Parameter Description

Table 5-6 GTP_ROM32X2 Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Description
INIT_0	<binary>	32'h0~32'hffffffff	32'h0	ROM Initialization Configuration Parameters
INIT_1	<binary>	32'h0~32'hffffffff	32'h0	ROM Initialization Configuration Parameters

5.2.5 Instantiation Template

```

GTP_ROM32X2 #(

.INIT_0      (32'h00000000),
.INIT_1      (32'h00000000)

)

GTP_ROM32X2_inst(
.I0      (i0),
.I1      (ii),
.I2      (i2),
.I3      (i3),
.I4      (i4),
.Z       (z )
);
    
```

5.2.6 Detailed Functional Description

This GTP implements the ROM storage function. Inputs I4~I0 form the address for reading the value of the specified bit of the ROM's Initialization Configuration Parameters.

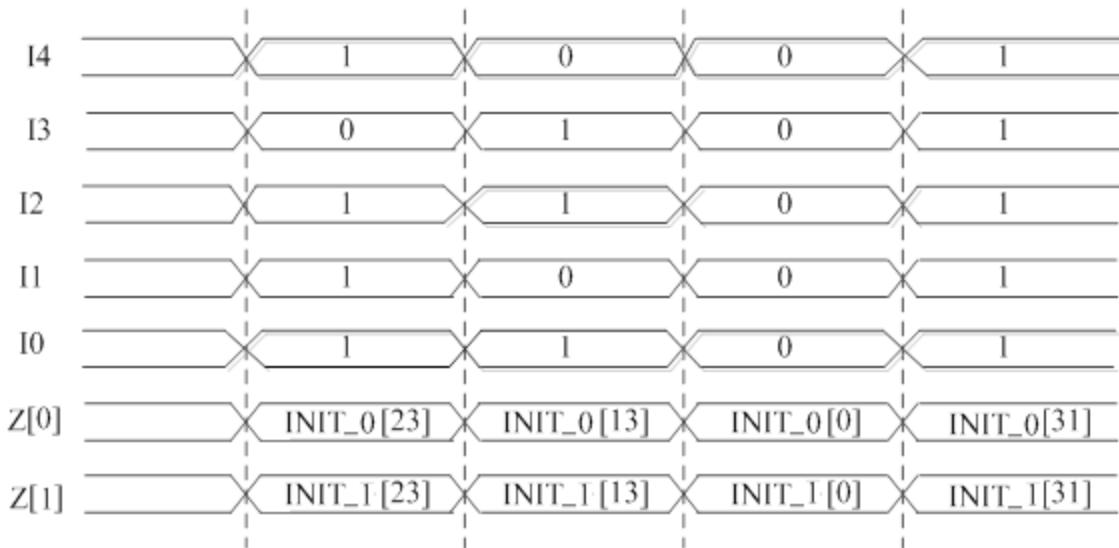


Figure 5-4 GTP_ROM32X2 Waveform Diagram

5.3 GTP_ROM64X1

5.3.1 Supported Devices

Table 5-7 GTP_ROM64X1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.3.2 Description of Functionality

GTP_ROM64X1 is a storage ROM with an address depth of 64 bits and a data width of 1 bit. The Structure Block Diagram is shown below.

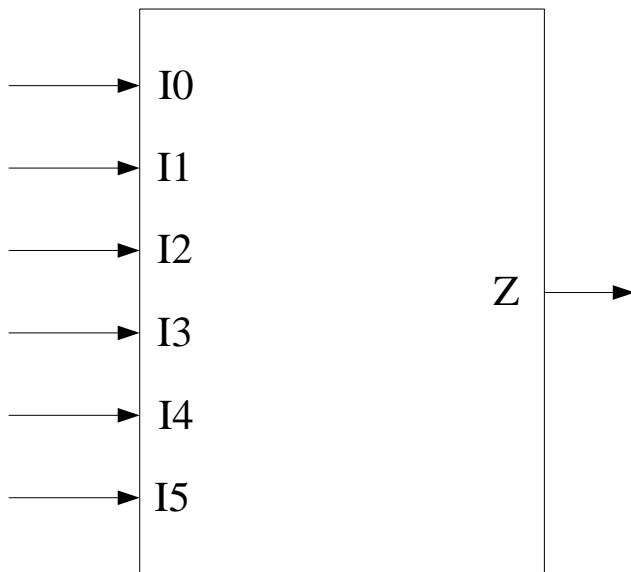


Figure 5-5 GTP_ROM64X1 Structure Block Diagram

5.3.3 Port Description

Table 5-8 GTP_ROM64X1 Port List

Port	Direction	Function Description
I0	Input	ROM read address addr[0]
I1	Input	ROM read address addr[1]
I2	Input	ROM read address addr[2]
I3	Input	ROM read address addr[3]
I4	Input	ROM read address addr[4]
I5	Input	ROM read address addr[5]
Z	Output	Read data

5.3.4 Parameter Description

Table 5-9 GTP_ROM64X1 Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
INIT	<binary>	64'h0~64'hfffffff_ffffffff	64'h0	ROM Initialization Configuration Parameters

5.3.5 Instantiation Template

```
GTP_ROM64X1#(
    .INIT      (64'h00000000_00000000),
)
GTP_ROM64X1_inst(
    .I0      (i0),
    .I1      (ii),
    .I2      (i2),
    .I3      (i3),
    .I4      (i4),
    .I5      (i5),
    .Z       (z )
);
```

5.3.6 Detailed Functional Description

This GTP implements the ROM storage function. Inputs I5~I0 form the address for reading the value of the specified bit of the ROM's Initialization Configuration Parameters.

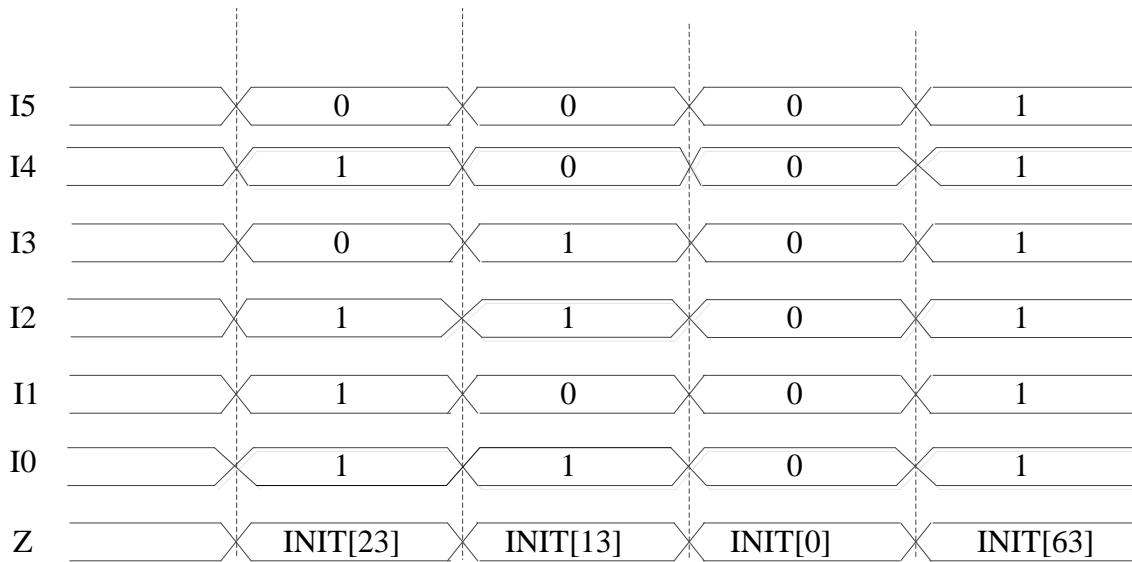


Figure 5-6 GTP_ROM64X1 Waveform Diagram

5.4 GTP_ROM128X1

5.4.1 Supported Devices

Table 5-10 GTP_ROM128X1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.4.2 Description of Functionality

GTP_ROM128X1 is a storage ROM with an address depth of 128 bits and a data width of 1 bit. The Structure Block Diagram is shown below.

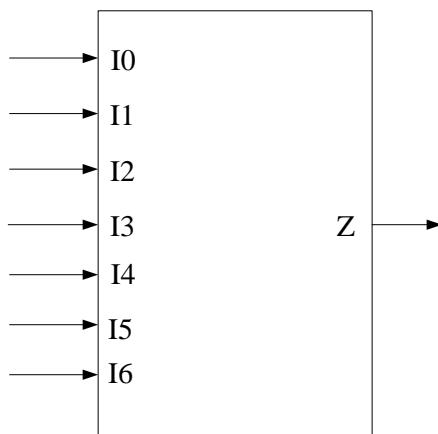


Figure 5-7 GTP_ROM128X1 Structure Block Diagram

5.4.3 Port Description

Table 5-11 GTP_ROM128X1 Port List

Port	Direction	Function Description
I0	Input	ROM read address addr[0]
I1	Input	ROM read address addr[1]
I2	Input	ROM read address addr[2]
I3	Input	ROM read address addr[3]
I4	Input	ROM read address addr[4]
I5	Input	ROM read address addr[5]
I6	Input	ROM read address addr[6]
Z	Output	Read data

5.4.4 Parameter Description

Table 5-12 GTP_ROM128X1 Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
INIT	<binary>	128'h00000000_00000000_000000 00_00000000~128'hfffffff_ffffff fffffff_fffffff	128'h00000000_00000000 0_00000000_00000000	ROM Initialization Configuration Parameters

5.4.5 Instantiation Template

```
GTP_ROM128X1 #(
    .INIT      (128'h00000000_00000000_00000000_00000000)
)
GTP_ROM128X1_inst(
    .I0      (i0),
    .I1      (ii),
    .I2      (i2),
    .I3      (i3),
    .I4      (i4),
    .I5      (i5),
    .I6      (i6),
    .Z       (z )
);
```

5.4.6 Detailed Functional Description

This GTP implements the ROM storage function. Inputs I6~I0 form the address for reading the value of the specified bit of the ROM's Initialization Configuration Parameters.

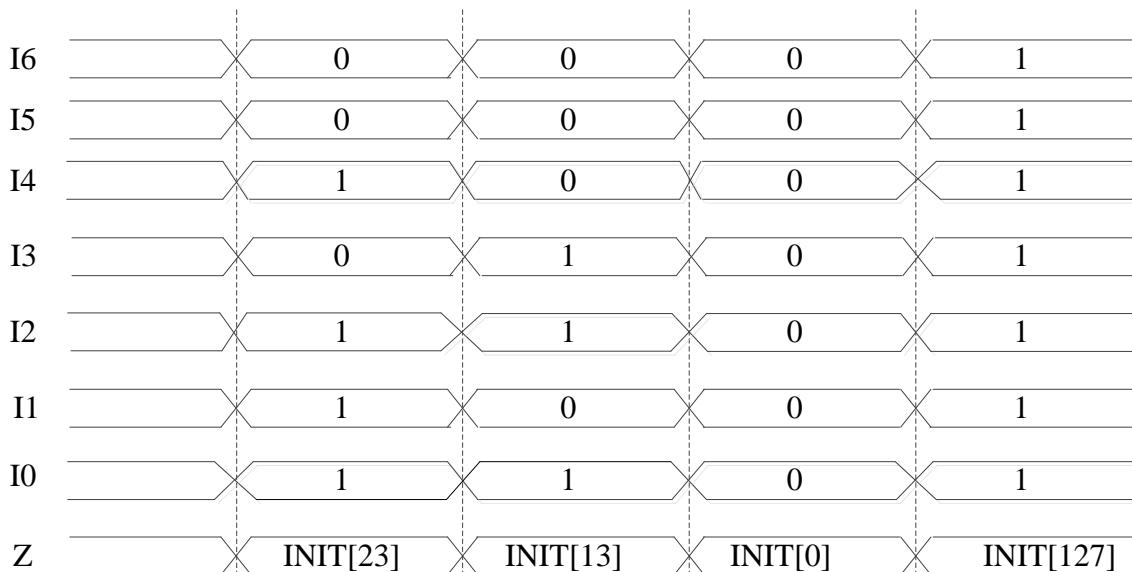


Figure 5-8 GTP_ROM128X1 Waveform Diagram

5.5 GTP_ROM256X1

5.5.1 Supported Devices

Table 5-13 GTP_ROM256X1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.5.2 Description of Functionality

GTP_ROM256X1 is a storage ROM with an address depth of 256 bits and a data width of 1 bit. The Structure Block Diagram is shown below.

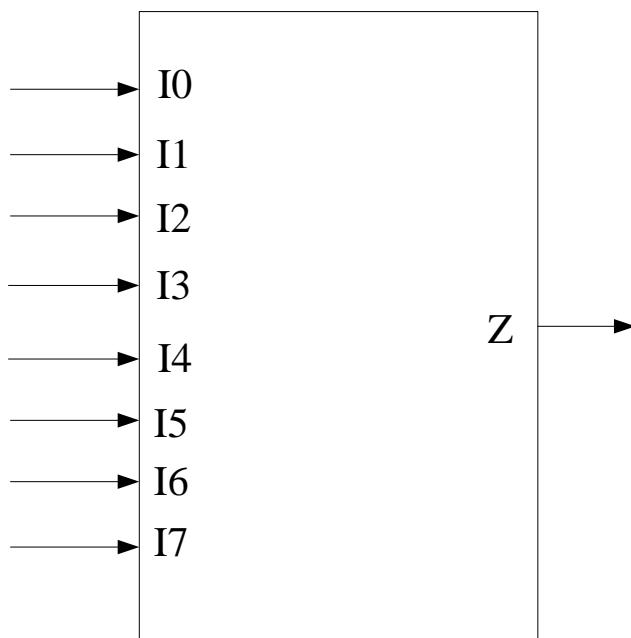


Figure 5-9 GTP_ROM256X1 Structure Block Diagram

5.5.3 Port Description

Table 5-14 GTP_ROM256X1 Port List

Port	Direction	Function Description
I0	Input	ROM read address addr[0]
I1	Input	ROM read address addr[1]
I2	Input	ROM read address addr[2]
I3	Input	ROM read address addr[3]
I4	Input	ROM read address addr[4]
I5	Input	ROM read address addr[5]
I6	Input	ROM read address addr[6]
I7	Input	ROM read address addr[7]
Z	Output	Read data

5.5.4 Parameter Description

Table 5-15 GTP_ROM256X1 Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
INIT	<binary>	256'h0~256'hffffffff_ffffffff_ffffffff_ffffffff_f fffff_fffff_fffff_fffff	256'h0	ROM Initialization Configuration Parameters

5.5.5 Instantiation Template

```
GTP_ROM256X1 #(
```

```
.INIT (256'h0)
```

```
)
```

```
GTP_ROM256X1_inst(
```

```
.I0 (i0),
```

```
.I1 (ii),
```

```
.I2 (i2),
```

```
.I3 (i3),
```

```
.I4 (i4),
```

```
.I5 (i5),
```

```
.I6 (i6),
```

```
.I7 (i7),
```

```
.Z (z )
```

```
);
```

5.5.6 Detailed Functional Description

This GTP implements the ROM storage function. Inputs I7–I0 constitute the address, reading the value of the specified bit of the ROM's initial configuration parameters.

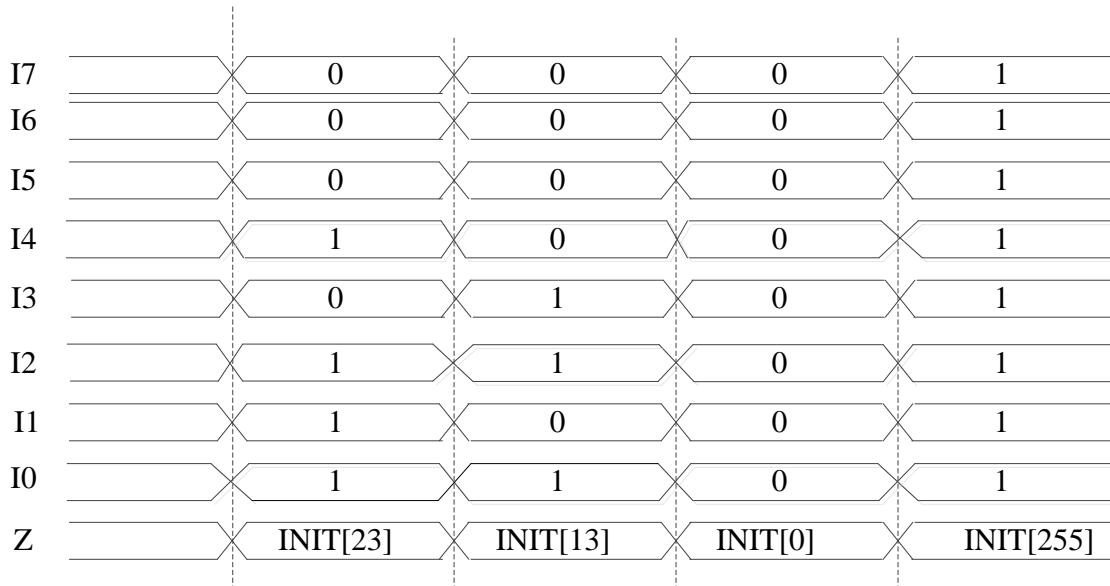


Figure 5-10 GTP_ROM256X1 Waveform Diagram

5.6 GTP_RAM32X1SP

5.6.1 Supported Devices

Table 5-16 GTP_RAM32X1SP-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.6.2 Description of Functionality

GTP_RAM32X1SP is a single-port random storage module with a data width of 1 bit and an address depth of 32 bits. The Structure Block Diagram is shown below.

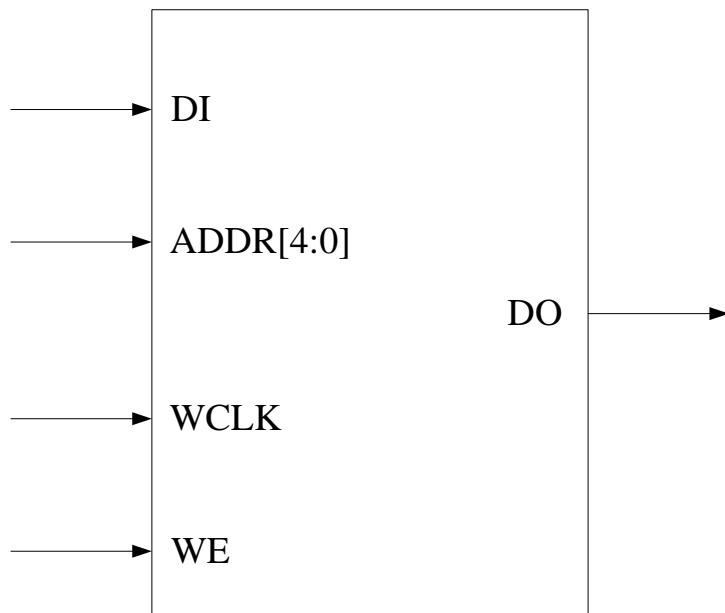


Figure 5-11 GTP_RAM32X1SP Structure Block Diagram

5.6.3 Port Description

Table 5-17 GTP_RAM32X1SP Port List

Port	Direction	Function Description
DI	Input	Data input ports
ADDR	Input	Read/write address
WCLK	Input	Write clock
WE	Input	Write enable
DO	Output	Data output ports

5.6.4 Parameter Description

Table 5-18 GTP_RAM32X1SP Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
INIT	<binary>	32'h0~32'hffffffff	32'h0	Memory initialization configuration parameters

5.6.5 Instantiation Template

```
GTP_RAM32X1SP#(
    .INIT      (32'h00000000),
    )
GTP_RAM32X1SP_inst(
    .DO      (do  ),
    .DI      (di  ),
    .ADDR    (addr ),
    .WCLK    (wclk ),
    .WE      (we  )
);
```

5.6.6 Detailed Functional Description

For detailed functions of this GTP, please refer to the "***UG040001_Logos2 Family FPGAs Configurable Logic Module (CLM) User Guide***".

5.7 GTP_RAM32X1DP

5.7.1 Supported Devices

Table 5-19 GTP_RAM32X1DP-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.7.2 Description of Functionality

GTP_RAM32X1DP is a dual-port random storage module with a data width of 1 bit and an address depth of 32, with read/write addresses input through two separate ports. The Structure Block Diagram is shown below.

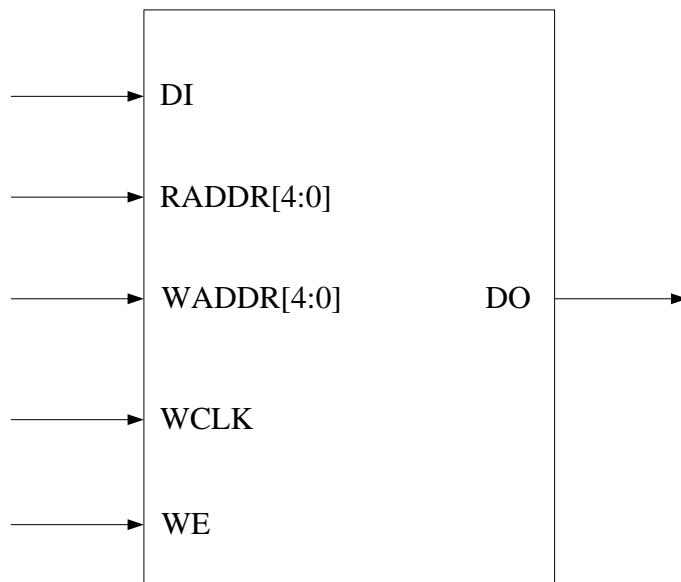


Figure 5-12 GTP_RAM32X1DP Structure Block Diagram

5.7.3 Port Description

Table 5-20 GTP_RAM32X1DP Port List

Port	Direction	Function Description
DI	Input	Data input ports
RADDR	Input	Read address
WADDR	Input	Write address
WCLK	Input	Write clock
WE	Input	Write enable
DO	Output	Data output ports

5.7.4 Parameter Description

Table 5-21 GTP_RAM32X1DP Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
INIT	<binary>	32'h0~32'hffffffff	32'h0	Memory initialization configuration parameters

5.7.5 Instantiation Template

```
GTP_RAM32X1DP #(  
    .INIT      (32'h0  ),  
    )  
GTP_RAM32X1DP_inst(  
    .DO       (do      ),  
    .DI       (di      ),  
    .RADDR   (raddr   ),  
    .WADDR   (waddr   ),  
    .WCLK    (wclk   ),  
    .WE      (we     )  
)
```

5.7.6 Detailed Functional Description

For detailed functions of this GTP, please refer to the "***UG040001_Logos2 Family FPGAs Configurable Logic Module (CLM) User Guide***".

5.8 GTP_RAM32X2SP

5.8.1 Supported Devices

Table 5-22 GTP_RAM32X2SP-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.8.2 Description of Functionality

GTP_RAM32X2SP is a single-port random storage module with a data width of 2 bits and an address depth of 32 bits. The Structure Block Diagram is shown below.

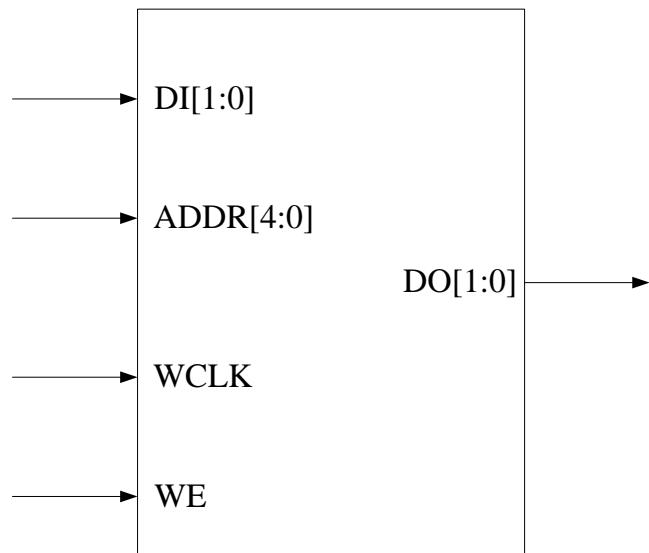


Figure 5-13 GTP_RAM32X2SP Structure Block Diagram

5.8.3 Port Description

Table 5-23 GTP_RAM32X2SP Port List

Port	Direction	Function Description
DI[1:0]	Input	Data input ports
ADDR	Input	Read/write address
WCLK	Input	Write clock
WE	Input	Write enable
DO[1:0]	Output	Data output ports

5.8.4 Parameter Description

Table 5-24 GTP_RAM32X2SP Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
INIT_0	<binary>	32'h0~32'hffffffff	32'h0	Memory initialization configuration parameters
INIT_1	<binary>	32'h0~32'hffffffff	32'h0	Memory initialization configuration parameters

5.8.5 Instantiation Template

```
GTP_RAM32X2SP#(  
    .INIT_0(32'h0),  
    .INIT_1(32'h0)  
)  
  
GTP_RAM32X2SP_inst(  
    .DO      (do      ),  
    .DI      (di      ),  
    .ADDR    (addr   ),  
    .WCLK    (wclk   ),  
    .WE      (we      )  
)
```

5.9 GTP_RAM32X2DP

5.9.1 Supported Devices

Table 5-25 GTP_RAM32X2DP-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.9.2 Description of Functionality

GTP_RAM32X2DP is a dual-port random storage module with a data width of 2 bits and an address depth of 32, with read/write addresses input through two separate ports. The Structure Block Diagram is shown below.

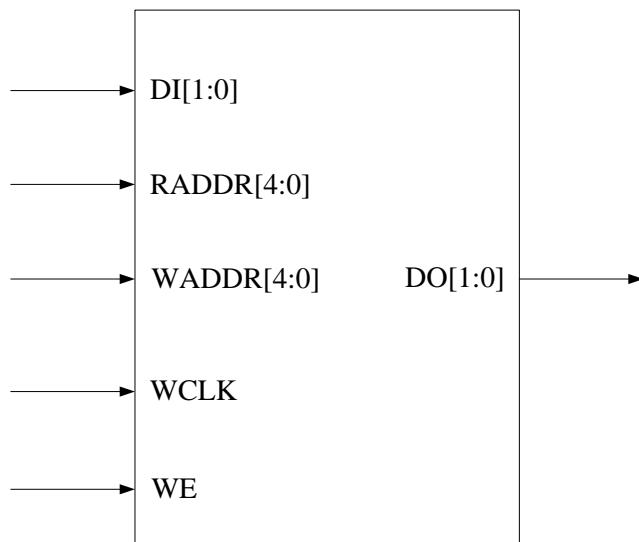


Figure 5-14 GTP_RAM32X2DP Structure Block Diagram

5.9.3 Port Description

Table 5-26 GTP_RAM32X2DP Port List

Port	Direction	Function Description
DI	Input	Data input ports
RADDR	Input	Read address
WADDR	Input	Write address
WCLK	Input	Write clock
WE	Input	Write enable
DO	Output	Data output ports

5.9.4 Parameter Description

Table 5-27 GTP_RAM32X2DP Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
INIT_0	<binary>	32'h0~32'hffffffff	32'h0	Memory initialization configuration parameters
INIT_1	<binary>	32'h0~32'hffffffff	32'h0	Memory initialization configuration parameters

5.9.5 Instantiation Template

```
GTP_RAM32X2DP #(  
    .INIT_0      (32'h0  ),  
    .INIT_1      (32'h0  )  
)  
  
GTP_RAM32X2DP_inst(  
    .DO          (do      ),  
    .DI          (di      ),  
    .RADDR       (raddr   ),  
    .WADDR       (waddr   ),  
    .WCLK        (wclk   ),  
    .WE          (we      ))  
);
```

5.10 GTP_RAM64X1SP

5.10.1 Supported Devices

Table 5-28 GTP_RAM64X1SP-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.10.2 Description of Functionality

GTP_RAM64X1SP is a single-port random storage module with a data width of 1 bits and an address depth of 64 bits. The Structure Block Diagram is shown below.

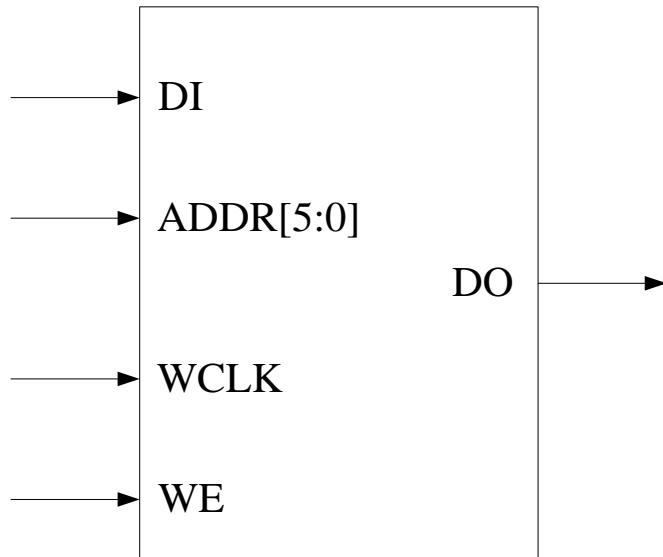


Figure 5-15 GTP_RAM64X1SP Structure Block Diagram

5.10.3 Port Description

Table 5-29 GTP_RAM64X1SP Port List

Port	Direction	Function Description
DI	Input	WRITE DATA
ADDR	Input	Write address
WCLK	Input	Write clock
WE	Input	Write enable
DO	Output	Read data

5.10.4 Parameter Description

Table 5-30 GTP_RAM64X1SP Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
INIT	<binary>	64'h0~64'hffffffffffff	64'h0	Memory initialization configuration parameters

5.10.5 Instantiation Template

```
GTP_RAM64X1SP#(
    .INIT      (64'h0  ),
    )
GTP_RAM64X1SP_inst(
    .DO       (do      ),
    .DI       (di      ),
    .ADDR     (addr    ),
    .WCLK     (wclk   ),
    .WE       (we      )
);
```

5.10.6 Detailed Functional Description

For detailed functions of this GTP, please refer to the "***UG040001_Logos2 Family FPGAs Configurable Logic Module (CLM) User Guide***".

5.11 GTP_RAM64X1DP

5.11.1 Supported Devices

Table 5-31 GTP_RAM64X1DP-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.11.2 Description of Functionality

GTP_RAM64X1DP is a dual-port random storage module with a data width of 1 bit and an address depth of 64 bits, with read/write addresses input through two separate ports. The Structure Block Diagram is shown below.

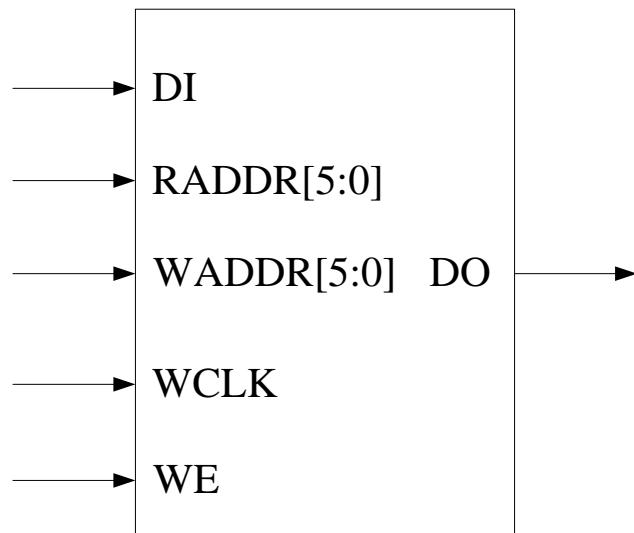


Figure 5-16 GTP_RAM64X1DP Structure Block Diagram

5.11.3 Port Description

Table 5-32 GTP_RAM64X1DP Port List

Port	Direction	Function Description
DI	Input	WRITE DATA
RADDR	Input	Read address
WADDR	Input	Write address
WCLK	Input	Write clock
WE	Input	Write enable
DO	Output	Read data

5.11.4 Parameter Description

Table 5-33 GTP_RAM64X1DP Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
INIT	<binary>	64'h0~64'hffffffffffff	64'h00000000	Memory initialization configuration parameters

5.11.5 Instantiation Template

```
GTP_RAM64X1DP #(  
    .INIT      (64'h0)  
);  
  
GTP_RAM64X1DP_inst(  
    .DO      (do      ),  
    .DI      (di      ),  
    .RADDR   (raddr   ),  
    .WADDR   (waddr   ),  
    .WCLK    (wclk    ),  
    .WE      (we      )  
)
```

5.11.6 Detailed Functional Description

For detailed functions of this GTP, please refer to the "***UG040001_Logos2 Family FPGAs Configurable Logic Module (CLM) User Guide***".

5.12 GTP_RAM128X1SP

5.12.1 Supported Devices

Table 5-34 GTP_RAM128X1SP-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.12.2 Description of Functionality

GTP_RAM128X1SP is a single-port random storage module with a data width of 1 bit and an address depth of 128 bits. The Structure Block Diagram is shown below.

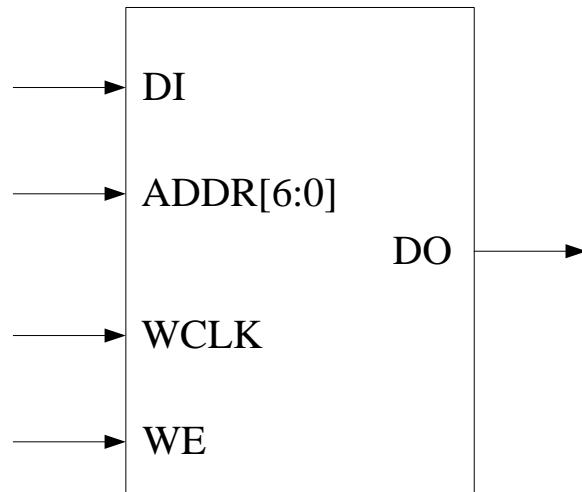


Figure 5-17 GTP_RAM128X1SP Structure Block Diagram

5.12.3 Port Description

Table 5-35 GTP_RAM128X1SP Port List

Port	Direction	Function Description
DI	Input	WRITE DATA
ADDR	Input	Write address
WCLK	Input	Write clock
WE	Input	Write enable
DO	Output	Read data

5.12.4 Parameter Description

Table 5-36 GTP_RAM128X1SP Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
INIT	<binary>	128'h0~128'hffffffffffff...ffff	128'h0	Memory initialization configuration parameters

5.12.5 Instantiation Template

```
GTP_RAM128X1SP#(
    .INIT      (128'h0),
    )
GTP_RAM128X1SP_inst(
    .DO      (do      ),
    .DI      (di      ),
    .ADDR    (addr    ),
    .WCLK    (wclk    ),
    .WE      (we      )
);
```

5.12.6 Detailed Functional Description

For detailed functions of this GTP, please refer to the "***UG040001_Logos2 Family FPGAs Configurable Logic Module (CLM) User Guide***".

5.13 GTP_RAM128X1DP

5.13.1 Supported Devices

Table 5-37 GTP_RAM128X1DP-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.13.2 Description of Functionality

GTP_RAM128X1DP is a dual-port random storage module with a data width of 1 bit and an address depth of 128 bits, with read/write addresses input through two separate ports. The Structure Block Diagram is shown below.

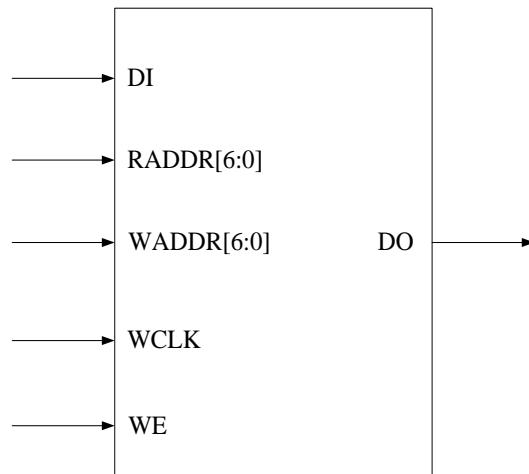


Figure 5-18 GTP_RAM128X1DP Structure Block Diagram

5.13.3 Port Description

Table 5-38 GTP_RAM128X1DP Port List

Port	Direction	Function Description
DI	Input	WRITE DATA
RADDR	Input	Read address
WADDR	Input	Write address
WCLK	Input	Write clock
WE	Input	Write enable
DO	Output	Read data

5.13.4 Paramater Description

Table 5-39 GTP_RAM128X1DP Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
INIT	<binary>	128'h0~128'hffffffffffff...ffff	128'h0	Memory initialization configuration parameters

5.13.5 Instantiation Template

```
GTP_RAM128X1DP #(  
    .INIT      (128'h0)  
);  
  
GTP_RAM128X1DP_inst(  
    .DO        (do      ),  
    .DI        (di      ),  
    .RADDR     (raddr   ),  
    .WADDR     (waddr   ),  
    .WCLK      (wclk   ),  
    .WE        (we      )  
);
```

5.13.6 Detailed Functional Description

For detailed functions of this GTP, please refer to the "**"UG040001_Logos2 Family FPGAs Configurable Logic Module (CLM) User Guide"**".

5.14 GTP_RAM256X1SP

5.14.1 Supported Devices

Table 5-40 GTP_RAM256X1SP-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.14.2 Description of Functionality

GTP_RAM256X1SP is a single-port random storage module with a data width of 1 bit and an address depth of 256 bits. The Structure Block Diagram is shown below.

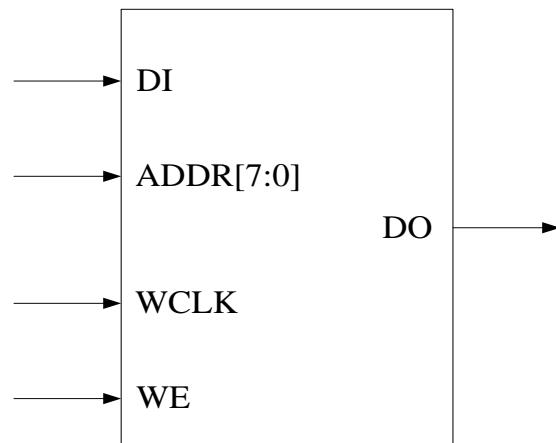


Figure 5-19 GTP_RAM256X1SP Structure Block Diagram

5.14.3 Port Description

Table 5-41 GTP_RAM256X1SP Port List

Port	Direction	Function Description
DI	Input	WRITE DATA
ADDR	Input	Write address
WCLK	Input	Write clock
WE	Input	Write enable
DO	Output	Read data

5.14.4 Parameter Description

Table 5-42 GTP_RAM256X1SP Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
INIT	<binary>	256'h0~256'hffffffffffff...ffff	128'h0	Memory initialization configuration parameters

5.14.5 Instantiation Template

```
GTP_RAM256X1SP#(
    .INIT      (256'h0),
    )
GTP_RAM256X1SP_inst(
    .DO      (do      ),
    .DI      (di      ),
    .ADDR    (addr    ),
    .WCLK    (wclk    ),
    .WE      (we      )
);
```

5.14.6 Detailed Functional Description

For detailed functions of this GTP, please refer to the "***UG040001_Logos2 Family FPGAs Configurable Logic Module (CLM) User Guide***".

5.15 GTP_DRM36K_E1

5.15.1 Supported Devices

Table 5-43 GTP_DRM36K_E1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.15.2 Description of Functionality

GTP_DRM36K_E1 has 36K bits storage units, with various operating modes including True Dual Port (DP) RAM, Simple Dual Port (SDP) RAM, Single Port (SP) RAM or ROM mode. The DRM supports configurable bit width and dual-port mixed bit width in both DP RAM and SDP RAM modes. The Structure Block Diagram is shown below.

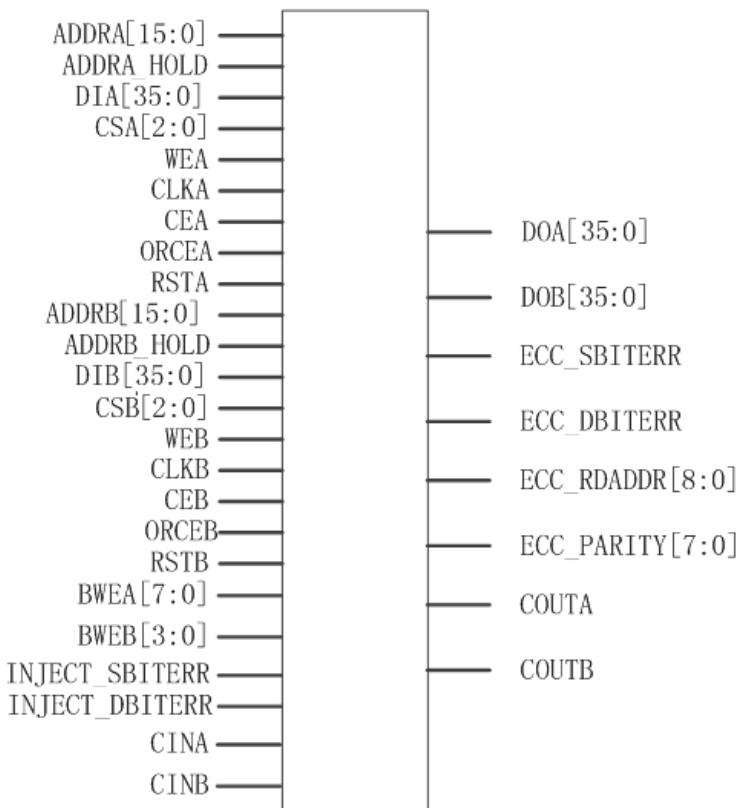


Figure 5-20 GTP_DRM36K_E1 Structure Block Diagram

5.15.3 Port Description

Table 5-44 GTP_DRM36K_E1 Port List

Port	Direction	Function Description
ADDRA	Input	Port A input address
ADDRA_HOLD	Input	Port A address input selection
DIA	Input	Port A data input bus
CSA	Input	Port A address extension
WEA	Input	Port A write enable
BWEA	Input	Port A byte write enable
CLKA	Input	Port A clock
CEA	Input	Port A clock enable
ORCEA	Input	Port A output register enable
RSTA	Input	Port A data register reset

Port	Direction	Function Description
DOA	Output	Port A data output bus
ADDRB	Input	Port B input address
ADDRB_HOLD	Input	Port B address input selection
DIB	Input	Port B data input bus
CSB	Input	Port B address extension
WEB	Input	Port B write enable
BWEB	Input	Port B byte write enable
CLKB	Input	Port B clock
CEB	Input	Port B clock enable
ORCEB	Input	Port B output register enable
RSTB	Input	Port B data register reset
CINA	Input	Cascade input of adjacent Port DRM A data output
CINB	Input	Cascade input of adjacent Port DRM B data output
INJECT_SBITERR	Input	Single-bit error injection in ECC mode
INJECT_DBITERR	Input	ECC mode double-bit error insertion
DOB	Output	Port B data output bus
COUTA	Output	Cascade output of adjacent Port DRM A data output
COUTB	Output	Cascade output of adjacent Port DRM B data output
ECC_SBITERR	Output	Single-bit error flag in ECC mode
ECC_DBITERR	Output	Dual-bit error flag in ECC mode
ECC_PARITY[7:0]	Output	ECC encode checksum bit output
ECC_RDADDR[8:0]	Output	ECC decode read address output

5.15.4 Paramater Description

Table 5-45 GTP_DRM36K_E1 Parameter List

Parameter Name	Function Description	Setting Value	Defaults
CSA_MASK[2:0]	Port A address extension control signal	0 ~ 7	3'b000
CSB_MASK[2:0]	Port B address extension control signal	0 ~ 7	3'b000
DATA_WIDTH_A	Data width of Port A	1, 2, 4, 8, 16, 32, 9, 18, 36, 64, 72	18
DATA_WIDTH_B	Data width of Port B	1, 2, 4, 8, 16, 32, 9, 18, 36, 64, 72	18
WRITE_MODE_A	Port A write mode	NORMAL_WRITE TRANSPARENT_WRITE READ_BEFORE_WRITE	"NORMAL_WRITE"
WRITE_MODE_B	Port B write mode	NORMAL_WRITE TRANSPARENT_WRITE READ_BEFORE_WRITE	"NORMAL_WRITE"

Parameter Name	Function Description	Setting Value	Defaults
DOA_REG	Port A output register	0 = Do not enable output register 1 = Enable output register	0
DOB_REG	Port B output register	0 = Do not enable output register 1 = Enable output register	0
RST_TYPE	Reset mode selection	SYNC: Synchronous reset ASYNC: Asynchronous reset	"SYNC"
RAM_MODE	RAM mode selection	TRUE_DUAL_PORT: Dual-port RAM SIMPLE_DUAL_PORT: Simple dual-port RAM SINGLE_PORT: Single-port RAM ROM: ROM	"TRUE_DUAL_PORT"
GRS_EN	Global reset enable signal (Internal Chip)	FALSE: Global Reset not enabled. TRUE: Global Reset enabled.	"TRUE"
DOA_REG_CLKINV	Port A output register clock inversion	0 = Clock not inverted 1 = Clock inverted	0
DOB_REG_CLKINV	Port B output register clock inversion	0 = Clock not inverted 1 = Clock inverted	0
RSTA_VAL	Port A output set/reset value	36'h0_0000_0000~36'hF_FFFF_FFFF	36'b0
RSTB_VAL	Port B output set/reset value	36'h0_0000_0000~36'hF_FFFF_FFFF	36'b0
RAM CASCADE	64Kx1 hard cascade mode	"NONE": No hard cascade "UPPER": Serves as a hard cascade data output module "LOWER": Serves as a hard cascade additional module	"NONE"
ECC_WRITE_EN	ECC write mode enable	"FALSE": Not enabled "TRUE": Enabled	"FALSE"
ECC_READ_EN	ECC read mode enable	"FALSE": Not enabled "TRUE": Enabled	"FALSE"
INIT_00 INIT_01 INIT_02 ... INIT_7F	RAM Initialization Configuration Parameters	288'b0 ~2^288-1	288'h0
INIT_FILE	Initialization files	"NONE": No initialization file is specified, and the initialization data will be the value set by the parameter INIT_00~ INIT_7F; "XXX": XXX represents the specific initialization file path	"NONE"
BLOCK_X	Data cascade coordinates when RAM36K is cascaded	Depends on the number of cascaded DRMs	0
BLOCK_Y	Address cascade coordinates when RAM36K is cascaded	Depends on the number of cascaded DRMs	0
RAM_DATA_WIDTH	Maximum data width after RAM is cascaded	Depends on the number of cascaded DRMs	9

Parameter Name	Function Description	Setting Value	Defaults
RAM_ADDR_WIDTH	Maximum address width after RAM is cascaded	Depends on the number of cascaded DRMs	12
INIT_FORMAT	Initialization file format "BIN": Binary "HEX": Hexadecimal	"BIN"	"BIN"

Note: SDP mode does not support read/write mode settings. When configuring DRM to SDP mode using GTP, users cannot manually modify the read/write mode parameter WRITE_MODE_A/B.

5.15.5 Instantiation Template

```
GTP_DRM36K_E1 #(
    .GRS_EN("TRUE"),
    .CSA_MASK(3'b0),
    .CSB_MASK(3'b0),
    .DATA_WIDTH_A(18),
    .DATA_WIDTH_B(18),
    .WRITE_MODE_A("NORMAL_WRITE"),
    .WRITE_MODE_B("NORMAL_WRITE"),
    .DOA_REG(0),
    .DOB_REG(0),
    .DOA_REG_CLKINV(0),
    .DOB_REG_CLKINV(0),
    .RSTA_VAL(36'b0),
    .RSTB_VAL(36'b0),
    .RST_TYPE("SYNC"),
    .RAM_MODE("TRUE_DUAL_PORT"),
    .RAM CASCADE("NONE"),
    .ECC_READ_EN("FALSE"),
    .ECC_WRITE_EN("FALSE"),
    .INIT_00(288'b0),
    .INIT_01(288'b0),
    .INIT_02(288'b0),
    .INIT_03(288'b0),
    .INIT_04(288'b0),
    .INIT_05(288'b0),
    .INIT_06(288'b0),
```

.INIT_07(288'b0),
.INIT_08(288'b0),
.INIT_09(288'b0),
.INIT_0A(288'b0),
.INIT_0B(288'b0),
.INIT_0C(288'b0),
.INIT_0D(288'b0),
.INIT_0E(288'b0),
.INIT_0F(288'b0),
.INIT_10(288'b0),
.INIT_11(288'b0),
.INIT_12(288'b0),
.INIT_13(288'b0),
.INIT_14(288'b0),
.INIT_15(288'b0),
.INIT_16(288'b0),
.INIT_17(288'b0),
.INIT_18(288'b0),
.INIT_19(288'b0),
.INIT_1A(288'b0),
.INIT_1B(288'b0),
.INIT_1C(288'b0),
.INIT_1D(288'b0),
.INIT_1E(288'b0),
.INIT_1F(288'b0),
.INIT_20(288'b0),
.INIT_21(288'b0),
.INIT_22(288'b0),
.INIT_23(288'b0),
.INIT_24(288'b0),
.INIT_25(288'b0),
.INIT_26(288'b0),
.INIT_27(288'b0),
.INIT_28(288'b0),

.INIT_29(288'b0),
.INIT_2A(288'b0),
.INIT_2B(288'b0),
.INIT_2C(288'b0),
.INIT_2D(288'b0),
.INIT_2E(288'b0),
.INIT_2F(288'b0),
.INIT_30(288'b0),
.INIT_31(288'b0),
.INIT_32(288'b0),
.INIT_33(288'b0),
.INIT_34(288'b0),
.INIT_35(288'b0),
.INIT_36(288'b0),
.INIT_37(288'b0),
.INIT_38(288'b0),
.INIT_39(288'b0),
.INIT_3A(288'b0),
.INIT_3B(288'b0),
.INIT_3C(288'b0),
.INIT_3D(288'b0),
.INIT_3E(288'b0),
.INIT_3F(288'b0),
.INIT_40(288'b0),
.INIT_41(288'b0),
.INIT_42(288'b0),
.INIT_43(288'b0),
.INIT_44(288'b0),
.INIT_45(288'b0),
.INIT_46(288'b0),
.INIT_47(288'b0),
.INIT_48(288'b0),
.INIT_49(288'b0),
.INIT_4A(288'b0),

.INIT_4B(288'b0),
.INIT_4C(288'b0),
.INIT_4D(288'b0),
.INIT_4E(288'b0),
.INIT_4F(288'b0),
.INIT_50(288'b0),
.INIT_51(288'b0),
.INIT_52(288'b0),
.INIT_53(288'b0),
.INIT_54(288'b0),
.INIT_55(288'b0),
.INIT_56(288'b0),
.INIT_57(288'b0),
.INIT_58(288'b0),
.INIT_59(288'b0),
.INIT_5A(288'b0),
.INIT_5B(288'b0),
.INIT_5C(288'b0),
.INIT_5D(288'b0),
.INIT_5E(288'b0),
.INIT_5F(288'b0),
.INIT_60(288'b0),
.INIT_61(288'b0),
.INIT_62(288'b0),
.INIT_63(288'b0),
.INIT_64(288'b0),
.INIT_65(288'b0),
.INIT_66(288'b0),
.INIT_67(288'b0),
.INIT_68(288'b0),
.INIT_69(288'b0),
.INIT_6A(288'b0),
.INIT_6B(288'b0),
.INIT_6C(288'b0),

```
.INIT_6D(288'b0),
.INIT_6E(288'b0),
.INIT_6F(288'b0),
.INIT_70(288'b0),
.INIT_71(288'b0),
.INIT_72(288'b0),
.INIT_73(288'b0),
.INIT_74(288'b0),
.INIT_75(288'b0),
.INIT_76(288'b0),
.INIT_77(288'b0),
.INIT_78(288'b0),
.INIT_79(288'b0),
.INIT_7A(288'b0),
.INIT_7B(288'b0),
.INIT_7C(288'b0),
.INIT_7D(288'b0),
.INIT_7E(288'b0),
.INIT_7F(288'b0),
.INIT_FILE("NONE"),
.BLOCK_X(0),
.BLOCK_Y(0),
.RAM_DATA_WIDTH(9),
.RAM_ADDR_WIDTH(12),
.INIT_FORMAT("BIN")
) GTP_DRM36K_E1_inst (
.DOA          (doa          ),
.DOB          (dob          ),
.ECC_PARITY   (ecc_parity   ),
.ECC_RDADDR   (ecc_rdaddr  ),
.ADDRA        (addra        ),
.ADDRB        (addrb        ),
.BWEA         (bwea         ),
.BWEB         (bweb         ),
```

```

.CSA          (csa          ),
.CSB          (csb          ),
.DIA          (dia          ),
.DIB          (dib          ),
.COUTA        (couta        ),
.COUTB        (coutb        ),
.ECC_DBITERR (ecc_dbiterr  ),
.ECC_SBITERR (ecc_sbiterr  ),
.ADDRA_HOLD   (addra_hold   ),
.ADDRB_HOLD   (addrb_hold   ),
.CEA          (cea          ),
.CEB          (ceb          ),
.CINA         (cina         ),
.CINB         (cinb         ),
.CLKA         (clka         ),
.CLKB         (clkb         ),
.INJECT_DBITERR (inject_dbiterr),
.INJECT_SBITERR (inject_sbiterr),
.ORCEA        (orcea        ),
.ORCEB        (orceb        ),
.RSTA         (rsta         ),
.RSTB         (rstb         ),
.WEA          (wea          ),
.WEB          (web          )
);

```

5.16 GTP_DRM18K_E1

5.16.1 Supported Devices

Table 5-46 GTP_DRM18K_E1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.16.2 Description of Functionality

GTP_DRM18K_E1 has 18K bits storage units, with various operating modes including True Dual Port (DP) RAM, Simple Dual Port (SDP) RAM, Single Port (SP) RAM or ROM mode. The DRM supports configurable bit width and dual-port mixed bit width in both DP RAM and SDP RAM modes. The Structure Block Diagram is shown below:

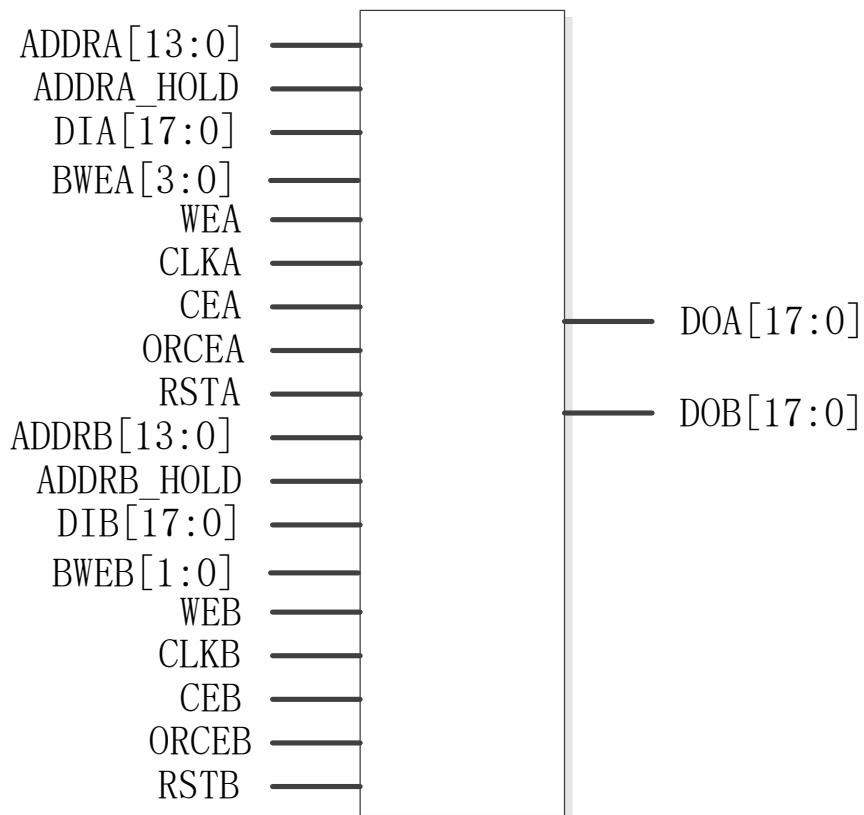


Figure 5-21 GTP_DRM18K_E1 Structure Block Diagram

5.16.3 Port Description

Table 5-47 GTP_DRM18K_E1 Port List

Port	Direction	Function Description
ADDRA	Input	Port A input address
ADDRA_HOLD	Input	Port A address input selection
DIA	Input	Port A data input bus
WEA	Input	Port A write enable
CLKA	Input	Port A clock
CEA	Input	Port A clock enable
ORCEA	Input	Port A output register enable
RSTA	Input	Port A data register reset
BWEA	Input	Port A byte write enable

Port	Direction	Function Description
DOA	Output	Port A data output bus
ADDRB	Input	Port B input address
ADDRB_HOLD	Input	Port B address input selection
DIB	Input	Port B data input bus
WEB	Input	Port B write enable
CLKB	Input	Port B clock
CEB	Input	Port B clock enable
ORCEB	Input	Port B output register enable
RSTB	Input	Port B data register reset
BWEB	Input	Port B byte write enable
DOB	Output	Port B data output bus

5.16.4 Paramater Description

Table 5-48 GTP_DRM18K_E1 Parameter List

Parameter Name	Function Description	Setting Value	Defaults
DATA_WIDTH_A	Data width of Port A	1, 2, 4, 8, 16, 32, 9, 18, 36	18
DATA_WIDTH_B	Data width of Port B	1, 2, 4, 8, 16, 32, 9, 18, 36	18
WRITE_MODE_A	Port A write mode	NORMAL_WRITE TRANSPARENT_WRITE READ_BEFORE_WRITE	NORMAL_WRITE
WRITE_MODE_B	Port B write mode	NORMAL_WRITE TRANSPARENT_WRITE READ_BEFORE_WRITE	NORMAL_WRITE
DOA_REG	Port A output register	0 = Do not enable output register 1 = Enable output register	0
DOB_REG	Port B output register	0 = Do not enable output register 1 = Enable output register	0
RST_TYPE	Reset mode selection	SYNC: Synchronous reset ASYNC: Asynchronous reset	SYNC
RSTA_VAL	Port A output set/reset value	18'h0_0000~18'h3_FFFF	18'b0
RSTB_VAL	Port B output set/reset value	18'h0_0000~18'h3_FFFF	18'b0
RAM_MODE	RAM mode selection	TRUE_DUAL_PORT: Dual-port RAM SIMPLE_DUAL_PORT: Simple dual-port RAM SINGLE_PORT: Single-port RAM ROM: ROM	TRUE_DUAL_PORT
GRS_EN	Global reset enable signal (Internal Chip)	FALSE: Global Reset not enabled. TRUE: Global Reset enabled.	TRUE
DOA_REG_CLKINV	Port A output register clock inversion	0 = Clock not inverted 1 = Clock inverted	0
DOB_REG_CLKINV	Port B output register clock inversion	0 = Clock not inverted 1 = Clock inverted	0

Parameter Name	Function Description	Setting Value	Defaults
INIT_00 INIT_01 INIT_02 ... INIT_3F	RAM Initialization Configuration Parameters	288'b0 ~2^288-1	288'h0
INIT_FILE	Initialization files	"NONE": No initialization file is specified, and the initialization data will be the value set by the parameter INIT_00~ INIT_3F; "XXX": XXX represents the specific initialization file path	"NONE"
BLOCK_X	Data cascade coordinates when RAM18K is cascaded	Depends on the number of cascaded DRMs	0
BLOCK_Y	Address cascade coordinates when RAM18K is cascaded	Depends on the number of cascaded DRMs	0
RAM_DATA_WIDTH	Maximum data width after RAM is cascaded	Depends on the number of cascaded DRMs	9
RAM_ADDR_WIDTH	Maximum address width after RAM is cascaded	Depends on the number of cascaded DRMs	11
INIT_FORMAT	Initialization file format	"BIN": Binary "HEX": Hexadecimal	BIN

Note: SDP mode does not support read/write mode settings. When configuring DRM to SDP mode using GTP, users cannot manually modify the read/write mode parameter WRITE_MODE_A/B.

5.16.5 Instantiation Template

```
GTP_DRM18K_E1 #(
    .GRS_EN("TRUE"),
    .DATA_WIDTH_A(18),
    .DATA_WIDTH_B(18),
    .DOA_REG(0),
    .DOB_REG(0),
    .DOA_REG_CLKINV(0),
    .DOB_REG_CLKINV(0),
    .RSTA_VAL(18'b0),
    .RSTB_VAL(18'b0),
    .RST_TYPE("SYNC"),
    .RAM_MODE("TRUE_DUAL_PORT"),
    .WRITE_MODE_A("NORMAL_WRITE"),
    .WRITE_MODE_B("NORMAL_WRITE"),
    .INIT_00(288'b0),
    .INIT_01(288'b0),
```

.INIT_02(288'b0),
.INIT_03(288'b0),
.INIT_04(288'b0),
.INIT_05(288'b0),
.INIT_06(288'b0),
.INIT_07(288'b0),
.INIT_08(288'b0),
.INIT_09(288'b0),
.INIT_0A(288'b0),
.INIT_0B(288'b0),
.INIT_0C(288'b0),
.INIT_0D(288'b0),
.INIT_0E(288'b0),
.INIT_0F(288'b0),
.INIT_10(288'b0),
.INIT_11(288'b0),
.INIT_12(288'b0),
.INIT_13(288'b0),
.INIT_14(288'b0),
.INIT_15(288'b0),
.INIT_16(288'b0),
.INIT_17(288'b0),
.INIT_18(288'b0),
.INIT_19(288'b0),
.INIT_1A(288'b0),
.INIT_1B(288'b0),
.INIT_1C(288'b0),
.INIT_1D(288'b0),
.INIT_1E(288'b0),
.INIT_1F(288'b0),
.INIT_20(288'b0),
.INIT_21(288'b0),
.INIT_22(288'b0),
.INIT_23(288'b0),

```
.INIT_24(288'b0),  
.INIT_25(288'b0),  
.INIT_26(288'b0),  
.INIT_27(288'b0),  
.INIT_28(288'b0),  
.INIT_29(288'b0),  
.INIT_2A(288'b0),  
.INIT_2B(288'b0),  
.INIT_2C(288'b0),  
.INIT_2D(288'b0),  
.INIT_2E(288'b0),  
.INIT_2F(288'b0),  
.INIT_30(288'b0),  
.INIT_31(288'b0),  
.INIT_32(288'b0),  
.INIT_33(288'b0),  
.INIT_34(288'b0),  
.INIT_35(288'b0),  
.INIT_36(288'b0),  
.INIT_37(288'b0),  
.INIT_38(288'b0),  
.INIT_39(288'b0),  
.INIT_3A(288'b0),  
.INIT_3B(288'b0),  
.INIT_3C(288'b0),  
.INIT_3D(288'b0),  
.INIT_3E(288'b0),  
.INIT_3F(288'b0),  
.INIT_FILE("NONE"),  
.BLOCK_X(0),  
.BLOCK_Y(0),  
.RAM_DATA_WIDTH(9),  
.RAM_ADDR_WIDTH(11),  
.INIT_FORMAT("BIN")
```

```
) GTP_DRM18K_E1_inst (
    .DOA      (doa      ),
    .DOB      (dob      ),
    .ADDRA    (addra    ),
    .ADDRB    (addrb    ),
    .BWEA     (bwea     ),
    .BWEB     (bweb     ),
    .DIA      (dia      ),
    .DIB      (dib      ),
    .ADDRA_HOLD (addra_hold),
    .ADDRB_HOLD (addrb_hold),
    .CEA      (cea      ),
    .CEB      (ceb      ),
    .CLKA     (clka     ),
    .CLKB     (clkb     ),
    .ORCEA    (orcea    ),
    .ORCEB    (orceb    ),
    .RSTA     (rsta     ),
    .RSTB     (rstb     ),
    .WEA      (wea      ),
    .WEB      (web      )
);
```

5.17 GTP_FIFO36K_E1

5.17.1 Supported Devices

Table 5-49 GTP_FIFO36K_E1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.17.2 Description of Functionality

GTP_FIFO36K_E1 supports 36K bits storage units, can be configured various data width mode such as 32K*1, 16K*2, 8K*4, 4K*9(8), 2K*18(16), 1K*36(32) and 512*72(64). GTP_FIFO36K_E1 does not support mixed bit width or byte enable write operations.

When using GTP_FIFO36K_E1, the DRM is configured to SDP mode. One DRM port is dedicated to FIFO data writing, and another is designated for FIFO data reading; in asynchronous FIFO mode, read and write ports can use different clocks.

The structure block diagram is shown below:

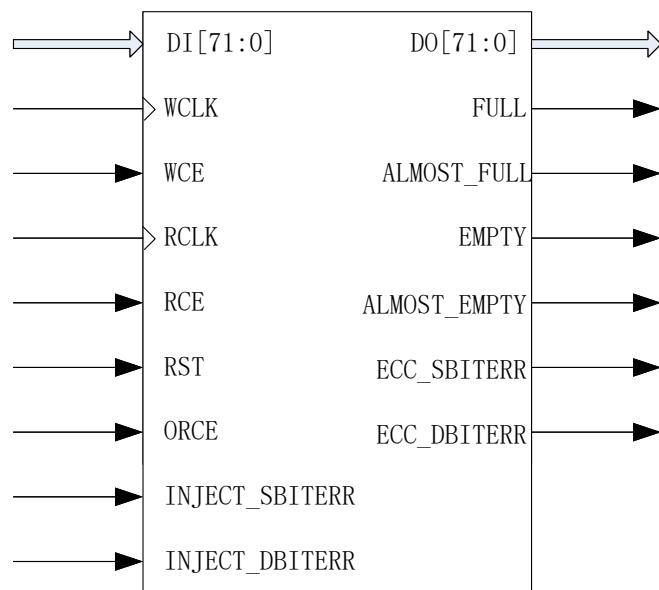


Figure 5-22 GTP_FIFO36K Structure Block Diagram

5.17.3 Port Description

Table 5-50 GTP_FIFO36K_E1 Port List

Port	Direction	Function Description
DI	Input	Data write in
WCLK	Input	Write clock signal
RCLK	Input	Read clock signal
WCE	Input	Write enable signal
RCE	Input	Read enable signal
RST	Input	Reset signal
ORCE	Input	Output register enable signal
INJECT_SBITERR	Input	Single-bit error injection in ECC mode
INJECT_DBITERR	Input	ECC mode double-bit error insertion
DO	Output	Data read out

Port	Direction	Function Description
EMPTY	Output	Read port empty flag
FULL	Output	Write port full flag
ALMOST_EMPTY	Output	Read port almost empty flag
ALMOST_FULL	Output	Write port almost full flag
ECC_SBITERR	Output	Single-bit error flag in ECC mode
ECC_DBITERR	Output	Dual-bit error flag in ECC mode

5.17.4 Paramater Description

Table 5-51 GTP_FIFO36K_E1 Parameter List

Parameter Name	Function Description	Setting Value	Defaults
GRS_EN	Global reset enable signal (Internal Chip)	TRUE: Enable global reset; FALSE: Do not enable global reset.	TRUE
DATA_WIDTH	FIFO data width	1, 2, 4, 8, 9, 16, 18, 32, 36, 64, 72	18
ALMOST_FULL_OFFSET	When the FIFO is almost full and the difference between the write and read pointers equals to ALMOST_FULL_OFFSET, the almost_full flag is generated.	DATA_WIDTH= 1bit: sync FIFO:1–32767 async FIFO:1–32764 2bits: sync FIFO:1–16383 async FIFO:1–16380 4bits: sync FIFO:1–8191 async FIFO:1–8188 8/9bits: sync FIFO:1–4095 async FIFO:1–4092 16/18bits: sync FIFO:1–2047 async FIFO:1–2044 32/36bits: sync FIFO:1–1023 async FIFO:1–1020 64/72bits: sync FIFO:1–511 async FIFO:1–508	15'h0000

Parameter Name	Function Description	Setting Value	Defaults
ALMOST_EMPTY_OFFSET	When the FIFO is almost empty and the difference between the read and write pointers equals to ALMOST_EMPTY_OFFSET, the almost_empty flag is generated.	DATA_WIDTH=1bit: sync FIFO:1~32767 async FIFO:4~32767 2bits: sync FIFO:1~16383 async FIFO: 4~16383 4bits: sync FIFO:1~8191 async FIFO: 4~8191 8/9bits: sync FIFO:1~4095 async FIFO: 4~4095 16/18bits: sync FIFO:1~2047 async FIFO: 4~2047 32/36bits: sync FIFO: 1~1023 async FIFO: 4~1023 64/72bits: sync FIFO: 1~511 async FIFO: 4~511	15'h0000
SYNC_FIFO	Asynchronous/Synchronous FIFO Selection	TRUE: Use synchronous FIFO; FALSE: Use asynchronous FIFO.	FALSE
USE_EMPTY	Enable read empty flag	1: Read empty flag enabled; 0: Read empty flag not enabled.	0
USE_FULL	Enable write full flag	1: Write full flag enabled; 0: Write full flag not enabled.	0
DO_REG	Output register enable	1: Enabled; 0: Not enabled.	0
ECC_WRITE_EN	Write port ECC mode enable	TRUE: Enabled; FALSE: Not enabled.	FALSE
ECC_READ_EN	Read port ECC mode enable	TRUE: Enabled; FALSE: Not enabled.	FALSE
RST_VAL	Output set/reset value	72'h00_0000_0000_0000_0000~ 72'hFF_FFFF_FFFF_FFFF_FFFF	72'h0

5.17.5 Instantiation Template

```

GTP_FIFO36K_E1 #(
    .GRS_EN("TRUE"),
    .DATA_WIDTH(18),
    .DO_REG(0),
    .ECC_READ_EN("FALSE"),
    .ECC_WRITE_EN("FALSE"),
    .ALMOST_FULL_OFFSET(15'b0),
    .ALMOST_EMPTY_OFFSET(15'b0),
    .RST_VAL(72'b0),
    .USE_EMPTY(0),
    .USE_FULL(0),
    .SYNC_FIFO("FALSE")
) GTP_FIFO36K_E1_inst (
    .DO(do),
    .DI(di),
    .ALMOST_EMPTY(almost_empty),
    .ALMOST_FULL(almost_full),
    .ECC_DBITERR(ecc_dbiterr),
    .ECC_SBITERR(ecc_sbiterr),
    .EMPTY(empty),
    .FULL(full),
    .INJECT_DBITERR(inject_dbiterr),
    .INJECT_SBITERR(inject_sbiterr),
    .ORCE(orce),
    .RCE(rce),
    .RCLK(rclk),
    .RST(rst),
    .WCE(wce),
    .WCLK(wclk)
);

```

5.18 GTP_FIFO18K_E1

5.18.1 Supported Devices

Table 5-52 GTP_FIFO18K_E1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

5.18.2 Description of Functionality

GTP_FIFO18K_E1 supports 18K bits storage units, can be configured various data width mode such as 16K*1, 8K*2, 4K*4, 2K*9(8) and 1K*18(16).

When using GTP_FIFO18K_E1, the DRM is configured to SDP mode, which does not support mixed bit width, nor Byte enable write operations. One DRM port is dedicated to FIFO data writing, and another is designated for FIFO data reading; in asynchronous FIFO mode, read and write ports can use different clocks.

The structure block diagram is shown below:

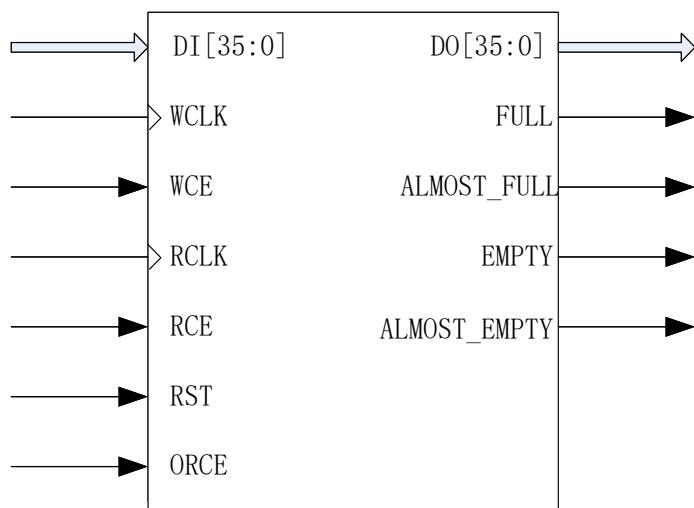


Figure 5-23 GTP_FIFO18K Structure Block Diagram

5.18.3 Port Description

Table 5-53 GTP_FIFO18K_E1 Port List

Port	Direction	Function Description
ALMOST_EMPTY	Output	Read port almost empty flag
ALMOST_FULL	Output	Write port almost full flag
EMPTY	Output	Read port empty flag
FULL	Output	Write port full flag
DO[35:0]	Output	Data read out

Port	Direction	Function Description
DI[35:0]	Input	Data write in
WCLK	Input	Write clock
RCLK	Input	Read clock
WCE	Input	Write enable
RCE	Input	Read enable
ORCE	Input	Output register enable signal
RST	Input	Reset (active high)

5.18.4 Paramater Description

Table 5-54 GTP_FIFO18K_E1 Parameter List

Parameter Name	Function Description	Setting Value	Defaults
GRS_EN	Global reset enable	"TRUE" "FALSE"	"TRUE"
DATA_WIDTH	FIFO data width	1,2,4,8,9,16,18,32,36	18
DO_REG	Output register enable	1: Enabled 0: Not enabled	0
ALMOST_FULL_OFFSET	When the FIFO is almost full and the difference between the write and read pointers equals to ALMOST_FULL_OFFSET, the almost_full flag is generated.	DATA_WIDTH= 1bit: sync FIFO:1–16383 async FIFO:1–16380 2bits: sync FIFO:1–8191 async FIFO:1–8188 4bits: sync FIFO:1–4095 async FIFO: 1–4092 8/9bits: sync FIFO:1–2047 async FIFO:1–2044 16/18bits: sync FIFO: 1–1023 async FIFO: 1–1020 32/36bits: sync FIFO: 1–511 async FIFO: 1–508	14'h0

Parameter Name	Function Description	Setting Value	Defaults
ALMOST_EMPTY_OFFSET	When the FIFO is almost empty and the difference between the read and write pointers equals to ALMOST_EMPTY_OFFSET, the almost_empty flag is generated.	DATA_WIDTH= 1bit: sync FIFO:1–16383 async FIFO: 4–16383 2bits: sync FIFO:1–8191 async FIFO: 4–8191 4bits: sync FIFO:1–4095 async FIFO: 4–4095 8/9bits: sync FIFO:1–2047 async FIFO: 4–2047 16/18bits: sync FIFO: 1–1023 async FIFO: 4–1023 32/36bits: sync FIFO: 1–511 async FIFO: 4–511	14'h0
RST_VAL	Outputs reset/set value	36'h0 – 36'hF_FFFF_FFFF	36'h0
USE_EMPTY	Enable read empty flag	1: Read empty flag enabled; 0: Read empty flag not enabled.	0
USE_FULL	Enable write full flag	1: Write full flag enabled; 0: Write full flag not enabled.	0
SYNC_FIFO	Asynchronous/Synchronous FIFO Selection	"TRUE": Enable synchronous FIFO "FALSE": Enable asynchronous FIFO	"FALSE"

5.18.5 Instantiation Template

```

GTP_FIFO18K_E1 #(
    .GRS_EN("TRUE"),
    .DATA_WIDTH(18),
    .DO_REG(0),
    .ALMOST_FULL_OFFSET(15'b0),
    .ALMOST_EMPTY_OFFSET(15'b0),
    .RST_VAL(36'b0),
    .USE_EMPTY(0),
    .USE_FULL(0),
    .SYNC_FIFO("FALSE")
) GTP_FIFO18K_E1_inst (
    .DO          (do          ),
    .DI          (di          ),
    .ALMOST_EMPTY(almost_empty),
    .ALMOST_FULL(almost_full ),
    .EMPTY       (empty       ),
    .FULL        (full        ),
    .ORCE        (orce        ),
    .RCE         (rce         ),
    .RCLK        (rclk        ),
    .RST         (rst         ),
    .WCE         (wce         ),
    .WCLK        (wclk        )
);

```

Chapter 6 Usage Instructions for IO-related GTPs

6.1 GTP_INBUF

6.1.1 Supported Devices

Table 6-1 GTP_INBUF-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.1.2 Description of Functionality

GTP_INBUF is an input BUFFER. It is shown in the following figure:

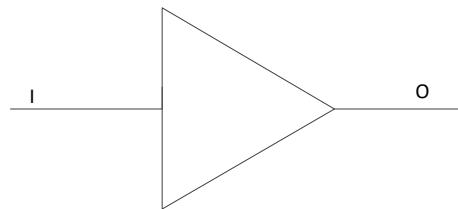


Figure 6-1 GTP_INBUF

6.1.3 Port Description

Table 6-2 GTP_INBUF Port List Description

Port	Direction	Function Description
I	Input	Input Signal
O	Output	Output signal

6.1.4 Parameter Description

Table 6-3 GTP_INBUF Parameter List

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	Refer to Table 6-4	DEFAULT	IO Standard
TERM_DDR	Refer to Table 6-4	"ON"	The built-in termination resistor is enabled or disabled during HSTL and SSTL standard inputs

Table 6-4 GTP_INBUF Valid Parameter Values

GTP_INBUF	
IOSTANDARD	TERM_DDR
LVTTL33	None
PCI33	
LVCMOS33	
LVCMOS25	
LVCMOS18	
LVCMOS15	
LVCMOS12	
SSTL25_I	OFF/ON
SSTL25_II	OFF/ON
SSTL18_I	OFF/ON
SSTL18_II	OFF/ON
SSTL15_I	OFF/ON
SSTL15_II	OFF/ON
HSTL18_I	OFF/ON
HSTL18_II	OFF/ON
HSTL15_I	OFF/ON
SSTL15_I_CAL	ON
SSTL15_II_CAL	ON
HSTL15_I_CAL	ON
SSTL135_I	OFF/ON
SSTL135_II	OFF/ON
SSTL12	OFF/ON
HSTL12_I	OFF/ON
HSUL12	OFF/ON
POD12	OFF/ON
HSTL15_II	OFF/ON
SSTL18_I_CAL	ON
SSTL18_II_CAL	ON
SSTL15_I_CAL	ON
SSTL15_II_CAL	ON
HSTL18_I_CAL	ON
HSTL18_II_CAL	ON
HSTL15_I_CAL	ON
HSTL15_II_CAL	ON
SSTL135_I_CAL	ON
SSTL135_II_CAL	ON
SSTL12_CAL	ON

GTP_INBUF	
IOSTANDARD	TERM_DDR
HSTL12_I_CAL	ON
HSUL12_CAL	ON
POD12_CAL	ON
LVCAL_15	None
LVCAL_18	
HSLVCAL_15	
HSLVCAL_18	

Note: Includes all standards for HR and HP (i.e., Common valid values of Titan2 and other families).

6.1.5 Instantiation Template

```
GTP_INBUF#(
    .IOSTANDARD ("DEFAULT"),
    .TERM_DDR      ("ON")
)
GTP_INBUF_inst (
    .I  (i),
    .O  (o)
);
```

6.2 GTP_INBUFG

6.2.1 Supported Devices

Table 6-5 GTP_INBUFG-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.2.2 Description of Functionality

GTP_INBUFG is a clock input BUFFER. It is shown in the following figure:

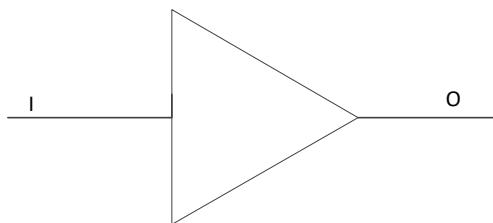


Figure 6-2 GTP_INBUFG

6.2.3 Port Description

Table 6-6 GTP_INBUFG Port List Description

Port	Direction	Function Description
I	Input	Input Signal
O	Output	Output signal

6.2.4 Parameter Description

Table 6-7 GTP_INBUFG Parameter List Description

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	Refer to Table 6-8	DEFAULT	IO Standard
TERM_DDR	Refer to Table 6-8	"ON"	The built-in termination resistor is enabled or disabled during HSTL and SSTL standard inputs

Table 6-8 GTP_INBUFG Valid Parameter Values

GTP_INBUFG	
IOSTANDARD	TERM_DDR
LVCMOS33	None
LVCMOS25	
LVCMOS18	
LVCMOS15	
LVCMOS12	
SSTL25_I	OFF/ON
SSTL25_II	OFF/ON
SSTL18_I	OFF/ON
SSTL18_II	OFF/ON
SSTL15_I	OFF/ON

GTP_INBUFG	
IOSTANDARD	TERM_DDR
SSTL15_I	OFF/ON
HSTL18_I	OFF/ON
HSTL18_II	OFF/ON
HSTL15_I	OFF/ON
SSTL15_I_CAL	ON
SSTL15_II_CAL	ON
HSTL15_I_CAL	ON
SSTL135_I	OFF/ON
SSTL135_II	OFF/ON
SSTL12	OFF/ON
HSTL12_I	OFF/ON
HSUL12	OFF/ON
POD12	OFF/ON
HSTL15_II	OFF/ON
SSTL18_I_CAL	ON
SSTL18_II_CAL	ON
HSTL18_I_CAL	ON
HSTL18_II_CAL	ON
HSTL15_II_CAL	ON
SSTL135_I_CAL	ON
SSTL135_II_CAL	ON
SSTL12_CAL	ON
HSTL12_I_CAL	ON
HSUL12_CAL	ON
POD12_CAL	ON
LVCAL_15	None
LVCAL_18	
HSLVCAL_15	
HSLVCAL_18	

Note: Includes all standards for HR and HP (i.e., Common valid values of Titan2 and other families).

6.2.5 Instantiation Template

```
GTP_INBUFG#(
    .IOSTANDARD ("DEFAULT"),
    .TERM_DDR ("ON")
)
GTP_INBUFG_inst (
    .I  (i),
    .O  (o)
);
```

6.3 GTP_INBUFDS

6.3.1 Supported Devices

Table 6-9 GTP_INBUFDS-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.3.2 Description of Functionality

GTP_INBUFDS is a differential input BUFFER. It is shown in the following figure:

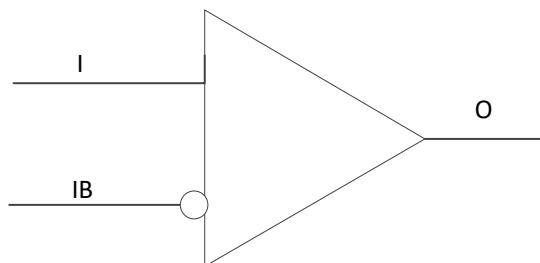


Figure 6-3 GTP_INBUFDS

6.3.3 Port Description

Table 6-10 GTP_INBUFDS Port List Description

Port	Direction	Function Description
I	Input	Differential P input signals
IB	Input	Differential N input signals
O	Output	Output signal

6.3.4 Parameter Description

Table 6-11 GTP_INBUFDS Parameter List

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	Refer to Table 6-12	DEFAULT	IO Standard
TERM_DIFF	Refer to Table 6-12	"ON"	The built-in termination resistor is enabled or disabled during differential input

Table 6-12 GTP_INBUFDS Valid Parameter Values

GTP_INBUFDS	
IOSTANDARD	TERM_DIFF
LVDS	OFF/ON
MINI-LVDS	OFF/ON
LVPECL	OFF/ON
SUB-LVDS	OFF/ON
SSTL18D_I	OFF/ON
SSTL18D_II	OFF/ON
SSTL15D_I	OFF/ON
SSTL15D_II	OFF/ON
HSTL18D_I	OFF/ON
HSTL18D_II	OFF/ON
HSTL15D_I	OFF/ON
SSTL25D_I	OFF/ON
RSDS	OFF/ON
PPDS	OFF/ON
TMDS	OFF/ON
SSTL25D_II	OFF/ON
BLVDS	OFF/ON
SSTL15D_I_CAL	ON
SSTL15D_II_CAL	ON
HSTL15D_I_CAL	ON

6.3.5 Instantiation Template

```
GTP_INBUFDS#(
    .IOSTANDARD ("DEFAULT"),
    .TERM_DIFF("ON")
)
GTP_INBUFDS_inst (
    .I      (i),
    .IB     (ib),
    .O      (o)
);
```

6.4 GTP_INBUFGDS

6.4.1 Supported Devices

Table 6-13 GTP_INBUFGDS-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.4.2 Description of Functionality

GTP_INBUFGDS is a differential clock input BUFFER. It is shown in the following figure:

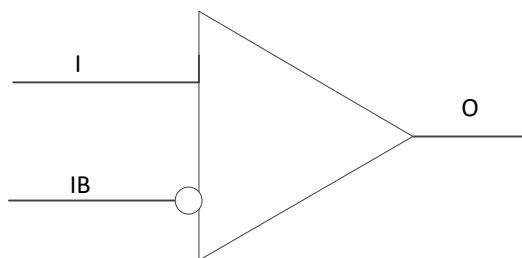


Figure 6-4 GTP_INBUFGDS

6.4.3 Port Description

Table 6-14 GTP_INBUFGDS Port List Description

Port	Direction	Function Description
I	Input	Differential P input signals
IB	Input	Differential N input signals
O	Output	Output signal

6.4.4 Parameter Description

Table 6-15 GTP_INBUFGDS Parameter Description

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	Refer to Table 6-16	DEFAULT	IO Standard
TERM_DIFF	Refer to Table 6-16	"ON"	The built-in termination resistor is enabled or disabled during differential input

Table 6-16 GTP_INBUFGDS Valid Parameter Values

GTP_INBUFGDS	
IOSTANDARD	TERM_DIFF
LVDS	OFF/ON
MINI-LVDS	OFF/ON
LVPECL	OFF/ON
SUB-LVDS	OFF/ON
SSTL18D_I	OFF/ON
SSTL18D_II	OFF/ON
SSTL15D_I	OFF/ON
SSTL15D_II	OFF/ON
HSTL18D_I	OFF/ON
HSTL18D_II	OFF/ON
HSTL15D_I	OFF/ON
SSTL25D_I	OFF/ON
RSDS	OFF/ON
PPDS	OFF/ON
TMDS	OFF/ON
SSTL25D_II	OFF/ON
BLVDS	OFF/ON
SSTL15D_I_CAL	ON
SSTL15D_II_CAL	ON
HSTL15D_I_CAL	ON

6.4.5 Instantiation Template

```
GTP_INBUFGDS#(
    .IOSTANDARD ("DEFAULT"),
    .TERM_DIFF ("ON")
)
GTP_INBUFGDS_inst (
    .I    (i),
    .IB   (ib),
    .O    (o)
);
```

6.5 GTP_INBUFE

6.5.1 Supported Devices

Table 6-17 GTP_INBUFE-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.5.2 Description of Functionality

GTP_INBUFE supports single-ended input driving function.

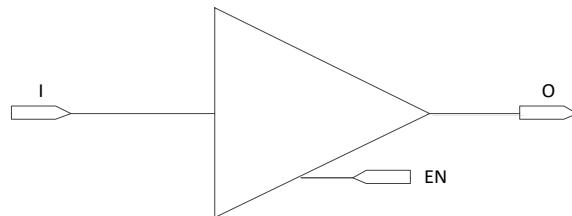


Figure 6-5 GTP_INBUFE

6.5.3 Port Description

Table 6-18 GTP_INBUFE Port List Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	Output from input buffer to the chip
EN	Input	Input buffer is disabled when set to 0.

6.5.4 Parameter Description

Table 6-19 GTP_INBUFE Parameter List Description

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	Refer to Table 6-20	DEFAULT	Input IO standard
TERM_DDR	Refer to Table 6-20	"ON"	The built-in termination resistor is enabled or disabled during HSTL and SSTL standard inputs

Table 6-20 GTP_INBUFE Valid Parameter Values

GTP_INBUFE	
IOSTANDARD	TERM_DDR
LVTTL33	
PCI33	
LVCMOS33	
LVCMOS25	None
LVCMOS18	
LVCMOS15	
LVCMOS12	
SSTL25_I	OFF/ON
SSTL25_II	OFF/ON
SSTL18_I	OFF/ON
SSTL18_II	OFF/ON
SSTL15_I	OFF/ON
SSTL15_II	OFF/ON
HSTL18_I	OFF/ON
HSTL18_II	OFF/ON
HSTL15_I	OFF/ON
SSTL135_I	OFF/ON
SSTL135_II	OFF/ON
SSTL12	OFF/ON
HSTL12_I	OFF/ON
HSUL12	OFF/ON
POD12	OFF/ON
HSTL15_II	OFF/ON
SSTL18_I_CAL	ON
SSTL18_II_CAL	ON
SSTL15_I_CAL	ON
SSTL15_II_CAL	ON
HSTL18_I_CAL	ON
HSTL18_II_CAL	ON
HSTL15_I_CAL	ON

GTP_INBUFE	
IOSTANDARD	TERM_DDR
HSTL15_II_CAL	ON
SSTL135_I_CAL	ON
SSTL135_II_CAL	ON
SSTL12_CAL	ON
HSTL12_I_CAL	ON
HSUL12_CAL	ON
POD12_CAL	ON
LVCAL_15	None
LVCAL_18	
HSLVCAL_15	
HSLVCAL_18	

Note: Includes all standards for HR and HP (i.e., Common valid values of Titan2 and other families).

6.5.5 Instantiation Template

```
GTP_INBUFE #(
    .IOSTANDARD("DEFAULT"),
    .TERM_DDR("ON")
) GTP_INBUFE_inst (
    .O(),
    .EN(),
    .I()
);
```

6.6 GTP_INBUFEDS

6.6.1 Supported Devices

Table 6-21 GTP_INBUFEDS-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.6.2 Description of Functionality

GTP_INBUFEDS supports input function. Compared to GTP_INBUFDS, GTP_INBUFEDS adds an EN signal that can disable the input, while other characteristics remain same.

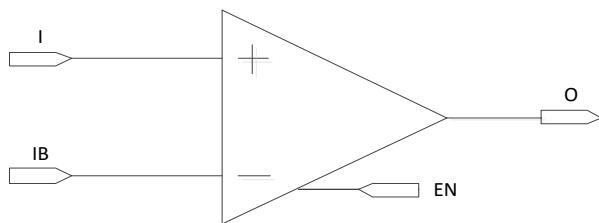


Figure 6-6 GTP_INBUFEDS

6.6.3 Port Description

Table 6-22 GTP_INBUFEDS Port List Description

Port	Direction	Function Description
I	Input	Noninverting differential input
IB	Input	Inverting differential input
O	Output	Differential output to the chip
EN	Input	Input buffer is disabled when set to 0.

6.6.4 Parameter Description

Table 6-23 GTP_INBUFEDS Parameter List Description

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	Refer to Table 6-24	DEFAULT	Input IO standard
TERM_DIFF	Refer to Table 6-24	"ON"	The built-in termination resistor is enabled or disabled during differential input

Table 6-24 GTP_INBUFEDS Valid Parameter Values

GTP_INBUFEDS	
IOSTANDARD	TERM_DIFF
LVDS	OFF/ON
MINI-LVDS	OFF/ON
LVPECL	OFF/ON
SUB-LVDS	OFF/ON
SSTL18D_I	OFF/ON
SSTL18D_II	OFF/ON
SSTL15D_I	OFF/ON

GTP_INBUFEDS	
IOSTANDARD	TERM_DIFF
SSTL15D_II	OFF/ON
HSTL18D_I	OFF/ON
HSTL18D_II	OFF/ON
HSTL15D_I	OFF/ON
SSTL25D_I	OFF/ON
RSDS	OFF/ON
PPDS	OFF/ON
TMDS	OFF/ON
SSTL25D_II	OFF/ON
BLVDS	OFF/ON
SSTL15D_I_CAL	ON
SSTL15D_II_CAL	ON
HSTL15D_I_CAL	ON

6.6.5 Instantiation Template

```
GTP_INBUFEDS #(
    .IOSTANDARD("DEFAULT"),
    .TERM_DIFF("ON")
) GTP_INBUFEDS_inst (
    .O(),
    .EN(),
    .I(),
    .IB()
);
```

6.7 GTP_OUTBUF

6.7.1 Supported Devices

Table 6-25 GTP_OUTBUF-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.7.2 Description of Functionality

GTP_OUTBUF is an output BUFFER. It is shown in the following figure:

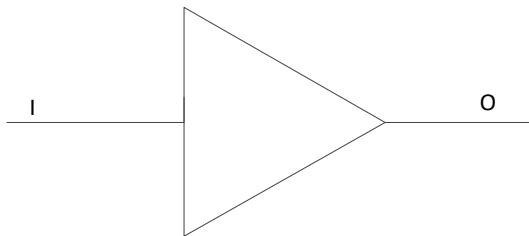


Figure 6-7 GTP_OUTBUF

6.7.3 Port Description

Table 6-26 GTP_OUTBUF Port List Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	Buffer output

6.7.4 Parameter Description

Table 6-27 GTP_OUTBUF Parameter Description

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	Refer to Table 6-28	DEFAULT	IO Standard
SLEW_RATE	"FAST", "SLOW", "MEDIUM"	"SLOW"	Slew rate
DRIVE_STRENGTH	2, 4, 6, 8, 12, 16, 24	"8"	Drive current strength

Table 6-28 GTP_OUTBUF Valid Parameter Values

GTP_OUTBUF		
IOSTANDARD	SLEW_RATE	DRIVE_STRENGTH
LVTTL33	FAST/SLOW	'4", "6", "12", "16", "24"
PCI33	FAST/SLOW	
LVCMOS33	FAST/SLOW	'4", "8", "12", "16"
LVCMOS25	FAST/SLOW	
LVCMOS18	FAST/SLOW	'4", "8", "12", '2", "6",
LVCMOS15	FAST/SLOW	
LVCMOS12	FAST/SLOW	None
SSTL25_I	FAST/SLOW	
SSTL25_II	FAST/SLOW	
SSTL18_I	FAST/SLOW	

GTP_OUTBUF		
IOSTANDARD	SLEW_RATE	DRIVE_STRENGTH
SSTL18_II	FAST/SLOW	
SSTL15_I	FAST/SLOW	
SSTL15_II	FAST/SLOW	
HSTL18_I	FAST/SLOW	
HSTL18_II	FAST/SLOW	
HSTL15_I	FAST/SLOW	
SSTL15_I_CAL	FAST/SLOW	
SSTL15_II_CAL	FAST/SLOW	
HSTL15_I_CAL	FAST/SLOW	

6.7.5 Instantiation Template

```
GTP_OUTBUF#(
    .IOSTANDARD ("DEFAULT"),
    .SLEW_RATE ("SLOW"),
    .DRIVE_STRENGTH (8)
)
GTP_OUTBUF_inst (
    .I  (i),
    .O  (o)
);
```

6.8 GTP_OUTBUFT

6.8.1 Supported Devices

Table 6-29 GTP_OUTBUFT-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.8.2 Description of Functionality

GTP_OUTBUFT is a tri-state output BUFFER. It is shown in the following figure:

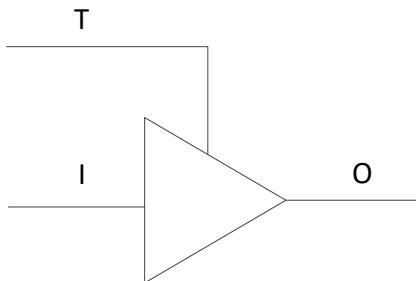


Figure 6-8 GTP_OUTBUFT

6.8.3 Port Description

Table 6-30 GTP_OUTBUFT Port List Description

Port	Direction	Function Description
I	Input	Input Signal
O	Output	Output signal
T	Input	Tri-state enable, T=1 sets the output port to tri-state, T=0 drives the input signal I to the output port

6.8.4 Parameter Description

Table 6-31 GTP_OUTBUFT Parameter Description

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	Refer to Table 6-32	DEFAULT	IO Standard
SLEW_RATE	"FAST", "SLOW", "MEDIUM"	"SLOW"	Slew rate
DRIVE_STRENGTH	"2", "4", "6", "8", "12", "16", "24"	"8"	Drive current strength

Table 6-32 GTP_OUTBUFT Valid Parameter Values

GTP_OUTBUFT		
IOSTANDARD	SLEW_RATE	DRIVE_STRENGTH
LVTTL33	FAST/SLOW	'4", "6", "12", "16", "24"
PCI33	FAST/SLOW	
LVCMOS33	FAST/SLOW	
LVCMOS25	FAST/SLOW	'4", "8", "12", "16"
LVCMOS18	FAST/SLOW	
LVCMOS15	FAST/SLOW	
LVCMOS12	FAST/SLOW	'2", "6",
SSTL25_I	FAST/SLOW	None

GTP_OUTBUFT		
IOSTANDARD	SLEW_RATE	DRIVE_STRENGTH
SSTL25_II	FAST/SLOW	
SSTL18_I	FAST/SLOW	
SSTL18_II	FAST/SLOW	
SSTL15_I	FAST/SLOW	
SSTL15_II	FAST/SLOW	
HSTL18_I	FAST/SLOW	
HSTL18_II	FAST/SLOW	
HSTL15_I	FAST/SLOW	
SSTL15_I_CAL	FAST/SLOW	
SSTL15_II_CAL	FAST/SLOW	
HSTL15_I_CAL	FAST/SLOW	

6.8.5 Instantiation Template

```
GTP_OUTBUFT#(
    .IOSTANDARD ("DEFAULT"),
    .SLEW_RATE ("SLOW "),
    .DRIVE_STRENGTH (8)
)
GTP_OUTBUFT_inst (
    .I  (i),
    .O  (o),
    .T  (t)
);
```

6.9 GTP_OUTBUFDS

6.9.1 Supported Devices

Table 6-33 GTP_OUTBUFDS-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.9.2 Description of Functionality

GTP_OUTBUFDS is a true differential output buffer. The Structure is shown below.

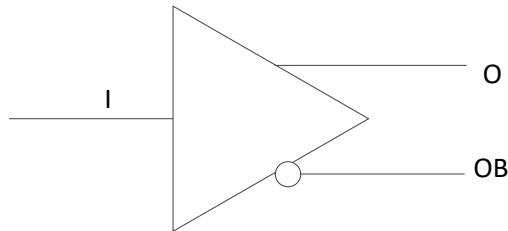


Figure 6-9 GTP_OUTBUFDS

6.9.3 Port Description

Table 6-34 GTP_OUTBUFDS Port List Description

Port	Direction	Function Description
I	Input	Input Signal
OB	Output	Differential N output signals
O	Output	Differential P output signals

6.9.4 Parameter Description

Table 6-35 GTP_OUTBUFDS Parameter List Description

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	"LVDS","MINI-LVDS","TMDS","RSDS","PPDS","LVDS_18"	DEFAULT	IO Standard

Note: The set value "LVDS_18" of Parameter IOSTANDARD is designated for TITAN2 HPIO, while others fall within the value range of LOGOS2+Titan2 HRIO.

6.9.5 Instantiation Template

```

GTP_OUTBUFDS#(
    .IOSTANDARD ("DEFAULT"),
)
    GTP_OUTBUFDS_inst (
        .I    (i),
        .OB(ob),
        .O    (o)
    );

```

6.10 GTP_OUTBUFTDS

6.10.1 Supported Devices

Table 6-36 GTP_OUTBUFTDS-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.10.2 Description of Functionality

GTP_OUTBUFTDS is a tri-state output true differential BUFFER. It is shown in the following figure:

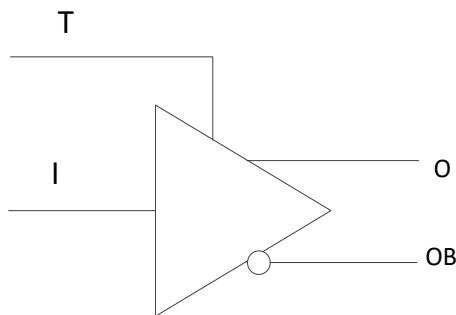


Figure 6-10 GTP_OUTBUFTDS

6.10.3 Port Description

Table 6-37 GTP_OUTBUFTDS Port List Description

Port	Direction	Function Description
I	Input	Input Signal
OB	Output	Differential N output signals
O	Output	Differential P output signals
T	Input	Tri-state enable, T=1 sets the output port to tri-state, T=0 drives the input signal I to the output port

6.10.4 Paramater Description

Table 6-38 GTP_OUTBUFTDS Parameter Description

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	"LVDS","MINI-LVDS" , "TMDS", "RSDS", "PPDS", "LVDS_18"	DEFAULT	Input IO standard

Note: The set value "LVDS_18" of Parameter IOSTANDARD is designated for TITAN2 HPIO, while others fall within the value range of LOGOS2+Titan2 HRIO.

6.10.5 Instantiation Template

```
GTP_OUTBUFTDS#(
    .IOSTANDARD ("DEFAULT")
)
GTP_OUTBUFTDS_inst (
    .I    (i),
    .T    (t),
    .OB   (ob),
    .O    (o)
);
```

6.11 GTP_OUTBUFCO

6.11.1 Supported Devices

Table 6-39 GTP_OUTBUFCO-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.11.2 Description of Functionality

GTP_OUTBUFCO is a pseudo-differential output buffer. It is shown in the following figure:

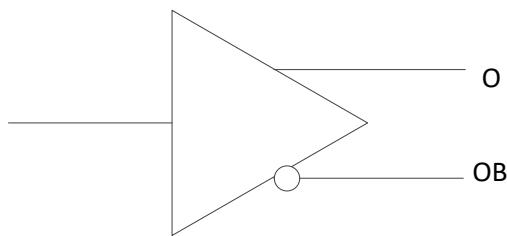


Figure 6-11 GTP_OUTBUFCO

6.11.3 Port Description

Table 6-40 GTP_OUTBUFCO Port List Information

Port	Direction	Function Description
I	Input	Input Signal
OB	Output	Differential N output signals
O	Output	Differential P output signals

6.11.4 Parameter Description

Table 6-41 GTP_OUTBUFCO Parameter List Information

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	Refer to Table 6-42	DEFAULT	IO Standard

Table 6-42 GTP_OUTBUFCO Valid Parameter Values

GTP_OUTBUFCO
IOSTANDARD
SSTL18D_I
SSTL18D_II
SSTL15D_I
SSTL15D_II
HSTL15D_I
SSTL25D_I
SSTL25D_II
SSTL15D_I_CAL
SSTL15D_II_CAL
HSTL15D_I_CAL
LVPECL
BLVDS

6.11.5 Instantiation Template

```

GTP_OUTBUFCO#(
    .IOSTANDARD ("LVCMOS33")
)
    GTP_OUTBUFCO_inst (
        .I    (i),
        .OB(ob ),
        .O    (o)
    );

```

6.12 GTP_OUTBUFTCO

6.12.1 Supported Devices

Table 6-43 GTP_OUTBUFTCO-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.12.2 Description of Functionality

GTP_OUTBUFTCO is a tri-state output pseudo-differential BUFFER. It is shown in the following figure:

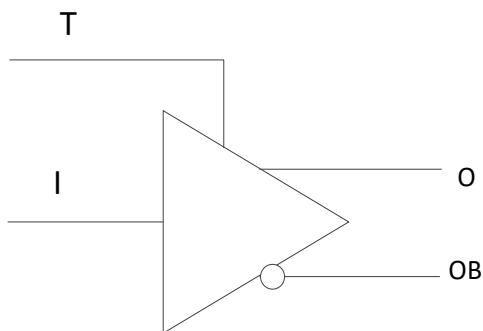


Figure 6-12 GTP_OUTBUFTCO

6.12.3 Port Description

Table 6-44 GTP_OUTBUFTCO Port List Description

Port	Direction	Function Description
I	Input	Input Signal
OB	Output	Differential N output signals
O	Output	Differential P output signals
T	Input	Tri-state enable, T=1 sets the output port to tri-state, T=0 drives the input signal I to the output port

6.12.4 Parameter Description

Table 6-45 GTP_OUTBUFTCO Parameter Description

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	Refer to Table 6-46	DEFAULT	IO Standard

Table 6-46 GTP_OUTBUFTCO Valid Parameter Values

GTP_OUTBUFTCO

IOSTANDARD
SSTL18D_I
SSTL18D_II
SSTL15D_I
SSTL15D_II
HSTL15D_I
SSTL25D_I
SSTL25D_II
SSTL15D_I_CAL
SSTL15D_II_CAL
HSTL15D_I_CAL
LVPECL
BLVDS

6.12.5 Instantiation Template

```
GTP_OUTBUFTCO#(
    .IOSTANDARD ("DEFAULT")
)
GTP_OUTBUFTCO_inst (
    .I  (i),
    .T  (t),
    .OB(ob ),
    .O  (o)
);
```

6.13 GTP_IOBUF

6.13.1 Supported Devices

Table 6-47 GTP_IOBUF-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.13.2 Description of Functionality

GTP_IOBUF is a bidirectional single-ended BUFFER, connecting external bidirectional pins with internal logic circuits. It is shown in the following figure:

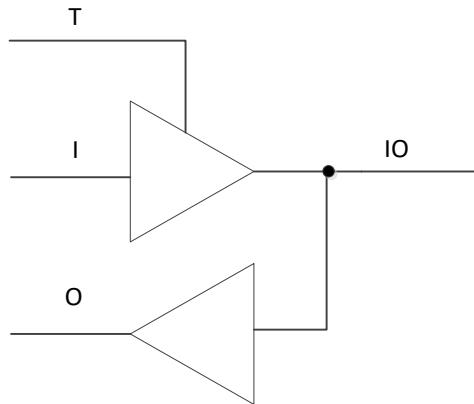


Figure 6-13 GTP_IOBUF

6.13.3 Port Description

Table 6-48 GTP_IOBUF Port List Description

Port	Direction	Function Description
I	Input	Input Signal
T	Input	Tri-state enable, T=1 sets the output port to tri-state, T=0 drives the input signal I to the output port
O	Output	Output signal
IO	Input/Output	Input/output signal (in/out)

6.13.4 Parameter Description

Table 6-49 GTP_IOBUF Parameter List Description

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	Refer to Table 6-50	DEFAULT	IO Standard
TERM_DDR	"ON", "OFF"	"ON"	The built-in termination resistor is enabled or disabled during HSTL and SSTL standard inputs
SLEW_RATE	"SLOW", "FAST"	"SLOW"	Slew rate
DRIVE_STRENGTH	"2", "4", "6", "8", "12", "16", "24"	"8"	Drive current strength

Table 6-50 GTP_IOBUF Valid Parameter Values

GTP_IOBUF			
IOSTANDARD	SLEW_RATE	TERM_DDR	DRIVE_STRENGTH
LVTTL33	FAST/SLOW	None	"4", "6", "12", "16", "24"
PCI33			
LVCMOS33			
LVCMOS25			
LVCMOS18			"4", "8", "12", "16"

GTP_Iobuf			
IOSTANDARD	SLEW_RATE	TERM_DDR	DRIVE_STRENGTH
LVCMOS15			"4", "8", "12",
LVCMOS12			"2", "6",
SSTL25_I		OFF/ON	None
SSTL25_II		OFF/ON	
SSTL18_I		OFF/ON	
SSTL18_II		OFF/ON	
SSTL15_I		OFF/ON	
SSTL15_II		OFF/ON	
HSTL18_I		OFF/ON	
HSTL18_II		OFF/ON	
HSTL15_I		OFF/ON	
SSTL15_I_CAL		ON	
SSTL15_II_CAL		ON	
HSTL15_I_CAL		ON	

6.13.5 Instantiation Template

```

GTP_Iobuf#(
    .IOSTANDARD ("DEFAULT"),
    .SLEW_RATE ("SLOW"),
    .DRIVE_STRENGTH ("8"),
    .TERM_DDR("ON")
)
    GTP_Iobuf_inst (
        .I  (i),
        .T  (t),
        .IO (io),
        .O  (o)
    );

```

6.14 GTP_Iobufco

6.14.1 Supported Devices

Table 6-51 GTP_Iobufco-Supported Devices

Device Family	LOGOS2
---------------	--------

Whether supports the GTP	Supported
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6.14.2 Description of Functionality

GTP_IOBUFCO is a bidirectional pseudo-differential buffer that only supports pseudo-differential levels (corresponding to GTP_IOBUFDS, which only supports true differential levels). The structure block diagram is shown below:

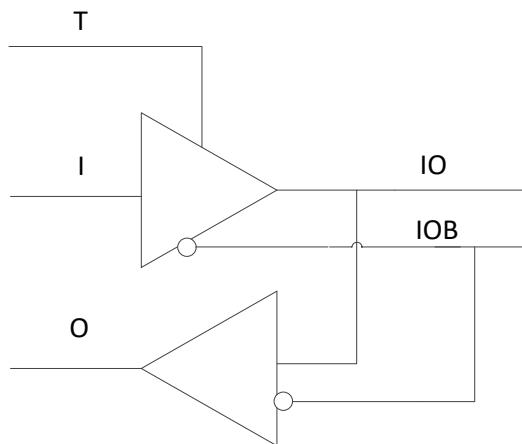


Figure 6-14 GTP_IOBUFCO

6.14.3 Port Description

Table 6-52 GTP_IOBUFCO Port List Description

Port	Direction	Function Description
I	Input	Input Signal
T	Input	Tri-state enable, T=1 sets the output port to tri-state, T=0 drives the input signal I to the output port
IO	Input/Output	Differential P side input/output
IOB	Input/Output	Differential Q side input/output
O	Output	Output signal

6.14.4 Parameter Description

Table 6-53 GTP_IOBUFCO Parameter List Description

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	Refer to Table 6-54	DEFAULT	IO Standard
TERM_DDR	"ON", "OFF"	"ON"	The built-in termination resistor is enabled or disabled during HSTL and SSTL standard inputs

Table 6-54 GTP_IOBUFCO Valid Parameter Values

IOSTANDARD	TERM_DDR
SSTL18D_I	OFF/ON
SSTL18D_II	OFF/ON
SSTL15D_I	OFF/ON
SSTL15D_II	OFF/ON
HSTL15D_I	OFF/ON
SSTL25D_I	OFF/ON
SSTL25D_II	OFF/ON
SSTL15D_I_CAL	ON
SSTL15D_II_CAL	ON
HSTL15D_I_CAL	ON
LVPECL	OFF/ON
BLVDS	OFF/ON

6.14.5 Instantiation Template

```
GTP_IOBUFCO#(
    .IOSTANDARD ("DEFAULT"),
    .TERM_DDR ("ON")
)
GTP_IOBUFCO_inst(
    .I  (i),
    .T  (t),
    .IO (io),
    .IOB(iob),
    .O  (o)
);
```

6.15 GTP_IOBUFDS

6.15.1 Supported Devices

Table 6-55 GTP_IOBUFDS-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.15.2 Description of Functionality

GTP_IOBUFDS is a bidirectional true differential buffer. It is shown in the following figure:

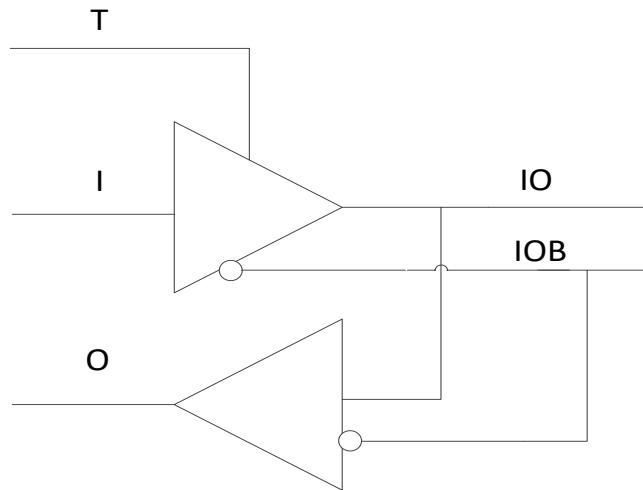


Figure 6-15 GTP_IOBUFDS

6.15.3 Port Description

Table 6-56 GTP_IOBUFDS Port List Description

Port	Direction	Function Description
I	Input	Input Signal
T	Input	Tri-state enable, T=1 sets the output port to tri-state, T=0 drives the input signal I to the output port
O	Output	Output signal
IO	Input/Output	Differential P input/output(in/out)
IOB	Input/Output	Differential N input/output(in/out)

6.15.4 Parameter Description

Table 6-57 GTP_IOBUFDS Parameter List Description

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	"LVDS", "MINI-LVDS", "PPDS", "RS DS", "TMDS", "LVDS_18"	DEFAULT	IO Standard
TERM_DIFF	"ON", "OFF"	"ON"	When using standard inputs such as LVDS, the built-in differential terminal resistor is enabled or disabled

Note: The set value "LVDS_18" of Parameter IOSTANDARD is designated for TITAN2 HPIO, while others fall within the value range of LOGOS2+Titan2 HRIO.

6.15.5 Instantiation Template

```
GTP_IOBUFDS#(
    .IOSTANDARD ("DEFAULT"),
    .TERM_DIFF("ON")
)
GTP_IOBUFDS_inst (
    .I      (i),
    .T      (t),
    .IO     (io),
    .IOB    (iob),
    .O      (o)
);
```

6.16 GTP_IOBUFE

6.16.1 Supported Devices

Table 6-58 GTP_IOBUFE-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.16.2 Description of Functionality

GTP_IOBUFE supports single-ended input and output driving function. It is shown in the following figure:

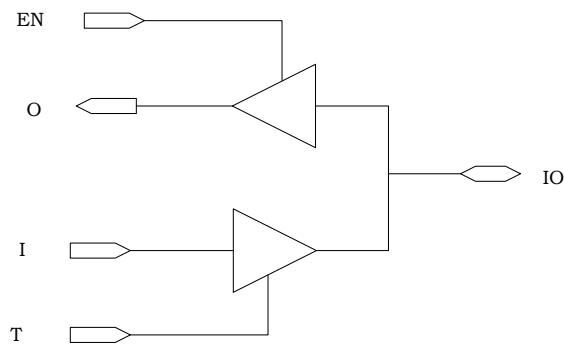


Figure 6-16 GTP_IOBUFE

6.16.3 Port Description

Table 6-59 GTP_IOBUFE Port List Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	Output from input buffer to the chip
T	Input	Tri-state enable, T=1 sets the output port to tri-state, T=0 drives the input signal I to the output port
IO	Bidirectional	PAD
EN	Input	Input buffer is disabled when set to 0.

6.16.4 Parameter Description

Table 6-60 GTP_IOBUFE Parameter List Description

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	Refer to Table 6-61	DEFAULT	IO Standard
TERM_DDR	"ON", "OFF"	"ON"	The built-in termination resistor is enabled or disabled during HSTL and SSTL standard inputs
SLEW_RATE	"SLOW", "FAST"	"SLOW"	Slew rate
DRIVE_STRENGTH	"2", "4", "6", "8", "12", "16", "24"	"8"	Drive current strength

Table 6-61 GTP_IOBUFE Valid Parameter Values

GTP_IOBUFE			
IOSTANDARD	SLEW_RATE	TERM_DDR	DRIVE_STRENGTH
LVTT33	FAST/SLOW	None	"4", "6", "12", "16", "24"
PCI33			"4", "8", "12", "16"
LVCMOS33			"4", "8", "12",
LVCMOS25			"2", "6",
LVCMOS18		OFF/ON	
LVCMOS15		OFF/ON	
LVCMOS12		OFF/ON	
SSTL25_I		None	
SSTL25_II			
SSTL18_I			
SSTL18_II			
SSTL15_I			
SSTL15_II			
HSTL18_I			
HSTL18_II			
HSTL15_I			
SSTL15_I_CAL			ON

GTP_IobufE			
IOSTANDARD	SLEW_RATE	TERM_DDR	DRIVE_STRENGTH
SSTL15_IIL_CAL		ON	
HSTL15_I_CAL		ON	

6.16.5 Instantiation Template

```
GTP_IobufE #(
    .IOSTANDARD("DEFAULT"),
    .SLEW_RATE("SLOW"),
    .DRIVE_STRENGTH("8"),
    .TERM_DDR("ON"),
    .HPIO("FALSE "),
    ) GTP_IobufE_inst (
    .IO (io),
    .O  (o ),
    .EN (en),
    .I  (i ),
    .T  (t )
);
```

6.17 GTP_IobufECO

6.17.1 Supported Devices

Table 6-62 GTP_IobufECO-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.17.2 Description of Functionality

GTP_IobufECO is a bidirectional pseudo-differential buffer. It is shown in the following figure:

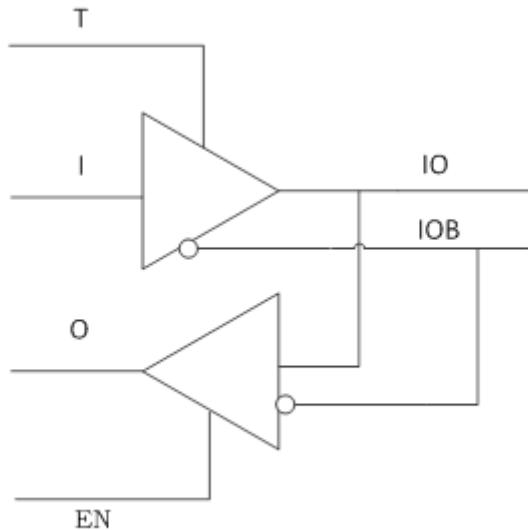


Figure 6-17 GTP_IOBUFECO

6.17.3 Port Description

Table 6-63 GTP_IOBUFECO Port List Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	Output from input buffer to the chip
T	Input	Tri-state enable, T=1 sets the output port to tri-state, T=0 drives the input signal I to the output port
IO	Bidirectional	First IO
IOB	Bidirectional	The second IO, opposite to IO's value
EN	Input	Input buffer is disabled when set to 0.

6.17.4 Parameter Description

Table 6-64 GTP_IOBUFECO Parameter List Description

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	Refer to Table 6-65	DEFAULT	IO Standard
TERM_DDR	"ON", "OFF"	"ON"	The built-in termination resistor is enabled or disabled during HSTL and SSTL standard inputs

Table 6-65 GTP_IOBUFECO Valid Parameter Values

IOSTANDARD	TERM_DDR
SSTL18D_I	OFF/ON
SSTL18D_II	OFF/ON
SSTL15D_I	OFF/ON
SSTL15D_II	OFF/ON

IOSTANDARD	TERM_DDR
HSTL15D_I	OFF/ON
SSTL25D_I	OFF/ON
SSTL25D_II	OFF/ON
SSTL15D_I_CAL	ON
SSTL15D_II_CAL	ON
HSTL15D_I_CAL	ON
LVPECL	OFF/ON
BLVDS	OFF/ON

6.17.5 Instantiation Template

```
GTP_IOBUFECO #(
    .IOSTANDARD("DEFAULT"),
    .TERM_DDR("ON"),
    .HPIO("FALSE "),
    ) GTP_IOBUFECO_inst (
        .IO      (io ),
        .IOB     (iob),
        .O       (o  ),
        .EN      (en ),
        .I       (i  ),
        .T       (t  )
    );
```

6.18 GTP_IOBUFEDS

6.18.1 Supported Devices

Table 6-66 GTP_IOBUFEDS-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.18.2 Description of Functionality

GTP_IOBUFEDS is a true differential buffer. Below shows the differential outputs under LVDS and other standards (input I and output IO/IOB), which can also be configured as inputs (IO, IOB >

O path in the figure)

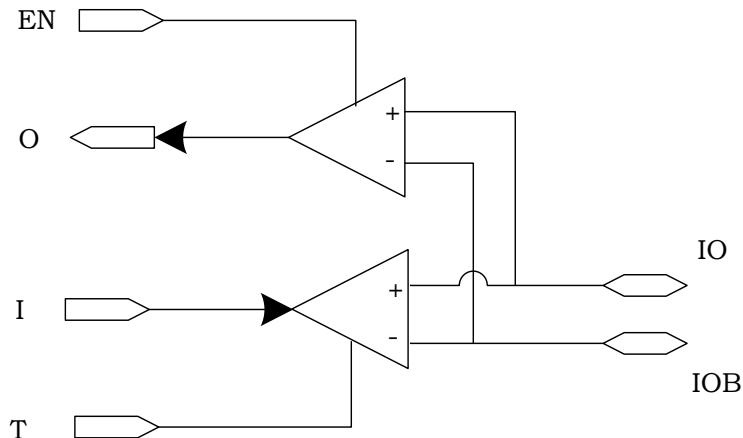


Figure 6-18 GTP_IOBUFEDS

6.18.3 Port Description

Table 6-67 GTP_IOBUFEDS Port List Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	Output from input buffer to the chip
T	Input	Tri-state enable, T=1 sets the output port to tri-state, T=0 drives the input signal I to the output port
IO	Bidirectional	IO's PAD
IOB	Bidirectional	IO's PAD, opposite to the IO value
EN	Input	Input buffer is disabled when set to 0.

6.18.4 Parameter Description

Table 6-68 GTP_IOBUFEDS Parameter List Description

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	"LVDS", "MINI-LVDS", "TMDS", "DEFAULT"	DEFAULT	IO Standard
TERM_DIFF	"ON", "OFF"	"ON"	When using standard inputs such as LVDS, the built-in differential terminal resistor is enabled or disabled

6.18.5 Instantiation Template

GTP_IOBUFEDS #(

```
.IOSTANDARD("DEFAULT"),
.TERM_DIFF("ON"),
.HPIO("FALSE ")
) GTP_Iobufeds_inst (
.IO      (io ),
.IOB     (iob),
.O       (o  ),
.EN      (en ),
.I        (i  ),
.T        (t  )
);
```

6.19 GTP_ISERDES_E2

6.19.1 Supported Devices

Table 6-69 GTP_ISERDES_E2-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.19.2 Description of Functionality

IOL flexibly supports various interface applications. In addition to the common direct input/output and input/output registers, IOL also supports input data rate conversion. GTP_I SERDES_E2 is used for input data processing, supporting direct input and output, ILATCH, IDFF, networking SDR/DDR, oversample, Low-Speed MEMORY DDR and High-Speed MEMORY DDR, along with SDR1TO2, SDR1TO3, SDR1TO4, SDR1TO5, SDR1TO6, SDR1TO7, SDR1TO8, DDR1TO2_SAME_PIPELINED, DDR1TO2_SAME_EDGE, DDR1TO2_OPPOSITE_EDGE, DDR1TO4, DDR1TO6, DDR1TO8, DDR1TO10, DDR1TO14, HMDDR1TO4, HMDDR1TO8, LMDDR1TO4, LMDDR1TO8, and OVERSAMPLE modes rate conversion. For detailed usage instructions, please refer to the "**"UG040006_Logos2 Family FPGAs Input/Output Interface (IO) User Guide"**". The Structure Block Diagram is shown below. The structure block diagram is shown below:

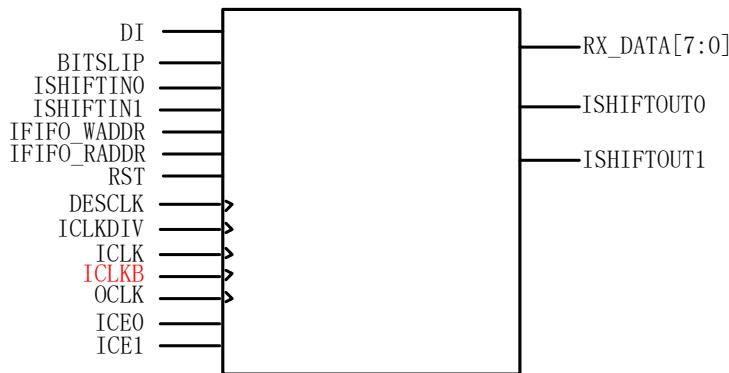


Figure 6-19 GTP_I SERDES_E2 Structure Block Diagram

6.19.3 Port Description

Table 6-70 GTP_I SERDES_E2 Port Description

Port Signal	Input/Output	Description
DI	Input	Data Input
BITSLIP	Input	Data Input
ISHIFTIN0	Input	Cascade input signal
ISHIFTIN1	Input	Cascade input signal
IFIFO_WADDR	Input	FIFO write address DQS falling edge trigger (Gray code)
IFIFO_RADDR	Input	FIFO read address (Gray code)
RST	Input	ILOGIC local reset signal
DESCLK	Input	ILOGIC deserialisation high-speed clock
ICLKDIV	Input	ILOGIC low-speed clock
ICLK	Input	ILOGIC first-stage high-speed clock
ICLKB	Input	ILOGIC first-level high-speed clock reverse input (only used as a

Port Signal	Input/Output	Description
		simulation port, without software mapping)
OCLK	Input	OLOGIC output stage high-speed clock
ICE0	Input	ILOGIC clock enable signal
ICE1	Input	ILOGIC clock enable signal
DO	Output	Deserialized output signal
ISHIFTOUT0	Output	Cascade output signals
ISHIFTOUT1	Output	Cascade output signals

6.19.4 Paramater Description

Table 6-71 GTP_I SERDES_E2 Parameter List Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
HPIO	String	"TRUE" "FALSE"	"FALSE"	"TRUE" mapped to HPIO, "FALSE" mapped to HRIO
ISERDES_MODE	String	"SDR1TO2" "SDR1TO3" "SDR1TO4" "SDR1TO5" "SDR1TO6" "SDR1TO7" "SDR1TO8" "ILATCH" "IDFF" "DDR1TO2_SAME_P IPELINED" "DDR1TO2_SAME_E DGE" "DDR1TO2_OPPOSI TE_EDGE" "DDR1TO4" "DDR1TO6" "DDR1TO8" "DDR1TO10" "DDR1TO14" "HMDDR1TO4" "HMDDR1TO8" "LMDDR1TO4" "LMDDR1TO8" "OVERSAMPLE"	SDR1TO4	"SDR1TO2": networking SDR 1:2 deserialization mode "SDR1TO3": networking SDR 1:3 deserialization mode "SDR1TO4": networking SDR 1:4 deserialization mode "SDR1TO5": networking SDR 1:5 deserialization mode "SDR1TO6": networking SDR 1:6 deserialization mode "SDR1TO7": networking SDR 1:7 deserialization mode "SDR1TO8": networking SDR 1:8 deserialization mode "ILATCH" latch input mode "IDFF" register input mode "DDR1TO2_same_pipelined": networking DDR 1:2 same pipelined deserialization mode "DDR1TO2_SAME_EDGE": networking DDR 1:2 SAME_EDGE deserialization mode "DDR1TO2_OPPOSITE_EDGE": networking DDR 1:2 OPPOSITE_EDGE deserialization mode "DDR1TO4": networking DDR 1:4 deserialization mode "DDR1TO6": networking DDR 1:6 deserialization mode "DDR1TO8": networking DDR 1:8 deserialization mode "DDR1TO10": networking DDR 1:10 deserialization mode "DDR1TO14": networking DDR 1:14 deserialization mode "HMDDR1TO4": High-Speed

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
				Memory DDR 1:4 deserialization mode "HMDDR1TO8": High-Speed Memory DDR 1:8 deserialization mode "LMDDR1TO4": Low-Speed Memory DDR 1:4 deserialization mode "LMDDR1TO8": Low-Speed Memory DDR 1:8 deserialization mode "OVERSAMPLE" deserialization mode
CASCADE_MODE	String	"MASTER" "SLAVE"	"MASTER"	Deserialisation cascade master mode
BITSLIP_EN	String	"FALSE" "TRUE"	"FALSE"	bitslip enabled
GRS_EN	String	"TRUE" "FALSE"	"TRUE"	Global reset/set enabled
NUM_ICE	Constance	1'b0 1'b1	1'b0	Selection of the number of ices
GRS_TYPE_Q0	String	"RESET" "SET"	"RESET"	Global asynchronous reset/set result of DFF0 in ILOGIC gear;
GRS_TYPE_Q1	String	"RESET" "SET"	"RESET"	Global asynchronous reset/set result of DFF1 in ILOGIC gear;
GRS_TYPE_Q2	String	"RESET" "SET"	"RESET"	Global asynchronous reset/set result of DFF2 in ILOGIC gear;
GRS_TYPE_Q3	String	"RESET" "SET"	"RESET"	Global asynchronous reset/set result of DFF3 in ILOGIC gear;
LRS_TYPE_Q0	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local asynchronous/synchronous/reset/set result of DFF0 in ILOGIC gear
LRS_TYPE_Q1	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local asynchronous/synchronous/reset/set result of DFF1 in ILOGIC gear
LRS_TYPE_Q2	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local asynchronous/synchronous/reset/set result of DFF2 in ILOGIC gear
LRS_TYPE_Q3	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local asynchronous/synchronous/reset/set result of DFF3 in ILOGIC gear

6.19.5 Instantiation Template

```
GTP_ISERDES_E2 #
(
    .HPIO("FALSE"),
    .ISERDES_MODE ("SDR1TO4"),
    .CASCADE("MASTER"),
    .BITSLIP_EN("FALSE"),
    .GRS_EN ("TRUE"),
    .NUM_ICE(1'b0),
    .GRS_TYPE_Q0("RESET"),
    .GRS_TYPE_Q1("RESET"),
    .GRS_TYPE_Q2("RESET"),
    .GRS_TYPE_Q3("RESET"),
    .LRS_TYPE_Q0("ASYNC_RESET"),
    .LRS_TYPE_Q1("ASYNC_RESET"),
    .LRS_TYPE_Q2("ASYNC_RESET"),
    .LRS_TYPE_Q3("ASYNC_RESET"),
    .ISERDES_FIFO_EN("FALSE"),
    .FIFO_DLY(2'b00),
    .FIFO_WCLK_INV("FALSE"),
    .FIFO_RCLK_INV("FALSE")
) gtp_iserdes_inst (
    .RST(rst),
    .ICE0(ice0),
    .ICE1(ice1),
    .DESCLK (desclk),
    .ICLK (iclk),
    .ICLK_B (iclkb),
    .OCLK (oclk),
    .ICLK_DIV(iclkdiv),
    .DI (di),
    .BITSLIP(bitslip),
    .ISHIFTIN0(ishiftin0),
    .ISHIFTIN1(ishiftin1),
```

```
.IFIFO_WADDR(ififo_waddr),
.IFIFO_RADDR(ififo_raddr),
.DO(DO),
.ISHIFTOUT0(ishiftout0),
.ISHIFTOUT1(ishiftout1),
.FIFO_RST(FIFO_RST),
.FIFO_EN(FIFO_EN),
.FIFO_WCLK(FIFO_WCLK),
.FIFO_RCLK(FIFO_RCLK),
.FIFO_VALID_I(FIFO_VALID_I),
.FIFO_FULL(FIFO_FULL),
.FIFO_EMPTY(FIFO_EMPTY),
.FIFO_VALID_O(FIFO_VALID_O)
);
```

6.20 GTP_OSERDES_E2

6.20.1 Supported Devices

Table 6-72 GTP_OSERDES_E2-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.20.2 Description of Functionality

IOL flexibly supports various application interfaces. In addition to the common direct input/output and input/output registers, IOL also supports data input/output rate conversion. GTP_OSERDES_E2 data output conversion module supports SDR2TO1, SDR3TO1, SDR4TO1, SDR5TO1, SDR6TO1, SDR7TO1, SDR8TO1, DDR2TO1_SAME_EDGE, DDR2TO1_OPPOSITE_EDGE, DDR4TO1, DDR6TO1, DDR8TO1, DDR10TO1, DDR14TO1, HMSDR2TO1, HMSDR4TO1, HMSDR8TO1, OLATCH, and ODFF modes rate conversion. For detailed usage instructions, please refer to the "UG040006_Logos2 Family FPGAs Input/Output Interface (IO) User Guide". The Structure Block Diagram is shown below. The structure block diagram is shown below:

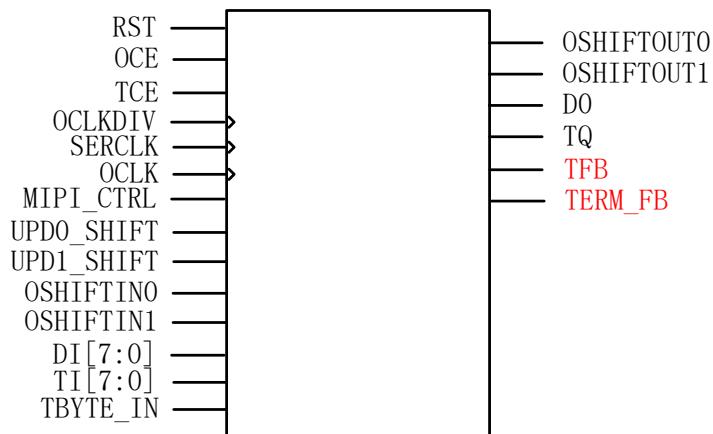


Figure 6-20 GTP_OSERDES_E2 Structure Block Diagram

6.20.3 Port Description

Table 6-73 GTP_OSERDES_E2 Port Description

Port Signal	Input/Output	Data Width	Description
RST	Input	1	Local reset signal
OCE	Input	1	Clock enable signal of output module
TCE	Input	1	Clock enable signal of tri-state module
OCLKDIV	Input	1	OLOGIC low-speed clock
SERCLK	Input	1	OLOGIC serialisation clock
OCLK	Input	1	OLOGIC output stage high-speed clock
MIPI_CTRL	Input	1	This port is reserved.
UPD0_SHIFT	Input	1	OLOGIC UPD0 position shift
UPD1_SHIFT	Input	1	OLOGIC UPD1 position shift
OSHIFTINO	Input	1	Cascade input signal
OSHIFTIN1	Input	1	Cascade input signal
DI	Input	8	Parallel input data signals
TI	Input	2	Parallel input tri-state control signal
TBYTE_IN	Input	1	Tri-state control input signal for one byte
OSHIFTOUT0	Output	1	Cascade input signal
OSHIFTOUT1	Output	1	Cascade input signal
DO	Output	1	Data output
TQ	Output	1	Tri-state control output (to IOB)
TFB	Output	1	Tri-state control output (to internal logic)
TERM_FB	Output	1	Terminal control output (to internal logic)

6.20.4 Parameter Description

Table 6-74 GTP_OSERDES_E2 Parameter List Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
HPIO	String	"TRUE", "FALSE"	"FALSE"	TRUE indicates to use OSERDES of HPIO, otherwise HRIO
ODELAY_EN	String	"TRUE", "FALSE"	"FALSE"	TRUE indicates to use ODELAY for the MUX data output source
TDELAY_EN	String	"TRUE", "FALSE"	"FALSE"	TRUE indicates to use TDELAY for the MUX data output source
OSERDES_MODE	String	"SDR2TO1" "SDR3TO1" "SDR4TO1" "SDR5TO1" "SDR6TO1" "SDR7TO1" "SDR8TO1" "OLATCH" "ODFF" "DDR2TO1_SAME_EDGE" "DDR2TO1_OPPOSITE_EDGE" "DDR4TO1" "DDR6TO1" "DDR8TO1" "DDR10TO1" "DDR14TO1" "HMSDR4TO1" "HMSDR8TO1"	SDR4TO1	"SDR2TO1": Generic SDR 2:1 serialization mode "SDR3TO1": Generic SDR 3:1 serialization mode "SDR4TO1": Generic SDR 4:1 serialization mode "SDR5TO1": Generic SDR 5:1 serialization mode "SDR6TO1": Generic SDR 6:1 serialization mode "SDR7TO1": Generic SDR 7:1 serialization mode "SDR8TO1": Generic SDR 8:1 serialization mode "OLATCH": Latch output mode "ODFF": Register output mode "DDR2TO1_SAME_EDGE": Generic DDR 2:1 serialization mode "DDR2TO1_OPPOSITE_EDGE": Generic DDR 2:1 serialization mode "DDR4TO1": Generic DDR 4:1 serialization mode "DDR6TO1": Generic DDR 6:1 serialization mode "DDR8TO1": Generic DDR 8:1 serialization mode "DDR10TO1": Generic DDR 10:1 serialization mode "DDR14TO1": Generic DDR 14:1 serialization mode "HMSDR4TO1": High-Speed Memory DDR 4:1 serialization mode "HMSDR8TO1": High-Speed Memory DDR 8:1 serialization mode

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
TSERDES_MODE	String	"SDR2TO1" "SDR4TO1" "SDR8TO1" "TLATCH" "TDFF" "DDR2TO1_SAME_EDGE" "DDR2TO1_OPPOSITE_EDGE" "DDR4TO1" "DDR8TO1" "HMSDR4TO1" "HMSDR8TO1"	SDR4TO1	"SDR2TO1": Generic SDR 2:1 serialization mode "SDR4TO1": Generic SDR 4:1 serialization mode "SDR8TO1": Generic SDR 8:1 serialization mode "TLATCH": Latch output mode "TDFF": Register output mode "DDR2TO1_SAME_EDGE": Generic DDR 2:1 serialization mode "DDR2TO1_OPPOSITE_EDGE": Generic DDR 2:1 serialization mode "DDR4TO1": Generic DDR 4:1 serialization mode "DDR8TO1": Generic DDR 8:1 serialization mode "HMSDR4TO1": High-Speed Memory DDR 4:1 serialization mode "HMSDR8TO1": High-Speed Memory DDR 8:1 serialization mode
UPD0_SHIFT_EN	String	"FALSE" "TRUE"	"FALSE"	Position control for upd0 in OLOGIC enabled
UPD1_SHIFT_EN	String	"FALSE" "TRUE"	"FALSE"	Position control for upd1 in OLOGIC enabled
TUPD0_SHIFT_EN	String	"FALSE" "TRUE"	"FALSE"	upd0 position control enable in TSERDES
TUPD1_SHIFT_EN	String	"FALSE" "TRUE"	"FALSE"	upd1 position control enable in TSERDES
INIT_SET[1:0]	Constance	2'b00, 2'b01, 2'b10, 2'b11	2'b00	upd0 and upd1 position static control in OSERDES 2'b00: Default position; 2'b01: Advance by one cycle; 2'b10: Advance by two cycles; 2'b11: Advance by three cycles;
TINIT_SET[1:0]	Constance	2'b00, 2'b01, 2'b10, 2'b11	2'b00	upd0 and upd1 position static control in TSERDES 2'b00: Default position; 2'b01: Advance by one cycle; 2'b10: Advance by two cycles; 2'b11: Advance by three cycles;
LRS_TYPE_DQ2	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local reset/set result of DFF2 in OLOGIC data gear;
LRS_TYPE_DQ3	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local reset/set result of DFF3 in OLOGIC data gear;
GRS_TYPE_TQ	String	"RESET" "SET"	"RESET"	Global reset results of DFF0, DFF1, DFF2, DFF3, and DFF4 in OLOGIC tri-state gear;
LRS_TYPE_TQ0	String	"ASYNC_RESET"	"ASYNC_	Local reset/set result of DFF0 in

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
		"ASYNC_SET" "SYNC_RESET" "SYNC_SET"	RESET"	OLOGIC tri-state gear;
LRS_TYPE_TQ1	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local reset/set result of DFF1 in OLOGIC tri-state gear;
LRS_TYPE_TQ2	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local reset/set result of DFF2 in OLOGIC tri-state gear;
LRS_TYPE_TQ3	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local reset/set result of DFF3 in OLOGIC tri-state gear;
TSERDES_EN	String	"FALSE" "TRUE"	"FALSE"	TSERDES enable *Note: When oserdes is used in conjunction with tserdes, TSERDES_EN equals to "FALSE" in oserdes, and "TRUE" in tserdes. When only oserdes is used, TSERDES_EN equals to "FALSE".
TRI_EN	String	"FALSE" "TRUE"	"FALSE"	Tri-state control enabled IOLHR: *Note: When oserdes is used in conjunction with tserdes, TRI_EN equals to "TRUE" in oserdes, and "FALSE" in tserdes. When only oserdes is used, TRI_EN equals to "TRUE" with the tri-state function enabled, and "FALSE" without the function enabled. IOLHP: Enable when using TSERDES, where TRI_EN = "TRUE"; Disable when not in use, where TRI_EN = "FALSE";
TBYTE_EN	String	"FALSE" "TRUE"	"FALSE"	BYTE control enabled *Note: When oserdes is used in conjunction with tserdes, TBYTE_EN equals to "TRUE" in oserdes, and "FALSE" in tserdes.
TERMBYTE_EN	String	"FALSE" "TRUE"	"FALSE"	TERM BYTE control enable
OCASCADE_EN	String	"FALSE" "TRUE"	"FALSE"	OSERDES extension enabled
TERM_EN	String	"FALSE" "TRUE"	"FALSE"	Terminal control signal TERM enable

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
TERM_OFF_SET	Constance	2'b00, 2'b01, 2'b10, 2'b11	2'b00	Bias when TERM signal disabled (falling edge) 2'b00: Synchronous with tri-state signal; 2'b01: Advance to TI data update (currently not supported); 2'b10: Advance to UPD0 active (currently not supported); 2'b11: Advance to UPD1 active (currently not supported);
TERM_ON_SET	Constance	2'b00, 2'b01, 2'b10, 2'b11	2'b00	Bias when TERM signal enabled (rising edge) 2'b00: Synchronous with tri-state signal; 2'b01: Delay by one cycle; 2'b10: Delay by two cycles; 2'b11: Delay by three cycles;
GRS_EN	String	"FALSE" "TRUE"	"TRUE"	Global reset enable
GRS_TYPE_DQ	String	"RESET" "SET"	"RESET"	Global reset results of DFF0, DFF1, DFF2, DFF3 and DFF4 in OLOGIC data gear;
LRS_TYPE_DQ0	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local reset/set results of DFF0 in OLOGIC data gear;
LRS_TYPE_DQ1	String	"ASYNC_RESET" "ASYNC_SET" "SYNC_RESET" "SYNC_SET"	"ASYNC_RESET"	Local reset/set result of DFF1 in OLOGIC data gear;
MIPI_EN	String	"FALSE" "TRUE"	"FALSE"	MIPI applications not supported, and should be set to "FALSE"

6.20.5 Instantiation Template

```
GTP_OSERDES_E2 #
(
    .GRS_EN ("TRUE"),
    .HPIO("FALSE"),
    .ODELAY_EN("FALSE"),
    .TDELAY_EN("FALSE"),
    .OSERDES_MODE ("SDR4TO1"),
    .TSERDES_MODE ("SDR4TO1"),
    .UPD0_SHIFT_EN ("FALSE"),
    .UPD1_SHIFT_EN ("FALSE"),
    .TUPD0_SHIFT_EN ("FALSE"),
    .TUPD1_SHIFT_EN ("FALSE"),
```

```
. INIT_SET (2'b00),
. TINIT_SET (2'b00),
. GRS_TYPE_DQ ("RESET"),
. LRS_TYPE_DQ0 ("ASYNC_RESET"),
. LRS_TYPE_DQ1 ("ASYNC_RESET"),
. LRS_TYPE_DQ2 ("ASYNC_RESET"),
. LRS_TYPE_DQ3 ("ASYNC_RESET"),
. GRS_TYPE_TQ ("RESET"),
. LRS_TYPE_TQ0 ("ASYNC_RESET"),
. LRS_TYPE_TQ1 ("ASYNC_RESET"),
. LRS_TYPE_TQ2 ("ASYNC_RESET"),
. LRS_TYPE_TQ3 ("ASYNC_RESET"),
. TRI_EN ("FALSE"),
. TSERDES_EN ("FALSE"),
. TBYTE_EN ("FALSE"),
. TERMBYTE_EN ("FALSE"),
. MIPI_EN ("FALSE"),
. OCASCADE_EN ("FALSE"),
. TERM_EN("FALSE"),
. TERM_OFF_SET(2'b00),
. TERM_ON_SET(2'b00),
. OSERDES_FIFO_EN("FALSE"),
. FIFO_DLY(2'b00),
. FIFO_WCLK_INV("FALSE"),
. FIFO_RCLK_INV("FALSE")
) GTP_OSERDES_E2_INST (
. RST (RST),
. OCE (OCE),
. TCE (TCE),
. OCLKDIV (OCLKDIV),
. SERCLK (SERCLK),
. OCLK (OCLK),
. MIPI_CTRL (MIPI_CTRL),
. UPD0_SHIFT (UPD0_SHIFT),
```

. UPD1_SHIFT (UPD1_SHIFT),
. OSHIFTIN0 (OSHIFTIN0),
. OSHIFTIN1 (OSHIFTIN1),
. DI (DI),
. TI (TI),
. TBYTE_IN (TBYTE_IN),
. OSHIFTOUT0 (OSHIFTOUT0),
. OSHIFTOUT1 (OSHIFTOUT1),
. DO (DO),
. TQ (TQ),
. TFB(TFB),
. TERM_FB(TERM_FB),
. FIFO_RST(FIFO_RST),
. FIFO_EN(FIFO_EN),
. FIFO_WCLK(FIFO_WCLK),
. FIFO_RCLK(FIFO_RCLK),
. FIFO_FULL(FIFO_FULL),
. FIFO_EMPTY(FIFO_EMPTY)
);

6.21 GTP_IODELAY_E2

6.21.1 Supported Devices

Table 6-75 GTP_IODELAY_E2-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.21.2 Description of Functionality

GTP_IODELAY_E2 is a data delay unit that supports dynamic or static delay control. For detailed usage instructions, please refer to the "***UG040006_Logos2 Family FPGAs Input/Output Interface (IO) User Guide***". The Structure Block Diagram is shown below. The structure block diagram is shown below:

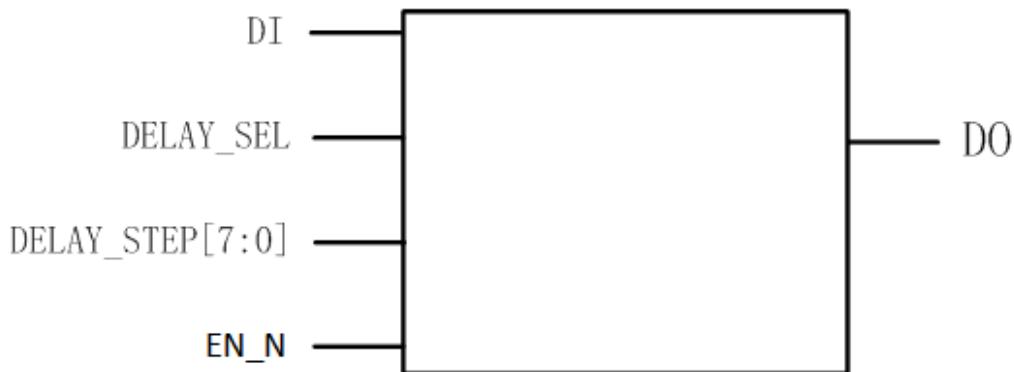


Figure 6-21 GTP_IODELAY_E2 Structure Block Diagram

6.21.3 Port Description

Table 6-76 GTP_IODELAY_E2 Port Description

Port Signal	Input/Output	Bit width	Description
DI	Input	1 bit	Data Input
DELAY_SEL	Input	1 bit	Cascade selection. When DELAY_SEL is 0, both the input and output delays per step are 5ps. When DELAY_SEL is 1, the input delay per step is 10ps, while the output delay per step is 5ps
DELAY_STEP	Input	8 bit	Delay control code configuration (Gray code), with the actual maximum valid value being 8'd247 for input delay and 8'd127 for output delay
DO	Output	1 bit	Data output
EN_N	Input	1 bit	Active low signal

6.21.4 Parameter Description

Table 6-77 GTP_IODELAY_E2 Parameter List Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
DELAY_STEP_SEL	String	"PARAMETER" "PORT"	"PARAMETER"	"PARAMETER": Select static configuration; "PORT": Dynamic configuration
DELAY_STEP_VALUE	Constant	8'h00–8'hF7	8'h00	Static configuration of delay control code (Gray code)
TDELAY_EN	String	"FALSE" "TRUE"	"FALSE"	"TRUE": Map Tian2 HPIO Tdelay function

6.21.5 Instantiation Template

```
GTP_IODELAY_E2 #
(
    .TDELAY_EN("FALSE"),
    .DELAY_STEP_SEL ("PARAMETER"),
    .DELAY_STEP_VALUE( 8'h00 )
) GTP_IODELAY_E2_inst (
    .EN_N(en_n),
    .DI(di),
    .DELAY_SEL(delay_sel),
    .DELAY_STEP(delay_step),
    .DO(do)
);
```

6.22 GTP_ZEROHOLDDELAY

6.22.1 Supported Devices

Table 6-78 GTP_ZEROHOLDDELAY-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.22.2 Description of Functionality

GTP_ZEROHOLDDELAY is a data delay unit that supports static delay control, with a maximum delay of 15 steps (16 delay combinations totally). The structure block diagram is shown below:

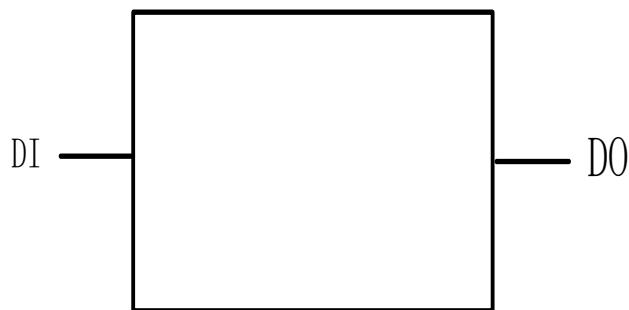


Figure 6-22 GTP_ZEROHOLDDELAY Structure Block Diagram

6.22.3 Port Description

Table 6-79 GTP_ZEROHOLDDELAY Port Description

Port Signal	Input/Output	Description
DI	Input	Data Input
DO	Output	Data output

6.22.4 Parameter Description

Table 6-80 GTP_ZEROHOLDDELAY Parameter List Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
ZHOLD_SET	String	"NODELAY", "100ps", "200ps", "300ps", "400ps", "500ps", "600ps", "700ps", "800ps", "900ps", "1000ps", "1100ps", "1200ps", "1300ps", "1400ps", "1500ps"	"NODELAY"	zeroholddelay delay control code

6.22.5 Instantiation Template

```
GTP_ZEROHOLDDELAY #
(
    .ZHOLD_SET ("NODELAY")
) GTP_ZEROHOLDDELAY_inst (
    .DI (di),
    .DO (do)
);
```

6.23 GTP_IOBUFCO_E1

6.23.1 Supported Devices

Table 6-81 GTP_IOBUFCO_E1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.23.2 Description of Functionality

GTP_IOBUFCO_E1 supports differential input and pseudo-differential (two single-ended) output driving function. The structure block diagram is shown below:

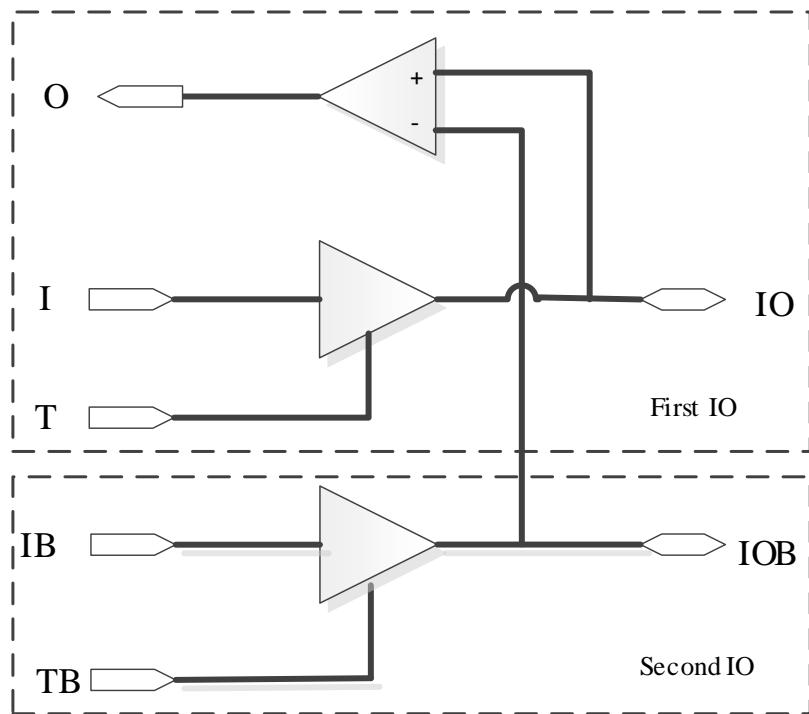


Figure 6-23 GTP_IOBUFCO_E1

6.23.3 Port Description

Table 6-82 GTP_IOBUFCO_E1 Port List Description

Port	Direction	Function Description
I	IN	First IO single-ended signal input
IB	IN	Second IO single-ended signal input
O	OUT	Output from input buffer to the chip
T	IN	First IO tri-state enable
TB	IN	Second IO tri-state enable
IO	INOUT	The first IO's PAD
IOB	INOUT	The second IO's PAD, opposite to IO's value

6.23.4 Parameter Description

Table 6-83 GTP_IOBUFCO_E1 Parameter List Description

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	Refer to Table 6-83	DEFAULT	IO Standard
TERM_DDR	"ON", "OFF"	"ON"	The built-in termination resistor is enabled or disabled during HSTL and SSTL standard inputs

Table 6-84 GTP_IOBUFCO_E1 Valid Parameter Values

GTP_IOBUFCO_E1	
IOSTANDARD	TERM_DDR
SSTL18D_I	OFF/ON
SSTL18D_II	OFF/ON
SSTL15D_I	OFF/ON
SSTL15D_II	OFF/ON
SSTL135D_I	OFF/ON
SSTL135D_II	OFF/ON
HSTL15D_I	OFF/ON
HSTL15D_II	OFF/ON
HSTL18D_I	OFF/ON
HSTL18D_II	OFF/ON
HSUL12D	OFF/ON

6.23.5 Instantiation Template

```

GTP_IOBUFCO_E1 #(
    .IOSTANDARD("DEFAULT"),
    .TERM_DDR("ON")
) GTP_IOBUFCO_E1_inst (
    .IO(), // INOUT
    .IOB(),// INOUT
    .O(), // OUTPUT
    .I(), // INPUT
    .IB(), // INPUT
    .T(), // INPUT
    .TB() // INPUT
);

```

6.24 GTP_OUTBUFCO_E1

6.24.1 Supported Devices

Table 6-85 GTP_OUTBUFCO_E1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.24.2 Description of Functionality

GTP_OUTBUFCO_E1 supports pseudo-differential (two single-ended) output driving function. It is shown in the following figure:

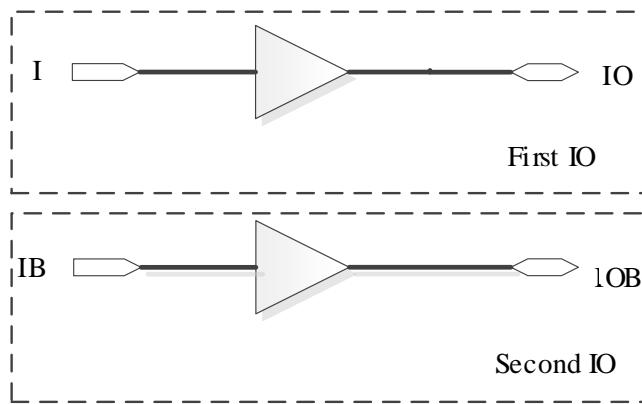


Figure 6-24 GTP_OUTBUFCO_E1

6.24.3 Port Description

Table 6-86 GTP_OUTBUFCO_E1 Port List Information

Port	Direction	Function Description
I	IN	First IO single-ended signal input
IB	IN	The second IO's single-end signal input, opposite to I's value
O	OUT	The first IO's PAD
OB	OUT	The second IO's PAD, opposite to IO's value

6.24.4 Parameter Description

Table 6-87 GTP_OUTBUFCO_E1 Parameter List Information

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	Refer to Table 6-88	DEFAULT	IO Standard

Table 6-88 GTP_OUTBUFCO_E1 Valid Parameter Values

GTP_OUTBUFCO_E1
IOSTANDARD
SSTL18D_I
SSTL18D_II
SSTL15D_I
SSTL15D_II
SSTL135D_I
SSTL135D_II
HSTL15D_I
HSTL15D_II
HSTL18D_I
HSTL18D_II
HSUL12D

6.24.5 Instantiation Template

```
GTP_OUTBUFCO_E1 #(
    .IOSTANDARD("DEFAULT")
) GTP_OUTBUFCO_E1_inst (
    .O(), // OUTPUT
    .OB(),// OUTPUT
    .I(), // INPUT
    .IB() // INPUT
);
```

6.25 GTP_OUTBUFTCO_E1

6.25.1 Supported Devices

Table 6-89 GTP_OUTBUFTCO_E1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.25.2 Description of Functionality

GTP_OUTBUFTCO_E1 supports pseudo-differential (two single-ended) output driving function. It is shown in the following figure:

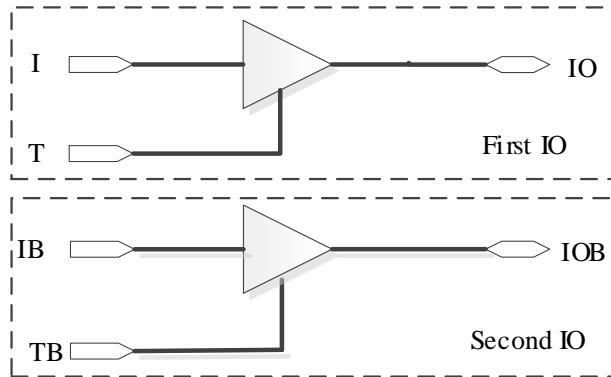


Figure 6-25 GTP_OUTBUFTCO_E1

6.25.3 Port Description

Table 6-90 GTP_OUTBUFTCO_E1 Port List Description

Port	Direction	Function Description
I	IN	First IO single-ended signal input
IB	IN	The second IO's single-end signal input, opposite to I's value
T	IN	First IO tri-state enable
TB	IN	Second IO tri-state enable
O	OUT	The first IO's PAD
OB	OUT	The second IO's PAD, opposite to IO's value

6.25.4 Parameter Description

Table 6-91 GTP_OUTBUFTCO_E1 Parameter Description

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	Refer to Table 6-92	DEFAULT	IO Standard

Table 6-92 GTP_OUTBUFTCO_E1 Valid Parameter Values

GTP_OUTBUFTCO_E1	
IOSTANDARD	
SSTL18D_I	
SSTL18D_II	
SSTL15D_I	
SSTL15D_II	
SSTL135D_I	
SSTL135D_II	
HSTL15D_I	
HSTL15D_II	
HSTL18D_I	
HSTL18D_II	
HSUL12D	

6.25.5 Instantiation Template

```

GTP_OUTBUFTCO_E1 #(
    .IOSTANDARD("DEFAULT")
) GTP_OUTBUFTCO_E1_inst (
    .O(), // OUTPUT
    .OB(),// OUTPUT
    .I(), // INPUT
    .IB(),// INPUT
    .T(), // INPUT
    .TB() // INPUT
);

```

6.26 GTP_INBUFDS_E1

6.26.1 Supported Devices

Table 6-93 GTP_INBUFDS_E1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.26.2 Description of Functionality

GTP_INBUFDS_E1 supports differential input driving function. It is shown in the following figure:

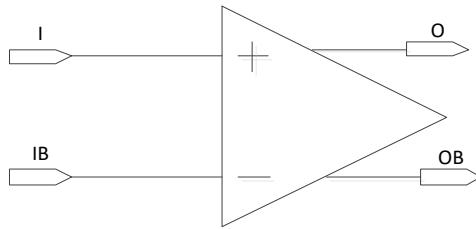


Figure 6-26 GTP_INBUFDS_E1

6.26.3 Port Description

Table 6-94 GTP_INBUFDS_E1 Port List Description

Port	Direction	Function Description
I	Input	Differential P input signals
IB	Input	Differential N input signals
O	Output	Output signal
OB	Output	Differential output inversion data, to the inside of the chip

6.26.4 Parameter Description

Table 6-95 GTP_INBUFDS_E1 Parameter List

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	"LVDS", "MINI-LVDS", "LVPECL", "SUB-LVDS", "SSTL18D_I", "SSTL18D_II", "SSTL15D_I", "SSTL15D_II", "HSTL18D_I", "HSTL18D_II", "HSTL15D_I", "SSTL25D_I", "RSDS", "PPDS", "TMDS", "SSTL25D_II", "BLVDS", "SSTL15D_I_CAL", "SSTL15D_II_CAL", "HSTL15D_I_CAL", "SSTL135D_I", "SSTL135D_II", "SSTL12D", "HSTL12D_I", "HSUL12D", "POD12D", "SSTL18D_I_CAL", "SSTL18D_II_CAL", "SSTL135D_II_CAL", "SSTL12D_CAL", "HSTL15D_II_CAL", "HSTL18D_I_CAL", "HSTL18D_II_CAL", "HSTL12D_I_CAL", "HSUL12D_CAL", "POD12D_CAL", "LVDS_18", "LVCMOS33D", "LVCMOS25D", "LVCMOS18D"	"DEFAULT"	IO Standard
TERM_DIFF	"ON", "OFF"	"ON"	The built-in termination resistor is enabled or disabled during differential input

6.26.5 Instantiation Template

```
GTP_INBUFDS_E1#(
    .IOSTANDARD ("DEFAULT"),
    .TERM_DIFF("ON")
)
GTP_INBUFDS_E1_inst (
    .I      (i),
    .IB     (ib),
    .O      (o),
    .OB     (ob)
);
```

6.27 GTP_INBUFEDS_E1

6.27.1 Supported Devices

Table 6-96 GTP_INBUFEDS_E1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

6.27.2 Description of Functionality

GTP_INBUFEDS_E1 supports input function. Compared to GTP_INBUFDS_E1, GTP_INBUFEDS_E1 adds an EN signal that can disable the input, while other characteristics remain same.

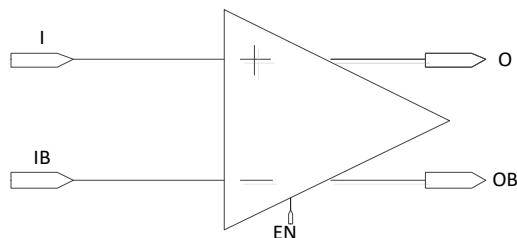


Figure 6-27 GTP_INBUFEDS_E1

6.27.3 Port Description

Table 6-97 GTP_INBUFEDS_E1 Port List Description

Port	Direction	Function Description
I	Input	Differential P input signals
IB	Input	Differential N input signals
O	Output	Output signal
OB	Output	Differential output inversion data, to the inside of the chip

6.27.4 Parameter Description

Table 6-98 GTP_INBUFEDS_E1 Parameter List

Parameter Name	Setting Value	Defaults	Function Description
IOSTANDARD	"LVDS", "MINI-LVDS", "LVPECL", "SUB-LVDS", "SSTL18D_I", "SSTL18D_II", "SSTL15D_I", "SSTL15D_II", "HSTL18D_I", "HSTL18D_II", "HSTL15D_I", "SSTL25D_I", "RSDS", "PPDS", "TMDS", "SSTL25D_II", "BLVDS", "SSTL15D_I_CAL", "SSTL15D_II_CAL", "HSTL15D_I_CAL", "SSTL135D_I", "SSTL135D_II", "SSTL12D", "HSTL12D_I", "HSUL12D", "POD12D", "SSTL18D_I_CAL", "SSTL18D_II_CAL", "SSTL135D_I_CAL", "SSTL135D_II_CAL", "SSTL12D_CAL", "HSTL15D_II_CAL", "HSTL18D_I_CAL", "HSTL18D_II_CAL", "HSTL12D_CAL", "POD12D_CAL", "LVDS_18", "LVCMOS33D", "LVCMOS25D", "LVCMOS18D"	"DEFAULT"	IO Standard
TERM_DIFF	"ON", "OFF"	"ON"	The built-in termination resistor is enabled or disabled during differential input

6.27.5 Instantiation Template

```
GTP_INBUFEDS_E1#(
    .IOSTANDARD ("DEFAULT"),
    .TERM_DIFF("ON")
)
GTP_INBUFEDS_E1_inst (
    .I      (i),
    .IB     (ib),
    .O      (o),
    .OB     (ob)
);
```

Chapter 7 Usage Instructions for Clock-Related GTPs

7.1 GTP_CLKBUFG

7.1.1 Supported Devices

Table 7-1 GTP_CLKBUFG-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

7.1.2 Description of Functionality

GTP_CLKBUFG provides a simple clock BUFFER function and can be instantiated to implement the global clock.

7.1.3 Port Description

Table 7-2 GTP_CLKBUFG Port Description

Port Signal	Input/Output	Description
CLKIN	Input	Input Clock
CLKOUT	Output	Output clock

7.1.4 Instantiation Template

```
GTP_CLKBUFG U_CLKBUFG (
    .CLKOUT      (clkout),
    .CLKIN       (clkin )
);
```

7.1.5 Detailed Description of Functionality

GTP_CLKBUFG provides a simple clock BUFFER function and can be instantiated to implement the global clock.

7.2 GTP_CLKBUFGCE

7.2.1 Supported Devices

Table 7-3 GTP_CLKBUFGCE-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

7.2.2 Description of Functionality

GTP_CLKBUFGCE is a clock BUFFER with an enable control port and can be instantiated to implement the global clock.

7.2.3 Port Description

Table 7-4 GTP_CLKBUFGCE Port Description

Port Signal	Input/Output	Description
CLKIN	Input	Input Clock
CE	Input	Clock enable signal (active-high)
CLKOUT	Output	Output clock

7.2.4 Parameter Description

Table 7-5 GTP_CLKBUFGCE Parameter List Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
DEFAULT_VALUE	Character	1'b0, 1'b1	1'b0	When CE = 0, output DEFAULT_VALUE; When CE=1, output CLKIN;
SIM_DEVICE	string	"TITAN" "LOGOS" "COMPACT" "LOGOS2" "TITAN2"	"TITAN"	Simulation parameter

7.2.5 Instantiation Template

```
GTP_CLKBUFGCE
#(.DEFAULT_VALUE      (1'b0      ), //1'b0; 1'b1
.SIM_DEVICE("TITAN")
) I_GTP_CLKBUFGCE (
.CLKIN      (clk      ),
.CE         (ce      ),
.CLKOUT     (clkout )
);
```

7.2.6 Detailed Description of Functionality

When CE = 1, output clock equals to input clock. When CE transitions from high to low levels, detect the falling edge of CLKIN twice before CLKOUT outputs translation from a low level to CLKIN. Until CE returns to a high level, the falling edge of CLKIN be detected twice before CLKOUT outputs translation from a low level to CLKIN.

When DEFAULT_VALUE = 1'b0, the Timing Diagrams are shown as follows:

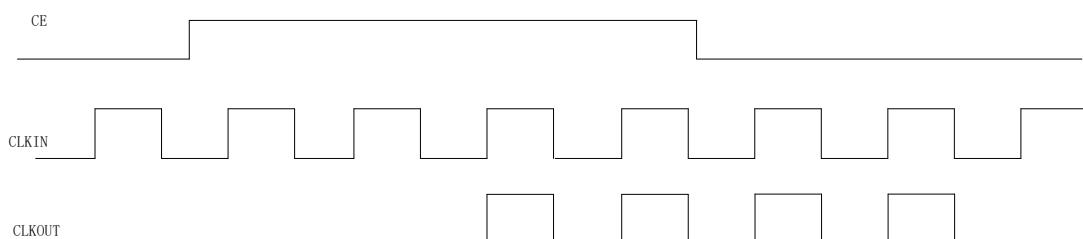


Figure 7-1 GTP_CLKBUFGCE Timing Diagrams (DEFAULT_VALUE = 0)

When DEFAULT_VALUE = 1'b1, the Timing Diagrams are shown as follows:

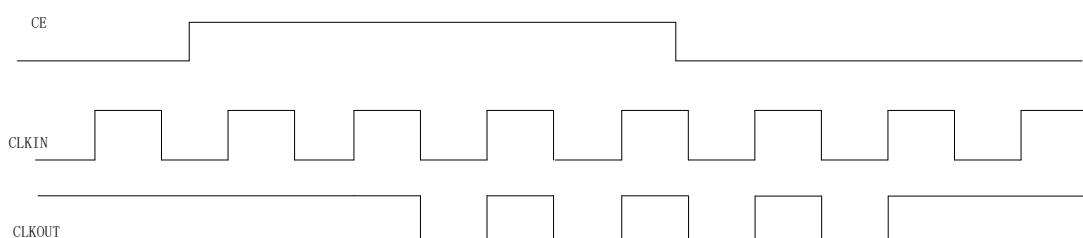


Figure 7-2 GTP_CLKBUFGCE Timing Diagrams (DEFAULT_VALUE = 1)

7.3 GTP_CLKBUFGMUX

7.3.1 Supported Devices

Table 7-6 GTP_CLKBUFGMUX-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

7.3.2 Description of Functionality

GTP_CLKBUFGMUX can be used for dynamic switching between two global clock input sources, allowing users to choose forced switching (corresponding to TRIGGER_MODE = "NORMAL") or debounced switching triggered by the falling edge of the clock (corresponding to TRIGGER_MODE = "NEGEDGE"), or debounced switching triggered by the rising edge of the clock (corresponding to TRIGGER_MODE = "POSEDGE"). Note that forced switching may introduce glitches, and users need to reset the related logic after switching to achieve the intended functionality.

7.3.3 Port Description

Table 7-7 GTP_CLKBUFGMUX Port Description

Port Signal	Input/Output	Description
CLKIN0	Input	Input clock CLKIN0
CLKIN1	Input	Input clock CLKIN1
SEL	Input	Clock selection signal: 0 for CLKIN0; 1 for CLKIN1;
CLKOUT	Output	Output clock

7.3.4 Parameter Description

Table 7-8 GTP_CLKBUFGMUX Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
TRIGGER_MODE	<string>	"NORMAL" "NEGEDGE" "POSEDGE"	"NORMAL"	(1) "NORMAL": In this mode, input clocks (CLKIN0 and CLKIN1) can be freely switched and the GLITCHLESS feature is not available (2) "NEGEDGE": In this mode, input clocks (CLKIN0 and CLKIN1) can be freely switched and the GLITCHLESS feature triggered on the falling edge of the clock is available. (3) "POSEDGE": In this mode, input clocks (CLKIN0 and CLKIN1) can be freely switched and the GLITCHLESS feature triggered on the rising edge of the clock is available.
SIM_DEVICE	string	"TITAN" "LOGOS" "COMPACT" "LOGOS2" "TITAN2"	"TITAN"	Simulation Model Device Identification "TITAN": When triggered on a rising or falling edge, it switches after 2 beats of the clock "LOGOS", "COMPACT", "LOGOS2" and "TITAN2": When triggered on a rising or falling edge, it switches after 4 beats of the clock

Notes:

1. The LOGOS2 Family supports "NORMAL", "NEGEDGE" and "POSEDGE" modes. For modes supported by other devices, please refer to the corresponding clock resource user guide.
2. When TRIGGER_MODE is set to "NEGEDGE" or "POSEDGE", the clocks can be only switched when the rising or falling edge of the clock is captured in both clock domains. Therefore, the GTP can only be used to switch clocks normally when both CLKIN0/CLKIN1 ports have a rising or falling edge.

7.3.5 Instantiation Template

GTP_CLKBUFGMUX

```
#(
    .TRIGGER_MODE("NORMAL"), // "NORMAL", "NEGEDGE"
    .SIM_DEVICE("TITAN")

    )I_CLKBUFGMUX (
        .CLKIN0      (clkin0 ),
        .CLKIN1      (clkin1 ),
        .SEL         (sel     ),
        .CLKOUT      (clkout )
);
```

7.3.6 Detailed Description of Functionality

Instantiated GTP_CLKBUFGMUX can be used for dynamic switching between two global clock input sources. When the TRIGGER_MODE parameter is set to "NORMAL", the CLKOUT is switched immediately after the SEL signal toggles. The corresponding timing diagram is as follows:

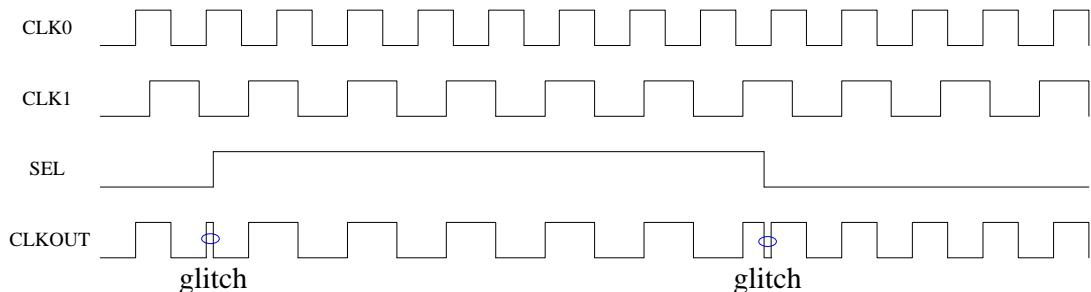


Figure 7-3 Timing Diagram for GTP_CLKBUFGMUX with Parameter TRIGGER_MODE = "NORMAL"

When the parameter TRIGGER_MODE is set to "NEGEDGE" and the value of the parameter SIM_DEVICE is "LOGOS2", if SEL switches from 0 to 1, detect the falling edge of the current clock CLKIN0 twice (maintaining the CLKOUT output as the current clock during the detection of the rising edge of the current clock) and then the falling edge of the switch-to clock CLKIN1 twice (with the CLKOUT output low during the detection of the falling edge of the switch-to clock). After the detection is completed, CLKOUT switches from CLKIN0 to CLKIN1. Otherwise, if SEL changes from 1 to 0, detect the falling edge of CLKIN1 twice (maintaining the CLKOUT output as the current clock during the detection of the rising edge of the current clock) and then the falling edge of CLKIN0 twice (with the CLKOUT output low during the detection of the falling edge of the switch-to clock CLKIN0). After the detection is completed, CLKOUT switches from CLKIN1 to CLKIN0. The corresponding timing diagram is as follows:

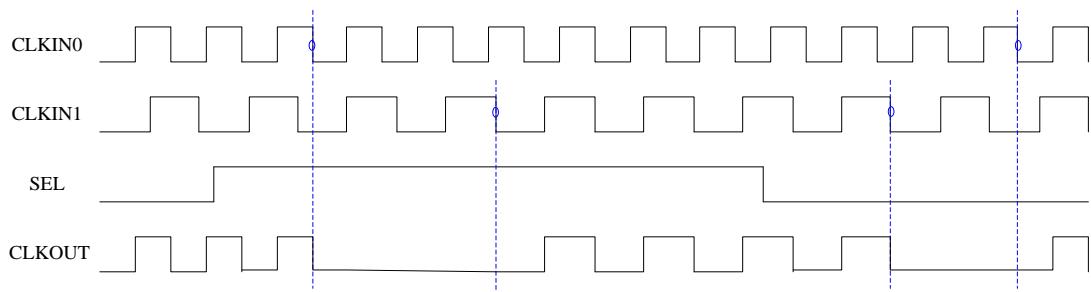


Figure 7-4 Timing Diagram for GTP_CLKBUFGMUX with Parameter TRIGGER_MODE = "NEGEDGE"

When the parameter TRIGGER_MODE is set to "POSEDGE" and the value of the parameter SIM_DEVICE is "LOGOS2", if SEL switches from 0 to 1, detect the rising edge of the current clock CLKIN0 twice (maintaining the CLKOUT output as the current clock during the detection of the rising edge of the current clock) and then the rising edge of the switch-to clock CLKIN1 twice

(with the CLKOUT output high during the detection of the rising edge of the switch-to clock). After the detection is completed, CLKOUT switches from CLKIN0 to CLKIN1. Otherwise, if SEL changes from 1 to 0, detect the rising edge of CLKIN1 twice (maintaining the CLKOUT output as the current clock during the detection of the rising edge of the current clock) and then the rising edge of CLKIN0 twice (with the CLKOUT output high during the detection of the rising edge of the switch-to clock CLKIN0). After the detection is completed, CLKOUT switches from CLKIN1 to CLKIN0. The corresponding timing diagram is as follows:

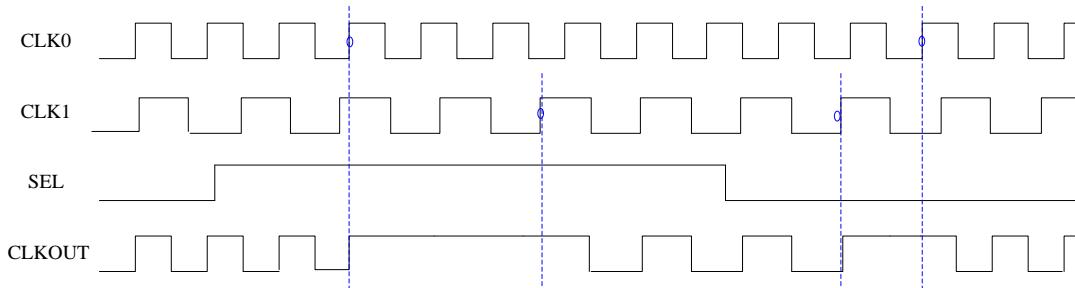


Figure 7-5 Timing Diagram for GTP_CLKBUFGMUX with Parameter TRIGGER_MODE = "POSEDGE"

7.4 GTP_CLKBUFR

7.4.1 Supported Devices

Table 7-9 GTP_CLKBUFR-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

7.4.2 Description of Functionality

GTP_CLKBUFR is a regional clock BUFFER, driving the logic units of a certain area.

7.4.3 Port Description

Table 7-10 GTP_CLKBUFR Port Description

Port Signal	Input/Output	Description
CLKIN	Input	Input Clock
CLKOUT	Output	Output clock

7.4.4 Instantiation Template

```
GTP_CLKBUFR U_BUFR(
    .CLKOUT      (clkout),
    .CLKIN       (clkin )
);
```

7.4.5 Detailed Description of Functionality

GTP_CLKBUFR is a regional clock BUFFER, driving the logic units of a certain area. The figure below shows the input and output timing diagrams of GTP_CLKBUFR.

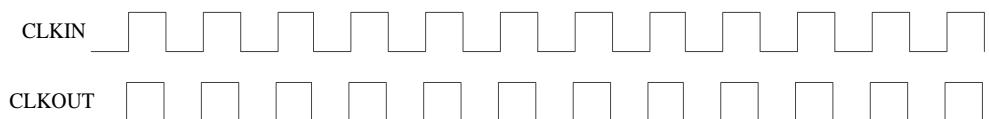


Figure 7-6 Timing Diagram of GTP_CLKBUFR

7.5 GTP_IOCLKBUF

7.5.1 Supported Devices

Table 7-11 GTP_IOCLKBUF-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

7.5.2 Description of Functionality

GTP_IOCLKBUF is a IO clock Buffer.

7.5.3 Port Description

Table 7-12 GTP_IOCLKBUF Port Description

Port Signal	Input/Output	Description
CLKIN	Input	Input Clock
DI	Input	Clock enable, not supported by Logos2. The CLKOUT output clock is independent of both high and low levels
CLKOUT	Output	Output clock

7.5.4 Parameter Description

Table 7-13 GTP_IOCLKBUF Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GATE_EN	<string>	<" FALSE "," TRUE ">	<"FALSE">	Logos2 can only be configured as "FALSE"

Note: The parameter GATE_EN of the Logos2 Family only accepts "FALSE"

7.5.5 Instantiation Template

```
GTP_IOCLKBUF
#(
    .GATE_EN      ("FALSE"  ), //FALSE; TRUE
    ) u_IOCLKBUF (
        .CLKOUT     (clkout ),
        .CLKIN      (clin    ),
        .DI         (di      )
    );
```

7.5.6 Detailed Description of Functionality

For the introduction of detailed functions, please refer to the IO clock GTP chapter of "**UG040004_Logos2 Family FPGAs Clock Resources (Clock) User Guide**".

7.6 GTP_IOCLKDIV_E2

7.6.1 Supported Devices

Table 7-14 GTP_IOCLKDIV_E2-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

7.6.2 Description of Functionality

GTP_IOCLKDIV_E2 has 3 inputs (CLKIN, RST_N, CE), 1 output (CLKDIVOUT) and 1 parameter (DIV_FACTOR). Division by 1, 2, 3, 4, 5, 6, 7, 8 and direct pass-through (BYPASS) can be achieved through DIV_FACTOR control. For divisions by odd numbers, the duration of the high pulse width is one input clock cycle shorter than that of the low pulse width.

CE represents the asynchronous enable control. When $CE = 0$, CLKDIVOUT maintains the current level. When $CE = 1$, CLKDIVOUT outputs divided clock.

RST_N represents the reset signal, supporting asynchronous reset and synchronous release. When $RST_N = 0$, the output clock is cleared. The BYPASS mode is not affected by CE or RST_N.

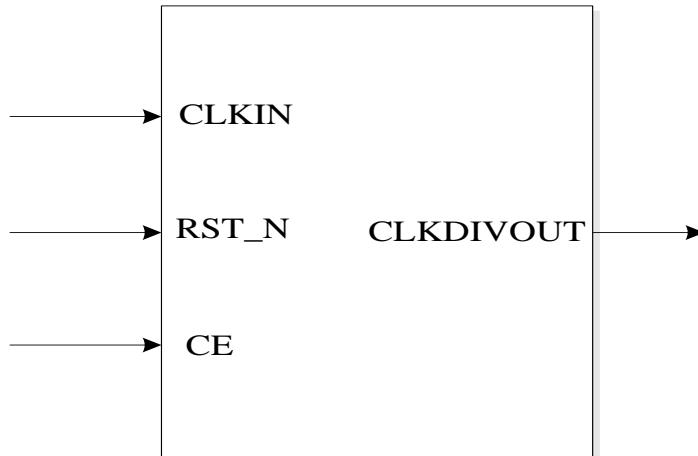


Figure 7-7 GTP_IOCLKDIV_E2 Structure Diagram

7.6.3 Port Description

Table 7-15 GTP_IOCLKDIV_E2 Port Description

Port Signal	Input/Output	Description
CLKIN	Input	Input Clock
RST_N	Input	Reset signal, active low
CE	Input	Enable control: $CE = 1$: Output divided clock signal $CE = 0$, output clock maintains current level
CLKDIVOUT	Output	Output clock

7.6.4 Parameter Description

Table 7-16 GTP_IOCLKDIV_E2 Parameter List Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
DIV_FACTOR	<string>	"BYPASS" "1" "2" "3" "4" "5""6" "7" "8"	"BYPASS"	Mode selection includes pass-through mode and 1~8 division modes.

7.6.5 Instantiation Template

```
GTP_IOCLKDIV_E2 #(
    .DIV_FACTOR("BYPASS")
) GTP_IOCLKDIV_E2_inst (
    .CLKDIVOUT (clkdivout),
    .CE        (ce      ),
    .CLKIN     (clkin   ),
    .RST_N     (rst_n   )
);
```

7.7 GTP_CLKBUFMCE

7.7.1 Supported Devices

Table 7-17 GTP_CLKBUFMCE-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

7.7.2 Description of Functionality

GTP_CLKBUFMCE can drive two clock regions in the vertical direction, with 2 inputs (CLKIN, CE), 1 output (CLKOUT), and 3 configuration parameters (CE_TYPE, TRIGGER_MODE, CE_INV).

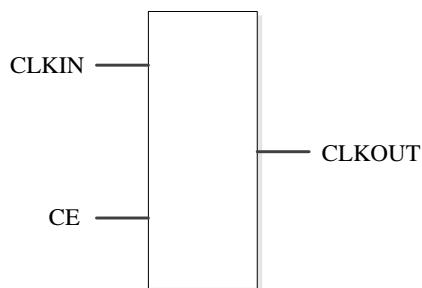


Figure 7-8 GTP_CLKBUFMCE Structure Diagram

7.7.3 Port Description

Table 7-18 GTP_CLKBUFMCE Port Description

Port Signal	Input/Output	Description
CLKIN	Input	Input clock signal
CE	Input	Clock enable signal
CLKOUT	Output	Output clock signal

7.7.4 Parameter Description

Table 7-19 GTP_CLKBUFMCE Parameter List Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
CE_TYPE	<string>	"SYNC", "ASYNC"	"SYNC"	CE_TYPE = "SYNC": Synchronous enable. CE_TYPE = "ASYNC": Asynchronous enable.
TRIGGER_MODE	<string>	"POSEDGE", "NEGEDGE"	"POSEDGE"	TRIGGER_MODE = "POSEDGE": Initial clock output value is 1'b1, triggered on the rising edge. TRIGGER_MODE = "NEGEDGE": Initial clock output value is 1'b0, triggered on the falling edge.
CE_INV	<string>	"TRUE", "FALSE"	"FALSE"	EN_INV = "FALSE": CE high active by default. EN_INV = "TRUE": CE low active by default.

7.7.5 Instantiation Template

```

GTP_CLKBUFMCE #(
    .CE_TYPE("SYNC"),
    .CE_INV("FALSE"),
    .TRIGGER_MODE("POSEDGE")
) GTP_CLKBUFMCE_inst (
    .CLKOUT      (clkout),
    .CE          (ce      ),
    .CLKIN       (clkin )
);
    
```

7.8 GTP_CLKBUFM

7.8.1 Supported Devices

Table 7-20 GTP_CLKBUFM-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

7.8.2 Description of Functionality

GTP_CLKBUFM can drive two clock regions in the vertical direction with one input (CLKIN), one output (CLKOUT) and no parameters.

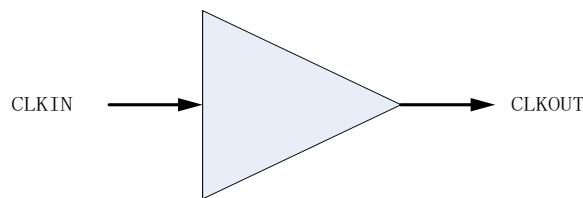


Figure 7-9 GTP_CLKBUFM Structure Diagram

7.8.3 Port Description

Table 7-21 GTP_CLKBUFM Port Description

Port Signal	Input/Output	Description
CLKIN	Input	Input Clock
CLKOUT	Output	Output clock

7.8.4 Instantiation Template

```

GTP_CLKBUFM GTP_CLKBUFM_inst (
    .CLKOUT(clkout),
    .CLKIN(clkin)
);
  
```

7.9 GTP_CLKBUFXCE

7.9.1 Supported Devices

Table 7-22 GTP_CLKBUFXCE-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

7.9.2 Description of Functionality

GTP_CLKBUFXCE can drive two clock regions in the vertical direction with 2 inputs (CLKIN, CE), 1 output (CLKOUT), and 3 configuration parameters (CE_TYPE, TRIGGER_MODE, CE_INV).

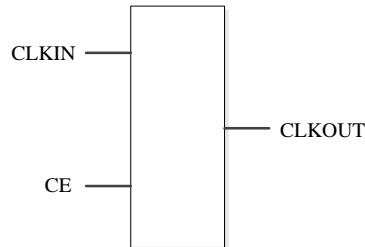


Figure 7-10 GTP_CLKBUFXCE Structure Diagram

7.9.3 Port Description

Table 7-23 GTP_CLKBUFXCE Port Description

Port Signal	Input/Output	Description
CLKIN	Input	Input clock signal
CE	Input	Clock enable end
CLKOUT	Output	Output clock signal

7.9.4 Parameter Description

Table 7-24 GTP_CLKBUFXCE Parameter List Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
CE_TYPE	<string>	"SYNC", "ASYNC"	"SYNC"	CE_TYPE = "SYNC": Synchronous enable. CE_TYPE = "ASYNC": Asynchronous enable.
TRIGGER_MODE	<string>	"POSEDGE", "NEGEDGE"	"POSEDGE"	TRIGGER_MODE = "POSEDGE": Initial clock output value is 1'b1, triggered on the rising edge. TRIGGER_MODE = "NEGEDGE": Initial clock output value is 1'b0, triggered on the falling edge.
CE_INV	<string>	"TRUE", "FALSE"	"FALSE"	EN_INV = "FALSE": CE high active by default. EN_INV = "TRUE": CE low active by default.

7.9.5 Instantiation Template

```
GTP_CLKBUFXCE #(
    .CE_TYPE("SYNC"),
    .CE_INV("FALSE"),
    .TRIGGER_MODE("POSEDGE")
) GTP_CLKBUFXCE_inst (
    .CLKOUT (clkout),
    .CE      (ce      ),
    .CLKIN   (clkin )
);
```

7.10 GTP_CLKBUFX

7.10.1 Supported Devices

Table 7-25 GTP_CLKBUFX-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

7.10.2 Description of Functionality

GTP_CLKBUFX can drive two clock regions in the vertical direction with one input (CLKIN), one output (CLKOUT) and no parameters.

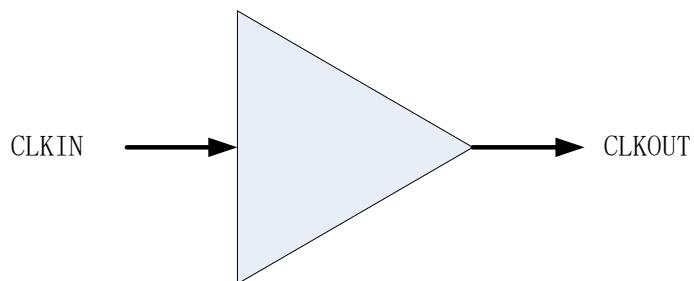


Figure 7-11 GTP_CLKBUFX Structure Diagram

7.10.3 Port Description

Table 7-26 GTP_CLKBUFX Port Description

Port Signal	Input/Output	Description
CLKIN	Input	Input Clock
CLKOUT	Output	Output clock

7.10.4 Instantiation Template

```
GTP_CLKBUFX GTP_CLKBUFX_inst (
    .CLKOUT(clkout),
    .CLKIN(clkin)
);
```

7.11 GTP_GPLL

7.11.1 Supported Devices

Table 7-27 GTP_GPLL-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

7.11.2 Description of Functionality

The Structure Block Diagram of GPLL is shown below.

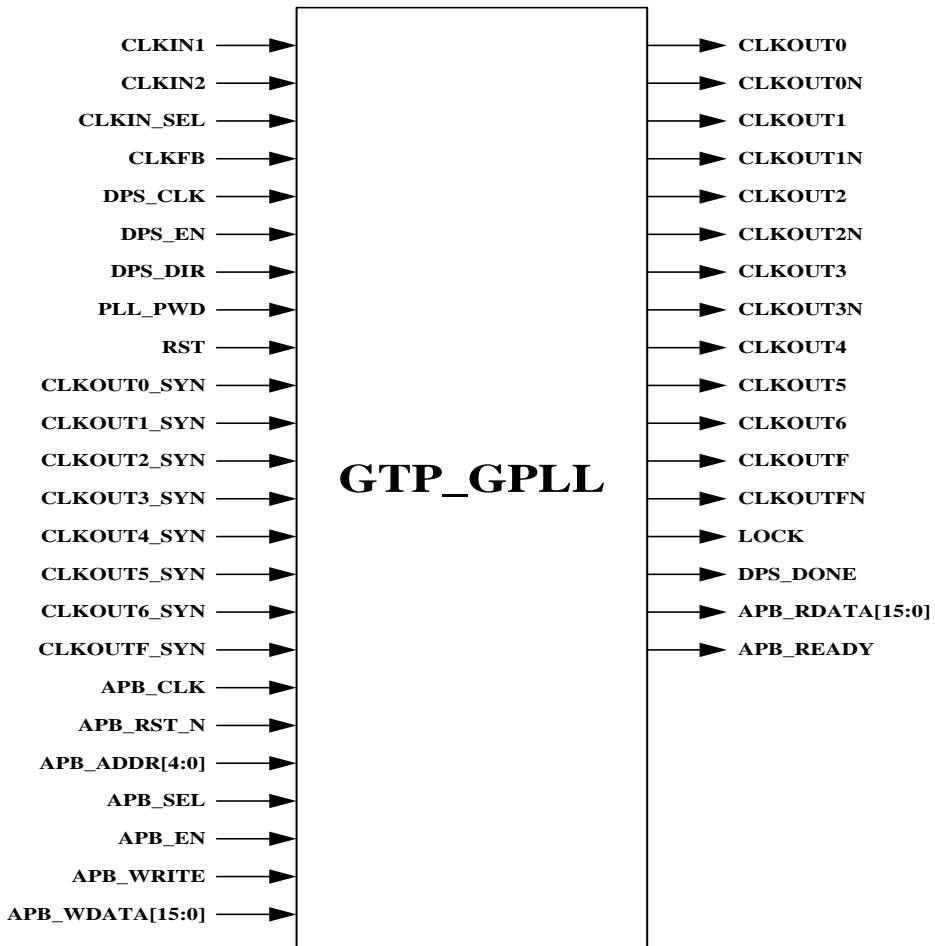


Figure 7-12 GTP_GPLL Structure Block Diagram

7.11.3 Port Description

Table 7-28 GTP_GPLL Port Description

Port Signal	Input/Output	Description
CLKOUT0	Output	PLL Channel 0 Positive Phase Output Clock;
CLKOUT0N	Output	PLL Channel 0 Inverted Phase Output Clock;
CLKOUT1	Output	PLL Channel 1 Positive Phase Output Clock;
CLKOUT1N	Output	PLL Channel 1 Inverted Phase Output Clock;
CLKOUT2	Output	PLL Channel 2 Positive Phase Output Clock;
CLKOUT2N	Output	PLL Channel 2 Inverted Phase Output Clock;
CLKOUT3	Output	PLL Channel 3 Positive Phase Output Clock;
CLKOUT3N	Output	PLL Channel 3 Inverted Phase Output Clock;
CLKOUT4	Output	PLL Channel 4 Output Clock;
CLKOUT5	Output	PLL Channel 5 Output Clock;
CLKOUT6	Output	PLL Channel 6 Output Clock;
CLKOUTF	Output	PLL Feedback Positive Phase Output Clock;
CLKOUTFN	Output	PLL Feedback Inverted Phase Output Clock;
LOCK	Output	PLL frequency lock indicator signal, asynchronous; When the signal is pulled high, it indicates that the PLL feedback clock signal is locked to the input clock signal;
DPS_DONE	Output	Dynamic interpolation phase shift adjustment indicator signal;
APB_RDATA[15:0]	Output	PLL APB interface data bus data output
APB_READY	Output	PLL APB interface data bus handshake signal; indicates the end of a normal bus cycle;
CLKIN1	Input	PLL reference input clock 1;
CLKIN2	Input	PLL reference input clock 2;
CLKFB	Input	PLL feedback clock;
CLKIN_SEL	Input	Input clock selection signal;
DPS_CLK	Input	Dynamic interpolation phase shift adjustment clock;
DPS_EN	Input	Dynamic interpolation phase shift adjustment enable; active high;
DPS_DIR	Input	Select the direction for dynamic phase shift adjustment; 1'b0: lag, 1'b1: lead;
PLL_PWD	Input	PLL Power Down, active high;
RST	Input	PLL reset signal, active high;
CLKOUT0_SYN	Input	CLKOUT0/N output clock enable control; active high; high level disables, low level enables;
CLKOUT1_SYN	Input	CLKOUT1/N output clock enable control; active high; high level disables, low level enables;
CLKOUT2_SYN	Input	CLKOUT2/N output clock enable control; active high; high level disables, low level enables;
CLKOUT3_SYN	Input	CLKOUT3/N output clock enable control; active high; high level disables, low level enables;
CLKOUT4_SYN	Input	CLKOUT4 output clock enable control; active high; high level disables, low level enables;
CLKOUT5_SYN	Input	CLKOUT5 output clock enable control; active high; high level disables, low level enables;

Port Signal	Input/Output	Description
CLKOUT6_SYN	Input	CLKOUT6 output clock enable control; active high; high level disables, low level enables;
CLKOUTF_SYN	Input	CLKOUTF/N output clock enable control; active high; high level disables, low level enables;
APB_CLK	Input	PLL APB interface data bus clock;
APB_RST_N	Input	PLL APB interface data bus asynchronous reset signal, active low;
APB_ADDR	Input	PLL APB interface data bus address;
APB_SEL	Input	PLL APB interface data bus selection signal to select the slave device;
APB_EN	Input	The PLL APB port data bus enable signal, indicating the second and subsequent cycles of transmission;
APB_WRITE	Input	PLL APB interface data bus write enable signal; 1'b0: read operation, 1'b0: write operation;
APB_WDATA[15:0]	Input	PLL APB interface data bus data input;

7.11.4 Paramater Description

Table 7-29 GTP_GPLL Parameter List Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
CLKIN_FREQ	real	10~800	50.0	Input clock frequency configuration, MHz;
LOCK_MODE	binary	1'b0, 1'b1	1'b0	PLL frequency detection mode configuration; 1'b0: Real-time monitoring of PLL working state; 1'b1: The PLL lock remains after locking, unless reset or power-down;
STATIC_RATIOI	interger	1-80	1	Enter divider ratio static configuration;
STATIC_RATIOM	interger	1-128	1	Feedback M divider ratio dynamic configuration;
STATIC_RATIO0	real	1-128 or 2.000~128.000, step 0.125	1.0	Output divider0 ratio static configuration; Integer division mode: supports 1~128; Fractional division mode, supports 2.000~128.000;
STATIC_RATIO1	interger	1-128	1	Output divider1 ratio static configuration;
STATIC_RATIO2	interger	1-128	1	Output divider2 ratio static configuration;
STATIC_RATIO3	interger	1-128	1	Output divider3 ratio static configuration;
STATIC_RATIO4	interger	1-128	1	Output divider4 ratio static configuration;
STATIC_RATIO5	interger	1-128	1	Output divider5 ratio static configuration;
STATIC_RATIO6	interger	1-128	1	Output divider6 ratio static configuration;
STATIC_RATIOF	real	1-128 or	1.0	Feedback F divider ratio static configuration;

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
		2.000~128.000 step 0.125		Integer division mode: supports 1~128; Fractional division mode, supports 2.000~128.000;
STATIC_DUTY0	integer	2~255	2	Output divider0 duty static configuration;
STATIC_DUTY1	integer	2~255	2	Output divider1 duty static configuration;
STATIC_DUTY2	integer	2~255	2	Output divider2 duty static configuration;
STATIC_DUTY3	integer	2~255	2	Output divider3 duty static configuration;
STATIC_DUTY4	integer	2~255	2	Output divider4 duty static configuration;
STATIC_DUTY5	integer	2~255	2	Output divider5 duty static configuration;
STATIC_DUTY6	integer	2~255	2	Output divider6 duty static configuration;
STATIC_DUTYF	integer	2~255	2	Feedback F divider duty static configuration;
STATIC_PHASE	integer	0-63	0	Interpolation phase shift static configuration;
STATIC_PHASE0	integer	0-7	0	Output divider0 fine phase static configuration;
STATIC_PHASE1	integer	0-7	0	Output divider1 fine phase static configuration;
STATIC_PHASE2	integer	0-7	0	Output divider2 fine phase static configuration;
STATIC_PHASE3	integer	0-7	0	Output divider3 fine phase static configuration;
STATIC_PHASE4	integer	0-7	0	Output divider4 fine phase static configuration;
STATIC_PHASE5	integer	0-7	0	Output divider5 fine phase static configuration;
STATIC_PHASE6	integer	0-7	0	Output divider6 fine phase static configuration;
STATIC_PHASEF	integer	0-7	0	Feedback F divider fine phase static configuration;
STATIC_CPHASE0	integer	0-127	0	Output divider0 coarse phase static configuration;
STATIC_CPHASE1	integer	0-127	0	Output divider1 coarse phase static configuration;
STATIC_CPHASE2	integer	0-127	0	Output divider2 coarse phase static configuration;
STATIC_CPHASE3	integer	0-127	0	Output divider3 coarse phase static configuration;
STATIC_CPHASE4	integer	0-127	0	Output divider4 coarse phase static configuration;
STATIC_CPHASE5	integer	0-127	0	Output divider5 coarse phase static configuration;
STATIC_CPHASE6	integer	0-127	0	Output divider6 coarse phase static configuration;
STATIC_CPHASEF	integer	0-127	0	Feedback F divider coarse phase static configuration;
CLK_DPS0_EN	string	"FALSE","TRUE"	"FALSE"	Output divider0 interpolation phase shift enable;

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
CLK_DPS1_EN	string	"FALSE","TRUE"	"FALSE"	Output divider1 interpolation phase shift enable;
CLK_DPS2_EN	string	"FALSE","TRUE"	"FALSE"	Output divider2 interpolation phase shift enable;
CLK_DPS3_EN	string	"FALSE","TRUE"	"FALSE"	Output divider3 interpolation phase shift enable;
CLK_DPS4_EN	string	"FALSE","TRUE"	"FALSE"	Output divider4 interpolation phase shift enable;
CLK_DPS5_EN	string	"FALSE","TRUE"	"FALSE"	Output divider5 interpolation phase shift enable;
CLK_DPS6_EN	string	"FALSE","TRUE"	"FALSE"	Output divider6 interpolation phase shift enable;
CLK_DPSF_EN	string	"FALSE","TRUE"	"FALSE"	Feedback F divider interpolation phase shift enable;
CLK_CAS5_EN	string	"FALSE","TRUE"	"FALSE"	Output divider5 clock cascade enable;
CLKOUT0_SYN_EN	string	"FALSE","TRUE"	"FALSE"	Configuration for CLKOUT0_SYN signal enable;
CLKOUT1_SYN_EN	string	"FALSE","TRUE"	"FALSE"	Configuration for CLKOUT1_SYN signal enable;
CLKOUT2_SYN_EN	string	"FALSE","TRUE"	"FALSE"	Configuration for CLKOUT2_SYN signal enable;
CLKOUT3_SYN_EN	string	"FALSE","TRUE"	"FALSE"	Configuration for CLKOUT3_SYN signal enable;
CLKOUT4_SYN_EN	string	"FALSE","TRUE"	"FALSE"	Configuration for CLKOUT4_SYN signal enable;
CLKOUT5_SYN_EN	string	"FALSE","TRUE"	"FALSE"	Configuration for CLKOUT5_SYN signal enable;
CLKOUT6_SYN_EN	string	"FALSE","TRUE"	"FALSE"	Configuration for CLKOUT6_SYN signal enable;
CLKOUTF_SYN_EN	string	"FALSE","TRUE"	"FALSE"	Configuration for CLKOUTF_SYN signal enable;
SSC_MODE	string	"DOWN_LOW", "DOWN_HIGH", "CENTER_LOW", "CENTER_HIGH", "DISABLE"	"DISABLE"	SSC Mode Configuration;
SSC_FREQ	real	25~250	50.0	SSC modulation frequency configuration, KHz;
INTERNAL_FB	string	"CLKOUT0", "CLKOUT1", "CLKOUT2", "CLKOUT3", "CLKOUT4", "CLKOUT5", "CLKOUT6", "CLKOUTF",	"CLKOUTF"	Internal feedback path select;

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
		"DISABLE"		
EXTERNAL_FB	string	"CLKOUT0", "CLKOUT1" "CLKOUT2", "CLKOUT3", "CLKOUT4", "CLKOUT5", "CLKOUT6", "CLKOUTF", "DISABLE"	"DISABLE"	External feedback path select;
BANDWIDTH	string	"LOW", "HIGH" "OPTIMIZED"	"OPTIMIZED"	Bandwidth select configuration;

Note: 1. The parameters CLK_DPS5_EN and CLK_CAS5_EN cannot be configured as "TRUE" simultaneously;

2. The parameters INTERNAL_FB and EXTERNAL_FB cannot be configured as "DISABLE" simultaneously;

7.11.5 Instantiation Template

```
GTP_GPLL #(
    .CLKIN_FREQ(50),
    .LOCK_MODE(0),
    .STATIC_RATIOI(1),
    .STATIC_RATIOM(1),
    .STATIC_RATIO0(1),
    .STATIC_RATIO1(1),
    .STATIC_RATIO2(1),
    .STATIC_RATIO3(1),
    .STATIC_RATIO4(1),
    .STATIC_RATIO5(1),
    .STATIC_RATIO6(1),
    .STATIC_RATIOF(1),
    .STATIC_DUTY0(2),
    .STATIC_DUTY1(2),
    .STATIC_DUTY2(2),
    .STATIC_DUTY3(2),
    .STATIC_DUTY4(2),
    .STATIC_DUTY5(2),
    .STATIC_DUTY6(2),
    .STATIC_DUTYF(2),
    .STATIC_PHASE(0),
```

```
.STATIC_PHASE0(0),  
.STATIC_PHASE1(0),  
.STATIC_PHASE2(0),  
.STATIC_PHASE3(0),  
.STATIC_PHASE4(0),  
.STATIC_PHASE5(0),  
.STATIC_PHASE6(0),  
.STATIC_PHASEF(0),  
.STATIC_CPHASE0(0),  
.STATIC_CPHASE1(0),  
.STATIC_CPHASE2(0),  
.STATIC_CPHASE3(0),  
.STATIC_CPHASE4(0),  
.STATIC_CPHASE5(0),  
.STATIC_CPHASE6(0),  
.STATIC_CPHASEF(0),  
.CLK_DPS0_EN("FALSE"),  
.CLK_DPS1_EN("FALSE"),  
.CLK_DPS2_EN("FALSE"),  
.CLK_DPS3_EN("FALSE"),  
.CLK_DPS4_EN("FALSE"),  
.CLK_DPS5_EN("FALSE"),  
.CLK_DPS6_EN("FALSE"),  
.CLK_DPSF_EN("FALSE"),  
.CLK_CAS5_EN("FALSE"),  
.CLKOUT0_SYN_EN("FALSE"),  
.CLKOUT1_SYN_EN("FALSE"),  
.CLKOUT2_SYN_EN("FALSE"),  
.CLKOUT3_SYN_EN("FALSE"),  
.CLKOUT4_SYN_EN("FALSE"),  
.CLKOUT5_SYN_EN("FALSE"),  
.CLKOUT6_SYN_EN("FALSE"),  
.CLKOUTF_SYN_EN("FALSE"),  
.SSC_MODE("DISABLE"),
```

```

.SSC_FREQ(50),
.INTERNAL_FB("CLKOUTF"),
.EXTERNAL_FB("DISABLE"),
.BANDWIDTH("OPTIMIZED")

) GTP_GPLL_inst (
.APB_RDATA  (apb_rdata  ),
.APB_ADDR   (apb_addr   ),
.APB_WDATA  (apb_wdata  ),
.APB_READY  (apb_ready  ),
.CLKOUT0    (clkout0    ),
.CLKOUT0N   (clkout0n   ),
.CLKOUT1    (clkout1    ),
.CLKOUT1N   (clkout1n   ),
.CLKOUT2    (clkout2    ),
.CLKOUT2N   (clkout2n   ),
.CLKOUT3    (clkout3    ),
.CLKOUT3N   (clkout3n   ),
.CLKOUT4    (clkout4    ),
.CLKOUT5    (clkout5    ),
.CLKOUT6    (clkout6    ),
.CLKOUTF    (clkoutf    ),
.CLKOUTFN   (clkoutfn   ),
.DPS_DONE   (dps_done   ),
.LOCK       (lock       ),
.APB_CLK    (apb_clk    ),
.APB_EN     (apb_en     ),
.APB_RST_N  (apb_rst_n ),
.APB_SEL    (apb_sel    ),
.APB_WRITE  (apb_write  ),
.CLKFB      (clkfb      ),
.CLKIN1     (clkin1     ),
.CLKIN2     (clkin2     ),
.CLKIN_SEL  (clkin_sel  ),
.CLKOUT0_SYN(clkout0_syn),

```

```
.CLKOUT1_SYN(clkout1_syn),
.CLKOUT2_SYN(clkout2_syn),
.CLKOUT3_SYN(clkout3_syn),
.CLKOUT4_SYN(clkout4_syn),
.CLKOUT5_SYN(clkout5_syn),
.CLKOUT6_SYN(clkout6_syn),
.CLKOUTF_SYN(clkoutf_syn),
.DPS_CLK      (dps_clk      ),
.DPS_DIR      (dps_dir      ),
.DPS_EN       (dps_en       ),
.PLL_PWD      (pll_pwd      ),
.RST          (rst          )
);
```

7.11.6 Detailed Description of Functionality

For the introduction of detailed functions, please refer to the "***UG040004_Logos2 Family FPGAs Clock Resources (Clock) User Guide***".

7.12 GTP_PPLL

7.12.1 Supported Devices

Table 7-30 GTP_PPLL-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

7.12.2 Description of Functionality

The Structure Block Diagram of GTP_PPLL is shown below.

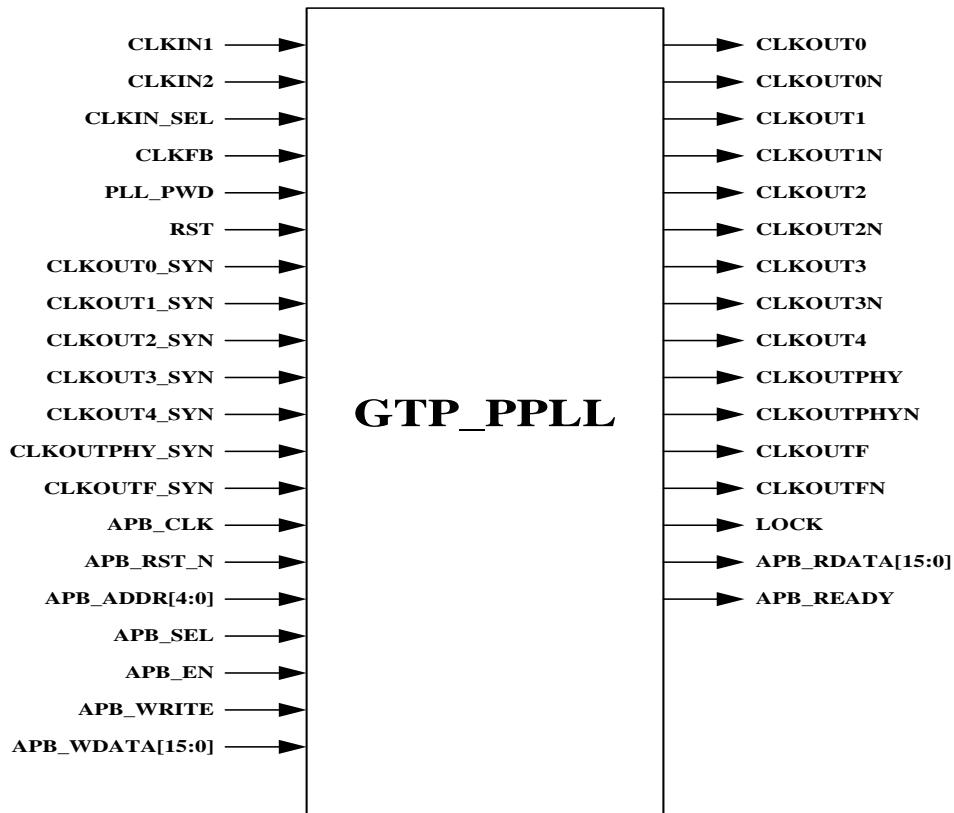


Figure 7-13 GTP_PPLL Structure Block Diagram

7.12.3 Port Description

Table 7-31 GTP_PPLL Port Description

Port Signal	Input/Output	Description
CLKOUT0	Output	PLL Channel 0 Positive Phase Output Clock;
CLKOUT0N	Output	PLL Channel 0 Inverted Phase Output Clock;
CLKOUT1	Output	PLL Channel 1 Positive Phase Output Clock;
CLKOUT1N	Output	PLL Channel 1 Inverted Phase Output Clock;
CLKOUT2	Output	PLL Channel 2 Positive Phase Output Clock;
CLKOUT2N	Output	PLL Channel 2 Inverted Phase Output Clock;
CLKOUT3	Output	PLL Channel 3 Positive Phase Output Clock;
CLKOUT3N	Output	PLL Channel 3 Inverted Phase Output Clock;
CLKOUT4	Output	PLL positive phase output clock 4;
CLKOUTPHY	Output	PLL provides a positive phase output clock for DDR PHY;
CLKOUTPHYN	Output	PLL provides an inverting phase output clock for DDR PHY;
CLKOUTF	Output	PLL Feedback Positive Phase Output Clock;
CLKOUTFN	Output	PLL Feedback Inverted Phase Output Clock;
LOCK	Output	PLL frequency lock indicator signal, asynchronous; When the signal is pulled high, it indicates that the PLL feedback clock signal is locked to the input clock signal;
APB_RDATA[15:0]	Output	PLL APB interface data bus data output

Port Signal	Input/Output	Description
APB_READY	Output	PLL APB interface data bus handshake signal; indicates the end of a normal bus cycle;
CLKIN1	Input	PLL reference input clock 1;
CLKIN2	Input	PLL reference input clock 2;
CLKFB	Input	PLL feedback clock;
CLKIN_SEL	Input	Input clock selection signal;
PLL_PWD	Input	PLL Power Down, active high;
RST	Input	PLL reset signal, active high;
CLKOUT0_SYN	Input	CLKOUT0/N output clock enable control; active high; high level disables, low level enables;
CLKOUT1_SYN	Input	CLKOUT1/N output clock enable control; active high; high level disables, low level enables;
CLKOUT2_SYN	Input	CLKOUT2/N output clock enable control; active high; high level disables, low level enables;
CLKOUT3_SYN	Input	CLKOUT3/N output clock enable control; active high; high level disables, low level enables;
CLKOUT4_SYN	Input	CLKOUT4 output clock enable control; active high; high level disables, low level enables;
CLKOUTPHY_SYN	Input	CLKOUTPHY output clock enable control; active high; high level turns off; low level enable;
CLKOUTF_SYN	Input	CLKOUTF/N output clock enable control; active high; high level disables, low level enables;
APB_CLK	Input	PLL APB interface data bus clock;
APB_RST_N	Input	PLL APB interface data bus asynchronous reset signal, active low;
APB_ADDR	Input	PLL APB interface data bus address;
APB_SEL	Input	PLL APB interface data bus selection signal to select the slave device;
APB_EN	Input	The PLL APB port data bus enable signal, indicating the second and subsequent cycles of transmission;
APB_WRITE	Input	PLL APB interface data bus write enable signal; 1'b0: read operation, 1'b0: write operation;
APB_WDATA[15:0]	Input	PLL APB interface data bus data input;

7.12.4 Paramater Description

Table 7-32 GTP_PPLL Parameter List Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
CLKIN_FREQ	real	19~800	50.0	Input clock frequency configuration, MHz;
LOCK_MODE	binary	1'b0, 1'b1	1'b0	PLL frequency detection mode configuration; 1'b0: Real-time monitoring of PLL working state; 1'b1: The PLL lock remains after locking, unless reset or power-down;
STATIC_RATIOI	interger	1-42	1	Enter divider ratio static configuration;
STATIC_RATIOM	interger	1-128	1	Feedback M divider ratio

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
				dynamic configuration;
STATIC_RATIO0	integer	1-128	1	Output divider0 ratio static configuration;
STATIC_RATIO1	integer	1-128	1	Output divider1 ratio static configuration;
STATIC_RATIO2	integer	1-128	1	Output divider2 ratio static configuration;
STATIC_RATIO3	integer	1-128	1	Output divider3 ratio static configuration;
STATIC_RATIO4	integer	1-128	1	Output divider4 ratio static configuration;
STATIC_RATIOPHY	integer	1-128	1	Output divider PHY ratio static configuration;
STATIC_RATIOF	integer	1-128	1	Feedback F divider ratio static configuration;
STATIC_DUTY0	integer	2~255	2	Output divider0 duty static configuration;
STATIC_DUTY1	integer	2~255	2	Output divider1 duty static configuration;
STATIC_DUTY2	integer	2~255	2	Output divider2 duty static configuration;
STATIC_DUTY3	integer	2~255	2	Output divider3 duty static configuration;
STATIC_DUTY4	integer	2~255	2	Output divider4 duty static configuration;
STATIC_DUTYPHY	integer	2~255	2	Output divider PHY duty static configuration;
STATIC_DUTYF	integer	2~255	2	Feedback F divider duty static configuration;
STATIC_PHASE0	integer	0-7	0	Output divider0 fine phase static configuration;
STATIC_PHASE1	integer	0-7	0	Output divider1 fine phase static configuration;
STATIC_PHASE2	integer	0-7	0	Output divider2 fine phase static configuration;
STATIC_PHASE3	integer	0-7	0	Output divider3 fine phase static configuration;
STATIC_PHASE4	integer	0-7	0	Output divider4 fine phase static configuration;
STATIC_PHASEPHY	integer	0-7	0	Output divider PHY fine phase static configuration;
STATIC_PHASEF	integer	0-7	0	Feedback F divider fine phase static configuration;
STATIC_CPHASE0	integer	0-127	0	Output divider0 coarse phase static configuration;
STATIC_CPHASE1	integer	0-127	0	Output divider1 coarse phase static configuration;
STATIC_CPHASE2	integer	0-127	0	Output divider2 coarse phase static configuration;
STATIC_CPHASE3	integer	0-127	0	Output divider3 coarse phase static configuration;
STATIC_CPHASE4	integer	0-127	0	Output divider4 coarse phase static configuration;
STATIC_CPHASEPHY	integer	0-127	0	Output divider PHY coarse phase static configuration;

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
STATIC_CPHASEF	integer	0-127	0	Feedback F divider coarse phase static configuration;
CLKOUT0_SYN_EN	string	"FALSE","TRUE"	"FALSE"	Configuration for CLKOUT0_SYN signal enable;
CLKOUT1_SYN_EN	string	"FALSE","TRUE"	"FALSE"	Configuration for CLKOUT1_SYN signal enable;
CLKOUT2_SYN_EN	string	"FALSE","TRUE"	"FALSE"	Configuration for CLKOUT2_SYN signal enable;
CLKOUT3_SYN_EN	string	"FALSE","TRUE"	"FALSE"	Configuration for CLKOUT3_SYN signal enable;
CLKOUT4_SYN_EN	string	"FALSE","TRUE"	"FALSE"	Configuration for CLKOUT4_SYN signal enable;
CLKOUTPHY_SYN_EN	string	"FALSE","TRUE"	"FALSE"	CLKOUTPHY_SYN signal enable configuration;
CLKOUTF_SYN_EN	string	"FALSE","TRUE"	"FALSE"	Configuration for CLKOUTF_SYN signal enable;
INTERNAL_FB	string	"CLKOUT0", "CLKOUT1", "CLKOUT2", "CLKOUT3", "CLKOUT4", "CLKOUTF", "DISABLE"	"CLKOUTF"	Internal feedback path select;
EXTERNAL_FB	string	"CLKOUT0", "CLKOUT1", "CLKOUT2", "CLKOUT3", "CLKOUT4", "CLKOUTF", "DISABLE"	"DISABLE"	External feedback path select;
BANDWIDTH	string	"LOW","HIGH" "OPTIMIZED"	"OPTIMIZED"	Bandwidth select configuration;

Note: The parameters INTERNAL_FB and EXTERNAL_FB cannot be configured as "DISABLE" simultaneously;

7.12.5 Instantiation Template

```
GTP_PPLL #(
    .CLKIN_FREQ(50),
    .LOCK_MODE(0),
    .STATIC_RATIOI(1),
    .STATIC_RATIOM(1),
    .STATIC_RATIO0(1),
    .STATIC_RATIO1(1),
```

```
.STATIC_RATIO2(1),  
.STATIC_RATIO3(1),  
.STATIC_RATIO4(1),  
.STATIC_RATIOPHY(1),  
.STATIC_RATIOF(1),  
.STATIC_DUTY0(2),  
.STATIC_DUTY1(2),  
.STATIC_DUTY2(2),  
.STATIC_DUTY3(2),  
.STATIC_DUTY4(2),  
.STATIC_DUTYPHY(2),  
.STATIC_DUTYF(2),  
.STATIC_PHASE0(0),  
.STATIC_PHASE1(0),  
.STATIC_PHASE2(0),  
.STATIC_PHASE3(0),  
.STATIC_PHASE4(0),  
.STATIC_PHASEPHY(0),  
.STATIC_PHASEF(0),  
.STATIC_CPHASE0(0),  
.STATIC_CPHASE1(0),  
.STATIC_CPHASE2(0),  
.STATIC_CPHASE3(0),  
.STATIC_CPHASE4(0),  
.STATIC_CPHASEPHY(0),  
.STATIC_CPHASEF(0),  
.CLKOUT0_SYN_EN("FALSE"),  
.CLKOUT1_SYN_EN("FALSE"),  
.CLKOUT2_SYN_EN("FALSE"),  
.CLKOUT3_SYN_EN("FALSE"),  
.CLKOUT4_SYN_EN("FALSE"),  
.CLKOUTPHY_SYN_EN("FALSE"),  
.CLKOUTF_SYN_EN("FALSE"),  
.INTERNAL_FB("CLKOUTF"),
```

```

.EXTERNAL_FB("DISABLE"),
.BANDWIDTH("OPTIMIZED")

) GTP_PPPLL_inst (
    .APB_RDATA      (apb_rdata      ),
    .APB_ADDR       (apb_addr       ),
    .APB_WDATA       (apb_wdata       ),
    .APB_READY       (apb_ready       ),
    .CLKOUT0        (clkout0        ),
    .CLKOUT0N       (clkout0n       ),
    .CLKOUT1        (clkout1        ),
    .CLKOUT1N       (clkout1n       ),
    .CLKOUT2        (clkout2        ),
    .CLKOUT2N       (clkout2n       ),
    .CLKOUT3        (clkout3        ),
    .CLKOUT3N       (clkout3n       ),
    .CLKOUT4        (clkout4        ),
    .CLKOUT4N       (clkout4n       ),
    .CLKOUTF        (clkoutf        ),
    .CLKOUTFN       (clkoutfn       ),
    .CLKOUTPHY      (clkoutphy      ),
    .CLKOUTPHYN     (clkoutphyn     ),
    .LOCK           (lock           ),
    .APB_CLK         (apb_clk         ),
    .APB_EN          (apb_en          ),
    .APB_RST_N       (apb_RST_n       ),
    .APB_SEL          (apb_sel          ),
    .APB_WRITE        (apb_write        ),
    .CLKFB           (clkfb           ),
    .CLKIN1          (clkin1          ),
    .CLKIN2          (clkin2          ),
    .CLKIN_SEL        (clkin_sel        ),
    .CLKOUT0_SYN     (clkout0_syn     ),
    .CLKOUT1_SYN     (clkout1_syn     ),
    .CLKOUT2_SYN     (clkout2_syn     ),

```

```
.CLKOUT3_SYN    (clkout3_syn  ),
.CLKOUT4_SYN    (clkout4_syn  ),
.CLKOUTF_SYN    (clkoutf_syn  ),
.CLKOUTPHY_SYN  (clkoutphy_syn),
.PLL_PWD        (pll_pwd      ),
.RST             (rst          )
);
```

7.12.6 Detailed Description of Functionality

For the introduction of detailed functions, please refer to the "***UG040004_Logos2 Family FPGAs Clock Resources (Clock) User Guide***".

7.13 GTP_DLL_E2

7.13.1 Supported Devices

Table 7-33 GTP_DLL_E2-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

7.13.2 Description of Functionality

The Structure Block Diagram of GTP_DLL_E2 is shown below.

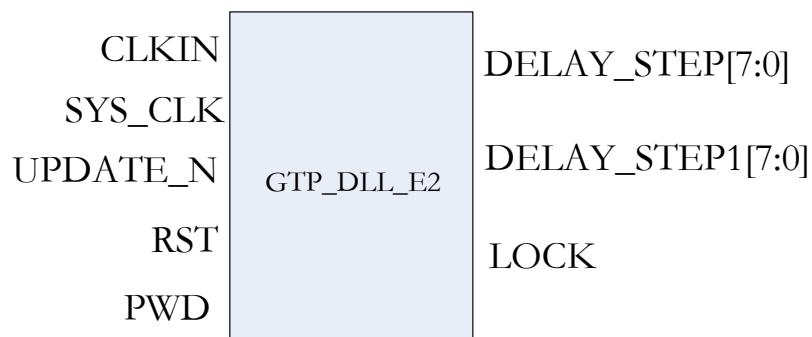


Figure 7-14 GTP_DLL_E2 Structure Block Diagram

7.13.3 Port Description

Table 7-34 GTP_DLL_E2 Port Description

Port Signal	Input/Output	Description
CLKIN	Input	From IOCLK tree, fast clock
SYS_CLK	Input	From PPLL/SRB, DLL FSM clock
UPDATE_N	Input	Request to update DLL's delay step (active-low)
RST	Input	Active-low reset signal
PWD	Input	Active-high power down signal
DELAY_STEP	Output	DLL output 90-degree delay control code
DELAY_STEP1	Output	DLL output 45-degree delay control code
LOCK	Output	LOCK flag signal, with active-high indicating locked

7.13.4 Paramater Description

Table 7-35 GTP_DLL_E2 Parameter List Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	<"TRUE", "FALSE">	<"TRUE">	Global reset enable signal
CAL_INIT	<interger>	<8'b00000000 ~ 8'b11111111>	<8'b00011111>	Calibration code
FAST_LOCK	<string>	<"TRUE", "FALSE">	<"FALSE">	DLL LOCK mode select
DELAY_STEP_OFFSET	<interger>	<-4, -3, -2, -1, 0, 1, 2, 3, 4>	<0>	DLL output code phase shift control
DELAY_SEL	<interger>	<0, 1>	<0>	DLL delay chain
FDIV	<interger>	<2'b00> <2'b01> <2'b10> <2'b11>	<2'b10>	Division configuration. CP_FDIV can only be set to 2'b10 in DDR2/3 and QDR applications.
INT_CLK	<interger>	<0, 1>	<0>	DLL FSM SYSCLK source
UPD_DLY	<interger>	2'b00: 2 ioclk_2x cycles 2'b01: 4 ioclk_2x cycles 2'b10: 8 ioclk_2x cycles 2'b11: 16 ioclk_2x cycles	<2'b01>	DLL FSM calibration code dly_cal_therm_dly<63:0> update delay
HPIO	<string>	<"TRUE", "FALSE">	<"FALSE">	"FALSE" HRIO,"TRUE" HPIO

7.13.5 Instantiation Template

```

GTP_DLL_E2 #(
    .GRS_EN("TRUE"),
    .CAL_INIT('b00011111),
    .DELAY_STEP_OFFSET(0),
    .DELAY_SEL(1'b0),
    .FAST_LOCK("FALSE"),
    .FDIV('b10),
    .INT_CLK(1'b0),
    .UPD_DLY('b01),
    .HPIO("FALSE")
) GTP_DLL_E2_inst (
    .DELAY_STEP(), // OUTPUT[7:0]
    .DELAY_STEP1(),// OUTPUT[7:0]
    .LOCK(),      // OUTPUT
    .CLKIN(),     // INPUT
    .PWD(),       // INPUT
    .RST(),       // INPUT
    .SYS_CLK(),   // INPUT
    .UPDATE_N()   // INPUT
);
    
```

7.14 GTP_OSC_E4

7.14.1 Supported Devices

Table 7-36 GTP_OSC_E4-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

7.14.2 Description of Functionality

When EN_N = 1, CLKOUT outputs a low level signal. When EN_N = 0, CLKOUT outputs a fixed 50MHz clock to CCS as the system clock. The Structure Block Diagram is shown below.

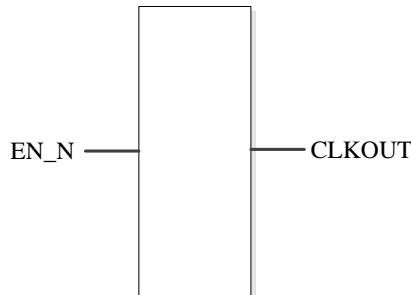


Figure 7-15 GTP_OSC_E4 Structure Diagram

7.14.3 Port Description

Table 7-37 GTP_OSC_E4 Port List

Port	Direction	Function Description
EN_N	Input	Output clock enable, active low
CLKOUT	Output	Output 50MHz clock

7.14.4 Instantiation Template

```
GTP_OSC_E4 GTP_OSC_E4_inst (
    .CLKOUT(clkout),
    .EN_N(en_n)
);
```

7.15 GTP_CLKBUFGMUX_E1

7.15.1 Supported Devices

Table 7-38 GTP_CLKBUFGMUX_E1-Supported Devices

Device Family	Titan2
Whether supports the GTP	Supported

7.15.2 Description of Functionality

GTP_CLKBUFGMUX_E1 has partial functions of GTP_CLKBUFGCE and GTP_CLKBUFGMUX. The EN signal controls the clock signal output behaviour of CLKOUT, while the SEL signal allows for dynamic switching between input clocks. Differing from GTP_CLKBUFGMUX parameter setting, it only accommodates two switching modes, namely "NEGEDGE" mode and "POSEDGE" mode. The "INIT_SEL" parameter can be used to set the

initial output clock.

7.15.3 Port Description

Table 7-39 GTP_CLKBUFGMUX_E1 Port Description

Port Signal	Input/Output	Description
CLKIN0	Input	Input clock CLKIN0
CLKIN1	Input	Input clock CLKIN1
SEL	Input	Clock selection signal: 0 for CLKIN0; 1 for CLKIN1;
CLKOUT	Output	Output clock
EN	Input	Clock enable control signal: EN = 1: CLKOUT outputs a clock signal. EN = 0: CLKOUT does not output a clock signal.

7.15.4 Parameter Description

Table 7-40 GTP_CLKBUFGMUX_E1 Parameter Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
TRIGGER_MODE	<string>	"NEGEDGE" "POSEDGE"	"NEGEDGE"	"NEGEDGE": In this mode, input clocks (CLKIN0 and CLKIN1) can be freely switched and the GLITCHLESS feature triggered on the falling edge of the clock is available. "POSEDGE": In this mode, input clocks (CLKIN0 and CLKIN1) can be freely switched and the GLITCHLESS feature triggered on the rising edge of the clock is available.
INIT_SEL	<string>	"CLK0" "CLK1"	"CLK0"	Select the initial output clock: When set to "CLK0", CLKOUT equals to CLKIN0. When set to "CLK1", CLKOUT = CLKIN1.

7.15.5 Instantiation Template

```

GTP_CLKBUFGMUX_E1 #(
    .TRIGGER_MODE("NEGEDGE"),
    .INIT_SEL("CLK0")
) GTP_CLKBUFGMUX_E1_inst (
    .CLKOUT(),// OUTPUT
    .CLKIN0(),// INPUT
    .CLKIN1(),// INPUT
    .EN(),    // INPUT
    .SEL()     // INPUT
);

```

7.15.6 Detailed Description of Functionality

When the parameter TRIGGER_MODE is set to "NEGEDGE" and INIT_SEL is set to "CLK0", it triggers on the falling edge, and CLKIN0 is selected for the initial clock.

When EN equals to 1 and SEL switches from 0 to 1, detect the falling edge of the current clock CLKIN0 twice (maintaining the CLKOUT output as the current clock during the detection of the rising edge of the current clock) and then the falling edge of the switch-to clock CLKIN1 twice (with the CLKOUT output low during the detection of the falling edge of the switch-to clock). After the detection is completed, CLKOUT switches from CLKIN0 to CLKIN1.

When EN equals to 1 and SEL switches from 1 to 0, detect the falling edge of CLKIN1 twice (maintaining the CLKOUT output as the current clock during the detection of the rising edge of the current clock) and then the falling edge of CLKIN0 twice (with the CLKOUT output low during the detection of the falling edge of the switch-to clock CLKIN0). After the detection is completed, CLKOUT switches from CLKIN1 to CLKIN0.

When EN equals to 0, no SEL signal transitions are allowed, and the output goes to a low level after detecting the falling edge of CLKOUT twice.

The corresponding timing diagram is as follows:

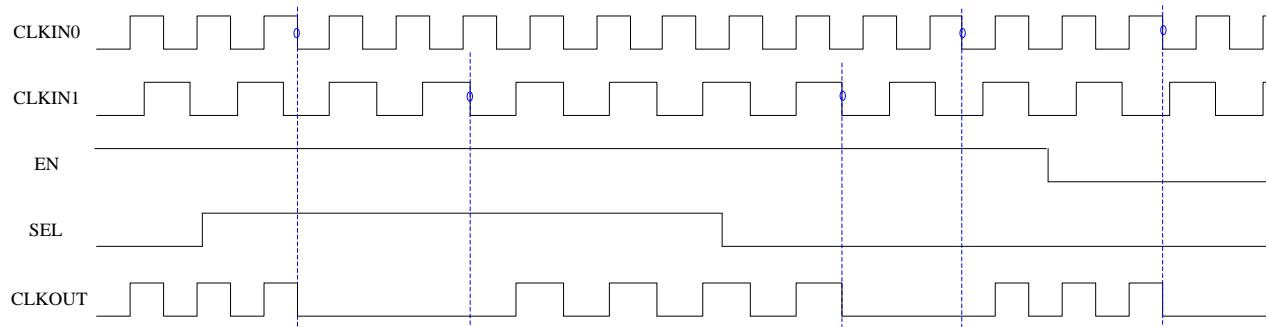


Figure 7-16 Timing Diagram for GTP_CLKBUFGMUX_E1 with Parameter TRIGGER_MODE = "NEGEDGE"

When the parameter TRIGGER_MODE is set to "POSEDGE" and INIT_SEL is set to "CLK0", it triggers on the falling edge, and CLKIN0 is selected for the initial clock.

When EN equals to 1 and SEL switches from 0 to 1, detect the rising edge of the current clock CLKIN0 twice (maintaining the CLKOUT output as the current clock during the detection of the rising edge of the current clock) and then the rising edge of the switch-to clock CLKIN1 twice (with the CLKOUT output high during the detection of the rising edge of the switch-to clock). After the detection is completed, CLKOUT switches from CLKIN0 to CLKIN1.

When EN is equal to 1 and SEL changes from 1 to 0, two rising edges of CLKIN1 are detected first (during the detection process of the current clock's rising edges, CLKOUT maintains the current clock). Two rising edges of CLKIN0 are then detected (during the detection process of the rising

edges of the switched clock CLKIN0, CLKOUT outputs a high level). After detection, CLKOUT switches from CLKIN1 to CLKIN0.

When EN is equal to 0, transitions in the SEL signal are not allowed. After detecting the rising edge of CLKOUT twice, it outputs high level.

The corresponding timing diagram is as follows:

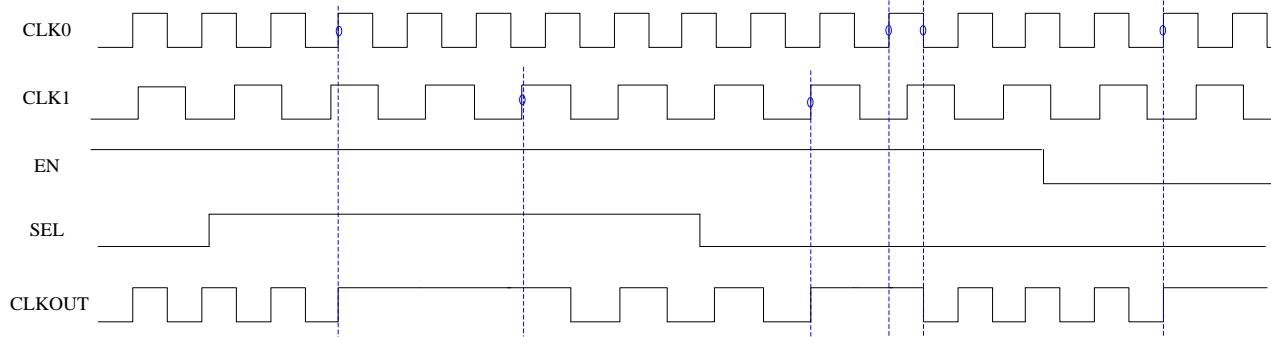


Figure 7-17 Timing Diagram for GTP_CLKBUFGMUX_E1 with Parameter TRIGGER_MODE = "POSEDGE"

7.16 GTP_CLKBUFGMUX_E2

7.16.1 Supported Devices

Table 7-41 GTP_CLKBUFGMUX_E2-Supported Devices

Device Family	Titan2
Whether supports the GTP	Supported

7.16.2 Description of Functionality

GTP_CLKBUFGMUX_E2 also allows for dynamic switching between different input clocks, inheriting some features of GTP_CLKBUFGMUX and GTP_CLKBUFGMUX_E1. The most significant divergence from the two precedents is that this GTP provides users with the option to decide which edge of the input clock to be switched for detection. (Detecting the edge of the two input clocks or one of it , or not detecting either one). When only one input clock edge is detected, the SEL signal can be considered an enable signal. For example, when DETECT_CLK0=1 and DETECT_CLK1=0, the output clock follows CLKIN0 with the SEL set to 0, while remaining at 1 or 0 with the SEL set to 1. When DETECT_CLK0=0 and DETECT_CLK1=1, the output clock remains at 1 or 0 with the SEL set to 0, while following CLKIN1 with the SEL set to 1. It also has parameters for the initial output clock (CLKIN0 or CLKIN1) and the clock source trigger method (rising edge or falling edge).

The following points need to be noted:

1. If neither of the input clock edges is detected, there will be glitches when switching the input clock.
2. If both input clock edges are initially set to be detected and then switched to detect only one, there may be glitches when DETECT_CLK0 and DETECT_CLK1 = 1 change from 1 to 0.
3. Switching with two input clock edge detection requires waiting for 4 cycles, switching with single input clock edge detection requires waiting for 2 cycles, and switching without detection occurs immediately. For details, refer to the interface timing description.

7.16.3 Port Description

Table 7-42 Port Description of GTP_CLKBUFGMUX_E2

Port Signal	Input/Output	Description
CLKIN0	Input	Input clock CLKIN0
CLKIN1	Input	Input clock CLKIN1
SEL	Input	Clock selection signal: 0 for CLKIN0; 1 for CLKIN1;
CLKOUT	Output	Output clock
DETECT_CLK0	Input	When set to 1: During the clock switching process, the clock edge of CLKIN0 is detected. When set to 0: During the clock switching process, the clock edge of CLKIN0 is not detected.
DETECT_CLK1	Input	When set to 1: During the clock switching process, the clock edge of CLKIN1 is detected. When set to 0: During the clock switching process, the clock edge of CLKIN1 is not detected.

7.16.4 Parameter Description

Table 7-43 Parameter Description of GTP_CLKBUFGMUX_E2

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
TRIGGER_MODE	<string>	"NEGEDGE" "POSEDGE"	"NEGEDGE"	"NEGEDGE": In this mode, input clocks (CLKIN0 and CLKIN1) can be freely switched and the GLITCHLESS feature triggered on the falling edge of the clock is available. "POSEDGE": In this mode, input clocks (CLKIN0 and CLKIN1) can be freely switched and the GLITCHLESS feature triggered on the rising edge of the clock is available.
INIT_SEL	<string>	"CLK0" "CLK1"	"CLK0"	Select the initial output clock: When set to "CLK0", CLKOUT equals to CLKIN0. When set to "CLK1", CLKOUT = CLKIN1.

7.16.5 Instantiation Template

```
GTP_CLKBUFGMUX_E2 #(  
    .TRIGGER_MODE("NEGEDGE"),  
    .INIT_SEL("CLK0")  
) GTP_CLKBUFGMUX_E2_inst (  
    .CLKOUT(),// OUTPUT  
    .CLKIN0(),// INPUT  
    .CLKIN1(),// INPUT  
    .DETECT_CLK0(),// INPUT  
    .DETECT_CLK1(),// INPUT  
    .SEL()      // INPUT  
);
```

7.16.6 Detailed Description of Functionality

For detailed description of the functions of GTP_CLKBUFGMUX_E2, please refer to "*UG020004_Logos Family FPGAs Clock Resources (Clock) User Guide*".

Chapter 8 Usage Instructions for Configuration-related GTPs

8.1 GTP_EFUSECODE

8.1.1 Supported Devices

Table 8-1 GTP_EFUSECODE -Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

8.1.2 Description of Functionality

This GTP is used to read EFUSECODE.

8.1.3 Port Description

Table 8-2 GTP_EFUSECODE Port List

Port	Direction	Function Description
EFUSE_CODE[31:0]	Output	Efusecode output data bus

8.1.4 Parameter Description

Table 8-3 GTP_EFUSECODE Parameter List

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
SIM_EFUSE_VALUE	Binary	0~32'hffffffff ;	32'h12345678	Efusecode Value

8.1.5 Instantiation Template

```
GTP_EFUSECODE#(
    .SIM_EFUSE_VALUE      (32'h12345678),
    ) GTP_EFUSECODE_inst(
        .EFUSE_CODE      (efuse  )
    );
```

8.2 GTP_IPAL_E2

8.2.1 Supported Devices

Table 8-4 GTP_IPAL_E2-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

8.2.2 Description of Functionality

GTP_IPAL_E2 is an internal slave parallel interface module designed to perform CRC (Cyclic Redundancy Check) or SEU (Single Event Upset) detection on the readback data. When writing a frame of data to the configuration memory, the higher bits must be written first, followed by the lower bits. Therefore, when read back, the higher bits are read first, followed by the lower bits. In X16 mode, higher 16bits of a 32-bit word are read firstly, then the lower 16 bits. Similarly, the X8 mode reads data in the same manner.

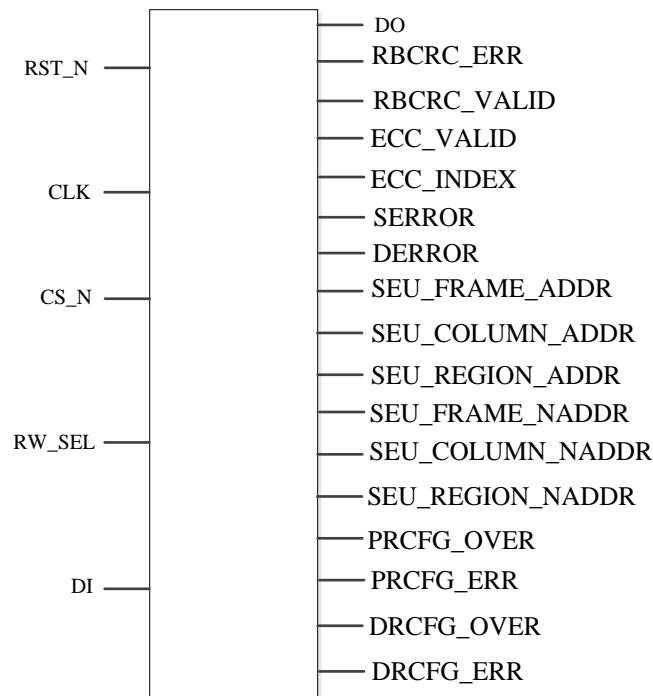


Figure 8-1 GTP_IPAL_E2 Structure Diagram

Table 8-5 Configuration Registers Supported by GTP_IPAL_E2 Simulation

Item	Direction	Address	Function Description
IDR	R/W	00001	IDCODE Register
CMDR	R/W	00010	Command register
CMEMIR	W	00101	Frame data input register
CMEMOR	R	00111	Frame data output register

ADRR	R/W	01011	Frame address register
SEUR	R/W	01101	SEU control register
SEUSTATUSR	R	01110	SEU status register
SEUADDR	R	11101	SEU frame address register
SEUNADDR	R	11111	SEU next frame address register

8.2.3 Port Description

Table 8-6 GTP_IPAL_E2 Port List

Port	Direction	Function Description
RST_N	Input	Reset, active low
CLK	Input	Internal parallel interface clock
CS_N	Input	Chip select signal, active-low
RW_SEL	Input	Read/write selection: 0 for write, 1 for read
DI[31:0]	Input	Data Input
DO[31:0]	Output	Data output
RBCRC_ERR	Output	Readback CRC Error Flag
RBCRC_VALID	Output	Readback CRC valid flag
ECC_VALID	Output	ECC valid flag
ECC_INDEX[11:0]	Output	Single-bit error address index
SERROR	Output	SEU detection single-bit error flag
DERROR	Output	SEU detection double-bit error flag
SEU_FRAME_ADDR[7:0]	Output	Current frame address of SEU detection
SEU_COLUMN_ADDR[7:0]	Output	Current column address of SEU detection
SEU_REGION_ADDR[4:0]	Output	Current region address of SEU detection
SEU_FRAME_NADDR[7:0]	Output	Next frame address of SEU detection
SEU_COLUMN_NADDR[7:0]	Output	Next column address of SEU detection
SEU_REGION_NADDR[4:0]	Output	Next region address of SEU detection
PRCFG_OVER	Output	Local reconfiguration end flag
PRCFG_ERR	Output	Partial reconfiguration error flag
DRCFG_OVER	Output	End flag of dynamic reconfiguration
DRCFG_ERR	Output	Dynamic reconfiguration error flag

8.2.4 Parameter Description

Table 8-7 GTP_IPAL_E2 Parameter List

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
IDCODE	<binary>	32'h0~32'hFFFF_FFFF	32'haaaa5555	Device IDCODE
DATA_WIDTH	<string>	"X8" "X16" "X32"	"X8"	Selection of input data bit width
SIM_DEVICE	<string>	"PG2L100H" "PG2T390H"	"PG2L100H"	Device type selection

8.2.5 Instantiation Template

```

GTP_IPAL_E2 #(
    .SIM_DEVICE("PG2L100H"),
    .DATA_WIDTH("X8"),
    .IDCODE('b10101010101010101001010101010101),
    ) GTP_IPAL_E2_inst (
        .DO(do),
        .ECC_INDEX(ecc_index),
        .SEU_COLUMN_ADDR(seu_column_addr),
        .SEU_COLUMN_NADDR(seu_column_naddr),
        .SEU_FRAME_ADDR(seu_frame_addr),
        .SEU_FRAME_NADDR(seu_frame_naddr),
        .SEU_REGION_ADDR(seu_region_addr),
        .SEU_REGION_NADDR(seu_region_naddr),
        .DI(di),
        .DERROR(derror),
        .ECC_VALID(ecc_valid),
        .PRCFG_ERR(prcfg_err),
        .PRCFG_OVER(prcfg_over),
        .RBCRC_ERR(rbcrc_err),
        .RBCRC_VALID(rbcrc_valid),
        .SERROR(serror),
        .CLK(clk),
        .CS_N(cs_n),
        .RST_N(rst_n),
        .RW_SEL(rw_sel)
);

```

);

8.3 GTP_SCANCHAIN_E1

8.3.1 Supported Devices

Table 8-8 GTP_SCANCHAIN_E1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

8.3.2 Description of Functionality

Read the value of the user data register through the JTAG interface.

8.3.3 Port Description

Table 8-9 GTP_SCANCHAIN_E1 Port List

Port	Direction	Function Description
TDI	Input	JTAG Interface
TDO	Output	JTAG Interface
TMS	Input	JTAG Interface
TCK	Input	JTAG Interface
RST	Output	Jtag soft reset output
CAPDR	Output	Jtag captureddr status indicator
SHFTDR	Output	Shiftdr status indicator
UPDR	Output	Updatedr status indicator
JCLK	Output	Shiftdr as the clock
FLG_USER	Output	User instruction indicator
TDI_USER	Output	Input data of user registers
TDO_USER	Input	Output data of user registers
JRTI	Output	Run/test idle status indicator
TCK_USER	Output	Tck to user
TMS_USER	Output	Tms to user

8.3.4 Parameter Description

Table 8-10 GTP_SCANCHAIN_E1 Parameter List

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
IDCODE	Binary	0~32'hfffffff ;	32'haaaa5555	IDCODE

CHAIN_NUM	Integer	1、2、3、4	1	User DR number
-----------	---------	---------	---	----------------

8.3.5 Instantiation Template

GTP_SCANCHAIN

```
#(
    .IDCODE      (32'haaaa5555),
    .CHAIN_NUM   (1)
)

GTP_SCANCHAIN_inst(
    .TCK         (tck        ),
    .TDI         (tdi        ),
    .TMS         (tms        ),
    .TDO         (tdo        ),
    .CAPDR       (capture    ),
    .JCLK        (jclk       ),
    .RST         (rst        ),
    .FLG_USER    (flg_user   ),
    .SHFTDR     (shift       ),
    .TDI_USER    (tdi_user   ),
    .TMS_USER    (tms_user   ),
    .JRTI        (jrti       ),
    .UPDR        (update     ),
    .TDO_USER    (tdo_user   )
);
```

8.3.6 Detailed Functional Description

Users can use it to read the chip IDCODE, or read/write multiple user logic data register values separately through the JTAG interface.

8.4 GTP_UDID

8.4.1 Supported Devices

Table 8-11 GTP_UDID-Supported Devices

Device Family	LOGOS2
---------------	--------

Whether supports the GTP	Supported
--------------------------	-----------

8.4.2 Description of Functionality

This GTP is used to read the UDID CODE value.

8.4.3 Port Description

Table 8-12 GTP_UDID Port List

Port	Direction	Function Description
DI	Input	Serial data input
DO	Output	Serial data output
SE	Input	Enables data shift
LOAD	Input	Data registers parallel load UID CODE
CLK	Input	Clock

8.4.4 Parameter Description

Table 8-13 GTP_UDID Parameter List

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
UDID_CODE	Binary	0~96'hffffffffffff...ffff	0	Chip identifier
UDID_WIDTH	integer	0~32'hffff_ffff	64	Set the bit width of UDID_CODE

Note: The above parameters are only used in simulation test. This interface model applies to Compact, Logos, Logos2 and Titan2 family devices. The UID length varies between families, with a default value of 64. Therefore, to maintain consistency between simulation and board operation, the default value should be changed to 96 for Logos2 devices.

8.4.5 Instantiation Template

```
GTP_UDID#(
    .UDID_WIDTH(64),
    .UDID_CODE (0)
)
GTP_UDID_inst(
    .DI      (di),
    .DO      (do),
    .LOAD   (load),
    .SE      (se),
)
```

```
.CLK (clk)
);
```

8.4.6 Detailed Functional Description

Serially output chip identifier data to the user.

8.5 GTP_JTAGIF

8.5.1 Supported Devices

Table 8-14 GTP_JTAGIF-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

8.5.2 Description of Functionality

GTP_JTAGIF has three input ports: TCK, TMS, and TDI; one output port TDO; and one parameter USERCODE to implement the user JTAG interface function. Simulation only supports JTAG instruction operations, read and write configuration registers, configuration memories.

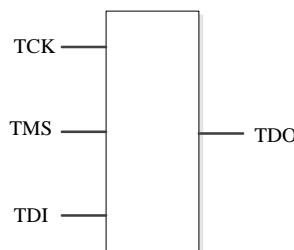


Figure 8-2 GTP_JTAGIF Structure Diagram

Table 8-15 Configuration Registers Supported by GTP_JTAGIF Simulation

Item	Direction	Address	Function Description
IDR	R/W	00001	IDCODE Register
CMDR	R/W	00010	Command register
CMEMIR	W	00101	Frame data input register
CMEMOR	R	00111	Frame data output register
ADRR	R/W	01011	Frame address register

8.5.3 Port Description

Table 8-16 GTP_JTAGIF Port List

Port	Direction	Function Description
TCK	Input	User JTAG clock
TMS	Input	User JTAG test mode selection
TDI	Input	User JTAG Test Data Input
TDO	Output	User JTAG test data output

8.5.4 Parameter Description

Table 8-17 GTP_JTAGIF Parameter List

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
USERCODE	binary	32'h0~32'hFFFF_FFFF	32'hFFFF_FFFF	USERCODE
IDCODE	binary	32'h0~32'hFFFF_FFFF	32'h5555_AAAA	IDCODE (provided in simulation but not mapped)

8.5.5 Instantiation Template

```
GTP_JTAGIF #(
    .USERCODE(32'hFFFF_FFFF),
    .IDCODE(32'h5555_AAAA),
    ) GTP_JTAGIF_inst (
        .TDO(tdo),
        .TCK(tck),
        .TDI(tdi),
        .TMS(tms)
    );
```

8.6 GTP_KEYRAM

8.6.1 Supported Devices

Table 8-18 GTP_KEYRAM-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

8.6.2 Description of Functionality

The function of GTP_KEYRAM is to clear the internal memory. The structure block diagram is shown below.

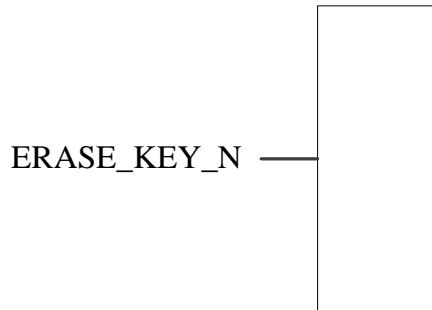


Figure 8-3 GTP_KEYRAM Structure Block Diagram

8.6.3 Port Description

Table 8-19 GTP_KEYRAM Port List

Port	Direction	Function Description
ERASE_KEY_N	Input	Cleared, Low-Active.

8.6.4 Instantiation Template

```

GTP_KEYRAM
GTP_KEYRAM_inst (
    .ERASE_KEY_N (key_n)
);
    
```

8.7 GTP_CFGCLK

8.7.1 Supported Devices

Table 8-20 GTP_CFGCLK-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

8.7.2 Description of Functionality

GTP_CFGCLK has only two inputs: a clock input signal and a clock enable signal. This GTP consists of the FLASH clock and clock enable sent from SRB to CCS.

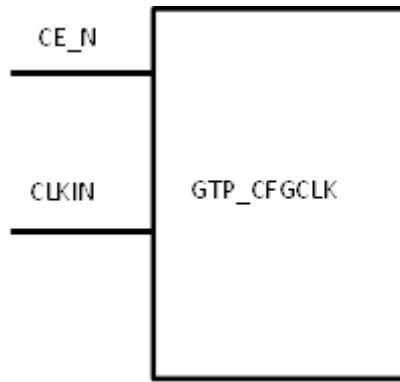


Figure 8-4 GTP_CFGCLK Structure Block Diagram

8.7.3 Port Description

Table 8-21 GTP_CFGCLK Port List

Port	Direction	Function Description
CLKIN	Input	User Master Clock: Used for SPI FLASH in-system direct programming and in-system indirect programming.
CE_N	Input	User Master Clock enable, active low.

8.7.4 Instantiation Template

```

GTP_CFGCLK GTP_CFGCLK_inst (
    .CE_N(ce_n), // INPUT
    .CLKIN(clkin) // INPUT
);
  
```

Chapter 9 Usage Instructions for DDR-related GTP

9.1 GTP_IOCLKDIV_E3

9.1.1 Supported Devices

Table 9-1 GTP_IOCLKDIV_E3-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

9.1.2 Description of Functionality

The function of this GTP is to divide the clock from the PLL to generate the system clock for DDRPHY, with a division factor adjustable to four or eight.

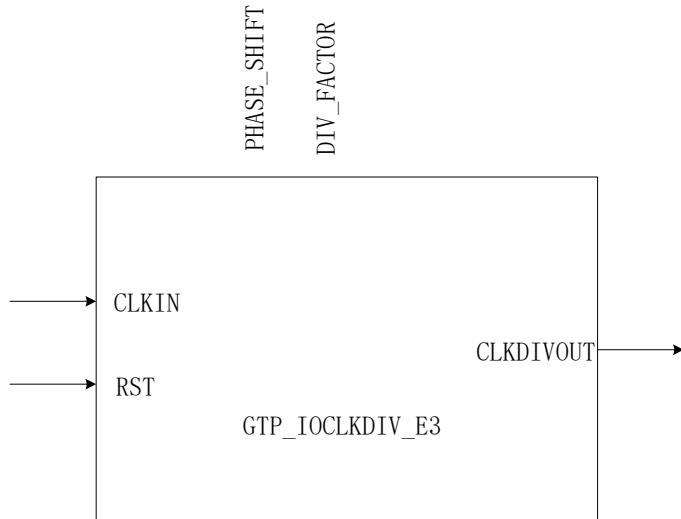


Diagram 9-1 GTP_IOCLKDIV_E3 Structural Diagram

9.1.3 Port Description

Table 9-2 GTP_IOCLKDIV_E3 Port Description

Port Signal	Input/Output	Description
CLKIN	Input	From the PLL IOCLK clock tree
RST	Input	Local control signal, active high
CLKDIVOUT	Output	DDRPHY system clock

9.1.4 Parameter Description

Table 9-3 Description of GTP_IOCLKDIV_E3 Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
PHASE_SHIFT	<string>	"0" "1" "2" "3" "4" "5" "6" "7"	<"0">	PHASE_SHIFT indicates the number of CLKIN cycles by which CLKDIVOUT is delayed after RST is released. The value of PHASE_SHIFT must be less than the division factor DIV_FACTOR.
DIV_FACTOR	<string>	"4" "8"	"8"	Division Factor "4": divide-by-four "8": divide-by-eight

9.1.5 Instantiation Template

```
GTP_IOCLKDIV_E3 #(
    .DIV_FACTOR      ( "8"      ),
    .PHASE_SHIFT     ( "0"      )
) GTP_IOCLKDIV_E3_inst (
    .CLKDIVOUT      (clkdivout),
    .CLKIN          (clkin      ),
    .RST_N          (rst       )
);
```

9.2 GTP_CLKPD

9.2.1 Supported Devices

Table 9-4 GTP_CLKPD-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

9.2.2 Description of Functionality

The main function of CLKPD is to detect the phase difference between the MEMORY CONTROLLER soft core clock and the DDR_PHY system clock, and output the FLAG_PD signal to the SRB. The soft core will convert this signal to the DPS interface to adjust the output phase of the PLL. FLAG_PD will change between 0 and 1 until phase is locked. At this point, LOCK changes to 1, indicating that the soft core clock and the system clock have achieved phase alignment.

When the parameter HPIO is set to "TRUE", CPD_EDGE can be selected as either "POSEDGE" for rising edge alignment or "NEGEDGE" for falling edge alignment.

The Structure Block Diagram is shown below:

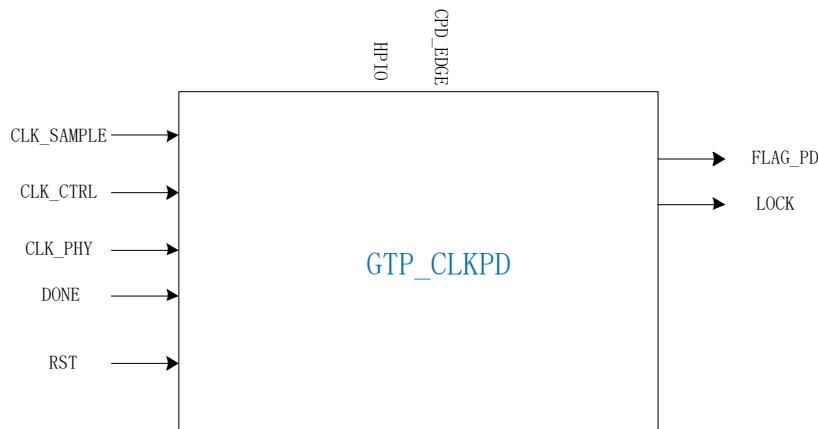


Figure 9-2 GTP_CLKPD Structure Block Diagram

9.2.3 Port Description

Table 9-5 Port Description of GTP_CLKPD

Port Signal	Input/Output	Description
RST	Input	CLKPD local reset control signal, active-low
CLK_SAMPLE	Input	FLAG_PD sampling clock
CLK_CTRL	Input	MEMORY CONTROLLER soft core clock
CLK_PHY	Input	DDR_PHY system clock
DONE	Input	CLKPD_DONE signal, which also changes to high level after LOCK changes from 0 to 1, thereby locking the CLKPD module.
FLAG_PD	Output	A value of "1" controls increasing delay in the PLL; "0" controls decreasing delay in the PLL
LOCK	Output	Upon detecting FLAG_PD jittering between 0 and 1, switch to high level

9.2.4 Parameter Description

Table 9-6 Description of GTP_CLKPD Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
HPIO	string	"TRUE", "FALSE"	"FALSE"	"TRUE" HPIO, "FALSE" HRIO
CPD_EDGE	string	"POSEDGE", "NEGEDGE"	"POSEDGE"	"POSEDGE" rising edge alignment, "NEGEDGE" falling edge alignment

9.2.5 Instantiation Template

GTP_CLKPD

```
gtp_cpd_a#(
    .HPIO ("TRUE"),
    .CPD_EDGE ("POSEDGE"),
    .FLAG_PD(cpd_up_dnb),
    .LOCK(cpd_lock),
    .RST(cpd_rstn),
    .CLK_SAMPLE(clk_io_2x),
    .CLK_CTRL(clk_fb),
    .CLK_PHY(pll_sysclk),
    .DONE(cpd_done)
);
```

9.3 GTP_DDC_E2

9.3.1 Supported Devices

Table 9-7 GTP_DDC_E2-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

9.3.2 Description of Functionality

The main function of DQSL is to generate the write operation clock for the DDR memory; support the write leveling process of DDR3, support clock shutdown operation in quad/half rate mode with shutoff time being an integer multiple of 4 CLKA cycles; phase shift the DQSI signal by ~90 degrees during read operations to capture input data and generate the correct gate identification signal DGTS; detect drift in DQS and send the results to update logic for further processing; generate read/write directional operation signal for the input FIFO; and generate read operation valid judgement signal for core logic.

The Structure Block Diagram is shown below:

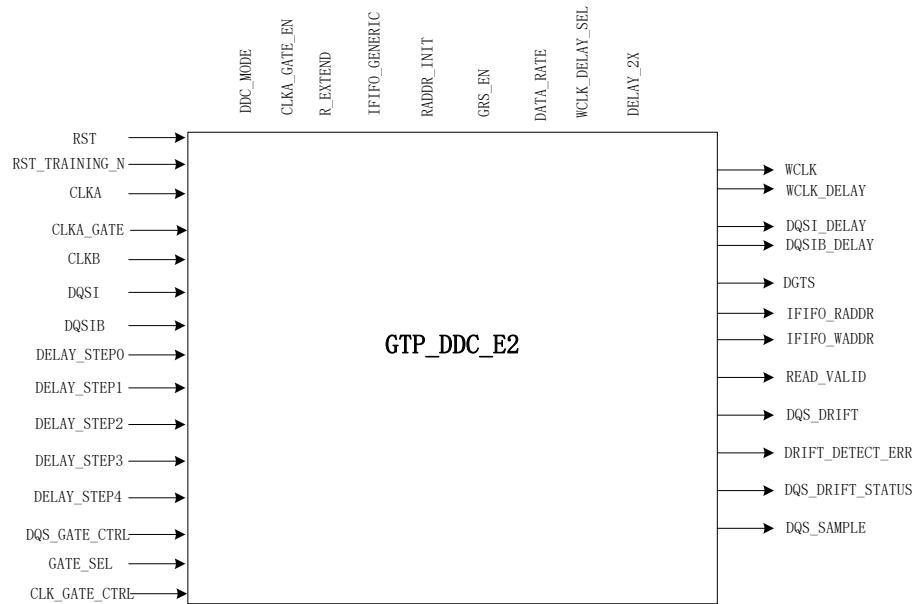


Figure 9-3 GTP_DDC_E2 Structure Block Diagram

9.3.3 Port Description

Table 9-8 Port Description of GTP_DDC_E2

Port Signal	Input/Output	Description
RST	Input	DQS local reset control signal, with polarity controlled by GRS_EN
RST_TRAINING_N	Input	Used to reset the read and write pointer generation and read pointer control logic of DQLS at the end of DQS gate training, active low
CLKA	Input	Clock source is the IOCLK tree
CLKA_GATE	Input	Used for gate clka clock
CLKB	Input	System clock from PLL/SRB
DQSI	Input	Read clock signal
DQSIB	Input	Read clock signal
DELAY_STEP0[7:0]	Input	Code for write leveling training, controlled by soft calibration logic.
DELAY_STEP1[7:0]	Input	Code for Read DQSi even eye training
DELAY_STEP2[7:0]	Input	Code for Read DQSi odd eye training
DELAY_STEP3[7:0]	Input	45L delay control code from the DLL
DELAY_STEP4[7:0]	Input	Code for DQ/DQS training
DQS_GATE_CTRL[3:0]	Input	Used to control the timing of DQS gate
GATE_SEL	Input	DQS GATE coarse tuning selection signal, where the signal selected with "1" is delayed by one clock cycle compared to the signal selected with "0"
CLK_GATE_CTRL[1:0]	Input	DQS GATE fine-tuning control signal, with a phase difference of 90° between each value
WCLK	Output	DQS Write clock
WCLK_DELAY	Output	WCLK phase shift 270K_CLK clock signal
DQSI_DELAY	Output	DQSI signal ~90I phase shift signal used to capture input data
DQSIB_DELAY	Output	DQSIB signal ~90I phase shift signal used to capture input data
DGTS	Output	DQS gate status indicator, "1" for correct gate, "0" for incorrect gate
DQS_DRIFT[1:0]	Output	DQS delay variation detection signal, update logic records this signal and determines whether to execute the update adjustment of gate window position
DRIFT_DETECT_ERR	Output	Error flag for DQS delay variation detection; When it goes high, the PHY triggers an update training operation
DQS_DRIFT_STATUS	Output	DQS delay overrange identification signal; When it goes high, the PHY triggers an update training operation
READ_VALID	Output	Read IFIFO operation active judgement signal, active-high
IFIFO_WADDR	Output	IFIFO write pointer, represented in Gray code
IFIFO_RADDR	Output	IFIFO read pointer, represented in Gray code
DQS_SAMPLE	Output	DQS gate sampling used by soft core training logic

9.3.4 Parameter Description

Table 9-9 Description of GTP_DDC_E2 Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
GRS_EN	<string>	<"TRUE","FALSE">	<"TRUE">	"TRUE" Global RST active, "FALSE" Global RST disable
DDC_MODE	<string>	<"HALF_RATE", "QUAD_RATE">	<"QUAD_RATE">	DQS Operating Mode selection signal "HALF_RATE": x2 mode; supports write leveling "QUAD_RATE": x4 mode; supports write leveling
CLKA_GATE_EN	<string>	<"TRUE","FALSE">	<"FALSE">	"TRUE": GATE function enable, shuts down CLKA, causing the entire DQS to be non-functional in QUAD/HALF_RATE mode; "FALSE": GATE function disable, does not shut down CLKA;
R_EXTEND	<string>	<"TRUE","FALSE">	<"FALSE">	DQS gate window position control signal "TRUE" gate window position has a delay compared to "FALSE": "QUAD_RATE" 1 wclk cycle delay; "HALF_RATE" 1 wclk cycle delay;
IFIFO_GENERIC	<string>	<"TRUE","FALSE">	<"FALSE">	Read/write fifo mode control signal "TRUE": GENERIC mode; "FALSE": DDR MEM mode;
RADDR_INIT	<bit>	<3'b000~3'b111>	<3'b000>	Initial read address value in Generic mode
WCLK_DELAY_SEL	<string>	<"TRUE","FALSE">	<"FALSE">	CLK_W_DEL source selection signal "FALSE" selects ~dqsw90, with a 270-degree phase shift relative to CLK_W; "TRUE" selects dqsw90, with a 90-degree phase shift relative to CLK_W;
DELAY_SEL	<bit>	<1'b1, 1'b0>	<1'b0 >	Add delay for delay chains on low-speed interfaces below 800MHz 1'b0: 1x delay range; 1'b1: 2x delay range
DATA_RATE	<bit>	<2'b00, 2'b01 >	<2'b00>	Adjust LDO output voltage according to different frequencies to meet the delay chain requirements 2'b00: 533-2133Mbps 2'b01: 400Mbps

9.3.5 Instantiation Template

```
GTP_DDC_E2 #(  
    .GRS_EN("TRUE"),  
    .CLKA_GATE_EN("FALSE"),  
    .WCLK_DELAY_SEL("FALSE"),  
    .DDC_MODE("QUAD_RATE"),  
    .R_EXTEND("FALSE"),  
    .DELAY_SEL(1'b0),  
    .IFIFO_GENERIC("FALSE"),  
    .RADDR_INIT('b000),  
    .DATA_RATE('b00)
```

```
) GTP_DDC_E2_inst (  
    .DQS_DRIFT(),  
    .IFIFO_RADDR(),  
    .IFIFO_WADDR(),  
    .CLK_GATE_CTRL(),  
    .DELAY_STEP0(),  
    .DELAY_STEP1(),  
    .DELAY_STEP2(),  
    .DELAY_STEP3(),  
    .DELAY_STEP4(),  
    .DQS_GATE_CTRL(),  
    .DGTS(),  
    .DQSIB_DELAY(),  
    .DQSI_DELAY(),  
    .DQS_DRIFT_STATUS(),  
    .DQS_SAMPLE(),  
    .DRIFT_DETECT_ERR(),  
    .READ_VALID(),  
    .WCLK(),  
    .WCLK_DELAY(),  
    .CLKA(),  
    .CLKA_GATE(),  
    .CLKB(),
```

```

.DQSI(),
.DQSIB(),
.GATE_SEL(),
.RST(),
.RST_TRAINING_N()
);

```

9.4 GTP_IDDR_E1

9.4.1 Supported Devices

Table 9-10 GTP_IDDR_E1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

9.4.2 Description of Functionality

GTP_IDDR_E2 is a data deserializer, with the function as shown below, supporting IDDRx1, SAME_PIPELINED, SAME_EDGE and OPPOSITE_EDGE modes.

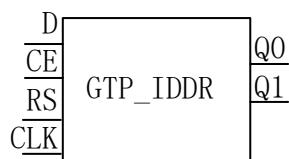


Figure 9-4 GTP_IDDR_E1 Structure Diagram

9.4.3 Port Description

Table 9-11 Port Description of GTP_IDDR_E1

Port Signal	Input/Output	Data Width	Description
D	Input	1	Data Input
CE	Input	1	Clock enable
RS	Input	1	Set/reset
CLK	Input	1	System clock
Q0	Output	1	Deserializer output
Q1	Output	1	Deserializer output

9.4.4 Parameter Description

Table 9-12 GTP_CLKBUFXCE Parameter List Description

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
IDDR_MODE	string	"SAME_PIPELINED" "SAME_EDGE" "OPPOSITE_EDGE"	"OPPOSITE_EDGE"	"SAME_PIPELINED": DDR 1:2 same pipelined deserialisation mode "SAME_EDGE": DDR 1:2 SAME_EDGE deserialisation mode "OPPOSITE_EDGE": DDR 1:2 OPPOSITE_EDGE deserialisation mode
RS_TYPE	string	"SYNC_SET" "ASYNC_SET" "SYNC_RESET" "ASYNC_RESET"	"ASYNC_RESET"	Reset/Set mode selection: Synchronous set, asynchronous set Synchronous reset, asynchronous reset
GRS_EN	string	"FALSE" "TRUE"	"TRUE"	Global reset enable

9.4.5 Instantiation Template

GTP_IDDR_E1 #

```
(  
    . GRS_EN("TRUE"),  
    . IDDR_MODE("OPPOSITE_EDGE"),  
    . RS_TYPE("ASYNC_RESET")  
)
```

GTP_IDDR_E1_inst (

```
.D(d),  
.CE(ce),  
.RS(rs),  
.CLK(clk),  
.Q0(q0),  
.Q1(q1)  
);
```

9.5 GTP_ODDR_E1

9.5.1 Supported Devices

Table 9-13 GTP_ODDR_E1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

9.5.2 Description of Functionality

The GTP_ODDR_E1 is a data parallel-to-serial processing module that supports 2:1, SAME_EDGE, and OPPOSITE_EDGE modes. Its structural diagram is shown below.

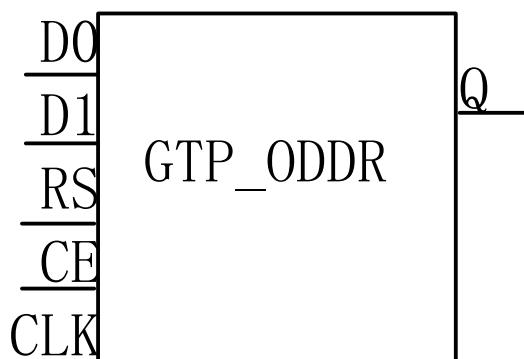


Figure 9-5 GTP_ODDR_E1 Structure Diagram

9.5.3 Port Description

Table 9-14 Port Description of GTP_ODDR_E1

Port Signal	Input/Output	Data Width	Description
D0	Input	1	Data Input
D1	Input	1	Data Input
CE	Input	1	Clock enable
RS	Input	1	Set/reset
CLK	Input	1	System clock
Q	Output	1	Serial data output

9.5.4 Parameter Description

Table 9-15 Description of GTP_ODDR_E1 Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
ODDR_MODE	string	"SAME_EDGE" "OPPOSITE_EDGE"	"SAME_EDGE"	"SAME_EDGE": DDR 2:1 serialisation mode "OPPOSITE_EDGE": DDR 2:1 serialisation mode
GRS_EN	string	"FALSE" "TRUE"	"TRUE"	Global reset enable
RS_TYPE	string	"SYNC_SET" "ASYNC_SET" "SYNC_RESET" "ASYNC_RESET"	"ASYNC_RESET"	Reset/Set mode selection: Synchronous set, asynchronous set Synchronous reset, asynchronous reset

9.5.5 Instantiation Template

```

GTP_ODDR_E1 #
(
    .GRS_EN("TRUE"),
    .ODDR_MODE("SAME_EDGE"),
    .RS_TYPE ("ASYNC_RESET")
) GTP_ODDR_E1_inst (
    .D0(d0),
    .D1(d1),
    .CE(ce),
    .RS(rs),
    .CLK(clk),
    .Q (q)
);
    
```

Chapter 10 Usage Instructions for Other GTPs

10.1 GTP_APM_E2

10.1.1 Supported Devices

Table 10-1 GTP_APM_E2-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

10.1.2 Description of Functionality

GTP_APM_E2 is an arithmetic logic unit that supports various types of logical operations, including multiplication, multiply-accumulate operations, general multiply-add operations, Wide-bit accumulate and add operation and FIR logic operations. The Structure Block Diagram is shown below:

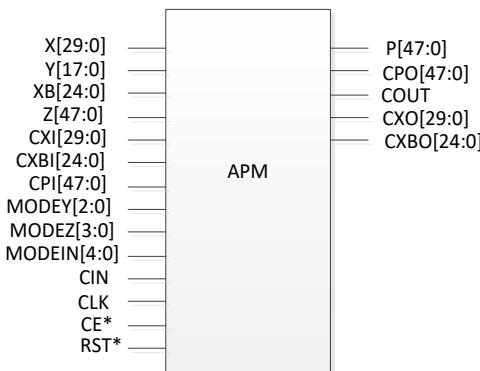


Figure 10-1 GTP_APM_E2 Structure Block Diagram

10.1.3 Port Description

Table 10-2 Port Description of GTP_APM_E2

Port Signal	Input/Output	Description
X[29:0]	Input	Parallel data input X
CXI[29:0]	Input	Cascade X input
CXBI[24:0]	Input	Cascade H input
XB[24:0]	Input	Parallel data input XB
Y[17:0]	Input	Parallel data input Y
Z[47:0]	Input	Parallel data input Z
CPI[47:0]	Input	Cascade P input

Port Signal	Input/Output	Description
CIN	Input	Cascade CIN input
MODEY[2:0]	Input	APM dynamic Y-side control operator
MODEZ[3:0]	Input	APM dynamic Z-side control operator
MODEIN[4:0]	Input	APM dynamic input control operator
CLK	Input	Clock input for DSP MU 0
CEX1	Input	Clock X REG1 enable input
CEX2	Input	Clock X REG2 enable input
CEX3	Input	Clock X REG3 enable input
RSTX	Input	Active-high X Reset input
CEXB	Input	Clock XB enable input
RSTXB	Input	Active-high XB Reset input
CEY1	Input	Clock Y REG1 enable input
CEY2	Input	Clock Y REG2 enable input
RSTY	Input	Active-high Y Reset input
CEZ	Input	Clock Z enable input
RSTZ	Input	Active-high Z Reset input
CEPRE	Input	Clock PRE enable input
RSTPRE	Input	Active-high PRE Reset input
CEM	Input	Clock M enable input
RSTM	Input	Active-high M Reset input
CEP	Input	Clock P enable input
RSTP	Input	Active-high P Reset input
CEMODEIN	Input	Clock MODEIN enable input
RSTMODEIN	Input	Active-high MODEIN Reset input
CEMODEY	Input	Clock MODEY enable input
RSTMODEY	Input	Active-high MODEY Reset input
CEMODEZ	Input	Clock MODEZ enable input
RSTMODEZ	Input	Active-high MODEZ Reset input
P[47:0]	Output	Parallel data output
CPO[47:0]	Output	Cascade P output
COUT	Output	Cascade CIN output
CXO[29:0]	Output	Cascade X output
CXBO[24:0]	Output	Cascade XB output

10.1.4 Parameter Description

Table 10-3 Description of GTP_APM_E2 Parameter List

Parameter Name	Parameter Type	Setting Value	Defaults	Function Description
USE_POSTADD	int	0,1	0	post adder enable
USE_PREADD	int	0,1	0	pre-adder enable
CXO_REG	int	0,1,2,3	0	X cascade out reg latency
X_REG	int	0,1,2,3	0	X_REG register enable
XB_REG	int	0,1	0	XB_REG register enable
Y_REG	int	0,1,2,3	0	Y_REG register enable
Z_REG	int	0,1	0	Z_REG register enable
PREADD_REG	int	0,1	0	preadd register enable
MULT_REG	int	0,1	0	mult register enable
P_REG	int	0,1	0	postadd register enable
MODEIN_REG	int	0,1	0	MODEIN_REG register enable
MODEY_REG	int	0,1	0	MODEY_REG register enable
MODEZ_REG	int	0,1	0	MODEZ_REG register enable
X_SEL	int	0,1	0	mult X input select
XB_SEL	int	0,1,2,3	0	X back propagate mux select
ASYNC_RST	int	0,1	0	async reset enable
USE SIMD	int	0,1	0	mode selector
P_INIT0	binary	48'h0-48'ffff	48'h0	P constant input0
P_INIT1	binary	48'h0-48'ffff	48'h0	P constant input1
ROUNDMODE_SEL	int	0,1	0	Roundmode selection
CPO_REG	int	0,1	0	PO,PCO use register output enable
USE_ACCLOW	int	0,1	0	acc use lower 18-bit feedback only enable
CIN_SEL	int	0,1	0	select PCI for postadder carry in
GRS_EN	string	"TRUE","FALSE"	"TRUE"	Global Reset enable
USE_MULT	int	0,1	1	Mult enable

10.1.5 Instantiation Template

```
GTP_APM_E2 #(
    .GRS_EN("TRUE"),
    .ASYNC_RST(0),
    .X_REG(0),
    .XB_REG(0),
    .Y_REG(0),
```



```

.Z          (z      ),
.COUT      (cout    ),
.CEM       (cem     ),
.CEMODEIN  (cemodein),
.CEMODEY   (cemodey ),
.CEMODEZ   (cemodez ),
.CEP       (cep     ),
.CEPRE     (cepre   ),
.CEX1      (cex1    ),
.CEX2      (cex2    ),
.CEX3      (cex3    ),
.CEXB      (cexb    ),
.CEY1      (cey1    ),
.CEY2      (cey2    ),
.CEZ       (cez     ),
.CIN       (cin     ),
.CLK       (clk     ),
.RSTM      (rstm    ),
.RSTMODEIN (rstmodein),
.RSTMODEY  (rstmodey ),
.RSTMODEZ  (rstmodez ),
.RSTP      (rstp    ),
.RSTPRE    (rstpre  ),
.RSTX      (rstx    ),
.RSTXB    (rstxb   ),
.RSTY      (rsty    ),
.RSTZ      (rstz    )
);

```

10.1.6 Detailed Description of Functionality

For detailed instructions, please refer to "*UG040003_Logos2 Family FPGAs Arithmetic Processing Module (APM) User Guide*"

10.2 GTP_GRS

10.2.1 Supported Devices

Table 10-4 GTP_GRS-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

10.2.2 Description of Functionality

This GTP is used to control the global reset signal.

10.2.3 Port Description

Table 10-5 GTP_GRS Port Description

Port Signal	Input/Output	Description
GRS_N	input	Global reset

10.2.4 Instantiation Template

```
GTP_GRS GTP_GRS_inst (
    .GRS_N(grs_n)
);
```

10.3 GTP_START_E1

10.3.1 Supported Devices

Table 10-6 GTP_START_E1-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

10.3.2 Description of Functionality

This GTP describes the process of releasing the global signal for the wake-up operation.

10.3.3 Port Description

Table 10-7 GTP_START_E1 Port Description

Port Signal	Input/Output	Description

Port Signal	Input/Output	Description
CLK	input	Wake-up clock
GOE	input	Global IO output enable
GRS_N	input	Global reset
GWE	input	Memory write enable
WAKEUP_OVER	Output	Wake-up completion flag signal

10.3.4 Instantiation Template

```
GTP_START_E1 GTP_START_E1_inst (
    .WAKEUP_OVER      (wakeup_over),
    .CLK              (clk      ),
    .GOE              (goe      ),
    .GRS_N            (grs_n   ),
    .GWE              (gwe      )
);
```

10.4 GTP_ADC_E2

10.4.1 Supported Devices

Table 10-8 GTP_ADC_E2-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

10.4.2 Description of Functionality

GTP_ADC_E2 is used to implement ADC functions. For detailed functionality, please refer to "UG040009_Logos2 Family FPGAs Analog-to-Digital Conversion (ADC) Module User Guide".

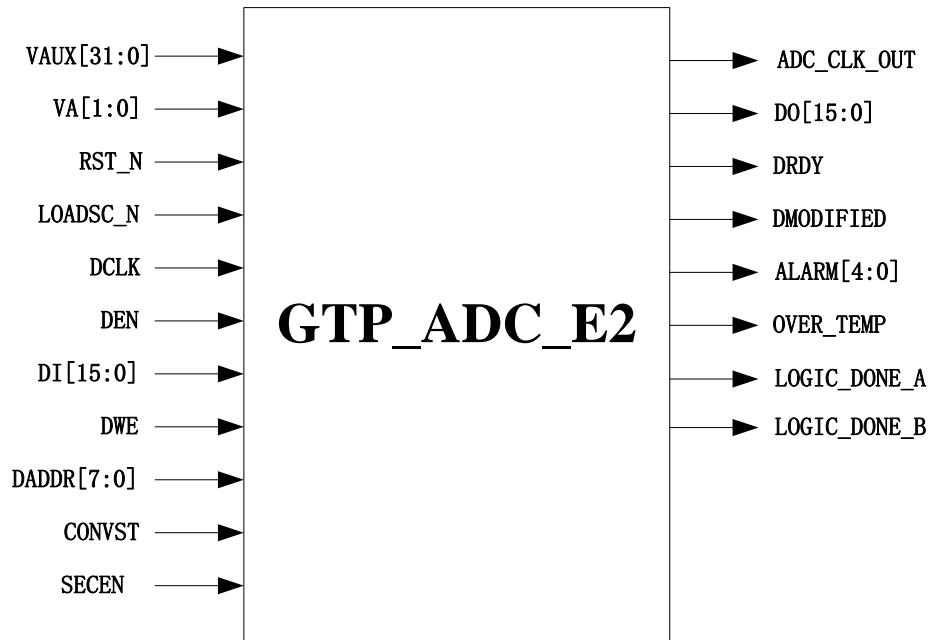


Figure 10-2 GTP_ADC_E2 Structure Diagram

10.4.3 Port Description

Table 10-9 GTP_ADC_E2 Port List

Port	Direction	Function Description
VA[1:0]	Input	Dedicated analogue input port, VA[1] and VA[0] form a differential pair, with VA[0] being the N terminal and VA[1] being the P terminal
VAUX[31:0]	Input	Multi-funtion analogue differential input port (multiplexed through IOB), with IOB constrained to 1.8V power standard. VAUX[2*n+1] and VAUX[2*n] form a differential pair, corresponding to the P and N terminals of port n
DCLK	Input	APB clock
DADDR[7:0]	Input	APB operation address bit
DEN	Input	Data transfer enable signal
SECEN	Input	Operation enable; initiates a read/write operation when active high
DWE	Input	Write operation enable: 0 for read, 1 for write
DI[15:0]	Input	APB data input
CONVST	Input	Event-drive control signal, which triggers sampling in event-drive mode
RST_N	Input	System reset signal, active-low
LOADSC_N	Input	Enable control register loaded into static configuration value signal, active low. Triggers internal reconfiguration of the ADC control register.

Port	Direction	Function Description
DO[15:0]	Output	APB data output
DRDY	Output	APB read/write execution end flag bit
OVER_TEMP	Output	Over temperature indicator signal
LOGIC_DONE_A	Output	ADC status register update signal
LOGIC_DONE_B	Output	ADC status register update signal
ADC_CLK_OUT	Output	ADC working clock ad_clk output port
DMODIFIED	Output	Control register modification flag, indicates that the control register has been written to by JTAG but the user has not performed any APB operation yet. After the JTAG write operation is completed, the DMODIFIED signal will be pulled high. The subsequent APB read/write operations will reset the DMODIFIED signal
ALARM[4:0]	Output	Alarm indicator signal ALARM[0] is the temperature alarm signal; ALARM[1] is the VCC alarm signal; ALARM[2] is the VCCA alarm signal; ALARM[3] is the VCC_CRAM alarm signal; ALARM[4] is the VCC_DRM alarm signal;

10.4.4 Paramater Description

Table 10-10 GTP_ADC_E2 Parameter List

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
CREG_00H[15:0]	<binary>	16'h0~16'hFFFF	16'h0001	For detailed instructions, please refer to "UG040009_Logos2 FPGAs Analog-to-Digital Converter (ADC) Module User Guide"
CREG_01H[15:0]	<binary>	16'h0~16'hFFFF	16'hC83F	
CREG_02H[15:0]	<binary>	16'h0~16'hFFFF	16'h0009	
CREG_31H[13:0]	<binary>	14'h0~14'h3FFF	14'h0	
CREG_03H[15:0]	<binary>	16'h0~16'hFFFF	16'h0	Enable channel: 1 enable; 0 disable
CREG_04H[15:0]	<binary>	16'h0~16'hFFFF	16'h0	Enable channel: 1 enable; 0 disable
CREG_0AH[15:0]	<binary>	16'h0~16'hFFFF	16'h0	Enable channel: 1 enable; 0 disable
CREG_05H[15:0]	<binary>	16'h0~16'hFFFF	16'h0	Select the scan mode: 1 bipolar; 0 unipolar
CREG_06H[15:0]	<binary>	16'h0~16'hFFFF	16'h0	Select the scan mode: 1 bipolar; 0 unipolar
CREG_0CH[15:0]	<binary>	16'h0~16'hFFFF	16'h0	Select the scan mode: 1 bipolar; 0 unipolar
CREG_07H[15:0]	<binary>	16'h0~16'hFFFF	16'h0	Whether to enable averaging: 1 enable; 0 disable
CREG_08H[15:0]	<binary>	16'h0~16'hFFFF	16'h0	Whether to enable averaging: 1 enable; 0 disable
CREG_0EH[15:0]	<binary>	16'h0~16'hFFFF	16'h0	Whether to enable averaging: 1 enable; 0 disable

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
CREG_20H[11:0]	<binary>	12'h0~12'hFFF	12'h0	Internal temperature sensor upper threshold setting
CREG_21H[11:0]	<binary>	12'h0~12'hFFF	12'h0	Internal temperature sensor lower threshold setting
CREG_22H[11:0]	<binary>	12'h0~12'hFFF	12'h0	Internal voltage VCC upper threshold setting
CREG_23H[11:0]	<binary>	12'h0~12'hFFF	12'h0	Internal voltage VCC lower threshold setting
CREG_24H[11:0]	<binary>	12'h0~12'hFFF	12'h0	Internal voltage VCCA upper threshold setting
CREG_25H[11:0]	<binary>	12'h0~12'hFFF	12'h0	Internal voltage VCCA lower threshold setting
CREG_26H[11:0]	<binary>	12'h0~12'hFFF	12'h0	Internal voltage VCC_DRM upper threshold setting
CREG_27H[11:0]	<binary>	12'h0~12'hFFF	12'h0	Internal voltage VCC_DRM lower threshold setting
CREG_28H[11:0]	<binary>	12'h0~12'hFFF	12'h0	Internal voltage VCC_CRAM upper threshold setting
CREG_29H[11:0]	<binary>	12'h0~12'hFFF	12'h0	Internal voltage VCC_CRAM lower threshold setting
CREG_2AH[11:0]	<binary>	12'h0~12'hFFF	12'hCC2	Over temperature upper threshold setting
CREG_2BH[11:0]	<binary>	12'h0~12'hFFF	12'hA5B	Over temperature lower threshold setting

10.4.5 Instantiation Template

GTP_ADC_E2 #(

```

    .CREG_00H('b0000000000000001),
    .CREG_01H('b110010000011111),
    .CREG_02H('b0000000000001001),
    .CREG_31H('b000000000000000),
    .CREG_03H('b000000000000000),
    .CREG_04H('b000000000000000),
    .CREG_0AH('b000000000000000),
    .CREG_05H('b000000000000000),
    .CREG_06H('b000000000000000),
    .CREG_0CH('b000000000000000),
    .CREG_07H('b000000000000000),
    .CREG_08H('b000000000000000),
    .CREG_OEH('b000000000000000),
    .CREG_20H('b000000000000),
    .CREG_21H('b000000000000),

```

```

.CREG_22H('b00000000000000),
.CREG_23H('b00000000000000),
.CREG_24H('b00000000000000),
.CREG_25H('b00000000000000),
.CREG_26H('b00000000000000),
.CREG_27H('b00000000000000),
.CREG_28H('b00000000000000),
.CREG_29H('b00000000000000),
.CREG_2AH('b110011000010),
.CREG_2BH('b101001011011))

GTP_ADC_E2_inst (
    .ALARM          (alarm      ),
    .DO             (do        ),
    .DADDR          (daddr      ),
    .DI             (di        ),
    .VAUX           (vaux      ),
    .ADC_CLK_OUT   (adc_clk_out ),
    .DMODIFIED      (dmodified  ),
    .DRDY           (drdy      ),
    .LOGIC_DONE_A   (logic_done_a),
    .LOGIC_DONE_B   (logic_done_b),
    .OVER_TEMP      (over_temp  ),
    .CONVST          (convst     ),
    .DCLK            (dclk      ),
    .DEN             (den       ),
    .DWE             (dwe       ),
    .LOADSC_N       (loadsc_n  ),
    .RST_N           (rst_n     ),
    .SECEN           (secen     ),
    .VA              (va        )
);

```

10.5 GTP_PCIEGEN2

10.5.1 Supported Devices

Table 10-11 GTP_PCIEGEN2-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

10.5.2 Description of Functionality

GTP_PCIEGEN2 (Peripheral Component Interconnect Express) high-speed serial interface module is compatible with PCIE2.1 protocol. Key items include: support both Gen1 and Gen2 rates (2.5Gb/s or 5Gb/s); support EP and RC modes as well as x1, x2, and x4; TLP packet max_payload can be flexibly configured to 128Bytes, 256 Bytes, 512 Bytes or 1024 Bytes; BAR registers are configurable; support three types of interrupt mechanisms: Legacy, MSI, and MSIX; Power Management, Lane Reversal, Lane Polarity Inversion are all achievable. A simplified block diagram of its structure is shown below:

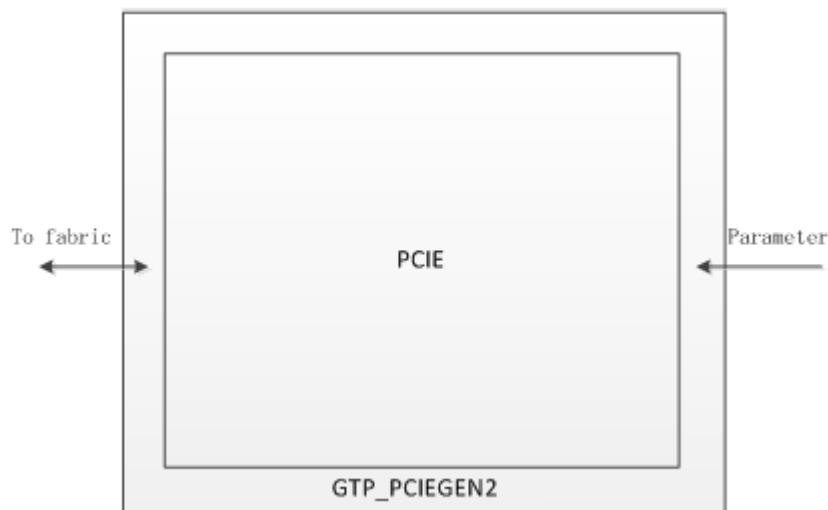


Figure 10-3 GTP_PCIEGEN2 Structure Diagram

10.5.3 Port Description

Table 10-12 GTP_PCIEGEN2 Port List

Port	Direction	Bit width	Function Description
PCLK	I	1	PIPE clock from external PHY Multiplexed as test_clk in DFT mode Gen1: 125Mhz Gen2: 250Mhz
PCLK_DIV2	I	1	pclk_div2 clock from external PHY, two divided from PCLK Multiplexed as test_clk in DFT mode Gen1: 62.5Mhz Gen2: 125Mhz
MEM_CLK	I	1	Used to receive the memory clock, which shares the same source with pclk.
BUTTON_RST	I	1	Button reset, Active high
POWER_UP_RST	I	1	Warm reset, Active high
PERST	I	1	Reset from Socket, Active high
CORE_RST_N	O	1	Resets the controller, except for the PMC module, It is recommended that you reset your application logic together with the controller, Active low
TRAINING_RST_N	O	1	Hot reset from upstream component, Active low
APP_INIT_RST	I	1	Request from your application to send a hot reset to the upstream port; Active high
PHY_RST_N	O	1	For phy rst, Active low
DEVICE_TYPE	I	3	Device/port type. Indicates the specific type of this PCI Express function. 3'b000: PCI Express endpoint 3'b001: Legacy PCI Express endpoint 3'b100: Root port of PCI Express root complex
RX_LANE_FLIP_EN	I	1	Performs manual lane reversal for receive lanes.
TX_LANE_FLIP_EN	I	1	Performs manual lane reversal for transmit lanes
APP_LTSSM_ENABLE	I	1	Driven low by your application after cold, warm or hot reset to hold the LTSSM in the Detect state until your application is ready for the link training to begin.
SMLH_LINK_UP	O	1	PHY Link up/down indicator
RDLH_LINK_UP	O	1	Data link layer up/down indicator
APP_REQ_RETRY_EN	I	1	Provides a capability to defer incoming configuration requests until initialisation is complete
SMLH_LTSSM_STATE	O	5	Current state of the LTSSM
AXIS_MASTER_TVALID	O	1	Active high to indicate that the ctrl is driving a valid transfer
AXIS_MASTER_TREADY	I	1	Active high to indicate that the user can accept a transfer in the current cycle
AXIS_MASTER_TDATA	O	128	Primary payload provide to user logic

Port	Direction	Bit width	Function Description
AXIS_MASTER_TKEEP	O	4	Active high to enable related DW in axis_master_tdata; axis_master_tkeep[3] control axis_master_tdata[127:96]; axis_master_tkeep[2] control axis_master_tdata[95:64]; axis_master_tkeep[1] control axis_master_tdata[63:32]; axis_master_tkeep[0] control axis_master_tdata[31:0]; Note: The difference from the AXIS standard is that here one bit corresponds to the enable of 4 bytes
AXIS_MASTER_TLAST	O	1	Active high to indicate last valid transfer of a packet from ctrl
AXIS_MASTER_TUSER	O	8	Sideband information transmitted alongside axis_master_tdata: 0: radm_trgt1_tlp_abort (Indicates to your application to drop the TLP because of malformed TLP on TRGT1, ECRC error, or completion lookup failures) 1: radm_trgt1_dllp_abort (Indicates to your application to drop the TLP on TRGT1 because of a Data Link Layer error such as LCRC or otherwise) 2: radm_trgt1_ecrc_err (Indicates to your application to drop the TLP because of an ECRC error in the received TLP on TRGT1) 3: radm_trgt1_cpl_last: Indicates the last completion TLP of a split completion transaction. [6:4]: radm_trgt1_in_membar_range[2:0] (Indicates which of the configured BARs contains the target address in the received TLP) 7: radm_trgt1_rom_in_range (Indicates that the target address in the received TLP in range of the expansion ROM)
TRGT1_RADM_PKT_HALT	I	3	Halts the transfer of packets from individual queues. There is one bit of trgt1_radm_pkt_halt for each TLP type for each configured VC: Bit 0: Halt posted TLPs for VC0 Bit 1: Halt non-posted TLPs for VC0 Bit 2: Halt CPL TLPs for VC0
RADM_GRANT_TLP_TYPE	O	6	Indicates that a particular VC and type transaction has been granted to output from the receive queue. There is one bit for each TLP type for each configured VC: Bit [1:0]: Grant posted TLPs for VC0 Bit [3:2]: Grant non-posted TLPs for VC0 Bit [5:4]: Grant CPL TLPs for VC0
AXIS_SLAVE0/1/2_TREADY	O	1	Active high to indicate that the ctrl can accept a transfer in the current cycle
AXIS_SLAVE0/1/2_TVALID	I	1	Active high to indicate that the user is driving a valid transfer
AXIS_SLAVE0/1/2_TDATA	I	128	Primary payload provide to ctrl
AXIS_SLAVE0/1/2_TLAST	I	1	Active high to indicate last valid transfer of a

Port	Direction	Bit width	Function Description
			packet to ctrl
AXIS_SLAVE0/1/2_TUSER	I	1	Sideband information transmitted alongside axis_slave_tdata: Bit 0: client0/1/2_tlp_bad_eot, Indicates that the current TLP must be nullified.
DBI_ADDR	I	32	Address of the configuration register for the current DBI access [31:2] register address, must be dword-aligned [1] not used [0] DBI access direction,0: internal register 1: external register via ELBI
DBI_DIN	I	32	Write data bus to the selected configuration register
DBI_CS	I	1	Chip select input to access the CDM or ELBI
DBI_CS2	I	1	Additional chip select that enables writing to BAR mask registers
DBI_WR	I	4	Indicates the configuration register access type (read or write).
APP_DBI_RO_WR_DISABLE	I	1	DBI Read-only Write Disable 0: MISC_CONTROL_1_OFF.DBI_RO_WR_EN register field is read-write. 1: MISC_CONTROL_1_OFF.DBI_RO_WR_EN register field is forced to 0 and is read-only.
LBC_DBI_ACK	O	1	Indicates that the requested read or write operation to the selected configuration register is complete.
LBC_DBI_DOUT	O	32	Read data bus from the selected configuration register.
SEDI	I	1	Serial signal input, driven by slave
SEDI_ACK	I	1	Serial signal input ACK, driven by slave
SEDO	O	1	Serial signal output, driven by master
SEDO_EN	O	1	Serial signal output enable, driven by master
CFG_INT_DISABLE	O	1	When high a functions ability to generate INTx messages is Disabled
SYS_INT	I	1	When sys_int goes from low to high, the controller generates an Assert_INTx Message
INTA_GRT_MUX	O	1	EP: 0->1: The signal indicates that the controller sent an Assert_INTA Message to the upstream device. 1->0: The signal indicates that the controller sent an Deassert_INTA Message to the upstream device. RC: 0->1: The signal indicates that the controller received an Assert_INTA Message from the downstream device 1->0: The signal indicates that the controller received an Deassert_INTA Message from the downstream device

Port	Direction	Bit width	Function Description
INTB_GRT_MUX	O	1	EP:Not used RC: 0->1: The signal indicates that the controller received an Assert_INTB Message from the downstream device 1->0: The signal indicates that the controller received an Deassert_INTB Message from the downstream device
INTC_GRT_MUX	O	1	EP:Not used RC: 0->1: The signal indicates that the controller received an Assert_INTC Message from the downstream device 1->0: The signal indicates that the controller received an Deassert_INTC Message from the downstream device
INTD_GRT_MUX	O	1	EP:Not used RC: 0->1: The signal indicates that the controller received an Assert_INTD Message from the downstream device 1->0: The signal indicates that the controller received an Deassert_INTD Message from the downstream device
VEN_MSI_REQ	I	1	Request from your application to send an MSI when MSI is enabled
VEN_MSI_TC	I	3	Traffic Class of the MSI request, valid when ven_msi_req is asserted
VEN_MSI_VECTOR	I	5	Used to modulate the lower five bits of the MSI Data register when multiple message mode is enabled
VEN_MSI_GRANT	O	1	One-cycle pulse that indicates that the controller has accepted the request to send an MSI
CFG_MSI_PENDING	I	32	Indication from application about which functions have a pending associated message
CFG_MSI_EN	O	1	Indicates that MSI is enabled (INTx message is not sent)
CFG_MSIX_EN	O	1	The MSI-X Enable bit of the MSI-X Control register in the MSI-X Capability structure
MSIX_ADDR	I	64	The address value for the MSI-X.
MSIX_DATA	I	32	The data value for the MSI-X.
CFG_MSIX_FUNC_MASK	O	1	The function Mask bit of the MSI-X Control register in the MSI-X Capability structure.
CFG_LINK_AUTO_BW_MUX	O	1	cfg_link_auto_bw_int when legacy int is used, cfg_link_auto_bw_msi when MSI or MSI-X is enabled. Only for RC
CFG_BW_MGT_MUX	O	1	cfg_bw_mgt_int when legacy int is used, cfg_bw_mgt_msi when MSI or MSI-X is enabled. Only for RC
CFG_PME_MUX	O	1	cfg_pme_int when legacy int is used, cfg_pme_msi when MSI or MSI-X is enabled.
CFG_AER_RC_ERR_MUX	O	1	cfg_aer_rc_err_int: when MSI/MSI-X is NOT enabled. Other wise used as cfg_aer_rc_err_msi
RADM_PM_TURNOFF	O	1	One-clock-cycle pulse that indicates that the controller received a PME Turnoff message

Port	Direction	Bit width	Function Description
RADM_MSG_UNLOCK	O	1	One-cycle pulse that indicates that the controller received an Unlock message
OUTBAND_PWRUP_CMD	I	1	Wake Up. Used by application logic to wake up the PMC state machine from a D1, D2 or D3 power state.
PM_XTLH_BLOCK_TLP	O	1	Indicates that your application must stop generating new outgoing request TLPs due to the current power management state
PM_STATUS	O	1	PME Status bit from the PMCSR
PM_DSTATE	O	3	The current power management D-state of the function
AUX_PM_EN	O	1	Auxiliary Power Enable bit in the Device Control register
PM_PME_EN	O	1	PME Enable bit in the PMCSR
PM_LINKST_IN_L0S	O	1	Power management is in L0s state.
PM_LINKST_IN_L1	O	1	Power management is in L1 state.
PM_LINKST_IN_L2	O	1	Power management is in L2 state.
PM_LINKST_L2_EXIT	O	1	Power management is exiting L2 state
APP_REQ_ENTR_L1	I	1	Application request to Enter L1 ASPM state
APP_READY_ENTR_L23	I	1	Application Ready to Enter L23.
APP_REQ_EXIT_L1	I	1	Application request to Exit L1
APP_XFER_PENDING	I	1	Indicates that your application has transfers pending and prevents the controller from entering L1.
WAKE	O	1	Wake Up. Wake up from power management unit.
RADM_PM_PME	O	1	One-clock-cycle pulse that indicates that the controller received a PM_PME message
RADM_PM_TO_ACK	O	1	One-clock-cycle pulse that indicates that the controller received a PME_TO_Ack message
APPS_PM_XMT_TURNOFF	I	1	Request from your application to generate a PM_Turn_Off message.
APP_UNLOCK_MSG	I	1	Request from your application to generate an Unlock message
APPS_PM_XMT_PME	I	1	Wake Up. Used by application logic to wake up the PMC state machine from a D1, D2 or D3 power state
APP_CLK_PM_EN	I	1	Clock PM feature enabled by application.
PM_MASTER_STATE	O	5	Power management master FSM state
PM_SLAVE_STATE	O	5	Power management slave FSM state
SYS_AUX_PWR_DET	I	1	Auxiliary Power Detected. Used to report to the host software that auxiliary power (Vaux) is present
CFG_MAX_RD_REQ_SIZE	O	3	The value of the Max_Read_Request_Size field in the Device Control register.
CFG_BUS_MASTER_EN	O	1	The state of the bus master enable bit in the PCI-compatible Command register.
CFG_MAX_PAYLOAD_SIZE	O	3	The value of the Max_Payload_Size field in the Device Control register
CFG_EXT_TAG_EN	O	1	When enabled, controller supports up to 8-bit tag values.

Port	Direction	Bit width	Function Description
CFG_RCB	O	1	The value of the RCB bit in the Link Control register.
CFG_MEM_SPACE_EN	O	1	The state of the Memory Space Enable bit in the PCI-compatible Command register.
CFG_PM_NO_SOFT_RST	O	1	This is the value of the No Soft Reset bit in the Power Management Control and Status Register
CFG_CRS_SW_VIS_EN	O	1	Indicates the value of the CRS Software Visibility enable bit in the Root Control register
CFG_NO_SNOOP_EN	O	1	Contents of the "Enable No Snoop" field (PCIE_CAP_EN_NO_SNOOP) in the "Device Control and Status" register (DEVICE_CONTROL_DEVICE_STATUS) register
CFG_RELAX_ORDER_EN	O	1	Contents of the "Enable Relaxed Ordering" field (PCIE_CAP_EN_REL_ORDER) in the "Device Control and Status" register (DEVICE_CONTROL_DEVICE_STATUS) register
CFG_TPH_REQ_EN	O	2	The 2-bit TPH Requester Enabled field of each TPH Requester Control register.
CFG_PF_TPH_ST_MODE	O	3	Steering Tag Mode of Operation for Physical Function
CFG_PBUS_NUM	O	8	The primary bus number assigned to the function
CFG_PBUS_DEV_NUM	O	5	The device number assigned to the function
CFG_ATOMIC_REQ_EN	O	1	The AtomicOp Requester Enable field of the Device Control 2 register
CFG_ATOMIC_EGRESS_BLOCK	O	1	The AtomicOp Egress Blocking field of the Device Control 2 register
RBAR_CTRL_UPDATE	O	1	Indicates that a resizable BAR control register has been updated
APP_HDR_VALID	I	1	One-clock-cycle pulse indicating that the data app_hdr_log,
APP_HDR_LOG	I	128	The header of the TLP that contained the error indicated app_err_bus, valid when app_hdr_valid is asserted; Provide app_tlp_prfx_log before app_hdr_valid is asserted if needed
APP_ERR_BUS	I	13	The type of error that your application detected
APP_ERR_ADVISORY	I	1	Indicates that your application error is an advisory error.
CFG_SEND_COR_ERR_MUX	O	1	EP: cfg_send_cor_err Sent Correctable Error. RC: radmin_correctable_err, One-clock-cycle pulse that indicates that the controller received an ERR_COR message.
CFG_SEND_NF_ERR_MUX	O	1	EP: radmin_nonfatal_err, Sent Non-Fatal Error RC: One-clock-cycle pulse that indicates that the controller received an ERR_NONFATAL message
CFG_SEND_F_ERR_MUX	O	1	EP: radmin_fatal_err, Sent Fatal Error RC: One-clock-cycle pulse that indicates that the controller received an ERR_FATAL message.
CFG_SYS_ERR_RC	O	1	System error detected
RADM_CPL_TIMEOUT	O	1	Indicates that the completion TLP for a request has not been received within the expected time window

Port	Direction	Bit width	Function Description
RADM_TIMEOUT_CPL_TC	O	3	The Traffic Class of the timed out completion
RADM_TIMEOUT_CPL_TAG	O	8	The Tag field of the timed out completion
RADM_TIMEOUT_CPL_ATTR	O	2	The Attributes field of the timed out completion.
RADM_TIMEOUT_CPL_LEN	O	11	Length (in bytes) of the timed out completion. For a split completion, it indicates the number of bytes remaining to be delivered when the completion timed out.
DYN_DEBUG_INFO_SEL	I	4	Dynamic debug_info_mux selection
APP_RAS DES_SD_HOLD_LTSSM	I	1	Hold and release LTSSM. For as long as this signal is '1', the controller stays in the current LTSSM.
APP_RAS DES_TBA_CTRL	I	2	Controls the start/end of time based analysis. You must only set the pins to the required value for the duration of one clock cycle. <ul style="list-style-type: none"> ■ 2'b00: No action ■ 2'b01: Start ■ 2'b10: End. This setting is only used when the TIME_BASED_DU-RATION_SELECT field of TIME_BASED_ANALYSIS_CONTROL_REG is set to "manual control". ■ 2'b11: Reserved
RADM_IDLE	O	1	RADM activity status signal
RADM_Q_NOT_EMPTY	O	1	Level indicating that the receive queues contain TLP header/data.
RADM_QOVERFLOW	O	1	Pulse indicating that one or more of the P/NP/CPL receive queues have overflowed
DIAG_CTRL_BUS	I	2	Diagnostic Control Bus, 01: Insert LCRC error by inverting the LSB of LCRC 10: Insert ECRC error by inverting the LSB of ECRC
DEBUG_INFO_MUX	O	133	When DYN_DEBUG_SEL_EN =0,use DEBUG_INFO_SEL When DYN_DEBUG_SEL_EN =1,use DYN_DEBUG_INFO_SEL * _DEBUG_INFO_SEL=0: MSI [31:0] cfg_msi_mask[31:0] [95:32] cfg_msi_addr[63:0] [127:96] cfg_msi_data[31:0] 128 cfg_msi_64 [131:129] cfg_multi_msi_en[2:0] 132 cfg_msi_ext_data_en * _DEBUG_INFO_SEL=1: MSI-X [10:0] cfg_msix_table_size[10:0] [13:11] cfg_msix_table_bir[2:0] [42:14] cfg_msix_table_offset[28:0] [45:43] cfg_msix_pba_bir[2:0] [74:46] cfg_msix_pba_offset[28:0] * _DEBUG_INFO_SEL=2: TX debug &DL debug 0 xadm_no_fc_credit[NVC-1:0]

Port	Direction	Bit width	Function Description
			1 xadm_notlp_pending 2 xadm_had_enough_credit[NVC-1:0] 3 xdlh_not_expecting_ack 4 xdlh_xmt_pme_ack 5 xdlh_nodllp_pending [14:6] rtfcgen_incr_amt[8:0] 15 rtfcgen_incr_enable [17:16] rtfcgen_fctype[1:0] 18 xdlh_xtlh_halt 19 xtlh_xdlh_badeot 20 xtlh_xdlh_eot 21 xtlh_xdlh_sot [26:22] active_grant[NCL+2-1:0] [31:27] grant_ack[NCL+2-1:0] [36:32] fc_cds_pass[(NCL+2)*NVC-1:0] [41:37] arb_reqs[NCL+2-1:0] 42 xmlh_xdlh_halt [44:43] xdlh_xmlh_sdp[1:0] [46:45] xdlh_xmlh_stp[1:0] [48:47] xdlh_xmlh_eot[1:0] [60:49] rdlh_xdlh_req_acknack_seqnum[11:0] 61 rdlh_xdlh_req2send_nack 62 rdlh_xdlh_req2send_ack_due2dup 63 rdlh_xdlh_req2send_ack [75:64] rdlh_xdlh_rcvd_acknack_seqnum[11:0] 76 rdlh_xdlh_rcvd_ack 77 rdlh_xdlh_rcvd_nack 78 cfg_link_retrain 79 rtlh_req_link_retrain 80 xdlh_smlh_start_link_retrain 81 rdlh_rtlh_tlp_dv [83:82] rdlh_rtlh_tlp_eot[1:0] [85:84] rdlh_rtlh_tlp_sot[1:0] 86 ecrc_err_asserted 87 lcrc_err_asserted *_DEBUG_INFO_SEL = 3: 0 unexpected_cpl_err 1 cpl_ca_err 2 cpl_ur_err 3 flt_q_cpl_last 4 flt_q_cpl_abort 5 cpl_mlf_err [8:6]flt_q_header_cpl_status[2:0] [10:9] flt_q_header_destination[1:0] 11 form_filt_ecrc_err 12 form_filt_malform_tlp_err 13 form_filt_dllp_err 14 form_filt_eot [16:15] form_filt_dwen[NW-1:0] 17 form_filt_dv 18 form_filt_hv [20:19] rmlh_rdlh_pkt_err[NW-1:0] 21 rmlh_rdlh_pkt_dv [23:22] rmlh_rdlh_pkt_edb[NW-1:0] [25:24] rmlh_rdlh_pkt_end[NW-1:0] [27:26] rmlh_rdlh_tlp_start[NW-1:0]

Port	Direction	Bit width	Function Description
			<p>[29:28] rmlh_rdlh_dllp_start[NW-1:0] [31:30] rmlh_rdlh_nak[NW-1:0] [35:32] smlh_lanes_rcving[NL-1:0]</p> <p>36 rmlh_rcvd_eidle_set 37 rmlh_rcvd_idle0 38 rmlh_rcvd_idle1 39 smlh_rcvd_lane_rev 40 smlh_ts_link_num_is_k237 41 rmlh_deskew_alignment_err 42 smlh_ts_lane_num_is_k237 43 smlh_ts2_rcvd 44 smlh_ts1_rcvd 45 smlh_ts_rcv_err 46 smlh_inskip_rcv</p> <p>*_DEBUG_INFO_SEL=4: [48:0] cxpl_debug_info[63:0] [64:49] cxpl_debug_info_ei[15:0] [67:65] pm_curnt_state[2:0]</p> <p>68 pm_sel_aux_clk 69 en_muxd_aux_clk_g 70 en_radm_clk_g 71 link_req_RST_NOT 72 pm_req_core_RST 73 pm_req_phy_RST 74 pm_req_sticky_RST 75 pm_req_non_sticky_RST</p> <p>*_DEBUG_INFO_SEL=5: [7:0]cfg_int_pin[7:0] [43:8] cfg_rbar_size[35:0] 44 cfg_br_ctrl_serren 45 xdlh_replay_timeout_err 46 xdlh_replay_num_rlover_err 47 rdlh_bad_dllp_err 48 rdlh_bad_tlp_err 49 rdlh_prot_err 50 rtlh_fc_prot_err 51 rmlh_rcvd_err 52 int_xadm_fc_prot_err 53 radm_unexp_cpl_err 54 radm_rcvd_cpl_ur 55 radm_rcvd_cpl_ca 56 radm_rcvd_req_ca 57 radm_rcvd_req_ur 58 radm_ecrc_err 59 radm_mlf_tlp_err 60 radm_rcvd_cpl_poisoned 61 radm_rcvd_wreq_poisoned 62 cfg_sys_err_rc_cor 63 cfg_sys_err_rc_nf 64 cfg_sys_err_rc_f</p> <p>*_DEBUG_INFO_SEL=6: 0 cdm_lbc_ack [4:1]lbc_cdm_wr[3:0] 5 lbc_cdm_cs</p>

Port	Direction	Bit width	Function Description
			[37:6] lbc_cdm_data[31:0] [69:38] lbc_cdm_addr[31:0] *_debug_info_sel=7 0 smlh_idle_inferred_in_l0: Level: Detect EI Infer 1 rmlh_rcvd_err: Pulse: Receiver Error 2 smlh_rx_rcvry_req: Level: Rx Recovery Request 3 smlh_timeout_nfts: Level: FTS Timeout 4 rmlh_framing_err: Pulse: Framing Error 5 rmlh_deskew_alignment_err: Level: Deskew Error 6 rdlh_bad_tlp_err_perltlp : Pulse: BAD TLP 7 rdlh_lcrc_tlp_err_perltlp : Pulse: LCRC Error 8 rdlh_bad_dllp_err_perdllp: Pulse: BAD DLLP 9 xdlh_replay_num_rlover_err: Pulse: Replay Num Rollover 10 xdlh_replay_timeout_err: Pulse: Replay Timeout 11 rdlh_rcvd_nack_perdllp: Pulse: Rx Nak DLLP 12 xdlh_nak_sent: Pulse: Tx Nak DLLP 13 xdlh_retry_req: Pulse: Retry TLP 14 rtlh_req_link_retrain: Level: FC Timeout [16:15] cfg_poisned_tlp: Pulse: Poisoned TLP [18:17] cfg_ecrc_tlp_err: Pulse: ECRC Error [20:19] cfg_ur_tlp: Pulse: Unsupported Request [22:21] cfg_ca_tlp: Pulse: Completer Abort [24:23] cfg_cpl_timeout[1:0]: Pulse: Completion Timeout 25 smlh_l0_to_recovery: Pulse: L0 to Recovery Entry 26 smlh_l1_to_recovery: Pulse: L1 to Recovery Entry 27 smlh_in_l0s: Level: Tx L0s Entry 28 smlh_in_rl0s: Level: Rx L0s Entry 29 pm_asnak: Level: ASPM L1 reject 30 smlh_in_l1: Level: L1 Entry 31 pm_in_l11: Level: L1.1 Entry 32 pm_in_l12: Level: L1.2 Entry 33 pm_in_l1_short: Level: L1 short duration 34 pm_in_l1_cpm: Level: L1 Clock PM (L1 with REFCLK removal/PLL Off) 35 pm_in_l1_abort: Level: L1.2 abort 36 smlh_in_l23: Level: L2 Entry 37 smlh_spd_change: Pulse: Speed Change 38 smlh_lwd_change: Pulse: Link width Change 39 xdlh_ack_sent: Pulse: Tx Ack DLLP 40 xdlh_update_fc_sent: Pulse: Tx Update FC DLLP 41 rdlh_rcvd_ack_perdllp: Pulse: Rx Ack DLLP 42 rtlh_rcvd_ufc_perdllp: Pulse: Rx Update FC DLLP 43 rdlh_nulified_tlp_err_perltlp : Pulse: Rx Nullified TLP 44 xtlh_xadm_restore_enable: Pulse: Tx

Port	Direction	Bit width	Function Description
			Nullified TLP 45 rdlh_duplicate_tlp_err_perltp: Pulse: Rx Duplicate TLP 46 xtlh_tx_memwr_evt: Pulse: Tx Memory Write 47 xtlh_tx_memrd_evt: Pulse: Tx Memory Read 48 xtlh_tx_cfgwr_evt: Pulse: Tx Config Write 49 xtlh_tx_cfgrd_evt: Pulse: Tx Config Read 50 xtlh_tx_iowr_evt: Pulse: Tx IO Write 51 xtlh_tx_iord_evt: Pulse: Tx IO Read 52 xtlh_tx_cplwod_evt: Pulse: Tx Completion w/o data 53 xtlh_tx_cplwd_evt: Pulse: Tx Completion w data 54 xtlh_tx_msg_evt: Pulse: Tx Message 55 xtlh_tx_atmcop_evt: Pulse: Tx AtomicOp 56 xtlh_tx_tlpwprefix_evt: Pulse: Tx TLP with Prefix 57 rtlh_rx_memwr_evt: Pulse: Rx Memory Write 58 rtlh_rx_memrd_evt: Pulse: Rx Memory Read 59 rtlh_rx_cfgwr_evt: Pulse: Rx Config Write 60 rtlh_rx_cfgrd_evt: Pulse: Rx Config Read 61 rtlh_rx_iowr_evt: Pulse: Rx IO Write 62 rtlh_rx_iord_evt: Pulse: Rx IO Read 63 rtlh_rx_cplwod_evt: Pulse: Rx Completion w/o data 64 rtlh_rx_cplwd_evt: Pulse: Rx Completion w data 65 rtlh_rx_msg_evt: Pulse: Rx Message TLP 66 rtlh_rx_atmcop_evt: Pulse: Rx Atomic 67 rtlh_rx_tlpwprefix_evt: Pulse: Rx TLP with Prefix 68 xtlh_tx_ccix_tlp_evt: Pulse: Tx CCIX TLP 69 rtlh_rx_ccix_tlp_evt: Pulse: Rx CCIX TLP 82:70 cdm_ras_des_ec_info_10[12:0] 95:83 cdm_ras_des_ec_info_11[12:0] 108:96 cdm_ras_des_ec_info_12[12:0] 121:109 cdm_ras_des_ec_info_13[12:0] 128:122 cdm_ras_des_tba_info_common[6:0] *_debug_info_sel=8 [4:0]pm_master_state[4:0]: Level: PM Internal State (Master) [8:5]pm_slave_state[3:0]: Level: PM Internal State (Slave) [15:9] rmlh_framing_err_ptr[6:0]: Pulse: 1st Framing Error Pointer [16] smlh_lane_reversed: Level: Lane Reversal Operation [17] pm_pme_resend_flag: Pulse: PME Re-Send flag [33:18] smlh_ltssm_variable [15:0]: Level: LTSSM Variable [36:34] ltssm_powerdown[1:0]: Level: PIPE: Power Down [44:37] latched_ts_nfts[7:0]: Level: Latched

Port	Direction	Bit width	Function Description
			NFTS [46:45] rdlh_dlcntrl_state [1:0]: Level: DLCM [47] rdlh_vc0_initfc1_status: Level: Init-FC Flag1 VC0 [48] rdlh_vc0_initfc2_status: Level: Init-FC Flag2 VC0 [60:49] rdlh_curnt_rx_ack_seqnum[11:0]: Level: Rx ACK SEQ# [72:61] xdlh_curnt_seqnum [11:0]: Level: Tx TLP SEQ# 85:73 cdm_ras_des_sd_info_l0[12:0] 98:86 cdm_ras_des_sd_info_l1[12:0] 111:99 cdm_ras_des_sd_info_l2[12:0] 124:112 cdm_ras_des_sd_info_l3[12:0]
			*_debug_info_sel=9 119:0 cdm_ras_des_sd_info_v0[239:120]
			*_debug_info_sel=10 119:0 cdm_ras_des_sd_info_v0[119:0]
CFG_IDO_REQ_EN	O	1	ID-Based Ordering Requests Enabled
CFG_IDO_CPL_EN	O	1	ID-Based Ordering Completions Enabled
XADM_PH_CDTs[7:0]	O	8	The amount of posted header buffer space currently available at the receiver at the other end of the link
XADM_PD_CDTs[11:0]	O	12	The amount of posted data buffer space currently available at the receiver at the other end of the link
XADM_NPH_CDTs[7:0]	O	8	The amount of non-posted header buffer space currently available at the receiver at the other end of the link
XADM_NPD_CDTs[11:0]	O	12	The amount of non-posted data buffer space currently available at the receiver at the other end of the link
XADM_CPLH_CDTs[7:0]	O	8	The amount of completion header buffer space currently available at the receiver at the other end of the link
XADM_CPLD_CDTs[11:0]	O	12	The amount of completion data buffer space currently available at the receiver at the other end of the link
MAC_PHY_POWERDOWN	O	2	Power control bits to the PHY 00: P0 (L0): normal 01: P0s (L0s): low recovery time, power saving. 10: P1 (L1): longer recovery time, additional power saving. 11: P2 (L2): lowest power state.
PHY_MAC_RXELECIDLE	I	4	Indicates receiver detection of an Electrical Idle for each lane
PHY_MAC_PHYSTATUS	I	4	Communicates completion of PHY functions, including power management transitions, receiver detection, speed change.
PHY_MAC_RXDATA	I	128	Parallel received data, 32 bits per lane
PHY_MAC_RXDATAK	I	16	Control (K character) indicator bits for received data
PHY_MAC_RXVALID	I	4	Indicates symbol lock and valid data for each lane

Port	Direction	Bit width	Function Description
PHY_MAC_RXSTATUS	I	12	Receive status and error codes for each lane(3bits per lane)
MAC_PHY_TXDATA	O	128	Parallel data for transmission
MAC_PHY_TXDATAK	O	16	Control (K character) indicator bits for transmitted data:
MAC_PHY_TXDETECTRX_LOOPBACK	O	4	Combined loopback and transmit detect control, as per PIPE specification.
MAC_PHY_TXELECIDLE_H	O	4	Forces transmit output to Electrical Idle for each lane which it is asserted.
MAC_PHY_TXELECIDLE_L	O	4	
MAC_PHY_TXCOMPLIANCE	O	4	Sets the running disparity to negative
MAC_PHY_RXPOLARITY	O	4	Directs the PHY to perform a polarity inversion the received data the specified lanes
MAC_PHY_RATE	O	1	Controls the link signaling rate
MAC_PHY_TXDEEMPH	O	2	For Gen2 configurations, this two bits wide output selects transmitter de-emphasis as follows
MAC_PHY_TXMARGIN	O	3	Selects transmitter voltage levels
MAC_PHY_TXSWING	O	1	Controls the PHY transmitter voltage swing level
CFG_HW_AUTO_SP_DIS	O	1	Autonomous speed disable.
RAM_TEST_EN	I	1	external_ram test enable signal (active high)
RAM_TEST_ADDRH	I	1	Test pattern: 1: test addr at the high data bit 0: test addr at the low data bit
RETRY_TEST_DATA_EN	I	1	Test mode (used only in single-port ram): 1: Test data line 0: Test control line
P_DATAQ_DATAOUT	I	66	Data buffer data output
P_DATAQ_ADDRA	O	10	Data buffer port A address
P_DATAQ_ADDRB	O	10	Data buffer port B address
P_DATAQ_DATAIN	O	66	Data buffer data input
P_DATAQ_ENA	O	1	Data buffer port A enable
P_DATAQ_ENB	O	1	Data buffer port B enable
P_DATAQ_WEA	O	1	Data buffer port A write enable
RETRYRAM_XDLH_DATA	I	68	retry buffer data output
XDLH_RETRYRAM_ADDR	O	10	retry buffer address
XDLH_RETRYRAM_DATA	O	68	retry buffer data input
XDLH_RETRYRAM_WE	O	1	retry buffer write enable
XDLH_RETRYRAM_EN	O	1	retry buffer enable
P_HDRQ_DATAOUT	I	138	Hdr buffer data output
P_HDRQ_ADDRA	O	9	Hdr buffer port A address
P_HDRQ_ADDRB	O	9	Hdr buffer port B address
P_HDRQ_DATAIN	O	138	Hdr buffer data input
P_HDRQ_ENA	O	1	Hdr buffer port A enable
P_HDRQ_ENB	O	1	Hdr buffer port B enable

Port	Direction	Bit width	Function Description
P_HDRQ_WEA	O	1	Hdr buffer port A write enable
RAM_TEST_MODE_N	I	1	ram_test_mode_n for opening ram test mode Active low
The above are the names and functional descriptions of all ports under operating mode. If in DFT test mode, the following three ports will be added			
TEST_SE_N	I	1	Test shift enable, active low
TEST_RST_N	I	1	Test reset, active low
TEST_MODE_N	I	1	Active low to enable test mode

10.5.4 Parameter Description

Table 10-13 GTP_PCIEGEN2 Parameter List

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
GRS_EN	<string>	"FALSE","TRUE"	TRUE	Bypass global rst
PIN_MUX_INT_FORCE_EN	<string>	"FALSE","TRUE"	FALSE	When setting "TRUE", it uses "PIN_MUX_INT_DISABLE" to judge whether "legacy int" should be disable .
PIN_MUX_INT_DISABLE	<string>	"FALSE","TRUE"	FALSE	Replace internal signal: "cfg_int_disable" when setting this signal and "PIN_MUX_INT_FORCE_EN" are "TRUE".
DIAG_CTRL_BUS_B2	<string>	"NORMAL", "FAST_LINK_MODE"	NORMAL	Select fast Link Mode for simulation when it is "FAST_LINK_MODE "
DYN_DEBUG_SEL_EN	<string>	"FALSE","TRUE"	FALSE	FALSE: "DEBUG_INFO_SEL" controls "debug_info_mux" TRUE: "DYN_DEBUG_INFO_SEL" controls "debug_info_mux"
DEBUG_INFO_SEL	<integer>	0 to 15	0	Control "DEBUG_DEBUG_INFO_MUX"
BAR_RESIZABLE	<integer>	" 0 to 56" Note: Please do not set more than 3 resizable bars at the same time	21 Note: 6'b010101 in binary	High active indicates that the corresponding bar is set to resizable. Note: the bar must be enabled; with a corresponding BAR_INDEX_0/1/2 indication and the maximum number of simultaneously valid bits is three.
NUM_OF_RBARS	<integer>	"0", "1", "2", "3"	3	Number of Resizable Bars in Resizable Bar Control Register
BAR_INDEX_0	<integer>	"0 to 5"	0	Correspond to the bar index in the Resizable BAR Control Register (at offset 008h)
BAR_INDEX_1	<integer>	"0 to 5"	2	Correspond to the bar index

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
				in the Resizable BAR Control Register (at offset 010h)
BAR_INDEX_2	<integer>	"0 to 5"	4	Correspond to the bar index in the Resizable BAR Control Register (at offset 018h)
TPH_DISABLE	<string>	"FALSE","TRUE"	FALSE	Bypass "TLP Processing Hints Supported"
MSIX_CAP_DISABLE	<string>	"FALSE","TRUE"	FALSE	Bypass "MSIX Capability"
MSI_CAP_DISABLE	<string>	"FALSE","TRUE"	FALSE	Bypass "MSI Capability"
MSI_PVM_DISABLE	<string>	"FALSE","TRUE"	FALSE	Bypass "Per vtor Masking Capable"
BAR_MASK_WRITABLE	<integer>	"0 to 63"	32	Active high indicates that the corresponding bar_mask value is writable
APP_DEV_NUM	<integer>	"0 to 31"	0	Device number. Your application must drive this signal to set the device number in the Requester ID for RC mode.
APP_BUS_NUM	<integer>	"0 to 255"	0	Bus number. Your application must drive this signal to set the bus number in the Requester ID for RC mode.
RAM_MUX_EN	<string>	"FALSE","TRUE"	FALSE	Enable merging of rcv hdr ram and rcv data ram outputs
ATOMIC_DISABLE	<string>	"FALSE","TRUE"	FALSE	Used to configure whether to disable the ATOMIC (active high)

Note: The above parameters can be used to configure internal functional modules of PCIE and can be flexibly selected

10.5.5 Instantiation Template

```
GTP_PCIEGEN2 #(
    .GRS_EN("TRUE"),
    .PIN_MUX_INT_FORCE_EN("FALSE"),
    .PIN_MUX_INT_DISABLE("FALSE"),
    .DIAG_CTRL_BUS_B2("NORMAL"),
    .DYN_DEBUG_SEL_EN("FALSE"),
    .DEBUG_INFO_SEL(0),
    .BAR_RESIZABLE(21),
    .NUM_OF_RBARS(3),
    .BAR_INDEX_0(0),
    .BAR_INDEX_1(2),
    .BAR_INDEX_2(4),
    .TPH_DISABLE("FALSE"),
)
```

```

.MSIX_CAP_DISABLE("FALSE"),
.MSI_CAP_DISABLE("FALSE"),
.MSI_PVM_DISABLE("FALSE"),
.BAR_MASK_WRITABLE(32),
.APP_DEV_NUM(0),
.APP_BUS_NUM(0),
.RAM_MUX_EN("FALSE"),
.ATOMIC_DISABLE("FALSE")

) GTP_PCIEGEN2_inst (
    .AXIS_MASTER_TDATA(),           // OUTPUT[127:0]
    .AXIS_MASTER_TKEEP(),          // OUTPUT[3:0]
    .AXIS_MASTER_TUSER(),          // OUTPUT[7:0]
    .CFG_MAX_PAYLOAD_SIZE(),       // OUTPUT[2:0]
    .CFG_MAX_RD_REQ_SIZE(),        // OUTPUT[2:0]
    .CFG_PBUS_DEV_NUM(),          // OUTPUT[4:0]
    .CFG_PBUS_NUM(),              // OUTPUT[7:0]
    .CFG_PF_TPH_ST_MODE(),        // OUTPUT[2:0]
    .CFG_TPH_REQ_EN(),            // OUTPUT[1:0]
    .DEBUG_INFO_MUX(),            // OUTPUT[132:0]
    .LBC_DBI_DOUT(),              // OUTPUT[31:0]
    .MAC_PHY_POWERDOWN(),         // OUTPUT[1:0]
    .MAC_PHY_RXPOLARITY(),        // OUTPUT[3:0]
    .MAC_PHY_TXCOMPLIANCE(),      // OUTPUT[3:0]
    .MAC_PHY_TXDATA(),            // OUTPUT[127:0]
    .MAC_PHY_TXDATAK(),           // OUTPUT[15:0]
    .MAC_PHY_TXDEEMPH(),          // OUTPUT[1:0]
    .MAC_PHY_TXDETECTRX_LOOPBACK(), // OUTPUT[3:0]
    .MAC_PHY_TXELECIDLE_H(),      // OUTPUT[3:0]
    .MAC_PHY_TXELECIDLE_L(),      // OUTPUT[3:0]
    .MAC_PHY_TXMARGIN(),          // OUTPUT[2:0]
    .PM_DSTATE(),                 // OUTPUT[2:0]
    .PM_MASTER_STATE(),           // OUTPUT[4:0]
    .PM_SLAVE_STATE(),            // OUTPUT[4:0]
    .P_DATAQ_ADDRA(),             // OUTPUT[9:0]

```

```

.P_DATAQ_ADDRB(),           // OUTPUT[9:0]
.P_DATAQ_DATAIN(),          // OUTPUT[65:0]
.P_HDRQ_ADDRA(),            // OUTPUT[8:0]
.P_HDRQ_ADDRB(),            // OUTPUT[8:0]
.P_HDRQ_DATAIN(),           // OUTPUT[137:0]
.RADM_GRANT_TLP_TYPE(),     // OUTPUT[5:0]
.RADM_TIMEOUT_CPL_ATTR(),   // OUTPUT[1:0]
.RADM_TIMEOUT_CPL_LEN(),    // OUTPUT[10:0]
.RADM_TIMEOUT_CPL_TAG(),    // OUTPUT[7:0]
.RADM_TIMEOUT_CPL_TC(),     // OUTPUT[2:0]
.SMLH_LTSSM_STATE(),        // OUTPUT[4:0]
.XADM_CPLD_CDT(),           // OUTPUT[11:0]
.XADM_CPLH_CDT(),           // OUTPUT[7:0]
.XADM_NPD_CDT(),             // OUTPUT[11:0]
.XADM_NPH_CDT(),             // OUTPUT[7:0]
.XADM_PD_CDT(),              // OUTPUT[11:0]
.XADM_PH_CDT(),              // OUTPUT[7:0]
.XDLH_RETRYRAM_ADDR(),      // OUTPUT[10:0]
.XDLH_RETRYRAM_DATA(),       // OUTPUT[67:0]
.APP_ERR_BUS(),               // INPUT[12:0]
.APP_HDR_LOG(),               // INPUT[127:0]
.APP_RAS DES_TBA_CTRL(),     // INPUT[1:0]
.AXIS_SLAVE0_TDATA(),         // INPUT[127:0]
.AXIS_SLAVE1_TDATA(),         // INPUT[127:0]
.AXIS_SLAVE2_TDATA(),         // INPUT[127:0]
.CFG_MSI_PENDING(),           // INPUT[31:0]
.DBI_ADDR(),                  // INPUT[31:0]
.DBI_DIN(),                   // INPUT[31:0]
.DBI_WR(),                     // INPUT[3:0]
.DEVICE_TYPE(),                // INPUT[2:0]
.DIAG_CTRL_BUS(),              // INPUT[1:0]
.DYN_DEBUG_INFO_SEL(),         // INPUT[3:0]
.MSIX_ADDR(),                  // INPUT[63:0]
.MSIX_DATA(),                  // INPUT[31:0]

```

```

.PHY_MAC_PHYSTATUS(),           // INPUT[3:0]
.PHY_MAC_RXDATA(),             // INPUT[127:0]
.PHY_MAC_RXDATAK(),            // INPUT[15:0]
.PHY_MAC_RXELECIDLE(),          // INPUT[3:0]
.PHY_MAC_RXSTATUS(),            // INPUT[11:0]
.PHY_MAC_RXVALID(),             // INPUT[3:0]
.P_DATAQ_DATAOUT(),             // INPUT[65:0]
.P_HDRQ_DATAOUT(),              // INPUT[137:0]
.RETRYRAM_XDLH_DATA(),          // INPUT[67:0]
.TRGT1_RADM_PKT_HALT(),         // INPUT[2:0]
.VEN_MSI_TC(),                  // INPUT[2:0]
.VEN_MSI_VECTOR(),               // INPUT[4:0]
.AUX_PM_EN(),                   // OUTPUT
.AXIS_MASTER_TLAST(),            // OUTPUT
.AXIS_MASTER_TVALID(),            // OUTPUT
.AXIS_SLAVE0_TREADY(),           // OUTPUT
.AXIS_SLAVE1_TREADY(),           // OUTPUT
.AXIS_SLAVE2_TREADY(),           // OUTPUT
.CFG_AER_RC_ERR_MUX(),           // OUTPUT
.CFG_ATOMIC_EGRESS_BLOCK(),       // OUTPUT
.CFG_ATOMIC_REQ_EN(),             // OUTPUT
.CFG_BUS_MASTER_EN(),             // OUTPUT
.CFG_BW_MGT_MUX(),               // OUTPUT
.CFG_CRS_SW_VIS_EN(),             // OUTPUT
.CFG_EXT_TAG_EN(),                // OUTPUT
.CFG_HW_AUTO_SP_DIS(),             // OUTPUT
.CFG_IDO_CPL_EN(),                // OUTPUT
.CFG_IDO_REQ_EN(),                 // OUTPUT
.CFG_INT_DISABLE(),                // OUTPUT
.CFG_LINK_AUTO_BW_MUX(),           // OUTPUT
.CFG_MEM_SPACE_EN(),                // OUTPUT
.CFG_MSIX_EN(),                   // OUTPUT
.CFG_MSIX_FUNC_MASK(),              // OUTPUT
.CFG_MSI_EN(),                   // OUTPUT

```

```

.CFG_NO_SNOOP_EN(),           // OUTPUT
.CFG_PME_MUX(),              // OUTPUT
.CFG_PM_NO_SOFT_RST(),        // OUTPUT
.CFG_RCB(),                  // OUTPUT
.CFG_RELAX_ORDER_EN(),        // OUTPUT
.CFG_SEND_COR_ERR_MUX(),      // OUTPUT
.CFG_SEND_F_ERR_MUX(),        // OUTPUT
.CFG_SEND_NF_ERR_MUX(),       // OUTPUT
.CFG_SYS_ERR_RC(),            // OUTPUT
.CORE_RST_N(),                // OUTPUT
.INTA_GRT_MUX(),              // OUTPUT
.INTB_GRT_MUX(),              // OUTPUT
.INTC_GRT_MUX(),              // OUTPUT
.INTD_GRT_MUX(),              // OUTPUT
.LBC_DBI_ACK(),               // OUTPUT
.MAC_PHY_RATE(),              // OUTPUT
.MAC_PHY_TXSWING(),           // OUTPUT
.PHY_RST_N(),                 // OUTPUT
.PM_LINKST_IN_L0S(),           // OUTPUT
.PM_LINKST_IN_L1(),             // OUTPUT
.PM_LINKST_IN_L2(),             // OUTPUT
.PM_LINKST_L2_EXIT(),          // OUTPUT
.PM_PME_EN(),                  // OUTPUT
.PM_STATUS(),                  // OUTPUT
.PM_XTLH_BLOCK_TLP(),          // OUTPUT
.P_DATAQ_ENA(),                // OUTPUT
.P_DATAQ_ENB(),                // OUTPUT
.P_DATAQ_WEA(),                // OUTPUT
.P_HDRQ_ENA(),                  // OUTPUT
.P_HDRQ_ENB(),                  // OUTPUT
.P_HDRQ_WEA(),                  // OUTPUT
.RADM_CPL_TIMEOUT(),            // OUTPUT
.RADM_IDLE(),                  // OUTPUT
.RADM_MSG_UNLOCK(),             // OUTPUT

```

```

.RADM_PM_PME(),           // OUTPUT
.RADM_PM_TO_ACK(),        // OUTPUT
.RADM_PM_TURNOFF(),       // OUTPUT
.RADM_QOVERFLOW(),         // OUTPUT
.RADM_Q_NOT_EMPTY(),       // OUTPUT
.RBAR_CTRL_UPDATE(),       // OUTPUT
.RDLH_LINK_UP(),          // OUTPUT
.SEDO(),                  // OUTPUT
.SEDO_EN(),                // OUTPUT
.SMLH_LINK_UP(),          // OUTPUT
.TRAINING_RST_N(),         // OUTPUT
.VEN_MSI_GRANT(),          // OUTPUT
.WAKE(),                  // OUTPUT
.XDLH_RETRYRAM_EN(),       // OUTPUT
.XDLH_RETRYRAM_WE(),       // OUTPUT
.APPS_PM_XMT_PME(),        // INPUT
.APPS_PM_XMT_TURNOFF(),    // INPUT
.APP_CLK_PM_EN(),          // INPUT
.APP_DBI_RO_WR_DISABLE(),   // INPUT
.APP_ERR_ADVISORY(),        // INPUT
.APP_HDR_VALID(),          // INPUT
.APP_INIT_RST(),            // INPUT
.APP_LTSSM_EN(),            // INPUT
.APP_RAS DES_SD_HOLD_LTSSM(), // INPUT
.APP_READY_ENTR_L23(),       // INPUT
.APP_REQ_ENTR_L1(),          // INPUT
.APP_REQ_EXIT_L1(),          // INPUT
.APP_REQ_RETRY_EN(),         // INPUT
.APP_UNLOCK_MSG(),           // INPUT
.APP_XFER_PENDING(),         // INPUT
.AXIS_MASTER_TREADY(),       // INPUT
.AXIS_SLAVE0_TLAST(),         // INPUT
.AXIS_SLAVE0_TUSER(),         // INPUT
.AXIS_SLAVE0_TVALID(),        // INPUT

```

```

.AXIS_SLAVE1_TLAST(),           // INPUT
.AXIS_SLAVE1_TUSER(),           // INPUT
.AXIS_SLAVE1_TVALID(),          // INPUT
.AXIS_SLAVE2_TLAST(),           // INPUT
.AXIS_SLAVE2_TUSER(),           // INPUT
.AXIS_SLAVE2_TVALID(),          // INPUT
.BUTTON_RST(),                  // INPUT
.DBI_CS(),                      // INPUT
.DBI_CS2(),                     // INPUT
.MEM_CLK(),                     // INPUT
.OUTBAND_PWRUP_CMD(),          // INPUT
.PCLK(),                        // INPUT
.PCLK_DIV2(),                   // INPUT
.PERST(),                       // INPUT
.POWER_UP_RST(),                // INPUT
.RAM_TEST_ADDRH(),              // INPUT
.RAM_TEST_EN(),                 // INPUT
.RAM_TEST_MODE_N(),              // INPUT
.RETRY_TEST_DATA_EN(),           // INPUT
.RX_LANE_FLIP_EN(),              // INPUT
.SEDI(),                         // INPUT
.SEDI_ACK(),                     // INPUT
.SYS_AUX_PWR_DET(),              // INPUT
.SYS_INT(),                      // INPUT
.TX_LANE_FLIP_EN(),              // INPUT
.VEN_MSI_REQ()                  // INPUT
);


```

10.6 GTP_HSSTLP_LANE

10.6.1 Supported Devices

Table 10-14 GTP_HSSTLP_LANE-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

10.6.2 Description of Functionality

For detailed functionality and usage instructions, please refer to "***G040008_Logos2 Family FPGAs High-Speed Serial Transceiver (HSST) User Guide***".

10.6.3 Port Description

Table 10-15 GTP_HSSTLP_LANE Port List

Port	Direction	Data Width	Function Description
PMA_RCLK	O	1	recovery clk from PMA
P_CFG_READY	O	1	Read/write ready output for the dynamic configuration interface, active high
P_CFG_RDATA	O	8	Read data for the dynamic configuration interface
P_CFG_INT	O	1	Dynamic configuration interface interrupt output, active high
P_RCLK2FABRIC	O	1	rclk to CORE
P_TCLK2FABRIC	O	1	tclk to CORE
P_RX_SIGDET_STATUS	O	1	rx signal detect
P_RX_SATA_COMINIT	O	1	sata related protocol signals
P_RX_SATA_COMWAKE	O	1	sata related protocol signals
P_RX_LS_DATA	O	1	rx output low speed data
P_RX_READY	O	1	rx ready signal
P_TEST_STATUS	O	20	rx output test status register
P_TX_RXDET_STATUS	O	1	tx_rxdet output state signal
P_CA_ALIGN_RX	O	1	Receiving Channel CLK Aligner dynamic state output, a 0-to-1 transition indicates aligner success, an asynchronous signal
P_CA_ALIGN_TX	O	1	Transmitting ChannelAligner dynamic state output, a 0-to-1 transition indicates aligner success, an asynchronous signal
P_PCS_LSM_SYNCED	O	1	Word Alignment successful, state machine lock flag, active high, an asynchronous signal.
P_PCS_RX_MCB_STATUS	O	1	channel bonding state,1:all channel has been bonded together.
P_RDATA	O	47	receive data to channel
P_TX_SDN	O	1	tx output pin n
P_TX_SDP	O	1	tx output pin p
TXPCLK_PLL	O	1	Output parallel clock
LANE_COUT_BUS_FORWARD	O	19	Transmission direction is COUT port bus of LANE0->LANE1->LANE2->LANE3, see each bit in Table 10-16
APATTERN_STATUS_COUT	O	1	slave find A, for next channel, transmission direction is LANE3->LANE2->LANE1->LANE0
SYNC	I	1	Output SYNC_PLL derived from PLL
RATE_CHANGE	I	1	Output RATE_CHANGE_PLL derived from PLL

Port	Direction	Data Width	Function Description
PLL_RESET_I	I	1	Output PLL_RST_O derived from PLL
PLL_LOCK_SEL	I	1	Output PMA_PLL_READY_O derived from PLL
P_RX_CLK_FR_CORE	I	1	rclk of channel, from CORE
P_RCLK2_FR_CORE	I	1	From CORE, generated by refck2core through PLL frequency multiplication
P_TX_CLK_FR_CORE	I	1	tclk of channel, from CORE
P_TCLK2_FR_CORE	I	1	From CORE, generated by refck2core through PLL frequency multiplication
P_PCS_TX_RST	I	1	Reset signal from CIM, per channel, inverted pcs_tx_rst signal from PCS port;
P_PCS_RX_RST	I	1	Reset signal from CIM, per channel, inverted pcs_rx_rst signal from PCS port;
P_PCS_CB_RST	I	1	Reset signal from CIM, per channel
P_RXGEAR_SLIP	I	1	slip indication to rx gear box with 64b66b/67b decoder mode
P_CFG_CLK	I	1	Dynamically configure the clock input of the interface
P_CFG_RST	I	1	Dynamic configuration interface reset signal, active low. All registers revert to the initial values set by the Parameter after reset
P_CFG_PSEL	I	1	cfg select to lane, from CORE
P_CFG_ENABLE	I	1	Dynamic configuration interface access enable, active high
P_CFG_WRITE	I	1	Dynamic configuration interface read and write select signal, high indicates write, low indicates read
P_CFG_ADDR	I	12	Dynamic configuration interface write address
P_CFG_WDATA	I	8	Dynamic configuration interface write data
P_TDATA	I	46	Transmit data
P_RX_POLARITY_INVERT	I	1	RX Sample Reg's polarity inversion enable, an asynchronous signal, active high, one per channel: P_RX_POLARITY_INVERT[0]: For Channel 0 P_RX_POLARITY_INVERT[1]: For Channel 1 P_RX_POLARITY_INVERT[2]: For Channel 2 P_RX_POLARITY_INVERT[3]: For Channel 3
P_CEB_ADETECT_EN	I	1	Test signal, set externally to 4'b1111' in normal mode
P_PCS_MCB_EXT_EN	I	1	Channel bonding enable under external state machine mode, an asynchronous signal, active-high
P_PCS_NEAREND_LOOP	I	1	pcs near end loopback ctrl signals Note: When enabled, the internal clock selection register will be configured accordingly;
P_PCS_FAREND_LOOP	I	1	pcs far end loopback ctrl signals Note: When enabled, the internal clock selection register configuration is required;
P_PMA_NEAREND_PLOOP	I	1	Related to pma_rx_reg_i[96] tx2rx paralleled loopback enable register 0: tx2rx paralleled loopback is off 1: tx2rx paralleled loopback is on
P_PMA_NEAREND_SLOOP	I	1	Related to pma_tx_reg_i[163]; Tx to rx serial loopback enable

Port	Direction	Data Width	Function Description
			0: serial loopback disabled 1: serial loopback enabled
P_PMA_FAREND_PLOOP	I	1	Related to pma_tx_reg_i[198:197]; parallel data mux select to select different data source 0: data from pcs 1: rx loopback data
P_LANE_PD	I	1	power down lane
P_LANE_RST	I	1	reset lane, high active
P_RX_LANE_PD	I	1	rx lane powerdown from core
P_RX_PMA_RST	I	1	Reset PMA Receiver, an asynchronous signal
P_CTLE_AD_P_RST	I	1	reset pin
P_TX_DEEMP	I	2	transmitter de-emphasis
P_TX_LS_DATA	I	1	tx low speed signal input
P_TX_BEACON_EN	I	1	TX beacon enable signal; 1'b0: Disable beacon; 1'b1: Enable beacon.
P_TX_SWING	I	1	tx_swing control signal
P_TX_RXDET_REQ	I	1	tx_rxdet_req signal
P_TX_RATE	I	3	TX rate control signal; 2'b00: datarate is 2 times of PLL clock frequency; 2'b01: datarate is the same of PLL clock frequency; 2'b10: datarate is 1/2 of PLL clock frequency; 2'b11: datarate is 1/4 of PLL clock frequency. bit[2] is reserved
P_TX_BUSWIDTH	I	3	TX buswidth control; 3'bX00: 8bit; 3'bX01:10bit; 3'bX10:16bit; 3'bX11:20bit; bit[2] is reserved.
P_TX_MARGIN	I	3	for pcie mode select transmitter voltage level ,from core
P_TX_PMA_RST	I	1	tx moclue reset, high active
P_TX_LANE_PD_CLKPATH	I	1	Power down enable for TX clockpath 1'b0: TX clockpath is power on; 1'b1: TX clockpath is power off.
P_TX_LANE_PD_PISO	I	1	Power down enable for TX PISO; 1'b0: TX PISO is power on; 1'b1: TX PISO is power down.
P_TX_LANE_PD_DRIVER	I	1	Power down enable for TX driver; 1'b0: TX driver is power on; 1'b1: TX driver is power down.
P_RX_RATE	I	3	TX rate control signal; 2'b00: datarate is 1/4 times of PLL clock frequency; 2'b01: datarate 1/2 times of PLL clock frequency; 2'b10: datarate is the same of PLL clock frequency; 2'b11: datarate is 2 times of PLL clock frequency. bit[2] is reserved

Port	Direction	Data Width	Function Description
P_RX_BUSWIDTH	I	3	Rx buswidth control; 3'bX00: 8bit; 3'bX01:10bit; 3'bX10:16bit; 3'bX11:20bit; bit[2] is reserved.
P_RX_HIGHZ	I	1	receiver termination res high z control register 0: receiver in 50-ohm low-impedance mode; 1: receiver in highZ mode;
P_CIM_CLK_ALIGNER_RX	I	8	CLK Aligner delay step selection at receiver side, an asynchronous signal
P_CIM_CLK_ALIGNER_TX	I	8	CLK Aligner delay step selection at transmit side, an asynchronous signal
P_CIM_DYN_DLY_SEL_RX	I	1	Receive Channel's CLK Aligner enable, active high, an asynchronous signal.
P_CIM_DYN_DLY_SEL_TX	I	1	Transmit Channel's CLK Aligner enable, active high, an asynchronous signal.
P_CIM_START_ALIGN_RX	I	1	Input source for generating receive ChannelCLK Aligner pulse, an asynchronous signal
P_CIM_START_ALIGN_TX	I	1	Input source for generating transmit ChannelCLK Aligner pulse, an asynchronous signal
P_PCS_WORD_ALIGN_EN	I	1	align_en input
LANE_CIN_BUS_FORWARD	O	19	Transmission direction is COUT port bus of LANE0->LANE1->LANE2->LANE3, see each bit in Table 10-17
APATTERN_STATUS_CIN	I	1	A detected signal from slave channels to master channel, transmission direction is LANE3->LANE2->LANE1->LANE0
MCB_RCLK	I	1	pma_rclk from Master
CLK_RX0	I	1	Input clock phase 0, from PLL output
CLK_RX90	I	1	Input clock phase 90, from PLL output
CLK_RX180	I	1	Input clock phase 180, from PLL output
CLK_RX270	I	1	Input clock phase 270, from PLL output
CLK_TXN	I	1	tx clock signal sent to pcs inverted, from PLL output
CLK_TXP	I	1	The clock signal sent from tx to pcs, from the PLL output
PLL_PD_I	I	1	PLL powerdown control 0: PLL is not powered down (default) 1: PLL is powered down Originating from the PLL output PLL_PD_O
PLL_REFCLK_I	I	1	Originating from the PLL output PLL_REFCLK_LANE_L
P_RX_SDN	I	1	Input data
P_RX_SDP	I	1	Input data
PLL_RES_TRIM_I	I	6	Rx termination resistor calibration register 101110: 100 ohms, originating from the PLL0 output P_RESCAL_I_CODE_O

Table 10-16 Descriptions of Each Segment of the LANE_COUT_BUS_FORWARD Bus

Bit segment	Original corresponding signal	Description
[18]	RFIFO_EN_CB_COUT	Control the write enable and read enable of the fifo in the channel bonding unit/CTC unit/bridge unit
[17]	RFIFO_EN_AFTER_CTC_COUT	Control the write enable and read enable of the fifo in the channel bonding unit/CTC unit/bridge unit
[16]	RFIFO_EN_AFTER_CTC_GB_COUT	Control the write enable and read enable of the fifo in the channel bonding unit/CTC unit/bridge unit
[15]	RFIFO_EN_BRIDGE_COUT	Control the write enable and read enable of the fifo in the channel bonding unit/CTC unit/bridge unit
[14]	TFIFO_EN_PCS_TX_COUT	Control the write enable and read enable of the fifo in the bridge unit
[13]	TFIFO_EN_BRIDGE_COUT	Control the write enable and read enable of the fifo in the bridge unit
[12]	PCS_TCLK_EN_COUT	In Tx clk mode 1/2, it is usually 1
[11]	GEAR_TCLK_EN_COUT	gear_tclk_en output for 2-beat synchronous processing; when valid, tdata data is sampled with the rising edge of tclk2 to obtain internal sampling data tdata_s for data split processing
[10]	APATTERN_MATCH_LSB_COUT	master detect A at lsb,output for next channel
[9]	APATTERN_MATCH_MSB_COUT	master detect A at msb,output for next channel
[8]	APATTERN_SEACHING_PROC_COUT	data delay signal to other channel from master lsm.
[7]	CB_RCLK_EN_COUT	Configured to 1, it will output a valid clock enable signal for the corresponding clk, otherwise the corresponding clock enable signal will be all 1
[6]	AFTER_CTC_RCLK_EN_COUT	Configured to 1, it will output a valid clock enable signal for the corresponding clk, otherwise the corresponding clock enable signal will be all 1
[5]	AFTER_CTC_RCLK_EN_GB_COUT	Configured to 1, it will output a valid clock enable signal for the corresponding clk, otherwise the corresponding clock enable signal will be all 1
[4]	SKIP_ADD_MCB_COUT	skip add flag signal,output to next channel
[3]	SKIP_DEL_MCB_COUT	skip del flag signal, output to next channel
[2]	SKIP_DEL_LSB_MCB_COUT	skip reg place information, output to next channel
[1]	SKIP_ADD_LSB_MCB_COUT	skip reg place information, output to next channel
[0]	CTC_RD_FIFO_COUT	FIFO read enable,output to next channel

Table 10-17 Descriptions of Each Segment of the LANE_CIN_BUS_FORWARD Bus

Bit segment	Original corresponding signal	Description
[18]	RFIFO_EN_CB_CIN	Control the write enable and read enable of the fifo in the channel bonding unit/CTC unit/bridge unit
[17]	RFIFO_EN_AFTER_CTC_CIN	Control the write enable and read enable of the fifo in the channel bonding unit/CTC unit/bridge unit
[16]	RFIFO_EN_AFTER_CTC_GB_CIN	Control the write enable and read enable of the fifo in the channel bonding unit/CTC unit/bridge unit
[15]	RFIFO_EN_BRIDGE_CIN	Control the write enable and read enable of the fifo in the channel bonding unit/CTC unit/bridge unit
[14]	TFIFO_EN_PCS_TX_CIN	Control the write enable and read enable of the fifo in the bridge unit
[13]	TFIFO_EN_BRIDGE_CIN	Control the write enable and read enable of the fifo in the

Bit segment	Original corresponding signal	Description
		bridge unit
[12]	PCS_TCLK_EN_CIN	In Tx clk mode 1/2, it is usually 1
[11]	GEAR_TCLK_EN_CIN	When valid, tdata data is sampled with the rising edge of tclk2 to obtain internal sampling data tdata_s for data split processing
[10]	APATTERN_MATCH_LSB_CIN	master detect A at lsb
[9]	APATTERN_MATCH_MSB_CIN	master detect A at msb
[8]	APATTERN_SEACHING_PROC_CIN	align_en from master channel to slave channel
[7]	CB_RCLK_EN_CIN	Configured to 1, it will output a valid clock enable signal for the corresponding clk, otherwise the corresponding clock enable signal will be all 1
[6]	AFTER_CTC_RCLK_EN_CIN	Configured to 1, it will output a valid clock enable signal for the corresponding clk, otherwise the corresponding clock enable signal will be all 1
[5]	AFTER_CTC_RCLK_EN_GB_CIN	Configured to 1, it will output a valid clock enable signal for the corresponding clk, otherwise the corresponding clock enable signal will be all 1
[4]	SKIP_ADD_MCB_CIN	skip add flag signal, input from previous channel
[3]	SKIP_DEL_MCB_CIN	skip del flag signal, input from previous channel
[2]	SKIP_DEL_LSB_MCB_CIN	skip reg place information, input from previous channel
[1]	SKIP_ADD_LSB_MCB_CIN	skip reg place information, input from previous channel
[0]	CTC_RD_FIFO_CIN	FIFO read enable, input from previous channel

10.6.4 Paramater Description

Table 10-18 GTP_HSSTLP_LANE Parameter List

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
MUX_BIAS	<integer>	0 to 7	2	Used in the module pma_trxclk_mux_top, it affects the output amplitude of the selected output clock signal (simulation not supported)
PD_CLK	<integer>	0,1	0	Used in the module pma_trxclk_mux_top, it controls the powerdown of the selected output clock signal (simulation not supported)
REG_SYNC	<integer>	0,1	0	Used in the module pma_tx_sync, it controls the new variable reg_sync to be 0 or 1;
REG_SYNC_OW	<integer>	0,1	0	Used in the module pma_tx_sync, it controls the output value to the original port pma_lane_sync_i to be sync or reg_sync
PLL_LOCK_OW	<integer>	0,1	0	Used in the module pma_status_mux, it controls the new variable pll_lock_ow to be 1'b0 or 1'b1

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PLL_LOCK_OW_EN	<integer>	0,1	0	Used in the module pma_status_mux, it controls the output value to the original port pll_ready_i to be the selection parameter of pll_lock_mid and pll_lock_ow
PCS_SLAVE	<integer>	0,1	0	Channel bonding setting excluding PCI Express 0:master 1:slave
PCS_BYPASS_WORD_ALIGN	<string >	"FALSE","TRUE"	"FALSE"	Active-high Bypass module Word Alignment
PCS_BYPASS_DENC	<string >	"FALSE","TRUE"	"FALSE"	Active-high Bypass module 8b10b Decoder
PCS_BYPASS_BONDING	<string >	"FALSE","TRUE"	"FALSE"	Active-high Bypass module Channel Bonding
PCS_BYPASS_CTC	<string >	"FALSE","TRUE"	"FALSE"	Active-high Bypass module Channel Bonding
PCS_BYPASS_GEAR	<string >	"FALSE","TRUE"	"FALSE"	Active-high Bypass module Rx Gear
PCS_BYPASS_BRIDGE	<string >	"FALSE","TRUE"	"FALSE"	Active-high Bypass module Rx Bridge unit
PCS_BYPASS_BRIDGE_FIFO	<string >	"FALSE", "TRUE"	"FALSE"	Active-high Bypass module Rx Bridge FIFO
PCS_DATA_MODE	<string >	"X8","X10", "X16","X20"	"X8"	One of the data bit width selections for the PCS Receiver module "X8", "X10": Used for 8-bit only, 10-bit only, or 8b/10b 8-bit width modes; "X16", "X20": Used for bit width modes other than 8-bit only, 10-bit only, or 8b/10b 8-bit modes;
PCS_RX_POLARITY_INVERSION	<string >	"DELAY", "BIT_POLARITY_INVERSION"; "BIT_REVERSAL"; "BOTH"	"DELAY" "	Rx Sample Reg module polarity inversion and bit order inversion; "DELAY", no inversion "BIT_POLARITY_INVERSION", enable polarity inversion "BIT_inversion", enable bit order inversion "BOTH", enable both polarity inversion and bit order inversion
PCS_ALIGN_MODE	<string >	"1GB"; "10GB"; "RAPIDIO"; "OUTSIDE"	"1GB"	Word Alignment Link State Machine selection "1GB"; select Link State Machine based on Gig Ethernet "10GB"; select Link State Machine based on 10G Ethernet "RAPIDIO"; select Link State Machine based on RapidIO "OUTSIDE"; select External State Machine control
PCS_SAMP_16B	<string >	"X20"; "X16"	"X20"	One of the data bit width selections for the PCS Receiver module "X20"; used for bit width modes other than 8/16/32 bits only; "X16"; used for 8/16/32 bits only

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
				bit width modes;
PCS_FARLP_PWR_REDUCTION	<string >	"FALSE","TRUE"	"FALSE"	Rx far loop power reduction option "TRUE": power reduction "FALSE": normal
PCS_COMMA_REG0	<integer>	0 to 1023	0	Word Alignment Comma byte definition 0
PCS_COMMA_MASK	<integer>	0 to 1023	0	Word Alignment Comma Mask bit definition
PCS_CEB_MODE	<string >	"10GB"; "RAPIDIO"; "OUTSIDE"	"10GB"	Channel Bonding State Machine selection "10GB"; selects the Channel Bonding State Machine based on XAUI "RAPIDIO"; selects the Channel Bonding State Machine based on RapidIO "OUTSIDE"; select External State Machine control
PCS_CTC_MODE	<string >	"1SKIP"; "2SKIP"; "PCIE_2BYTE"; "4SKIP"	"1SKIP"	CTC mode selection "1SKIP"; the inserted/deleted SKIP character is 1 byte "2SKIP"; the inserted/deleted SKIP characters are 2 bytes "PCIE_2BYTE"; PCIe's 2-byte mode, only adds or deletes the subsequent skip "4SKIP"; PCIe's 4-byte mode, the SKIP bytes are 4 bytes, but only the last byte of the SKIP characters is inserted/deleted
PCS_A_REG	<integer>	0 to 255	0	Definition of Align Pattern used for Channel Bonding
PCS_GE_AUTO_EN	<string >	"FALSE","TRUE"	"FALSE"	Active-high, enable automatic replacement from /C/ to /I2/ based on 1 Gig Ethernet
PCS_SKIP_REG0	<integer>	0 to 1023	0	SKIP character Byte 0 used by CTC
PCS_SKIP_REG1	<integer>	0 to 1023	0	SKIP character Byte 1 used by CTC
PCS_SKIP_REG2	<integer>	0 to 1023	0	SKIP character Byte 2 used by CTC
PCS_SKIP_REG3	<integer>	0 to 1023	0	SKIP character Byte 3 used by CTC
PCS_DEC_DUAL	<string >	"FALSE","TRUE"	"FALSE"	One of the data bit width selections for the PCS Receiver module
PCS_SPLIT	<string >	"FALSE","TRUE"	"FALSE"	One of the data bit width selections for the PCS Receiver module "FALSE"; for bit width modes other than 8bit only, 10bit only, or 8B10B 8bit; "TRUE"; for 8bit only, 10bit only, or 8B10B 8bit bit width modes;
PCS_FIFOFLAG_CTC	<string >	"FALSE","TRUE"	"FALSE"	CTC priority encoding flag signal in rxstatus encoding, configured as 1 indicates high priority signal in CTC
PCS_COMMA_DET_M	<string >	"RX_CLK_SLIP";	"COMM"	Alignment mode selection in Word

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
ODE		"COMMA_PATTE RN"	A_PATT ERN"	Alignment module "COMMA_PATTERN"; select Comma Alignment mode "RX_CLK_SLIP"; select RX CLK Slip mode
PCS_ERRDETECT_SILENCE	<string >	"FALSE","TRUE"	"FALSE"	cfg_errdetect_silence=1, k code decoding error will be forcibly overridden without reporting an error. cfg_errdetect_silence=0, k code decoding error will report an error
PCS_PMA_RCLK_POLINV	<string >	"PMA_RCLK","REVERSE_OF_PMA_RCLK"	"PMA_RCLK"	"PMA_RCLK":pma_rclk "REVERSE_OF_PMA_RCLK":reverse of pma_rclk
PCS_PCS_RCLK_SEL	<string >	"PMA_RCLK", "PMA_TCLK", "RCLK"	"PMA_RCLK"	choose pcs_rclk "PMA_RCLK": pma_rclk; "PMA_TCLK": pma_tclk; "MCB_RCLK": rclk 2'b11: reserved
PCS_CB_RCLK_SEL	<string >	"PMA_RCLK", "PMA_TCLK", "MCB_RCLK"	"PMA_RCLK"	choose cb_rclk "PMA_RCLK":pma_rclk; "PMA_TCLK":pma_tclk; "MCB_RCLK":mcb_rclk 2'b11:reserved
PCS_AFTER_CTC_RCLK_SEL	<string >	"PMA_RCLK", "PMA_TCLK", "MCB_RCLK", "RCLK2"	"PMA_RCLK"	AFTER_CTC_RCLK clock source selection
PCS_RCLK_POLINV	<string >	"RCLK"; "REVERSE_OF_RCLK"	"RCLK"	RCLK clock source selection
PCS_BRIDGE_RCLK_SEL	<string >	"PMA_RCLK", "PMA_TCLK", "MCB_RCLK", "RCLK"	"PMA_RCLK"	choose bridge_rclk "PMA_RCLK":pma_rclk; "PMA_TCLK":pma_tclk; "MCB_RCLK":mcb_rclk "RCLK":rclk
PCS_PCS_RCLK_EN	<string >	"FALSE", "TRUE"	"FALSE"	One of the data bit width selections for the PCS Receiver module "FALSE"; for bit width modes other than 8bit only, 10bit only, or 8b10b 8bit; "TRUE"; for 8bit only, 10bit only, or 8b10b 8bit bit width modes;
PCS_CB_RCLK_EN	<string >	"FALSE", "TRUE"	"FALSE"	One of the data bit width selections for the PCS Receiver module "FALSE"; for bit width modes other than 8bit only, 10bit only, or 8b10b 8bit; "TRUE"; for 8bit only, 10bit only, or 8b10b 8bit bit width modes;
PCS_AFTER_CTC_RCLK_EN	<string >	"FALSE", "TRUE"	"FALSE"	One of the data bit width selections for the PCS Receiver module "FALSE"; for bit width modes other than 8bit only, 10bit only, or 8b10b 8bit;

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PCS_AFTER_CTC_RC_LK_EN_GB	<string >	"FALSE","TRUE"	"FALSE"	"TRUE"; for 8bit only, 10bit only, or 8b10b 8bit bit width modes; One of the data bit width selections for the PCS Receiver module "FALSE"; for bit width modes other than 32bit only, 40bit only, or 8b10b 32bit; "TRUE"; for 32bit only, 40bit only, or 8b10b 32bit bit width modes;
PCS_PCS_RX_RSTN	<string >	"FALSE","TRUE"	"FALSE"	Reset register for the PCS Receiver, i.e., cfg_pcs_rx_rstn, active low
PCS_PCIE_SLAVE	<string >	"MASTER","SLAVE"	"MASTER"	Channel bonding setting excluding PCI Express
PCS_RX_64B66B_67B	<string >	"NORMAL", "64B_66B", "64B_67B"	"NORMAL"	"NORMAL": without 64b_66b/67b; "64B_66B": 64b_66b; "64B_67B": 64b_67b
PCS_RX_BRIDGE_CLK_POLINV	<string >	"RX_BRIDGE_CLK", "REVERSE_OF_RX_BRIDGE_CLK"	"RX_BRIDGE_CLK"	"REVERSE_OF_RX_BRIDGE_CLK": clk invert; "RX_BRIDGE_CLK": without clk invert
PCS_PCS_CB_RSTN	<string >	"FALSE","TRUE"	"FALSE"	PCS CB reset register, i.e., cfg_pcs_cb_rstn, active low.
PCS_TX_BRIDGE_GEAR_SEL	<string >	"FALSE","TRUE"	"FALSE"	Configuration selection for the order of bridge unit and gear modules in tx direction "FALSE": bridge unit first; "TRUE": gear module first
PCS_TX_BYPASS_BRIDGE_UINT	<string >	"FALSE","TRUE"	"FALSE"	Tx Bridge FIFO module Bypass enable, active high
PCS_TX_BYPASS_BRIDGE_FIFO	<string >	"FALSE","TRUE"	"FALSE"	Configured to "TRUE" indicates that the FIFO in the bridge unit module is bypassed. Used when enabling tx clkaligner.
PCS_TX_BYPASS_GEAR	<string >	"FALSE","TRUE"	"FALSE"	One of the data bit width selections for the PCS Transmitter module "FALSE", for 32bit only, 40bit only, or 8b10b 32bit bit width modes; "TRUE", for bit width modes other than 32bit only, 40bit only, or 8b10b 32bit;
PCS_TX_BYPASS_ENCODER	<string >	"FALSE","TRUE"	"FALSE"	8b10b Encoder module Bypass enable, active high
PCS_TX_BYPASS_BIT_SLIP	<string >	"FALSE","TRUE"	"FALSE"	Tx BitSlip module Bypass enable, active high
PCS_TX_GEAR_SPLIT	<string >	"FALSE","TRUE"	"FALSE"	One of the data bit width selections for the PCS Transmitter module "FALSE", for other modes "TRUE", for 32bit only, 40bit only, or 8b10b 32bit bit width modes
PCS_TX_DRIVE_REG_MODE	<string >	"NO_CHANGE", "EN_POLARITY_REV", "EN_BIT_REV", "EN_BOTH"	"NO_CHANGE"	Tx Drive Reg module polarity inversion and bit order inversion; "NO_CHANGE"; no inversion "EN_POLARITY_REV"; enable polarity inversion "EN_BIT_REV"; enable bit order inversion

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
				"EN_BOTH"; enable both polarity inversion and bit order inversion
PCS_TX_BIT_SLIP_CY_CLES	<integer>	0 to 31	0	Determine the number of bits for Slip in the Tx Bit Slip module
PCS_INT_TX_MASK_0	<string>	"FALSE","TRUE"	"FALSE"	Active-high Mask transmit channel interrupt status register (offset address 0x27) bit 0
PCS_INT_TX_MASK_1	<string>	"FALSE","TRUE"	"FALSE"	Active-high Mask transmit channel interrupt status register (offset address 0x27) bit 1
PCS_INT_TX_MASK_2	<string>	"FALSE","TRUE"	"FALSE"	Active-high Mask transmit channel interrupt status register (offset address 0x27) bit 2
PCS_INT_TX_CLR_0	<string>	"FALSE","TRUE"	"FALSE"	Active-high clear transmit channel interrupt status register (offset address 0x27) bit 0
PCS_INT_TX_CLR_1	<string>	"FALSE","TRUE"	"FALSE"	Active-high clear transmit channel interrupt status register (offset address 0x27) bit 1
PCS_INT_TX_CLR_2	<string>	"FALSE","TRUE"	"FALSE"	Active-high clear transmit channel interrupt status register (offset address 0x27) bit 2
PCS_TX_PMA_TCLK_POLINV	<string>	"PMA_TCLK", "REVERSE_OF_PMA_TCLK"	"PMA_TCLK"	"PMA_TCLK":pma_tclk "REVERSE_OF_PMA_TCLK":reverse of pma_tclk
PCS_TX_PCS_CLK_EN_SEL	<string>	"FALSE","TRUE"	"FALSE"	One of the data bit width selections for the PCS Transmitter module "FALSE", for other modes "TRUE"; used for 32bit only, 40bit only, or 8b10b 32bit bit width modes;
PCS_TX_BRIDGE_TCLK_SEL	<string>	"TCLK", "TCLK2"	"TCLK"	TCLK clock source selection choose bridge_tclk "TCLK": tclk "TCLK2": tclk2
PCS_TX_TCLK_POLINV	<string>	"TCLK", "REVERSE_OF_TCLK"	"TCLK"	"TCLK":tclk "REVERSE_OF_TCLK":reverse of tclk
PCS_PCS_TCLK_SEL	<string>	"PMA_TCLK", "TCLK"	"PMA_TCLK"	choose pcs_tclk "PMA_TCLK": pma_tclk "TCLK":tclk
PCS_TX_PCS_TX_RSTN	<string>	"FALSE","TRUE"	"FALSE"	Reset register for the PCS Transmitter, i.e., cfg_pcs_tx_rstn, active low
PCS_TX_SLAVE	<string>	"MASTER", "SLAVE"	"MASTER"	Channel bonding setting at the transmit side "SLAVE":slave channel "MASTER":master channel
PCS_TX_GEAR_CLK_EN_SEL	<string>	"FALSE","TRUE"	"FALSE"	One of the data bit width selections for the PCS Transmitter module "FALSE", for other modes "TRUE"; for 32bit only, 40bit only, or 8b10b 32bit width modes, and Bypass Tx Bridge FIFO mode;
PCS_DATA_WIDTH_MODE	<string>	"X20","X16","X10", ,"X8"	"X20"	One of the data bit width selections for the PCS Transmitter module

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
				"X20"; for 20bit only, 8b10b 16bit, 8b10b 32bit, and 40bit only modes "X16"; for 16bit only and 32bit only modes "X10"; for 10bit only and 8b10b 8bit modes "X8"; for 8bit only mode
PCS_TX_64B66B_67B	<string >	"NORMAL","64B_66B","64B_67B"	"NORM AL"	"NORMAL": without 64b_66b/67b; "64B_66B": 64b_66b; "64B_67B": 64b_67b
PCS_GEAR_TCLK_SEL	<string >	"PMA_TCLK","TCLK2"	"PMA_TCLK"	choose gear_tclk "PMA_TCLK": pma_tclk "TCLK2":tclk2
PCS_TX_TCLK2FABRIC_SEL	<string >	"FALSE","TRUE"	"FALSE"	One of the data bit width selections for the PCS Transmitter module 1"FALSE"; for modes other than 32bit only, 40bit only, and 8b10b 32bit "TRUE"; for 32bit only, 40bit only, and 8b10b 32bit modes
PCS_TX_OUTZZ	<string >	"FALSE","TRUE"	"FALSE"	Used to distinguish the output format of 16bit/32bit only mode 1: 16/32bit only mode (currently not in use) 0: other data width mode
PCS_ENC_DUAL	<string >	"FALSE","TRUE"	"FALSE"	One of the data bit width selections for the PCS Transmitter module "FALSE"; used for modes other than 8b10b 16bit and 8b10b 32bit "TRUE", used for 8b10b 16bit and 8b10b 32bit modes
PCS_TX_BITSLIP_DATA_MODE	<string >	"X10", "X20"	"X10"	One of the data bit width selections for the PCS Transmitter module "X10"; for 10bit only and 8b10b 8bit modes "X20"; used for modes other than 10bit only and 8b10b 8bit
PCS_TX_BRIDGE_CLK_POLINV	<string >	"TX_BRIDGE_CLK", "REVERSE_OF_TX_BRIDGE_CLK"	"TX_BRIDGE_CLK"	"REVERSE_OF_TX_BRIDGE_CLK": clk invert; "TX_BRIDGE_CLK": without clk invert
PCS_COMMA_REG1	<integer>	0 to 1023	0	Word Alignment Comma byte definition 1
PCS_RAPID_IMAX	<integer>	0 to 7	0	Number of bytes for lock state detection in Rapid IO Link State Machine
PCS_RAPID_VMIN_1	<integer>	0 to 255	0	Number of bytes for exit state detection in Rapid IO Link State Machine
PCS_RAPID_VMIN_2	<integer>	0 to 255	0	Number of bytes for exit state detection in Rapid IO Link State Machine
PCS_RX_PRBS_MODE	<string >	"DISABLE","PRBS_7","PRBS_15","PRBS_23","PRBS_31"	"DISABLE"	PRBS Checker mode selection at the receive side

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PCS_RX_ERRCNT_CLR	<string >	"FALSE","TRUE"	"FALSE"	prbs_errcnt_clr, active high to clear error counts in the PRBS checker
PCS_PRBS_ERR_LPBK	<string >	"FALSE","TRUE"	"FALSE"	prbs_err_lpbk
PCS_TX_PRBS_MODE	<string >	"DISABLE","PRBS_7","PRBS_15","PRBS_23","PRBS_31","LONG_1","LONG_0","20UI","D10_2","PCIE"	"DISABLE"	prbs gen mode signal
PCS_TX_INSERT_ER	<string >	"FALSE","TRUE"	"FALSE"	prbs_insert_er, a high pulse from 0 to 1 can insert an error code during PRBS generation
PCS_ENABLE_PRBS_GEN	<string >	"FALSE","TRUE"	"FALSE"	PRBS generation enable, active high "FALSE", for other modes "TRUE"; used for 32bit only, 40bit only, or 8b10b 32bit bit width modes;
PCS_DEFAULT_RADDR	<integer>	0 to 15	0	Default address for channel detection A in channel bonding
PCS_MASTER_CHECK_OFFSET	<integer>	0 to 15	0	Offset address for master channel detection in channel bonding
PCS_DELAY_SET	<integer>	0 to 15	0	Channel delay configuration between channel bondings.
PCS_SEACH_OFFSET	<string >	"20BIT","30BIT","40BIT","50BIT","60BIT","70BIT","80BIT"	"20BIT"	Search range configuration for the auxiliary channel of channel bonding: "20BIT": 20 bits; "30BIT": 30 bits; "40BIT": 40 bits; "50BIT": 50 bits; "60BIT": 60 bits; "70BIT": 70 bits; "80BIT": 80 bits.
PCS_CEB_RAPIDLS_MMAX	<integer>	0 to 7	0	MMAX value used by Channel Bonding RapidIO state machine
PCS_CTC_AFULL	<integer>	0 to 31	20	The Almost Full threshold for the CTC FIFO, which should be set to 5'd20 by default
PCS_CTC_AEMPTY	<integer>	0 to 31	12	The Almost Empty threshold for the CTC FIFO, which should be set to 5'd12 by default
PCS_CTC_CONTI_SKP_SET	<integer>	0 to 1	0	Enable SKP Ordered set skip delete continuously
PCS_FAR_LOOP	<string >	"FALSE","TRUE"	"FALSE"	PCS far-end loopback enable, active high
PCS_NEAR_LOOP	<string >	"FALSE","TRUE"	"FALSE"	PCS near-end loopback enable, active high
PCS_PMA_TX2RX_PL_OOP_EN	<string >	"FALSE","TRUE"	"FALSE"	Enable PCS_PMA_TX2RX_PLOOP
PCS_PMA_TX2RX_SL_OOP_EN	<string >	"FALSE","TRUE"	"FALSE"	Enable PCS_PMA_TX2RX_SLOOP
PCS_PMA_RX2TX_PL_OOP_EN	<string >	"FALSE","TRUE"	"FALSE"	Enable PCS_PMA_RX2TX_PLOOP
PCS_INT_RX_MASK_0	<string >	"FALSE","TRUE"	"FALSE"	Receive channel interrupt status

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
				register (offset address 0x28) bit 0 mask, active high
PCS_INT_RX_MASK_1	<string >	"FALSE","TRUE"	"FALSE"	Receive channel interrupt status register (offset address 0x28) bit 1 mask, active high
PCS_INT_RX_MASK_2	<string >	"FALSE","TRUE"	"FALSE"	Receive channel interrupt status register (offset address 0x28) bit 2 mask, active high
PCS_INT_RX_MASK_3	<string >	"FALSE","TRUE"	"FALSE"	Receive channel interrupt status register (offset address 0x28) bit 3 mask, active high
PCS_INT_RX_MASK_4	<string >	"FALSE","TRUE"	"FALSE"	Receive channel interrupt status register (offset address 0x28) bit 4 mask, active high
PCS_INT_RX_MASK_5	<string >	"FALSE","TRUE"	"FALSE"	Receive channel interrupt status register (offset address 0x28) bit 5 mask, active high
PCS_INT_RX_MASK_6	<string >	"FALSE","TRUE"	"FALSE"	Receive channel interrupt status register (offset address 0x28) bit 6 mask, active high
PCS_INT_RX_MASK_7	<string >	"FALSE","TRUE"	"FALSE"	Receive channel interrupt status register (offset address 0x28) bit 7 mask, active high
PCS_INT_RX_CLR_0	<string >	"FALSE","TRUE"	"FALSE"	Clear receive channel interrupt status register (offset address 0x28) bit 0, active high
PCS_INT_RX_CLR_1	<string >	"FALSE","TRUE"	"FALSE"	Clear receive channel interrupt status register (offset address 0x28) bit 1, active high
PCS_INT_RX_CLR_2	<string >	"FALSE","TRUE"	"FALSE"	Clear receive channel interrupt status register (offset address 0x28) bit 2, active high
PCS_INT_RX_CLR_3	<string >	"FALSE","TRUE"	"FALSE"	Clear receive channel interrupt status register (offset address 0x28) bit 3, active high
PCS_INT_RX_CLR_4	<string >	"FALSE","TRUE"	"FALSE"	Clear receive channel interrupt status register (offset address 0x28) bit 4, active high
PCS_INT_RX_CLR_5	<string >	"FALSE","TRUE"	"FALSE"	Clear receive channel interrupt status register (offset address 0x28) bit 5, active high
PCS_INT_RX_CLR_6	<string >	"FALSE","TRUE"	"FALSE"	Clear receive channel interrupt status register (offset address 0x28) bit 6, active high
PCS_INT_RX_CLR_7	<string >	"FALSE","TRUE"	"FALSE"	Clear receive channel interrupt status register (offset address 0x28) bit 7, active high
PCS_CA_RSTN_RX	<string >	"FALSE","TRUE"	"FALSE"	Rx CLK Aligner reset, i.e., cfg_ca_rstn_rx, active low.
PCS_CA_DYN_DLY_E_N_RX	<string >	"FALSE","TRUE"	"FALSE"	When set to "FALSE", the CLK Aligner output for the corresponding receive channel is forced to 0. When set to "TRUE", the CLK Aligner delay step is determined by CLK_ALIGNER_RX or

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
				P_CIM_CLK_ALIGNER_RXx [7:0].
PCS_CA_DYN_DLY_SEL_RX	<string >	"FALSE", "TRUE"	"FALSE"	When set to "FALSE", the CLK Aligner function for the corresponding receive channel is disabled, and the CLK Aligner is bypassed. When set to "TRUE", the CLK Aligner function for the corresponding receive channel is enabled.
PCS_CA_RX	<integer>	0 to 255	0	The static setting for the CLK Aligner delay step of the corresponding receive channel, used when P_CIM_CLK_DYN_DLY_SEL_RX[x] is invalid
PCS_CA_RSTN_TX	<string >	"FALSE", "TRUE"	"FALSE"	Tx CLK Aligner reset, i.e., cfg_ca_rstn_tx, active low.
PCS_CA_DYN_DLY_EN_TX	<string >	"FALSE", "TRUE"	"FALSE"	When set to "FALSE", the CLK Aligner output for the corresponding transmit channel is forced to 0. When set to "TRUE", the CLK Aligner delay step is determined by CLK_ALIGNER_TXx or P_CIM_CLK_ALIGNER_TXx [7:0].
PCS_CA_DYN_DLY_SEL_TX	<string >	"FALSE", "TRUE"	"FALSE"	When set to "FALSE", the CLK Aligner function for the corresponding transmit channel is disabled, and the CLK Aligner is bypassed. When set to "TRUE", the CLK Aligner function for the corresponding transmit channel is enabled.
PCS_CA_TX	<integer>	0 to 255	0	Static setting for the CLK Aligner delay step of the corresponding transmission channel, Used when P_CIM_CLK_DYN_DLY_SEL_TX[x] is invalid
PCS_RXPRBS_PWR_REDUCTION	<string >	"NORMAL", "POWER_REDUCTION"	"NORMAL"	Rx prbs power reduction option
PCS_WDALIGN_PWR_REDUCTION	<string >	"NORMAL", "POWER_REDUCTION"	"NORMAL"	Rx wordalign power reduction option
PCS_RXDEC_PWR_REDUCTION	<string >	"NORMAL", "POWER_REDUCTION"	"NORMAL"	Rx 8b10b decoder power reduction option
PCS_RXCB_PWR_REDUCTION	<string >	"NORMAL", "POWER_REDUCTION"	"NORMAL"	Rx cbonding power reduction option
PCS_RXCTC_PWR_REDUCTION	<string >	"NORMAL", "POWER_REDUCTION"	"NORMAL"	Rx ctc power reduction option

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PCS_RXGEAR_PWR_REDUCTION	<string >	"NORMAL","POWER_REDUCATION"	"NORMAL"	Rx gear power reduction option
PCS_RXBRG_PWR_REDUCTION	<string >	"NORMAL","POWER_REDUCATION"	"NORMAL"	Rx bridge unit power reduction option
PCS_RXTEST_PWR_REDUCTION	<string >	"NORMAL","POWER_REDUCATION"	"NORMAL"	Rx teststatus power reduction option
PCS_TXBRG_PWR_REDUCTION	<string >	"NORMAL","POWER_REDUCATION"	"NORMAL"	tx bridge unit power reduction option
PCS_TXGEAR_PWR_REDUCTION	<string >	"NORMAL","POWER_REDUCATION"	"NORMAL"	tx gear power reduction option
PCS_TXENC_PWR_REDUCTION	<string >	"NORMAL","POWER_REDUCATION"	"NORMAL"	tx 8b10b encoder power reduction option
PCS_TXBSP_PWR_REDUCTION	<string >	"NORMAL","POWER_REDUCATION"	"NORMAL"	tx bitslip power reduction option
PCS_TXPRBS_PWR_REDUCTION	<string >	"NORMAL","POWER_REDUCATION"	"NORMAL"	tx prbs power reduction option
PMA_REG_RX_PD	<string >	"ON","OFF"	"ON"	rx power down "ON": receiver is fully power on "OFF": receiver is fully power off
PMA_REG_RX_PD_EN	<string >	"FALSE","TRUE"	"FALSE"	enable rx power down control from register "FALSE": rx power down controlled by pma_rx_pd_x "TRUE": rx power down controlled by reg_rx_pd
PMA_REG_RX_RESET_2	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_RX_RESET_3	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_RX_DATAPATH_PD	<string >	"ON","OFF"	"ON"	"ON": receiver datapath is power on "OFF": receiver datapath is power off
PMA_REG_RX_DATAPATH_EN	<string >	"FALSE","TRUE"	"FALSE"	enable the data path power down control from register: "FALSE": data path power down controlled by pma_rx_pd_x "TRUE": data path power down controlled by reg_rx_datapath_pd
PMA_REG_RX_SIGDET_PD	<string >	"ON","OFF"	"ON"	"ON": receiver signal detect is power on "OFF": receiver signal detect is power off

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PMA_REG_RX_SIGDET_PD_EN	<string >	"FALSE","TRUE"	"FALSE"	enable rx signal detect power down control from register "FALSE": rx signal detect power down controlled by pma_rx_pd_x "TRUE": rx signal detect power down controlled by reg_rx_sigdet_pd
PMA_REG_RX_DCC_RST_N	<string >	"FALSE","TRUE"	"TRUE"	RX DCC reset register, low valid "FALSE": reset rx duty cycle correction "TRUE": normal operation of rx DCC
PMA_REG_RX_DCC_RST_N_EN	<string >	"FALSE","TRUE"	"FALSE"	enable the DCC reset control from register "FALSE": cdr reset controlled by pma_rx_reset_n_x "TRUE": cdr reset controlled by reg_rx_dcc_RST_n
PMA_REG_RX_CDR_RST_N	<string >	"FALSE","TRUE"	"TRUE"	CDR reset register, low valid "FALSE": reset CDR "TRUE": normal operation of CDR
PMA_REG_RX_CDR_RST_N_EN	<string >	"FALSE","TRUE"	"FALSE"	enable the cdr reset control from register "FALSE": cdr reset controlled by pma_rx_reset_n_x "TRUE": cdr reset controlled by rx_reg_cdr_rst_n
PMA_REG_RX_SIGDET_RST_N	<string >	"FALSE","TRUE"	"TRUE"	rx signal detect reset register, low valid "FALSE": reset sigdet, and the output rx_sigdet_status is 0 "TRUE": normal operation of sigdet
PMA_REG_RX_SIGDET_RST_N_EN	<string >	"FALSE","TRUE"	"FALSE"	enable the sigdet reset control from register "FALSE": sigdet reset controlled by pma_rx_reset_n_x "TRUE": sigdet reset controlled by reg_rx_sigdet_RST_n
PMA_REG_RXPCLK_SLIP	<string >	"FALSE","TRUE"	"FALSE"	rxpclk delay by 1 UI if reg_rxpclk_slip changes from 0 to 1
PMA_REG_RXPCLK_SLIP_OW	<string >	"FALSE","TRUE"	"FALSE"	enable rxpclk slip control from register "FALSE": rxpclk_slip controlled by pma_rxpclk_slip_x "TRUE": rxpclk_slip controlled by reg_rxpclk_slip_ow
PMA_REG_RX_PCLKS_WITCH_RST_N	<string >	"FALSE","TRUE"	"TRUE"	rx sync reset register, low valid "FALSE": reset rx pclk switch block "TRUE": normal operation

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PMA_REG_RX_PCLKS_WITCH_RST_N_EN	<string >	"FALSE","TRUE"	"FALSE"	enable the rx pclk switch reset control from register "FALSE": rx pclk switch block controlled by pma_rx_reset_n_x "TRUE": rx pclk swithc controlled by reg_rx_pclkswitch_rst_n
PMA_REG_RX_PCLKS_WITCH	<string >	"FALSE","TRUE"	"FALSE"	rx pclk switch control register: "FALSE": refclk is selected as rxpclk "TRUE": cdr recovered pclk is selected as rxpclk
PMA_REG_RX_PCLKS_WITCH_EN	<string >	"FALSE","TRUE"	"FALSE"	enable the tx pclk switch control from register "FALSE": rx pclk switch controlled by pll_ready "TRUE": rx pclk switch controlled by reg_rx_pclkswitch
PMA_REG_RX_HIGHZ	<string >	"FALSE","TRUE"	"FALSE"	receiver termination res high z control register "FALSE": receiver in 50-ohm low-impedance mode "TRUE": receiver in highZ mode
PMA_REG_RX_HIGHZ_EN	<string >	"FALSE","TRUE"	"FALSE"	enable the Rx highZ control from register "FALSE": Rx highZ controlled by pma_rx_highz_x "TRUE": Rx highZ controlled by rx_highz
PMA_REG_RX_SIGDET_CLK_WINDOW	<string >	"FALSE","TRUE"	"FALSE"	Register configuration reg_rx_sigdet_clk_window
PMA_REG_RX_SIGDET_CLK_WINDOW_OW	<string >	"FALSE","TRUE"	"FALSE"	When set to "TRUE", rx_sigdet_clk_window comes from reg_rx_sigdet_clk_window; otherwise, it comes from internal circuit.
PMA_REG_RX_PD_BIAS_RX	<string >	"FALSE","TRUE"	"FALSE"	Register configuration reg_rx_pd_bias_rx "FALSE": rx_bias is power on "TRUE": rx_bias is power off
PMA_REG_RX_PD_BIAS_RX_OW	<string >	"FALSE","TRUE"	"FALSE"	Overwrite PMA_REG_RX_PD_BIAS_RX
PMA_REG_RX_RESET_N	<string >	"FALSE","TRUE"	"FALSE"	rx reset
PMA_REG_RX_RESET_N_OW	<string >	"FALSE","TRUE"	"FALSE"	Overwrite PMA_REG_RX_RESET_N
PMA_REG_RX_RESET_VED_29_28	<integer>	0 to 3	0	Reserved
PMA_REG_RX_BUSWIDTH	<string >	"8BIT","10BIT","16BIT","20BIT",	"20BIT"	rx buswidth control . "8BIT": 8bit "10BIT": 10bit "16BIT": 16bit "20BIT": 20bit

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PMA_REG_RX_BUSW_IDTH_EN	<string >	"FALSE","TRUE"	"FALSE"	Enable PMA_REG_RX_BUSWIDTH., when set to "TRUE", reg_rx_buswidth_i is used instead of pma_rx_buswidth_i
PMA_REG_RX_RATE	<string >	"DIV4","DIV2","DIV1","MUL2"	"DIV1"	Rx rate control register."DIV4": highest datarate /4 "DIV2": highest datarate /2 "DIV1": highest datarate "MUL2": highest datarate*2
PMA_REG_RX_RESERVED_36	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_RX_RATE_EN	<string >	"FALSE","TRUE"	"FALSE"	enable the Rx rate control from register "FALSE": Rx rate controlled by pma_rx_rate_x[2:0] "TRUE": Rx rate controlled by reg_rx_rate[2:0]
PMA_REG_RX_RES_T_RIM	<integer>	0 to 63	46	Rx termination resistor calibration register, 101110: 100 ohm
PMA_REG_RX_RESERVED_44	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_RX_RESERVED_45	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_RX_SIGDET_STATUS_EN	<string >	"FALSE","TRUE"	"FALSE"	When set to "TRUE", pma_rx_sigdet_status_o and rx_sigdet_status_2oob_det_o are directly controlled by the register reg_rx_sigdet_status
PMA_REG_RX_RESERVED_48_47	<integer>	0 to 3	0	Reserved
PMA_REG_RX_ICTRL_SIGDET	<integer>	0 to 15	5	sigdet bias current control register, [1:0] to control sigdet module, [3:2] to control sigdet preamp module 00: sigdet bias current is 43.75uA 01: 50uA 10: 56.25uA 11: 62.5uA
PMA_REG_CDR_READY_THD	<integer>	0 to 4095	2734	Rx cdr ready output status
PMA_REG_RX_RESERVED_65	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_RX_PCLK_EDGE_SEL	<string >	"POS_EDGE","NEG_EDGE"	"POS_EDGE"	rx pclk edge select: "NEG_EDGE": rx_pdata is clocked out to Tx on the falling edge of rxpclk "POS_EDGE": rx_pdata is clocked out to Tx on the rising edge of rxpclk
PMA_REG_RX_PIBUF_IC	<integer>	0 to 3	1	rx pi buf bandwidth control logic
PMA_REG_RX_RESERVED_69	<string >	"FALSE","TRUE"	"FALSE"	Reserved

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PMA_REG_RX_DCC_IC_RX	<integer>	0 to 3	1	rx_dcc_ic_rx<1>: RX clkpath mode control. 1'b1: only one PI is working; 1'b0: two PI are working; (default). rx_dcc_ic_rx<0>: rx pi buf bandwidth control logic, equal to rx_pibuf_ic<2>.
PMA_REG_CDR_READY_CHECK_CTRL	<integer>	0 to 3	0	cdr_ready_after_check selection: 0: CDR ready signal comes from the cdr_ready_o port of the pma6g_cdr_pseudo_lockdet module; When set to 1, select ready_reg_once to output to cdr_ready; When set to 2, select ready_reg to output to cdr_ready; 3: reserved
PMA_REG_RX_ICTRL_TRX	<string >	"87_5PCT","100PCT","112_5PCT","125PCT"	"100PCT"	rx bias current control register. "87_5PCT": 87.5% "100PCT": 100% "112_5PCT": 112.5% "125PCT": 125%
PMA_REG_RX_RESERVED_77_76	<integer>	0 to 3	0	Reserved
PMA_REG_RX_RESERVED_79_78	<integer>	0 to 3	1	Reserved
PMA_REG_RX_RESERVED_81_80	<integer>	0 to 3	1	Reserved
PMA_REG_RX_ICTRL_PIBUF	<string >	"87_5PCT","100PCT","112_5PCT","125PCT"	"100PCT"	phase interpolator pre-buffer bias current control "87_5PCT": 87.5% "100PCT": 100% "112_5PCT": 112.5% "125PCT": 125%
PMA_REG_RX_ICTRL_PI	<string >	"87_5PCT","100PCT","112_5PCT","125PCT"	"100PCT"	phase interpolator path bias current control "87_5PCT": 87.5% "100PCT": 100% "112_5PCT": 112.5% "125PCT": 125%
PMA_REG_RX_ICTRL_DCC	<string >	"87_5PCT","100PCT","112_5PCT","125PCT"	"100PCT"	receiver DCC bias current control "87_5PCT": 87.5% "100PCT": 100% "112_5PCT": 112.5% "125PCT": 125%
PMA_REG_RX_RESERVED_89_88	<integer>	0 to 3	1	Reserved
PMA_REG_TX_RATE	<string >	"DIV4","DIV2","DIV1","MUL2"	"DIV1"	TX rate control signal;"DIV4": highest datarate /4 "DIV2": highest datarate /2 "DIV1": highest datarate "MUL2": highest datarate*2
PMA_REG_RX_RESERVED_92	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_TX_RATE_	<string >	"FALSE","TRUE"	"FALSE"	enable the tx rate control from

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
EN				register "FALSE": tx rate controlled by pma_tx_rate_x[2:0] "TRUE": tx rate controlled by reg_rx_rate[2:0]
PMA_REG_RX_TX2RX_PLPBK_RST_N	<string >	"FALSE","TRUE"	"TRUE"	rx tx2rx parallel loop back block reset register, low valid "FALSE": reset tx2rx parallel loop back block "TRUE": normal operation
PMA_REG_RX_TX2RX_PLPBK_RST_N_EN	<string >	"FALSE","TRUE"	"FALSE"	enable the tx2rx parallel loop back reset control from register "FALSE": sigdet reset controlled by pma_rx_reset_n_x "TRUE": sigdet reset controlled by reg_rx_tx2rx_plpbk_RST_n
PMA_REG_RX_TX2RX_PLPBK_EN	<string >	"FALSE","TRUE"	"FALSE"	Enable PMA_REG_RX_TX2RX_PLPBK
PMA_REG_TXCLK_SEL	<string >	"PLL","RXCLK"	"PLL"	"PLL": select pll clock as txclk "RXCLK": select rxclk as txclk
PMA_REG_RX_DATA_POLARITY	<string >	"NORMAL","REVERSE"	"NORMAL"	rx data polarity control register, default is "NORMAL" "REVERSE": reverse the rx parallel output polarity "NORMAL": normal output
PMA_REG_RX_ERR_INSERT	<string >	"FALSE","TRUE"	"FALSE"	reg_rx_err_insert rising edge is used to generate on clock cycle pulse, default is "FALSE"
PMA_REG_UDP_CHK_EN	<string >	"FALSE","TRUE"	"FALSE"	Enable PMA_REG_UDP_CHK. When enabled, data_i is captured to udp_o on the rising edge
PMA_REG_PRBS_SEL	<string >	"PRBS7","PRBS15","PRBS23","PRBS31"	"PRBS7"	PRBS pattern select "PRBS7": PRBS7 "PRBS15": PRBS15 "PRBS23": PRBS23 "PRBS31": PRBS31
PMA_REG_PRBS_CHK_EN	<string >	"FALSE","TRUE"	"FALSE"	Enable PMA_REG_PRBS_CHK
PMA_REG_PRBS_CHK_WIDTH_SEL	<string >	"8BIT","10BIT","16BIT","20BIT",	"20BIT"	bist checker input data bus width selection "8BIT": 8bit "10BIT": 10bit "16BIT": 16bit "20BIT": 20bit
PMA_REG_BIST_CHK_PATTERN_SEL	<string >	"PRBS","CONSTANT"	"PRBS"	BIST constant pattern or PRBS pattern selection. Selecting "PRBS" enables PRBS checking, while selecting "CONSTANT" enables UDP checking (UDP check not used)
PMA_REG_LOAD_ERROR_CNT	<string >	"FALSE","TRUE"	"FALSE"	When set to "TRUE" err_counter_o remains unchanged, When set to "FALSE" err_counter_o is the internal error count value
PMA_REG_CHK_COU	<string >	"FALSE","TRUE"	"FALSE"	Enable

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
NTER_EN				PMA_REG_CHK_COUNTER
PMA_REG_CDR_PROP_GAIN	<integer>	0 to 7	7	Normal mode proportional gain control: 000:1/2^10 001:1/2^9 010:1/2^8 011:1/2^7 100:1/2^6 101:1/2^5 110:1/2^4 111:1/2^3
PMA_REG_CDR_PROP_TURBO_GAIN	<integer>	0 to 7	5	turbo mode proportional gain control: 000:1/2^10 001:1/2^9 010:1/2^8 011:1/2^7 100:1/2^6 101:1/2^5 110:1/2^4 111:1/2^3
PMA_REG_CDR_INT_GAIN	<integer>	0 to 7	7	Normal mode integral gain control: 000:1/2^14 001:1/2^13 010:1/2^12 011:1/2^11 100:1/2^10 101:1/2^9 110:1/2^8 111:1/2^7
PMA_REG_CDR_INT_TURBO_GAIN	<integer>	0 to 7	5	turbo mode integral gain control: 000:1/2^14 001:1/2^13 010:1/2^12 011:1/2^11 100:1/2^10 101:1/2^9 110:1/2^8 111:1/2^7
PMA_REG_CDR_INT_SAT_MAX	<integer>	0 to 1023	768	Set the maximum positive deviation of the integral path, The default value (255) is +3700ppm, approximately (x/255*+3700ppm) for other configurations
PMA_REG_CDR_INT_SAT_MIN	<integer>	0 to 1023	255	Set the maximum negative deviation of the integral path. The default value (255) is -3700ppm, approximately (x/255*-3700ppm) for other configurations
PMA_REG_CDR_INT_RST	<string>	"FALSE","TRUE"	"FALSE"	Reset the integral path, active high. "FALSE": disable "TRUE": reset the integral path

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PMA_REG_CDR_INT_RST_OW	<string >	"FALSE","TRUE"	"FALSE"	Integral path reset rewrite, active high. "FALSE": disable "TRUE": control integral path reset with reg_cdr_int_rst
PMA_REG_CDR_PROP_RST	<string >	"FALSE","TRUE"	"FALSE"	Reset the proportional path, active high. "FALSE": disable "TRUE": reset the proportional path
PMA_REG_CDR_PROP_RST_OW	<string >	"FALSE","TRUE"	"FALSE"	Proportional path reset overwrite, active high. "FALSE": disable "TRUE": control proportional path reset with reg_cdr_prop_rst
PMA_REG_CDR_LOC_K_RST	<string >	"FALSE","TRUE"	"FALSE"	CDR lock counter reset, active high. "FALSE": disable "TRUE": reset the lock counter
PMA_REG_CDR_LOC_K_RST_OW	<string >	"FALSE","TRUE"	"FALSE"	CDR lock counter reset overwrite, active high. "FALSE": disable "TRUE": control lock counter reset with reg_cdr_lock_rst. (Default to 0, the above three resets are by default controlled by CDR reset, signal detection status or saturation reset)
PMA_REG_CDR_RX_PI_FORCE_SEL	<integer>	0,1	0	Force selection of CDR phase interpolator control value. 0: rx pi ctrl uses Postadder output. 1: rx pi ctrl uses force data
PMA_REG_CDR_RX_PI_FORCE_D	<integer>	0 to 255	0	CDR rx pi ctrl force data
PMA_REG_CDR_LOC_K_TIMER	<string >	"0_8U","1_2U","1_6U","2_4U","3_2U","4_8U","12_8U","25_6U"	"1_2U"	pseudo control of cdr lock time (for 312.5MHz clock) "0_8U": 0.8u 256 cycles "1_2U": 1.2u 384 cycles (PCIE default: 001) ; "1_6U": 1.6u 512cycles ; "2_4U": 2.4u 768cycles; "3_2U": 3.2u 1024cycles ; "4_8U": 4.8u 1536cycles; "12_8U": 12.8u 4096cycles ; "25_6U": 25.6u 8192cycles ;(others default: "25_6U") (the default counter counts to 384 cycles before outputting CDR ready)

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PMA_REG_CDR_TURBO_MODE_TIMER	<integer>	0 to 3	1	0: turbo_mode time is the same as lock time. 1: turbo_mode time is 3/4 of lock time. 2: turbo_mode time is 1/2 of lock time. 3: turbo_mode time is 1/4 of lock time. (First execute turbo mode, and after the turbo mode time, switch to normal mode. The '/' uses floor (round down))
PMA_REG_CDR_LOC_K_VAL	<string>	"FALSE","TRUE"	"FALSE"	cdr ready rewrite value
PMA_REG_CDR_LOC_K_OW	<string>	"FALSE","TRUE"	"FALSE"	cdr ready rewrite enable. "FALSE": disabled "TRUE": cdr ready value uses reg_cdr_lock_val
PMA_REG_CDR_INT_SAT_DET_EN	<string>	"FALSE","TRUE"	"TRUE"	Integration path saturation detection enable. "FALSE": disable "TRUE": enable (When enabled, the integration upper limit is the saturation setting value)
PMA_REG_CDR_SAT_AUTO_DIS	<string>	"FALSE","TRUE"	"TRUE"	cdr_sat_max/min selection control signal "TRUE": cdr_sat_max directly from reg_cdr_sat_max, cdr_sat_min directly from reg_cdr_sat_min; "FALSE": dynamically selected based on rx_rate
PMA_REG_CDR_GAIN_AUTO	<string>	"FALSE","TRUE"	"FALSE"	Gain selection signal "TRUE": from dynamically selected based on rx_rate; "FALSE": cdr_prop_gain_sel from reg_cdr_prop_gain_sel, cdr_int_gain_sel directly from reg_cdr_int_gain_sel.
PMA_REG_CDR_TURBO_GAIN_AUTO	<string>	"FALSE","TRUE"	"FALSE"	Turbo Gain selection signal "TRUE": from dynamically selected based on rx_rate; "FALSE": cdr_turbo_prop_gain_sel from reg_cdr_turbo_prop_gain_sel, cdr_turbo_int_gain_sel from reg_cdr_turbo_int_gain_sel
PMA_REG_RX_RESET_VED_171_167	<integer>	0 to 31	0	Reserved
PMA_REG_RX_RESET_VED_175_172	<integer>	0 to 31	0	Reserved
PMA_REG_CDR_SAT_DET_STATUS_EN	<string>	"FALSE","TRUE"	"FALSE"	Integration saturation state enable. "FALSE": disable "TRUE": enable
PMA_REG_CDR_SAT_DET_STATUS_RESET_EN	<string>	"FALSE","TRUE"	"FALSE"	When saturation of the cdr is detected, reset the cdr. "FALSE": disable

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
				"TRUE": enable
PMA_REG_CDR_PI_C_TRL_RST	<string >	"FALSE", "TRUE"	"FALSE"	Phase interpolator control value reset register
PMA_REG_CDR_PI_C_TRL_RST_OW	<string >	"FALSE", "TRUE"	"FALSE"	Phase interpolator control reset rewrite, active high. "FALSE": disable "TRUE": use reg_cdr_pi_ctrl_RST to control phase interpolator control reset (In "FALSE" condition, use cdr_RST to control whether to reset)
PMA_REG_CDR_SAT_DET_RST	<string >	"FALSE", "TRUE"	"FALSE"	Saturation detection reset, active high. "FALSE": disable "TRUE": saturation detection module reset
PMA_REG_CDR_SAT_DET_RST_OW	<string >	"FALSE", "TRUE"	"FALSE"	Saturation detection reset rewrite, active high. "FALSE": disable "TRUE": use reg_cdr_sat_det_RST to decide whether the saturation detection module reset (In "FALSE" condition, control reset using cdr_RST or sig_not_det)
PMA_REG_CDR_SAT_DET_STICKY_RST	<string >	"FALSE", "TRUE"	"FALSE"	Saturation detection status sticky reset, active high. "FALSE": disable "TRUE": reset sat_det status sticky
PMA_REG_CDR_SAT_DET_STICKY_RST_OW	<string >	"FALSE", "TRUE"	"FALSE"	sat_det status sticky reset rewrite, active high. "FALSE": disable "TRUE": use reg_cdr_sat_det_sticky_RST to control whether sat_det status sticky resets. (In "FALSE" condition, use cdr_RST to control reset)
PMA_REG_CDR_SIGDET_STATUS_DIS	<string >	"FALSE", "TRUE"	"FALSE"	disable sigdet_status "FALSE": cdr resets when sigdet_status is low "TRUE": cdr does not respond to sigdet_status
PMA_REG_CDR_SAT_DET_TIMER	<integer>	0 to 3	2	0: Saturation is considered reached if saturation is detected in 64 out of 1024 cycles 1: Saturation is considered reached if saturation is detected in 128 out of 1024 cycles 2: Saturation is considered reached if saturation is detected in 256 out of 1024 cycles 3: Saturation is considered reached if saturation is detected in 512 out of 1024 cycles
PMA_REG_CDR_SAT_DET_STATUS_VAL	<string >	"FALSE", "TRUE"	"FALSE"	Saturation detection status rewrite register

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PMA_REG_CDR_SAT_DET_STATUS_OW	<string >	"FALSE","TRUE"	"FALSE"	Saturation detection status rewrite register enable "FALSE": disable "TRUE": use reg_cdr_sat_det_status_val to rewrite saturation status
PMA_REG_CDR_TURBO_MODE_EN	<string >	"FALSE","TRUE"	"TRUE"	cdr turbo mode enable "FALSE": disable. "TRUE": enable.
PMA_REG_RX_RESET_VED_190	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_RX_RESET_VED_193_191	<integer>	0 to 7	0	Reserved
PMA_REG_CDR_STATUS_FIFO_EN	<string >	"FALSE","TRUE"	"TRUE"	cdr status fifo enable "FALSE": disable "TRUE": enable
PMA_REG_PMA_TEST_SEL	<integer>	0,1	0	register reg_pma_test_sel Select which signal connected to fifo for test 0: cdr pictrl value 1: cdr int data others reserved
PMA_REG_OOB_COM_WAKE_GAP_MIN	<integer>	0 to 63	3	Minimum length threshold for a COMWAKE signal gap.
PMA_REG_OOB_COM_WAKE_GAP_MAX	<integer>	0 to 63	11	Maximum length threshold for a COMWAKE signal gap.
PMA_REG_OOB_COM_INIT_GAP_MIN	<integer>	0 to 255	15	Minimum length threshold for a COMINIT signal gap.
PMA_REG_OOB_COM_INIT_GAP_MAX	<integer>	0 to 255	35	Maximum length threshold for a COMINIT signal gap.
PMA_REG_RX_RESET_VED_227_226	<integer>	0 to 3	1	Reserved
PMA_REG_COMWAKE_STATUS_CLEAR	<integer>	0,1	0	Clear pma_rx_sata_comwake status, high active. When comwake needs clearing, this register should be written twice: first with "1" (clear enabled) and second with "0" (clear disabled, waiting for new detection).
PMA_REG_COMINIT_STATUS_CLEAR	<integer>	0,1	0	Clear pma_rx_sata_cominit status, high active. When cominit needs clearing, this register should be written twice: first with "1" (clear enabled) and second with "0" (clear disabled, waiting for new detection).
PMA_REG_RX_SYNC_RST_N_EN	<string >	"FALSE","TRUE"	"FALSE"	rx sync module reset overwrite FALSE: rx sync reset controlled by internal logic TRUE: rx sync reset controlled by reg_rx_sync_rst_n
PMA_REG_RX_SYNC_RST_N	<string >	"FALSE","TRUE"	"TRUE"	rx sync module reset register
PMA_REG_RX_RESET_VED_233_232	<integer>	0 to 3	0	Reserved
PMA_REG_RX_RESET	<integer>	0 to 3	0	Reserved

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
VED_235_234				
PMA_REG_RX_SATA_COMINIT_OW	<string >	"FALSE","TRUE"	"FALSE"	Overwrite PMA_REG_RX_SATA_COMINIT FALSE: use FSM output signal TRUE: use reg_rx_sata_cominit
PMA_REG_RX_SATA_COMINIT	<string >	"FALSE","TRUE"	"FALSE"	FALSE: COMINIT signal is not detected. TRUE: COMINIT signal is detected
PMA_REG_RX_SATA_COMWAKE_OW	<string >	"FALSE","TRUE"	"FALSE"	Overwrite PMA_REG_RX_SATA_COMWAKE FALSE: use FSM output signal; TRUE: use reg_rx_sata_cominit
PMA_REG_RX_SATA_COMWAKE	<string >	"FALSE","TRUE"	"FALSE"	FALSE: COMWAKE signal is not detected. TRUE: COMWAKE signal is detected
PMA_REG_RX_RESER_VED_241_240	<integer>	0 to 3	0	Reserved
PMA_REG_RX_DCC_DISABLE	<string >	"FALSE","TRUE"	"FALSE"	rx dcc disable control. "FALSE": dcc is enable "TRUE": dcc is disable
PMA_REG_RX_RESER_VED_243	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_RX_SLIP_SEL_EN	<string >	"FALSE","TRUE"	"FALSE"	overwrite enable signal of reg_rx_slip_sel
PMA_REG_RX_SLIP_SEL	<integer>	0 to 15	0	slip output selection signal based on counter value of slip control
PMA_REG_RX_SLIP_EN	<string >	"FALSE","TRUE"	"FALSE"	"TRUE": bypass cdr demux "FALSE": cdr demux works normally
PMA_REG_RX_SIGDET_STATUS_SEL	<integer>	0 to 7	5	rx signal detection status signals selection: 000: channel 0 (comparator based signal detector) 001: channel 1 (comparator based signal detector+ check window filter) 010: channel 2 (slicer based signal detector) 011: channel0 channel1 100: channel0 channel2 101: channel0 channel1 channel2 channel3 110: channel1 channel2 111: channel 3
PMA_REG_RX_SIGDET_FSM_RST_N	<string >	"FALSE","TRUE"	"TRUE"	rx signal status post process fsm resetn: "FALSE": active "TRUE": normal mode, reset by pma_por_n & pma_rx_reset_n
PMA_REG_RX_RESER_VED_254	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_RX_SIGDET_STATUS	<string >	"FALSE","TRUE"	"FALSE"	Sigdet output status, set monitoring signal status value

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PMA_REG_RX_SIGDET_VTH	<string>	"9MV","18MV","27MV","36MV","45MV","54MV","63MV","72MV"	"27MV"	rx signal detect single end peak-peak voltage threshold control: x111: 72 MV x110: 63 MV x101: 54 MV x100: 45 MV x011: 36 MV x010: 27 MV x001: 18 MV x000: 9 MV Bit[3] is reserved.
PMA_REG_RX_SIGDET_GRM	<integer>	0,1,2,3	0	glitch remove setting for rx signal detection.
PMA_REG_RX_SIGDET_PULSE_EXT	<string>	"FALSE","TRUE"	"FALSE"	signal pulse extention enable for rx signal detection.
PMA_REG_RX_SIGDET_CH2_SEL	<integer>	0,1	0	rx signal detect channel 2 input signal selection. 0: the RC filtered comparison signal is sent to detect channel 2. 1: the comparison signal is directly sent to signal detect channel 2
PMA_REG_RX_SIGDET_CH2_CHK_WINDOW	<integer>	0 to 31	3	channel 2 sigdet filter check window is 1 cycle to 32 cycles configurable. 0: 1 refclk clock cycle 31: 32 refclk clock cycles
PMA_REG_RX_SIGDET_CHK_WINDOW_EN	<string>	"FALSE","TRUE"	"TRUE"	Enable PMA_REG_RX_SIGDET_CHK_WINDOW, when "FALSE", the analog input selected by reg_rx_sigdet_status_sel is directly output through port pma_rx_sigdet_status_o (filter bypass); the analog input selected by reg_rx_sigdet_4oob_det_sel_rw is directly output through port rx_sigdet_status_2oob_det_o (filter bypass)
PMA_REG_RX_SIGDET_NOSIG_COUNT_SETTING	<integer>	0 to 7	4	counter of consecutive clock cycles during which no signal is detected. 0: nosig_count_timeout=8'd0 1: nosig_count_timeout=8'd3 2: nosig_count_timeout=8'd7 3: nosig_count_timeout=8'd15 4: nosig_count_timeout=8'd31 5: nosig_count_timeout=8'd63 6: nosig_count_timeout=8'd127 7: nosig_count_timeout=8'd255
PMA_REG_SLIP_FIFO_INV_EN	<string>	"FALSE","TRUE"	"FALSE"	overwrite enable signal of reg_slip_fifo_inv
PMA_REG_SLIP_FIFO_INV	<string>	"POS_EDGE", "NEG_EDGE"	"POS_EDGE"	Slip fifo clock domain edge select signal. POS_EDGE: slip clock domain uses rising edge

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
				NEG_EDGE: slip clock domain uses falling edge
PMA_REG_RX_SIGDET_OOB_DET_COUNT_VAL	<integer>	0 to 31	0	counter value of sigdet in oob detection mode, rx_sigdet_status_2oob_det_o filter parameter M; M= reg_rx_sigdet_oob_det_count_val+1
PMA_REG_RX_SIGDET_4OOB_DET_SEL	<integer>	0 to 7	7	Description is the same as pma_rx_reg_i[252:250]. It's for oob application. rx signal detection status signals selection: 000: channel 1 (comparator based signal detector) 001: channel 2 (comparator based signal detector+ check window filter) 010: channel 3 (slicer based signal detector) 011: channel1 channel2 100: channel1 channel3 101: channel1 channel2 channel3 channel4 110: channel2 channel3 111: channel 4
PMA_REG_RX_RESET_VED_285_283	<integer>	0 to 7	0	Reserved
PMA_REG_RX_RESET_VED_286	<string>	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_RX_SIGDET_IC_I	<integer>	0 to 15	10	rx signal detector mux and comparator current control.
PMA_REG_RX_OOB_DETECTOR_RESET_N_OW	<string>	"FALSE","TRUE"	"FALSE"	Overwrite PMA_REG_RX_OOB_DETECTOR_RESET_N "FALSE": oob detector reset controlled by pma_rx_reset_n&pma_por_n ,"TRUE": oob detector reset controlled by reg_rx_oob_detector_reset_n
PMA_REG_RX_OOB_DETECTOR_RESET_N	<string>	"FALSE","TRUE"	"FALSE"	rx oob detector reset register, low effect FALSE: reset rx oob detector TRUE: normal operation
PMA_REG_RX_OOB_DETECTOR_PD_OW	<string>	"FALSE","TRUE"	"FALSE"	Overwrite PMA_REG_RX_OOB_DETECTOR_PD "FALSE": use FSM output signal ,"TRUE":use reg_rx_oob_detector_pd
PMA_REG_RX_OOB_DETECTOR_PD	<string>	"ON","OFF"	"ON"	rx oob detector powerdown: ON: poweron rx oob detector OFF:powerdown rx oob detector
PMA_REG_RX_LS_M	<string>	"FALSE","TRUE"	"FALSE"	Enable Low-speed mode;

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
ODE_EN				1'b0: Disable low-speed mode; 1'b1: Enable low-speed mode.
PMA_REG_ANA_RX_EQ1_R_SET_FB_O_SEL	<string >	"FALSE","TRUE"	"FALSE"	ana_rx_eq1_r_set_fb_o selection: FALSE: from reg_rx_eq1_r_set_fb; TRUE: from ctle_ctrl_res_i
PMA_REG_ANA_RX_EQ2_R_SET_FB_O_SEL	<string >	"FALSE","TRUE"	"FALSE"	ana_rx_eq2_r_set_fb_o selection: FALSE: from reg_rx_eq2_r_set_fb; TRUE: from ctle_ctrl_res_i
PMA_REG_RX_EQ1_R_SET_TOP	<integer>	0 to 3	0	0,2: 150 ohm 1,3: 110 ohm
PMA_REG_RX_EQ1_R_SET_FB	<integer>	0 to 15	0	eq1 Res fb setting: stage1 eq tuning, 9dB total, 0.5dB/step
PMA_REG_RX_EQ1_C_SET_FB	<integer>	0 to 15	0	ana_rx_eq1_c_set_o setting
PMA_REG_RX_EQ1_OFF	<string >	"FALSE","TRUE"	"FALSE"	Shut off equalisation for 1st stage of EQ1
PMA_REG_RX_EQ2_R_SET_TOP	<integer>	0 to 3	0	0,2: 150 ohm 1,3: 110 ohm
PMA_REG_RX_EQ2_R_SET_FB	<integer>	0 to 15	0	eq1 Res fb setting: stage1 eq tuning, 9dB total, 0.5dB/step
PMA_REG_RX_EQ2_C_SET_FB	<integer>	0 to 15	0	ana_rx_eq2_r_set_o setting
PMA_REG_RX_EQ2_OFF	<string >	"FALSE","TRUE"	"FALSE"	Shut off equalisation for 1st stage of EQ1
PMA_REG_EQ_DAC	<integer>	0 to 63	0	Eq dc offset current dac setting. 0: min setting 63: max setting
PMA_REG_RX_ICTRL_EQ	<integer>	0 to 3	2	Eq base current setting. 0: 87.5% 1: 100% 2: 112.5% 3: 125%
PMA_REG_EQ_DC_C_ALIB_EN	<string >	"FALSE","TRUE"	"FALSE"	Dc calib enable "TRUE": enable "FALSE": disable
PMA_REG_EQ_DC_C_ALIB_SEL	<string >	"FALSE","TRUE"	"FALSE"	Dc offset calib sel. "TRUE": EQ positive output is selected for calib "FALSE": EQ negative output is selected for calib
PMA_REG_RX_RESERVED_337_330	<integer>	0 to 255	0	reg_rx_config_reserved1
PMA_REG_RX_RESERVED_345_338	<integer>	0 to 255	0	reg_rx_config_reserved1
PMA_REG_RX_RESERVED_353_346	<integer>	0 to 255	0	reg_rx_config_reserved1
PMA_REG_RX_RESERVED_361_354	<integer>	0 to 255	0	reg_rx_config_reserved1
PMA_CTLE_CTRL_REG_RG_I	<integer>	0 to 15	0	gain adjustment configuration value read from external register
PMA_CTLE_REG_FOR_CE_SEL_I	<string >	"FALSE","TRUE"	"FALSE"	Selection configuration signal "FALSE": ctle_ctrl_res_o outputs adaptive result

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
				"TRUE": ctle_ctrl_res_o outputs external register configuration value ctle_ctrl_reg_i
PMA_CTLE_REG_HOLD_I	<string>	"FALSE","TRUE"	"FALSE"	Accumulator hold enable signal "FALSE": accumulator operating properly; "TRUE": hold current state
PMA_CTLE_REG_INIT_DAC_I	<integer>	0 to 15	0	Dac Initial Value
PMA_CTLE_REG_POLARITY_I	<string>	"FALSE","TRUE"	"FALSE"	Input Polarity Indicator Signal "FALSE": no polarity inversion; "TRUE": input signal polarity inversion
PMA_CTLE_REG_SHIFTER_GAIN_I	<integer>	0 to 7	0	initial gain setting
PMA_CTLE_REG_THRESHOLD_I	<integer>	0 to 4095	0	threshold value required by lock_detect module used by module
PMA_REG_RX_RES_TRIM_EN	<string>	"FALSE","TRUE"	"FALSE"	Enable PMA_REG_RX_RES_TRIM
PMA_REG_RX_RESERVED_393_389	<integer>	0 to 31	0	reg_rx_config_reserved1
PMA_CFG_RX_LANE_POWERUP	<string>	"ON","OFF"	"OFF"	RX_LANE power-up setting
PMA_CFG_RX_PMA_RSTN	<string>	"FALSE","TRUE"	"FALSE"	RX_PMA reset
PMA_INT_PMA_RX_MASK_0	<string>	"FALSE","TRUE"	"FALSE"	PMA_RX interrupt mask
PMA_INT_PMA_RX_CLR_0	<string>	"FALSE","TRUE"	"FALSE"	PMA_RX interrupt clear
PMA_CFG_CTLE_ADJUST_RSTN	<string>	"FALSE","TRUE"	"TRUE"	reset pin, low active
PMA_REG_TX_PD	<string>	"ON","OFF"	"ON"	transmitter power down 0: transmitter is fully power on 1: transmitter is fully power off
PMA_REG_TX_PD_OW	<string>	"FALSE","TRUE"	"TRUE"	enable tx power down control from register "FALSE": tx power down controlled by pma_tx_pd_x "TRUE": tx power down controlled by reg_tx_pd
PMA_REG_TX_MAIN_PRE_Z	<string>	"FALSE","TRUE"	"FALSE"	Enable EI for PCIE mode; "FALSE": disable EI; "TRUE": enable EI.
PMA_REG_TX_MAIN_PRE_Z_OW	<string>	"FALSE","TRUE"	"FALSE"	Overwrite PMA_REG_TX_MAIN_PRE_Z
PMA_REG_TX_BEACON_TIMER_SEL	<integer>	0 to 3	0	tx beacon timer selection register
PMA_REG_TX_RXDET_REQ_OW	<string>	"FALSE","TRUE"	"FALSE"	Overwrite PMA_REG_TX_RXDET_REQ
PMA_REG_TX_RXDET_REQ	<string>	"FALSE","TRUE"	"FALSE"	RX detection require signal; "FALSE": disable RX detection; "TRUE": enable RX detection.
PMA_REG_TX_BEACON_EN_OW	<string>	"FALSE","TRUE"	"FALSE"	Overwrite PMA_REG_TX_BEACON_EN
PMA_REG_TX_BEACON_EN	<string>	"FALSE","TRUE"	"FALSE"	TX beacon enable signal; "FALSE": Disable beacon;

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
				TRUE": Enable beacon.
PMA_REG_TX_EI_EN_OW	<string >	"FALSE","TRUE"	"FALSE"	Overwrite PMA_REG_TX_EI_EN
PMA_REG_TX_EI_EN	<string >	"FALSE","TRUE"	"FALSE"	tx_ei enable signal "FALSE": no EI "TRUE": EI mode
PMA_REG_TX_BIT_C_ONV	<string >	"FALSE","TRUE"	"FALSE"	set whether the order of tx data_o[19:0] is reversed
PMA_REG_TX_RES_CTRL	<integer>	0 to 63	50	register tx res ctrl code default is 50ohm
PMA_REG_TX_RESERVE_19	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_TX_RESERVE_25_20	<integer>	0 to 63	32	Reserved
PMA_REG_TX_RESERVE_33_26	<integer>	0 to 255	0	Reserved
PMA_REG_TX_RESERVE_41_34	<integer>	0 to 255	0	Reserved
PMA_REG_TX_RESERVE_49_42	<integer>	0 to 255	0	Reserved
PMA_REG_TX_RESERVE_57_50	<integer>	0 to 255	0	Reserved
PMA_REG_TX_SYNC_OW	<string >	"FALSE","TRUE"	"FALSE"	Sync_reg overwrite signal; "FALSE": TX lane sync is controlled by lane_sync; "TRUE": TX lane sync is controlled by tx_sync_reg.
PMA_REG_TX_SYNC	<string >	"FALSE","TRUE"	"FALSE"	Register for TX lane sync control.
PMA_REG_TX_PD_POST	<string >	"ON","OFF"	"OFF"	TX driver state selection;
PMA_REG_TX_PD_POST_OW	<string >	"FALSE","TRUE"	"TRUE"	Overwrite PMA_REG_TX_PD_POST
PMA_REG_TX_RESET_N_OW	<string >	"FALSE","TRUE"	"FALSE"	Overwrite PMA_REG_TX_RESET_N
PMA_REG_TX_RESET_N	<string >	"FALSE","TRUE"	"TRUE"	TX reset signal for clock to digital part; "FALSE": reset clock to digital part to 0; "TRUE": enable clock to digital part.
PMA_REG_TX_RESET_64	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_TX_RESET_65	<string >	"FALSE","TRUE"	"TRUE"	Reserved
PMA_REG_TX_BUSWIDTH_OW	<string >	"FALSE","TRUE"	"FALSE"	Overwrite PMA_REG_TX_BUSWIDTH
PMA_REG_TX_BUSWIDTH	<string >	"8BIT","10BIT","16BIT","20BIT"	"20BIT"	TX buswidth control; "8BIT": 8bit; "10BIT":10bit; "16BIT":16bit; "20BIT":20bit;
PMA_REG_PLL_READY_OW	<string >	"FALSE","TRUE"	"FALSE"	Overwrite PMA_REG_PLL_READY
PMA_REG_PLL_READY	<string >	"FALSE","TRUE"	"TRUE"	PLL ready control signal; "FALSE": PLL is not ready; "TRUE": PLL is ready.

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PMA_REG_TX_RESER_VED_72	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_TX_RESER_VED_73	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_TX_RESER_VED_74	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_EI_PCLK_DELAY_SEL	<integer>	0 to 3	0	Control tx_main_pre_z, tx_post_pre_z, tx_main_bdata, tx_post_bdata delay relative with normal parallel data. 00: 0 pclk cycle, the four signals are synchronized with parallel data. 01: -1 pclk cycle, the four signals are 1 cycle earlier than parallel data. 01: +1 pclk cycle, the four signals are 1 cycle later than parallel data. 11: reserved
PMA_REG_TX_RESER_VED_77	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_TX_RESER_VED_83_78	<integer>	0 to 63	0	Reserved
PMA_REG_TX_RESER_VED_89_84	<integer>	0 to 63	0	Reserved
PMA_REG_TX_RESER_VED_95_90	<integer>	0 to 63	0	Reserved
PMA_REG_TX_RESER_VED_101_96	<integer>	0 to 63	0	Reserved
PMA_REG_TX_RESER_VED_107_102	<integer>	0 to 63	0	Reserved
PMA_REG_TX_RESER_VED_113_108	<integer>	0 to 63	0	Reserved
PMA_REG_TX_AMP_DAC0	<integer>	0 to 63	25	tx full swing bias control, bit 5 reserved
PMA_REG_TX_AMP_DAC1	<integer>	0 to 63	19	tx full swing bias control, bit 5 reserved
PMA_REG_TX_AMP_DAC2	<integer>	0 to 63	14	tx full swing bias control, bit 5 reserved
PMA_REG_TX_AMP_DAC3	<integer>	0 to 63	9	tx full swing bias control, bit 5 reserved
PMA_REG_TX_RESER_VED_143_138	<integer>	0 to 63	5	Reserved
PMA_REG_TX_MARG_IN	<integer>	0 to 7	0	tx margin
PMA_REG_TX_MARG_IN_OW	<string >	"FALSE","TRUE"	"FALSE"	Overwrite PMA_REG_TX_MARGIN, when "TRUE" reg_tx_margin_i replaces pma_tx_margin_i
PMA_REG_TX_RESER_VED_149_148	<integer>	0 to 3	0	Reserved
PMA_REG_TX_RESER_VED_150	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_TX_SWING	<string >	"FALSE","TRUE"	"FALSE"	tx_swing control signal
PMA_REG_TX_SWING_OW	<string >	"FALSE","TRUE"	"FALSE"	Overwrite PMA_REG_TX_SWING

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PMA_REG_TX_RESER_VED_153	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_TX_RXDET_THRESHOLD	<string >	"28MV","56MV","84MV","112MV"	"84MV"	Tx rxdet threshold select; 2'b00: vdda-28mV; 2'b01: vdda-56mV; 2'b10: vdda-84mV; 2'b11: vdda-112mV;
PMA_REG_TX_RESER_VED_157_156	<integer>	0 to 3	0	Reserved
PMA_REG_TX_BEACON_OSC_CTRL	<string >	"FALSE","TRUE"	"FALSE"	beacon osc frequnce ctrl output to tx analog block "TRUE": 18M "FALSE": 36M
PMA_REG_TX_RESER_VED_160_159	<integer>	0 to 3	0	Reserved
PMA_REG_TX_RESER_VED_162_161	<integer>	0 to 3	0	Reserved
PMA_REG_TX_RX2RX_SLPBACK_EN	<string >	"FALSE","TRUE"	"FALSE"	Enable PMA_REG_TX_RX2RX_SLPBACK
PMA_REG_TX_PCLK_EDGE_SEL	<string >	"FALSE","TRUE"	"FALSE"	rx pclk edge select: "TRUE": rx_pdata is clocked out to Tx on the falling edge of rxpclk "FALSE": rx_pdata is clocked out to Tx on the rising edge of rxpclk
PMA_REG_TX_RXDET_STATUS_OW	<string >	"FALSE","TRUE"	"FALSE"	Overwrite PMA_REG_TX_RXDET_STATUS
PMA_REG_TX_RXDET_STATUS	<string >	"FALSE","TRUE"	"TRUE"	RX detection status; "FALSE": RX is not detected(TX output terminal is floating); "TRUE": RX detected(50-ohm termination);
PMA_REG_TX_PRBS_GEN_EN	<string >	"FALSE","TRUE"	"FALSE"	Enable PMA_REG_TX_PRBS_GEN
PMA_REG_TX_PRBS_GEN_WIDTH_SEL	<string >	"8BIT","10BIT","16BIT","20BIT"	"20BIT"	PRBS width select
PMA_REG_TX_PRBS_SEL	<string >	"PRBS7","PRBS15","PRBS23","PRBS31"	"PRBS7"	PRBS pattern select
PMA_REG_TX_UDP_D ATA_7_TO_0	<integer>	0 to 255	5	constant 20-bit pattern, default = K28.5
PMA_REG_TX_UDP_D ATA_15_TO_8	<integer>	0 to 255	235	constant 20-bit pattern, default = K28.5
PMA_REG_TX_UDP_D ATA_19_TO_16	<integer>	0 to 15	3	constant 20-bit pattern, default = K28.5
PMA_REG_TX_RESER_VED_192	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_TX_FIFO_WP_CTRL	<integer>	0 to 7	4	fifo write probe to ctrl distance write probe to read probe
PMA_REG_TX_FIFO_EN	<string >	"FALSE","TRUE"	"FALSE"	Enable PMA_REG_TX_FIFO
PMA_REG_TX_DATA_MUX_SEL	<integer>	0 to 3	0	parallel data mux select to select different data source 00: data from pcs 01: prbs bist data 10: udp data

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
				11: rx loopback data
PMA_REG_TX_ERR_INSER T	<string >	"FALSE","TRUE"	"FALSE"	tx error insertion add an error at reg_tx_err_ins riseedge in txpdata_order[0]
PMA_REG_TX_RESERVED_203_200	<integer>	0 to15	0	Reserved
PMA_REG_TX_RESERVED_204	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_TX_SATA_EN	<string >	"FALSE","TRUE"	"FALSE"	SATA mode enable register "FALSE": SATA mode is disabled. "TRUE": SATA mode is enabled. This register is combined with pma_tx_ei_en_x to determine whether normal EI mode or OOB_EI mode valid only for SATA is active.
PMA_REG_TX_RESERVED_207_206	<integer>	0 to3	0	Reserved
PMA_REG_RATE_CHANNEL_TXPCLK_ON_O W	<string >	"FALSE","TRUE"	"FALSE"	Rate_change_txpclk_on overwrite signal; "FALSE": txpclk enable signal is controlled by rate_change_txpclk_on; "TRUE": txpclk enable signal is controlled by rate_change_txpclk_on_reg.
PMA_REG_RATE_CHANNEL_TXPCLK_ON	<string >	"FALSE","TRUE"	"TRUE"	txpclk enable signal when rate changes "FALSE": txpclk is gated off during rate change "TRUE": txpclk is on
PMA_REG_TX_CFG_POST1	<integer>	0 to 31	0	based on tx_deemp setting, the selection source of ana_tx_cfg_post_o output
PMA_REG_TX_CFG_POST2	<integer>	0 to 31	0	based on tx_deemp setting, the selection source of ana_tx_cfg_post_o output
PMA_REG_TX_DEEMP	<integer>	0 to 3	0	tx_deemp control register tx_deemp_s is an internal signal, when reg_tx_deemp_ow_i is 1, tx_deemp_s is from reg_tx_deemp; when reg_tx_deemp_ow_i is 0, tx_deemp_s is from pma_tx_deemp_i; when tx_deemp_s is, 00: ana_tx_cfg_post_o is from reg_tx_cfg_post; 01: ana_tx_cfg_post_o is from reg_tx_cfg_post1; 10: ana_tx_cfg_post_o is from reg_tx_cfg_post2; 11: ana_tx_cfg_post_o is from reg_tx_cfg_post.
PMA_REG_TX_DEEMP_O W	<string >	"FALSE","TRUE"	"FALSE"	Overwrite PMA_REG_TX_DEEMP TRUE: tx_deemp is controlled by

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
				reg_tx_deemp FALSE: tx_deemp is controlled by pma_tx_deemp
PMA_REG_TX_RESERVED_224_223	<integer>	0 to 3	0	Reserved
PMA_REG_TX_RESERVED_225	<string>	"FALSE", "TRUE"	"FALSE"	Reserved
PMA_REG_TX_RESERVED_229_226	<integer>	0 to 15	0	Reserved
PMA_REG_TX_OOB_DELAY_SEL	<integer>	0 to 15	0	controls the oob ei enable signal delay steps to compensate data latency. xx00: 0 pclk cycle, tx_oob_ei_en is synchronized with parallel data. xx01: -1 pclk cycle, tx_oob_ei_en is 1 cycle earlier than parallel data. xx10: +1 pclk cycle, tx_oob_ei_en is 1 cycle later than parallel data. others: reserved
PMA_REG_TX_POLARITY	<string>	"NORMAL", "REVERSE"	"NORMAL"	Invert input parallel data; "NORMAL": txpdata_out[19:0]=txpdata_in[19:0]; "REVERSE": txpdata_out[19:0]=~txpdata_in[19:0].
PMA_REG_ANA_TX_JTAG_DATA_O_SEL	<string>	"FALSE", "TRUE"	"FALSE"	jtag_mode data tx selection: TRUE: from reg_tx_jtag_data; FALSE: from pma_tx_jtag_data_i;
PMA_REG_TX_RESERVED_236	<string>	"FALSE", "TRUE"	"FALSE"	Reserved
PMA_REG_TX_LS_MODE_EN	<string>	"FALSE", "TRUE"	"FALSE"	Enable Low-speed mode; "FALSE": Disable low-speed mode; "TRUE": Enable low-speed mode.
PMA_REG_TX_JTAG_MODE_EN_OW	<string>	"FALSE", "TRUE"	"FALSE"	Overwrite PMA_REG_TX_JTAG_MODE_EN, when "TRUE" reg_tx_jtag_mode_en_i replaces pma_tx_jtag_mode_en_i
PMA_REG_TX_JTAG_MODE_EN	<string>	"FALSE", "TRUE"	"FALSE"	rx JTAG enable signal. Receiver can enter AC JTAG mode by asserting this pin high.
PMA_REG_RX_JTAG_MODE_EN_OW	<string>	"FALSE", "TRUE"	"FALSE"	Overwrite PMA_REG_RX_JTAG_MODE_EN
PMA_REG_RX_JTAG_MODE_EN	<string>	"FALSE", "TRUE"	"FALSE"	rx JTAG enable signal. Receiver can enter AC JTAG mode by asserting this pin high.
PMA_REG_RX_JTAG_OE	<string>	"FALSE", "TRUE"	"TRUE"	rx jtag module enable register "FALSE": disabled; "TRUE": enable
PMA_REG_RX_ACJTAG_VHYSTSEL	<integer>	0 to 7	0	rx acjtag hysteresis voltage control register 00:60mV;01=120mV 10:180mV;11=240mV b<2>=1, increase the RC time.
PMA_REG_TX_RES_CAL_EN	<string>	"FALSE", "TRUE"	"FALSE"	Enable PMA_REG_TX_RES_CAL

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PMA_REG_RX_TERM_MODE_CTRL	<integer>	0 to 7	4	rx terminatin working mode control register [2](default1'b1): 0: on-chip commom bias is disable for EQ input; 1: on-chip commom bias is enable for EQ input; [1](default1'b0): 0: on-chip ac couple is enable; 1: on-chip ac couple is disable; [0](default1'b0): 0: P/N bridge; 1: terminate to ground;
PMA_REG_TX_RESERVED_251_250	<integer>	0 to 7	0	Reserved
PMA_REG_PLPBK_TX_PCLK_EN	<string >	"FALSE","TRUE"	"FALSE"	Enable PMA_REG_PLPBK_TXPCLK
PMA_REG_TX_RESERVED_253	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_TX_RESERVED_254	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_TX_RESERVED_255	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_TX_RESERVED_256	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_TX_RESERVED_257	<string >	"FALSE","TRUE"	"FALSE"	Reserved
PMA_REG_TX_PH_SEL	<integer>	0 to 63	1	TX PISO sample clock phase selection.
PMA_REG_TX_CFG_PRE	<integer>	0 to 31	0	pre cursor tap coefficient.
PMA_REG_TX_CFG_MAIN	<integer>	0 to 63	0	main cursor tap coefficient.
PMA_REG_CFG_POST	<integer>	0 to 31	0	post cursor tap coefficient.
PMA_REG_PD_MAIN	<string >	"FALSE","TRUE"	"TRUE"	TX driver state selection;
PMA_REG_PD_PRE	<string >	"FALSE","TRUE"	"TRUE"	TX driver state selection;
PMA_REG_TX_LS_DATA	<string >	"FALSE","TRUE"	"FALSE"	tx low speed signal input
PMA_REG_TX_DCC_BUFFER_SIZE_SEL	<integer>	0 to 3	0	Buffer size selection for input clock; 0: for 2GHz clock; 3: for 8GHz clock.
PMA_REG_TX_DCC_CAL_CUR_TUNE	<integer>	0 to 63	0	Rising/falling tuning configuration for DCC.
PMA_REG_TX_DCC_CAL_EN	<string >	"FALSE","TRUE"	"FALSE"	Duty cycle calibration enable; "FALSE": Disable duty cycle calibration; "TRUE": Enable duty cycle calibration.
PMA_REG_TX_DCC_CUR_SS	<integer>	0 to 3	0	Current control of DCC for SS corner; 0: for other corner; 3: for SS corner.
PMA_REG_TX_DCC_FA_CTRL	<string >	"FALSE","TRUE"	"FALSE"	Enable falling tuning configuration for DCC;

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
				"FALSE": disable falling tuning configuration; "TRUE": enable falling tuning configuration.
PMA_REG_TX_DCC_R_I_CTRL	<string>	"FALSE", "TRUE"	"FALSE"	Enable rising tuning configuration for DCC; "FALSE": disable rising tuning configuration; "TRUE": enable rising tuning configuration.
PMA_REG_ATB_SEL_2_TO_0	<integer>	0 to 7	0	Analog test selection.
PMA_REG_ATB_SEL_9_TO_3	<integer>	0 to 127	0	Analog test selection.
PMA_REG_TX_CFG_7_TO_0	<integer>	0 to 255	0	Reserved.
PMA_REG_TX_CFG_15_TO_8	<integer>	0 to 255	0	Reserved.
PMA_REG_TX_CFG_23_TO_16	<integer>	0 to 255	0	Reserved.
PMA_REG_TX_CFG_31_TO_24	<integer>	0 to 255	0	when reg_tx_cfg_31_to_24[7] is 1, ana_tx_pd_driver_o is from pma_tx_pd_driver_o; when reg_tx_cfg_31_to_24[7] is 0, ana_tx_pd_driver_o is from reg_tx_cfg_31_to_24[6]
PMA_REG_TX_OOB_EI_EN	<string>	"FALSE", "TRUE"	"FALSE"	OOB and EI mode enable signal Enable OOB EI for SATA mode; "FALSE": disable OOB EI; "TRUE": enable OOB EI.
PMA_REG_TX_OOB_EI_EN_OW	<string>	"FALSE", "TRUE"	"FALSE"	Overwrite PMA_REG_TX_OOB_EI_EN
PMA_REG_TX_BEACON_EN_DELAYED	<string>	"FALSE", "TRUE"	"FALSE"	Beacon mode enable signal with delay. "FALSE": Disable beacon mode; "TRUE": Enable beacon mode.
PMA_REG_TX_BEACON_EN_DELAYED_OW	<string>	"FALSE", "TRUE"	"FALSE"	Overwrite PMA_REG_TX_BEACON_EN_DELAYED
PMA_REG_TX_JTAG_DATA	<string>	"FALSE", "TRUE"	"FALSE"	Input data when TX working in jtag mode.
PMA_REG_TX_RXDET_TIMER_SEL	<integer>	0 to 255	87	register enable rx detect sample waiting time control. the sampling point delay is selected by reg_tx_rxdet_timer_sel (delay is reg_tx_rxdet_timer_sel + 4 pll_refclk cycles)
PMA_REG_TX_CFG1_7_0	<integer>	0 to 255	0	Reserved.
PMA_REG_TX_CFG1_15_8	<integer>	0 to 255	0	Reserved.
PMA_REG_TX_CFG1_23_16	<integer>	0 to 255	0	Reserved.
PMA_REG_TX_CFG1_31_24	<integer>	0 to 255	0	Reserved.

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PMA_REG_CFG_LAN_E_POWERUP	<string >	"OFF","ON"	"OFF"	This parameter controls the powerup of PMA_LANE
PMA_REG_CFG_TX_LANE_POWERUP_CLK_PATH	<string >	"FALSE","TRUE"	"FALSE"	Pma tx lane clkpath powerup
PMA_REG_CFG_TX_LANE_POWERUP_PISO	<string >	"FALSE","TRUE"	"FALSE"	Pma tx lane piso powerup
PMA_REG_CFG_TX_LANE_POWERUP_DRI	<string >	"FALSE","TRUE"	"FALSE"	Pma tx lane driver powerup
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Note:

1. The parameter values FALSE and TRUE correspond to signal values 0 and 1, respectively;
2. Parameters with values "ON" and "OFF" are all power control parameters. According to the parameters being powerdown or powerup, the corresponding SC conversion differs. However, the parameter value "ON" corresponds to power being present, while "OFF" corresponds to power being absent.

10.6.5 Instantiation Template

```
GTP_HSSTLP_LANE #(
    .MUX_BIAS(2),
    .PD_CLK(0),
    .REG_SYNC(0),
    .REG_SYNC_OW(0),
    .PLL_LOCK_OW(0),
    .PLL_LOCK_OW_EN(0),
    .PCS_SLAVE(0),
    .PCS_BYPASS_WORD_ALIGN("FALSE"),
    .PCS_BYPASS_DENC("FALSE"),
    .PCS_BYPASS_BONDING("FALSE"),
    .PCS_BYPASS_CTC("FALSE"),
    .PCS_BYPASS_GEAR("FALSE"),
    .PCS_BYPASS_BRIDGE("FALSE"),
    .PCS_BYPASS_BRIDGE_FIFO("FALSE"),
    .PCS_DATA_MODE("X8"),
    .PCS_RX_POLARITY_INV("DELAY"),
    .PCS_ALIGN_MODE("1GB"),
    .PCS_SAMP_16B("X20"),
    .PCS_FARLP_PWR_REDUCTION("FALSE"),
    .PCS_COMM_REG0(0),
```

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.PCS_COMMAMASK(0),
.PCS_CEB_MODE("10GB"),
.PCS_CTC_MODE("1SKIP"),
.PCS_A_REG(0),
.PCS_GEAUTO_EN("FALSE"),
.PCS_SKIP_REG0(0),
.PCS_SKIP_REG1(0),
.PCS_SKIP_REG2(0),
.PCS_SKIP_REG3(0),
.PCS_DEC_DUAL("FALSE"),
.PCS_SPLIT("FALSE"),
.PCS_FIFOFLAG_CTC("FALSE"),
.PCS_COMMADET_MODE("COMMA_PATTERN"),
.PCS_ERRDETECT_SILENCE("FALSE"),
.PCS_PMA_RCLK_POLINV("PMA_RCLK"),
.PCS_PCS_RCLK_SEL("PMA_RCLK"),
.PCS_CB_RCLK_SEL("PMA_RCLK"),
.PCS_AFTER_CTC_RCLK_SEL("PMA_RCLK"),
.PCS_RCLK_POLINV("RCLK"),
.PCS_BRIDGE_RCLK_SEL("PMA_RCLK"),
.PCS_PCS_RCLK_EN("FALSE"),
.PCS_CB_RCLK_EN("FALSE"),
.PCS_AFTER_CTC_RCLK_EN("FALSE"),
.PCS_AFTER_CTC_RCLK_EN_GB("FALSE"),
.PCS_PCS_RX_RSTN("FALSE"),
.PCS_PCIE_SLAVE("MASTER"),
.PCS_RX_64B66B_67B("NORMAL"),
.PCS_RX_BRIDGE_CLK_POLINV("RX_BRIDGE_CLK"),
.PCS_PCS_CB_RSTN("FALSE"),
.PCS_TX_BRIDGE_GEAR_SEL("FALSE"),
.PCS_TX_BYPASS_BRIDGE_UINT("FALSE"),
.PCS_TX_BYPASS_BRIDGE_FIFO("FALSE"),
.PCS_TX_BYPASS_GEAR("FALSE"),
.PCS_TX_BYPASS_ENC("FALSE"),
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.PCS_TX_BYPASS_BIT_SLIP("FALSE"),
.PCS_TX_GEAR_SPLIT("FALSE"),
.PCS_TX_DRIVE_REG_MODE("NO_CHANGE"),
.PCS_TX_BIT_SLIP_CYCLES(0),
.PCS_INT_TX_MASK_0("FALSE"),
.PCS_INT_TX_MASK_1("FALSE"),
.PCS_INT_TX_MASK_2("FALSE"),
.PCS_INT_TX_CLR_0("FALSE"),
.PCS_INT_TX_CLR_1("FALSE"),
.PCS_INT_TX_CLR_2("FALSE"),
.PCS_TX_PMA_TCLK_POLINV("PMA_TCLK"),
.PCS_TX_PCS_CLK_EN_SEL("FALSE"),
.PCS_TX_BRIDGE_TCLK_SEL("TCLK"),
.PCS_TX_TCLK_POLINV("TCLK"),
.PCS_PCS_TCLK_SEL("PMA_TCLK"),
.PCS_TX_PCS_TX_RSTN("FALSE"),
.PCS_TX_SLAVE("MASTER"),
.PCS_TX_GEAR_CLK_EN_SEL("FALSE"),
.PCS_DATA_WIDTH_MODE("X20"),
.PCS_TX_64B66B_67B("NORMAL"),
.PCS_GEAR_TCLK_SEL("PMA_TCLK"),
.PCS_TX_TCLK2FABRIC_SEL("FALSE"),
.PCS_TX_OUTZZ("FALSE"),
.PCS_ENC_DUAL("FALSE"),
.PCS_TX_BITSLIP_DATA_MODE("X10"),
.PCS_TX_BRIDGE_CLK_POLINV("TX_BRIDGE_CLK"),
.PCS_COMMA_REG1(0),
.PCS_RAPID_IMAX(0),
.PCS_RAPID_VMIN_1(0),
.PCS_RAPID_VMIN_2(0),
.PCS_RX_PRBS_MODE("DISABLE"),
.PCS_RX_ERRCNT_CLR("FALSE"),
.PCS_PRBS_ERR_LPBK("FALSE"),
.PCS_TX_PRBS_MODE("DISABLE"),
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.PCS_TX_INSERT_ER("FALSE"),
.PCS_ENABLE_PRBS_GEN("FALSE"),
.PCS_DEFAULT_RADDR(0),
.PCS_MASTER_CHECK_OFFSET(0),
.PCS_DELAY_SET(0),
.PCS_SEACH_OFFSET("20BIT"),
.PCS_CEB_RAPIDLS_MMAX(0),
.PCS_CTC_AFULL(20),
.PCS_CTC_AEMPTY(12),
.PCS_CTC_CONTI_SKP_SET(0),
.PCS_FAR_LOOP("FALSE"),
.PCS_NEAR_LOOP("FALSE"),
.PCS_PMA_TX2RX_PLOOP_EN("FALSE"),
.PCS_PMA_RX2TX_PLOOP_EN("FALSE"),
.PCS_PMA_RX2TX_PLOOP_EN("FALSE"),
.PCS_INT_RX_MASK_0("FALSE"),
.PCS_INT_RX_MASK_1("FALSE"),
.PCS_INT_RX_MASK_2("FALSE"),
.PCS_INT_RX_MASK_3("FALSE"),
.PCS_INT_RX_MASK_4("FALSE"),
.PCS_INT_RX_MASK_5("FALSE"),
.PCS_INT_RX_MASK_6("FALSE"),
.PCS_INT_RX_MASK_7("FALSE"),
.PCS_INT_RX_CLR_0("FALSE"),
.PCS_INT_RX_CLR_1("FALSE"),
.PCS_INT_RX_CLR_2("FALSE"),
.PCS_INT_RX_CLR_3("FALSE"),
.PCS_INT_RX_CLR_4("FALSE"),
.PCS_INT_RX_CLR_5("FALSE"),
.PCS_INT_RX_CLR_6("FALSE"),
.PCS_INT_RX_CLR_7("FALSE"),
.PCS_CA_RSTN_RX("FALSE"),
.PCS_CA_DYN_DLY_EN_RX("FALSE"),
.PCS_CA_DYN_DLY_SEL_RX("FALSE"),
```

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.PCS_CA_RX(0),  
.PCS_CA_RSTN_TX("FALSE"),  
.PCS_CA_DYN_DLY_EN_TX("FALSE"),  
.PCS_CA_DYN_DLY_SEL_TX("FALSE"),  
.PCS_CA_TX(0),  
.PCS_RXPRBS_PWR_REDUCTION("NORMAL"),  
.PCS_WDALIGN_PWR_REDUCTION("NORMAL"),  
.PCS_RXDEC_PWR_REDUCTION("NORMAL"),  
.PCS_RXCB_PWR_REDUCTION("NORMAL"),  
.PCS_RXCTC_PWR_REDUCTION("NORMAL"),  
.PCS_RXGEAR_PWR_REDUCTION("NORMAL"),  
.PCS_RXBRG_PWR_REDUCTION("NORMAL"),  
.PCS_RXTEST_PWR_REDUCTION("NORMAL"),  
.PCS_TXBRG_PWR_REDUCTION("NORMAL"),  
.PCS_TXGEAR_PWR_REDUCTION("NORMAL"),  
.PCS_TXENC_PWR_REDUCTION("NORMAL"),  
.PCS_TXBSLP_PWR_REDUCTION("NORMAL"),  
.PCS_TXPRBS_PWR_REDUCTION("NORMAL"),  
.PMA_REG_RX_PD("ON"),  
.PMA_REG_RX_PD_EN("FALSE"),  
.PMA_REG_RX_RESERVED_2("FALSE"),  
.PMA_REG_RX_RESERVED_3("FALSE"),  
.PMA_REG_RX_DATAPATH_PD("ON"),  
.PMA_REG_RX_DATAPATH_PD_EN("FALSE"),  
.PMA_REG_RX_SIGDET_PD("ON"),  
.PMA_REG_RX_SIGDET_PD_EN("FALSE"),  
.PMA_REG_RX_DCC_RST_N("TRUE"),  
.PMA_REG_RX_DCC_RST_N_EN("FALSE"),  
.PMA_REG_RX_CDR_RST_N("TRUE"),  
.PMA_REG_RX_CDR_RST_N_EN("FALSE"),  
.PMA_REG_RX_SIGDET_RST_N("TRUE"),  
.PMA_REG_RX_SIGDET_RST_N_EN("FALSE"),  
.PMA_REG_RXPCLK_SLIP("FALSE"),  
.PMA_REG_RXPCLK_SLIP_OW("FALSE"),
```

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.PMA_REG_RX_PCLKSWITCH_RST_N("TRUE"),
.PMA_REG_RX_PCLKSWITCH_RST_N_EN("FALSE"),
.PMA_REG_RX_PCLKSWITCH("FALSE"),
.PMA_REG_RX_PCLKSWITCH_EN("FALSE"),
.PMA_REG_RX_HIGHZ("FALSE"),
.PMA_REG_RX_HIGHZ_EN("FALSE"),
.PMA_REG_RX_SIGDET_CLK_WINDOW("FALSE"),
.PMA_REG_RX_SIGDET_CLK_WINDOW_OW("FALSE"),
.PMA_REG_RX_PD_BIAS_RX("FALSE"),
.PMA_REG_RX_PD_BIAS_RX_OW("FALSE"),
.PMA_REG_RX_RESET_N("FALSE"),
.PMA_REG_RX_RESET_N_OW("FALSE"),
.PMA_REG_RX_RESERVED_29_28(0),
.PMA_REG_RX_BUSWIDTH("20BIT"),
.PMA_REG_RX_BUSWIDTH_EN("FALSE"),
.PMA_REG_RX_RATE("DIV1"),
.PMA_REG_RX_RESERVED_36("FALSE"),
.PMA_REG_RX_RATE_EN("FALSE"),
.PMA_REG_RX_RES_TRIM(46),
.PMA_REG_RX_RESERVED_44("FALSE"),
.PMA_REG_RX_RESERVED_45("FALSE"),
.PMA_REG_RX_SIGDET_STATUS_EN("FALSE"),
.PMA_REG_RX_RESERVED_48_47(0),
.PMA_REG_RX_ICTRL_SIGDET(5),
.PMA_REG_CDR_READY_THD(2734),
.PMA_REG_RX_RESERVED_65("FALSE"),
.PMA_REG_RX_PCLK_EDGE_SEL("POS_EDGE"),
.PMA_REG_RX_PIBUF_IC(1),
.PMA_REG_RX_RESERVED_69("FALSE"),
.PMA_REG_RX_DCC_IC_RX(1),
.PMA_REG_CDR_READY_CHECK_CTRL(0),
.PMA_REG_RX_ICTRL_TRX("100PCT"),
.PMA_REG_RX_RESERVED_77_76(0),
.PMA_REG_RX_RESERVED_79_78(1),
```

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.PMA_REG_RX_RESERVED_81_80(1),  
.PMA_REG_RX_ICTRL_PIBUF("100PCT"),  
.PMA_REG_RX_ICTRL_PI("100PCT"),  
.PMA_REG_RX_ICTRL_DCC("100PCT"),  
.PMA_REG_RX_RESERVED_89_88(1),  
.PMA_REG_TX_RATE("DIV1"),  
.PMA_REG_RX_RESERVED_92("FALSE"),  
.PMA_REG_TX_RATE_EN("FALSE"),  
.PMA_REG_RX_TX2RX_PLPBK_RST_N("TRUE"),  
.PMA_REG_RX_TX2RX_PLPBK_RST_N_EN("FALSE"),  
.PMA_REG_RX_TX2RX_PLPBK_EN("FALSE"),  
.PMA_REG_TXCLK_SEL("PLL"),  
.PMA_REG_RX_DATA_POLARITY("NORMAL"),  
.PMA_REG_RX_ERR_INSERT("FALSE"),  
.PMA_REG_UDP_CHK_EN("FALSE"),  
.PMA_REG_PRBS_SEL("PRBS7"),  
.PMA_REG_PRBS_CHK_EN("FALSE"),  
.PMA_REG_PRBS_CHK_WIDTH_SEL("20BIT"),  
.PMA_REG_BIST_CHK_PAT_SEL("PRBS"),  
.PMA_REG_LOAD_ERR_CNT("FALSE"),  
.PMA_REG_CHK_COUNTER_EN("FALSE"),  
.PMA_REG_CDR_PROP_GAIN(7),  
.PMA_REG_CDR_PROP_TURBO_GAIN(5),  
.PMA_REG_CDR_INT_GAIN(7),  
.PMA_REG_CDR_INT_TURBO_GAIN(5),  
.PMA_REG_CDR_INT_SAT_MAX(768),  
.PMA_REG_CDR_INT_SAT_MIN(255),  
.PMA_REG_CDR_INT_RST("FALSE"),  
.PMA_REG_CDR_INT_RST_OW("FALSE"),  
.PMA_REG_CDR_PROP_RST("FALSE"),  
.PMA_REG_CDR_PROP_RST_OW("FALSE"),  
.PMA_REG_CDR_LOCK_RST("FALSE"),  
.PMA_REG_CDR_LOCK_RST_OW("FALSE"),  
.PMA_REG_CDR_RX_PI_FORCE_SEL(0),
```

```
.PMA_REG_CDR_RX_PI_FORCE_D(0),
.PMA_REG_CDR_LOCK_TIMER("1_2U"),
.PMA_REG_CDR_TURBO_MODE_TIMER(1),
.PMA_REG_CDR_LOCK_VAL("FALSE"),
.PMA_REG_CDR_LOCK_OW("FALSE"),
.PMA_REG_CDR_INT_SAT_DET_EN("TRUE"),
.PMA_REG_CDR_SAT_AUTO_DIS("TRUE"),
.PMA_REG_CDR_GAIN_AUTO("FALSE"),
.PMA_REG_CDR_TURBO_GAIN_AUTO("FALSE"),
.PMA_REG_RX_RESERVED_171_167(0),
.PMA_REG_RX_RESERVED_175_172(0),
.PMA_REG_CDR_SAT_DET_STATUS_EN("FALSE"),
.PMA_REG_CDR_SAT_DET_STATUS_RESET_EN("FALSE"),
.PMA_REG_CDR_PI_CTRL_RST("FALSE"),
.PMA_REG_CDR_PI_CTRL_RST_OW("FALSE"),
.PMA_REG_CDR_SAT_DET_RST("FALSE"),
.PMA_REG_CDR_SAT_DET_RST_OW("FALSE"),
.PMA_REG_CDR_SAT_DET_STICKY_RST("FALSE"),
.PMA_REG_CDR_SAT_DET_STICKY_RST_OW("FALSE"),
.PMA_REG_CDR_SIGDET_STATUS_DIS("FALSE"),
.PMA_REG_CDR_SAT_DET_TIMER(2),
.PMA_REG_CDR_SAT_DET_STATUS_VAL("FALSE"),
.PMA_REG_CDR_SAT_DET_STATUS_OW("FALSE"),
.PMA_REG_CDR_TURBO_MODE_EN("TRUE"),
.PMA_REG_RX_RESERVED_190("FALSE"),
.PMA_REG_RX_RESERVED_193_191(0),
.PMA_REG_CDR_STATUS_FIFO_EN("TRUE"),
.PMA_REG_PMA_TEST_SEL(0),
.PMA_REG_OOB_COMWAKE_GAP_MIN(3),
.PMA_REG_OOB_COMWAKE_GAP_MAX(11),
.PMA_REG_OOB_COMINIT_GAP_MIN(15),
.PMA_REG_OOB_COMINIT_GAP_MAX(35),
.PMA_REG_RX_RESERVED_227_226(1),
.PMA_REG_COMWAKE_STATUS_CLEAR(0),
```

```
.PMA_REG_COMINIT_STATUS_CLEAR(0),
.PMA_REG_RX_SYNC_RST_N_EN("FALSE"),
.PMA_REG_RX_SYNC_RST_N("TRUE"),
.PMA_REG_RX_RESERVED_233_232(0),
.PMA_REG_RX_RESERVED_235_234(0),
.PMA_REG_RX_SATA_COMINIT_OW("FALSE"),
.PMA_REG_RX_SATA_COMINIT("FALSE"),
.PMA_REG_RX_SATA_COMWAKE_OW("FALSE"),
.PMA_REG_RX_SATA_COMWAKE("FALSE"),
.PMA_REG_RX_RESERVED_241_240(0),
.PMA_REG_RX_DCC_DISABLE("FALSE"),
.PMA_REG_RX_RESERVED_243("FALSE"),
.PMA_REG_RX_SLIP_SEL_EN("FALSE"),
.PMA_REG_RX_SLIP_SEL(0),
.PMA_REG_RX_SLIP_EN("FALSE"),
.PMA_REG_RX_SIGDET_STATUS_SEL(5),
.PMA_REG_RX_SIGDET_FSM_RST_N("TRUE"),
.PMA_REG_RX_RESERVED_254("FALSE"),
.PMA_REG_RX_SIGDET_STATUS("FALSE"),
.PMA_REG_RX_SIGDET_VTH("27MV"),
.PMA_REG_RX_SIGDET_GRM(0),
.PMA_REG_RX_SIGDET_PULSE_EXT("FALSE"),
.PMA_REG_RX_SIGDET_CH2_SEL(0),
.PMA_REG_RX_SIGDET_CH2_CHK_WINDOW(3),
.PMA_REG_RX_SIGDET_CHK_WINDOW_EN("TRUE"),
.PMA_REG_RX_SIGDET_NOSIG_COUNT_SETTING(4),
.PMA_REG_SLIP_FIFO_INV_EN("FALSE"),
.PMA_REG_SLIP_FIFO_INV("POS_EDGE"),
.PMA_REG_RX_SIGDET_OOB_DET_COUNT_VAL(0),
.PMA_REG_RX_SIGDET_4OOB_DET_SEL(7),
.PMA_REG_RX_RESERVED_285_283(0),
.PMA_REG_RX_RESERVED_286("FALSE"),
.PMA_REG_RX_SIGDET_IC_I(10),
.PMA_REG_RX_OOB_DETECTOR_RESET_N_OW("FALSE"),
```

```
.PMA_REG_RX_OOB_DETECTOR_RESET_N("FALSE"),
.PMA_REG_RX_OOB_DETECTOR_PD_OW("FALSE"),
.PMA_REG_RX_OOB_DETECTOR_PD("ON"),
.PMA_REG_RX_LS_MODE_EN("FALSE"),
.PMA_REG_ANA_RX_EQ1_R_SET_FB_O_SEL("FALSE"),
.PMA_REG_ANA_RX_EQ2_R_SET_FB_O_SEL("FALSE"),
.PMA_REG_RX_EQ1_R_SET_TOP(0),
.PMA_REG_RX_EQ1_R_SET_FB(0),
.PMA_REG_RX_EQ1_C_SET_FB(0),
.PMA_REG_RX_EQ1_OFF("FALSE"),
.PMA_REG_RX_EQ2_R_SET_TOP(0),
.PMA_REG_RX_EQ2_R_SET_FB(0),
.PMA_REG_RX_EQ2_C_SET_FB(0),
.PMA_REG_RX_EQ2_OFF("FALSE"),
.PMA_REG_EQ_DAC(0),
.PMA_REG_RX_ICTRL_EQ(2),
.PMA_REG_EQ_DC_CALIB_EN("FALSE"),
.PMA_REG_EQ_DC_CALIB_SEL("FALSE"),
.PMA_REG_RX_RESERVED_337_330(0),
.PMA_REG_RX_RESERVED_345_338(0),
.PMA_REG_RX_RESERVED_353_346(0),
.PMA_REG_RX_RESERVED_361_354(0),
.PMA_CTLE_CTRL_REG_I(0),
.PMA_CTLE_REG_FORCE_SEL_I("FALSE"),
.PMA_CTLE_REG_HOLD_I("FALSE"),
.PMA_CTLE_REG_INIT_DAC_I(0),
.PMA_CTLE_REG_POLARITY_I("FALSE"),
.PMA_CTLE_REG_SHIFTER_GAIN_I(0),
.PMA_CTLE_REG_THRESHOLD_I(0),
.PMA_REG_RX_RES_TRIM_EN("FALSE"),
.PMA_REG_RX_RESERVED_393_389(0),
.PMA_CFG_RX_LANE_POWERUP("OFF"),
.PMA_CFG_RX_PMA_RSTN("FALSE"),
.PMA_INT_PMA_RX_MASK_0("FALSE"),
```

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.PMA_INT_PMA_RX_CLR_0("FALSE"),
.PMA_CFG_CTLE_ADP_RSTN("TRUE"),
.PMA_REG_TX_PD("ON"),
.PMA_REG_TX_PD_OW("TRUE"),
.PMA_REG_TX_MAIN_PRE_Z("FALSE"),
.PMA_REG_TX_MAIN_PRE_Z_OW("FALSE"),
.PMA_REG_TX_BEACON_TIMER_SEL(0),
.PMA_REG_TX_RXDET_REQ_OW("FALSE"),
.PMA_REG_TX_RXDET_REQ("FALSE"),
.PMA_REG_TX_BEACON_EN_OW("FALSE"),
.PMA_REG_TX_BEACON_EN("FALSE"),
.PMA_REG_TX_EI_EN_OW("FALSE"),
.PMA_REG_TX_EI_EN("FALSE"),
.PMA_REG_TX_BIT_CONV("FALSE"),
.PMA_REG_TX_RES_CAL(50),
.PMA_REG_TX_RESERVED_19("FALSE"),
.PMA_REG_TX_RESERVED_25_20(32),
.PMA_REG_TX_RESERVED_33_26(0),
.PMA_REG_TX_RESERVED_41_34(0),
.PMA_REG_TX_RESERVED_49_42(0),
.PMA_REG_TX_RESERVED_57_50(0),
.PMA_REG_TX_SYNC_OW("FALSE"),
.PMA_REG_TX_SYNC("FALSE"),
.PMA_REG_TX_PD_POST("OFF"),
.PMA_REG_TX_PD_POST_OW("TRUE"),
.PMA_REG_TX_RESET_N_OW("FALSE"),
.PMA_REG_TX_RESET_N("TRUE"),
.PMA_REG_TX_RESERVED_64("FALSE"),
.PMA_REG_TX_RESERVED_65("TRUE"),
.PMA_REG_TX_BUSWIDTH_OW("FALSE"),
.PMA_REG_TX_BUSWIDTH("20BIT"),
.PMA_REG_PLL_READY_OW("FALSE"),
.PMA_REG_PLL_READY("TRUE"),
.PMA_REG_TX_RESERVED_72("FALSE"),
```

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.PMA_REG_TX_RESERVED_73("FALSE"),
.PMA_REG_TX_RESERVED_74("FALSE"),
.PMA_REG_EI_PCLK_DELAY_SEL(0),
.PMA_REG_TX_RESERVED_77("FALSE"),
.PMA_REG_TX_RESERVED_83_78(0),
.PMA_REG_TX_RESERVED_89_84(0),
.PMA_REG_TX_RESERVED_95_90(0),
.PMA_REG_TX_RESERVED_101_96(0),
.PMA_REG_TX_RESERVED_107_102(0),
.PMA_REG_TX_RESERVED_113_108(0),
.PMA_REG_TX_AMP_DAC0(25),
.PMA_REG_TX_AMP_DAC1(19),
.PMA_REG_TX_AMP_DAC2(14),
.PMA_REG_TX_AMP_DAC3(9),
.PMA_REG_TX_RESERVED_143_138(5),
.PMA_REG_TX_MARGIN(0),
.PMA_REG_TX_MARGIN_OW("FALSE"),
.PMA_REG_TX_RESERVED_149_148(0),
.PMA_REG_TX_RESERVED_150("FALSE"),
.PMA_REG_TX_SWING("FALSE"),
.PMA_REG_TX_SWING_OW("FALSE"),
.PMA_REG_TX_RESERVED_153("FALSE"),
.PMA_REG_TX_RXDET_THRESHOLD("84MV"),
.PMA_REG_TX_RESERVED_157_156(0),
.PMA_REG_TX_BEACON_OSC_CTRL("FALSE"),
.PMA_REG_TX_RESERVED_160_159(0),
.PMA_REG_TX_RESERVED_162_161(0),
.PMA_REG_TX_TX2RX_SLPBACK_EN("FALSE"),
.PMA_REG_TX_PCLK_EDGE_SEL("FALSE"),
.PMA_REG_TX_RXDET_STATUS_OW("FALSE"),
.PMA_REG_TX_RXDET_STATUS("TRUE"),
.PMA_REG_TX_PRBS_GEN_EN("FALSE"),
.PMA_REG_TX_PRBS_GEN_WIDTH_SEL("20BIT"),
.PMA_REG_TX_PRBS_SEL("PRBS7"),
```

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.PMA_REG_TX_UDP_DATA_7_TO_0(5),  
.PMA_REG_TX_UDP_DATA_15_TO_8(235),  
.PMA_REG_TX_UDP_DATA_19_TO_16(3),  
.PMA_REG_TX_RESERVED_192("FALSE"),  
.PMA_REG_TX_FIFO_WP_CTRL(4),  
.PMA_REG_TX_FIFO_EN("FALSE"),  
.PMA_REG_TX_DATA_MUX_SEL(0),  
.PMA_REG_TX_ERR_INSERT("FALSE"),  
.PMA_REG_TX_RESERVED_203_200(0),  
.PMA_REG_TX_RESERVED_204("FALSE"),  
.PMA_REG_TX_SATA_EN("FALSE"),  
.PMA_REG_TX_RESERVED_207_206(0),  
.PMA_REG_RATE_CHANGE_TXPCLK_ON_OW("FALSE"),  
.PMA_REG_RATE_CHANGE_TXPCLK_ON("TRUE"),  
.PMA_REG_TX_CFG_POST1(0),  
.PMA_REG_TX_CFG_POST2(0),  
.PMA_REG_TX_DEEMP(0),  
.PMA_REG_TX_DEEMP_OW("FALSE"),  
.PMA_REG_TX_RESERVED_224_223(0),  
.PMA_REG_TX_RESERVED_225("FALSE"),  
.PMA_REG_TX_RESERVED_229_226(0),  
.PMA_REG_TX_OOB_DELAY_SEL(0),  
.PMA_REG_TX_POLARITY("NORMAL"),  
.PMA_REG_ANA_TX_JTAG_DATA_O_SEL("FALSE"),  
.PMA_REG_TX_RESERVED_236("FALSE"),  
.PMA_REG_TX_LS_MODE_EN("FALSE"),  
.PMA_REG_TX_JTAG_MODE_EN_OW("FALSE"),  
.PMA_REG_TX_JTAG_MODE_EN("FALSE"),  
.PMA_REG_RX_JTAG_MODE_EN_OW("FALSE"),  
.PMA_REG_RX_JTAG_MODE_EN("FALSE"),  
.PMA_REG_RX_JTAG_OE("TRUE"),  
.PMA_REG_RX_ACJTAG_VHYSTSEL(0),  
.PMA_REG_TX_RES_CAL_EN("FALSE"),  
.PMA_REG_RX_TERM_MODE_CTRL(4),
```

```
.PMA_REG_TX_RESERVED_251_250(0),  
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.PMA_REG_TX_RESERVED_253("FALSE"),  
.PMA_REG_TX_RESERVED_254("FALSE"),  
.PMA_REG_TX_RESERVED_255("FALSE"),  
.PMA_REG_TX_RESERVED_256("FALSE"),  
.PMA_REG_TX_RESERVED_257("FALSE"),  
.PMA_REG_TX_PH_SEL(1),  
.PMA_REG_TX_CFG_PRE(0),  
.PMA_REG_TX_CFG_MAIN(0),  
.PMA_REG_CFG_POST(0),  
.PMA_REG_PD_MAIN("TRUE"),  
.PMA_REG_PD_PRE("TRUE"),  
.PMA_REG_TX_LS_DATA("FALSE"),  
.PMA_REG_TX_DCC_BUF_SZ_SEL(0),  
.PMA_REG_TX_DCC_CAL_CUR_TUNE(0),  
.PMA_REG_TX_DCC_CAL_EN("FALSE"),  
.PMA_REG_TX_DCC_CUR_SS(0),  
.PMA_REG_TX_DCC_FA_CTRL("FALSE"),  
.PMA_REG_TX_DCC_RI_CTRL("FALSE"),  
.PMA_REG_ATB_SEL_2_TO_0(0),  
.PMA_REG_ATB_SEL_9_TO_3(0),  
.PMA_REG_TX_CFG_7_TO_0(0),  
.PMA_REG_TX_CFG_15_TO_8(0),  
.PMA_REG_TX_CFG_23_TO_16(0),  
.PMA_REG_TX_CFG_31_TO_24(0),  
.PMA_REG_TX_OOB_EI_EN("FALSE"),  
.PMA_REG_TX_OOB_EI_EN_OW("FALSE"),  
.PMA_REG_TX_BEACON_EN_DELAYED("FALSE"),  
.PMA_REG_TX_BEACON_EN_DELAYED_OW("FALSE"),  
.PMA_REG_TX_JTAG_DATA("FALSE"),  
.PMA_REG_TX_RXDET_TIMER_SEL(87),  
.PMA_REG_TX_CFG1_7_0(0),  
.PMA_REG_TX_CFG1_15_8(0),
```

```

.PMA_REG_TX_CFG1_23_16(0),
.PMA_REG_TX_CFG1_31_24(0),
.PMA_REG_CFG_LANE_POWERUP("OFF"),
.PMA_REG_CFG_TX_LANE_POWERUP_CLKPATH("FALSE"),
.PMA_REG_CFG_TX_LANE_POWERUP_PISO("FALSE"),
.PMA_REG_CFG_TX_LANE_POWERUP_DRIVER("FALSE")

) GTP_HSSTLP_LANE_inst (
    .LANE_COUT_BUS_FORWARD(),// OUTPUT[18:0]
    .P_CFG_RDATA(),          // OUTPUT[7:0]
    .P_RDATA(),              // OUTPUT[46:0]
    .P_TEST_STATUS(),        // OUTPUT[19:0]
    .LANE_CIN_BUS_FORWARD(), // INPUT[18:0]
    .PLL_RES_TRIM_I(),      // INPUT[5:0]
    .P_CFG_ADDR(),           // INPUT[11:0]
    .P_CFG_WDATA(),           // INPUT[7:0]
    .P_CIM_CLK_ALIGNER_RX(), // INPUT[7:0]
    .P_CIM_CLK_ALIGNER_TX(), // INPUT[7:0]
    .P_RX_BUSWIDTH(),         // INPUT[2:0]
    .P_RX_RATE(),             // INPUT[2:0]
    .P_TDATA(),               // INPUT[45:0]
    .P_TX_BUSWIDTH(),         // INPUT[2:0]
    .P_TX_DEEMP(),            // INPUT[1:0]
    .P_TX_MARGIN(),           // INPUT[2:0]
    .P_TX_RATE(),             // INPUT[2:0]
    .APATTERN_STATUS_COUT(), // OUTPUT
    .PMA_RCLK(),              // OUTPUT
    .P_CA_ALIGN_RX(),          // OUTPUT
    .P_CA_ALIGN_TX(),          // OUTPUT
    .P_CFG_INT(),              // OUTPUT
    .P_CFG_READY(),             // OUTPUT
    .P_PCS_LSM_SYNCED(),       // OUTPUT
    .P_PCS_RX_MCB_STATUS(),   // OUTPUT
    .P_RCLK2FABRIC(),          // OUTPUT
    .P_RX_LS_DATA(),           // OUTPUT

```

```

.P_RX_READY(),           // OUTPUT
.P_RX_SATA_COMINIT(),   // OUTPUT
.P_RX_SATA_COMWAKE(),   // OUTPUT
.P_RX_SIGDET_STATUS(),  // OUTPUT
.P_TCLK2FABRIC(),       // OUTPUT
.P_TX_RXDET_STATUS(),   // OUTPUT
.P_TX_SDN(),            // OUTPUT
.P_TX_SDP(),            // OUTPUT
.TXPCLK_PLL(),          // OUTPUT
.APATTERN_STATUS_CIN(), // INPUT
.CLK_RX0(),              // INPUT
.CLK_RX90(),             // INPUT
.CLK_RX180(),            // INPUT
.CLK_RX270(),            // INPUT
.CLK_TXN(),              // INPUT
.CLK_TXP(),              // INPUT
.MCB_RCLK(),             // INPUT
.PLL_LOCK_SEL(),          // INPUT
.PLL_PD_I(),              // INPUT
.PLL_REFCLK_I(),          // INPUT
.PLL_RESET_I(),            // INPUT
.P_CEB_ADETECT_EN(),     // INPUT
.P_CFG_CLK(),             // INPUT
.P_CFG_ENABLE(),           // INPUT
.P_CFG_PSEL(),             // INPUT
.P_CFG_RST(),              // INPUT
.P_CFG_WRITE(),             // INPUT
.P_CIM_DYN_DLY_SEL_RX(), // INPUT
.P_CIM_DYN_DLY_SEL_TX(), // INPUT
.P_CIM_START_ALIGN_RX(), // INPUT
.P_CIM_START_ALIGN_TX(), // INPUT
.P_CTLE_ADJ_RST(),         // INPUT
.P_LANE_PD(),              // INPUT
.P_LANE_RST(),              // INPUT

```

```

.P_PCS_CB_RST(),           // INPUT
.P_PCS_FAREND_LOOP(),     // INPUT
.P_PCS_MCB_EXT_EN(),      // INPUT
.P_PCS_NEAREND_LOOP(),    // INPUT
.P_PCS_RX_RST(),          // INPUT
.P_PCS_TX_RST(),          // INPUT
.P_PCS_WORD_ALIGN_EN(),   // INPUT
.P_PMA_FAREND_PLOOP(),   // INPUT
.P_PMA_NEAREND_PLOOP(),  // INPUT
.P_PMA_NEAREND_SLOOP(),  // INPUT
.P_RCLK2_FR_CORE(),       // INPUT
.P_RXGEAR_SLIP(),         // INPUT
.P_RX_CLK_FR_CORE(),      // INPUT
.P_RX_HIGHZ(),             // INPUT
.P_RX_LANE_PD(),           // INPUT
.P_RX_PMA_RST(),           // INPUT
.P_RX_POLARITY_INVERT(),  // INPUT
.P_RX_SDN(),               // INPUT
.P_RX_SDP(),               // INPUT
.P_TCLK2_FR_CORE(),        // INPUT
.P_TX_BEACON_EN(),         // INPUT
.P_TX_CLK_FR_CORE(),       // INPUT
.P_TX_LANE_PD_CLKPATH(),  // INPUT
.P_TX_LANE_PD_DRIVER(),   // INPUT
.P_TX_LANE_PD_PISO(),     // INPUT
.P_TX_LS_DATA(),           // INPUT
.P_TX_PMA_RST(),           // INPUT
.P_TX_RXDET_REQ(),         // INPUT
.P_TX_SWING(),              // INPUT
.RATE_CHANGE(),              // INPUT
.SYNC()                    // INPUT
);

```

10.7 GTP_HSSTLP_PLL

10.7.1 Supported Devices

Table 10-19 GTP_HSSTLP_PLL-Supported Devices

Device Family	LOGOS2
Whether supports the GTP	Supported

10.7.2 Description of Functionality

For detailed functionality and usage instructions, please refer to "**G040008_Logos2 Family FPGAs High-Speed Serial Transceiver (HSST) User Guide**".

10.7.3 Port Description

Table 10-20 GTP_HSSTLP_PLL Port List

Port	Direction	Data Width	Function Description
SYNC_PLL	O	1	Used to generate LANE input SYNC
RATE_CHANGE_PLL	O	1	Used to generate LANE input RATE_CHANGE
PLL_PD_O	O	1	Used to generate LANE input PLL_PD_I
PLL_RST_O	O	1	Used to generate LANE input PLL_RESET_I
PMA_PLL_READY_O	O	1	Used to generate LANE input PLL_LOCK_SEL
P_CFG_READY_PLL	O	1	Read/write ready output for the configuration interface
P_CFG_RDATA_PLL	O	8	Read data for the configuration interface
P_CFG_INT_PLL	O	1	Configuration interface interrupt output, active high
P_REFCK2CORE	O	1	Pin input reference clock output to Fabric
P_PLL_READY	O	1	Active high indicates the PLL is in a locked state, and is an asynchronous signal
P_RESCAL_I_CODE_O	O	6	The resistance control output code when invalid Default (6b'101110)
PLL_CLK0	O	1	Output clock phase 0
PLL_CLK90	O	1	Output clock phase 90
PLL_CLK180	O	1	Output clock phase 180
PLL_CLK270	O	1	Output clock phase 270
PLL_REFCLK_LANE_L	O	1	PLL reference clock out to tx/rx
TXPCLK_PLL_SELECTED	I	1	The clock signal of the D flip-flop in the pma_rate_change module (triggered on the falling edge), derived from LANE's TXPCLK_PLL output
P_CFG_RST_PLL	I	1	Configuration interface reset signal, active high. All registers revert to the initial values set by the Parameter after reset

Port	Direction	Data Width	Function Description
P_CFG_CLK_PLL	I	1	Configure the clock input of the interface
P_CFG_PSEL_PLL	I	1	Selection input of the configuration interface, active high
P_CFG_ENABLE_PLL	I	1	Configuration interface access enable, active high
P_CFG_WRITE_PLL	I	1	Configure the interface's read/write selection signal. A high level indicates write, while a low level indicates read.
P_CFG_ADDR_PLL	I	12	Configuration interface write address
P_CFG_WDATA_PLL	I	8	Configuration interface write data
P_PLLPOWERDOWN	I	1	PLL powerdown control 0: PLL is not powered down (default) 1: PLL is powered down
P_PLL_RST	I	1	PLL reset control 0: PLL is no reset (default) 1: PLL is reset
P_RESCAL_RST_I	I	1	Resistor calibration reset
P_RESCAL_I_CODE_I	I	6	pma manual configuration of the resistance value default (6b'101110)
P_PLL_REF_CLK	I	1	Reference clock
P_LANE_SYNC	I	1	TX lane sync control; TX lanes sync up once input a positive pulse to lane_sync.
P_RATE_CHANGE_TCLK_ON	I	1	Register for txpclk enable signal when rate changes.
P_PLL_LOCKDET_RST_I	I	1	pll lockdetecotr reset
REFCLK_CML_N	I	1	cml reference clock input neg
REFCLK_CML_P	I	1	cml reference clock input pos

Note: The GTP file does not contain DFT-related ports.

10.7.4 Paramater Description

Table 10-21 GTP_HSSTLP_PLL Parameter List

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
TX_SYNCK_PD	<integer>	0,1	0	Control the powerdown signal of tx_syncp 1: tx_syncp is powerdown; 0: tx_syncp is not powerdown;
PMA_PLL_REG_REFCLK_TERM_IMP_CTRL	<string>	"FALSE", "TRUE"	"TRUE"	refclk termination impedance selection register, default ("TRUE"), simulation not supported
PMA_PLL_REG_BG_T_RIM	<integer>	0 to 3	2	Select the vref output voltage value in v2i circuit, default (2), simulation not supported
PMA_PLL_REG_IBUP_A1	<integer>	0 to 262143	262143	Output current branch control bit in v2i circuit, default (262143), simulation not supported
PMA_PLL_REG_IBUP_A2	<integer>	0 to 262143	0	Output current branch control bit in v2i circuit, default (0), simulation not supported

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
				supported
PMA_PLL_REG_IBUP_PD	<integer>	0 to 262143	0	Output current pd signal in v2i circuit, default (0), simulation not supported
PMA_PLL_REG_V2I_BIAS_SEL	<string>	"FALSE", "TRUE"	"FALSE"	Bias selection signal in v2i circuit, default ("FALSE"), simulation not supported
PMA_PLL_REG_V2I_EN	<string>	"FALSE", "TRUE"	"TRUE"	Enable signal in v2i circuit, default ("TRUE"), simulation not supported
PMA_PLL_REG_V2I_TB_SEL	<integer>	0 to 15	0	Test control bit in v2i circuit, default (0), simulation not supported
PMA_PLL_REG_V2I_RCALTEST_PD	<string>	"FALSE", "TRUE"	"FALSE"	Resistance calibration circuit pd signal in v2i circuit, default ("FALSE"), simulation not supported
PMA_PLL_REG_RES_CAL_TEST	<integer>	0 to 63	0	Resistance calibration control bit (internally connected) in v2i circuit, simulation not supported
PMA_RES_CAL_DIV	<integer>	0 to 3	0	Used to control v2i circuit input res_cal_div[1:0], simulation not supported
PMA_RES_CAL_CLK_SEL	<string>	"FALSE", "TRUE"	"FALSE"	Used to control the source of v2i circuit input ref_clk_in "FALSE": sourced from PLL0's output refclk_rescal_buf; "TRUE": sourced from PLL1's output refclk_rescal_buf; simulation not supported
PMA_PLL_REG_PLL_PFDDELAY_EN	<string>	"FALSE", "TRUE"	"TRUE"	Pll pfd delay enable "TRUE":enable (default) "FALSE":disable
PMA_PLL_REG_PFDD_ELAYSEL	<integer>	0 to 3	1	Pll pfd delay sel, default :1
PMA_PLL_REG_PLL_VCTRL_SET	<integer>	0 to 3	0	Pll vctrl start voltage, default:0
PMA_PLL_REG_REA_DY_OR_LOCK	<string>	"FALSE", "TRUE"	"FALSE"	reg_ready_or_lock, ready and Lock selection
PMA_PLL_REG_PLL_CP	<integer>	0 to 1023	31	Pll charge pump current select, Min current :1, Max current:1023, Default: 31
PMA_PLL_REG_PLL_REFDIV	<integer>	0 to 31	16	Pll reference clock divider M, default: 16 -----> M=1
PMA_PLL_REG_PLL_LOCKDET_EN	<string>	"FALSE", "TRUE"	"FALSE"	Lockdet en of the register input, default ("FALSE")
PMA_PLL_REG_PLL_READY	<string>	"FALSE", "TRUE"	"FALSE"	pll ready signal rewrite value, "FALSE":pll unlock(default) "TRUE":pll locked
PMA_PLL_REG_PLL_READY_OW	<string>	"FALSE", "TRUE"	"FALSE"	pll ready rewrite enable signal "FALSE": (default) pma_pll_ready_o_x=lockdetector output "TRUE": pma_pll_ready_o_x= reg_pll_ready_i_x

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PMA_PLL_REG_PLL_FBDIV	<integer>	0 to 63	36	Pll feedback divider N2 is Pll_fbdv<5> : Pll_fbdv<5>=1 ---> N2=5, Pll_fbdv<5>=0 ---> N2=4, Pll feedback divider N1 is Pll_fbdv<4:0> : Valid settings are 1, 2, 3, 4, and 5. Default(36): pll_fbdv<5:0>=1 00100 ---> N1 X N2=20
PMA_PLL_REG_LPF_RES	<integer>	0 to 15	1	LPF resistor control Default(1): lpf_res<3:0>=0001
PMA_PLL_REG_JTAG_OE	<string>	"FALSE", "TRUE"	"FALSE"	Pll jtag oe
PMA_PLL_REG_JTAG_VHYSTSEL	<integer>	0 to 7	0	Pll jtag threshold voltage selection, default (0)
PMA_PLL_REG_PLL_LOCKDET_EN_OW	<string>	"FALSE", "TRUE"	"FALSE"	"TRUE": select reg_pll_lockdet_en_i_x "FALSE": select internal enable (default)
PMA_PLL_REG_PLL_LOCKDET_FBCT	<integer>	0 to 7	7	Feedback clock domain counter overflow value counter value for feedback clock time out value of lock detect 0: 2^9 1: 2^10 2: 2^11 3: 2^12 4: 2^13 5: 2^14 6: 2^15 7: 2^16-1 (default)
PMA_PLL_REG_PLL_LOCKDET_ITER	<integer>	0 to 7	3	Lock loop count Register value of number of iterations of consecutive successful one-time lock detection before set pll_lock. 0: 1 1: 2 2: 4 3: 8(default) 4: 16 5: 32 6: 64 7: 127
PMA_PLL_REG_PLL_LOCKDET_MODE	<string>	"FALSE", "TRUE"	"FALSE"	Lockdet mode, Default: "FALSE"

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PMA_PLL_REG_PLL_LOCKDET_LOCKCT	<integer>	0 to 7	4	Difference counter overflow value Register value of lock detection threshold for count difference between ref_clk & fb_clk counters. 0: 2 1: 4 2: 8 3: 16 4: 32 (default) 5: 64 6: 128 7: 256
PMA_PLL_REG_PLL_LOCKDET_REFCT	<integer>	0 to 7	7	Reference clock domain counter overflow value Counter value for reference clock time out value of lock detect 0: 2^9 1: 2^10 2: 2^11 3: 2^12 4: 2^13 5: 2^14 6: 2^15 7: 2^16-1 (default)
PMA_PLL_REG_PLL_LOCKDET_RESET_N	<string>	"FALSE", "TRUE"	"TRUE"	pll lockdetecotr reset by registor default ("TRUE")
PMA_PLL_REG_PLL_LOCKDET_RESET_N_OW	<string>	"FALSE", "TRUE"	"FALSE"	pll lockdetecotr reset overwrite enable default ("FALSE")
PMA_PLL_REG_PLL_LOCKED	<string>	"FALSE", "TRUE"	"FALSE"	Locked signal input of the register, Default: "FALSE"
PMA_PLL_REG_PLL_LOCKED_OW	<string>	"FALSE", "TRUE"	"FALSE"	"TRUE": select reg_pll_locked_i_x "FALSE": select internal signal default ("FALSE")
PMA_PLL_REG_PLL_LOCKED_STICKY_CLEAR	<string>	"FALSE", "TRUE"	"FALSE"	Clear continuous PLL lock signal. When set to "TRUE", pma_pll_ready_o_x is cleared default ("FALSE")
PMA_PLL_REG_PLL_UNLOCKED	<string>	"FALSE", "TRUE"	"FALSE"	Unlocked signal input of the register default ("FALSE")
PMA_PLL_REG_PLL_UNLOCKDET_ITER	<integer>	0 to 3	2	Non-lock loop count Register value of number of iterations of lock detection attempts before set pll_unlock. 00: 63; 01: 127; 10: 255 (default); 11: 1023
PMA_PLL_REG_PLL_UNLOCKED_OW	<string>	"FALSE", "TRUE"	"FALSE"	"TRUE": select reg_pll_unlocked_i_x "FALSE": select internal signal default ("FALSE")
PMA_PLL_REG_PLL_UNLOCKED_STICKY_CLEAR	<string>	"FALSE", "TRUE"	"FALSE"	Pll continuous loss of lock signal clear signal default ("FALSE")
PMA_PLL_REG_I_CT_RL_MAX	<integer>	0 to 63	63	Maximum auto calibration value, Default: 6b'111111

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PMA_PLL_REG_REFCLK_LK_TEST_EN	<string>	"FALSE", "TRUE"	"FALSE"	refclk port test select,default ("FALSE")
PMA_PLL_REG_RESCAL_EN	<string>	"FALSE", "TRUE"	"FALSE"	Auto calibration enable "FALSE"-disable (default) "TRUE"-normal work
PMA_PLL_REG_I_CTRL_MIN	<integer>	0 to 63	0	Minimum auto calibration value, Default: 0
PMA_PLL_REG_RESCAL_DONE_OW	<string>	"FALSE", "TRUE"	"FALSE"	done signal overwrite enable "FALSE" enable calibration detection indication function (default) "TRUE" select the done signal register reg_rescal_done_val_i_x
PMA_PLL_REG_RESCAL_DONE_VAL	<string>	"FALSE", "TRUE"	"FALSE"	done signal overwrite value (default "FALSE")
PMA_PLL_REG_RESCAL_I_CODE	<integer>	0 to 63	46	Resistance control output code when invalid, Default (46)
PMA_PLL_REG_RESCAL_I_CODE_OW	<string>	"FALSE", "TRUE"	"FALSE"	Overwrite resistance control output code "FALSE": select the value controlled by reg_rescal_i_code_pma_i_x (default) "TRUE": Overwrite output code value is reg_rescal_i_code_val_i_x
PMA_PLL_REG_RESCAL_I_CODE_PMA	<string>	"FALSE", "TRUE"	"FALSE"	Manual resistor control output code selection signal, only enabled when reg_rescal_i_code_ow_i_x is 0 "FALSE": Select the corrected output code value "TRUE": Select the value of pma_rescal_i_code_i_x
PMA_PLL_REG_RESCAL_I_CODE_VAL	<integer>	0 to 63	46	Overwrite value of the resistor control output code Default (46)
PMA_PLL_REG_RESCAL_INT_R_SMALL_OW	<string>	"FALSE", "TRUE"	"FALSE"	Overwrite comparator output "FALSE": Select the automatic calibration comparator output (default) "TRUE": Select the overwrite value
PMA_PLL_REG_RESCAL_INT_R_SMALL_VAL	<string>	"FALSE", "TRUE"	"FALSE"	Comparator overwrite value Default("FALSE")
PMA_PLL_REG_RESCAL_ITER_VALID_SEL	<integer>	0 to 3	0	Select the number of automatic calibration cycles 0: 64 calibration cycles (default) 1: 32 calibration cycles 2: 16 calibration cycles 3: 8 calibration cycles
PMA_PLL_REG_RESCAL_RESET_N_OW	<string>	"FALSE", "TRUE"	"FALSE"	pll lockdetecotr reset overwrite enable default ("FALSE")
PMA_PLL_REG_RESCAL_RST_N_VAL	<string>	"FALSE", "TRUE"	"FALSE"	Reset signal overwrite value Default("FALSE")
PMA_PLL_REG_RESCAL_WAIT_SEL	<string>	"FALSE", "TRUE"	"TRUE"	Resistor calibration waiting time, which is the duration of each calibration cycle "FALSE": 0-64 clock cycles "TRUE": 1-32 clock cycles (default)
PMA_PLL_REFCLK2LANE_PD_L	<string>	"FALSE", "TRUE"	"FALSE"	pll_refclk_lane_1 power down control,default ("FALSE")

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description
PMA_PLL_REFCLK2L_ANE_PD_R	<string>	"FALSE", "TRUE"	"FALSE"	pll_refclk_lane_r power down control,default ("FALSE")
PMA_PLL_REG_LOC_KDET_REPEAT	<string>	"FALSE", "TRUE"	"FALSE"	Re-detect after lock Default("FALSE")
PMA_PLL_REG_NOF_BCLK_STICKY_CLEA_R	<string>	"FALSE", "TRUE"	"FALSE"	When set to "TRUE", pll_nofbclk_sticky_o_x cleared. default ("FALSE")
PMA_PLL_REG_NOR_EFCLK_STICKY_CLEAR	<string>	"FALSE", "TRUE"	"FALSE"	When set to "TRUE", pll_norefclk_sticky_o_x cleared. default ("FALSE")
PMA_PLL_REG_TEST_SEL	<integer>	0 to 20	0	test signal selection (test_sel<4> = 0) 0: vssa (default) 1: vdda 2: vdda1p2/3 3: vc_cap_test 4: vco_vbn_test 5: cp_amp_test 15: reserved test signal selection (test_sel<4> = 1) 16: pll_fbclk 17: pll_refclk 18: plllocked 19: refclk_test 20: reserved
PMA_PLL_REG_TEST_V_EN	<string>	"FALSE", "TRUE"	"FALSE"	test signal voltage enable "FALSE": test signal of voltage is disabled(default) "TRUE": test signal of voltage is enabled
PMA_PLL_REG_TEST_SIG_HALF_EN	<string>	"FALSE", "TRUE"	"FALSE"	test signal voltage half enable "FALSE": test signal voltage out is 1:1 (default) "TRUE": test signal voltage out is 1:2
PMA_PLL_REG_REFCLK_PAD_SEL	<string>	"FALSE", "TRUE"	"FALSE"	select reference clock from PAD or internal circuit "FALSE": from pad reference clock(default) "TRUE":reference clock from fabric
PARM_PLL_POWERUP	<string>	"OFF", "ON"	"OFF"	This parameter controls the power-up of the PMA_PLL Default: "OFF"

10.7.5 Instantiation Template

```
GTP_HSSTLP_PLL #(
    .TX_SYNCK_PD(0),
    .PMA_PLL_REG_REFCLK_TERM_IMP_CTRL("TRUE"),
    .PMA_PLL_REG_BG_TRIM(2),
    .PMA_PLL_REG_IBUP_A1(262143),
```

```
.PMA_PLL_REG_IBUP_A2(0),
.PMA_PLL_REG_IBUP_PD(0),
.PMA_PLL_REG_V2I_BIAS_SEL("FALSE"),
.PMA_PLL_REG_V2I_EN("TRUE"),
.PMA_PLL_REG_V2I_TB_SEL(0),
.PMA_PLL_REG_V2I_RCALTEST_PD("FALSE"),
.PMA_PLL_REG_RES_CAL_TEST(0),
.PMA_RES_CAL_DIV(0),
.PMA_RES_CAL_CLK_SEL("FALSE"),
.PMA_PLL_REG_PLL_PFDDELAY_EN("TRUE"),
.PMA_PLL_REG_PFDDELAYSEL(1),
.PMA_PLL_REG_PLL_VCTRL_SET(0),
.PMA_PLL_REG_READY_OR_LOCK("FALSE"),
.PMA_PLL_REG_PLL_CP(31),
.PMA_PLL_REG_PLL_REFDIV(16),
.PMA_PLL_REG_PLL_LOCKDET_EN("FALSE"),
.PMA_PLL_REG_PLL_READY("FALSE"),
.PMA_PLL_REG_PLL_READY_OW("FALSE"),
.PMA_PLL_REG_PLL_FBDIV(36),
.PMA_PLL_REG_LPF_RES(1),
.PMA_PLL_REG_JTAG_OE("FALSE"),
.PMA_PLL_REG_JTAG_VHYSTSEL(0),
.PMA_PLL_REG_PLL_LOCKDET_EN_OW("FALSE"),
.PMA_PLL_REG_PLL_LOCKDET_FBCT(7),
.PMA_PLL_REG_PLL_LOCKDET_ITER(3),
.PMA_PLL_REG_PLL_LOCKDET_MODE("FALSE"),
.PMA_PLL_REG_PLL_LOCKDET_LOCKCT(4),
.PMA_PLL_REG_PLL_LOCKDET_REFCT(7),
.PMA_PLL_REG_PLL_LOCKDET_RESET_N("TRUE"),
.PMA_PLL_REG_PLL_LOCKDET_RESET_N_OW("FALSE"),
.PMA_PLL_REG_PLL_LOCKED("FALSE"),
.PMA_PLL_REG_PLL_LOCKED_OW("FALSE"),
.PMA_PLL_REG_PLL_LOCKED_STICKY_CLEAR("FALSE"),
.PMA_PLL_REG_PLL_UNLOCKED("FALSE"),
```

```

.PMA_PLL_REG_PLL_UNLOCKDET_ITER(2),
.PMA_PLL_REG_PLL_UNLOCKED_OW("FALSE"),
.PMA_PLL_REG_PLL_UNLOCKED_STICKY_CLEAR("FALSE"),
.PMA_PLL_REG_I_CTRL_MAX(63),
.PMA_PLL_REG_REFCLK_TEST_EN("FALSE"),
.PMA_PLL_REG_RESCAL_EN("FALSE"),
.PMA_PLL_REG_I_CTRL_MIN(0),
.PMA_PLL_REG_RESCAL_DONE_OW("FALSE"),
.PMA_PLL_REG_RESCAL_DONE_VAL("FALSE"),
.PMA_PLL_REG_RESCAL_I_CODE(46),
.PMA_PLL_REG_RESCAL_I_CODE_OW("FALSE"),
.PMA_PLL_REG_RESCAL_I_CODE_PMA("FALSE"),
.PMA_PLL_REG_RESCAL_I_CODE_VAL(46),
.PMA_PLL_REG_RESCAL_INT_R_SMALL_OW("FALSE"),
.PMA_PLL_REG_RESCAL_INT_R_SMALL_VAL("FALSE"),
.PMA_PLL_REG_RESCAL_ITER_VALID_SEL(0),
.PMA_PLL_REG_RESCAL_RESET_N_OW("FALSE"),
.PMA_PLL_REG_RESCAL_RST_N_VAL("FALSE"),
.PMA_PLL_REG_RESCAL_WAIT_SEL("TRUE"),
.PMA_PLL_REFCLK2LANE_PD_L("FALSE"),
.PMA_PLL_REFCLK2LANE_PD_R("FALSE"),
.PMA_PLL_REG_LOCKDET_REPEAT("FALSE"),
.PMA_PLL_REG_NOFBCLK_STICKY_CLEAR("FALSE"),
.PMA_PLL_REG_NOREFCLK_STICKY_CLEAR("FALSE"),
.PMA_PLL_REG_TEST_SEL(0),
.PMA_PLL_REG_TEST_V_EN("FALSE"),
.PMA_PLL_REG_TEST_SIG_HALF_EN("FALSE"),
.PMA_PLL_REG_REFCLK_PAD_SEL("FALSE"),
.PARM_PLL_POWERUP("OFF")

) <InstanceName> (
    .P_CFG_RDATA_PLL(),          // OUTPUT[7:0]
    .P_RESCAL_I_CODE_O(),        // OUTPUT[5:0]
    .P_CFG_ADDR_PLL(),          // INPUT[11:0]
    .P_CFG_WDATA_PLL(),          // INPUT[7:0]

```

```

.P_ESCAL_I_CODE_I(),      // INPUT[5:0]
.PPLL_CLK0(),            // OUTPUT
.PPLL_CLK90(),           // OUTPUT
.PPLL_CLK180(),          // OUTPUT
.PPLL_CLK270(),          // OUTPUT
.PPLL_PD_O(),            // OUTPUT
.PPLL_REFCLK_LANE_L(),   // OUTPUT
.PPLL_RST_O(),           // OUTPUT
.PMA_PLL_READY_O(),      // OUTPUT
.P_CFG_INT_PLL(),         // OUTPUT
.P_CFG_READY_PLL(),       // OUTPUT
.P_PLL_READY(),           // OUTPUT
.P_REFCK2CORE(),          // OUTPUT
.RATE_CHANGE_PLL(),       // OUTPUT
.SYNC_PLL(),              // OUTPUT
.P_CFG_CLK_PLL(),         // INPUT
.P_CFG_ENABLE_PLL(),      // INPUT
.P_CFG_PSEL_PLL(),        // INPUT
.P_CFG_RST_PLL(),         // INPUT
.P_CFG_WRITE_PLL(),        // INPUT
.P_LANE_SYNC(),            // INPUT
.P_PLLPOWERDOWN(),         // INPUT
.P_PLL_LOCKDET_RST_I(),   // INPUT
.P_PLL_REF_CLK(),          // INPUT
.P_PLL_RST(),              // INPUT
.P_RATE_CHANGE_TCLK_ON(), // INPUT
.P_ESCAL_RST_I(),          // INPUT
.REFCLK_CML_N(),           // INPUT
.REFCLK_CML_P(),           // INPUT
.TXPCLK_PLL_SELECTED()    // INPUT
);

```

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