PK02001_PGL22G_FBG256

(V1.4)

(30.06.2020)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.4	30.06.2020	Initial release

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
POD	Package Outline Drawing

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Chapter 1 Introduction to Packaging

PGL22G_FBG256 uses a wire-bond Ball Grid Array (BGA) type of packaging. Package size: 17x17mm; Number of balls: 256; Ball pitch: 1.0mm; Maximum package thickness: 1.43mm

Chapter 2 Package Dimension and Pins

2.1 Package Outline Dimension

Table 2-1 Dimensional Values

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
D	16.9	17.0	17.1	A	1.23	1.33	1.43
D1	n/a	15.0	n/a	A1	0.32	0.37	0.42
E	16.9	17.0	17.1	A2	0.91	0.96	1.01
E1	n/a	15.0	n/a	c	0.22	0.26	0.3
b	0.45	0.5	0.55	e	n/a	1.0	n/a
DDD (Die-to-Die Alignment)	0.2						

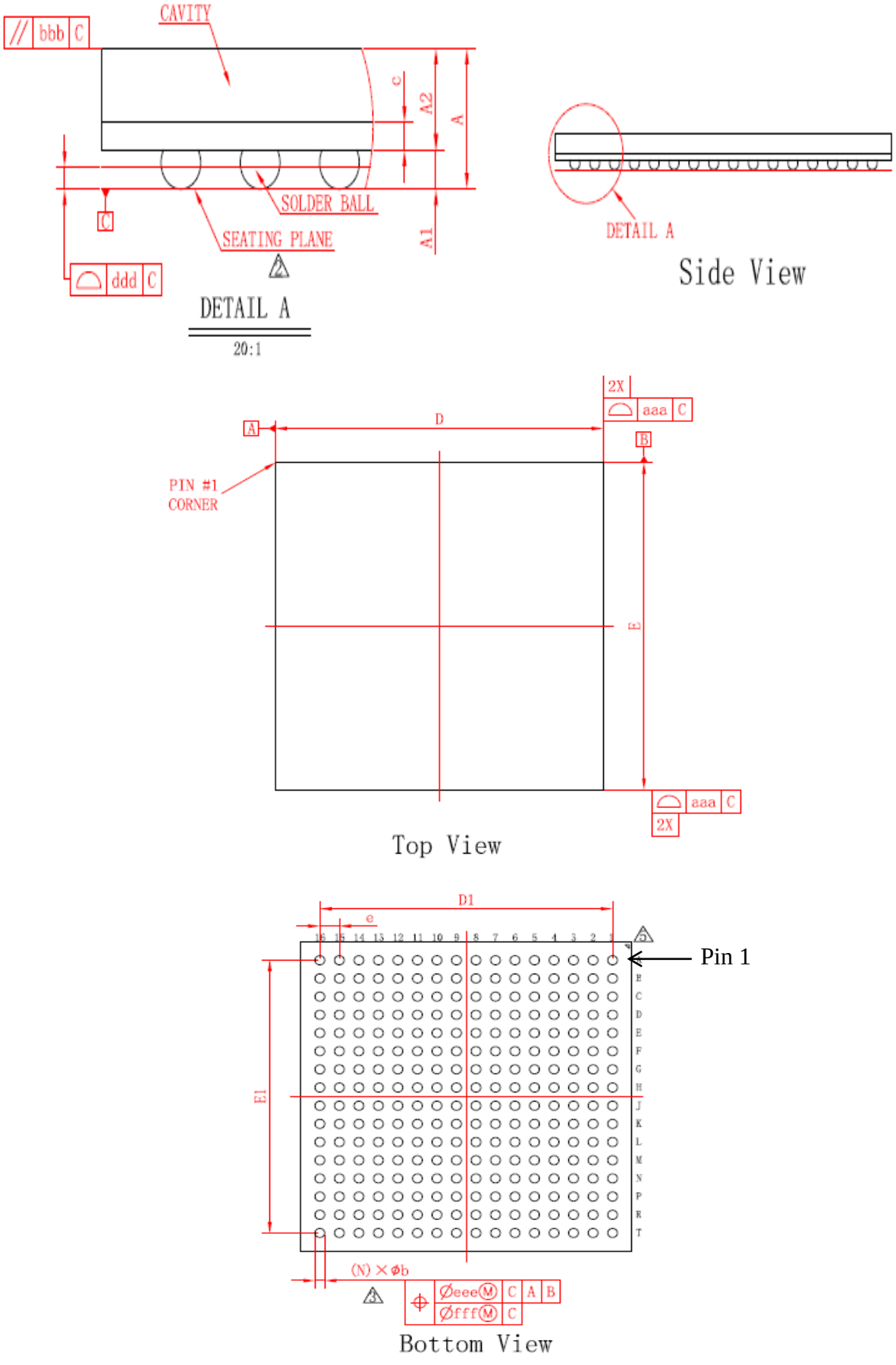

Figure 2-1 Package Outline Dimension (POD)

Note: PIN #1 indicates the position of the first pin

2.2 Pin Description

Table 2-2 Product Pin Definitions

PIN name	PIN type	PIN description
General Pin		
DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]	input/output	All general IOs are marked as DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]. DIFFIO: indicates that all general IOs support differential input/output, such as LVDS; [L0, L1, L2, R0, R1, R2]: indicates BANK names [0…n]: indicates the unique differential pair number in the BANK; [N, P]: N indicates the negative end of the differential pair and P represents the positive end.
Multiplexed Pin		
DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]/XXX		Multiplexed pins are marked as DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]/XXX, where XXX indicates one or more of the functions described below. When the multiplexed pin is not used for special applications, it can serve as a general IO
--Configuration Pin		
MODE_2, MODE_1, MODE_0	input	They are used for configuration mode selection during configuration, as follows: 000: JTAG 001: Master SPI (X1, X2, X4, X8) 010: Master BPI (X8, X16) 011: Slave Serial (X1) 100: Slave Parallel (X8, X16, X32) 101: Slave SPI (X1) 111: Internal Master SPI (X1, X2, X4)
INIT_FLAG_N	Bidirectional (open-drain)	When the FPGA is powered up completion during configuration, the pin is driven to a low level. Once the FPGA completes initialization, the pin is released. During configuration, this pin serves as an output for the configuration error indication state. During the configuration or initialization process, this pin can also accept an external low level input to indicate an error or delay the configuration.
CFG_CLK	input/output	Configuration Clock Pin. In the slave mode, the pin serves as a clock input to obtain configuration data from external sources; In the master mode, the pin serves as a clock output to obtain configuration data from external sources;
D[31, 30…1, 0]	input/output	32-bit configuration data bus input/output pins: (1) In the Master SPI X1 configuration mode, pin D[0], as command output, is connected to the data input of the SPI flash, and pin D[1], as data input, is connected to the data output of the SPI flash. (2) In the Master SPI X2 configuration mode, pins D[1:0] serve as the data bus. (3) In the Master SPI X4 configuration mode, pins D[3:0] serve as the data bus.

PIN name	PIN type	PIN description
		(4) In the Master SPI X8 configuration mode, pins D[3:0] serve as the data bus for the first SPI FLASH, and pins D[7:4] serve as the data bus for the second SPI FLASH. (5) In the Slave Serial configuration mode, pin D[1] serves as the data bus. (6) In the Slave SPI configuration mode, pin D[0] is for the master device output and slave device input, pin D[1] is for the master device input and slave device output, and pin D[3] is for chip hold. (7) In the Master BPI configuration X8 asynchronous mode, pins D[7:0] serve as an 8-bit data bus. (8) In the Master BPI configuration X16 asynchronous/synchronous mode, pins D[15:0] serve as a 16-bit data bus. (9) In the Slave Parallel X8 configuration mode, pins D[7:0] are an 8-bit data bus. (10) In the Slave Parallel X16 configuration mode, pins D[15:0] are a 16-bit data bus. (11) In the Slave Parallel X32 configuration mode, pins D[31:0] are a 32-bit data bus.
CS_N	input	Multi-function Configuration Pin. for chip select input. Active-low. (1) When it is low level, this pin enables the Slave Parallel mode configuration interface. (2) In other configuration modes, this pin is high-z. (3) To make this pin continue playing its configuration function after configuration is complete, users need to set the configuration register to preserve its configuration function.
RWSEL	input	Multi-function Configuration Pin. For selecting the read/write input in the Slave Parallel configuration mode (high for read and low for write). (1) When it is high level, the Slave Parallel configuration mode reads data from the data bus; (2) When it is low level, the Slave Parallel configuration mode writes data to the data bus; (3) Read and write can be switched only when CS_N is high level. (4) To make this pin continue playing its configuration function after configuration is complete, users need to set the configuration register to preserve its configuration function. (5) In other configuration modes, this pin is high-z.
BUSY	output	Multi-function Configuration Pin. (1) During readback in the Slave Parallel mode, a high level output indicates that the data read from the bus is invalid. (2)To make this pin continue playing its configuration function in the user mode, users need to set the configuration register to preserve its configuration function. (3) In other configuration modes, this pin is in the high-z state.
CSO_DOUT	output	Multi-function Configuration Pin. Needed for cascade.

PIN name	PIN type	PIN description
		(1) In the Master SPI and X1 mode, this pin serves as cascaded data output; (2) In the Slave Serial configuration mode, this pin serves as cascaded data output; (3) In the Slave Parallel configuration mode, this pin serves as a chip select signal output;
FCS_N	output	Multi-function configuration pin, used for the external Master SPI configuration mode. (1) In the Master SPI mode, this pin outputs a chip select signal to external flash, active-low
VS1, VS0	input	Multi-function configuration pins, used in the Master SPI or internal Master SPI mode. (1) It is used for selecting the bitstream version: 00 for the first set of bitstreams, 01 for the second set, 10 for the third set, 11 for the fourth set; (2) Enable the internal pull-down resistors during configuration.
IO_STATUS_C	input	Multi-function pin, used for inputting signals and controlling the state of all general IOs during the configuration process. (1) "1" keeps all general IOs in a pull-up state during configuration. (2) "0" keeps all general IOs in a tri-state during configuration.
ADR[25:0]	output	Multi-function configuration pins, used for outputting addresses in the BPI configuration mode.
BFOE_N	output	Multi-function configuration pin, used for providing a low level output enable control signal for parallel NOR FLASH in the BPI configuration mode. (1) In the BPI configuration mode, this pin should be connected to the flash's output enable input and to VCCIO via a 4.7K resistor.
BADRVO_N	output	Multi-function configuration pin, used for providing a low-level address valid control signal for parallel NOR FLASH in the BPI configuration mode. (1) In the BPI configuration mode, if the external FLASH supports address valid signal input, then this pin should be connected to the FLASH's address valid input pin and to VCCIO via a 4.7K resistor. If the external flash does not support address valid signal input, then there is no need to connect this pin.
BFWE_N	output	Multi-function configuration pin, used for providing a low level write enable signal for parallel NOR FLASH in the BPI configuration mode. (1) In the BPI configuration mode, this pin should be connected to the flash's write enable input and to VCCIO via a 4.7K resistor;
BFCE_N	output	Multi-function configuration pin, used for providing a low level chip select control signal for parallel NOR FLASH in the BPI configuration mode; (1) In the BPI configuration mode, this pin should

PIN name	PIN type	PIN description
		be connected to the flash's chip select input and to VCCIO via a 4.7K resistor.
FCS2_N	output	Multi-function configuration pin, used for the external Master SPI X8 configuration mode. (1) In the Master SPI X8 mode, this pin outputs a chip select signal to external flash, active-low. The pin should be connected to VCCIO via an external pull-up resistor not more than 4.7K.
ECCLKIN	input	Multi-function configuration pin, used for inputting signals and serves as clock input for the Master configuration mode.
-- Clock, PLL, Crystal Oscillator Multi-function Pin		
CLK[0,1,2,3]_[L0,L1,L2,R0,R1,R2]	input	Dedicated global clock input pins, 4 pins for each bank
DIFFCLK[0,1]_[L0,L1,L2,R0,R1,R2]_[N,P]	input	Dedicated global differential clock input pins, 2 pairs for each bank
PLL[0,1,2,…10]_CLKOUT_[P,N]	output	Direct selection of PLL[0, 1, …, 19] output to these pins are possible
PLL[0,1,2,…10]_CLKIN[0,1,2,3]	input	Optional PLL input, PLL can select directly the input clock from these pins
PLL[0,1,2,…10]_CLKFB_[P,N]	input	Optional PLL feedback clock input, PLL can input external feedback clock from these pins
XTALA_[L0,L1,L2,R0,R1,R2]	input	Dedicated external crystal input at port A. Input for the on-die inverter, 1 pin for each bank
XTALB_[L0,L1,L2,R0,R1,R2]	output	Dedicated external crystal output at port B. Output for the on-die inverter, 1 pin for each bank
-- External Memory Interface Pin		
DQS[0,1,2][#]_[L0,L1,L2,R0,R1,R2]	input/output	Used to connect to the DQS/DQS# signal pins of external memory
DQ[0,1,2]_[L0,L1,L2,R0,R1,R2]	input/output	Can connect to the DQ signal pins of external memory
--HMEMC Memory Interface Pin		
[R,L]_A[0,..,15]	output	DDR memory address
[R,L]_CS_N	output	DDR memory chip selection signal, active-low, depends on whether the memory is in use.
[R,L]_RAS_N	output	RAS, active-low
[R,L]_CAS_N	output	CAS, active-low
[R,L]_WE_N	output	Write enable, active-low
[R,L]_BA[0,1,2]	output	DDR BANK address
[R,L]_ODT	output	ODT, on-die terminal
[R,L]_CK	output	P side of DDR memory
[R,L]_CK_N	output	N side of DDR memory
[R,L]_CKE	output	DDR memory clock enable signal, active-high
[R,L]_RESET_N	output	DDR memory reset, active-low
[R,L]_DML	output	Write data mask signal of DQ0-DQ7
[R,L]_DQSL	input/output	DQS signals related to DQ0-DQ7
[R,L]_DQSL_N	input/output	DQS# signals related to DQ0-DQ7
[R,L]_DQ[0,…,15]	input/output	Memory data bus
[R,L]_DMU	output	Write data mask signals of DQ8-DQ15

PIN name	PIN type	PIN description
[R,L]_DQSU	input/output	DQS signals related to DQ8-DQ15
[R,L]_DQSU_N	input/output	DQS# signals related to DQ8-DQ15
[R,L]_DQSL_GATE_IN	input	DQS gate window signal feedback (low bit) after compensating for read command path delay
[R,L]_DQSL_GATE_OUT	output	DQS gate window signal output (low bit) after compensating for read command path delay
[R,L]_DQSU_GATE_IN	input	DQS gate window signal feedback (high bit) after compensating for read command path delay
[R,L]_DQSU_GATE_OUT	output	DQS gate window signal output (high bit) after compensating for read command path delay
--Reference Pin		
RRP_[L0,L1,L2,R0,R1,R2]	input	External reference resistor pins, one for each bank. Provides a reference resistor to the power supply for on-die terminal resistor adjustment.
RRN_[L0,L1,L2,R0,R1,R2]	input	External reference resistor pins, one for each bank. Provides a reference resistor to the ground for on-die terminal resistor adjustment.
VREF_[L0,L1,L2,R0,R1,R2]	input	External reference voltage pins, one for each bank. Provides reference voltage input for each BANK
--ADC Pin		
VAUX[9,8,7,..0]	input	Input analog signals
Dedicated Pin		
--Configuration Pin, JTAG Pin		
CFG_DONE	Bidirectional (open-drain)	Dedicated pin for configuration state. Serves as a status output, driven low level before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released.
RST_N	input	Dedicated configuration input pin, internally weak pull-up, for restarting the configuration process, active-low. It is recommended that users externally pull up the RST_N with a resistor when using this pin. When this pin is low level, the FPGA enters a reset state, and all IOs are in the high-z state.
TCK	input	Dedicated JTAG test clock input pin
TMS	input	Dedicated JTAG test mode selection input pin
TDI	input	Dedicated JTAG test data input pin.
TDO	output	Dedicated JTAG test data output pin.
--Reference Pin		
REXT	input	Dedicated external high-precision resistor pin, with a resistance of 10k and an accuracy of 1%. Provides resistance for the bandgap.
--ADC Pin		
VA[1,0]	input	Dedicated analog input signals
VREF_EXT	input	Dedicated external reference 2.5V voltage.
Power Pin, Ground Pin		
VCC	POWER	Core power, 1.1V. Power supply for core logic
VCCAUX	POWER	3.3V auxiliary power supply for IOB, LDO, and other modules

PIN name	PIN type	PIN description
VCCIO[L0,L1,L2,R0,R1,R2]	POWER	IO BANK power, the banks on the left are BANKL0, BANKL1, BANKL2, and so on from top to down; the banks on the right side are BANKR0, BANKR1, BANKR2, and so on from top to down
VCCAUX_A	POWER	Power supply for ADC, BANDGAP, and POR
VSS	GROUND	GND relative to VCC&VCCAUX
VSSA	GROUND	GND relative to VCCAUX_A
VCCEFUSE	POWER	Efuse programming voltage
VCCIOCFG	POWER	BANKCFG power supply

Note: PGL22G_FBG256 has 186 general IOs.

2.2.1 Pinout Diagram

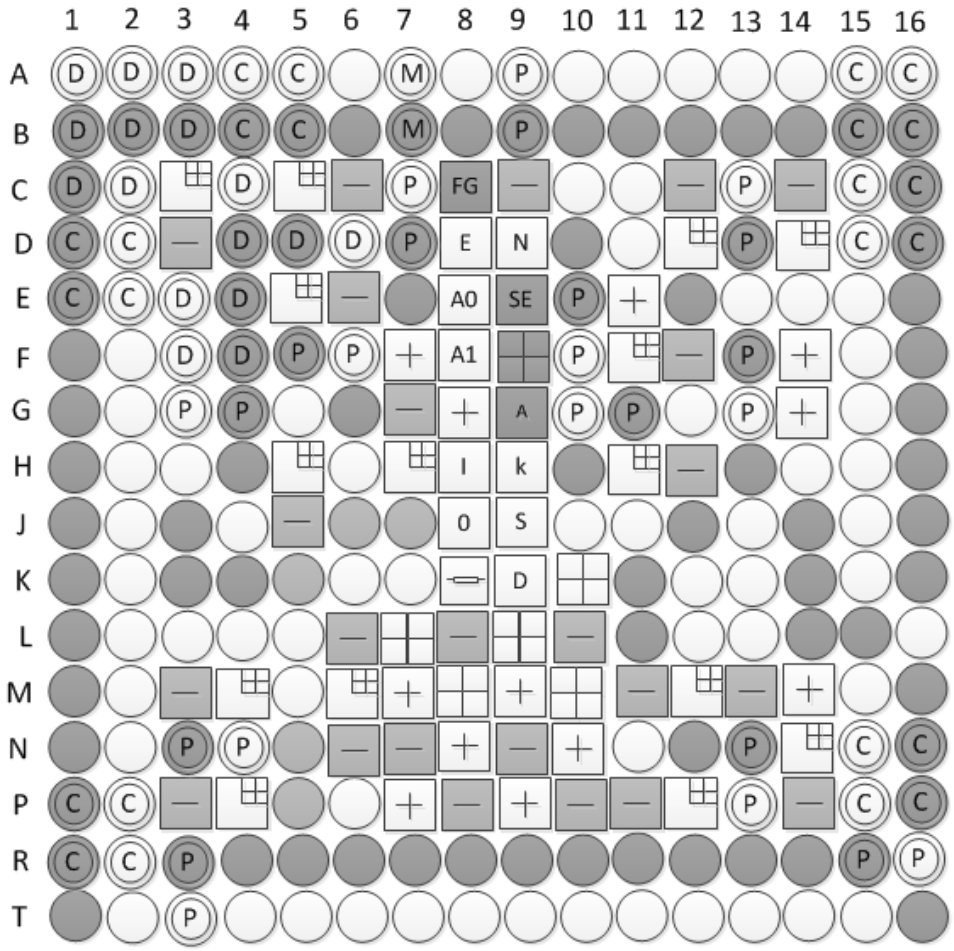

Figure 2-1 Pinout Diagram

Note: the Pinout symbols have the following meanings:

General IO	DIFFIO*	COMP(N) TRUE(P)	Dedicated IO		Other IO	
			REST_N	N	VSS	—
Multiplex IO	DIFFIO*/D0~D31	D D	CFG_DONE	D	VCC	+
	DIFFIO*/MODE*	M M	VREF_EXT	E	VCCAUX	
	DIFFIO*/BUSY	B B	VA1	A1	VDDIO*	
	DIFFIO*/CS_N	C C	VA0	A0	VSSA	A
	DIFFIO*/FCS_N	FC FC	REXT		VDDEFUSE	SE
	DIFFIO*/VREF	V V	TMS	S	VCCAUX_A	
	DIFFIO*/CLK*	C C	TCK	K	VDDIOCFG	FG
	DIFFIO*/PLL*	P P	TDI	I		
	DIFFIO*/RR*	R R	TDO	O		

2.2.2 IO Banks

Top view

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	L0	L0	L0	L0	L0	L0	L0	L0	L0	L0	R0	R0	R0	R0	R0	R0
B	L0	L0	L0	L0	L0	L0	L0	L0	L0	L0	R0	R0	R0	R0	R0	R0
C	L0	L0		L0			L0			L0	R0		R0		R1	R1
D	L1	L1		L0	L0	L0	L0			L0	R0		R0		R1	R1
E	L1	L1	L0	L0			L0			R0		R0	R0	R0	R1	R1
F	L1	L1	L0	L0	L1	L1				R0			R1		R1	R1
G	L1	L1	L1	L1	L1	L1				R1	R1	R1	R1		R1	R1
H	L1	L1	L1	L1		L1				R1			R1	R1	R1	R1
J	L1	L1	L1	L1		L2	L1			R1	R1	R1	R1	R1	R2	R2
K	L2	L2	L2	L2	L2	L2	L1				R2	R2	R2	R2	R2	R2
L	L2	L2	L2	L2	L2						R2	R2	R2	R2	R2	R2
M	L2	L2			L2										R2	R2
N	L2	L2	L2	L2	L2						R2	R2	R2		R2	R2
P	L2	L2			L2	L2							R2		R2	R2
R	L2	L2	L2	L2	L2	L2	L2	L2	R2	R2	R2	R2	R2	R2	R2	R2
T	L2	L2	L2	L2	L2	L2	L2	L2	R2	R2	R2	R2	R2	R2	R2	R2

Figure 2-2 IO Banks

2.2.3 Memory Grouping

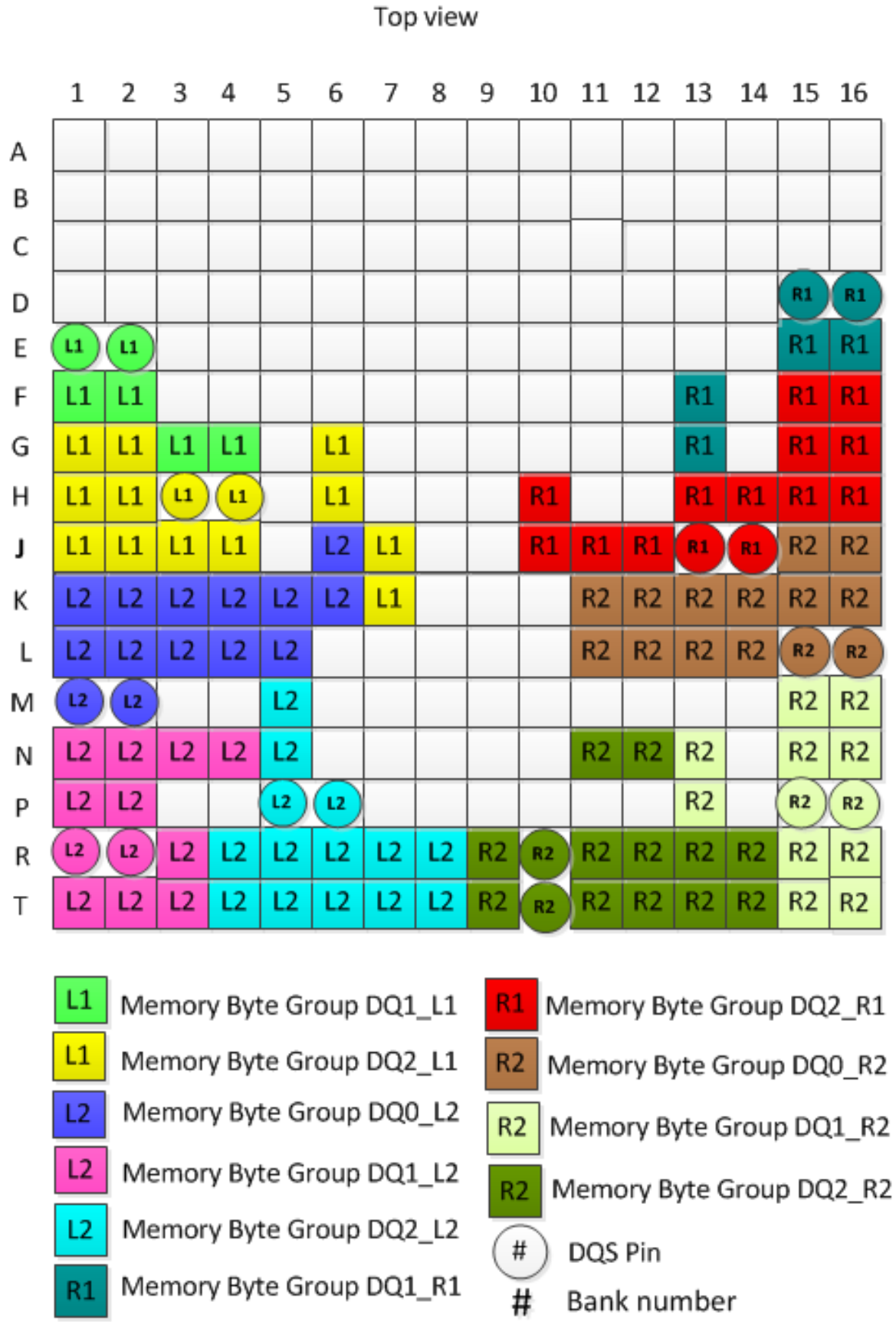

Figure 2-3 Memory Grouping

2.2.4 Power and GND Placement

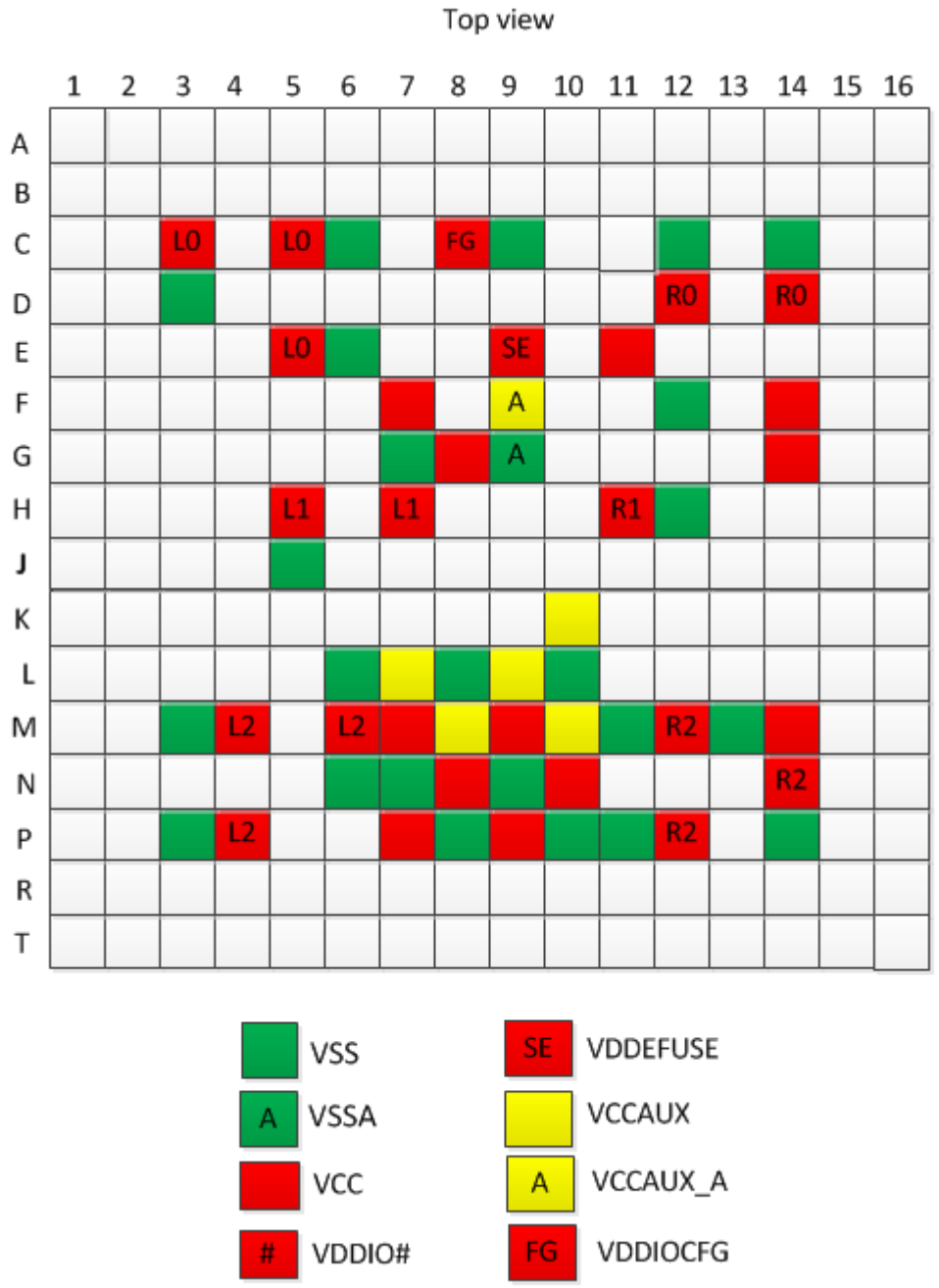

Figure 2-4 Power and GND Placement

2.2.5 Ball Name List

Table 2-3 Ball Name List

Bank Name	Ball Name (Function Name)	Ball Number	Memory Byte Group	Time Delay (ps)
BANKCFG	RST_N	D9		
BANKCFG	CFG_DONE	K9		
BANKCFG	TCK	H9		
BANKCFG	TMS	J9		
BANKCFG	TDI	H8		
BANKCFG	TDO	J8		
BANKCFG	VREF_EXT	D8		
BANKCFG	VA0	E8		54.2937
BANKCFG	VA1	F8		51.7296
BANKCFG	REXT	K8		
BANKL0	DIFFIO_L0_0_P/BUSY	E7		33.9649
BANKL0	DIFFIO_L0_3_P/IO_STATUS_C	B8		111.916
BANKL0	DIFFIO_L0_3_N/CFG_CLK	A8		114.199
BANKL0	DIFFIO_L0_4_P/FCS_N	D10		94.3845
BANKL0	DIFFIO_L0_4_N/CS_N	C10		88.025
BANKL0	DIFFIO_L0_5_P/MODE_0	B7		113.72
BANKL0	DIFFIO_L0_5_N/MODE_1	A7		116.101
BANKL0	DIFFIO_L0_6_P/MODE_2	B10		123.49
BANKL0	DIFFIO_L0_6_N/VREF_L0/CSO_DOUT	A10		124.7
BANKL0	DIFFIO_L0_7_P/RWSEL	B6		116.364
BANKL0	DIFFIO_L0_7_N/INIT_FLAG_N	A6		118.445
BANKL0	DIFFIO_L0_8_P/PLL0_CLKOUT_P	D7		60.849
BANKL0	DIFFIO_L0_8_N/PLL0_CLKOUT_N	C7		61.1062
BANKL0	DIFFIO_L0_9_P/CLK0_L0/DIFFCLK0_L0_P/PLL0_CLKFB_P/XTALA_L0	B5		114.302
BANKL0	DIFFIO_L0_9_N/CLK1_L0/DIFFCLK0_L0_N/PLL0_CLKFB_N/XTALB_L0	A5		121.611
BANKL0	DIFFIO_L0_10_P/CLK2_L0/DIFFCLK1_L0_P/PLL1_CLKIN0	B4		122.667
BANKL0	DIFFIO_L0_10_N/CLK3_L0/DIFFCLK1_L0_N/PLL1_CLKIN1	A4		119.311
BANKL0	DIFFIO_L0_11_P/PLL1_CLKIN2	B9		121.12
BANKL0	DIFFIO_L0_11_N/PLL1_CLKIN3	A9		124.223
BANKL0	DIFFIO_L0_12_P/D0	B3		119.266
BANKL0	DIFFIO_L0_12_N/RRN_L0/D1	A3		118.849
BANKL0	DIFFIO_L0_13_P/RRP_L0/D2	D5		57.0984
BANKL0	DIFFIO_L0_13_N/D3	D6		51.1101
BANKL0	DIFFIO_L0_14_P/D4	B2		117.421
BANKL0	DIFFIO_L0_14_N/D5	A2		116.543

Bank Name	Ball Name (Function Name)	Ball Number	Memory Byte Group	Time Delay (ps)
BANKL0	DIFFIO_L0_15_P/D6	D4		63.8651
BANKL0	DIFFIO_L0_15_N/D7	C4		62.5254
BANKL0	DIFFIO_L0_16_P/D8	B1		112.884
BANKL0	DIFFIO_L0_16_N/D9	A1		117.981
BANKL0	DIFFIO_L0_17_P/D10	E4		47.8823
BANKL0	DIFFIO_L0_17_N/D11	E3		45.0627
BANKL0	DIFFIO_L0_18_P/D12	C1		93.522
BANKL0	DIFFIO_L0_18_N/D13	C2		91.1554
BANKL0	DIFFIO_L0_19_P/D14	F4		44.535
BANKL0	DIFFIO_L0_19_N/D15	F3		42.3111
BANKL1	DIFFIO_L1_6_N/VREF_L1	G5		32.2202
BANKL1	DIFFIO_L1_8_P/PLL2_CLKOUT_P	F5		42.1327
BANKL1	DIFFIO_L1_8_N/PLL2_CLKOUT_N	F6		39.0311
BANKL1	DIFFIO_L1_9_P/CLK0_L1/DIFFCLK0_L1_P/PLL2_CLKFB_P/XTALA_L1	D1		95.5235
BANKL1	DIFFIO_L1_9_N/CLK1_L1/DIFFCLK0_L1_N/PLL2_CLKFB_N/XTALB_L1	D2		91.5143
BANKL1	DIFFIO_L1_10_P/CLK2_L1/DIFFCLK1_L1_P/PLL3_CLKIN0	E1	L_A15	84.8201
BANKL1	DIFFIO_L1_10_N/CLK3_L1/DIFFCLK1_L1_N/PLL3_CLKIN1	E2	L_A14	82.5384
BANKL1	DIFFIO_L1_11_P/PLL3_CLKIN2	G4	L_A13	47.1148
BANKL1	DIFFIO_L1_11_N/PLL3_CLKIN3	G3	L_A12	46.2927
BANKL1	DIFFIO_L1_12_P	F1	L_A11	81.4072
BANKL1	DIFFIO_L1_12_N/RRN_L1	F2		81.8278
BANKL1	DIFFIO_L1_13_P/RRP_L1	G6		42.9394
BANKL1	DIFFIO_L1_13_N	H6	L_A10	43.2864
BANKL1	DIFFIO_L1_14_P	G1	L_A9	78.8609
BANKL1	DIFFIO_L1_14_N	G2	L_RESET_N	79.5689
BANKL1	DIFFIO_L1_15_P	H4	L_A8	46.8207
BANKL1	DIFFIO_L1_15_N	H3	L_CKE	45.8728
BANKL1	DIFFIO_L1_16_P	H1	L_A7	82.1701
BANKL1	DIFFIO_L1_16_N	H2	L_A6	79.1875
BANKL1	DIFFIO_L1_17_P	J3	L_A5	42.7685
BANKL1	DIFFIO_L1_17_N	J4	L_A4	44.5721
BANKL1	DIFFIO_L1_18_P	J1	L_A3	83.2955
BANKL1	DIFFIO_L1_18_N	J2	L_A2	85.5844
BANKL1	DIFFIO_L1_19_P	J7	L_A1	48.0842
BANKL1	DIFFIO_L1_19_N	K7	L_A0	46.9213
BANKL2	DIFFIO_L2_0_P	K3	L_DQSU_GATE_OUT	60.6722
BANKL2	DIFFIO_L2_0_N	L3	L_DQSU_GA	65.2487

Bank Name	Ball Name (Function Name)	Ball Number	Memory Byte Group	Time Delay (ps)
			TE_IN	
BANKL2	DIFFIO_L2_1_P	K1	L_DMU	83.5264
BANKL2	DIFFIO_L2_1_N	K2	L_DQ15	80.8125
BANKL2	DIFFIO_L2_2_P	J6	L_DQ14	33.7101
BANKL2	DIFFIO_L2_2_N	K6	L_DQ13	32.9055
BANKL2	DIFFIO_L2_3_P	L1	L_DQ12	65.7679
BANKL2	DIFFIO_L2_3_N	L2	L_DQ11	70.5198
BANKL2	DIFFIO_L2_4_P	M1	L_DQSU	72.2523
BANKL2	DIFFIO_L2_4_N	M2	L_DQSU_N	65.3576
BANKL2	DIFFIO_L2_5_P	K4	L_DQ10	48.1719
BANKL2	DIFFIO_L2_5_N	L4	L_DQ9	47.5445
BANKL2	DIFFIO_L2_6_P	K5	L_DQ8	29.9347
BANKL2	DIFFIO_L2_6_N/VREF_L2	L5		31.2892
BANKL2	DIFFIO_L2_7_P	N1	L_CS_N	73.0222
BANKL2	DIFFIO_L2_7_N	N2	L_RAS_N	74.0535
BANKL2	DIFFIO_L2_8_P/PLL4_CLKOUT_P	R3	L_CAS_N	94.2504
BANKL2	DIFFIO_L2_8_N/PLL4_CLKOUT_N	T3	L_BA2	93.4058
BANKL2	DIFFIO_L2_9_P/CLK0_L2/DIFFCLK0_L2_P/PLL4_CLKFB_P/XTALA_L2	P1	L_BA1	77.6015
BANKL2	DIFFIO_L2_9_N/CLK1_L2/DIFFCLK0_L2_N/PLL4_CLKFB_N/XTALB_L2	P2	L_BA0	77.2835
BANKL2	DIFFIO_L2_10_P/CLK2_L2/DIFFCLK1_L2_P/PLL5_CLKIN0	R1	L_WE_N	85.4692
BANKL2	DIFFIO_L2_10_N/CLK3_L2/DIFFCLK1_L2_N/PLL5_CLKIN1	R2	L_ODT	81.5118
BANKL2	DIFFIO_L2_11_P/PLL5_CLKIN2	N3	L_CK	59.8083
BANKL2	DIFFIO_L2_11_N/PLL5_CLKIN3	N4	L_CK_N	56.7024
BANKL2	DIFFIO_L2_12_P	T1		91.5233
BANKL2	DIFFIO_L2_12_N/RRN_L2	T2		90.1063
BANKL2	DIFFIO_L2_13_P/RRP_L2	R7		72.3462
BANKL2	DIFFIO_L2_13_N	T7	L_DQ7	84.1576
BANKL2	DIFFIO_L2_14_P	R4	L_DQ6	77.1148
BANKL2	DIFFIO_L2_14_N	T4	L_DQ5	78.632
BANKL2	DIFFIO_L2_15_P	P5	L_DQSL	48.4971
BANKL2	DIFFIO_L2_15_N	P6	L_DQSL_N	54.4473
BANKL2	DIFFIO_L2_16_P	R5	L_DQ4	75.2718
BANKL2	DIFFIO_L2_16_N	T5	L_DQ3	78.0891
BANKL2	DIFFIO_L2_17_P	R8	L_DQ2	70.7083
BANKL2	DIFFIO_L2_17_N	T8	L_DQ1	78.5744
BANKL2	DIFFIO_L2_18_P	R6	L_DQ0	73.3085
BANKL2	DIFFIO_L2_18_N	T6	L_DML	77.146

Bank Name	Ball Name (Function Name)	Ball Number	Memory Byte Group	Time Delay (ps)
BANKL2	DIFFIO_L2_19_P	N5	L_DQSL_GATE_OUT	40.2253
BANKL2	DIFFIO_L2_19_N	M5	L_DQSL_GATE_IN	38.968
BANKR0	DIFFIO_R0_0_N/VAUX4	C11		26.3472
BANKR0	DIFFIO_R0_1_P/VAUX3	B13		70.9206
BANKR0	DIFFIO_R0_1_N/VAUX2	A13		72.3254
BANKR0	DIFFIO_R0_2_P/VAUX1	B11		65.2503
BANKR0	DIFFIO_R0_2_N/VAUX0	A11		67.5474
BANKR0	DIFFIO_R0_3_N/ECCLKIN	E13		42.2802
BANKR0	DIFFIO_R0_4_P/FCS2_N	B12		69.6444
BANKR0	DIFFIO_R0_4_N/BFCE_N	A12		71.6613
BANKR0	DIFFIO_R0_6_N/VREF_R0	D11		59.0174
BANKR0	DIFFIO_R0_7_P/VS1	B14		71.2695
BANKR0	DIFFIO_R0_7_N/VS0	A14		75.0903
BANKR0	DIFFIO_R0_8_P/PLL0_CLKIN0	D13		67.4135
BANKR0	DIFFIO_R0_8_N/PLL0_CLKIN1	C13		64.6017
BANKR0	DIFFIO_R0_9_P/CLK0_R0/DIFFCLK0_R0_P/PLL0_CLKIN2/XTALA_R0	B15		77.2615
BANKR0	DIFFIO_R0_9_N/CLK1_R0/DIFFCLK0_R0_N/PLL0_CLKIN3/XTALB_R0	A15		83.8704
BANKR0	DIFFIO_R0_10_P/CLK2_R0/DIFFCLK1_R0_P/PLL1_CLKFB_P	B16		88.3244
BANKR0	DIFFIO_R0_10_N/CLK3_R0/DIFFCLK1_R0_N/PLL1_CLKFB_N	A16		83.1333
BANKR0	DIFFIO_R0_11_P/PLL1_CLKOUT_P	E10		58.7395
BANKR0	DIFFIO_R0_11_N/PLL1_CLKOUT_N	F10		57.8999
BANKR0	DIFFIO_R0_12_N/RRN_R0/D17/ADR1	E14		50.3624
BANKR0	DIFFIO_R0_13_P/RRP_R0/D18/ADR2	E12		37.1236
BANKR1	DIFFIO_R1_6_N/VREF_R1	G12		32.5532
BANKR1	DIFFIO_R1_8_P/PLL2_CLKIN0	G11		51.3123
BANKR1	DIFFIO_R1_8_N/PLL2_CLKIN1	G10		50.8471
BANKR1	DIFFIO_R1_9_P/CLK0_R1/DIFFCLK0_R1_P/PLL2_CLKIN2/XTALA_R1	C16		102.44
BANKR1	DIFFIO_R1_9_N/CLK1_R1/DIFFCLK0_R1_N/PLL2_CLKIN3/XTALB_R1	C15		98.8505
BANKR1	DIFFIO_R1_10_P/CLK2_R1/DIFFCLK1_R1_P/PLL3_CLKFB_P	D16	R_A15	90.9851
BANKR1	DIFFIO_R1_10_N/CLK3_R1/DIFFCLK1_R1_N/PLL3_CLKFB_N	D15	R_A14	85.8662
BANKR1	DIFFIO_R1_11_P/PLL3_CLKOUT_P	F13	R_A13	41.8291
BANKR1	DIFFIO_R1_11_N/PLL3_CLKOUT_N	G13	R_A12	33.5733
BANKR1	DIFFIO_R1_12_P	E16	R_A11	81.2154
BANKR1	DIFFIO_R1_12_N/RRN_R1	E15		78.181
BANKR1	DIFFIO_R1_13_P/RRP_R1	H13		27.2278

Bank Name	Ball Name (Function Name)	Ball Number	Memory Byte Group	Time Delay (ps)
BANKR1	DIFFIO_R1_13_N	H14	R_A10	33.4265
BANKR1	DIFFIO_R1_14_P	F16	R_A9	75.312
BANKR1	DIFFIO_R1_14_N	F15	R_RESET_N	74.4289
BANKR1	DIFFIO_R1_15_P	J14	R_A8	36.0229
BANKR1	DIFFIO_R1_15_N	J13	R_CKE	33.7423
BANKR1	DIFFIO_R1_16_P	G16	R_A7	79.0877
BANKR1	DIFFIO_R1_16_N	G15	R_A6	72.4733
BANKR1	DIFFIO_R1_17_P	H10	R_A5	51.6056
BANKR1	DIFFIO_R1_17_N	J10	R_A4	50.1377
BANKR1	DIFFIO_R1_18_P	H16	R_A3	74.7535
BANKR1	DIFFIO_R1_18_N	H15	R_A2	74.9894
BANKR1	DIFFIO_R1_19_P	J12	R_A1	41.9398
BANKR1	DIFFIO_R1_19_N	J11	R_A0	43.5907
BANKR2	DIFFIO_R2_0_P	K14	R_DQSU_GATE_OUT	36.8714
BANKR2	DIFFIO_R2_0_N	K13	R_DQSU_GATE_IN	35.0893
BANKR2	DIFFIO_R2_1_P	J16	R_DMU	74.4218
BANKR2	DIFFIO_R2_1_N	J15	R_DQ15	73.6784
BANKR2	DIFFIO_R2_2_P	K11	R_DQ14	42.2595
BANKR2	DIFFIO_R2_2_N	K12	R_DQ13	41.3417
BANKR2	DIFFIO_R2_3_P	K16	R_DQ12	74.1886
BANKR2	DIFFIO_R2_3_N	K15	R_DQ11	77.6681
BANKR2	DIFFIO_R2_4_P	L15	R_DQSU	85.0193
BANKR2	DIFFIO_R2_4_N	L16	R_DQSU_N	85.8853
BANKR2	DIFFIO_R2_5_P	L11	R_DQ10	93.1869
BANKR2	DIFFIO_R2_5_N	L12	R_DQ9	92.0106
BANKR2	DIFFIO_R2_6_P	L14	R_DQ8	37.0396
BANKR2	DIFFIO_R2_6_N/VREF_R2	L13		35.388
BANKR2	DIFFIO_R2_7_P	M16	R_CS_N	78.5795
BANKR2	DIFFIO_R2_7_N	M15	R_RAS_N	80.0053
BANKR2	DIFFIO_R2_8_P/PLL4_CLKIN0	N13	R_CAS_N	58.8917
BANKR2	DIFFIO_R2_8_N/PLL4_CLKIN1	P13	R_BA2	62.0866
BANKR2	DIFFIO_R2_9_P/CLK0_R2/DIFFCLK0_R2_P/PLL4_CLKIN2/XTALA_R2	N16	R_BA1	88.3898
BANKR2	DIFFIO_R2_9_N/CLK1_R2/DIFFCLK0_R2_N/PLL4_CLKIN3/XTALB_R2	N15	R_BA0	95.7046
BANKR2	DIFFIO_R2_10_P/CLK2_R2/DIFFCLK1_R2_P/PLL5_CLKFB_P	P16	R_WE_N	97.9081
BANKR2	DIFFIO_R2_10_N/CLK3_R2/DIFFCLK1_R2_N/PLL5_CLKFB_N	P15	R_ODT	97.2606
BANKR2	DIFFIO_R2_11_P/PLL5_CLKOUT_P	R15	R_CK	113.046

Bank Name	Ball Name (Function Name)	Ball Number	Memory Byte Group	Time Delay (ps)
BANKR2	DIFFIO_R2_11_N/PLL5_CLKOUT_N	R16	R_CK_N	116.289
BANKR2	DIFFIO_R2_12_P	T16		89.5816
BANKR2	DIFFIO_R2_12_N/RRN_R2	T15		91.729
BANKR2	DIFFIO_R2_13_P/RRP_R2	R11		80.6103
BANKR2	DIFFIO_R2_13_N	T11	R_DQ7	79.5469
BANKR2	DIFFIO_R2_14_P	R14	R_DQ6	73.4387
BANKR2	DIFFIO_R2_14_N	T14	R_DQ5	83.3959
BANKR2	DIFFIO_R2_15_P	R10	R_DQSL	74.4033
BANKR2	DIFFIO_R2_15_N	T10	R_DQSL_N	76.87
BANKR2	DIFFIO_R2_16_P	R13	R_DQ4	77.2637
BANKR2	DIFFIO_R2_16_N	T13	R_DQ3	80.524
BANKR2	DIFFIO_R2_17_P	R9	R_DQ2	79.236
BANKR2	DIFFIO_R2_17_N	T9	R_DQ1	79.9163
BANKR2	DIFFIO_R2_18_P	R12	R_DQ0	94.7515
BANKR2	DIFFIO_R2_18_N	T12	R_DML	90.0916
BANKR2	DIFFIO_R2_19_P	N12	R_DQSL_GATE_OUT	52.2424
BANKR2	DIFFIO_R2_19_N	N11	R_DQSL_GATE_IN	51.1546
	VCC	E11		
	VCC	F7		
	VCC	F14		
	VCC	G8		
	VCC	G14		
	VCC	M7		
	VCC	M9		
	VCC	M14		
	VCC	N8		
	VCC	N10		
	VCC	P7		
	VCC	P9		
	VCCAUX	K10		
	VCCAUX	L7		
	VCCAUX	L9		
	VCCAUX	M8		
	VCCAUX	M10		
BANKCFG	VCCAUX_A	F9		
BANKCFG	VCCEFUSE	E9		
BANKCFG	VCCIOCFG	C8		
BANKL0	VCCIOL0	C3		

Bank Name	Ball Name (Function Name)	Ball Number	Memory Byte Group	Time Delay (ps)
BANKL0	VCCIOL0	C5		
BANKL0	VCCIOL0	E5		
BANKL1	VCCIOL1	H5		
BANKL1	VCCIOL1	H7		
BANKL2	VCCIOL2	M4		
BANKL2	VCCIOL2	M6		
BANKL2	VCCIOL2	P4		
BANKR0	VCCIOR0	D12		
BANKR0	VCCIOR0	D14		
BANKR1	VCCIOR1	F11		
BANKR1	VCCIOR1	H11		
BANKR2	VCCIOR2	M12		
BANKR2	VCCIOR2	N14		
BANKR2	VCCIOR2	P12		
	VSS	C6		
	VSS	C9		
	VSS	C12		
	VSS	C14		
	VSS	D3		
	VSS	E6		
	VSS	F12		
	VSS	G7		
	VSS	H12		
	VSS	J5		
	VSS	L6		
	VSS	L8		
	VSS	L10		
	VSS	M3		
	VSS	M11		
	VSS	M13		
	VSS	N6		
	VSS	N7		
	VSS	N9		
	VSS	P3		
	VSS	P8		
	VSS	P10		
	VSS	P11		
	VSS	P14		
BANKCFG	VSSA	G9		

2.2.6 Thermal Resistance

Table 2-4 Thermal Resistance

θJA(℃/W) (Flow: 0m/s)	**θJB (℃/W)**	**θJC (℃/W)**	**θJA(℃/W) (Flow: 1m/s)**	**θJA(℃/W) (Flow: 2m/s)**
20.7	7.9	9.5	18.7	17.6

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