PK03015_PGC4KD_FBG256

(V1.2)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.2	30.12.2020	Initial release

About this Manual

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Chapter 1 Introduction to Packaging

The PGC4KD_FBG256 device is packaged with a Wire Bond BGA. Its package size is 17mmx17mm, with 256 solder balls, a pitch of 1.0mm, and a maximum package thickness of 1.57mm.

Chapter 2 Package Dimension and Pins

2.1 Package Outline Dimension

Table 2-1 Dimensional Data

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	1.27	1.42	1.57	c	0.31	0.35	0.39
A1	0.32	0.37	0.42	e	-	1.0	-
A2	1.0	1.05	1.10	b	0.45	0.50	0.55
D	16.9	17.0	17.1	aaa	-	-	0.20
E	16.9	17.0	17.1	bbb	-	-	0.25
D1	-	15.0	-	ddd	-	-	0.20
E1	-	15.0	-	eee	-	-	0.25

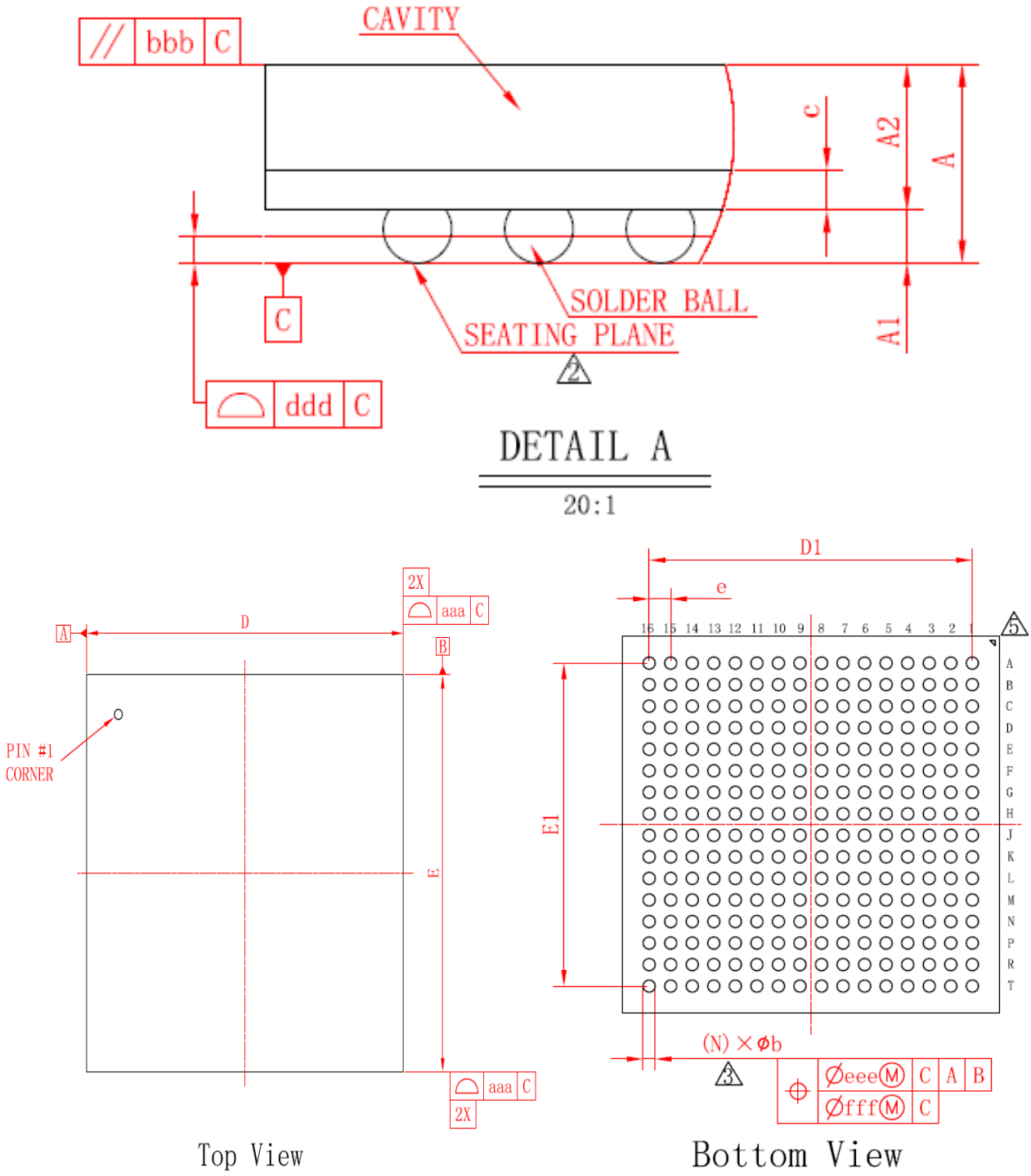

Figure 2-1 Package Outline Drawing (POD)

2.2 Pin Description

The PGC4KD_FBG256 device has 207 user I/Os.

Table 2-2 Device Pin Definitions

Pin Name	Pin Type	Direction	Pin Description
User I/O Pin			
DIFF[I,IO]_XX_NN[P,N]	User pin	Input/Output	User I/O. (1) DIFFI indicates support for differential signal input and pseudo-differential output; DIFFIO indicates support for differential signal input and true differential output, which can be used for transmitting and receiving LVDS signals; (2) “XX” denotes the Bank number, with possible values being B0, B1, B2, B3, B4, and B5; (3) “NN” denotes the sequence number of the programmable I/O group within the Bank, starting from 0 and increasing incrementally; (4) [P,N]: “P” denotes the positive side of the differential pair, and “N” denotes the negative side; During power-up, the user I/O is at a low voltage; After power-up is complete but before configuration, the general user I/O is at pull-down status; During configuration, the user I/O is at pull-down status;
Configuration[1]			
INIT_FLAG_N	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, with an internal weak pull-up resistor. When used as a configuration pin: During power-up, it is at a low voltage; After power-up is complete before configuration, it is open-drain at weak pull-up status; During configuration, it is open-drain at weak pull-up status; During initialization, the pin can be driven to a low voltage by an external input to indicate an error or to delay configuration. During configuration, the pin serves as an indicator output for configuration errors, where a low voltage indicates an error has occurred;
CFG_DONE	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, with an internal weak pull-up resistor. When it is used as configuration pin, it serves as an indicator output for configuration completion, where a high voltage indicates configuration is complete; Before or during configuration, the pin is driven to a low voltage; after configuration is complete, the pin can continue to be driven to a low voltage by an external source. If the internal start-up timing detects CFG_DONE at a low voltage, the internal start-up circuitry maintains its state until CFG_DONE goes high to continue the start-up process;
RSTN	Multi-function pin	Input	Configurable multiplexed reset pin, with an internal weak pull-up resistor. When it is used as a reset pin, it serves to restart the configuration process, active low. At this situation, it must be pulled up with an external resistor (internal weak pull-up resistor typically has a value of over 20kOhms, with a relatively weak pull-up strength); when the pin is at a low voltage, the CPLD enters reset state, with all I/Os in a weak pull-down status;
CFG_CLK	Multi-function pin	Input/Output	Configurable multiplexed clock pin, with an internal weak pull-up resistor. When it is used as a configuration pin: In slave SPI configuration mode, the pin serves as a clock

Pin Name	Pin Type	Direction	Pin Description
			input to acquire configuration data from an external source; In master SPI configuration mode, the pin serves as a clock output to acquire configuration data from an external source; in this mode, a 1kOhms pull-up resistor is needed; Master SPI mode and slave SPI mode are allowed to be enabled simultaneously, but using them at the same time is not permitted;
TCK	Multi-function pin	Input	Multiplexed JTAG test clock input pin; requires an external 4.7kOhms pull-down resistor;
TMS	Multi-function pin	Input	Multiplexed JTAG test mode select input pin; with an internal weak pull-up resistor, pulled up to VCCIO0;
TDI	Multi-function pin	Input	Multiplexed JTAG test data input pin; with an internal weak pull-up resistor, pulled up to VCCIO0;
TDO	Multi-function pin	Output	Multiplexed JTAG test data output pin; with an internal weak pull-up resistor, pulled up to VCCIO0.
JTAGEN	Multi-function pin	Input	Optional JTAG port behaviour control pin, usually used in user mode, when JTAG pins are configured as configuration I/Os, this pin is user I/O, with the state controlled by the user; when JTAG pins serve as user I/Os, JTAGEN serves as a dedicated input used to control the availability of JTAG pins; the default state is weak pull-down; when JTAGEN is configured as a dedicated I/O: (1) When at a low voltage, the JTAG pins function as user I/Os; (2) When at a high voltage, the JTAG pins function as JTAG configuration port.
FCS_N	Multi-function pin	Output	Configurable multiplexed pin, used for master SPI configuration mode, (1) In master SPI mode, outputs an active-low chip select signal to an external Flash; (2) After configuration is completed, it can be used as a user I/O.
MISO_SO	Multi-function pin	Input/Output	Configurable multiplexed pin; (1) MISO, serial data input in master SPI mode; (2) SO, serial data output in slave SPI mode; Master and slave SPI modes are allowed to be enabled simultaneously, but using them at the same time is not permitted.
MOSI_SI	Multi-function pin	Input/Output	Configurable multiplexed pin; (1) MOSI, serial data output in master SPI mode; (2) SI, serial data input in slave SPI mode; Master and slave SPI modes are allowed to be enabled simultaneously, but using them at the same time is not permitted.
FCSI_N	Multi-function pin	Input	Configurable multiplexed pin, with an internal weak pull-up resistor; In slave SPI mode, active-low chip select input.
SCL	Multi-function pin	Input (Open-drain)	Configurable multiplexed pin, clock input in slave I2C mode; requires an external weak pull-up resistor.
SDA	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, data input/output in I2C mode; requires an external weak pull-up resistor.

Pin Name	Pin Type	Direction	Pin Description
SPAL_CLK	Multi-function pin	Input	Clock input in slave parallel X16 configuration mode.
SPAL_CS_N	Multi-function pin	Input	Chip select input in slave parallel X16 configuration mode. Active-low
SPAL_RDWR_N	Multi-function pin	Input	Read/write control input in slave parallel X16 configuration mode; 1: read; 0: write.
SPAL_BUSY	Multi-function pin	Output	Busy indicator in slave parallel X16 configuration mode; During readback, if the data is not ready, SPAL_BUSY changes to high voltage.
SPAL_D15~SPAL_D0	Multi-function pin	Input/Output	Data bus in slave parallel X16 configuration mode.
Clock, PLL			
CLK[0,1,2][P,N]_[B0,B1,…,B5]	Multi-function pin	Input	Global clock input pin; can also be used as user I/O; (1) [0,1,2]: clock pin numbers; (2) [P,N]: positive and negative sides of the differential clock pins; (3) [B0,B1,…,B5]: bank numbers.
PLL[0,1]_CLKIN_[P,N]	Multi-function pin	Input	PLL input. PLL can choose to directly input a clock from these pins; they can also be used as user I/Os; (1) [0,1]: corresponds to PLL0 and PLL1; (2) [P,N]: positive and negative sides of the differential clock pins.
PLL[0,1]_CLKFB_[P,N]	Multi-function pin	Input	Optional PLL feedback clock input. PLL can select to feedback clock externally from these pins; they can also be used as user I/Os; (1) [0,1]: corresponds to PLL0 and PLL1; (2) [P,N]: positive and negative sides of the differential clock pins.
Power			
VCC		Power	External power supply of 2.5V or 3.3V, providing power to the core logic.
VCCIO[0,1,2,3,4,5]		Power	I/O Bank power.
VSS		Ground	Ground associated with VCC;

Note:

1. When the configured multi-function pin is used as a user I/O, its status is the same as the user I/O pin.

2.2.1 Pin Name list

Table 2-3 Pin Name List

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B0	DIFFI_B0_0N/CFG_DONE	C13	IO_1_N	63.4575
B0	DIFFI_B0_0P/INIT_FLAG_N	A13	IO_1_P	65.7533
B0	DIFFIO_B0_1N/SPAL_CLK	A15	IO_2_N	69.1434
B0	DIFFIO_B0_1P/SPAL_CS_N	B14	IO_2_P	64.3254
B0	DIFFIO_B0_3N/SPAL_RDWR_N	B12	IO_4_N	41.9117
B0	DIFFIO_B0_3P/SPAL_BUSY	C12	IO_4_P	46.0724
B0	DIFFIO_B0_5N/SPAL_D15	A14	IO_6_N	70.4122

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B0	DIFFIO_B0_5P/SPAL_D14	B13	IO_6_P	68.0534
B0	DIFFIO_B0_7N/SPAL_D13	A12	IO_8_N	59.6199
B0	DIFFIO_B0_7P/SPAL_D12	B11	IO_8_P	60.6499
B0	DIFFI_B0_8N/SPAL_D11	D11	IO_9_N	55.8104
B0	DIFFI_B0_8P/SPAL_D10	F10	IO_9_P	56.5298
B0	DIFFIO_B0_9N/SPAL_D9	C11	IO_10_N	58.1813
B0	DIFFIO_B0_9P/SPAL_D8	A11	IO_10_P	63.8063
B0	DIFFI_B0_10N/RSTN	B10	IO_11_N	41.5524
B0	DIFFI_B0_10P/JTAGEN	C10	IO_11_P	48.8136
B0	DIFFIO_B0_11N/SPAL_D7	E10	IO_12_N	31.5889
B0	DIFFIO_B0_11P/SPAL_D6	D10	IO_12_P	39.0185
B0	DIFFIO_B0_13N/SPAL_D5	E11	IO_14_N	38.3439
B0	DIFFIO_B0_13P/SPAL_D4	F9	IO_14_P	44.8077
B0	DIFFIO_B0_15N/SPAL_D3	A10	IO_16_N	64.2795
B0	DIFFIO_B0_15P/SPAL_D2	B9	IO_16_P	60.9539
B0	DIFFI_B0_16N/SDA/CLK0N_B0	C9	IO_17_N	54.2445
B0	DIFFI_B0_16P/SCL/CLK0P_B0	A9	IO_17_P	66.2538
B0	DIFFIO_B0_17N/SPAL_D1	D9	IO_18_N	46.3332
B0	DIFFIO_B0_17P/SPAL_D0	F8	IO_18_P	49.7109
B0	DIFFIO_B0_19N	E9	IO_20_N	40.3452
B0	DIFFIO_B0_19P	D8	IO_20_P	38.0186
B0	DIFFIO_B0_21N/CLK1N_B0	A8	IO_22_N	65.1141
B0	DIFFIO_B0_21P/CLK1P_B0	C8	IO_22_P	63.2941
B0	DIFFI_B0_22N/TMS	B8	IO_23_N	60.1182
B0	DIFFI_B0_22P/TCK	A7	IO_23_P	60.1908
B0	DIFFIO_B0_23N	E8	IO_24_N	33.7143
B0	DIFFIO_B0_23P	F7	IO_24_P	35.2979
B0	DIFFI_B0_24N	D7	IO_25_N	50.39
B0	DIFFI_B0_24P	E6	IO_25_P	52.4149
B0	DIFFIO_B0_25N	C7	IO_26_N	39.3423
B0	DIFFIO_B0_25P	B7	IO_26_P	40.6147
B0	DIFFI_B0_26N/TDI	A6	IO_27_N	63.3012
B0	DIFFI_B0_26P/TDO	C6	IO_27_P	57.1469
B0	DIFFIO_B0_27N	E7	IO_28_N	42.2474
B0	DIFFIO_B0_27P	D6	IO_28_P	39.566
B0	DIFFIO_B0_29N	B4	IO_30_N	82.5837
B0	DIFFIO_B0_29P	A3	IO_30_P	83.4241
B0	DIFFIO_B0_31N	B6	IO_32_N	57.6025
B0	DIFFIO_B0_31P	A5	IO_32_P	57.9984

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B0	DIFFIO_B0_33N	C5	IO_34_N	66.8022
B0	DIFFIO_B0_33P	A4	IO_34_P	63.9071
B0	DIFFI_B0_34P	B3	IO_35_P	69.1886
B0	DIFFIO_B0_35N	B5	IO_36_N	69.1897
B0	DIFFIO_B0_35P	C4	IO_36_P	64.3873
B1	DIFFI_B1_0P/PLL1_CLKFB_P	D14	IO_43_P	69.0177
B1	DIFFI_B1_0N/PLL1_CLKFB_N	E15	IO_43_N	67.6809
B1	DIFFI_B1_1P	C15	IO_44_P	75.618
B1	DIFFI_B1_1N	B16	IO_44_N	80.6547
B1	DIFFI_B1_2P/PLL1_CLKIN_P	D16	IO_45_P	69.6686
B1	DIFFI_B1_2N/PLL1_CLKIN_N	E14	IO_45_N	61.3214
B1	DIFFI_B1_5P	C16	IO_48_P	76.9167
B1	DIFFI_B1_5N	D15	IO_48_N	75.8922
B1	DIFFI_B1_6P	E16	IO_49_P	59.9578
B1	DIFFI_B1_6N	F15	IO_49_N	59.5562
B1	DIFFI_B1_7P	F13	IO_50_P	60.8149
B1	DIFFI_B1_7N	G12	IO_50_N	66.2335
B1	DIFFI_B1_8P	F14	IO_51_P	54.1622
B1	DIFFI_B1_8N	F16	IO_51_N	58.0693
B1	DIFFI_B1_9P	F12	IO_52_P	49.864
B1	DIFFI_B1_9N	G13	IO_52_N	47.4442
B1	DIFFI_B1_12P	G15	IO_55_P	49.9564
B1	DIFFI_B1_12N	G14	IO_55_N	34.7652
B1	DIFFI_B1_13P	G11	IO_56_P	49.5992
B1	DIFFI_B1_13N	H12	IO_56_N	49.0021
B1	DIFFI_B1_14P	G16	IO_57_P	56.5848
B1	DIFFI_B1_14N	H15	IO_57_N	56.9157
B1	DIFFI_B1_15P	H13	IO_58_P	49.1428
B1	DIFFI_B1_15N	J12	IO_58_N	51.8341
B1	DIFFI_B1_16P/CLK0P_B1	H14	IO_59_P	53.838
B1	DIFFI_B1_16N/CLK0N_B1	H16	IO_59_N	59.1551
B1	DIFFI_B1_17P	J16	IO_60_P	62.0209
B1	DIFFI_B1_17N	J14	IO_60_N	65.0302
B1	DIFFI_B1_18P	J15	IO_61_P	53.0739
B1	DIFFI_B1_18N	K16	IO_61_N	56.6694
B1	DIFFI_B1_19P	H11	IO_62_P	50.5592
B1	DIFFI_B1_19N	J13	IO_62_N	48.0258
B1	DIFFI_B1_20P	K14	IO_63_P	44.2202
B1	DIFFI_B1_20N	K15	IO_63_N	50.2501

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B1	DIFFI_B1_21P	J11	IO_64_P	50.9108
B1	DIFFI_B1_21N	L12	IO_64_N	47.0789
B1	DIFFI_B1_22P	L16	IO_65_P	57.5539
B1	DIFFI_B1_22N	L14	IO_65_N	59.6944
B1	DIFFI_B1_23P	K13	IO_66_P	37.9488
B1	DIFFI_B1_23N	K12	IO_66_N	37.3626
B1	DIFFI_B1_24P	L15	IO_67_P	56.2338
B1	DIFFI_B1_24N	M16	IO_67_N	58.9671
B1	DIFFI_B1_25P	K11	IO_68_P	54.3946
B1	DIFFI_B1_25N	L13	IO_68_N	50.7557
B1	DIFFI_B1_28P	M14	IO_71_P	48.9068
B1	DIFFI_B1_28N	M15	IO_71_N	43.7402
B1	DIFFI_B1_29P	N15	IO_72_P	78.9092
B1	DIFFI_B1_29N	P16	IO_72_N	80.2664
B1	DIFFI_B1_30P	N16	IO_73_P	60.5159
B1	DIFFI_B1_30N	N14	IO_73_N	68.5622
B1	DIFFI_B1_33P	P15	IO_76_P	66.513
B1	DIFFI_B1_33N	R16	IO_76_N	66.8313
B2	DIFFI_B2_0N	R14	IO_85_N	69.0635
B2	DIFFI_B2_0P	T15	IO_85_P	71.0375
B2	DIFFI_B2_1N/MOSI_SI	P13	IO_86_N	74.5425
B2	DIFFI_B2_1P/FCSI_N	R12	IO_86_P	78.0666
B2	DIFFI_B2_3N	T13	IO_88_N	71.6114
B2	DIFFI_B2_3P	P12	IO_88_P	67.2857
B2	DIFFI_B2_5N	T12	IO_90_N	61.0759
B2	DIFFI_B2_5P	R11	IO_90_P	58.1198
B2	DIFFI_B2_7N	T14	IO_92_N	88.8413
B2	DIFFI_B2_7P	R13	IO_92_P	88.4109
B2	DIFFI_B2_8N	N11	IO_93_N	46.8137
B2	DIFFI_B2_8P	M10	IO_93_P	39.2253
B2	DIFFI_B2_9N	P11	IO_94_N	60.3815
B2	DIFFI_B2_9P	T11	IO_94_P	53.3188
B2	DIFFI_B2_10N	M11	IO_95_N	53.762
B2	DIFFI_B2_10P	N10	IO_95_P	52.8717
B2	DIFFI_B2_11N	R10	IO_96_N	38.043
B2	DIFFI_B2_11P	P10	IO_96_P	47.2416
B2	DIFFI_B2_12N	L10	IO_97_N	57.6605
B2	DIFFI_B2_12P	M9	IO_97_P	57.145
B2	DIFFI_B2_13N	T10	IO_98_N	58.4659

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B2	DIFFI_B2_13P	R9	IO_98_P	53.7833
B2	DIFFI_B2_15N/CLK1N_B2	P9	IO_100_N	51.9282
B2	DIFFI_B2_15P/CLK1P_B2	T9	IO_100_P	59.9265
B2	DIFFI_B2_17N	N9	IO_102_N	34.9712
B2	DIFFI_B2_17P	M8	IO_102_P	26.3783
B2	DIFFI_B2_18N	L9	IO_103_N	57.1413
B2	DIFFI_B2_18P	N8	IO_103_P	57.5046
B2	DIFFI_B2_19N	T8	IO_104_N	65.532
B2	DIFFI_B2_19P	P8	IO_104_P	55.0523
B2	DIFFI_B2_21N/CLK0N_B2	R8	IO_106_N	55.8715
B2	DIFFI_B2_21P/CLK0P_B2	T7	IO_106_P	57.5592
B2	DIFFI_B2_23N	L8	IO_108_N	46.8925
B2	DIFFI_B2_23P	M6	IO_108_P	44.2761
B2	DIFFI_B2_24N	N7	IO_109_N	44.5391
B2	DIFFI_B2_24P	M7	IO_109_P	45.6706
B2	DIFFI_B2_25N	P7	IO_110_N	73.734
B2	DIFFI_B2_25P	R7	IO_110_P	66.2394
B2	DIFFI_B2_26N	L7	IO_111_N	59.6521
B2	DIFFI_B2_26P	N6	IO_111_P	54.1452
B2	DIFFI_B2_27N/MISO_SO	T6	IO_112_N	65.2404
B2	DIFFI_B2_27P/CFG_CLK	P6	IO_112_P	54.8088
B2	DIFFI_B2_29N	R6	IO_114_N	60.5504
B2	DIFFI_B2_29P	T5	IO_114_P	54.5454
B2	DIFFI_B2_31N	R4	IO_116_N	69.2609
B2	DIFFI_B2_31P	T3	IO_116_P	76.4199
B2	DIFFI_B2_33N	P5	IO_118_N	63.3807
B2	DIFFI_B2_33P/FCS_N	R5	IO_118_P	59.2287
B2	DIFFI_B2_34N	R3	IO_119_N	87.231
B2	DIFFI_B2_34P	T2	IO_119_P	87.6233
B2	DIFFI_B2_35N	T4	IO_120_N	56.0675
B2	DIFFI_B2_35P	P4	IO_120_P	55.3215
B3	DIFFI_B3_2P	L1	IO_129_P	61.2948
B3	DIFFI_B3_2N	L3	IO_129_N	60.9435
B3	DIFFI_B3_3P	K4	IO_130_P	60.937
B3	DIFFI_B3_3N	L5	IO_130_N	57.7443
B3	DIFFI_B3_4P/CLK0P_B3	L2	IO_131_P	57.9072
B3	DIFFI_B3_4N/CLK0N_B3	M1	IO_131_N	62.5957
B3	DIFFI_B3_5P	K5	IO_132_P	41.9713
B3	DIFFI_B3_5N	L4	IO_132_N	49.2574

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B3	DIFFI_B3_7P	N2	IO_134_P	68.9476
B3	DIFFI_B3_7N	P1	IO_134_N	68.146
B3	DIFFI_B3_8P	M3	IO_135_P	66.238
B3	DIFFI_B3_8N	N1	IO_135_N	71.107
B3	DIFFI_B3_10P	M2	IO_137_P	77.5544
B3	DIFFI_B3_10N	N3	IO_137_N	75.2454
B3	DIFFI_B3_11P	R1	IO_138_P	87.8422
B3	DIFFI_B3_11N	P2	IO_138_N	84.6267
B4	DIFFI_B4_0P	G1	IO_141_P	66.3785
B4	DIFFI_B4_0N	H2	IO_141_N	56.902
B4	DIFFI_B4_1P	H4	IO_142_P	37.7858
B4	DIFFI_B4_1N	J6	IO_142_N	39.5012
B4	DIFFI_B4_2P	H3	IO_143_P	54.3361
B4	DIFFI_B4_2N	H1	IO_143_N	58.0439
B4	DIFFI_B4_3P/CLK0P_B4	J1	IO_144_P	61.0701
B4	DIFFI_B4_3N/CLK0N_B4	J3	IO_144_N	58.4746
B4	DIFFI_B4_4P	J2	IO_145_P	52.8596
B4	DIFFI_B4_4N	K1	IO_145_N	55.2138
B4	DIFFI_B4_5P	H5	IO_146_P	48.0549
B4	DIFFI_B4_5N	J4	IO_146_N	50.0303
B4	DIFFI_B4_6P	K3	IO_147_P	49.2855
B4	DIFFI_B4_6N	K2	IO_147_N	49.4422
B4	DIFFI_B4_7P	J5	IO_148_P	48.7848
B4	DIFFI_B4_7N	K6	IO_148_N	47.2149
B5	DIFFI_B5_1P	B1	IO_154_P	70.8195
B5	DIFFI_B5_1N	C2	IO_154_N	71.4755
B5	DIFFI_B5_2P/PLL0_CLKFB_P	D3	IO_155_P	67.2938
B5	DIFFI_B5_2N/PLL0_CLKFB_N	D1	IO_155_N	67.1119
B5	DIFFI_B5_4P/PLL0_CLKIN_P	E2	IO_157_P	61.7599
B5	DIFFI_B5_4N/PLL0_CLKIN_N	E3	IO_157_N	56.9317
B5	DIFFI_B5_5P	C1	IO_158_P	86.0455
B5	DIFFI_B5_5N	D2	IO_158_N	86.9259
B5	DIFFI_B5_8P/CLK0P_B5	E1	IO_161_P	59.8333
B5	DIFFI_B5_8N/CLK0N_B5	F2	IO_161_N	59.7329
B5	DIFFI_B5_9P	F4	IO_162_P	39.8999
B5	DIFFI_B5_9N	G6	IO_162_N	44.7465
B5	DIFFI_B5_10P	F3	IO_163_P	61.1147
B5	DIFFI_B5_10N	F1	IO_163_N	62.1014
B5	DIFFI_B5_11P	G5	IO_164_P	36.696

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B5	DIFFI_B5_11N	G4	IO_164_N	43.0566
B5	DIFFI_B5_12P	G2	IO_165_P	46.9519
B5	DIFFI_B5_12N	G3	IO_165_N	47.2483
B5	DIFFI_B5_13P	F5	IO_166_P	47.3042
B5	DIFFI_B5_13N	H6	IO_166_N	54.4022
	NC	A2		
	VCC	A1		
	VCC	A16		
	VCC	G7		
	VCC	G10		
	VCC	K7		
	VCC	K10		
	VCC	T1		
	VCC	T16		
	VCCIO0	D5		
	VCCIO0	D12		
	VCCIO0	G8		
	VCCIO0	G9		
	VCCIO1	E13		
	VCCIO1	H10		
	VCCIO1	J10		
	VCCIO1	M13		
	VCCIO2	K8		
	VCCIO2	K9		
	VCCIO2	N5		
	VCCIO2	N12		
	VCCIO3	M4		
	VCCIO4	H7		
	VCCIO4	J7		
	VCCIO5	E4		
	VSS	B2		
	VSS	B15		
	VSS	C3		
	VSS	C14		
	VSS	D4		
	VSS	D13		
	VSS	E5		
	VSS	E12		
	VSS	F6		

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
	VSS	F11		
	VSS	H8		
	VSS	H9		
	VSS	J8		
	VSS	J9		
	VSS	L6		
	VSS	L11		
	VSS	M5		
	VSS	M12		
	VSS	N4		
	VSS	N13		
	VSS	P3		
	VSS	P14		
	VSS	R2		
	VSS	R15		

2.2.2 Thermal Resistance

Table 2-4 Thermal Resistance Data

θJA(℃/W) (Flow: 0m/s)	θJB (℃/W)	θJC (℃/W)	θJA(℃/W) (Flow: 1m/s)	θJA(℃/W) (Flow: 2m/s)
25.5	16.4	12.1	21.6	20.5

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