PK02005_PGL12G_LPG144

(V1.2)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.2	30.06.2020	Initial release

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
POD	Package Outline Drawing
QFP	Quad Flat Package

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Chapter 1 Introduction to Packaging

The PGL12G_LPG144 device uses a wire bonding Quad Flat Package (QFP) form factor. Its package size is 20mm x 20mm, with 144 pins, a pin pitch of 0.5mm, and a maximum package thickness of 1.60mm.

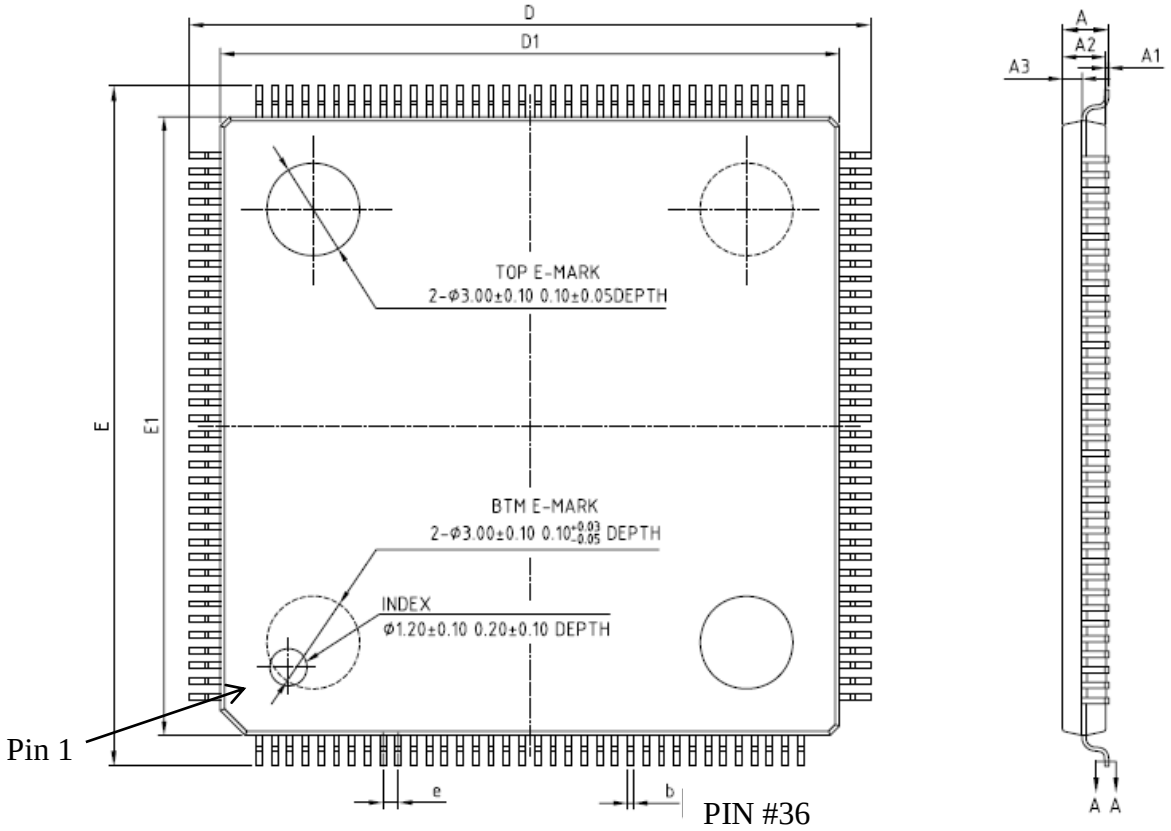
Chapter 2 Package Dimension and Pins

2.1 Package Outline Dimension

Table 2-1 Dimensional Data

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
D	21.80	22.00	22.20	A	n/a	n/a	1.60
D1	19.90	20.00	20.10	A1	0.05	n/a	0.15
E	21.80	22.00	22.20	A2	1.35	1.40	1.45
E1	19.90	20.00	20.10	A3	0.59	0.64	0.69
e	0.40	0.50	0.60	b	0.17	n/a	0.27
L	0.45	0.60	0.75	b1	0.17	0.20	0.23
c	0.127	n/a	0.18	c1	0.119	0.127	0.135



Note: PIN #1 indicates the position of the first pin

Figure 2-1 Package Outline Dimension (POD)

2.2 Pin Description

Table 2-1 Device Pin Definitions

PIN name	PIN type	PIN description
USER IO PIN		
DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]	Input/Output	All general USER IOs are marked as DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]. DIFFIO: indicates that all user IOs support differential input/output, such as LVDS; [L0, L1, L2, R0, R1, R2]: indicate BANK names [0…n]: indicates the unique differential pair number in the BANK; [N, P]: N indicates the negative side of the differential pair and P represents the positive side.

PIN name	PIN type	PIN description
Multiplexed Pin		
DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]/XXX		Multiplexed pins are marked as DIFFIO_[L0,L1,L2,R0,R1,R2]_[0…n]_[N,P]/XXX, where XXX indicates one or more of the functions described below. When the multiplexed pin is not used for special applications, it can serve as a general IO
--Configuration Pin		
MODE_2, MODE_1, MODE_0	input	They are used for configuration mode selection during configuration, as follows: 000: JTAG 001: Master SPI (X1, X2, X4, X8) 010: Master BPI (X8, X16) 011: Slave Serial (X1) 100: Slave Parallel (X8, X16, X32) 101: Slave SPI (X1) 111: Internal Master SPI (X1, X2, X4)
INIT_FLAG_N	Bidirectional (open-drain)	When the FPGA powers up during configuration, the pin is driven to a low voltage. Once the FPGA completes initialization, the pin is released. During configuration, this pin serves as an output for the configuration error indication state. During the configuration or initialization process, this pin can also accept an external low-voltage input to indicate an error or delay the configuration.
CFG_CLK	Input/Output	Configuration Clock Pin. In the slave mode, the pin serves as a clock input to obtain configuration data from external sources; In the master mode, the pin serves as a clock output to obtain configuration data from external sources;
D[31, 30…1, 0]	Input/Output	32-bit configuration data bus input/output pin: (1) In the Master SPI X1 configuration mode, D[0], as command output, is connected to the data input of the SPI flash. D[1], as data input, is connected to the data output of the SPI flash. (2) In the Master SPI X2 configuration mode, D[1:0] serves as the data bus. (3) In the Master SPI X4 configuration mode, D[3:0] serves as the data bus. (4) In the Master SPI X8 configuration mode, D[3:0] serves as the data bus for the first SPI FLASH. D[7:4] serves as the data bus for the second SPI FLASH. (5) In the Slave Serial configuration mode, D[1] serves as the data bus. (6) In the Slave SPI configuration mode, D[0] is for the master device output and slave device input. D[1] is for the master device input and slave device output. D[3] is connected to the chip-hold of the SPI flash. (7) In the Master BPI configuration X8 asynchronous mode, D[7:0] serve as an 8-bit data bus. (8) In the Master BPI configuration X16 asynchronous/synchronous mode, D[15:0] serve as

PIN name	PIN type	PIN description
		a 16-bit data bus. (9) In the Slave Parallel X8 configuration mode, D[7:0] are an 8-bit data bus. (10) In the Slave Parallel X16 configuration mode, D[15:0] are a 16-bit data bus. (11) In the Slave Parallel X32 configuration mode, D[31:0] are a 32-bit data bus.
CS_N	input	Multi-function Configuration Pin. for chip-select input. Active low. (1) When it is low, this pin enables the Slave Parallel mode configuration interface. (2) In other configuration modes, this pin is high-Z. (3) To make this pin continue playing its configuration function after configuration is complete, users need to set the configuration register to preserve its configuration function.
RWSEL	input	Multi-function Configuration Pin. For selecting the read/write input in the Slave Parallel configuration mode (High for read and Low for write). (1) When it is High, the Slave Parallel configuration mode reads data from the data bus; (2) When it is Low, the Slave Parallel configuration mode writes data to the data bus; (3) Read and write can be switched only when CS_N is High. (4) To make this pin continue playing its configuration function after configuration is complete, users need to set the configuration register to preserve its configuration function. (5) In other configuration modes, this pin is high-Z.
BUSY	output	Multi-function Configuration Pin. (1) During readback in the Slave Parallel mode, a high output indicates that the data read from the bus is invalid. (2)To make this pin continue playing its configuration function in the user mode, users need to set the configuration register to preserve its configuration function. (3) In other configuration modes, this pin is high-Z
CSO_DOUT	output	Multi-function Configuration Pin. (1) In the Master SPI and X1 modes, this pin serves as cascaded data output; (2) In the Slave Serial configuration mode, this pin serves as cascaded data output; (3) In the Slave Parallel configuration mode, this pin serves as a chip select signal output;
FCS_N	output	Multi-function configuration pin, used for the external Master SPI configuration mode. (1) In the Master SPI mode, this pin outputs a chip-select signal to external flash when the signal is active-low；
VS1, VS0	input	Multi-function configuration pin, used in the Master SPI or internal Master SPI mode. (1) It is used for selecting the bitstream version:

PIN name	PIN type	PIN description
		"00" for the first set of bitstreams, "01" for the second set, "10" for the third set, "11" for the fourth set; (2) It is internal pull-down resistors during configuration.
IO_STATUS_C	input	Multi-function pin, used for inputting signals and controlling the state of all user IOs during the configuration process. (1) "1" keeps all user IOs in a pull-up state during configuration. (2) "0" keeps all user IOs in a tri-state during configuration.
ADR[25:0]	output	Multi-function configuration pin, used for outputting addresses in the BPI configuration mode.
BFOE_N	output	Multi-function configuration pin, used for providing a low-voltage output enable control signal for parallel NOR FLASH in the BPI configuration mode. (1) In the BPI configuration mode, this pin should be connected to the FLASH's output enable input and to VCCIO via a 4.7K resistor.
BADRVO_N	output	Multi-function configuration pin, used for providing a low-level address valid control signal for parallel NOR FLASH in the BPI configuration mode. (1) In the BPI configuration mode, if the external FLASH supports address valid signal input, then this pin should be connected to the FLASH's address valid input pin and to VCCIO via a 4.7K resistor. If the external flash does not support address valid signal input, then there is no need to connect this pin.
BFWE_N	output	Multi-function configuration pin, used for providing a low-voltage write-enable signal for parallel NOR FLASH in the BPI configuration mode. (1) In the BPI configuration mode, this pin should be connected to the flash's write-enable input and to VCCIO via a 4.7K resistor;
BFCE_N	output	Multi-function configuration pin, used for providing a low-voltage chip-select control signal for parallel NOR FLASH in the BPI configuration mode; (1) In the BPI configuration mode, should be connected to the flash's chip-select input and to VCCIO via a 4.7K resistor.
FCS2_N	output	Multi-function configuration pin, used for the external Master SPI X8 configuration mode. (1) In the Master SPI X8 mode, this pin outputs a chip-select signal to the external flash when the signal is active-low and should be connected to VCCIO via an external pull-up resistor not more than 4.7K.
ECCLKIN	input	Multi-function configuration pin, used for inputting signals and serves as clock input for the Master configuration mode.

PIN name	PIN type	PIN description
-- Clock, PLL, Crystal Oscillator Multi-function Pin		
CLK[0,1,2,3]_[L0,L1,L2,R0,R1,R2]	input	Dedicated global clock input pins, 4 pins for each bank
DIFFCLK[0,1]_[L0,L1,L2,R0,R1,R2]_[N,P]	input	Dedicated global differential clock input pins, 2 pairs for each bank
PLL[0,1,2,…10]_CLKOUT_[P,N]	output	Direct selection of PLL[0, 1, …, 19] output to pin is possible
PLL[0,1,2,…10]_CLKIN[0,1,2,3]	input	Optional PLL input, PLL can directly the input clock from these pins.
PLL[0,1,2,…10]_CLKFB_[P,N]	input	Optional PLL feedback clock input, PLL can input external feedback clock from these pins.
XTALA_[L0,L1,L2,R0,R1,R2]	input	Dedicated external crystal input at port A. Input for the on-die inverter, 1 pin for each bank
XTALB_[L0,L1,L2,R0,R1,R2]	output	Dedicated external crystal output at port B. Output for the on-die inverter, 1 pin for each bank
-- External Memory Interface Pin		
DQS[0,1,2][#]_[L0,L1,L2,R0,R1,R2]	Input/Output	Used to connect to the DQS/DQS# signal pins of external memory
DQ[0,1,2]_[L0,L1,L2,R0,R1,R2]	Input/Output	Can connect to the DQ signal pins of external memory
--HMEMC Memory Interface Pin		
[R,L]_A[0,..,15]	output	DDR memory address
[R,L]_CS_N	output	DDR memory chip selection signal, active-low, depends on whether the memory is in use.
[R,L]_RAS_N	output	RAS, active-low
[R,L]_CAS_N	output	CAS, active-low
[R,L]_WE_N	output	Write enable, active-low
[R,L]_BA[0,1,2]	output	ddr BANK address
[R,L]_ODT	output	ODT, on-die terminal
[R,L]_CK	output	P side of DDR memory
[R,L]_CK_N	output	N side of DDR memory
[R,L]_CKE	output	DDR memory clock enable signal, active-high
[R,L]_RESET_N	output	DDR memory reset, active-low
[R,L]_DML	output	Write data mask signal of DQ0-DQ7
[R,L]_DQSL	Input/Output	DQS signals related to DQ0-DQ7
[R,L]_DQSL_N	Input/Output	DQS# signals related to DQ0-DQ7
[R,L]_DQ[0,…,15]	Input/Output	Memory data bus
[R,L]_DMU	output	Write data mask signals of DQ8-DQ15
[R,L]_DQSU	Input/Output	DQS signals related to DQ8-DQ15
[R,L]_DQSU_N	Input/Output	DQS# signals related to DQ8-DQ15
[R,L]_DQSL_GATE_IN	input	DQS gate window signal feedback (lower bits) after compensating for read command path delay
[R,L]_DQSL_GATE_OUT	output	DQS gate window signal output (lower bits) after compensating for read command path delay

PIN name	PIN type	PIN description
[R,L]_DQSU_GATE_IN	input	DQS gate window signal feedback (higher bits) after compensating for read command path delay
[R,L]_DQSU_GATE_OUT	output	DQS gate window signal output (higher bits) after compensating for read command path delay
--Reference Pin		
RRP_[L0,L1,L2,R0,R1,R2]	input	External reference resistor pin, one for each bank. Provides a reference resistor to the power supply for on-die terminal resistor adjustment.
RRN_[L0,L1,L2,R0,R1,R2]	input	External reference resistor pin, one for each bank. Provides a reference resistor to the ground for on-die terminal resistor adjustment.
VREF_[L0,L1,L2,R0,R1,R2]	input	External reference power pin, one for each bank. Provides reference voltage input for each BANK
--ADC Pin		
VAUX[9,8,7,..0]	input	Analog input signals
Dedicated Pin		
--Configuration Pin, JTAG Pin		
CFG_DONE	Bidirectional (open-drain)	Dedicated pin for configuration state. Serves as a status output, driven low before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released.
RST_N	input	Dedicated configuration input pin, internally weak pull-up, for restarting the configuration process, active-low. It is recommended that users externally pull up the RST_N with a resistor when using this pin. When this pin is low, the FPGA enters a reset state, and all IOs are in the high-Z state.
TCK	input	Dedicated JTAG test clock input pin
TMS	input	Dedicated JTAG test mode selection input pin
TDI	input	Dedicated JTAG test data input pin.
TDO	output	Dedicated JTAG test data output pin.
--Reference Pin		
REXT	input	Dedicated external high-precision resistor pin, with a resistance of 10k and an accuracy of 1%. Provides resistance for the bandgap.
--ADC Pin		
VA[1,0]	input	Dedicated analog input signal
VREF_EXT	input	Dedicated external reference 2.5V voltage.
Power Pin, Ground Pin		
VCC	POWER	Core power, 1.1V. Power supply for core logic
VCCAUX	POWER	3.3V auxiliary power supply for IOB, LDO, and other modules
VDDIO[L0,L1,L2,R0,R1,R2]	POWER	IO BANK power, the banks on the left are BANKL0, BANKL1, and BANKL2; the banks on the right side are BANKR0, BANKR1, and BANKR2
VCCAUX_A	POWER	Power supply for ADC, BANDGAP, and POR
VSS	GROUND	GND relative to VCC&VCCAUX

PIN name	PIN type	PIN description
VSSA	GROUND	GND relative to VCCAUX_A
VDDEFUSE	POWER	Efuse Programming Voltage
VDDIOCFG	POWER	BANKCFG power supply

Note: PGL12G_LPG144 has 103 user IOs.

2.2.1 Pin Name list

Table 2-2 Pin Name List

Pin Number	Pin Name
1	DIFFIO_R0_7_N/VS0
2	DIFFIO_R0_7_P/VS1
3	DIFFIO_R0_4_P/FCS2_N
4	DIFFIO_R0_3_N/ECCLKIN
5	DIFFIO_R0_2_P/VAUX1
6	VCCAUX
7	DIFFIO_R0_1_N/VAUX2
8	DIFFIO_R0_1_P/VAUX3
9	VDDIOR0
10	DIFFIO_R0_0_P/VAUX5
11	DIFFIO_R0_0_N/VAUX4
12	VSS
13	VCC
14	VCCAUX_A
15	VDDEFUSE
16	TCK
17	TDO
18	TMS
19	TDI
20	VDDIOCFG
21	RST_N
22	CFG_DONE
23	REXT
24	VCCAUX_A
25	VSS
26	VCC
27	VSS
28	DIFFIO_L0_0_P/BUSY
29	VDDIOL0
30	DIFFIO_L0_3_P/IO_STATUS_C

Pin Number	Pin Name
31	DIFFIO_L0_3_N/CFG_CLK
32	DIFFIO_L0_5_P/MODE_0
33	DIFFIO_L0_5_N/MODE_1
34	DIFFIO_L0_4_P/FCS_N
35	DIFFIO_L0_4_N/CS_N
36	DIFFIO_L0_7_P/RWSEL
37	DIFFIO_L0_6_P/MODE_2
38	DIFFIO_L0_7_N/INIT_FLAG_N
39	DIFFIO_L0_6_N/VREF_L0/CSO_DOUT
40	DIFFIO_L0_8_P/PLL0_CLKOUT_P
41	DIFFIO_L0_8_N/PLL0_CLKOUT_N
42	DIFFIO_L0_9_P/CLK0_L0/DIFFCLK0_L0_P/PLL0_CLKFB_P/XTALA_L0
43	DIFFIO_L0_9_N/CLK1_L0/DIFFCLK0_L0_N/PLL0_CLKFB_N/XTALB_L0
44	DIFFIO_L0_10_P/CLK2_L0/DIFFCLK1_L0_P/PLL1_CLKIN0
45	DIFFIO_L0_10_N/CLK3_L0/DIFFCLK1_L0_N/PLL1_CLKIN1
46	DIFFIO_L0_11_P/PLL1_CLKIN2
47	DIFFIO_L0_11_N/PLL1_CLKIN3
48	DIFFIO_L0_12_P/D0
49	DIFFIO_L0_12_N/RRN_L0/D1
50	DIFFIO_L0_13_P/RRP_L0/D2
51	DIFFIO_L0_13_N/D3
52	DIFFIO_L0_14_P/D4
53	DIFFIO_L0_14_N/D5
54	DIFFIO_L0_15_P/D6
55	DIFFIO_L0_15_N/D7
56	VDDIOL0
57	VSS
58	DIFFIO_L1_2_P
59	DIFFIO_L1_2_N
60	DIFFIO_L1_4_P
61	DIFFIO_L1_4_N
62	VDDIOL1
63	VCCAUX
64	DIFFIO_L1_6_N/VREF_L1
65	DIFFIO_L1_8_P/PLL2_CLKOUT_P
66	DIFFIO_L1_8_N/PLL2_CLKOUT_N
67	VCC
68	VSS
69	DIFFIO_L1_11_P/PLL3_CLKIN2

Pin Number	Pin Name
70	DIFFIO_L1_10_N/CLK3_L1/DIFFCLK1_L1_N/PLL3_CLKIN1
71	DIFFIO_L1_11_N/PLL3_CLKIN3
72	DIFFIO_L1_13_P/RRP_L1
73	DIFFIO_L1_12_N/RRN_L1
74	DIFFIO_L1_15_P
75	DIFFIO_L1_15_N
76	DIFFIO_L1_17_P
77	DIFFIO_L1_17_N
78	VSS
79	DIFFIO_L1_16_N
80	DIFFIO_L1_18_P
81	DIFFIO_L1_18_N
82	VSS
83	VDDIOL1
84	DIFFIO_L1_19_N
85	DIFFIO_L1_19_P
86	DIFFIO_L1_10_P/CLK2_L1/DIFFCLK1_L1_P/PLL3_CLKIN0
87	DIFFIO_L1_9_N/CLK1_L1/DIFFCLK0_L1_N/PLL2_CLKFB_N/XTALB_L1
88	DIFFIO_L1_9_P/CLK0_L1/DIFFCLK0_L1_P/PLL2_CLKFB_P/XTALA_L1
89	VCC
90	VSS
91	VCCAUX
92	DIFFIO_R1_9_P/CLK0_R1/DIFFCLK0_R1_P/PLL2_CLKIN2/XTALA_R1
93	DIFFIO_R1_9_N/CLK1_R1/DIFFCLK0_R1_N/PLL2_CLKIN3/XTALB_R1
94	DIFFIO_R1_10_P/CLK2_R1/DIFFCLK1_R1_P/PLL3_CLKFB_P
95	DIFFIO_R1_19_P
96	DIFFIO_R1_19_N
97	DIFFIO_R1_10_N/CLK3_R1/DIFFCLK1_R1_N/PLL3_CLKFB_N
98	VDDIOR1
99	DIFFIO_R1_18_N
100	DIFFIO_R1_18_P
101	DIFFIO_R1_16_N
102	DIFFIO_R1_16_P
103	DIFFIO_R1_14_N
104	VSS
105	DIFFIO_R1_17_N
106	DIFFIO_R1_17_P
107	DIFFIO_R1_15_N
108	DIFFIO_R1_15_P

Pin Number	Pin Name
109	DIFFIO_R1_12_N/RRN_R1
110	DIFFIO_R1_13_P/RRP_R1
111	DIFFIO_R1_11_N/PLL3_CLKOUT_N
112	DIFFIO_R1_11_P/PLL3_CLKOUT_P
113	VDDIOR1
114	VSS
115	VCC
116	DIFFIO_R1_8_N/PLL2_CLKIN1
117	DIFFIO_R1_8_P/PLL2_CLKIN0
118	DIFFIO_R1_6_N/VREF_R1
119	VDDIOR1
120	DIFFIO_R1_4_N/ADR24
121	DIFFIO_R1_4_P/ADR23
122	DIFFIO_R1_2_N/ADR20
123	DIFFIO_R1_2_P/ADR19
124	VCCAUX
125	VSS
126	VDDIOR0
127	DIFFIO_R0_15_N/D23/ADR7
128	DIFFIO_R0_15_P/D22/ADR6
129	DIFFIO_R0_14_N/D21/ADR5
130	DIFFIO_R0_14_P/D20/ADR4
131	DIFFIO_R0_13_N/D19/ADR3
132	DIFFIO_R0_13_P/RRP_R0/D18/ADR2
133	DIFFIO_R0_12_N/RRN_R0/D17/ADR1
134	DIFFIO_R0_11_N/PLL1_CLKOUT_N
135	DIFFIO_R0_12_P/D16/ADR0
136	DIFFIO_R0_11_P/PLL1_CLKOUT_P
137	DIFFIO_R0_10_N/CLK3_R0/DIFFCLK1_R0_N/PLL1_CLKFB_N
138	DIFFIO_R0_10_P/CLK2_R0/DIFFCLK1_R0_P/PLL1_CLKFB_P
139	DIFFIO_R0_9_N/CLK1_R0/DIFFCLK0_R0_N/PLL0_CLKIN3/XTALB_R0
140	VDDIOR0
141	DIFFIO_R0_9_P/CLK0_R0/DIFFCLK0_R0_P/PLL0_CLKIN2/XTALA_R0
142	DIFFIO_R0_8_N/PLL0_CLKIN1
143	DIFFIO_R0_8_P/PLL0_CLKIN0
144	DIFFIO_R0_6_N/VREF_R0

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