Compa Family GTP User Guide

(UG030008, V1.2)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.2	16.08.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
GTP	Generic Technology Primitive

Related Documentation

The following documentation is related to this manual:

1. ***UG030001_Compa Family CPLDs Configurable Logic Module (CLM) User Guide***
2. ***UG030002_Compa Family CPLDs Dedicated RAM Module (DRM) User Guide***
3. ***UG030003_Compa Family CPLDs Clock Resources (Clock&PLL) User Guide***
4. ***UG030005_Compa Family CPLDs Input/Output Interface (IO) User Guide***
5. ***UG030007_Compa Family CPLDs Embedded Hard Core User Guide***

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Chapter 1 Trigger GTPs

Trigger GTP has 2 parameters: GRS_EN and INIT. The initial values of different types of triggers are determined by the default value of the INIT parameter, and changes to the INIT parameter do not affect the initial values of the triggers.

1.1 GTP_DFF

1.1.1 Description of Functionality

GTP_DFF is a D flip-flop with a data input D and a data output Q. It triggers and transfers the input signal to the output on the rising edge of the clock. The structure block diagram is shown below.

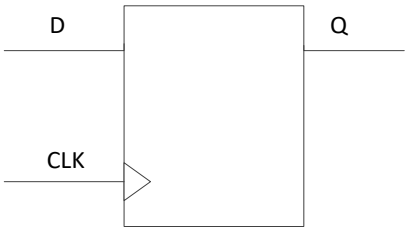

Figure 1-1 GTP_DFF Structure Block Diagram

1.1.2 Port Description

Table 1-1 GTP_DFF Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger

1.1.3 Paramater Description

Table 1-2 GTP_DFF Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
GRS_EN	"TRUE","FALSE"	"TRUE"	Global reset signal enable; "TRUE" indicates that the global reset signal is valid
INIT	1'b0	1'b0	The initial value is 0 when entering user mode

1.1.4 Instantiation template

```
GTP_DFF GTP_DFF_inst (
.CLK (CLK),
.D (D),
.Q (Q));
```

1.2 GTP_DFF_C

1.2.1 Description of Functionality

GTP_DFF_C is a D flip-flop with a asynchronous clear signal C. It is triggered on the rising edge of the clock, transferring the input signal to the output signal. The structure block diagram is shown below.

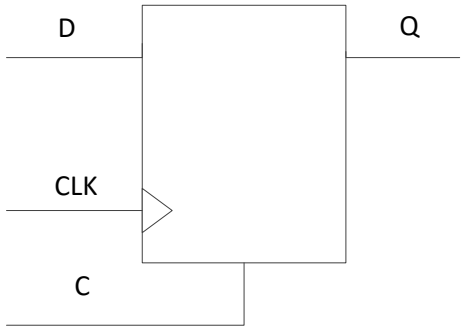

Figure 1-2 GTP_DFF_C Structure Block Diagram

1.2.2 Port Description

Table 1-3 GTP_DFF_C Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger
C	Input	Asynchronous clear signal, active high

1.2.3 Paramater Description

Table 1-4 GTP_DFF_C Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
GRS_EN	"TRUE","FALSE"	"TRUE"	Global reset signal enable; "TRUE" indicates that the global reset signal is valid

Parameter Name	Valid Values	Defaults	Function Description
INIT	1'b0	1'b0	The initial value is 0 when entering user mode

1.2.4 Instantiation template

```
GTP_DFF_C GTP_DFF_C_int (
.CLK (CLK),
.D (D),
.C (C),
.Q (Q));
```

1.3 GTP_DFF_E

1.3.1 Description of Functionality

GTP_DFF_E is a D flip-flop with an enable signal CE. It is triggered on the rising edge of the clock, transferring the input signal to the output signal when CE is high. The structure block diagram is shown below.

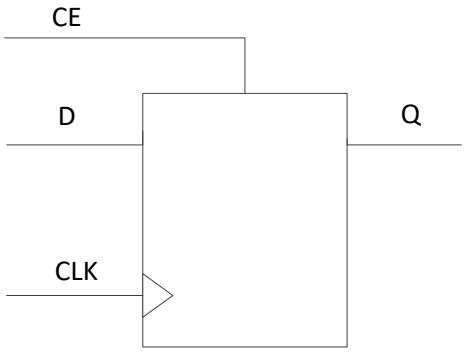

Figure 1-3 GTP_DFF_E Structure Block Diagram

1.3.2 Port Description

Table 1-5 GTP_DFF_E Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger
CE	Input	Active-high enable signal

1.3.3 Paramater Description

Table 1-6 GTP_DFF_E Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
GRS_EN	"TRUE","FALSE"	"TRUE"	Global reset signal enable; "TRUE" indicates that the global reset signal is valid
INIT	1'b0	1'b0	The initial value is 0 when entering user mode

1.3.4 Instantiation template

```
GTP_DFF_E GTP_DFF_E_inst (
.CLK (CLK),
.CE (CE),
.D (D),
.Q (Q));
```

1.4 GTP_DFF_CE

1.4.1 Description of Functionality

GTP_DFF_CE is a D flip-flop with an enable signal CE and asynchronous clear signal C, triggered on the rising edge of the clock, transferring the input signal to the output signal when CE is high. The structure block diagram is shown below.

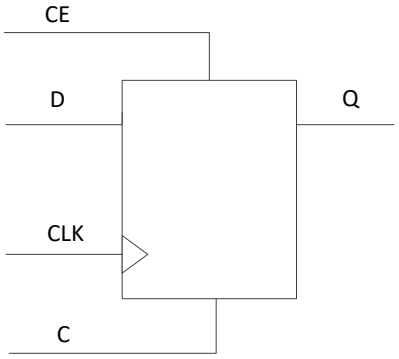

Figure 1-4 GTP_DFF_CE Structure Block Diagram

1.4.2 Port Description

Table 1-7 GTP_DFF_CE Port Description

Port	Direction	Function Description
CLK	Input	Input Clock

D	Input	Input signal of trigger
Q	Output	Output signal of trigger
C	Input	Asynchronous clear signal, active high
CE	Input	Active-high enable signal

1.4.3 Paramater Description

Table 1-8 GTP_DFF_CE Parameter Description

Parameter Name	**Valid Values**	**Defaults**	**Function Description**
GRS_EN	"TRUE","FALSE"	"TRUE"	Global reset signal enable; "TRUE" indicates that the global reset signal is valid
INIT	1'b0	1'b0	The initial value is 0 when entering user mode

1.4.4 Instantiation template

```
GTP_DFF_CE GTP_DFF_CE_inst(
.CLK (CLK),
.C (C),
.CE (CE),
.D (D),
.Q (Q));
```

1.5 GTP_DFF_P

1.5.1 Description of Functionality

GTP_DFF_P is a D flip-flop with a asynchronous set signal P. It is triggered on the rising edge of the clock, transferring the input signal to the output signal. The structure block diagram is shown below.

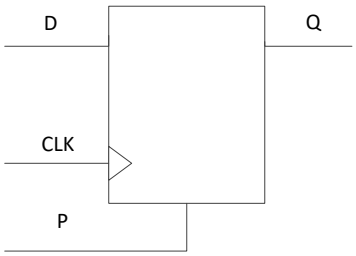

Figure 1-5 GTP_DFF_P Structure Block Diagram

1.5.2 Port Description

Table 1-9 GTP_DFF_P Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger
P	Input	Asynchronous set signal, active high

1.5.3 Paramater Description

Table 1-10 GTP_DFF_P Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
GRS_EN	"TRUE","FALSE"	"TRUE"	Global reset signal enable; "TRUE" indicates that the global reset signal is valid
INIT	1'b1	1'b1	The initial value is 1 when entering user mode

1.5.4 Instantiation template

```
GTP_DFF_P GTP_DFF_P_inst(
.CLK (CLK),
.P (P),
.D (D),
.Q (Q));
```

1.6 GTP_DFF_PE

1.6.1 Description of Functionality

GTP_DFF_PE is a D flip-flop with an asynchronous set signal P and an enable signal CE. It is triggered on the rising edge of the clock, transferring the input signal to the output signal when CE is high. The structure block diagram is shown below.

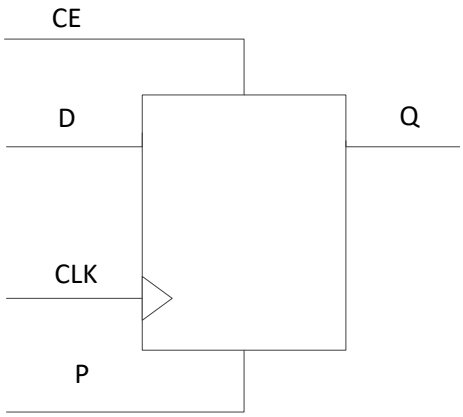

Figure 1-6 GTP_DFF_PE Structure Block Diagram

1.6.2 Port Description

Table 1-11 GTP_DFF_PE Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger
P	Input	Asynchronous set signal, active high
CE	Input	Active-high enable signal

1.6.3 Paramater Description

Table 1-12 GTP_DFF_PE Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
GRS_EN	"TRUE","FALSE"	"TRUE"	Global reset signal enable; "TRUE" indicates that the global reset signal is valid
INIT	1'b1	1'b1	The initial value is 1 when entering user mode

1.6.4 Instantiation template

```
GTP_DFF_PE GTP_DFF_PE_inst(
.CLK (CLK),
.P (P),
.CE (CE),
.D (D),
.Q (Q));
```

1.7 GTP_DFF_R

1.7.1 Description of Functionality

GTP_DFF_R is a D flip-flop with a synchronous clear signal R. It is triggered on the rising edge of the clock, transferring the input signal to the output signal. The structure block diagram is shown below.

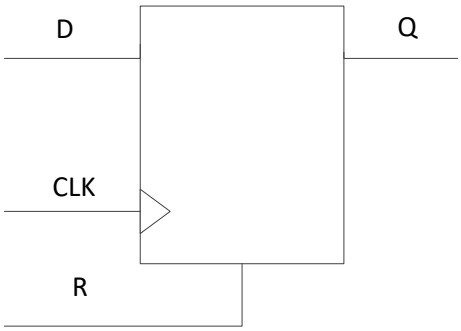

Figure 1-7 GTP_DFF_R Structure Block Diagram

1.7.2 Port Description

Table 1-13 GTP_DFF_R Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger
R	Input	Synchronous clear signal, active high

1.7.3 Paramater Description

Table 1-14 GTP_DFF_R Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
GRS_EN	"TRUE","FALSE"	"TRUE"	Global reset signal enable; "TRUE" indicates that the global reset signal is valid
INIT	1'b0	1'b0	The initial value is 0 when entering user mode

1.7.4 Instantiation template

```
GTP_DFF_R GTP_DFF_R_inst(
.CLK (CLK),
.R (R),
```

```
.D (D),
.Q (Q)
);
```

1.8 GTP_DFF_RE

1.8.1 Description of Functionality

GTP_DFF_RE is a D flip-flop with a synchronous clear signal R and an enable signal CE. It is triggered on the rising edge of the clock, transferring the input signal to the output signal when CE is high. The structure block diagram is shown below.

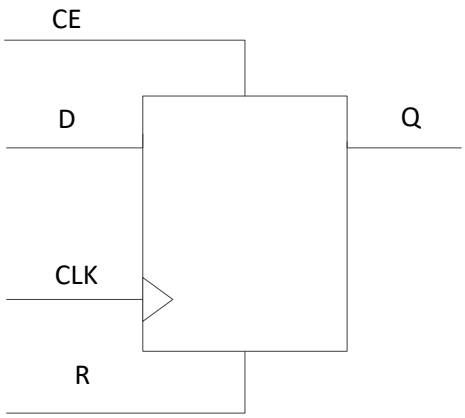

Figure 1-8 GTP_DFF_RE Structure Block Diagram

1.8.2 Port Description

Table 1-15 GTP_DFF_RE Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger
R	Input	Synchronous clear signal, active high
CE	Input	Active-high enable signal

1.8.3 Paramater Description

Table 1-16 GTP_DFF_RE Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
GRS_EN	"TRUE","FALSE"	"TRUE"	Global reset signal enable; "TRUE" indicates that the global reset signal is valid
INIT	1'b0	1'b0	The initial value is 0 when entering user mode

1.8.4 Instantiation template

```
GTP_DFF_RE GTP_DFF_RE_inst(
.CLK (CLK),
.R (R),
.CE (CE),
.D (D),
.Q (Q)
);
```

1.9 GTP_DFF_S

1.9.1 Description of Functionality

GTP_DFF_S is a D flip-flop with a synchronous set signal S. It is triggered on the rising edge of the clock, transferring the input signal to the output signal. The structure block diagram is shown below.

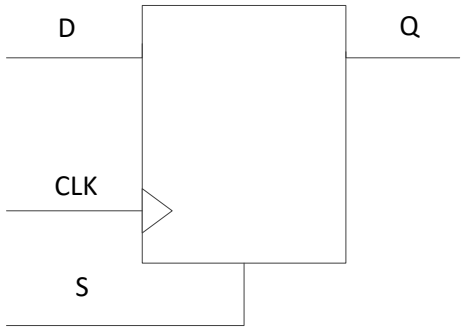

Figure 1-9 GTP_DFF_S Structure Block Diagram

1.9.2 Port Description

Table 1-17 GTP_DFF_S Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger

Q	Output	Output signal of trigger
S	Input	Synchronous set signal, active high

1.9.3 Paramater Description

Table 1-18 GTP_DFF_S Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
GRS_EN	"TRUE","FALSE"	"TRUE"	Global reset signal enable; "TRUE" indicates that the global reset signal is valid
INIT	1'b1	1'b1	The initial value is 1 when entering user mode

1.9.4 Instantiation template

```
GTP_DFF_S GTP_DFF_S_inst(
.CLK (CLK),
.S (S),
.D (D),
.Q (Q));
```

1.10 GTP_DFF_SE

1.10.1 Description of Functionality

GTP_DFF_SE is a D flip-flop with a synchronous set signal S and an enable signal CE. It is triggered on the rising edge of the clock, transferring the input signal to the output signal when CE is high. The structure block diagram is shown below.

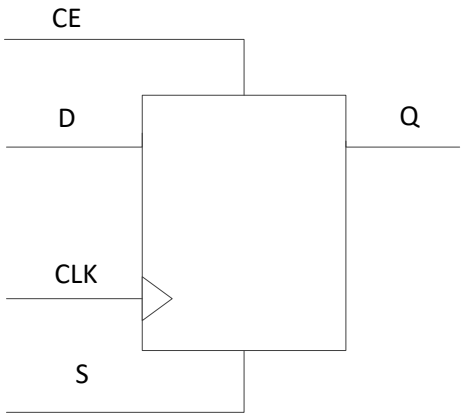

Figure 1-10 GTP_DFF_SE Structure Block Diagram

1.10.2 Port Description

Table 1-19 GTP_DFF_SE Port Description

Port	Direction	Function Description
CLK	Input	Input Clock
D	Input	Input signal of trigger
Q	Output	Output signal of trigger
S	Input	Synchronous set signal, active high
CE	Input	Active-high enable signal

1.10.3 Paramater Description

Table 1-20 GTP_DFF_SE Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
GRS_EN	"TRUE","FALSE"	"TRUE"	Global reset signal enable; "TRUE" indicates that the global reset signal is valid
INIT	1'b1	1'b1	The initial value is 1 when entering user mode

1.10.4 Instantiation template

```
GTP_DFF_SE GTP_DFF_SE_inst(
.CLK (CLK),
.S (S),
.CE (CE),
.D (D),
.Q (Q) );
```

Chapter 2 Latch GTPs

Table 2-1 Latch GTP Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
GRS_EN	"TRUE","FALSE"	"TRUE"	Global reset signal enable

INIT parameter does not affect the output of the latch.

2.1 GTP_DLATCH

2.1.1 Description of Functionality

GTP_DLATCH is a latch with D as data input and Q as data output. It can send the input signal to the output when G is high. The structure block diagram is shown below.

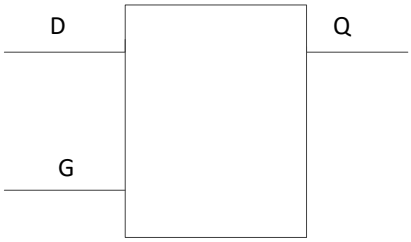

Figure 2-1 GTP_DLATCH Structure Block Diagram

2.1.2 Port Description

Table 2-2 GTP_DLATCH Port Description

Port	Direction	Function Description
G	Input	Level-triggered signal, active high
D	Input	Latch input signal
Q	Output	Latch output signal

2.1.3 Instantiation template

```
GTP_DLATCH#(
.GRS_EN("TURE"),//"TURE"; "FALSE"
.INIT(1'b0)
)
```

```
GTP_DLATCH_inst (
.Q (q),
.D (d),
.G (g));
```

2.2 GTP_DLATCH_E

2.2.1 Description of Functionality

GTP_DLATCH_E is a latch with an enable signal GE, transmitting the input signal to the output signal when G and GE are both high. The structure block diagram is shown below.

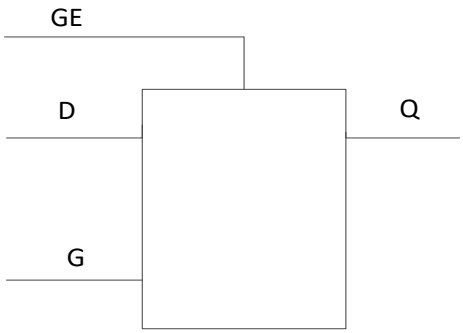

Figure 2-2 GTP_DLATCH_E Structure Block Diagram

2.2.2 Port Description

Table 2-3 GTP_DLATCH_E Port Description

Port	Direction	Function Description
G	Input	Level-triggered signal, active high
D	Input	Latch input signal
Q	Output	Latch output signal
GE	Input	Active-high enable signal

2.2.3 Instantiation template

```
GTP_DLATCH_E#(
.GRS_EN("TURE"),//"TURE"; "FALSE"
.INIT(1'b0)
)
GTP_DLATCH_E_inst (
.Q (q),
```

```
.D (d),
.G (g),
.GE (en)
);
```

2.3 GTP_DLATCH_C

2.3.1 Description of Functionality

GTP_DLATCH_C is a latch with an asynchronous clear signal C, transmitting the input signal to the output signal when G is high. The structure block diagram is shown below.

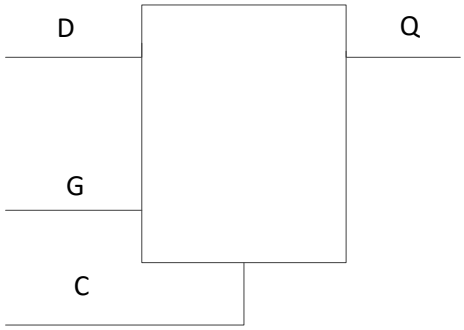

Figure 2-3 GTP_DLATCH_C Structure Block Diagram

2.3.2 Port Description

Table 2-4 GTP_DLATCH_C Port Description

Port	Direction	Function Description
G	Input	Level-triggered signal, active high
D	Input	Latch input signal
Q	Output	Latch output signal
C	Input	Asynchronous clear signal, active high

2.3.3 Instantiation template

```
GTP_DLATCH_C#(
.GRS_EN("TURE"),//"TURE"; "FALSE"
.INIT(1'b0)
)
GTP_DLATCH_C_inst (
.Q (q),
```

.D (d),

.G (g),

.C (c)

);

2.4 GTP_DLATCH_CE

2.4.1 Description of Functionality

GTP_DLATCH_CE is a latch with an asynchronous clear signal C and an enable signal GE, transmitting the input signal to the output when G and GE are both high. The structure block diagram is shown below.

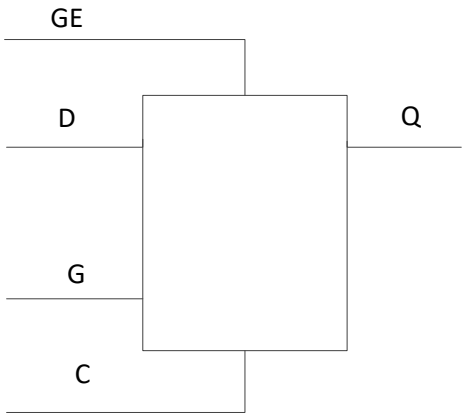

Figure 2-4 GTP_DLATCH_CE Structure Block Diagram

2.4.2 Port Description

Table 2-5 GTP_DLATCH_CE Port Description

Port	Direction	Function Description
G	Input	Level-triggered signal, active high
D	Input	Latch input signal
Q	Output	Latch output signal
C	Input	Asynchronous clear signal, active high
GE	Input	Active-high enable signal

2.4.3 Instantiation template

GTP_DLATCH_CE#(

.GRS_EN("TURE"),//"TURE"; "FALSE"

```
.INIT(1'b0)
)
GTP_DLATCH_CE_inst (
.Q (q),
.D (d),
.G (g),
.C (c),
.GE (ge));
```

2.5 GTP_DLATCH_P

2.5.1 Description of Functionality

GTP_DLATCH_P is a latch with an asynchronous set signal P, transmitting the input signal to the output when G is high. The structure block diagram is shown below.

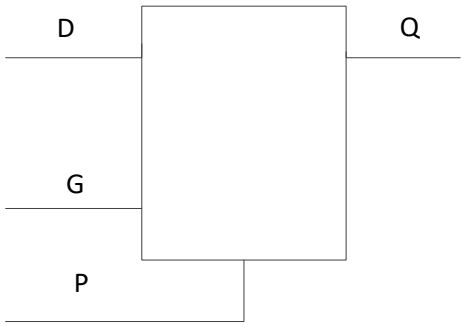

Figure 2-5 GTP_DLATCH_P Structure Block Diagram

2.5.2 Port Description

Table 2-6 GTP_DLATCH_P Port Description

Port	Direction	Function Description
G	Input	Level-triggered signal, active high
D	Input	Latch input signal
Q	Output	Latch output signal
P	Input	Asynchronous set signal; when it is 1'b1, Q=1; when it is 1b0, Q=D

2.5.3 Instantiation template

```
GTP_DLATCH_P#(
.GRS_EN("TURE"),//"TURE"; "FALSE"
```

```
.INIT(1'b1)
)
GTP_DLATCH_P_inst (
.Q (q),
.D (d),
.G (g),
.P (p));
```

2.6 GTP_DLATCH_PE

2.6.1 Description of Functionality

GTP_DLATCH_PE is a latch with an asynchronous set signal P and an enable signal GE, transmitting the input signal to the output when G and GE are both high. The structure block diagram is shown below.

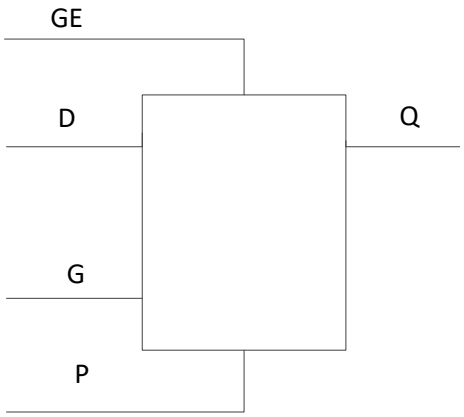

Figure 2-6 GTP_DLATCH_PE Structure Block Diagram

2.6.2 Port Description

Table 2-7 GTP_DLATCH_PE Port Description

Port	Direction	Function Description
G	Input	Level-triggered signal, active high
D	Input	Latch input signal
Q	Output	Latch output signal
P	Input	Asynchronous set signal; when it is 1'b1, Q=1; when it is 1b0, Q=D
GE	Input	Active-high enable signal

2.6.3 Instantiation template

```
GTP_DLATCH_PE#(
.GRS_EN("TURE"),//"TURE"; "FALSE"
.INIT(1'b1)
)
GTP_DLATCH_PE_inst (
.Q (q),
.D (d),
.G (g),
.P (p),
.GE (en));
```

Chapter 3 LUT-related GTP

3.1 GTP_ONE

3.1.1 Description of Functionality

GTP_ONE outputs a high level signal. The structure block diagram is shown below.

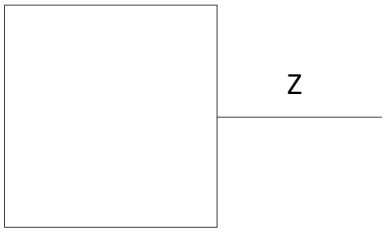

Figure 3-1 GTP_ONE Structure Block Diagram

3.1.2 Port Description

Table 3-1 GTP_ONE Port Description

Port	Direction	Function Description
Z	Output	High-level output

3.1.3 Instantiation template

```
GTP_ONE GTP_ONE_inst (
.Z    (Z)
);
```

3.2 GTP_ZERO

3.2.1 Description of Functionality

GTP_ZERO outputs a low level signal. The structure block diagram is shown below.

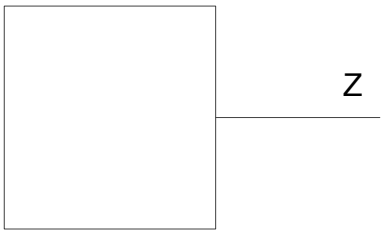

Figure 3-2 GTP_ZERO Structure Block Diagram

3.2.2 Port Description

Table 3-2 GTP_ZERO Port Description

Port	Direction	Function Description
Z	Output	Low-level output

3.2.3 Instantiation template

```
GTP_ZERO GTP_ZERO_inst (
.Z    (z)
);
```

3.3 GTP_BUF

3.3.1 Description of Functionality

GTP_BUF is a general 1-bit buffer, with the structure block diagram shown below.

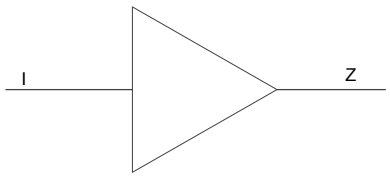

Figure 3-3 GTP_BUF Structure Block Diagram

3.3.2 Port Description

Table 3-3 GTP_BUF Port Description

Port	Direction	Function Description
Z	Output	Output signal
I	Input	Input Signal

3.3.3 Functional Description

GTP_BUF is not a mandatory GTP, which will be optimized away by the software after MAP flow.

3.3.4 Instantiation template

```
GTP_BUF GTP_BUF_inst (
.I     (I),
```

.Z (Z)

);

3.4 GTP_INV

3.4.1 Description of Functionality

GTP_INV is an inverter. The structure block diagram is shown below.

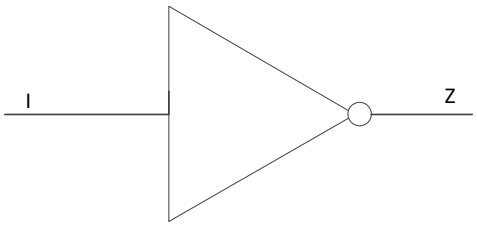

Figure 3-4 GTP_INV Structure Block Diagram

3.4.2 Port Description

Table 3-4 GTP_INV Port Description

Port	Direction	Function Description
Z	Output	Output signal
I	Input	Input Signal

3.4.3 Instantiation template

GTP_INV GTP_INV_inst (

.I (i),

.Z (z)

);

3.5 GTP_LUT1

3.5.1 Description of Functionality

GTP_LUT1 is a Look Up Table with 1-bit input and 1-bit output. The structure block diagram is shown below.

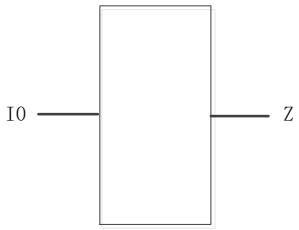

Figure 3-5 GTP_LUT1 Structure Block Diagram

3.5.2 Port Description

Table 3-5 GTP_LUT1 Port Description

Port	Direction	Function Description
Z	Output	Output signal
I0	Input	Input Signal

Truth Table:

Table 3-6 GTP_LUT1 Truth Table

Input	Output
I0	Z
0	INIT[0]
1	INIT[1]

3.5.3 Paramater Description

Table 3-7 GTP_LUT1 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
INIT	0~3	2'h0	Output Configuration Parameter

3.5.4 Instantiation template

```
GTP_LUT1
#(
.INIT     (2'h0)
)GTP_LUT1_inst (
.Z        (z),
.I0       (i0)
);
```

3.6 GTP_LUT2

3.6.1 Description of Functionality

GTP_LUT2 is a dual-input Look Up Table, with different INIT parameter values corresponding to different functions of LUT2; the corresponding INIT parameter must be specified when used. The structure block diagram is shown below.

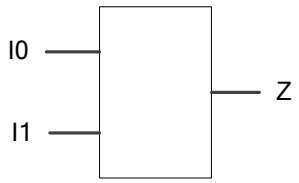

Figure 3-6 GTP_LUT2 Structure Block Diagram

3.6.2 Port Description

Table 3-8 GTP_LUT2 Port Description

Port	Direction	Function Description
Z	Output	Output signal
I0	Input	Input Signal
I1	Input	Input Signal

Truth Table:

Table 3-9 GTP_LUT2 Truth Table

Input		Output
I1	I0	Z
0	0	INIT[0]
0	1	INIT[1]
1	0	INIT[2]
1	1	INIT[3]

3.6.3 Paramater Description

Table 3-10 GTP_LUT2 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
INIT	0~15	4'h0	Output Configuration Parameter

3.6.4 Instantiation template

```
GTP_LUT2
#(
.INIT     (4'h0)
)GTP_LUT2_inst (
.Z        (z),
.I0       (i0),
.I1       (i1)
);
```

3.7 GTP_LUT3

3.7.1 Description of Functionality

GTP_LUT3 is a triple-input Look Up Table, with different INIT parameter values corresponding to different functions of LUT3; the corresponding INIT parameter must be specified when used. The structure block diagram is shown below.

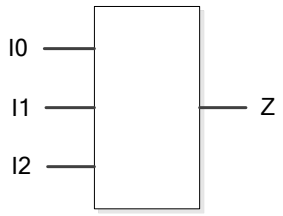

Figure 3-7 GTP_LUT3 Structure Block Diagram

3.7.2 Port Description

Table 3-11 GTP_LUT3 Port Description

Port	**Direction**	**Function Description**
Z	Output	Output signal
I0	Input	Input Signal
I1	Input	Input Signal
I2	Input	Input Signal

Truth Table:

Table 3-12 GTP_LUT3 Truth Table

Input			**Output**
I2	I1	I0	Z
0	0	0	INIT[0]
0	0	1	INIT[1]
0	1	0	INIT[2]
0	1	1	INIT[3]
1	0	0	INIT[4]
1	0	1	INIT[5]
1	1	0	INIT[6]
1	1	1	INIT[7]

3.7.3 Paramater Description

Table 3-13 GTP_LUT3 Parameter Description

Parameter Name	**Valid Values**	**Defaults**	**Function Description**
INIT	0~255	8'h00	Output Configuration Parameter

3.7.4 Instantiation template

```
GTP_LUT3
#(
.INIT        (8'h00)
)GTP_LUT3_inst (
.Z           (z),
.I0          (i0),
.I1          (i1),
.I2          (i2)
);
```

3.8 GTP_LUT4

3.8.1 Description of Functionality

GTP_LUT4 is a 4-input Look Up Table, with different INIT parameter values corresponding to different functions of LUT4; the corresponding INIT parameter must be specified when used. The structure block diagram is shown below.

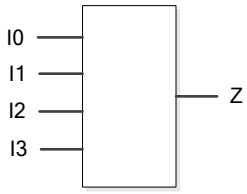

Figure 3-8 GTP_LUT4 Structure Block Diagram

3.8.2 Port Description

Table 3-14 GTP_LUT4 Port Description

Port	**Direction**	**Function Description**
Z	Output	Output signal
I0	Input	Input Signal
I1	Input	Input Signal
I2	Input	Input Signal
I3	Input	Input Signal

Truth Table:

Table 3-15 GTP_LUT4 Truth Table

Input				**Output**
I3	I2	I1	I0	Z
0	0	0	0	INIT[0]
0	0	0	1	INIT[1]
0	0	1	0	INIT[2]
0	0	1	1	INIT[3]
0	1	0	0	INIT[4]
0	1	0	1	INIT[5]
0	1	1	0	INIT[6]
0	1	1	1	INIT[7]
1	0	0	0	INIT[8]
1	0	0	1	INIT[9]
1	0	1	0	INIT[10]
1	0	1	1	INIT[11]
1	1	0	0	INIT[12]
1	1	0	1	INIT[13]
1	1	1	0	INIT[14]
1	1	1	1	INIT[15]

3.8.3 Paramater Description

Table 3-16 GTP_LUT4 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
INIT	0~2^16-1	16'h0000	Output Configuration Parameter

3.8.4 Instantiation template

```
GTP_LUT4
#(
.INIT     (16'h0000)
)GTP_LUT4_inst (
.Z        (z),
.I0       (i0),
.I1       (i1),
.I2       (i2),
.I3       (i3)
);
```

3.9 GTP_LUT5

3.9.1 Description of Functionality

GTP_LUT5 is a 5-input Look Up Table, with different INIT parameter values corresponding to different functions of LUT5; the corresponding INIT parameter must be specified when used. The structure block diagram is shown below.

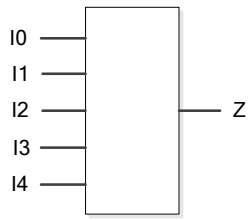

Figure 3-9 GTP_LUT5 Structure Block Diagram

3.9.2 Port Description

Table 3-17 GTP_LUT5 Port Description

Port	Direction	Function Description
Z	Output	Output signal
I0	Input	Input Signal
I1	Input	Input Signal
I2	Input	Input Signal
I3	Input	Input Signal
I4	Input	Input Signal

Truth Table:

Table 3-18 GTP_LUT5 Truth Table

Input					Output
I4	I3	I2	I1	I0	Z
0	0	0	0	0	INIT[0]
0	0	0	0	1	INIT[1]
0	0	0	1	0	INIT[2]
0	0	0	1	1	INIT[3]
0	0	1	0	0	INIT[4]
0	0	1	0	1	INIT[5]
0	0	1	1	0	INIT[6]
0	0	1	1	1	INIT[7]
0	1	0	0	0	INIT[8]
0	1	0	0	1	INIT[9]
0	1	0	1	0	INIT[10]
0	1	0	1	1	INIT[11]
0	1	1	0	0	INIT[12]
0	1	1	0	1	INIT[13]
0	1	1	1	0	INIT[14]
0	1	1	1	1	INIT[15]
1	0	0	0	0	INIT[16]
1	0	0	0	1	INIT[17]
1	0	0	1	0	INIT[18]
1	0	0	1	1	INIT[19]
1	0	1	0	0	INIT[20]
1	0	1	0	1	INIT[21]
1	0	1	1	0	INIT[22]
1	0	1	1	1	INIT[23]
1	1	0	0	0	INIT[24]
1	1	0	0	1	INIT[25]
1	1	0	1	0	INIT[26]

Input					Output
1	1	0	1	1	INIT[27]
1	1	1	0	0	INIT[28]
1	1	1	0	1	INIT[29]
1	1	1	1	0	INIT[30]
1	1	1	1	1	INIT[31]

3.9.3 Paramater Description

Table 3-19 GTP_LUT5 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
INIT	0 ~ 2^32-1	32'h0000_0000	Output Configuration Parameter

3.9.4 Instantiation template

```
GTP_LUT5
#(
.INIT     (32'h0000_0000)
)GTP_LUT5_inst (
.Z        (z),
.I0       (i0),
.I1       (i1),
.I2       (i2),
.I3       (i3),
.I4       (i4)
);
```

3.10 GTP_LUT5CARRY

3.10.1 Description of Functionality

GTP_LUT5CARRY is a fast carry logic, typically used for counter counting, subtraction, address logic, etc. The structure block diagram is shown below.

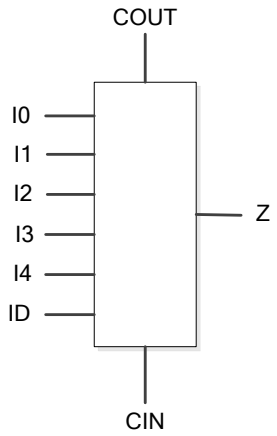

Figure 3-10 GTP_LUT5CARRY Structure Block Diagram

3.10.2 Port Description

Table 3-20 GTP_LUT5CARRY Port Description

Port	Direction	Function Description
I0	Input	Input Signal
ID	Input	Input signal, valid when ID_TO_LUT = "TRUE"
I1	Input	Input Signal
I2	Input	Input Signal
I3	Input	Input Signal
I4	Input	Input signal, valid when I4_TO_CARRY = "TRUE"
CIN	Input	Cascade input, valid when CIN_TO_LUT = "TRUE", must be connected to COUT
COUT	Output	Cascade output
Z	Output	Output signal

3.10.3 Paramater Description

Table 3-21 GTP_LUT5CARRY Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
INIT	32'h0 ~ 32'hffff_ffff	32'h0000_0000	Output Configuration Parameter
ID_TO_LUT	TRUE: The selection of ID is valid; FALSE: The selection of I0 is valid.	"FALSE"	Select either I0 or ID as an input for the LUT
CIN_TO_LUT	TRUE: The selection of CIN is valid; FALSE: The selection of I0 is valid.	"TRUE"	Select either CIN or I0 as an input for the LUT
I4_TO_CARRY	TRUE: The selection of I4 is valid;	"TRUE"	Select the output of either I4 or LUT4 for the CARRY

Parameter Name	Valid Values	Defaults	Function Description
	FALSE: The selection of LUT4 output is valid.		CHAIN
I4_TO_LUT	TRUE: The selection of I4 is valid; FALSE: The selection of 1'b1 is valid.	"FALSE"	Select either I4 or 1'b1 as an input for the LUT

3.10.4 Instantiation template

```
GTP_LUT5CARRY
#(
.INIT              (32'h0000_0000),
.ID_TO_LUT         ("FALSE"),
.CIN_TO_LUT        ("TRUE"),
.I4_TO_CARRY       ("TRUE"),
.I4_TO_LUT         ("FALSE")
)GTP_LUT5CARRY_inst (
.COUT      (cout),
.Z         (z),
.CIN             (cin),
.I0        (i0),
.ID        (id),
.I1        (i1),
.I2        (i2),
.I3        (i3),
.I4        (i4));
```

3.11 GTP_LUT6

3.11.1 Description of Functionality

GTP_LUT6 is a 6-input Look Up Table, with different INIT parameter values corresponding to different functions of LUT6. The corresponding INIT parameter must be specified when used. The structure block diagram is shown below.

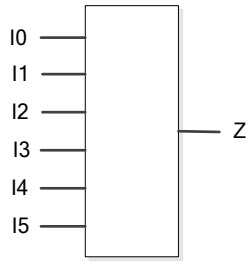

Figure 3-11 GTP_LUT6 Structure Block Diagram

3.11.2 Port Description

Table 3-22 GTP_LUT6 Port Description

Port	**Direction**	**Function Description**
Z	Output	Output signal
I0	Input	Input Signal
I1	Input	Input Signal
I2	Input	Input Signal
I3	Input	Input Signal
I4	Input	Input Signal
I5	Input	Input Signal

Truth Table:

Table 3-23 GTP_LUT6 Truth Table

Input						**Output**
I5	I4	I3	I2	I1	I0	Z
0	0	0	0	0	0	INIT[0]
0	0	0	0	0	1	INIT[1]
0	0	0	0	1	0	INIT[2]
0	0	0	0	1	1	INIT[3]
0	0	0	1	0	0	INIT[4]
0	0	0	1	0	1	INIT[5]
0	0	0	1	1	0	INIT[6]
0	0	0	1	1	1	INIT[7]
0	0	1	0	0	0	INIT[8]
0	0	1	0	0	1	INIT[9]
0	0	1	0	1	0	INIT[10]
0	0	1	0	1	1	INIT[11]
0	0	1	1	0	0	INIT[12]
0	0	1	1	0	1	INIT[13]
0	0	1	1	1	0	INIT[14]
0	0	1	1	1	1	INIT[15]

Input						Output
0	1	0	0	0	0	INIT[16]
0	1	0	0	0	1	INIT[17]
0	1	0	0	1	0	INIT[18]
0	1	0	0	1	1	INIT[19]
0	1	0	1	0	0	INIT[20]
0	1	0	1	0	1	INIT[21]
0	1	0	1	1	0	INIT[22]
0	1	0	1	1	1	INIT[23]
0	1	1	0	0	0	INIT[24]
0	1	1	0	0	1	INIT[25]
0	1	1	0	1	0	INIT[26]
0	1	1	0	1	1	INIT[27]
0	1	1	1	0	0	INIT[28]
0	1	1	1	0	1	INIT[29]
0	1	1	1	1	0	INIT[30]
0	1	1	1	1	1	INIT[31]
1	0	0	0	0	0	INIT[32]
1	0	0	0	0	1	INIT[33]
1	0	0	0	1	0	INIT[34]
1	0	0	0	1	1	INIT[35]
1	0	0	1	0	0	INIT[36]
1	0	0	1	0	1	INIT[37]
1	0	0	1	1	0	INIT[38]
1	0	0	1	1	1	INIT[39]
1	0	1	0	0	0	INIT[40]
1	0	1	0	0	1	INIT[41]
1	0	1	0	1	0	INIT[42]
1	0	1	0	1	1	INIT[43]
1	0	1	1	0	0	INIT[44]
1	0	1	1	0	1	INIT[45]
1	0	1	1	1	0	INIT[46]
1	0	1	1	1	1	INIT[47]
1	1	0	0	0	0	INIT[48]
1	1	0	0	0	1	INIT[49]
1	1	0	0	1	0	INIT[50]
1	1	0	0	1	1	INIT[51]
1	1	0	1	0	0	INIT[52]
1	1	0	1	0	1	INIT[53]
1	1	0	1	1	0	INIT[54]

Input						Output
1	1	0	1	1	1	INIT[55]
1	1	1	0	0	0	INIT[56]
1	1	1	0	0	1	INIT[57]
1	1	1	0	1	0	INIT[58]
1	1	1	0	1	1	INIT[59]
1	1	1	1	0	0	INIT[60]
1	1	1	1	0	1	INIT[61]
1	1	1	1	1	0	INIT[62]
1	1	1	1	1	1	INIT[63]

3.11.3 Paramater Description

Table 3-24 GTP_LUT6 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
INIT	0 ~ 2^64-1	64’h0000_0000_0000_0000	Output Configuration Parameter

3.11.4 Instantiation template

```
GTP_LUT6
#(
.INIT    (64'h0000_0000_0000_0000)
)GTP_LUT6_inst (
.Z       (z),
.I0      (i0),
.I1      (i1),
.I2      (i2),
.I3      (i3),
.I4      (i4),
.I5      (i5)
);
```

3.12 GTP_LUT7

3.12.1 Description of Functionality

GTP_LUT7is a 7-input Look Up Table, with different INIT parameter values corresponding to different functions of LUT7; the corresponding INIT parameter must be specified when used. The structure block diagram is shown below.

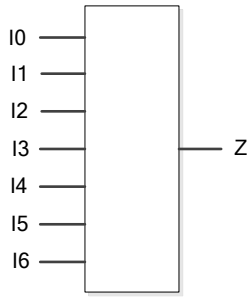

Figure 3-12 GTP_LUT7 Structure Block Diagram

3.12.2 Port Description

Table 3-25 GTP_LUT7 Port Description

Port	**Direction**	**Function Description**
Z	Output	Output signal
I0	Input	Input Signal
I1	Input	Input Signal
I2	Input	Input Signal
I3	Input	Input Signal
I4	Input	Input Signal
I5	Input	Input Signal
I6	Input	Input Signal

Truth Table:

Table 3-26 GTP_LUT7 Truth Table

Input							**Output**
I6	I5	I4	I3	I2	I1	I0	Z
0	0	0	0	0	0	0	INIT[0]
0	0	0	0	0	0	1	INIT[1]
0	0	0	0	0	1	0	INIT[2]
0	0	0	0	0	1	1	INIT[3]
0	0	0	0	1	0	0	INIT[4]
0	0	0	0	1	0	1	INIT[5]
0	0	0	0	1	1	0	INIT[6]
0	0	0	0	1	1	1	INIT[7]
0	0	0	1	0	0	0	INIT[8]
0	0	0	1	0	0	1	INIT[9]
0	0	0	1	0	1	0	INIT[10]
0	0	0	1	0	1	1	INIT[11]
0	0	0	1	1	0	0	INIT[12]
0	0	0	1	1	0	1	INIT[13]

Input							Output
0	0	0	1	1	1	0	INIT[14]
0	0	0	1	1	1	1	INIT[15]
0	0	1	0	0	0	0	INIT[16]
0	0	1	0	0	0	1	INIT[17]
0	0	1	0	0	1	0	INIT[18]
0	0	1	0	0	1	1	INIT[19]
0	0	1	0	1	0	0	INIT[20]
0	0	1	0	1	0	1	INIT[21]
0	0	1	0	1	1	0	INIT[22]
0	0	1	0	1	1	1	INIT[23]
0	0	1	1	0	0	0	INIT[24]
0	0	1	1	0	0	1	INIT[25]
0	0	1	1	0	1	0	INIT[26]
0	0	1	1	0	1	1	INIT[27]
0	0	1	1	1	0	0	INIT[28]
0	0	1	1	1	0	1	INIT[29]
0	0	1	1	1	1	0	INIT[30]
0	0	1	1	1	1	1	INIT[31]
0	1	0	0	0	0	0	INIT[32]
0	1	0	0	0	0	1	INIT[33]
0	1	0	0	0	1	0	INIT[34]
0	1	0	0	0	1	1	INIT[35]
0	1	0	0	1	0	0	INIT[36]
0	1	0	0	1	0	1	INIT[37]
0	1	0	0	1	1	0	INIT[38]
0	1	0	0	1	1	1	INIT[39]
0	1	0	1	0	0	0	INIT[40]
0	1	0	1	0	0	1	INIT[41]
0	1	0	1	0	1	0	INIT[42]
0	1	0	1	0	1	1	INIT[43]
0	1	0	1	1	0	0	INIT[44]
0	1	0	1	1	0	1	INIT[45]
0	1	0	1	1	1	0	INIT[46]
0	1	0	1	1	1	1	INIT[47]
0	1	1	0	0	0	0	INIT[48]
0	1	1	0	0	0	1	INIT[49]
0	1	1	0	0	1	0	INIT[50]
0	1	1	0	0	1	1	INIT[51]
0	1	1	0	1	0	0	INIT[52]

Input							Output
0	1	1	0	1	0	1	INIT[53]
0	1	1	0	1	1	0	INIT[54]
0	1	1	0	1	1	1	INIT[55]
0	1	1	1	0	0	0	INIT[56]
0	1	1	1	0	0	1	INIT[57]
0	1	1	1	0	1	0	INIT[58]
0	1	1	1	0	1	1	INIT[59]
0	1	1	1	1	0	0	INIT[60]
0	1	1	1	1	0	1	INIT[61]
0	1	1	1	1	1	0	INIT[62]
0	1	1	1	1	1	1	INIT[63]
1	0	0	0	0	0	0	INIT[64]
1	0	0	0	0	0	1	INIT[65]
1	0	0	0	0	1	0	INIT[66]
1	0	0	0	0	1	1	INIT[67]
1	0	0	0	1	0	0	INIT[68]
1	0	0	0	1	0	1	INIT[69]
1	0	0	0	1	1	0	INIT[70]
1	0	0	0	1	1	1	INIT[71]
1	0	0	1	0	0	0	INIT[72]
1	0	0	1	0	0	1	INIT[73]
1	0	0	1	0	1	0	INIT[74]
1	0	0	1	0	1	1	INIT[75]
1	0	0	1	1	0	0	INIT[76]
1	0	0	1	1	0	1	INIT[77]
1	0	0	1	1	1	0	INIT[78]
1	0	0	1	1	1	1	INIT[79]
1	0	1	0	0	0	0	INIT[80]
1	0	1	0	0	0	1	INIT[81]
1	0	1	0	0	1	0	INIT[82]
1	0	1	0	0	1	1	INIT[83]
1	0	1	0	1	0	0	INIT[84]
1	0	1	0	1	0	1	INIT[85]
1	0	1	0	1	1	0	INIT[86]
1	0	1	0	1	1	1	INIT[87]
1	0	1	1	0	0	0	INIT[88]
1	0	1	1	0	0	1	INIT[89]
1	0	1	1	0	1	0	INIT[90]
1	0	1	1	0	1	1	INIT[91]

Input							Output
1	0	1	1	1	0	0	INIT[92]
1	0	1	1	1	0	1	INIT[93]
1	0	1	1	1	1	0	INIT[94]
1	0	1	1	1	1	1	INIT[95]
1	1	0	0	0	0	0	INIT[96]
1	1	0	0	0	0	1	INIT[97]
1	1	0	0	0	1	0	INIT[98]
1	1	0	0	0	1	1	INIT[99]
1	1	0	0	1	0	0	INIT[100]
1	1	0	0	1	0	1	INIT[101]
1	1	0	0	1	1	0	INIT[102]
1	1	0	0	1	1	1	INIT[103]
1	1	0	1	0	0	0	INIT[104]
1	1	0	1	0	0	1	INIT[105]
1	1	0	1	0	1	0	INIT[106]
1	1	0	1	0	1	1	INIT[107]
1	1	0	1	1	0	0	INIT[108]
1	1	0	1	1	0	1	INIT[109]
1	1	0	1	1	1	0	INIT[110]
1	1	0	1	1	1	1	INIT[111]
1	1	1	0	0	0	0	INIT[112]
1	1	1	0	0	0	1	INIT[113]
1	1	1	0	0	1	0	INIT[114]
1	1	1	0	0	1	1	INIT[115]
1	1	1	0	1	0	0	INIT[116]
1	1	1	0	1	0	1	INIT[117]
1	1	1	0	1	1	0	INIT[118]
1	1	1	0	1	1	1	INIT[119]
1	1	1	1	0	0	0	INIT[120]
1	1	1	1	0	0	1	INIT[121]
1	1	1	1	0	1	0	INIT[122]
1	1	1	1	0	1	1	INIT[123]
1	1	1	1	1	0	0	INIT[124]
1	1	1	1	1	0	1	INIT[125]
1	1	1	1	1	1	0	INIT[126]
1	1	1	1	1	1	1	INIT[127]

3.12.3 Paramater Description

Table 3-27 GTP_LUT7 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
INIT	0 ~ 2^128-1	128'h00000000_00000000_00000000_00000000	Output Configuration Parameter

3.12.4 Instantiation template

```
GTP_LUT7
#(
.INIT    (128'h00000000_00000000_00000000_00000000)
)GTP_LUT7_inst (
.Z       (z),
.I0      (i0),
.I1      (i1),
.I2      (i2),
.I3      (i3),
.I4      (i4),
.I5      (i5),
.I6      (i6)
);
```

3.13 GTP_LUT8

3.13.1 Description of Functionality

GTP_LUT8is an 8-input Look Up Table, with different INIT parameter values corresponding to different functions of LUT8; the corresponding INIT parameter must be specified when used. The structure block diagram is shown below.

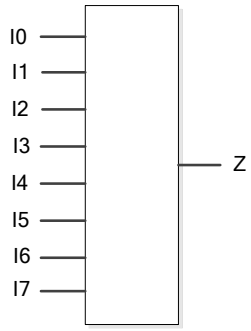

Figure 3-13 GTP_LUT8 Structure Block Diagram

3.13.2 Port Description

Table 3-28 GTP_LUT8 Port Description

Port	**Direction**	**Function Description**
Z	Output	Output signal
I0	Input	Input Signal
I1	Input	Input Signal
I2	Input	Input Signal
I3	Input	Input Signal
I4	Input	Input Signal
I5	Input	Input Signal
I6	Input	Input Signal
I7	Input	Input Signal

Truth Table:

Table 3-29 GTP_LUT8 Truth Table

Input								**Output**
I7	I6	I5	I4	I3	I2	I1	I0	Z
0	0	0	0	0	0	0	0	INIT[0]
0	0	0	0	0	0	0	1	INIT[1]
0	0	0	0	0	0	1	0	INIT[2]
0	0	0	0	0	0	1	1	INIT[3]
0	0	0	0	0	1	0	0	INIT[4]
0	0	0	0	0	1	0	1	INIT[5]
0	0	0	0	0	1	1	0	INIT[6]
0	0	0	0	0	1	1	1	INIT[7]
0	0	0	0	1	0	0	0	INIT[8]
0	0	0	0	1	0	0	1	INIT[9]
0	0	0	0	1	0	1	0	INIT[10]
0	0	0	0	1	0	1	1	INIT[11]

Input								Output
0	0	0	0	1	1	0	0	INIT[12]
0	0	0	0	1	1	0	1	INIT[13]
0	0	0	0	1	1	1	0	INIT[14]
0	0	0	0	1	1	1	1	INIT[15]
0	0	0	1	0	0	0	0	INIT[16]
0	0	0	1	0	0	0	1	INIT[17]
0	0	0	1	0	0	1	0	INIT[18]
0	0	0	1	0	0	1	1	INIT[19]
0	0	0	1	0	1	0	0	INIT[20]
0	0	0	1	0	1	0	1	INIT[21]
0	0	0	1	0	1	1	0	INIT[22]
0	0	0	1	0	1	1	1	INIT[23]
0	0	0	1	1	0	0	0	INIT[24]
0	0	0	1	1	0	0	1	INIT[25]
0	0	0	1	1	0	1	0	INIT[26]
0	0	0	1	1	0	1	1	INIT[27]
0	0	0	1	1	1	0	0	INIT[28]
0	0	0	1	1	1	0	1	INIT[29]
0	0	0	1	1	1	1	0	INIT[30]
0	0	0	1	1	1	1	1	INIT[31]
0	0	1	0	0	0	0	0	INIT[32]
0	0	1	0	0	0	0	1	INIT[33]
0	0	1	0	0	0	1	0	INIT[34]
0	0	1	0	0	0	1	1	INIT[35]
0	0	1	0	0	1	0	0	INIT[36]
0	0	1	0	0	1	0	1	INIT[37]
0	0	1	0	0	1	1	0	INIT[38]
0	0	1	0	0	1	1	1	INIT[39]
0	0	1	0	1	0	0	0	INIT[40]
0	0	1	0	1	0	0	1	INIT[41]
0	0	1	0	1	0	1	0	INIT[42]
0	0	1	0	1	0	1	1	INIT[43]
0	0	1	0	1	1	0	0	INIT[44]
0	0	1	0	1	1	0	1	INIT[45]
0	0	1	0	1	1	1	0	INIT[46]
0	0	1	0	1	1	1	1	INIT[47]
0	0	1	1	0	0	0	0	INIT[48]
0	0	1	1	0	0	0	1	INIT[49]
0	0	1	1	0	0	1	0	INIT[50]

Input								Output
0	0	1	1	0	0	1	1	INIT[51]
0	0	1	1	0	1	0	0	INIT[52]
0	0	1	1	0	1	0	1	INIT[53]
0	0	1	1	0	1	1	0	INIT[54]
0	0	1	1	0	1	1	1	INIT[55]
0	0	1	1	1	0	0	0	INIT[56]
0	0	1	1	1	0	0	1	INIT[57]
0	0	1	1	1	0	1	0	INIT[58]
0	0	1	1	1	0	1	1	INIT[59]
0	0	1	1	1	1	0	0	INIT[60]
0	0	1	1	1	1	0	1	INIT[61]
0	0	1	1	1	1	1	0	INIT[62]
0	0	1	1	1	1	1	1	INIT[63]
0	1	0	0	0	0	0	0	INIT[64]
0	1	0	0	0	0	0	1	INIT[65]
0	1	0	0	0	0	1	0	INIT[66]
0	1	0	0	0	0	1	1	INIT[67]
0	1	0	0	0	1	0	0	INIT[68]
0	1	0	0	0	1	0	1	INIT[69]
0	1	0	0	0	1	1	0	INIT[70]
0	1	0	0	0	1	1	1	INIT[71]
0	1	0	0	1	0	0	0	INIT[72]
0	1	0	0	1	0	0	1	INIT[73]
0	1	0	0	1	0	1	0	INIT[74]
0	1	0	0	1	0	1	1	INIT[75]
0	1	0	0	1	1	0	0	INIT[76]
0	1	0	0	1	1	0	1	INIT[77]
0	1	0	0	1	1	1	0	INIT[78]
0	1	0	0	1	1	1	1	INIT[79]
0	1	0	1	0	0	0	0	INIT[80]
0	1	0	1	0	0	0	1	INIT[81]
0	1	0	1	0	0	1	0	INIT[82]
0	1	0	1	0	0	1	1	INIT[83]
0	1	0	1	0	1	0	0	INIT[84]
0	1	0	1	0	1	0	1	INIT[85]
0	1	0	1	0	1	1	0	INIT[86]
0	1	0	1	0	1	1	1	INIT[87]
0	1	0	1	1	0	0	0	INIT[88]
0	1	0	1	1	0	0	1	INIT[89]

Input								Output
0	1	0	1	1	0	1	0	INIT[90]
0	1	0	1	1	0	1	1	INIT[91]
0	1	0	1	1	1	0	0	INIT[92]
0	1	0	1	1	1	0	1	INIT[93]
0	1	0	1	1	1	1	0	INIT[94]
0	1	0	1	1	1	1	1	INIT[95]
0	1	1	0	0	0	0	0	INIT[96]
0	1	1	0	0	0	0	1	INIT[97]
0	1	1	0	0	0	1	0	INIT[98]
0	1	1	0	0	0	1	1	INIT[99]
0	1	1	0	0	1	0	0	INIT[100]
0	1	1	0	0	1	0	1	INIT[101]
0	1	1	0	0	1	1	0	INIT[102]
0	1	1	0	0	1	1	1	INIT[103]
0	1	1	0	1	0	0	0	INIT[104]
0	1	1	0	1	0	0	1	INIT[105]
0	1	1	0	1	0	1	0	INIT[106]
0	1	1	0	1	0	1	1	INIT[107]
0	1	1	0	1	1	0	0	INIT[108]
0	1	1	0	1	1	0	1	INIT[109]
0	1	1	0	1	1	1	0	INIT[110]
0	1	1	0	1	1	1	1	INIT[111]
0	1	1	1	0	0	0	0	INIT[112]
0	1	1	1	0	0	0	1	INIT[113]
0	1	1	1	0	0	1	0	INIT[114]
0	1	1	1	0	0	1	1	INIT[115]
0	1	1	1	0	1	0	0	INIT[116]
0	1	1	1	0	1	0	1	INIT[117]
0	1	1	1	0	1	1	0	INIT[118]
0	1	1	1	0	1	1	1	INIT[119]
0	1	1	1	1	0	0	0	INIT[120]
0	1	1	1	1	0	0	1	INIT[121]
0	1	1	1	1	0	1	0	INIT[122]
0	1	1	1	1	0	1	1	INIT[123]
0	1	1	1	1	1	0	0	INIT[124]
0	1	1	1	1	1	0	1	INIT[125]
0	1	1	1	1	1	1	0	INIT[126]
0	1	1	1	1	1	1	1	INIT[127]
1	0	0	0	0	0	0	0	INIT[128]

Input								Output
1	0	0	0	0	0	0	1	INIT[129]
1	0	0	0	0	0	1	0	INIT[130]
1	0	0	0	0	0	1	1	INIT[131]
1	0	0	0	0	1	0	0	INIT[132]
1	0	0	0	0	1	0	1	INIT[133]
1	0	0	0	0	1	1	0	INIT[134]
1	0	0	0	0	1	1	1	INIT[135]
1	0	0	0	1	0	0	0	INIT[136]
1	0	0	0	1	0	0	1	INIT[137]
1	0	0	0	1	0	1	0	INIT[138]
1	0	0	0	1	0	1	1	INIT[139]
1	0	0	0	1	1	0	0	INIT[140]
1	0	0	0	1	1	0	1	INIT[141]
1	0	0	0	1	1	1	0	INIT[142]
1	0	0	0	1	1	1	1	INIT[143]
1	0	0	1	0	0	0	0	INIT[144]
1	0	0	1	0	0	0	1	INIT[145]
1	0	0	1	0	0	1	0	INIT[146]
1	0	0	1	0	0	1	1	INIT[147]
1	0	0	1	0	1	0	0	INIT[148]
1	0	0	1	0	1	0	1	INIT[149]
1	0	0	1	0	1	1	0	INIT[150]
1	0	0	1	0	1	1	1	INIT[151]
1	0	0	1	1	0	0	0	INIT[152]
1	0	0	1	1	0	0	1	INIT[153]
1	0	0	1	1	0	1	0	INIT[154]
1	0	0	1	1	0	1	1	INIT[155]
1	0	0	1	1	1	0	0	INIT[156]
1	0	0	1	1	1	0	1	INIT[157]
1	0	0	1	1	1	1	0	INIT[158]
1	0	0	1	1	1	1	1	INIT[159]
1	0	1	0	0	0	0	0	INIT[160]
1	0	1	0	0	0	0	1	INIT[161]
1	0	1	0	0	0	1	0	INIT[162]
1	0	1	0	0	0	1	1	INIT[163]
1	0	1	0	0	1	0	0	INIT[164]
1	0	1	0	0	1	0	1	INIT[165]
1	0	1	0	0	1	1	0	INIT[166]
1	0	1	0	0	1	1	1	INIT[167]

Input								Output
1	0	1	0	1	0	0	0	INIT[168]
1	0	1	0	1	0	0	1	INIT[169]
1	0	1	0	1	0	1	0	INIT[170]
1	0	1	0	1	0	1	1	INIT[171]
1	0	1	0	1	1	0	0	INIT[172]
1	0	1	0	1	1	0	1	INIT[173]
1	0	1	0	1	1	1	0	INIT[174]
1	0	1	0	1	1	1	1	INIT[175]
1	0	1	1	0	0	0	0	INIT[176]
1	0	1	1	0	0	0	1	INIT[177]
1	0	1	1	0	0	1	0	INIT[178]
1	0	1	1	0	0	1	1	INIT[179]
1	0	1	1	0	1	0	0	INIT[180]
1	0	1	1	0	1	0	1	INIT[181]
1	0	1	1	0	1	1	0	INIT[182]
1	0	1	1	0	1	1	1	INIT[183]
1	0	1	1	1	0	0	0	INIT[184]
1	0	1	1	1	0	0	1	INIT[185]
1	0	1	1	1	0	1	0	INIT[186]
1	0	1	1	1	0	1	1	INIT[187]
1	0	1	1	1	1	0	0	INIT[188]
1	0	1	1	1	1	0	1	INIT[189]
1	0	1	1	1	1	1	0	INIT[190]
1	0	1	1	1	1	1	1	INIT[191]
1	1	0	0	0	0	0	0	INIT[192]
1	1	0	0	0	0	0	1	INIT[193]
1	1	0	0	0	0	1	0	INIT[194]
1	1	0	0	0	0	1	1	INIT[195]
1	1	0	0	0	1	0	0	INIT[196]
1	1	0	0	0	1	0	1	INIT[197]
1	1	0	0	0	1	1	0	INIT[198]
1	1	0	0	0	1	1	1	INIT[199]
1	1	0	0	1	0	0	0	INIT[200]
1	1	0	0	1	0	0	1	INIT[201]
1	1	0	0	1	0	1	0	INIT[202]
1	1	0	0	1	0	1	1	INIT[203]
1	1	0	0	1	1	0	0	INIT[204]
1	1	0	0	1	1	0	1	INIT[205]
1	1	0	0	1	1	1	0	INIT[206]

Input								Output
1	1	0	0	1	1	1	1	INIT[207]
1	1	0	1	0	0	0	0	INIT[208]
1	1	0	1	0	0	0	1	INIT[209]
1	1	0	1	0	0	1	0	INIT[210]
1	1	0	1	0	0	1	1	INIT[211]
1	1	0	1	0	1	0	0	INIT[212]
1	1	0	1	0	1	0	1	INIT[213]
1	1	0	1	0	1	1	0	INIT[214]
1	1	0	1	0	1	1	1	INIT[215]
1	1	0	1	1	0	0	0	INIT[216]
1	1	0	1	1	0	0	1	INIT[217]
1	1	0	1	1	0	1	0	INIT[218]
1	1	0	1	1	0	1	1	INIT[219]
1	1	0	1	1	1	0	0	INIT[220]
1	1	0	1	1	1	0	1	INIT[221]
1	1	0	1	1	1	1	0	INIT[222]
1	1	0	1	1	1	1	1	INIT[223]
1	1	1	0	0	0	0	0	INIT[224]
1	1	1	0	0	0	0	1	INIT[225]
1	1	1	0	0	0	1	0	INIT[226]
1	1	1	0	0	0	1	1	INIT[227]
1	1	1	0	0	1	0	0	INIT[228]
1	1	1	0	0	1	0	1	INIT[229]
1	1	1	0	0	1	1	0	INIT[230]
1	1	1	0	0	1	1	1	INIT[231]
1	1	1	0	1	0	0	0	INIT[232]
1	1	1	0	1	0	0	1	INIT[233]
1	1	1	0	1	0	1	0	INIT[234]
1	1	1	0	1	0	1	1	INIT[235]
1	1	1	0	1	1	0	0	INIT[236]
1	1	1	0	1	1	0	1	INIT[237]
1	1	1	0	1	1	1	0	INIT[238]
1	1	1	0	1	1	1	1	INIT[239]
1	1	1	1	0	0	0	0	INIT[240]
1	1	1	1	0	0	0	1	INIT[241]
1	1	1	1	0	0	1	0	INIT[242]
1	1	1	1	0	0	1	1	INIT[243]
1	1	1	1	0	1	0	0	INIT[244]
1	1	1	1	0	1	0	1	INIT[245]

Input								Output
1	1	1	1	0	1	1	0	INIT[246]
1	1	1	1	0	1	1	1	INIT[247]
1	1	1	1	1	0	0	0	INIT[248]
1	1	1	1	1	0	0	1	INIT[249]
1	1	1	1	1	0	1	0	INIT[250]
1	1	1	1	1	0	1	1	INIT[251]
1	1	1	1	1	1	0	0	INIT[252]
1	1	1	1	1	1	0	1	INIT[253]
1	1	1	1	1	1	1	0	INIT[254]
1	1	1	1	1	1	1	1	INIT[255]

3.13.3 Paramater Description

Table 3-30 GTP_LUT8 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
INIT	0 ~ 2^256-1	256'h0000000000000000_0000000000000000 _0000000000000000_0000000000000000	Output Configuration Parameter

3.13.4 Instantiation template

```
GTP_LUT8
#(
.INIT    (256'h0000000000000000_0000000000000000_0000000000000000_0000000000000000)
)GTP_LUT8_inst (
.Z       (z),
.I0      (i0),
.I1      (i1),
.I2      (i2),
.I3      (i3),
.I4      (i4),
.I5      (i5),
.I6      (i6),
.I7      (i7)
);
```

3.14 GTP_LUTMUX4

3.14.1 Description of Functionality

GTP_LUTMUX4is a 4:1 multiplexer, with I0, I1, I2, and I3 as data inputs, S1 and S0 as selection signals. It outputs I0 when {S1, S0} is 2'b00, I1 when {S1, S0} is 2'b01, I2 when {S1, S0} is 2'b10, and I3 when {S1, S0} is 2'b11. Its structure block diagram is as follows.

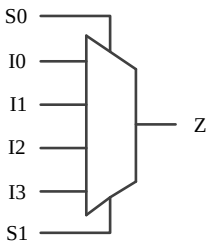

Figure 3-14 GTP_LUTMUX4 Structure Block Diagram

3.14.2 Port Description

Table 3-31 GTP_LUTMUX4 Port Description

Port	**Direction**	**Function Description**
S0	Input	Select signal
S1	Input	Select signal
I0	Input	MUX input signal
I1	Input	MUX input signal
I2	Input	MUX input signal
I3	Input	MUX input signal
Z	Output	MUX output signal

Truth Table:

Table 3-32 GTP_LUTMUX4 Truth Table

Input						**Output**
S1	S0	I3	I2	I1	I0	Z
0	0	?	?	?	0	0
0	0	?	?	?	1	1
0	1	?	?	0	?	0
0	1	?	?	1	?	1
1	0	?	0	?	?	0
1	0	?	1	?	?	1
1	1	0	?	?	?	0
1	1	1	?	?	?	1

3.14.3 Instantiation template

```
GTP_LUTMUX4 GTP_LUTMUX4_inst
(
.S0    (s0),
.S1    (s1),
.I0    (i0),
.I1    (i1),
.I2    (i2),
.I3    (i3),
. Z    (z)
);
```

Chapter 4 ROM & RAM Related GTPs

4.1 GTP_ROM32X1

4.1.1 Description of Functionality

GTP_ROM32X1 is a ROM with an address depth of 32 bits and a data width of 1 bit. The structure block diagram is shown below.

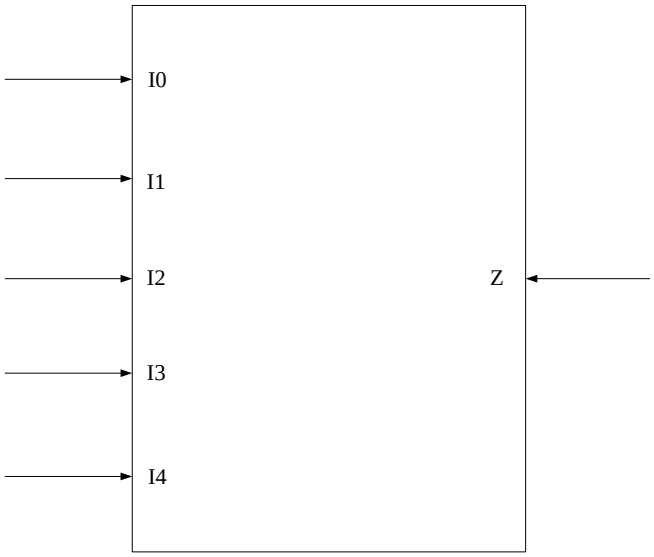

Figure 4-1 GTP_ROM32X1 Structure Block Diagram

4.1.2 Port Description

Table 4-1 GTP_ROM32X1 Port Description

Port	Direction	Function Description
I0	Input	ROM read address addr[0]
I1	Input	ROM read address addr[1]
I2	Input	ROM read address addr[2]
I3	Input	ROM read address addr[3]
I4	Input	ROM read address addr[4]
Z	Output	Read data

4.1.3 Paramater Description

Table 4-2 GTP_ROM32X1 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
INIT	32'h00000000~32'hffffffff	32'h00000000	ROM Initialization Configuration Parameters

4.1.4 Functional Description

This GTP implements the ROM storage function. Inputs I4~I0 form the read address for reading the value of the specified address of the ROM.

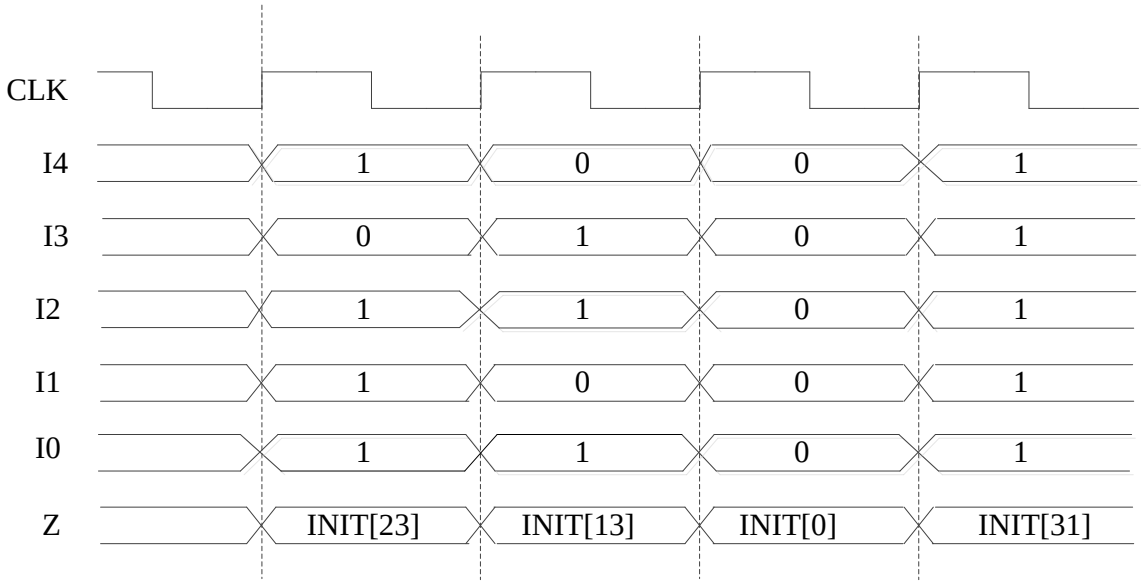

Figure 4-2 GTP_ROM32X1 Timing Diagram

4.1.5 Instantiation template

```
GTP_ROM32X1    #(
      .INIT          (32'h00000000)
)
GTP_ROM32X1_inst(
      .I0                  (     I0          ),
      .I1                  (     II          ),
      .I2                        (     I2                ),
      .I3                        (     I3          ),
      .I4                           (  I4          ),
.Z                         (     Z          )
);
```

4.2 GTP_ROM64X1

4.2.1 Description of Functionality

GTP_ROM64X1 is a ROM with an address depth of 64 bits and a data width of 1 bit. The structure block diagram is shown below.

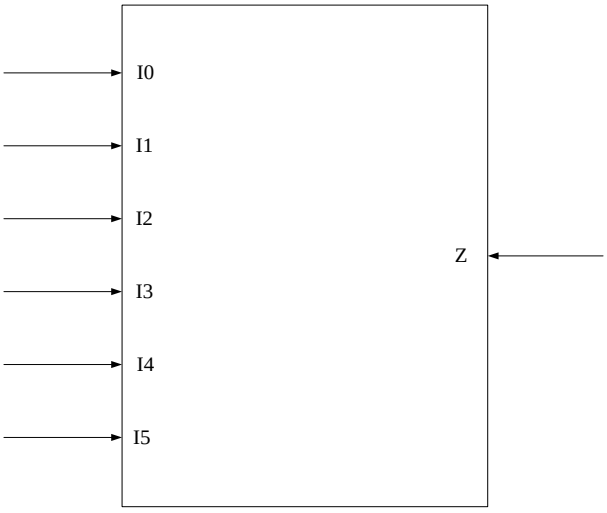

Figure 4-3 GTP_ROM64X1 Structure Block Diagram

4.2.2 Port Description

Table 4-3 GTP_ROM64X1 Port Description

Port	Direction	Function Description
I0	Input	ROM read address addr[0]
I1	Input	ROM read address addr[1]
I2	Input	ROM read address addr[2]
I3	Input	ROM read address addr[3]
I4	Input	ROM read address addr[4]
I5	Input	ROM read address addr[5]
Z	Output	Read data

4.2.3 Paramater Description

Table 4-4 GTP_ROM64X1 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
INIT	64'h00000000_00000000~64'hffffffff_ffffffff	64'h00000000_00000000	ROM Initialization Configuration Parameters

4.2.4 Functional Description

This GTP implements the ROM storage function. Inputs I4~I0 form the read address for reading the value of the specified address of the ROM.

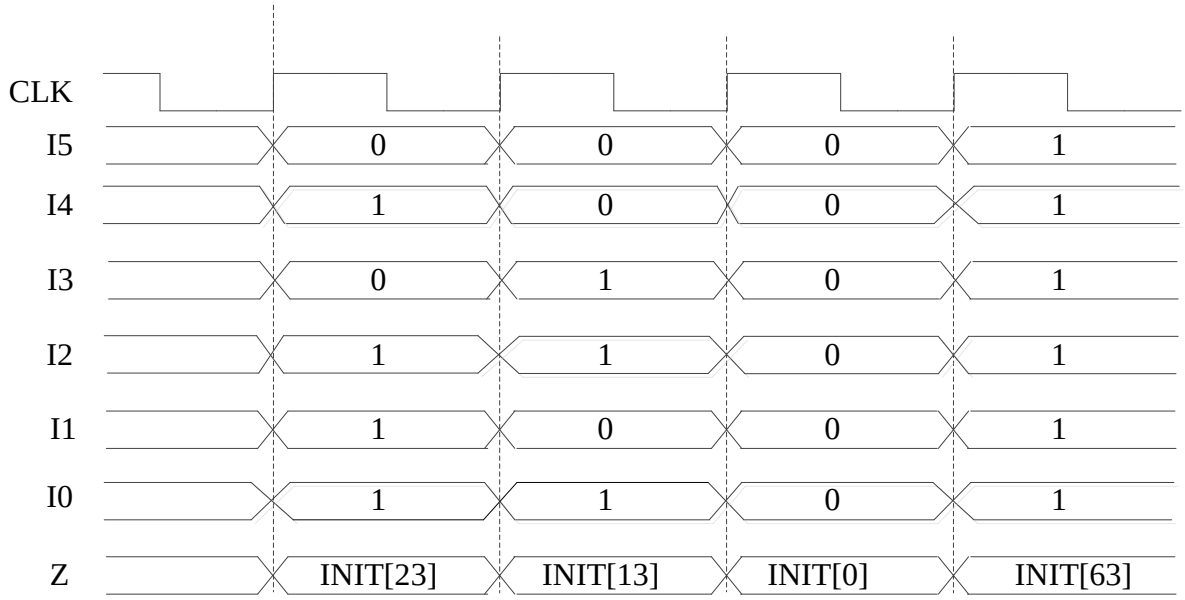

Figure 4-4 GTP_ROM64X1 Timing Diagram

4.2.5 Instantiation template

```
GTP_ROM64X1#(
    .INIT        (64'h00000000_00000000)
)
GTP_ROM64X1_inst(
    .I0          (  I0      ),
    .I1          (  II      ),
    .I2          (  I2      ),
    .I3          (  I3      ),
    .I4          (  I4      ),
    .I5          (  I5      ),
.Z               (  Z       )
);
```

4.3 GTP_ROM128X1

4.3.1 Description of Functionality

GTP_ROM128X1 is a ROM with an address depth of 128 bits and a data width of 1 bit. The structure block diagram is shown below.

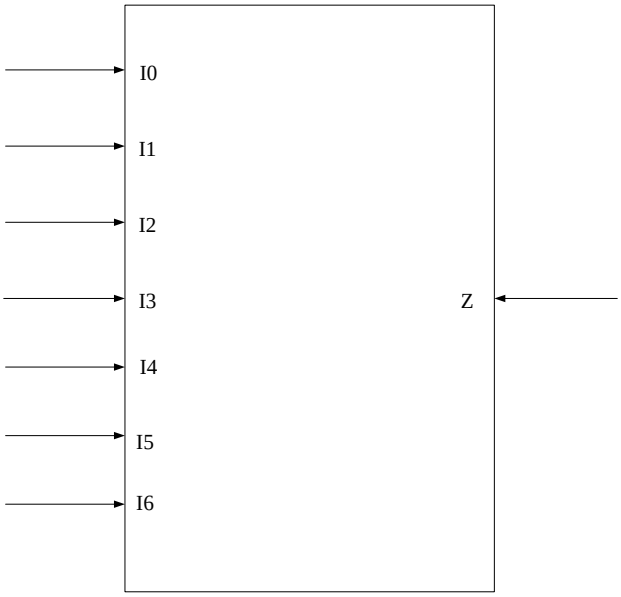

Figure 4-5 GTP_ROM128X1 Structure Block Diagram

4.3.2 Port Description

Table 4-5 GTP_ROM128X1 Port Description

Port	Direction	Function Description
I0	Input	ROM read address addr[0]
I1	Input	ROM read address addr[1]
I2	Input	ROM read address addr[2]
I3	Input	ROM read address addr[3]
I4	Input	ROM read address addr[4]
I5	Input	ROM read address addr[5]
I6	Input	ROM read address addr[6]
Z	Output	Read data

4.3.3 Paramater Description

Table 4-6 GTP_ROM128X1 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
INIT	128'h00000000_00000000_00000000_00000000~128'hffffffff_ffffffff_ffffffff_ffffffff	128'h00000000_00000000_00000000_00000000	ROM Initialization Configuration Parameters

4.3.4 Functional Description

This GTP implements the ROM storage function. Inputs I4~I0 form the read address for reading the value of the specified address of the ROM.

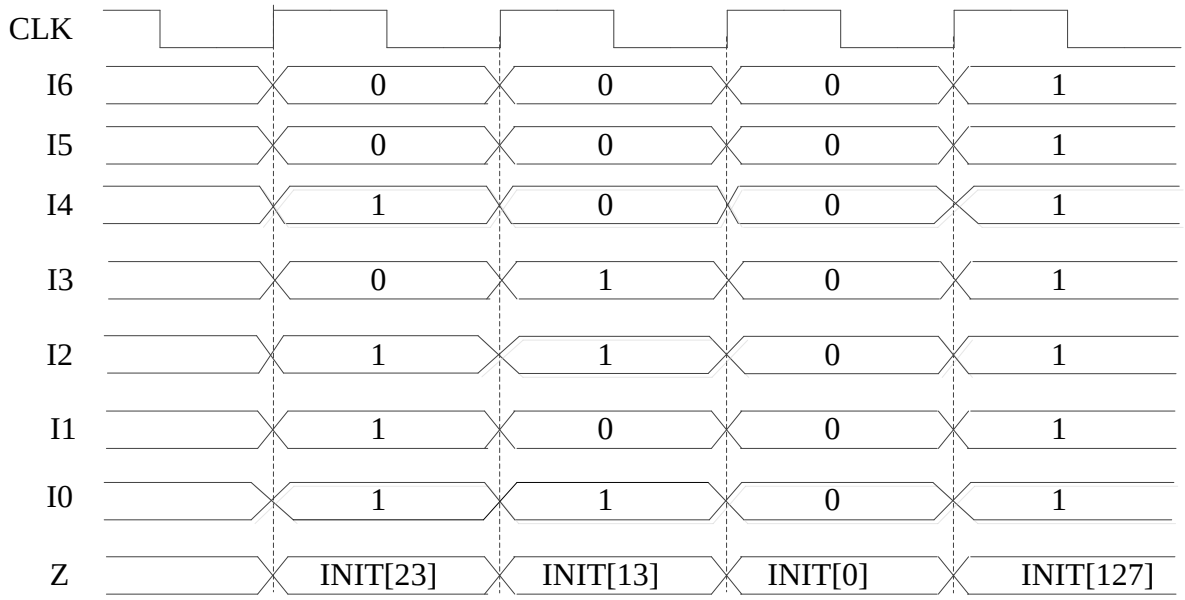

Figure 4-6 GTP_ROM128X1 Timing Diagram

4.3.5 Instantiation template

```
GTP_ROM128X1    #(
    .INIT          (128'h00000000_00000000_00000000_00000000)
)
GTP_ROM128X1_inst(
    .I0                ( I0        ),
    .I1                ( II        ),
    .I2                    ( I2            ),
    .I3                    ( I3            ),
    .I4                      ( I4        ),
    .I5                    ( I5            ),
    .I6                      ( I6        ),
.Z                     ( Z         )
);
```

4.4 GTP_ROM256X1

4.4.1 Description of Functionality

GTP_ROM256X1 is a ROM with an address depth of 256 bits and a data width of 1 bit. The structure block diagram is shown below.

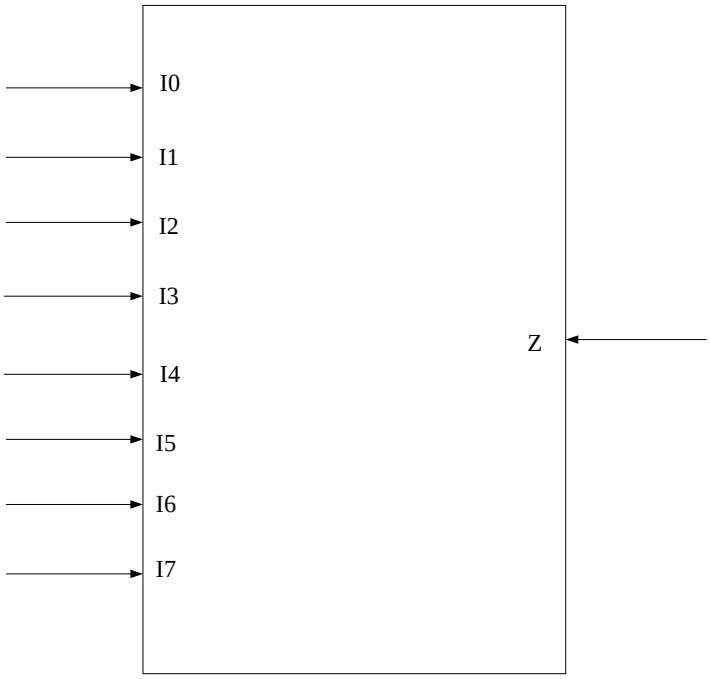

Figure 4-7 GTP_ROM256X1 Structure Block Diagram

4.4.2 Port Description

Table 4-7 GTP_ROM256X1 Port Description

Port	Direction	Function Description
I0	Input	ROM read address addr[0]
I1	Input	ROM read address addr[1]
I2	Input	ROM read address addr[2]
I3	Input	ROM read address addr[3]
I4	Input	ROM read address addr[4]
I5	Input	ROM read address addr[5]
I6	Input	ROM read address addr[6]
I7	Input	ROM read address addr[7]
Z	Output	Read data

4.4.3 Paramater Description

Table 4-8 GTP_ROM256X1 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
INIT	256'h00000000_00000000_00000000_00000000_00000000_00000000_00000000_00000000~256'hffffffff_ffffffff_ffffffff_ffffffff_ffffffff_ffffffff_ffffffff_ffffffff	256'h00000000_00000000_00000000_00000000_00000000_00000000_00000000_00000000	ROM Initialization Configuration Parameters

4.4.4 Functional Description

This GTP implements the ROM storage function. Inputs I4~I0 form the read address for reading the value of the specified address of the ROM.

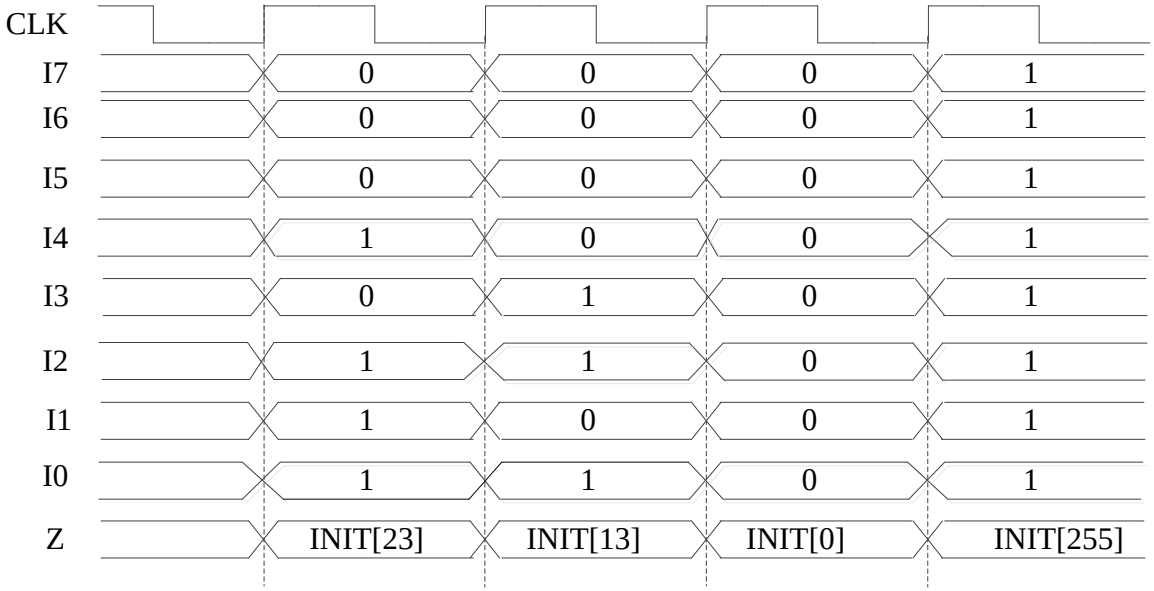

Figure 4-8 GTP_ROM256X1 Timing Diagram

4.4.5 Instantiation template

```
GTP_ROM256X1    #(
    .INIT
    (256'h00000000_00000000_00000000_00000000_00000000_00000000_00000000_00000000)
)
GTP_ROM256X1_inst(
    .I0             (   I0      ),
    .I1             (   II      ),
    .I2                 (   I2      ),
    .I3                 (   I3      ),
```

```
    .I4                 ( I4        ),
    .I5                 (  I5           ),
    .I6                 (  I6       ),
    .I7                 ( I7        ),
.Z                  (  Z        )
);
```

4.5 GTP_RAM16X4SP

4.5.1 Description of Functionality

GTP_RAM16X4SP is a single-port RAM with a data width of 4 bits and an address depth of 16 bits, and read/write address share one port. The structure block diagram is shown below.

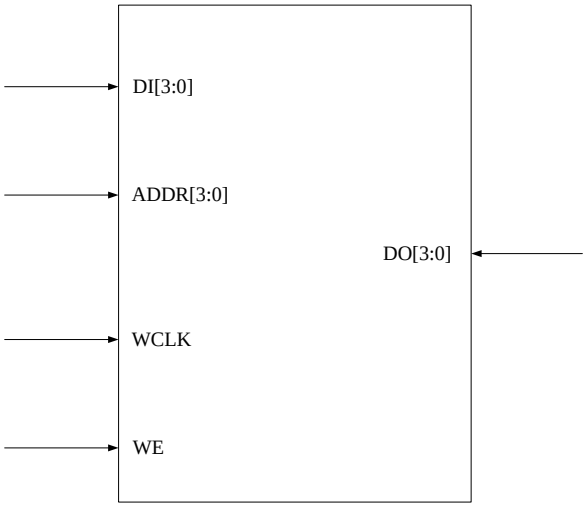

Figure 4-9 GTP_RAM16X4SP Structure Block Diagram

4.5.2 Port Description

Table 4-9 GTP_RAM16X4SP Port Description

Port	**Direction**	**Function Description**
DI	Input	Write dataWrite data
ADDR	Input	Read/write address
WCLK	Input	Write clock
WE	Input	Write enable
DO	Output	Read data

4.5.3 Paramater Description

Table 4-10 GTP_RAM16X4SP Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
INIT_0	16'h0000~16'hffff	16'h0000	Memory initialization configuration parameters
INIT_1	16'h0000~16'hffff	16'h0000	Memory initialization configuration parameters
INIT_2	16'h0000~16'hffff	16'h0000	Memory initialization configuration parameters
INIT_3	16'h0000~16'hffff	16'h0000	Memory initialization configuration parameters

4.5.4 Functional Description

For the functional description of this GTP, please refer to the distributed RAM mode section of the "***UG030001_Compa Family CPLD Configurable Logic Module (CLM) User Guide***".

4.5.5 Instantiation template

```
GTP_RAM16X4SP    #(
      .INIT_0                (16'h0000),
      .INIT_1          (16'h0000),
      .INIT_2          (16'h0000),
      .INIT_3          (16'h0000)
)
GTP_RAM16X4SP_inst(
      .DO              (    DO      ),
      .DI              (    DI      ),
      .ADDR                 (    ADDR  ),
      .WCLK                 (    WCLK  ),
      .WE                   (    WE      )
);
```

4.6 GTP_RAM16X4DP

4.6.1 Description of Functionality

GTP_RAM16X4DP is a dual-port RAM with a data width of 4 bits and an address depth of 16 bits, and read/write addresses use two different ports. The structure block diagram is shown below.

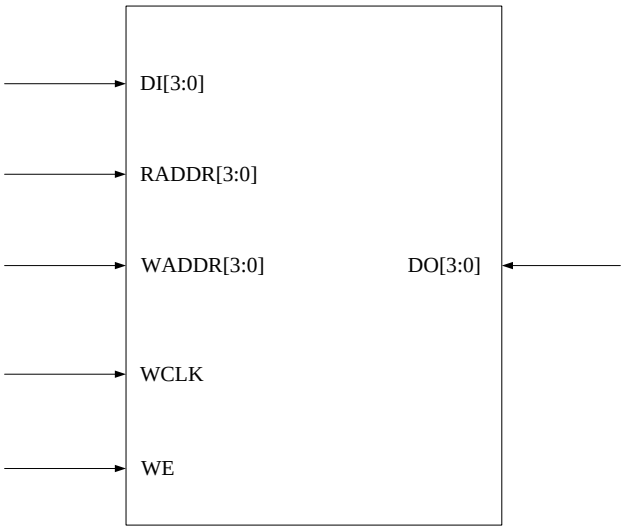

Figure 4-10 GTP_RAM16X4DP Structure Block Diagram

4.6.2 Port Description

Table 4-11 GTP_RAM16X4DP Port Description

Port	**Direction**	**Function Description**
DI	Input	Write data
RADDR	Input	Read address
WADDR	Input	Write address
WCLK	Input	Write clock
WE	Input	Write enable
DO	Output	Read data

4.6.3 Paramater Description

Table 4-12 GTP_RAM16X4DP Parameter Description

Parameter Name	**Valid Values**	**Defaults**	**Function Description**
INIT_0	16'h0000~16'hffff	16'h0000	Memory initialization configuration parameters
INIT_1	16'h0000~16'hffff	16'h0000	Memory initialization configuration parameters
INIT_2	16'h0000~16'hffff	16'h0000	Memory initialization configuration parameters
INIT_3	16'h0000~16'hffff	16'h0000	Memory initialization configuration parameters

4.6.4 Functional Description

For the functional description of this GTP, please refer to the distributed RAM mode section of the "***UG030001_Compa Family CPLD Configurable Logic Module (CLM) User Guide***".

4.6.5 Instantiation template

```
GTP_RAM16X4DP    #(
      .INIT_0                 (16'h0000),
      .INIT_1           (16'h0000),
      .INIT_2           (16'h0000),
      .INIT_3           (16'h0000)
)
GTP_RAM16X4DP_inst(
      .DO               (     DO       ),
      .DI               (     DI       ),
      .RADDR                  (  RADDR      ),
      .WADDR                  (     WADDR      ),
      .WCLK                   (     WCLK   ),
      .WE                     (     WE       )
);
```

4.7 GTP_RAM16X1SP

4.7.1 Description of Functionality

GTP_RAM16X1SP is a single-port RAM with a data width of 1 bit and an address depth of 16 bits, and read/write address share one port. The structure block diagram is shown below.

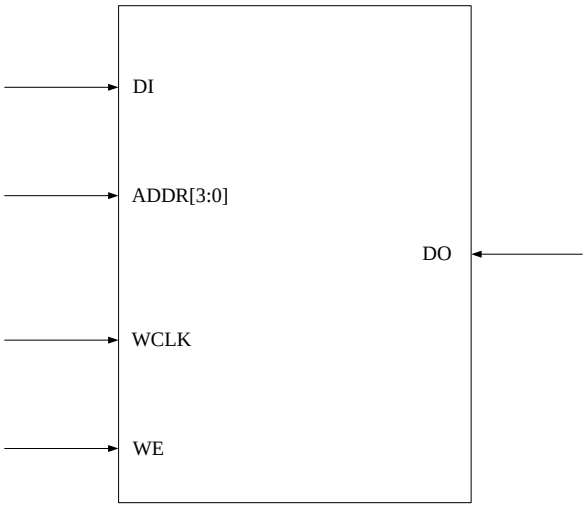

Figure 4-11 GTP_RAM16X1SP Structure Block Diagram

4.7.2 Port Description

Table 4-13 GTP_RAM16X1SP Port Description

Port	Direction	Function Description
DI	Input	Write data
ADDR	Input	Read/write address
WCLK	Input	Write clock
WE	Input	Write enable
DO	Output	Read data

4.7.3 Paramater Description

Table 4-14 GTP_RAM16X1SP Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
INIT	16’h0000~16’hffff	16’h0000	Memory initialization configuration parameters

4.7.4 Functional Description

For the functional description of this GTP, please refer to the distributed RAM mode section of the "***UG030001_Compa Family CPLD Configurable Logic Module (CLM) User Guide***".

4.7.5 Instantiation template

```
GTP_RAM16X1SP#(
    .INIT           (16'h0000)
)
GTP_RAM16X1SP_inst(
    .DO             (  DO     ),
    .DI             (  DI     ),
    .ADDR           (  ADDR   ),
    .WCLK           (  WCLK   ),
    .WE             (  WE     )
);
```

4.8 GTP_RAM16X1DP

4.8.1 Description of Functionality

GTP_RAM16X1DP is a dual-port RAM with a data width of 1 bit and an address depth of 16 bits, and read/write addresses use two different ports. The structure block diagram is shown below.

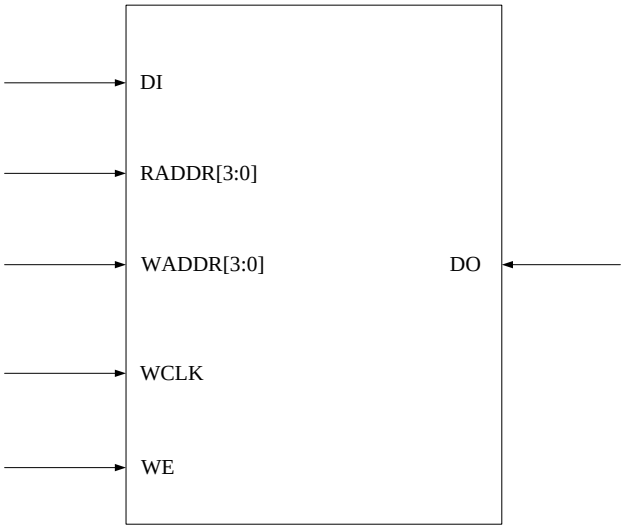

Figure 4-12 GTP_RAM16X1DP Structure Block Diagram

4.8.2 Port Description

Table 4-15 GTP_RAM16X1DP Port Description

Port	Direction	Function Description
DI	Input	Write data
RADDR	Input	Read address
WADDR	Input	Write address
WCLK	Input	Write clock
WE	Input	Write enable
DO	Output	Read data

4.8.3 Paramater Description

Table 4-16 GTP_RAM16X1DP Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
INIT	16'h0000~16'hffff	16'h0000	Memory initialization configuration parameters

4.8.4 Functional Description

For the functional description of this GTP, please refer to the distributed RAM mode section of the

"***UG030001_Compa Family CPLD Configurable Logic Module (CLM) User Guide*** ".

4.8.5 Instantiation template

```
GTP_RAM16X1DP #(
    .INIT           (16'h0000)
)
GTP_RAM16X1DP_inst(
    .DO             (  DO     ),
    .DI             (  DI     ),
    .RADDR              (  RADDR    ),
    .WADDR          (  WADDR    ),
    .WCLK           (  WCLK  ),
    .WE             (  WE     )
);
```

4.9 GTP_DRM9K_E1

4.9.1 Description of Functionality

GTP_DRM9K_E1 supports 9Kbits storage, with various operating modes including True Dual Port (DP) RAM, Simple Dual Port (SDP) RAM, Single Port (SP) RAM and ROM mode. The DRM supports configurable bit width and dual-port mixed bit width in both DP RAM and SDP RAM modes. The structure block diagram is shown in Figure 4-13.

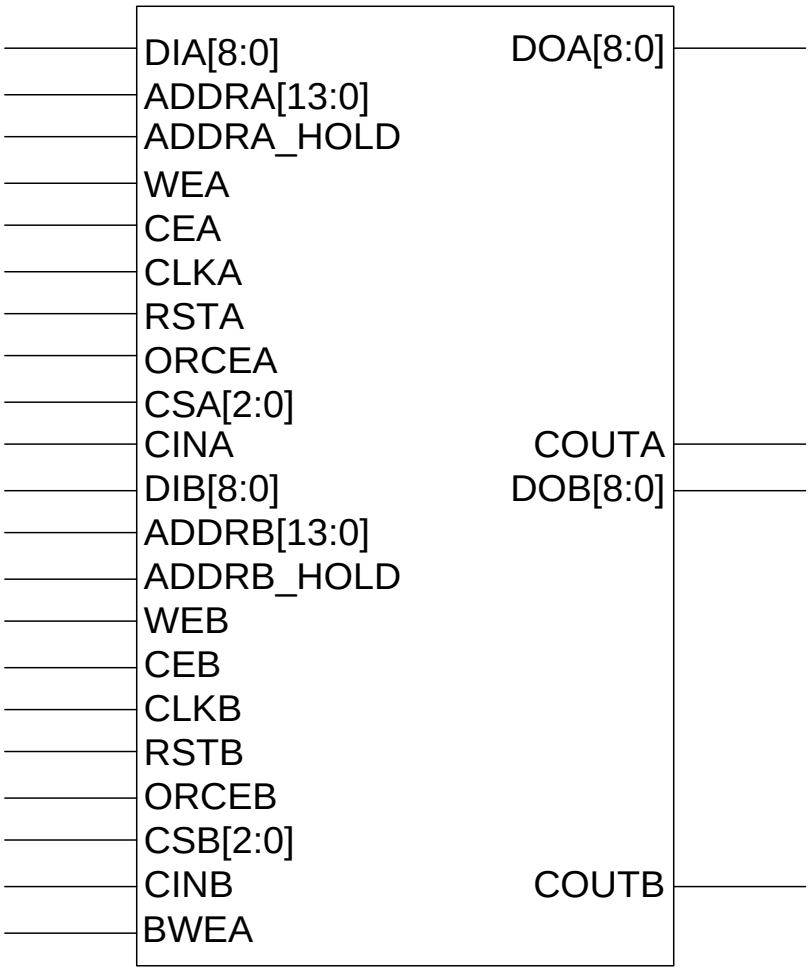

Figure 4-13 GTP_DRM9K_E1 Structure Block Diagram

4.9.2 Port Description

Table 4-17 GTP_DRM9K_E1 Port Description

Port	Direction	Function Description
ADDRA[13:0]	Input	Port A address input. ADDRA[13] is the cascading input for the Port A address among adjacent DRMs; when not cascading, ADDRA[13] is set to 1
ADDRA_HOLD	Input	Port A address input selection
CSA[2:0]	Input	Port A address extension input
DIA[8:0]	Input	Port A data input
WEA	Input	Port A write enable, active high
CLKA	Input	Port A clock
CEA	Input	Port A clock enable, active high
ORCEA	Input	Port A output register enable signal, with 1 enabling the output register, causing one clock delay in the read data output; and 0 keeping the read data unchanged
RSTA	Input	Port A data register reset, active high
DOA[8:0]	Output	Port A data output
ADDRB[13:0]	Input	Port B address input. ADDRB[13] is the cascading input for the Port B address among adjacent DRMs; when not cascading, ADDRB[13] is set to 1

Port	Direction	Function Description
ADDRB_HOLD	Input	Port B address input selection
CSB[2:0]	Input	Port B address extension input
DIB[8:0]	Input	Port B data input
WEB	Input	Port B write enable, active high
CLKB	Input	Port B clock
CEB	Input	Port B clock enable, active high
ORCEB	Input	Port B output register enable signal, with 1 enabling the output register, causing one clock delay in the read data output; and 0 keeping the read data unchanged
RSTB	Input	Port B data register reset, active high
DOB[8:0]	Output	Port B data output
BWEA	Input	Port A byte write enable, active high
CINA	Input	Port A cascade input
CINB	Input	Port B cascade input
COUTA	Output	Port A cascade output
COUTB	Output	Port B cascade output

4.9.3 Paramater Description

Table 4-18 GTP_DRM9K_E1 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
CSA_MASK[2:0]	0 ~ 7	3'b000	Port A address extension control signal
CSB_MASK[2:0]	0 ~ 7	3'b000	Port B address extension control signal
DATA_WIDTH_A	1, 2, 4, 8, 16, 9, 18	9	Data width of Port A
DATA_WIDTH_B	1, 2, 4, 8, 16, 9, 18	9	Data width of Port B
WRITE_MODE_A	"NORMAL_WRITE" "TRANSPARENT_WRITE" "READ_BEFORE_WRITE"	"NORMAL_WRITE"	Port A write mode
WRITE_MODE_B	"NORMAL_WRITE" "TRANSPARENT_WRITE" "READ_BEFORE_WRITE"	"NORMAL_WRITE"	Port B write mode
DOA_REG	0 = Do not enable output register 1 = Enable output register	0	Port A output register
DOB_REG	0 = Do not enable output register 1 = Enable output register	0	Port B output register
RST_TYPE	"SYNC": Synchronous reset "ASYNC": Asynchronous reset	"SYNC"	Reset mode selection
RAM_MODE	"TRUE_DUAL_PORT": DP RAM "SIMPLE_DUAL_PORT": SDP RAM "SINGLE_PORT": SP RAM "ROM":ROM	"TRUE_DUAL_PORT"	RAM mode selection
RAM_CASCADE	"NONE": No hard cascade "UPPER": Serves as a hard cascade data output module	"NONE"	16Kx1 cascade mode

Parameter Name	Valid Values	Defaults	Function Description
	"LOWER": Serves as a hard cascade additional module		
GRS_EN	"FALSE": Global Reset not enabled; "TRUE": Global Reset enabled.	"TRUE"	Global reset enable signal (Internal Chip)
DOA_REG_CLKINV	0 = Clock not inverted 1 = Clock inverted	0	Port A output register clock inversion
DOB_REG_CLKINV	0 = Clock not inverted 1 = Clock inverted	0	Port B output register clock inversion
RSTA_VAL[8:0]	0 = Reset 1 = Set	9'b000000000	Port A output is reset or set
RSTB_VAL[8:0]	0 = Reset 1 = Set	9'b000000000	Port B output is reset or set
INIT_00 INIT_01 INIT_02 … INIT_1F	0 ~2^288-1	288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000	RAM Initialization Configuration Parameters
INIT_FILE	"NONE": No initialization file is specified, the default initialization data will be the value set by the parameter INIT_00~INIT_1F; "XXX": XXX represents the specific initialization file path	"NONE"	Initialization files
BLOCK_X	Depends on the number of cascaded DRMs	0	Data cascade coordinates when RAM is cascaded
BLOCK_Y	Depends on the number of cascaded DRMs	0	Address cascade coordinates when RAM is cascaded
RAM_DATA_WIDTH	Depends on the number of cascaded DRMs	9	Maximum data width as RAM is cascaded
RAM_ADDR_WIDTH	Depends on the number of cascaded DRMs	10	Maximum address width as RAM is cascaded
INIT_FORMAT	"BIN": Binary "HEX": Hexadecimal	"BIN"	Initialization file format

4.9.4 Functional Description

For read and write timing of different modes of GTP_DRM9K_E1, please refer to "***UG030002_Compa Family CPLD Dedicated RAM Module (DRM) User Guide***"

4.9.5 Instantiation template

```
GTP_DRM9K_E1
#(
  .DATA_WIDTH_A       ( 9),
  .DATA_WIDTH_B       ( 9),
.CSA_MASK                 (3'b000),
```

```
.CSB_MASK                (3'b000),
.WRITE_MODE_A        ( "NORMAL_WRITE"),
 .WRITE_MODE_B       ( "NORMAL_WRITE"),
 .DOA_REG            ( 0),
 .DOB_REG            ( 0),
 .RST_TYPE           ("SYNC"),
  .RAM_MODE          ("TRUE_DUAL_PORT"),
.RAM_CASCADE            ("NONE"),
 .GRS_EN             ("TRUE"),
 .DOA_REG_CLKINV       (1'b0),
 .DOB_REG_CLKINV   (1'b0),
.RSTA_VAL                (9'b000000000),
.RSTB_VAL                (9'b000000000),
 .INIT_00
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
 .INIT_01
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_02
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_03
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_04
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_05
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_06
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_07
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_08
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_09
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_0A
```

(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_0B
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_0C
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_0D
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_0E
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_0F
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_10
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_11
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_12
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_13
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_14
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_15
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_16
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_17
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_18
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_19
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_1A
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_1B

```
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_1C
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_1D
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_1E
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_1F
(288'h000000000000000000000000000000000000000000000000000000000000000000000000),
.INIT_FILE ("NONE"),
.BLOCK_X                (0 ),
.BLOCK_Y                (0 ),
.RAM_DATA_WIDTH    ( 9 ),
.RAM_ADDR_WIDTH    ( 10 ),
.INIT_FORMAT            ("BIN")
)
GTP_DRM9K_E1_inst (
      .DOA                  (DOA          ),
      .ADDRA                (ADDRA      ),
      .ADDRA_HOLD     (ADDRA_HOLD),
      .DIA                  (DIA          ),
      .WEA                  (WEA            ),
      .CLKA           (CLKA       ),
      .CEA                  (CEA            ),
      .ORCEA                (ORCEA     ),
      .RSTA           (RSTA           ),
     .CSA                    (CSA      ),
     .CINA             (CINA       ),
     .COUTA                  (COUTA       ),
      .DOB                  (DOB      ),
      .ADDRB                (ADDRB          ),
      .ADDRB_HOLD     (ADDRB_HOLD ),
      .DIB                  (DIB          ),
      .WEB                  (WEB      ),
```

```
    .CLKB       (CLKB       ),
    .CEB        (CEB        ),
    .ORCEB      (ORCEB      ),
    .RSTB       (RSTB       ),
    .CSB        (CSB        ),
    .CINB       (CINB       ),
    .COUTB      (COUTB      ),
    .BWEA       (BWEA       )
);
```

4.10 GTP_FIFO9K

4.10.1 Description of Functionality

GTP_FIFO9K supports 9K bits storage, configurable in data width modes of 8K*1, 4K*2, 2K*4, 1K*9, 512*16, and 512*18. When using GTP_FIFO9K, the DRM is configured to SDP mode, which does not support mixed bit width, nor Byte enable write operation. One set of ports of DRM are used for writing FIFO, and another set is used for reading FIFO; in asynchronous FIFO mode, read and write ports may use different clocks. The structure block diagram is shown below.

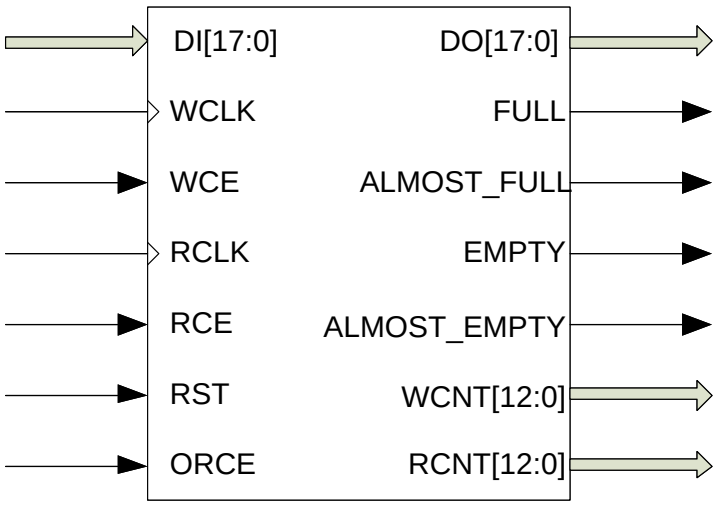

Figure 4-14 GTP_FIFO9K Structure Block Diagram

4.10.2 Port Description

Table 4-19 GTP_FIFO9K Port Description

Port	Input/Output	Description
DI[17:0]	Input	Data write in

Port	Input/Output	Description
WCLK	Input	Write clock signal
RCLK	Input	Read clock signal
WCE	Input	Write enable signal, active high
RCE	Input	Read enable signal, active high
RST	Input	Active-high reset signal
ORCE	Input	Output register enable signal, active high
DO[17:0]	Output	Data read out
EMPTY	Output	Read port empty flag, active high
FULL	Output	Write port full flag, active high
ALMOST_EMPTY	Output	Read port almost empty flag, active high
ALMOST_FULL	Output	Write port almost full flag, active high
WCNT[12:0]	Output	Write pointer
RCNT[12:0]	Output	Read pointer

4.10.3 Paramater Description

Table 4-20 GTP_FIFO9K Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
GRS_EN	"TRUE": Global Reset enabled; "FALSE": Global Reset not enabled.	"TRUE"	Global reset enable signal (Internal Chip)
DATA_WIDTH	1, 2, 4, 8, 9, 16, 18	9	FIFO data width
ALMOST_FULL_OFFSET	DATA_WIDTH= 1: 1~8190 2: 1~4094 4: 1~2046 8/9: 1~1022 16/18: 1~510	13'h0000	When the FIFO is almost full and the difference between the write and read pointers equals to ALMOST_FULL_OFFSET, the almost_full flag is asserted.
ALMOST_EMPTY_OFFSET	DATA_WIDTH= 1: 1~8190 2: 1~4094 4: 1~2046 8/9: 1~1022 16/18: 1~510	13'h0000	When the FIFO is almost empty and the difference between the read and write pointers equals to ALMOST_EMPTY_OFFSET, the almost_empty flag is asserted.
SYNC_FIFO	TRUE: Use synchronous FIFO; FALSE: Use asynchronous FIFO.	"FALSE"	Asynchronous/Synchronous FIFO Selection
USE_EMPTY	1: Read empty flag enabled; 0: Read empty flag not enabled.	0	Enable read empty flag
USE_FULL	1: Write full flag enabled; 0: Write full flag not enabled.	0	Enable write full flag
DO_REG	1: Enable output register; 0: Do not enable output register;	0	Enable output register

4.10.4 Functional Description

For read and write timing of GTP_FIFO9K, please refer to "***UG030002_Compa Family CPLD Dedicated RAM Module (DRM) User Guide***".

4.10.5 Instantiation template

```
GTP_FIFO9K  #(
    .GRS_EN                 (  "TRUE "    ),
    .DATA_WIDTH             (  9          ),
    .DO_REG                 (  0          ),
    .ALMOST_FULL_OFFSET     (  13'h0000),
    .ALMOST_EMPTY_OFFSET    (  13'h0000),
    .USE_EMPTY              (  0          ),
    .USE_FULL           (  0          ),
    .SYNC_FIFO              (  "FALSE"    )
)
GTP_FIFO9K_inst(
    .ALMOST_EMPTY       (  ALMOST_EMPTY),
    .ALMOST_FULL        (  ALMOST_FULL  ),
    .EMPTY              (  EMPTY        ),
    .FULL               (  FULL         ),
    .WCNT               (  WCNT         ),
    .RCNT               (  RCNT         ),
    .DO                 (  DO           ),
    .DI                 (  DI           ),
    .WCLK               (  WCLK         ),
    .RCLK               (  RCLK         ),
    .WCE                (  WCE          ),
    .RCE                (  RCE          ),
    .ORCE               (  ORCE         ),
    .RST                (  RST          )
);
```

Chapter 5 BUF-related GTPs

Compa Family devices do not support HSTL or SSTL standard, thus BUF-related GTPs do not support the parameter "TERM_DDR".

5.1 GTP_INBUF

5.1.1 Description of Functionality

GTP_INBUF is an input buffer. The structure block diagram is shown below.

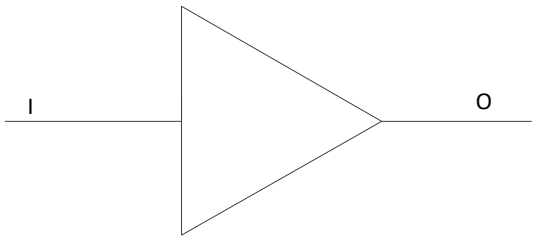

Figure 5-1 GTP_INBUF Structure Block Diagram

5.1.2 Port Description

Table 5-1 GTP_INBUF Port Description

Port	Direction	Function Description
I	Input	Input Signal
O	Output	Output signal

5.1.3 Paramater Description

Table 5-2 GTP_INBUF Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
IOSTANDARD	"LVTTL33""PCI33""LVCMOS33""LVCMOS25" "LVCMOS18""LVCMOS15""LVCMOS12"	"DEFAULT" (LVCMOS33)	I/O Standard

5.1.4 Instantiation template

GTP_INBUF#(

.IOSTANDARD ("DEFAULT"))

GTP_INBUF_inst (

.I (i),

.O (o)

);

5.2 GTP_INBUFDS

5.2.1 Description of Functionality

GTP_INBUFDS is a differential input buffer. The structure block diagram is shown below.

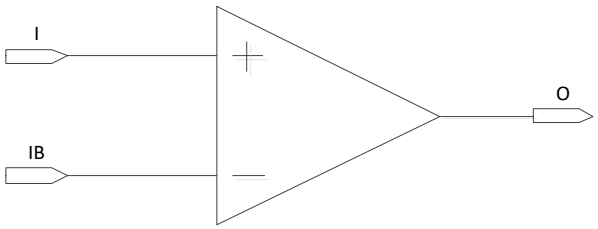

Figure 5-2 GTP_INBUFDS Structure Block Diagram

5.2.2 Port Description

Table 5-3 GTP_INBUFDS Port Description

Port Name	Input/Output	Description
I	Input	P-side differential input
IB	Input	N-side differential input
O	Output	Single-ended output to fabric

5.2.3 Paramater Description

Table 5-4 GTP_INBUFDS Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
IOSTANDARD	"LVDS""LVPECL""RSDS""BLVDS" "LVCMOS33D""LVCMOS25D""DEFAULT"	"DEFAULT" (LVDS)	I/O Standard
TERM_DIFF	"ON","OFF"	"ON"	When in differential input, the built-in terminal resistor is enabled or disabled

5.2.4 Instantiation template

GTP_INBUFDS#(

.IOSTANDARD ("DEFAULT"),

```
.TERM_DIFF      ("ON")
)
  GTP_INBUFDS_inst (
.I          (i),
.IB         (ib ),
.O          (o)
);
```

5.3 GTP_INBUFG

5.3.1 Description of Functionality

GTP_INBUFG is a clock buffer. The structure block diagram is shown below.

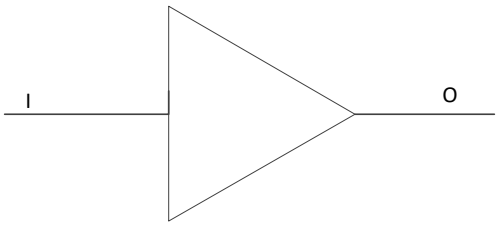

Figure 5-3 GTP_INBUFG Structure Block Diagram

5.3.2 Port Description

Table 5-5 GTP_INBUFG Port Description

Port	Direction	Function Description
I	Input	Input Signal
O	Output	Output signal

5.3.3 Paramater Description

Table 5-6 GTP_INBUFG Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
IOSTANDARD	"LVCMOS33""LVCMOS25" "LVCMOS18""LVCMOS15""LVCMOS12"	"DEFAULT" (LVCMOS33)	I/O Standard

5.3.4 Instantiation template

GTP_INBUFG#(

.IOSTANDARD ("DEFAULT"))

GTP_INBUFG_inst (

.I (i),

.O (o)

);

5.4 GTP_INBUFGDS

5.4.1 Description of Functionality

GTP_INBUFGDS is a differential clock input buffer. The structure block diagram is shown below.

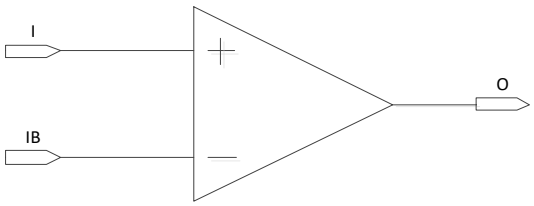

Figure 5-4 GTP_INBUFGDS Structure Block Diagram

5.4.2 Port Description

Table 5-7 GTP_INBUFGDS Port Description

Port	Direction	Function Description
I	Input	Differential P input signals
IB	Input	Differential N input signals
O	Output	Output signal

5.4.3 Paramater Description

Table 5-8 GTP_INBUFGDS Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
IOSTANDARD	"LVDS""LVPECL""RSDS""BLVDS" "LVCMOS33D""LVCMOS25D""DEFAULT"	"DEFAULT" (LVDS)	I/O Standard
TERM_DIFF	"ON", "OFF"	"ON"	When in differential input, the built-in terminal resistor is enabled or disabled

5.4.4 Instantiation template

GTP_INBUFGDS#(

```
    .IOSTANDARD ("DEFAULT"),
    .TERM_DIFF ("ON")
)
 GTP_INBUFGDS_inst (
.I    (i),
.IB  (ib ),
.O   (o)
);
```

5.5 GTP_INBUFE

5.5.1 Description of Functionality

GTP_INBUFE is a single-ended input buffer with an input enable port EN, connecting external ports to fabric. The structure block diagram is shown below.

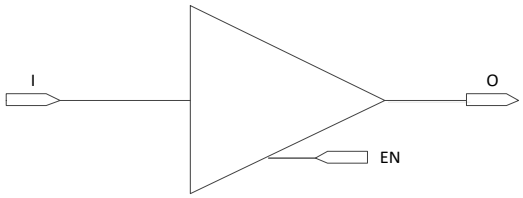

Figure 5-5 GTP_INBUFE Structure Block Diagram

5.5.2 Port Description

Table 5-9 GTP_INBUFE Port Description

Port	Direction	Function Description
I	Input	Single-ended signal input
O	Output	Output from the input buffer to the fabric
EN	Input	Input buffer enable control signal; when set to 0, the input buffer is disabled

5.5.3 Paramater Description

Table 5-10 GTP_INBUFE Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
IOSTANDARD	"LVTTL33""PCI33""LVCMOS33""LVCMOS25" "LVCMOS18""LVCMOS15""LVCMOS12"	"DEFAULT" (LVCMOS33)	Input I/O standard

5.5.4 Instantiation template

```
GTP_INBUFE#(
    .IOSTANDARD ("DEFAULT"))
  GTP_INBUFE_inst (
.I    (i    ),
.EN (en ),
.O   (o    )
);
```

5.6 GTP_INBUFEDS

5.6.1 Description of Functionality

GTP_INBUFEDS is a differential input buffer with an input enable port EN, connecting external ports to fabric. The structure block diagram is shown below.

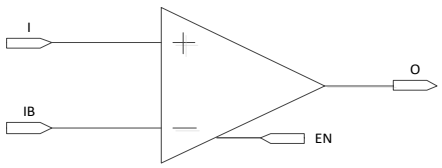

Figure 5-6 GTP_INBUFEDS Structure Block Diagram

5.6.2 Port Description

Table 5-11 GTP_INBUFEDS Port Description

Port	Direction	Function Description
I	Input	P-side differential input
IB	Input	N-side differential input
O	Output	Single-ended output to fabric
EN	Input	Enable signal, 0 disables the buffer, and 1 enables the buffer

5.6.3 Paramater Description

Table 5-12 GTP_INBUFEDS Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
IOSTANDARD	"LVDS""LVPECL""RSDS""BLVDS" "LVCMOS33D""LVCMOS25D""DEFAULT"	"DEFAULT"(LVDS)	Input I/O standard
TERM_DIFF	"ON", "OFF"	"ON"	Internal termination resistor enabled or

Parameter Name	Valid Values	Defaults	Function Description
			disabled in differential input

5.6.4 Instantiation template

```
GTP_INBUFEDS#(
    .IOSTANDARD ("DEFAULT"),
    .TERM_DIFF     ("ON")
)
 GTP_INBUFEDS_inst (
.I    (I    ),
.IB  (ib ),
.EN (en),
.O   (o ) );
```

5.7 GTP_IOBUF

5.7.1 Description of Functionality

GTP_IOBUF is a bidirectional single-ended buffer, connecting external bidirectional ports to fabric. The structure block diagram is shown below.

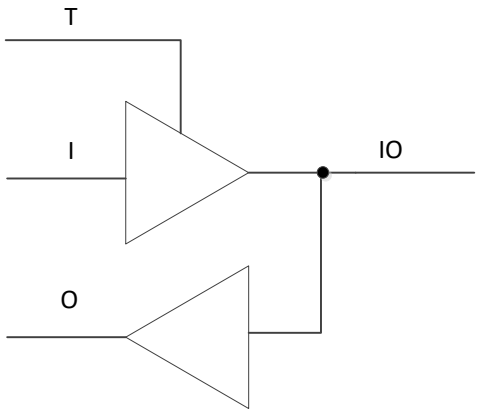

Figure 5-7 GTP_IOBUF Structure Block Diagram

5.7.2 Port Description

Table 5-13 GTP_IOBUF Port Description

Port	Direction	Function Description

Port	Direction	Function Description
I	Input	Input Signal
T	Input	Tri-state enable; when T=1, IO is an input; when T=0, IO is an output
O	Output	Output signal
IO	Bidirectional	Bidirectional signal (in or out)

5.7.3 Paramater Description

Table 5-14 GTP_IOBUF Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
IOSTANDARD	"LVTTL33""PCI33""LVCMOS33""LVCMOS25" "LVCMOS18""LVCMOS15""LVCMOS12"	"DEFAULT" (LVCMOS33)	I/O Standard
SLEW_RATE	"FAST", "SLOW"	"SLOW"	Slew rate
DRIVE_STRENGTH	2, 4, 6, 8, 12, 16	8	Output Drive

5.7.4 Instantiation template

```
GTP_IOBUF#(
.IOSTANDARD ("DEFAULT"),
.SLEW_RATE ("SLOW"),
.DRIVE_STRENGTH ("8"))
  GTP_IOBUF_inst (
.I    (i),
.T    (t),
.IO  (io ),
.O    (o)
);
```

5.8 GTP_IOBUFCO

5.8.1 Description of Functionality

GTP_IOBUFCO is a bidirectional pseudo-differential buffer, only supporting pseudo-differential standards. The structure block diagram is shown below.

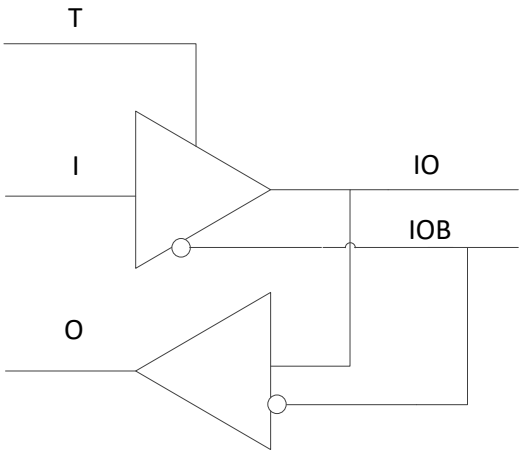

Figure 5-8 GTP_IOBUFCO Structure Block Diagram

5.8.2 Port Description

Table 5-15 GTP_IOBUFCO Port Description

Port	Direction	Function Description
I	Input	Input Signal
T	Input	Tri-state enable; when T=1, IO and IOB act as differential inputs; when T=0, IO and IOB act as pseudo-differential outputs
IO	Bidirectional	Differential P side input or output
IOB	Bidirectional	Differential Q side input or output
O	Output	Output signal

5.8.3 Paramater Description

Table 5-16 GTP_IOBUFCO Parameter Description

Parameter	Valid Values	Defaults	Function Description
IOSTANDARD	"LVCMOS33D","LVCMOS25D", "LVPECL","RSDS","LVDS25E", "BLVDS", "MLVDS", "DEFAULT"	"DEFAULT" (LVCMOS33D)	I/O Standard
TERM_DDR	"ON", "OFF"	"ON"	For HSTL or SSTL standard inputs, enable or disable internal terminal resistors

5.8.4 Instantiation template

```
GTP_IOBUFCO#(
   .IOSTANDARD ("DEFAULT")
   )
  GTP_IOBUFCO_inst(
.I    (i),
```

.T (t),

.IO (io),

.IOB(iob),

.O (o));

5.9 GTP_OUTBUF Usage Instructions

5.9.1 Description of Functionality

GTP_OUTBUF is an output buffer. The structure block diagram is shown below.

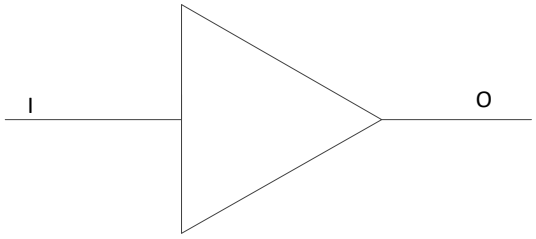

Figure 5-9 GTP_OUTBUF Structure Block Diagram

5.9.2 Port Description

Table 5-17 GTP_OUTBUF Port Description

Port	Direction	Function Description
I	Input	Input Signal
O	Output	Output signal

5.9.3 Paramater Description

Table 5-18 GTP_OUTBUF Parameter Description

Parameter	Valid Values	Defaults	Function Description
IOSTANDARD	"LVTTL33""PCI33""LVCMOS33""LVCMOS25" "LVCMOS18""LVCMOS15""LVCMOS12"	"DEFAULT" (LVCMOS33)	I/O Standard
SLEW_RATE	"FAST", "SLOW"	"SLOW"	Slew rate
DRIVE_STRENGTH	2, 4, 6, 8, 12, 16	8	Output Drive

5.9.4 Instantiation template

GTP_OUTBUF#(

.IOSTANDARD ("DEFAULT"),

```
.SLEW_RATE    ("SLOW"),
.DRIVE_STRENGTH (8)
)
  GTP_OUTBUF_inst (
.I    (i),
.O   (o)
);
```

5.10 GTP_OUTBUFCO

5.10.1 Description of Functionality

GTP_OUTBUFCO is a pseudo-differential output buffer. The structure block diagram is shown below.

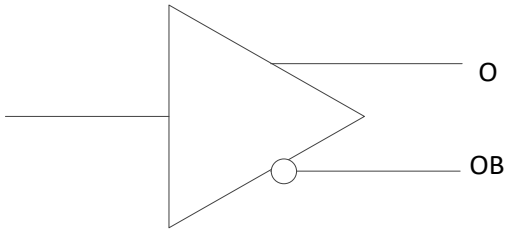

Figure 5-10 GTP_OUTBUFCO Structure Block Diagram

5.10.2 Port Description

Table 5-19 GTP_OUTBUFCO Port Description

Port	Direction	Function Description
I	Input	Input Signal
OB	Output	N-side for pseudo-differential output signal
O	Output	P-side for pseudo-differential output signal

5.10.3 Paramater Description

Table 5-20 GTP_OUTBUFCO Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
IOSTANDARD	"LVPECL""BLVDS""RSDS""MLVDS" "LVCMOS33D""LVCMOS25D""LVDS25E""DEFAULT"	"DEFAULT" (LVCMOS33D)	I/O Standard

5.10.4 Instantiation template

```
GTP_OUTBUFCO#(
```

```
   .IOSTANDARD ("DEFAULT")
)
 GTP_OUTBUFCO_inst (
.I    (i),
.OB (ob ),
.O   (o) );
```

5.11 GTP_OUTBUFDS

5.11.1 Description of Functionality

GTP_OUTBUFDS is a true differential output buffer, with the structure block diagram as shown below.

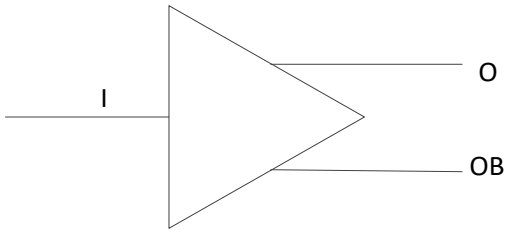

Figure 5-11 GTP_OUTBUFDS Structure Block Diagram

5.11.2 Port Description

Table 5-21 GTP_OUTBUFDS Port Description

Port	Direction	Function Description
I	Input	Input Signal
OB	Output	N-side for true differential output signal
O	Output	P-side for true differential output signal

5.11.3 Paramater Description

Table 5-22 GTP_OUTBUFDS Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
IOSTANDARD	"LVDS"	"DEFAULT"(LVDS)	I/O Standard

5.11.4 Instantiation template

GTP_OUTBUFDS#(

```
    .IOSTANDARD ("DEFAULT")
)
 GTP_OUTBUFDS_inst (
.I      (i ),
.OB    (ob),
.O     (o)
);
```

5.12 GTP_OUTBUFT

5.12.1 Description of Functionality

GTP_OUTBUFT is a tri-state output buffer. The structure block diagram is shown below.

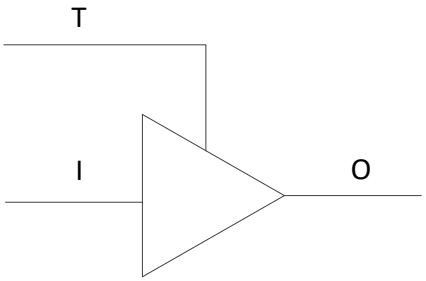

Figure 5-12 GTP_OUTBUFT Structure Block Diagram

5.12.2 Port Description

Table 5-23 GTP_OUTBUFT Port Description

Port	Direction	Function Description
I	Input	Input Signal
O	Output	Output signal
T	Input	Tri-state enable. T=1 sets the output port to tri-state; T=0 drives the input signal I to the output port

5.12.3 Paramater Description

Table 5-24 GTP_OUTBUFT Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
IOSTANDARD	"LVTTL33""PCI33""LVCMOS33""LVCMOS25" "LVCMOS18""LVCMOS15""LVCMOS12"	"DEFAULT" (LVCMOS33)	I/O Standard
SLEW_RATE	"FAST", "SLOW"	"SLOW"	Slew rate
DRIVE_STRENGTH	2, 4, 6, 8, 12, 16	8	Output Drive

5.12.4 Instantiation template

```
GTP_OUTBUFT#(
.IOSTANDARD ("DEFAULT"),
.SLEW_RATE ("SLOW"),
.DRIVE_STRENGTH ("8")
)
  GTP_OUTBUFT_inst (
.I    (i),
.O    (o),
.T    (t)
);
```

5.13 GTP_OUTBUFTCO

5.13.1 Description of Functionality

GTP_OUTBUFTCO is a tri-state output pseudo-differential buffer. The structure block diagram is shown below.

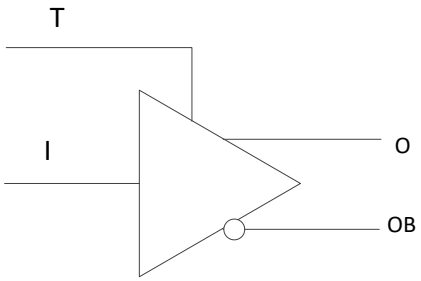

Figure 5-13 GTP_OUTBUFTCO Structure Block Diagram

5.13.2 Port Description

Table 5-25 GTP_OUTBUFTCO Port Description

Port	Direction	Function Description
I	Input	Input Signal
OB	Output	N-side for pseudo-differential output signal
O	Output	P-side for pseudo-differential output signal
T	Input	Tri-state enable. T=1 sets the output port to tri-state; T=0 drives the input signal I to the output port

5.13.3 Paramater Description

Table 5-26 GTP_OUTBUFTCO Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
IOSTANDARD	"LVPECL""RSDS""BLVDS""MLVDS" "LVCMOS33D""LVCMOS25D""LVDS25E""DEFAULT"	"DEFAULT" (LVCMOS33D)	I/O Standard

5.13.4 Instantiation template

```
GTP_OUTBUFTCO#(
    .IOSTANDARD ("DEFAULT")
)
 GTP_OUTBUFTCO_inst (
.I    (i),
.T    (t),
.OB (ob ),
.O    (o)
);
```

5.14 GTP_OUTBUFTDS

5.14.1 Description of Functionality

GTP_OUTBUFTDS is a tri-state output true differential buffer. The structure block diagram is shown below.

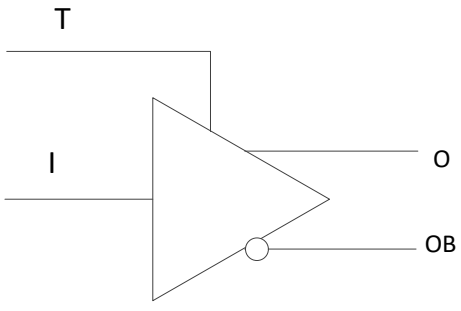

Figure 5-14 GTP_OUTBUFTDS Structure Block Diagram

5.14.2 Port Description

Table 5-27 GTP_OUTBUFTDS Port Description

Port	Direction	Function Description
I	Input	Input Signal
OB	Output	Differential N side output signals
O	Output	Differential P side output signals
T	Input	Tri-state enable. T=1 sets the output port to tri-state; T=0 drives the input signal I to the output port

5.14.3 Paramater Description

Table 5-28 GTP_OUTBUFTDS Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
IOSTANDARD	"LVDS", "DEFAULT"	"DEFAULT"(LVDS)	I/O Standard

5.14.4 Instantiation template

```
GTP_OUTBUFTDS#(
    .IOSTANDARD ("DEFAULT")
)
  GTP_ OUTBUFTDS_inst (
.I    (i),
.T    (t),
.OB (ob ),
.O    (o)
);
```

5.15 GTP_IOBUF_RX_MIPI

5.15.1 Description of Functionality

GTP_IOBUF_RX_MIPI supports MIPI DPHY high-speed input, and single-ended input/output in low power mode (LP). The structure block diagram is shown below.

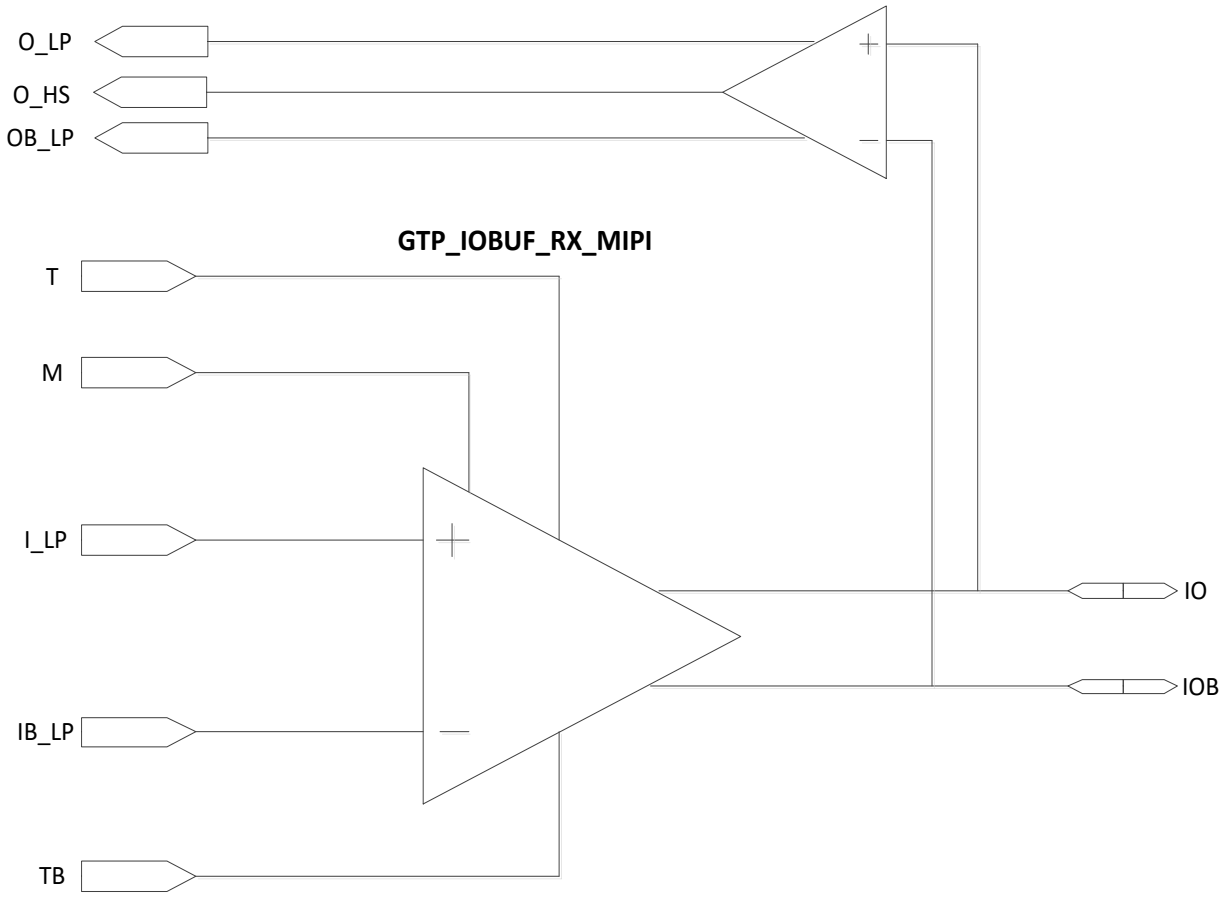

Figure 5-15 GTP_IOBUF_RX_MIPI Structure Block Diagram

5.15.2 Port Description

Table 5-29 GTP_IOBUF_RX_MIPI Port Description

Port	Direction	Function Description
I_LP	Input	The input signal for the single-ended output buffer from "fabric" in LP mode
IB_LP	Input	The input signal for the single-ended output buffer from "fabric" in LP mode
M	Input	Mode selection signal. 1: Differential input in HS mode; 0: Signle-ended bidirectional in LP mode
T	Input	Single-ended output enable signal; when it is 0, IO serves as output, and when it is 1, IO serves as input
TB	Input	Single-ended output enable signal; when it is 0, IOB serves as output, and when it is 1, IOB serves as input
O_HS	Output	Differential output (HS) to fabric
O_LP	Output	Single-ended output (LP)
OB_LP	Output	Single-ended output (LP)
IO	Bidirectional	P side differential input (HS mode), or single-ended bidirectional (LP mode)
IOB	Bi-Directional	N side differential input (HS mode), or single-ended bidirectional (LP mode)

5.15.3 Paramater Description

Table 5-30 GTP_IOBUF_RX_MIPI Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
IOSTANDARD	"MIPI", "DEFAULT"	"DEFAULT"(MIPI)	I/O Standard VCCIO=1.2V
DRIVE_STRENGTH	"2", "6"	"6"	Drive current strength
SLEW_RATE	"SLOW", "FAST"	"SLOW"	Slew rate
TERM_DIFF	"ON", "OFF"	"ON"	Internal terminal resistor enabled or disabled

5.15.4 Instantiation template

```
GTP_IOBUF_RX_MIPI #
(
.IOSTANDARD          ( "DEFAULT" ),
.TERM_DIFF           ( "ON" ),
.DRIVE_STRENGTH ("6"),
.SLEW_RATE           ("SLOW")
)
GTP_IOBUF_RX_MIPI_inst (
.O_LP    (O_LP),
.OB_LP (OB_LP),
.O_HS    (O_HS),
.IO       (IO),
.IOB      (IOB),
.I_LP    (I_LP),
.IB_LP    (IB_LP),
.T          (T),
.TB      (TB),
.M       (M)
);
```

5.16 GTP_IOBUF_TX_MIPI

5.16.1 Description of Functionality

GTP_IOBUF_TX_MIPI supports MIPI DPHY tri-state output, including input/output in low-power mode (LP) and differential output in high-speed (HS) mode, with both modes being switchable according to practical application. The structure block diagram is shown below.

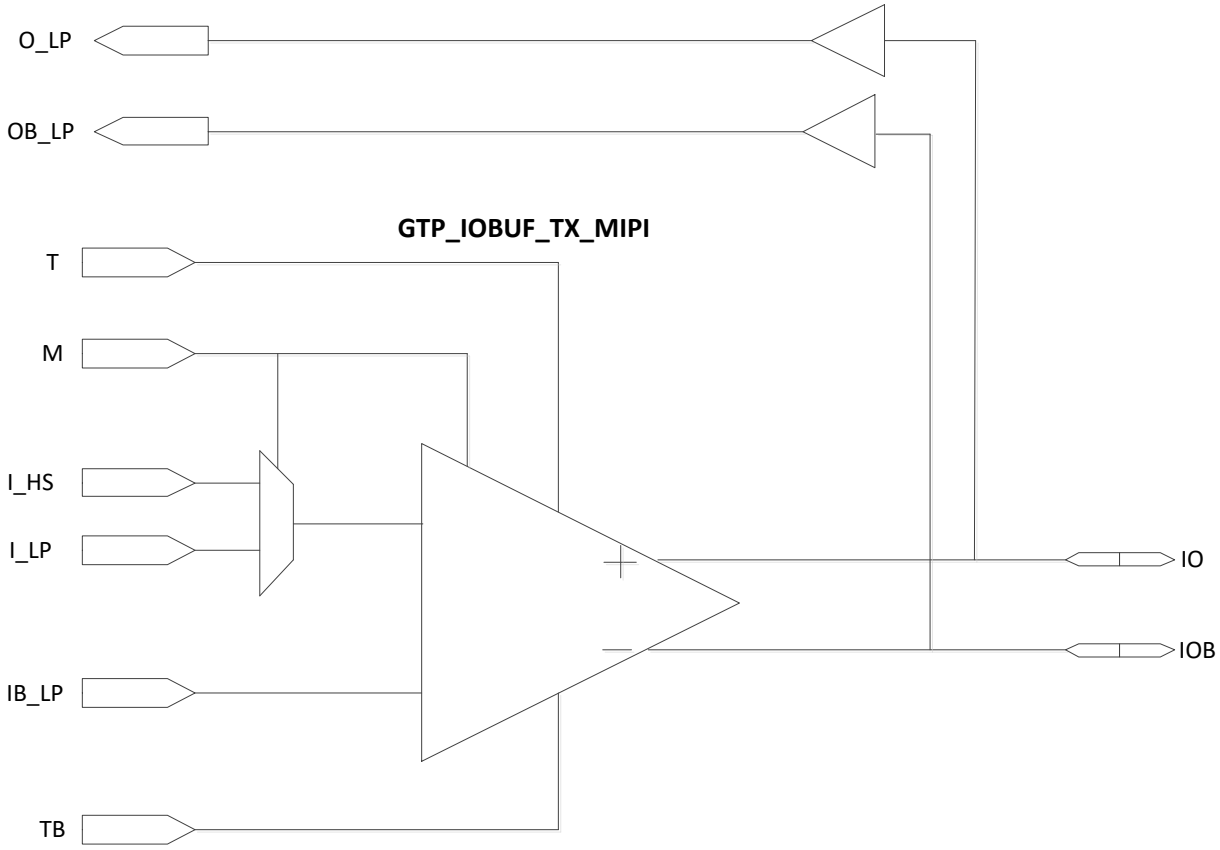

Figure 5-16 GTP_IOBUF_TX_MIPI Structure Block Diagram

5.16.2 Port Description

Table 5-31 GTP_IOBUF_TX_MIPI Port Description

Port	Direction	Function Description
I_HS	Input	The input signal for the HS differential output buffer from IOL
I_LP	Input	The input signal for the single-ended output buffer from IOL in LP mode
IB_LP	Input	The input signal for the single-ended output buffer from IOL in LP mode
M	Input	Mode selection signal. 1: HS mode, differential input; 0: LP mode, single-ended input and output
T	Input	Differential and single-ended output enable signal
TB	Input	Single-ended output enable signal
O_LP	Output	Single-ended (LP) input to IOL
OB_LP	Output	Single-ended (LP) input to IOL
IO	Bi-Directional	P-side differential output or input
IOB	Bi-Directional	N-side differential output or input

5.16.3 Paramater Description

Table 5-32 GTP_IOBUF_TX_MIPI Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
IOSTANDARD	"MIPI","DEFAULT"	"DEFAULT"(MIPI)	I/O Standard VCCIO=1.2V
DRIVE_STRENGTH	"2", "6"	"6"	Drive current strength
SLEW_RATE	"SLOW", "FAST"	"SLOW"	Slew rate
TERM_DIFF	"ON", "OFF"	"ON"	Internal terminal resistor enabled or disabled

5.16.4 Instantiation template

```
GTP_IOBUF_TX_MIPI #
(
.IOSTANDARD         ( "DEFAULT" ),
.DRIVE_STRENGTH ( "6" ),
.SLEW_RATE          ( "SLOW" ),
.TERM_DIFF          ( "ON" )
)
GTP_IOBUF_TX_MIPI_inst
(
.O_LP     (O_LP ),
.OB_LP    (OB_LP ),
.IO         ( IO ),
.IOB        ( IOB ),
.I_HS       ( I_HS ),
.I_LP       ( I_LP ),
.IB_LP     ( IB_LP),
.T          ( T ),
.TB         ( TB ),
.M          ( M )
);
```

Chapter 6 IO Logic-related GTPs

6.1 GTP_ISERDES_E1

6.1.1 Description of Functionality

GTP_ISERDES_E1 is a data deserializer that performs double-edge data sampling on both rising and falling edges of the clock and supports 1:4, 1:7, 1:8 gearing logic. The structure block diagram is shown below.

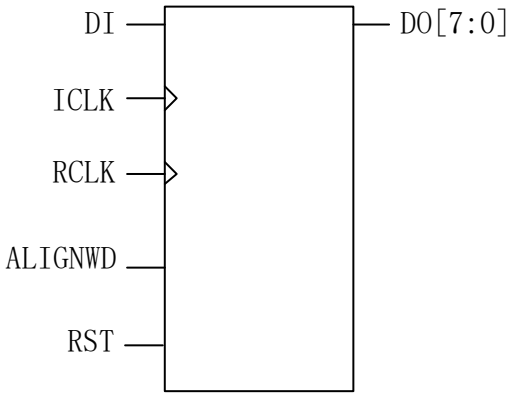

Figure 6-1 GTP_ISERDES_E1 Structure Block Diagram

6.1.2 Port Description

Table 6-1 GTP_ISERDES_E1 Port Description

Port	Direction	Width	Function Description
DO	Output	8	In "IDES4" mode, DO [7:4] is the deserialized data for DIA, and DO [3:0] is the deserialized data for DIC In "IDES8" mode, DO [7:0] is the deserialized data for DIA In "IDES7" mode, DO [6:0] is the deserialized data for DIA
DI	Input	1	Serial input data
ICLK	Input	1	Input clock of Serial data
RCLK	Input	1	Deserialization clock generated byCLKDIVOUT of GTP_IOCLKDIV_E1
ALIGNWD	Input	1	Word alignment request signal, active high
RST	Input	1	Reset signal, active high

6.1.3 Paramater Description

Table 6-2 GTP_ISERDES_E1 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
GRS_EN	"TRUE","FALSE"	"TRUE"	Global reset enable; "TRUE" indicates valid
ISERDES_MODE	"IDES4","IDES8", "IDES7"	"IDES4"	Deserialization mode

6.1.4 Functional Description

For GTP_ISERDES_E1 timing instructions, please refer to "***UG030005 Compa Family CPLD Input/Output Interface (IO) User Guide***".

6.1.5 Instantiation template

```
GTP_ISERDES_E1 #
(
.ISERDES_MODE          ("IDES4"),    //"IDES4","IDES8","IDES7"
.GRS_EN                ("TRUE" )     //"TRUE","FALSE"
) GTP_ISERDES_E1_inst    (
.DI                     ( di       ),
.ICLK                   ( iclk     ),
.RCLK                   ( rclk     ),
.ALIGNWD                ( alignwd),
.RST                    ( rst      ),
.DO                     ( do       )
);
```

6.2 GTP_OSERDES_E1

6.2.1 Description of Functionality

GTP_OSERDES_E1 is a serializer that performs double-edge data sampling on both rising and falling edges of the clock and supports 4:1, 7:1, 8:1 gearing logic. The structure block diagram is shown below.

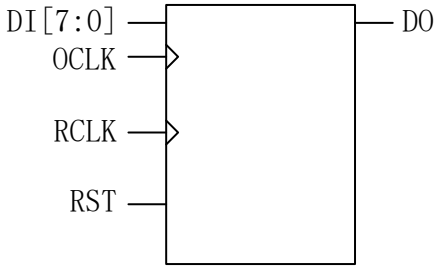

Figure 6-2 GTP_OSERDES_E1 Structure Block Diagram

6.2.2 Port Description

Table 6-3 GTP_OSERDES_E1 Port Description

Port	Direction	Width	Function Description
DI	Input	8	Parallel input data In "OSER4" mode, DI[3:0] are valid In "OSER8" mode, DI[7:0] are valid In "OSER7" mode, DI[6:0] are valid
DO	Output	1	In "OSER4" mode, DOA is the serial output for DI[3:0] In "OSER8" mode, DOA is the serial output for DI[7:0] In "OSER7" mode, DOA is the serial output for DI[6:0]
OCLK	Input	1	Clock of serial data output
RCLK	Input	1	Input clock of parallel data
RST	Input	1	Reset signal, active high

6.2.3 Paramater Description

Table 6-4 GTP_OSERDES_E1 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
GRS_EN	"TRUE","FALSE"	"TRUE"	Global reset enable; "TRUE" indicates valid
OSERDES_MODE	"OSER4","OSER8", "OSER7"	"OSER4"	Serialization mode

6.2.4 Functional Description

For GTP_OSERDES_E1 timing instructions, please refer to "***UG030005 Compa Family CPLD Input/Output Interface (IO) User Guide***".

6.2.5 Instantiation template

```
GTP_OSERDES _E1#
(
.OSERDES_MODE        ("OSER4"),    //"OSER4","OSER8","OSER7"
```

```
.GRS_EN                ("TRUE" )     //"TRUE","FALSE"
) GTP_OSERDES _E1_inst (
.DI                    ( di        ),
.OCLK                  ( oclk      ),
.RCLK                  ( rclk      ),
.RST                   ( rst       ),
.DO                    ( do        )
);
```

6.3 GTP_IDDR

6.3.1 Description of Functionality

GTP_IDDR is a data deserializer that supports 1:2 and performs double-edge data sampling on both rising and falling edges of the clock. The structure block diagram is shown below.

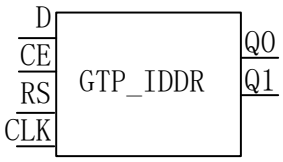

Figure 6-3 GTP_IDDR Structure Block Diagram

6.3.2 Port Description

Table 6-5 GTP_IDDR Port Description

Port	Direction	Width	Function Description
D	Input	1	Input data port
CE	Input	1	Clock enable signal, active high
RS	Input	1	Set/reset signal, active high
CLK	Input	1	System clock
Q0	Output	1	Deserializer data output
Q1	Output	1	Deserializer data output

6.3.3 Paramater Description

Table 6-6 GTP_IDDR Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
GRS_EN	"TRUE","FALSE"	"TRUE"	Global reset enable; "TRUE" indicates valid
RS_TYPE	"SYNC_SET" , "ASYNC_SET" , "SYNC_RESET" , "ASYNC_RESET"	"ASYNC_SET"	Reset/Set mode select

6.3.4 Functional Description

For GTP_IDDR timing instructions, please refer to "***UG030005 Compa Family CPLD Input/Output Interface (IO) User Guide***".

6.3.5 Instantiation template

```
GTP_IDDR #
(
.GRS_EN        ("TRUE"        ),    //"TRUE","FALSE"
.RS_TYPE                                                    ("ASYNC_SET")
//"SYNC_SET","ASYNC_SET","SYNC_RESET","ASYNC_RESET"
) GTP_IDDR_inst (
.D             ( d             ),
.CE            ( ce            ),
.RS            ( rs            ),
.CLK           ( clk           ),
.Q0            ( q0            ),
.Q1            ( q1            )
);
```

6.4 GTP_ODDR

6.4.1 Description of Functionality

The GTP_ODDR is a serializer, which performs double edge data sampling on both rising and falling edges of the clock and supports 2:1 rate. Its structure block diagram is shown below.

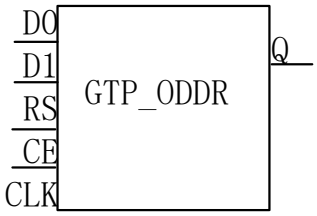

Figure 6-4 GTP_ODDR Structure Block Diagram

6.4.2 Port Description

Table 6-7 GTP_ODDR Port Description

Port	Direction	Width	Function Description
D0	Input	1	Input data port
D1	Input	1	Input data port
CE	Input	1	Clock enable signal, active high
RS	Input	1	Set/reset signal, active high
CLK	Input	1	System clock
Q	Output	1	Serial data output

6.4.3 Paramater Description

Table 6-8 GTP_ODDR Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
GRS_EN	"TRUE","FALSE"	"TRUE"	Global reset enable; "TRUE" indicates valid
RS_TYPE	"SYNC_SET" , "ASYNC_SET" , "SYNC_RESET" , "ASYNC_RESET"	"ASYNC_SET"	Reset/Set mode select

6.4.4 Functional Description

For GTP_ODDR timing instructions, please refer to "***UG030005 Compa Family CPLD Input/Output Interface (IO) User Guide***".

6.4.5 Instantiation template

```
GTP_ODDR #
(
  .GRS_EN        ("TRUE"          ),    //"TRUE","FALSE"
  .RS_TYPE                                                    ("ASYNC_SET"              )
```

```
//"SYNC_SET","ASYNC_SET","SYNC_RESET","ASYNC_RESET"
) GTP_ODDR_inst (
.D0             ( d0              ),
.D1             ( d1              ),
.CE             ( ce              ),
.RS             ( rs              ),
.CLK            ( clk             ),
.Q              ( q               )
);
```

6.5 GTP_IODELAY_E1

6.5.1 Description of Functionality

The GTP_IODELAY_E1 is an I/O delay unit that supports dynamic or static delay control, with a maximum delay of 31 steps. The structure block diagram is shown below.

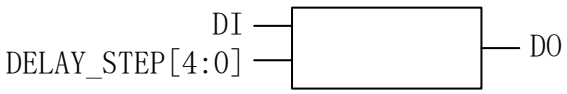

Figure 6-5 GTP_IODELAY_E1 Structure Block Diagram

6.5.2 Port Description

Table 6-9 GTP_IODELAY_E1 Port Description

Port	Direction	Width	Function Description
DI	Input	1	Data input
DELAY_STEP	Input	5	Dynamic delay control
DO	Output	1	Data output

6.5.3 Paramater Description

Table 6-10 GTP_IODELAY_E1 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
DELAY_UNIT	"110ps", "58ps"	"110ps"	Used to select the size of each delay step; the Compa device only supports "110ps"
DELAY_STEP_VALUE	5'h0 ~ 5'h1F	5'h0	Static delay control
DELAY_STEP_SEL	"PARAMETER" "PORT"	"PARAMETER"	Selection of the delay control signal source: "PARAMETER" indicates static configuration controlled by parameter DELAY_STEP_VALUE; "PORT" indicates dynamic input from the port DELAY_STEP

6.5.4 Instantiation template

```
GTP_IODELAY_E1 #
(
.DELAY_STEP_VALUE ( 5`h0                ),      // 5`h0 ~ 5`h1F
.DELAY_STEP_SEL     ("PARAMETER")     //"PARAMETER", "PORT"
) GTP_IODELAY_E1_inst (
.DI                         ( di              ),
.DELAY_STEP           ( delay_step      ),
.DO                         ( do              )
);
```

Chapter 7 Clock-Related GTPs

7.1 GTP_CLKBUFG

7.1.1 Description of Functionality

The GTP_CLKBUFG offers a simple clock buffer function; global clock network can be implemented by instantiating the GTP_CLKBUFG. The structure block diagram is shown below.

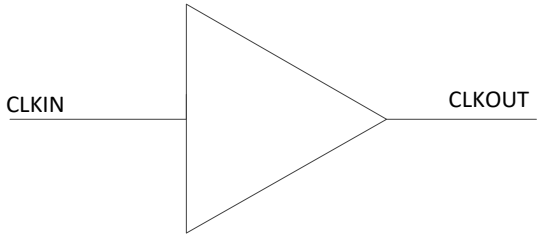

Figure 7-1 GTP_CLKBUFG Structure Block Diagram

7.1.2 Port Description

Table 7-1 GTP_CLKBUFG Port Description

Port	Direction	Function Description
CLKIN	Input	Input Clock
CLKOUT	Output	Output clock

7.1.3 Instantiation template

```
GTP_CLKBUFG CLKBUFG_inst (
    .CLKOUT          (CLKOUT),
    .CLKIN       (CLKIN )
);
```

7.2 GTP_BUFGS

7.2.1 Description of Functionality

GTP_BUFGS provides global signal network, allowing signals reaching all areas of the chip evenly. The structure block diagram is shown below.

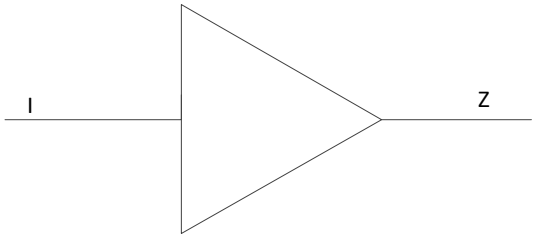

Figure 7-2 GTP_BUFGS Structure Block Diagram

7.2.2 Port Description

Table 7-2 GTP_BUFGS Port Description

Port	**Direction**	**Function Description**
I	Input	Global signal input
Z	Output	Global signal output

7.2.3 Functional Description

The input signals for GTP_BUFGS can be either reset signals or clock signals. Users can resolve the shortage of global clock resources by instantiating the GTP_BUFGS.

7.2.4 Instantiation template

```
GTP_BUFGS BUFGS_inst (
    .I          (I),
    .Z          (Z )
);
```

7.3 GTP_CLKBUFGCE

7.3.1 Description of Functionality

The GTP_CLKBUFGCE is a clock buffer with an enable port. The structure block diagram is shown below.

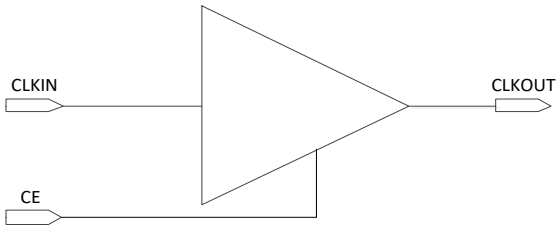

Figure 7-3 GTP_CLKBUFGCE Structure Block Diagram

7.3.2 Port Description

Table 7-3 GTP_CLKBUFGCE Port Description

Port	Direction	Function Description
CLKIN	Input	Input Clock
CE	Input	When CE=1'b1, CLKOUT=CLKIN; when CE=1'b0, CLKOUT outputs DEFAULT_VALUE
CLKOUT	Output	Output clock

7.3.3 Paramater Description

Table 7-4 GTP_CLKBUFGCE Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
DEFAULT_VALUE	1'b0, 1'b1	1'b0	When DEFAULT_VALUE=1'b0 and CE=1'b0, CLKOUT outputs 1'b0; For Compa device, this parameter can only be configured as 0
SIM_DEVICE	"TITAN","LOGOS", "COMPACT","LOGOS2", "TITAN2","TITAN3"	"TITAN"	Device family selection

7.3.4 Functional Description

For a detailed functional description of GTP_CLKBUFGCE, please refer to "***UG030003_Compa Family CPLD Clock Resources (Clock & PLL) User Guide***".

7.3.5 Instantiation template

```
GTP_CLKBUFGCE
#(.DEFAULT_VALUE        (1'b0              ),
   .SIM_DEVICE           ("COMPACT")
) GTP_CLKBUFGCE_inst    (
      .CLKIN             (CLKIN      ),
```

```
    .CE                 ( CE            ),
    .CLKOUT             (CLKOUT         )
);
```

7.4 GTP_CLKBUFGMUX

7.4.1 Description of Functionality

GTP_CLKBUFGMUX can be used for dynamic switching between two global clock inputs. GTP_CLKBUFGMUX provides a glitchless switch triggered by the falling edge of the clock (corresponding to TRIGGER_MODE="NEGEDGE"). It is important to note that both clock sources must be active. Otherwise, an abnormal CLKOUT output will occur during switching. The structure block diagram is shown below.

Figure 7-4 GTP_CLKBUFGMUX Structure Block Diagram

7.4.2 Port Description

Table 7-5 GTP_CLKBUFGMUX Port Description

Port	Direction	Function Description
CLKIN0	Input	Input clock CLKIN0
CLKIN1	Input	Input clock CLKIN1
SEL	Input	Clock select signal. Select CLKIN0 when it is 1'b0; select CLKIN1 when it is 1'b1;
CLKOUT	Output	Output clock

7.4.3 Paramater Description

Table 7-6 GTP_CLKBUFGMUX Parameter Description

Parameter Name	Valid Values	Defaults	Functional Description
TRIGGER_MODE	"NORMAL", "NEGEDGE"	"NORMAL"	Mode selection. Compa device only support "NEGEDGE". "NEGEDGE": In this mode, input clocks (CLKIN0 and CLKIN1) can be freely switched with the glitchless function triggered by the falling edge of the clock.
SIM_DEVICE	"TITAN","LOGOS", "COMPACT","LOGOS2", "TITAN2","TITAN3"	"TITAN"	Device family selection

7.4.4 Functional Description

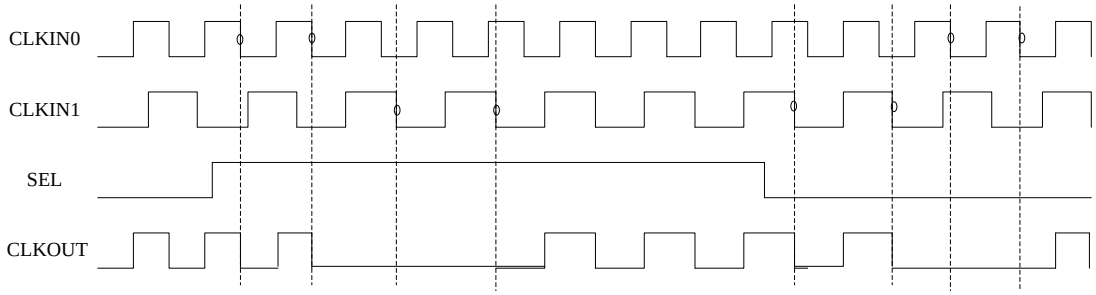

Figure 7-5 GTP_CLKBUFGMUX Waveform Diagram

7.4.5 Instantiation template

```
GTP_CLKBUFGMUX
#(
      .TRIGGER_MODE ("NEGEDGE "),
     .SIM_DEVICE       ("COMPACT")
)GTP_CLKBUFGMUX_inst        (
      .CLKIN0              (CLKIN0      ),
      .CLKIN1              (CLKIN1    ),
      .SEL                 (SEL          ),
      .CLKOUT              (CLKOUT    )
);
```

7.5 GTP_IOCLKBUF

7.5.1 Description of Functionality

Like a "gate", GTP_IOCLKBUF can be used to enable or disable the I/O clock. The structure block diagram is shown below.

Figure 7-6 GTP_IOCLKBUF Structure Block Diagram

7.5.2 Port Description

Table 7-7 GTP_IOCLKBUF Port Description

Port	Direction	Function Description
CLKIN	Input	Input Clock
DI	Input	Enable signal. When DI is active, 1'b0 denotes IO clock disabled, and 1'b1 denotes IO clock enabled
CLKOUT	Output	Output clock

7.5.3 Paramater Description

Table 7-8 GTP_IOCLKBUF Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
GATE_EN	"FALSE", "TRUE"	"FALSE"	When "TRUE", the enable signal DI is valid; when "FALSE", the enable signal DI is invalid;

7.5.4 Functional Description

When the parameter GATE_EN is "TRUE" or "FALSE", the corresponding waveform diagrams are as shown in the two figures below.

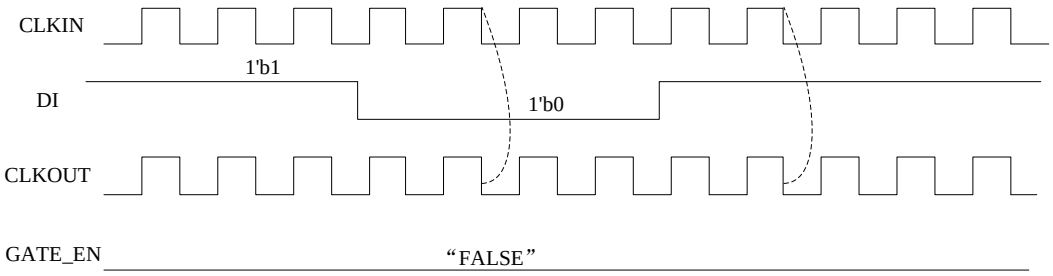

Figure 7-7 Timing diagram of GTP_IOCLKBUF with GATE_EN="FALSE"

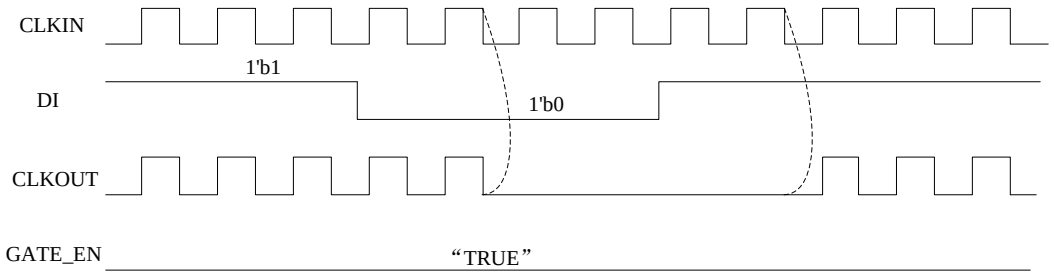

Figure 7-8 Timing diagram of GTP_IOCLKBUF with GATE_EN="TRUE"

7.5.5 Instantiation template

```
GTP_IOCLKBUF
#(
    .GATE_EN        ("FALSE"    )     //FALSE; TRUE
) GTP_IOCLKBUF_inst  (
.CLKOUT             (CLKOUT    ),
.CLKIN          (CLKIN),
.DI             (DI        )
);
```

7.6 GTP_IOCLKDIV_E1

7.6.1 Description of Functionality

GTP_IOCLKDIV_E1 converses the clock domain from I/O clock to global clock and can implement clock frequency division, supporting division by 2, 3.5, 4, or bypass output. The structure block diagram is shown below.

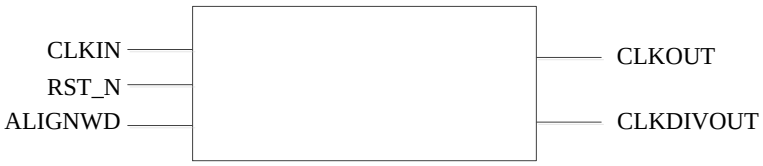

Figure 7-9 GTP_IOCLKDIV_E1 Structure Block Diagram

7.6.2 Port Description

Table 7-9 GTP_IOCLKDIV_E1 Port Description

Port	Direction	Function Description
CLKIN	Input	Input Clock
ALIGNWD	Input	Provides the level hold function to the output division clock; in divide-by-2 or divide-by-4 modes, it is triggered by the rising edge of the input clock, during even-numbered ALIGNWD pulses, the division clock is held for one input clock cycle upon the fourth rising edge of the input clock. In the 3.5 division mode, the division clock is maintained for one input clock cycle when the fourth rising edge of the input clock occurs in each ALIGNWD pulse.
RST_N	Input	Active-low reset
CLKDIVOUT	Output	Divided output clock
CLKOUT	Output	Output clock without division

7.6.3 Paramater Description

Table 7-10 GTP_IOCLKDIV_E1 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
DIV_FACTOR	"DIV_DIS", "2", "3.5", "4"	"DIV_DIS"	When set to "DIV_DIS", CLKOUT=1'b1, and CLKDIVOUT=1'b1; when the division ratio is "2", "3.5" or "4", CLKOUT=CLKIN and CLKDIVOUT outputs the division clock.
GRS_EN	"TRUE", "FALSE"	"TRUE"	Global enable signal. "TRUE" indicates the global enable signal is active; “FALSE” indicates the global enable signal is inactive.

7.6.4 Functional Description

For a detailed functional description of GTP_IOCLKDIV_E1, please refer to "***UG030003_Compa Family CPLD Clock Resources (Clock & PLL) User Guide***".

7.6.5 Instantiation template

```
GTP_IOCLKDIV_E1 #(
.DIV_FACTOR             ("DIV_DIS" ),    //"DIV_DIS", "2", "3.5", "4";
.GRS_EN                 ("TRUE"    )    //"TRUE", "FALSE"
)GTP_IOCLKDIV_E1_inst(
.CLKIN                   (CLKIN     ),
.RST_N                   (RST_N     ),
.ALIGNWD            (ALIGNWD    ),
.CLKOUT                 (CLKOUT      ),
.CLKDIVOUT              (CLKDIVOUT   )
);
```

7.7 GTP_IOCLKMUX

7.7.1 Description of Functionality

GTP_IOCLKMUX enables bridging I/O clocks across different regions, meaning the I/O clock on top can be bridged to the bottom of the chip through instantiating GTP_IOCLKMUX to drive the I/O logic underneath, and similarly, the IO clock on the bottom can be bridged to the top to drive the I/O logic above. The structure block diagram is shown below.

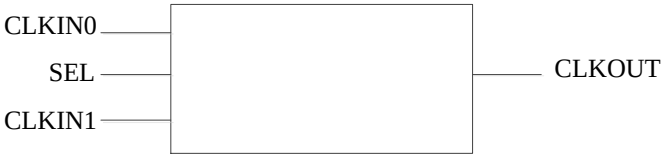

Figure 7-10 GTP_IOCLKMUX Structure Block Diagram

7.7.2 Port Description

Table 7-11 GTP_IOCLKMUX Port Description

Port	Direction	Function Description
CLKIN0	Input	Input clock 0
CLKIN1	Input	Input clock 1
SEL	Input	Clock select signal. Select CLKIN0 when it is 1'b0; select CLKIN1 when it is 1'b1
CLKOUT	Output	Output clock

7.7.3 Functional Description

For a detailed functional description of GTP_IOCLKMUX, please refer to "***UG030003_Compa Family CPLD Clock Resources (Clock & PLL) User Guide***".

7.7.4 Instantiation template

```
GTP_IOCLKMUX GTP_IOCLKMUX_inst
(
    .CLKIN0         (CLKIN0     ),
    .CLKIN1         (CLKIN1     ),
    .SEL            (SEL        ),
    .CLKOUT         (CLKOUT     )
     );
```

7.8 GTP_IOCLKDELAY

7.8.1 Description of Functionality

The clock input pins offer an optional delay function, allowing users to instantiate GTP_IOCLKDELAY to achieve a delay on the input clock. Users can statically configure the delay step (adjust the number of delay steps, with each step delaying by 20ps; the minimum delay chain

count is 0, and the maximum is 127 (8'b0–8'b0111_1111)), or dynamically obtain the delay steps using the DLL. Furthermore, GTP_IOCLKDELAY also provides a user interface to adjust delay steps dynamiclyfine adjustment. The structure block diagram is shown below.

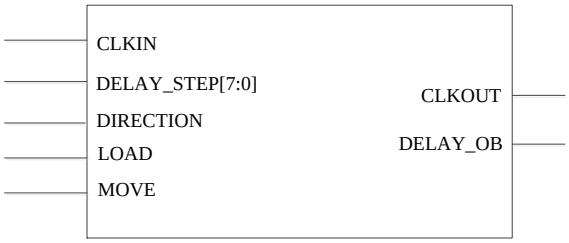

Figure 7-11 GTP_IOCLKDELAY Structure Block Diagram

7.8.2 Port Description

Table 7-12 GTP_IOCLKDELAY Port Description

Port	**Direction**	**Function Description**
CLKIN	Input	Clock input from pin
DELAY_STEP[7:0]	Input	Delay step from DLL
DIRECTION	Input	Set to 0 to dynamically increase the delay step; set to 1 to dynamically decrease the delay step.
LOAD	Input	Active-high, reset the delay step to DELAY_STEP or a static delay value.
MOVE	Input	The falling edge triggers dynamic fine adjustment, increasing or decreasing one step depending on the DIRECTION.
DELAY_OB	Output	Dynamic fine adjustment overflow flag for Delay Step. When parameter SIM_DEVICE is set to COMPA, the signal goes high at 127 when DIRECTION is set to 0; it goes high at 0 when DIRECTION is set to 1.
CLKOUT	Output	Delayed clock output

7.8.3 Paramater Description

Table 7-13 GTP_IOCLKDELAY Parameter Description

Parameter Name	**Valid Values**	**Defaults**	**Functional Description**
DELAY_STEP_VALUE	0-127	8'd0	Static delay step, effective when DELAY_STEP_SEL is set to "PARAMETER"
DELAY_STEP_SEL	"PARAMETER" "PORT"	"PARAMETER"	"PORT" selects the value of port DELAY_STEP as the reference delay step; "PARAMETER" selects DELAY_STEP_VALUE as the reference delay step
SIM_DEVICE	"TITAN" "LOGOS" "COMPACT"	"TITAN"	Device family selection

7.8.4 Functional Description

For a detailed functional description of GTP_IOCLKDELAY, please refer to "***UG030003_Compa Family CPLD Clock Resources (Clock & PLL) User Guide***".

7.8.5 Instantiation template

```
GTP_IOCLKDELAY
#(
    .DELAY_STEP_VALUE (8'd0              ), //Used for static delay step setting, 0~127
    .DELAY_STEP_SEL      ("PARAMETER"),   //"PARAMETER", "PORT"
   .SIM_DEVICE          ("COMPACT"   )
) GTP_IOCLKDELAY_inst(
    .CLKIN                  (CLKIN       ),
    .DELAY_STEP      (DELAY_STEP  ),
    .CLKOUT              (CLKOUT      ),
    .DIRECTION       (DIRECTION   ),
    .LOAD            (LOAD        ),
    .MOVE                (MOVE        ),
    .DELAY_OB        (DELAY_OB    ));
```

7.9 GTP_OSC_E2

7.9.1 Description of Functionality

GTP_OSC_E2 provides users with a configurable output clock. The structure block diagram is shown below.

Figure 7-12 GTP_OSC_E2 Structure Block Diagram

7.9.2 Port Description

Table 7-14 GTP_OSC_E2 Port Description

Port	Direction	Function Description
CLKOUT	Output	Output clock for user, with output frequency configured by CLK_DIV, through the global clock network
CLKCRC	Output	Output clock, default frequency of 2.08MHz, provides clock for GTP_RBCRC
EN_N	Input	OSC output enable signal; when it is 1'b1, OSC is disabled; when it is 1'b0, OSC is enabled

7.9.3 Paramater Description

Table 7-15 GTP_OSC_E2 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
CLK_DIV	0-127	0	Clock division factor setting, valid values are 0–127
USER_DIV_EN	"TRUE", "FALSE"	"TRUE"	User division parameter CLK_DIV enable; "TRUE" for enable; "FALSE" for disable

7.9.4 Functional Description

Provide user-configurable output clock, which can serve as an input source for the global clock. The correspondence between the output clock and CLK_DIV is as follows:

Table 7-16 GTP_OSC_E2 Division Factor and Output Clock Relationship

CLK_DIV	CLKOUT(MHz)
0	266/128
1	266/2
2	266/2
3	266/3
…	…
125	266/125
126	266/126
127	266/127

7.9.5 Instantiation template

```
GTP_OSC_E2
#(
.CLK_DIV      (0            ),
.USER_DIV_EN    ("TRUE" )
) GTP_OSC_E2_inst (
```

```
.CLKOUT         (CLKOUT    ),
.EN_N           (EN_N      ),
.CLKCRC         (CLKCRC    ));
```

7.10 GTP_PLL_E2

7.10.1 Description of Functionality

GTP_PLL_E2 mainly implements frequency division, frequency multiplication, and phase adjustment. This GTP supports dynamic selection of input clock, internal and external feedback modes, dynamic reconfiguration, and output clock gating. The structure block diagram is shown below.

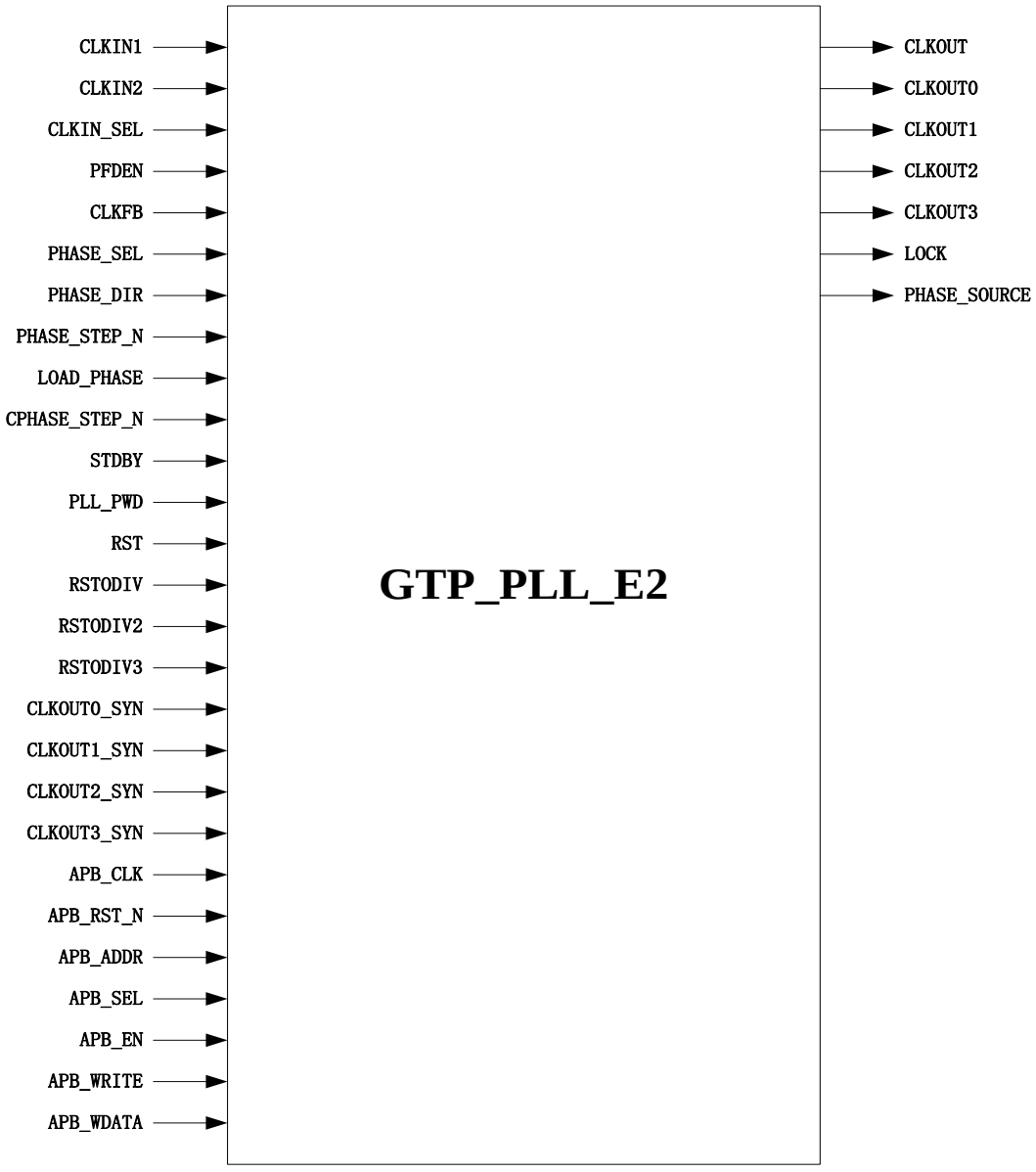

Figure 7-13 GTP_PLL_E2 Structure Block Diagram

7.10.2 Port Description

Table 7-17 GTP_PLL_E2 Port Description

Port Signal	Direction	Function Description
CLKOUT	Output	PLL reference clock output; reference clock enters the PLL and is directly bypassed output (Bypass PLL) without going through the input clock divider, PFD, CP, LPF, VCO, and output divider;
CLKOUT0	Output	First PLL output clock, with phase adjustment function;
CLKOUT1	Output	Second PLL output clock, with phase adjustment function;
CLKOUT2	Output	Third PLL output clock, with phase adjustment function;
CLKOUT3	Output	Fourth PLL output clock, with phase adjustment function;
PHASE_SOURCE	Output	Indication signal for the source of dynamic phase adjustment control signal; 1'b0: Indicates that the control signal comes from the APB interface. 1'b1: Indicates that the control signal comes from dynamic ports CPHASE_STEP_N, LOAD_PHASE, PHASE_SEL, PHASE_DIR, and PHASE_STEP_N. If the user didn't choose a dynamic port, the register with the APB interface will be used by default for dynamic phase adjustment settings.
LOCK	Output	An asynchronous PLL frequency lock indication signal; when the signal goes high, it indicates that the PLL feedback clock signal is locked to the input clock signal; when the clock recovers from a lost or unstable state, PLL needs to be reset via the reset pin RST
CLKIN1	Input	PLL reference input clock 1;
CLKIN2	Input	PLL reference input clock 2;
CLKFB	Input	PLL feedback clock input;
CLKIN_SEL	Input	The input clock selection signal, which selects either of the input reference clocks CLKIN1 and CLKIN2 as the input clock for the input divider; selects CLKIN1 when it is 1'b0 and selects CLKIN2 when it is 1'b1
PFDEN	Input	PFD enable signal for the PLL; 1'b0 indicates that the PFD is disabled, and 1'b1 indicates that the PFD is enabled; PFDEN is an optional signal, and the user can decide whether PFDEN is effective through the static configuration parameter PFDEN_EN. Note that after PFD is turned off, the LOCK signal still maintains a high level for a period of time before pulling down, during which there will still be clock output, but the clock will be unstable
PHASE_SEL	Input	Select any PLL output clock for phase adjustment; 2'b00: Selects CLKOUT0, 2'b01: Selects CLKOUT3, 2'b10: Selects CLKOUT2, 2'b11: Selects CLKOUT1;
PHASE_DIR	Input	Select the direction for dynamic phase fine adjustment; 1'b0: lag shift, 1'b1: lead shift;
PHASE_STEP_N	Input	Dynamic phase fine adjustment trigger signal; with each trigger, the output clock phase is adjusted by 1/8 Tvco
LOAD_PHASE	Input	Load signal for the current phase fine adjustment value of the selected channel, pulse signal, active-high;
CPHASE_STEP_N	Input	Dynamic phase coarse adjustment trigger signal; each trigger increments the counter by +1, adjusting the output clock phase by n*Tvco, where n*Tvco is set through phase coarse static configuration;
CLKOUT0_SYN	Input	CLKOUT0 output clock enable control; active high. The signal is active when the user sets CLKOUT0_SYN_EN to "TRUE." If the user sets the CLKOUT0 output as active, or if there is no requirement for the signal CLKOUT0_SYN, the CLKOUT0 output clock is always active unless the PLL is in Standby mode.
CLKOUT1_SYN	Input	CLKOUT1 clock output enable control; active high; its function is the same

Port Signal	Direction	Function Description
		as CLKOUT0_SYN
CLKOUT2_SYN	Input	CLKOUT2 clock output enable control; active high; its function is the same as CLKOUT0_SYN
CLKOUT3_SYN	Input	CLKOUT3 clock output enable control; active high; its function is the same as CLKOUT0_SYN
STDBY	Input	Standby mode control signal; active high; turns off all PLL modules; the STDBY signal can be controlled via user logic or the Power Controller module. The STDBY signal is optional and is controlled by the configuration bit STDBY_EN. It is active when set to "TRUE" and inactive when set to "FALSE."
PLL_PWD	Input	PLL Power Down; active high; disable modules except for the LDO;
RST	Input	The PLL reset signal, active high; this signal resets the VCO, PFD, CP, LPF, and all clock dividers, including input dividers and output dividers. The reset signal will pull down the PLL output directly to ground. After the reset is released, the PLL starts to enter the lock state, and the PLL frequency lock is completed after the tLOCK (PLL lock time).
RSTODIV	Input	PLL reset signal, active high; this signal can reset the VCO, PFD, CP, LPF, and all dividers except the input divider; the reset signal cannot reset the reference input divider; after reset release, the PLL begins to enter the lock state and completes frequency lock after the tLOCK (PLL lock time).
RSTODIV2	Input	PLL reset signal only to reset the output divider of CLKOUT2; active high. If the CLKOUT2 output is used in the PLL feedback path, it is recommended to use the RST or RSTODIV signal to reset the PLL, rather than the RSTODIV2 reset signal
RSTODIV3	Input	PLL reset signal only to reset the output divider of CLKOUT3; active high. If the CLKOUT3 output is used in the PLL feedback path, it is recommended to use the RST or RSTODIV signal to reset the PLL, rather than the RSTODIV3 reset signal
APB_CLK	Input	PLL APB interface bus clock;
APB_RST_N	Input	PLL APB interface bus asynchronous reset signal, active low;
APB_ADDR	Input	PLL APB interface bus address;
APB_SEL	Input	PLL APB interface bus select signal to select the slave device, active high;
APB_EN	Input	The PLL APB port bus enable signal, which indicates the second and subsequent cycles of transmission, active high;
APB_WRITE	Input	PLL APB interface bus write enable signal; 1'b0: read operation, 1'b0: write operation;
APB_WDATA	Input	PLL APB interface bus data input;

7.10.3 Paramater Description

Table 7-18 GTP_PLL_E2 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
CLKIN_FREQ	10~500	50	Input Clock Frequency
PFDEN_EN	"FALSE", "TRUE"	"FALSE"	PFDEN signal enable configuration; "FALSE": PFDEN signal input is invalid; "TRUE": PFDEN signal input is active;
PFDEN_APB_EN	"FALSE", "TRUE"	"FALSE"	PLL PFD enable signal source configuration; "FALSE": from port; "TRUE": from APB interface;
LOCK_MODE	1’b0~1’b1	1’b0	PLL frequency detection mode configuration;

Parameter Name	Valid Values	Defaults	Function Description
			1'b0: real-time monitoring mode; 1'b1: hold mode
STATIC_RATIOI	1~50	1	The division ratio configuration of the input clock divider;
STATIC_RATIO0	1~128	1	The division ratio configuration of the CLKOUT0 divider;
STATIC_RATIO1	1~128	1	The division ratio configuration of the CLKOUT1 divider;
STATIC_RATIO2	1~128	1	The division ratio configuration of the CLKOUT2 divider;
STATIC_RATIO3	1~128	1	The division ratio configuration of the CLKOUT3 divider;
STATIC_RATIOF	1~128	1	The division ratio configuration of the feedback divider; Integer divider: 1~128 Fractional divider: 7~120
FRACN_EN	"FALSE", "TRUE"	"FALSE"	Fractional Division function enable; "FALSE": fractional division function disabled; "TRUE": fractional division function enabled;
FRACN_DIV	0~65535	0	Fractional division fraction configuration;
PHASE_APB_EN	"FALSE", "TRUE"	"FALSE"	Source configuration for control signal of dynamic phase adjustment; "FALSE": from port; "TRUE": from APB interface;
STATIC_PHASE0	0~7	0	CLKOUT0 phase fine adjustment static configuration parameter
STATIC_PHASE1	0~7	0	CLKOUT1 phase fine adjustment static configuration parameter
STATIC_PHASE2	0~7	0	CLKOUT2 phase fine adjustment static configuration parameter
STATIC_PHASE3	0~7	0	CLKOUT3 phase fine adjustment static configuration parameter
STATIC_CPHASE0	0~127	0	CLKOUT0 phase coarse adjustment static configuration parameter
STATIC_CPHASE1	0~127	0	CLKOUT1 phase coarse adjustment static configuration parameter
STATIC_CPHASE2	0~127	0	CLKOUT2 phase coarse adjustment static configuration parameter
STATIC_CPHASE3	0~127	0	CLKOUT3 phase coarse adjustment static configuration parameter
VCOCLK_BYPASS0	"FALSE", "TRUE"	"FALSE"	VCO clock bypass configuration (MUXA0 configuration bit); "FALSE": select VCO clock; "TRUE": select PLL reference clock;
VCOCLK_BYPASS1	"FALSE", "TRUE"	"FALSE"	VCO clock bypass configuration (MUXB0 configuration bit); "FALSE": select VCO clock; "TRUE": select PLL reference clock;
VCOCLK_BYPASS2	"FALSE", "TRUE"	"FALSE"	VCO clock bypass configuration (MUXC0 configuration bit); "FALSE": select VCO clock; "TRUE": select PLL reference clock;
VCOCLK_BYPASS3	"FALSE", "TRUE"	"FALSE"	VCO clock bypass configuration (MUXD0 configuration bit); "FALSE": select VCO clock;

Parameter Name	Valid Values	Defaults	Function Description
			"TRUE": select PLL reference clock;
ODIV0_CLKIN_SEL	0~3	0	MUXA1 configuration in front of the CLKOUT0 divider; 0: select the output of MUXA0; 1: select the output of CLKOUT3 divider; 2: select the output of CLKOUT1 divider; 3: select the output of CLKOUT2 divider;
ODIV1_CLKIN_SEL	0~3	0	MUXB1 configuration in front of the CLKOUT1 divider; 0: select the output of MUXB0; 1: select the output of CLKOUT0 divider; 2: select the output of CLKOUT3 divider; 3: select the output of CLKOUT2 divider;
ODIV2_CLKIN_SEL	0~3	0	MUXC1 configuration in front of the CLKOUT2 divider; 0: select the output of MUXC0; 1: select the output of CLKOUT0 divider; 2: select the output of CLKOUT1 divider; 3: select the output of CLKOUT3 divider;
ODIV3_CLKIN_SEL	0~3	0	MUXD1 configuration in front of the CLKOUT3 divider; 0: select the output of MUXD0; 1: select the output of CLKOUT0 divider; 2: select the output of CLKOUT1 divider; 3: select the output of CLKOUT2 divider;
CLKOUT0_SEL	0~4	0	MUXA2 configuration behind the CLKOUT0 divider; 0: select the output of the CLKOUT0 divider; 1: select the output of the CLKOUT1 divider; 2: select the output of the CLKOUT2 divider; 3: select the output of CLKOUT3 divider; 4: select PLL reference clock;
CLKOUT1_SEL	0~4	0	MUXB2 configuration behind the CLKOUT1 divider; 0: select the output of the CLKOUT1 divider; 1: select the output of the CLKOUT2 divider; 2: select the output of CLKOUT3 divider; 3: select the output of the CLKOUT0 divider; 4: select PLL reference clock;
CLKOUT2_SEL	0~4	0	MUXC2 configuration behind the CLKOUT2 divider; 0: select the output of the CLKOUT2 divider; 1: select the output of CLKOUT3 divider; 2: select the output of the CLKOUT0 divider; 3: select the output of the CLKOUT1 divider; 4: select PLL reference clock;
CLKOUT3_SEL	0~4	0	MUXD2 configuration behind the CLKOUT3 divider; 0: select the output of the CLKOUT3 divider; 1: select the output of CLKOUT0 divider; 2: select the output of CLKOUT1 divider; 3: select the output of CLKOUT2 divider; 4: select PLL reference clock;
CLKOUT0_SYN_EN	"FALSE", "TRUE"	"FALSE"	Configuration for CLKOUT0_SYN signal enable; "FALSE": CLKOUT0_SYN input is inactive,

Parameter Name	Valid Values	Defaults	Function Description
			"TRUE": CLKOUT0_SYN input is active;
CLKOUT1_SYN_EN	"FALSE", "TRUE"	"FALSE"	Configuration for CLKOUT1_SYN signal enable; "FALSE": CLKOUT1_SYN input is inactive, "TRUE": CLKOUT1_SYN input is active;
CLKOUT2_SYN_EN	"FALSE", "TRUE"	"FALSE"	Configuration for CLKOUT2_SYN signal enable; "FALSE": CLKOUT2_SYN input is inactive, "TRUE": CLKOUT2_SYN input is active;
CLKOUT3_SYN_EN	"FALSE", "TRUE"	"FALSE"	Configuration for CLKOUT3_SYN signal enable; "FALSE": CLKOUT3_SYN input is inactive, "TRUE": CLKOUT3_SYN input is active;
INTERNAL_FB	"CLKOUT0" "CLKOUT1" "CLKOUT2" "CLKOUT3" "DISABLE"	"CLKOUT0"	Internal feedback path select;
EXTERNAL_FB	"CLKOUT0" "CLKOUT1" "CLKOUT2" "CLKOUT3" "DISABLE"	"DISABLE"	External feedback path select;
BANDWIDTH	"LOW", "HIGH" "OPTIMIZED"	"OPTIMIZED"	Bandwidth select configuration;
STDBY_EN	"FALSE", "TRUE"	"FALSE"	STDBY signal enable configuration; "FALSE": STDBY input is inactive, "TRUE": STDBY input is active;
RST_INNER_EN	"FALSE", "TRUE"	"TRUE"	Reset signal RST enable configuration; "FALSE": RST input is inactive, "TRUE": RST input is active;
RSTODIV_EN	"FALSE", "TRUE"	"TRUE"	Reset signal RSTODIV enable configuration; "FALSE": RSTODIV input is inactive, "TRUE": RSTODIV input is active;
RSTODIV2_EN	"FALSE", "TRUE"	"FALSE"	Reset signal RSTODIV2 enable configuration; "FALSE": RSTODIV2 input is inactive, "TRUE": RSTODIV2 input is active;
RSTODIV3_EN	"FALSE", "TRUE"	"FALSE"	Reset signal RSTODIV3 enable configuration; "FALSE": RSTODIV3 input is inactive, "TRUE": RSTODIV3 input is active;

7.10.4 Functional Description

For detailed information on GTP_PLL_E2, please refer to the "***UG030003_Compa Family CPLD Clock Resources (Clock & PLL) User Guide***".

Chapter 8 Embedded Hard Core GTP

8.1 GTP_I2C

8.1.1 Description of Functionality

GTP_I2C will be mapped as an I^2C hard core. GTP_I2C supports Fast/Standard mode I^2C bus protocol with up to 400 kHz data transfer rate. It supports master/slave operations, synchronisation, arbitration, clock stretching, 7-bit/10-bit addressing, all call addressing, soft reset, start byte, device identification, interrupts, and other functions. The structure block diagram is shown below.

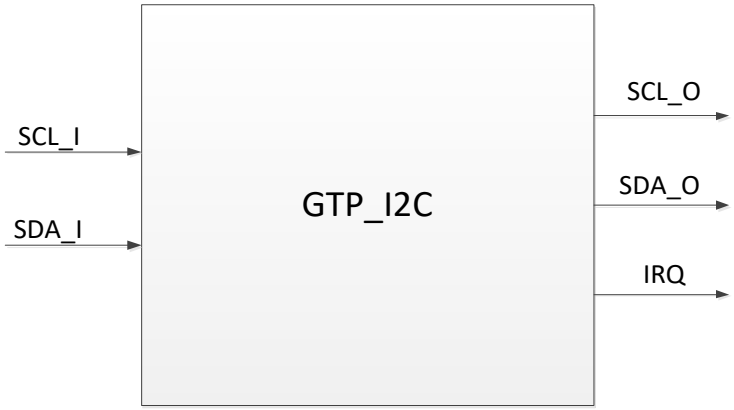

Figure 8-1 GTP_I2C Structure Block Diagram

8.1.2 Port Description

Table 8-1 GTP_I2C Port Description

Port	Direction	Function Description
SCL_I	Input	Serial clock input, with a maximum frequency of 400KHz In slave mode, the minimum frequency ratio of pclk to scl is 25:1. For an scl of 400KHz, the minimum pclk frequency is 10MHz.
SCL_O	Output	Serial clock output, with a maximum frequency of 400KHz
SDA_I	Input	Serial data input
SDA_O	Output	Serial data output
IRQ	Output	Interrupt request

8.1.3 Paramater Description

Table 8-2 GTP_I2C Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
I2C_NUM	0, 1	0	User called I2C number

8.1.4 Functional Description

GTP_I2C must be used in conjunction with GTP_APB. When implementing different functions of the I^2C hard core, users must operate registers through the APB interface. For detailed instructions on GTP_I2C, please refer to "***UG030007_Compa Family CPLD Embedded Hard Core User Guide***".

8.1.5 Instantiation template

```
GTP_I2C #(
      .I2C_NUM    (0)  // 0    1 available
) GTP_I2C_inst (
.SCL_I              (SCL_I),
.SCL_O              (SCL_O),
.SDA_I              (SDA_I),
.SDA_O              (SDA_O),
.IRQ                (IRQ)
);
```

8.2 GTP_SPI

8.2.1 Description of Functionality

GTP_SPI will be mapped as an SPI hard core. GTP_SPI can be used as a universal SPI interface in conjunction with GTP_APB. Users can implement master mode, slave mode, and interrupt function by operating registers through the APB interface. The structure block diagram is shown below.

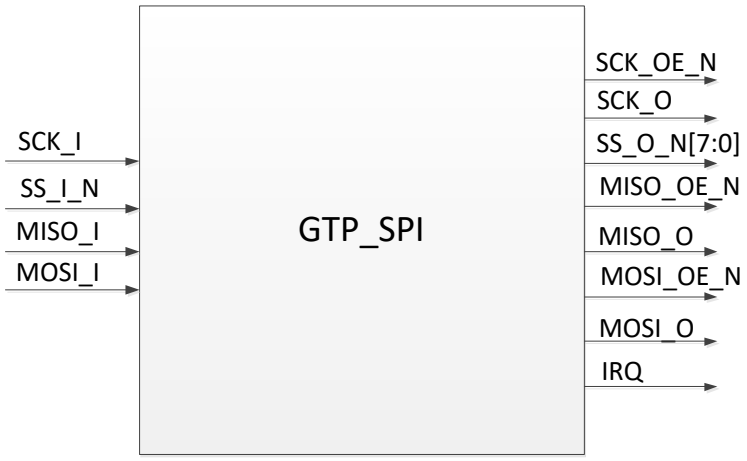

Figure 8-2 GTP_SPI Structure Block Diagram

8.2.2 Port Description

Table 8-3 GTP_SPI Port Description

Port	Direction	Function Description
SCK_OE_N	Output	Serial clock output enable, active low
SCK_I	Input	Serial clock input The maximum frequency ratio between slave mode sck and pclk: Write: 45:100 Write Before Read: 2.5:100 Write Before Fast Read: 15:100
SCK_O	Output	Serial clock output, with a maximum frequency of 50MHz
SS_O_N	Output	Chip select output, active low
SS_I_N	Input	Chip select input, active low
MISO_OE_N	Output	Slave output enable, active low
MISO_I	Input	Master input
MISO_O	Output	Slave output
MOSI_OE_N	Output	Master output enable, active low
MOSI_I	Input	Slave input
MOSI_O	Output	Master output
IRQ	Output	Interrupt request

8.2.3 Functional Description

For usage methods and register details of GTP_SPI, please refer to "***UG030007_Compa Family CPLD Embedded Hard Core User Guide***".

8.2.4 Instantiation template

```
GTP_SPI    GTP_SPI_inst
(
.SCK_OE_N        (SCK_OE_N),
.SCK_I           (SCK_I),
. SCK_O          (SCK_O),
.SS_O_N          (SS_O_N),
.SS_I_N          (SS_I_N),
.MISO_OE_N    (MISO_OE_N),
.MISO_I          (MISO_I),
.MISO_O          (MISO_O),
.MOSI_OE_N    (MOSI_OE_N),
.MOSI_I          (MOSI_I),
```

.MOSI_O (MOSI_O),

.IRQ (IRQ));

8.3 GTP_TIMER

8.3.1 Description of Functionality

GTP_TIMER will be mapped as a TIMER core. GTP_TIMER can implement a common 16-bit timing counter module with an independent output comparison unit and Pulse Width Modulation (PWM) function. The structure block diagram is shown below.

Figure 8-3 GTP_TIMER Structure Block Diagram

8.3.2 Port Description

Table 8-4 GTP_TIMER Port Description

Port	**Direction**	**Function Description**
RST_N	Input	Asynchronous reset, active low
CLK	Input	Timing clock, with the maximum frequency of 4MHz pclk and clk are asynchronous clocks
STAMP	Input	Time stamp collection Pulse signal
PWM	Output	Pulse width modulation
IRQ	Output	Interrupt request

8.3.3 Functional Description

When using the TIMER hard core, users need to instantiate the corresponding GTP_TIMER, which should be used in conjunction with GTP_APB. For detailed instructions on GTP_TIMER, please refer to "***UG030007_Compa Family CPLD Embedded Hard Core User Guide***".

8.3.4 Instantiation template

```
GTP_TIMER     GTP_TIMER_inst
(
    .RST_N        (rst_sys_n),
    .CLK          (clk          ),
    .STAMP        (stamp        ),
    .PWM          (pwm          ),
    .IRQ          (irq_timer    )
);
```

8.4 GTP_POWERCTL

8.4.1 Description of Functionality

The power consumption controller GTP_POWERCTL can put the device into low power mode; it can control the POR circuit, Bandgap circuit, and logic modules to enter a standby state, thus reducing power consumption. The structure block diagram is shown below.

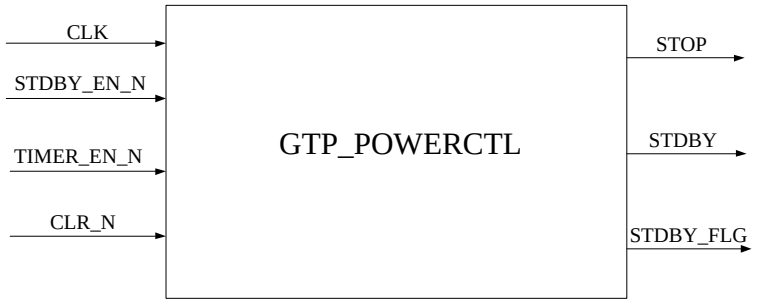

Figure 8-4 GTP_POWERCTL Structure Block Diagram

8.4.2 Port Description

Table 8-5 GTP_POWERCTL Port Description

Port	Direction	Function Description
CLK	Input	External input clock, with a maximum frequency of 50MHz
STDBY_EN_N	Input	Standby enable, active low Enter the shutdown process from operating mode to standby mode, starting from the falling edge of standby enable. Enter the wake-up process from standby mode to operating mode, starting from the rising edge of standby enable
TIMER_EN_N	Input	Timer enable, active low Pulse signal, for starting the timer counting

Port	Direction	Function Description
CLR_N	Input	Standby complete, active low Pulse signal, for clearing the standby flag after wake-up
STOP	Output	Stop Used for standby preparation. User logic prepares for standby by shutting down signals such as the clock
STDBY	Output	Standby Global signal, output via SRB to user logic, IO PAD, and PLL. Used for controlling logic circuits to enter standby mode
STDBY_FLG	Output	Standby flag Indicates that the device is in standby mode

8.4.3 Functional Description

GTP_POWERCTL controls the device to work or standby through switching between different modes, as shown in the timing diagram below.

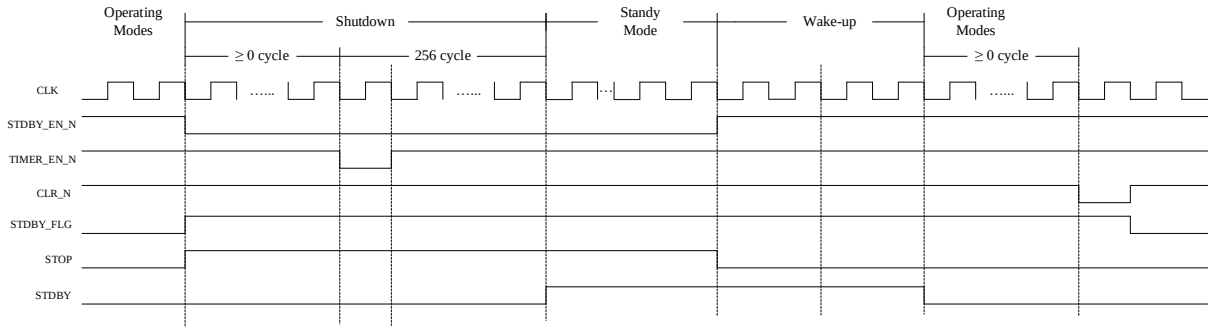

Figure 8-5 GTP_POWERCTL Timing Diagram

Shutdown:

When the standby enable STDBY

6. EN_N changes to active from inactive, the power controller enters shutdown mode from operating mode:
   1) Generates a standby flag STDBY_FLG, indicating that the device is in standby mode.
   2) Generates a standby preparation STOP, where user logic prepares for standby through signals like shutdown clock.
7. The timer enable TIMER_EN_N pulse becomes active, starting the timer counting.
8. After counting 256 clock cycles by the timer:
   1) Generates a global standby signal which is outputted via SRB to user logic, IO PAD, OSC, and PLL for controlling logic circuits to enter standby mode.
   2) Shuts down the band gap circuit and the power-up reset circuit. When the band gap circuit is shut down, the power-up reset circuit and analogue circuits (PLL, OSC) are also shut down.

Wake-up:

9. When the standby enable STDBY_EN_N changes from active to inactive, the power controller enters wake-up mode from standby mode:
   1) Clears standby preparation STOP.
   2) Turns on the band gap circuit.
10. After the band gap circuit stabilises, the global standby signal is cleared, and the power controller enters operating mode from wake-up mode.
11. After entering the operating mode, the user logic generates a standby end pulse:
   1) Turns on the power-up reset circuit.
   2) Clears the standby flag STDBY_FLG.

8.4.4 Instantiation template

```
GTP_POWERCTL     GTP_ POWERCTL_inst
(
    .STDBY_EN_N        (STDBY_EN_N    ),
    .CLK               (CLK           ),
    .TIMER_EN_N        (TIMER_EN_N    ),
    .CLR_N             (CLR_N         ),
    .STOP              (STOP          ),
    .STDBY             (STDBY         ),
    .STDBY_FLG         (STDBY_FLG     )
);
```

8.5 GTP_BANKCTL

8.5.1 Description of Functionality

GTP_BANKCTL supports dynamic enabling and disabling true differential outputs in BANK0 and differential input I/O in BANK0-5, to save power. The structure block diagram is shown below.

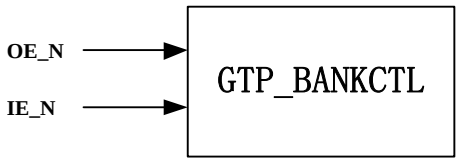

Figure 8-6 GTP_BANKCTL Structure Block Diagram

8.5.2 Port Description

Table 8-6 GTP_BANKCTL Port Description

Port	Direction	Function Description
OE_N	Input	Disable or enable true differential output in bank0 0: Enable output; 1: Disable output
IE_N	Input	Disable or enable differential input in banks 0-5 0: Enable input; 1: Disable input

8.5.3 Paramater Description

Table 8-7 GTP_BANKCTL Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
DIFFO_DYN_EN	"FALSE","TRUE"	"FALSE"	Differential output dynamic control. TRUE: Enable; FALSE: Disable
DIFFI_DYN_EN	"FALSE", "TRUE"	"FALSE"	Differential input dynamic control. TRUE: Enable; FALSE: Disable
BANK_LOC	"BK0", "BK1", "BK2", "BK3", "BK4", "BK5"	"BK0"	Specify bank location

8.5.4 Functional Description

GTP_BANKCTL is only effective when differential I/O is used in the application.

8.5.5 Instantiation template

```
GTP_BANKCTL    GTP_BANKCTL_inst
(
    .OE_N          (OE_N),
    .IE_N          (IE_N     )
);
```

Chapter 9 Other GTPs

9.1 GTP_DLL_E1

9.1.1 Description of Functionality

GTP_DLL_E1 is mainly used to dynamically lock the frequency of the input reference clock and output the number of delay steps equivalent to a quarter of the clock cycle. The delay step can be used to track changes in temperature and voltage in real time.

9.1.2 Port Description

Table 9-1 GTP_DLL_E1 Port Description

Port	Direction	Function Description
CLKIN	Input	Clock input from pin
UPDATE_N	Input	Request to update DLL's delay step (active-low)
RST	Input	Active-high reset signal
PWD	Input	Low power control signal, active high
DELAY_STEP	Output	DLL output delay steps controlled by UPDATE_N
DELAY_STEP1	Output	DLL output delay steps not controlled by UPDATE_N
LOCK	Output	LOCK flag signal. 1 indicates that it is locked

9.1.3 Paramater Description

Table 9-2 GTP_DLL_E1 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
GRS_EN	"TRUE", "FALSE"	"TRUE"	Global reset enable signal
FAST_LOCK	"TRUE", "FALSE"	"TRUE"	DLL LOCK mode select
DELAY_STEP_OFFSET	-4, -3, -2, -1, 0, 1, 2, 3, 4	0	Static fine adjustment of DLL output DELAY_STEP

9.1.4 Functional Description

GTP_DLL_E1 must be used in conjunction with GTP_IOCLKDELAY, which employs the delay step outputted by GTP_DLL_E1 to accomplish a 1/4 cycle delay of the input clock signal for proper data sampling; the ISERDES in the IOL will use this GTP_IOCLKDELAY delay step to generate a clock phase-shifted by 90 degrees with the data.

9.2 GTP_GRS

9.2.1 Description of Functionality

This GTP is used to control the global reset signal and must be instantiated during simulation.

9.2.2 Port Description

Table 9-3 GTP_GRS Port Description

Port	Direction	Function Description
GRS_N	Input	Global reset

9.2.3 Instantiation template

```
GTP_GRS GRS_INST(
        .GRS_N (grs_n)
    );
```

9.3 GTP_START_E1

9.3.1 Description of Functionality

This GTP describes the process of releasing the global signal for the wake-up operation.

9.3.2 Port Description

Table 9-4 GTP_START_E1 Port Description

Port	Direction	Function Description
CLK	Input	Wake-up clock
GOE	Input	Global I/O output enable
GRS_N	Input	Global reset
GWE_N	Input	Memory write enable
WAKEUP_OVER	Output	Wake-up completion flag signal

9.3.3 Functional Description

Used for wake-up operation and the release of the global signal.

9.3.4 Instantiation template

```
GTP_START GTP_START_inst(
    .CLK        (clk ),
    .GOE        (gouten),
    .GRS_N          (grs_n),
    .GWE        (gwe),
   .WAKEUP_OVER         (wakeup_over)
);
```

9.4 GTP_SCANCHAIN_E1

9.4.1 Description of Functionality

Read the value of the user data register through the JTAG interface.

9.4.2 Port Description

Table 9-5 GTP_SCANCHAIN_E1 Port Description

Port	Direction	Function Description
TDI	Input	Jtag interface, from pad
TDO	Output	Jtag interface, output to pad
TMS	Input	Jtag interface, from pad
TCK	Input	Jtag interface, from pad
RST	Output	Jtag soft reset output
CAPDR	Output	Jtag Capturedr status indication
SHFTDR	Output	Shiftdr status indicator
UPDR	Output	Updatedr status indicator
JCLK	Output	Gate clock for user registers
FLG_USER	Output	User instruction indicator
TDI_USER	Output	Input data of user registers
TDO_USER	Input	Output data of user registers
JRTI	Output	Run/test idle status indicator
TCK_USER	Output	Tck to user
TMS_USER	Output	Tms to user

9.4.3 Paramater Description

Table 9-6 GTP_SCANCHAIN_E1 Parameter Description

Parameter Name	Valid Values	Defaults	Function Description
IDCODE	0~32'hffffffff ;	32'haaaa5555	Device identification code
CHAIN_NUM	1, 2, 3, 4	1	User DR number

9.4.4 Functional Description

Users can use it to read the chip IDCODE, or read/write multiple user logic data register values separately through the JTAG interface.

9.4.5 Instantiation template

```
GTP_SCANCHAIN
#(
    .IDCODE (32'haaaa5555),
    .CHAIN_NUM (1)
)
GTP_SCANCHAIN_inst(
    .TCK        (tck),
    .TDI        (tdi),
    .TMS        (tms),
    .TDO        (tdo),
    .CAPDR      (capture),
    .JCLK       (jclk),
    .RST        (rst),
    .FLG_USER   (flg_user),
    .SHFTDR     (shift),
    .TDI_USER   (tdi_user),
   .TMS_USER    (tms_user),
   .JRTI        (jrti),
    .UPDR       (update),
    .TDO_USER   (tdo_user));
```

9.5 GTP_UDID

9.5.1 Description of Functionality

This GTP is used to read the UDID CODE value.

9.5.2 Port Description

Table 9-7 GTP_UDID Port Description

Port	Direction	Function Description
DI	Input	Serial data input
DO	Output	Serial data output
SE	Input	Data shift enable, active high
LOAD	Input	Load UDID_CODE into Data registers
CLK	Input	Clock

9.5.3 Paramater Description

Table 9-8 GTP_UDID Parameter Description[1]

Parameter Name	Valid Values	Defaults	Function Description
UDID_CODE	0~96' hffff_ffff_ffff_ffff_ffff_ffff	0	Chip identity code, 96 bits
UDID_WIDTH	0~32' hffff_ffff	64	Set the valid bit width of UDID_CODE. The UID for Compa device is 64 bits

Note: 1. The GTP_UDID parameter is only used for simulation and do not affect the real UID value read back from the chip on the board.

9.5.4 Functional Description

Serially output 64-bit UID to the user. The operation timing diagram is as follows.

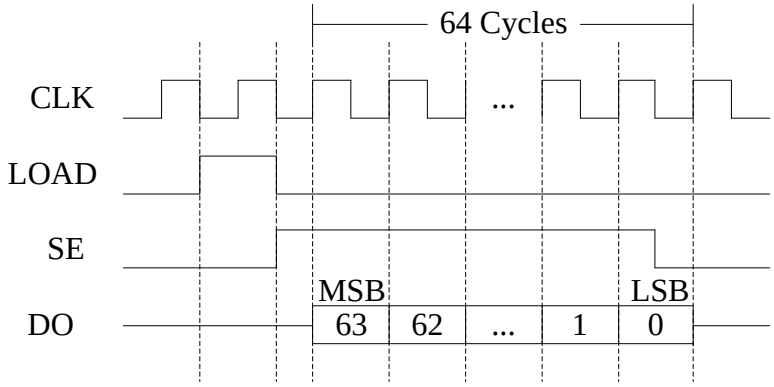

Figure 9-1 Read UID Timing Diagram

9.5.5 Instantiation template

```
GTP_UDID#(
        .UDID_CODE (0),
      .UDID_WIDTH(64)
)
GTP_UDID_inst(
    .DI     (di),
    .DO         (do),
    .LOAD (load),
    .SE     (se),
    .CLK    (clk)
);
```

9.6 GTP_RBCRC

9.6.1 Description of Functionality

GTP_RBCRC is used to read back non-DRM data stored in CRAM (excluding DRM initialization data) to calculate the CRC value, compare the calculated CRC value with the value in the RBCRC register and output the comparison result.

The working clock of GTP_RBCRC comes from OSC, supporting up to 33.25MHz, with a default clock frequency of 2.08MHz, which can be configured through PDS software, as shown in the figure below. At the same time, it is necessary to select the 2nd and 5th options on the [Readback] page. The 2nd option shields the initialisation data of distributed RAM, preventing it from participating in CRC calculations; the 5th option enables the OSC clock.

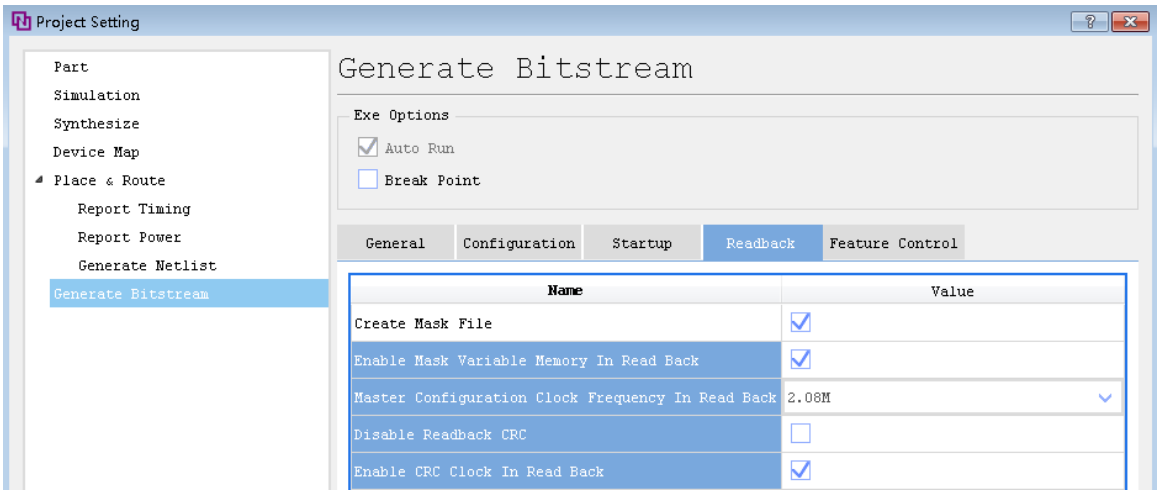

Figure 9-2 GTP_RBCRC Working Clock Frequency Configuration Diagram

9.6.2 Port Description

Table 9-9 GTP_RBCRC Port Description

Port	Direction	Function Description
RST	Input	Readback CRC reset signal, active high, used to reset the readback CRC error flag and clear the readback CRC initial value; the module cannot work when RST and START are both active; reset operation can only be performed before the start and after the end of readback CRC, rather than during the readback CRC process (from START going high to VALID going high).
START	Input	Readback CRC starts, active high; the START signal is invalid during the readback CRC process. A new readback CRC can only be started after one readback cycle is completed
ERR	Output	Readback CRC error flag, active high
VALID	Output	Readback CRC information valid flag, active high, indicating readback CRC error flag validity and readback completion
SEC_START	Input	Readback CRC correction initiation, active high; SEC_START is invalid when there is no readback CRC error. A new readback CRC correction can only be started after the previous readback correction is completed
SEC_OVER	Output	Readback CRC correction completion flag, active high, indicating the completion of readback CRC correction

9.6.3 Functional Description

GTP_RBCRC is typically used in soft error correction applications. The readback CRC functionality is initiated by taking the START signal high, and after several clock cycles, the VALID signal is taken high, indicating that readback CRC is complete. At this point, the user can check the ERR signal; if ERR is high, soft error correction can be initiated by taking SEC_START high, and after several clock cycles, SEC_OVER goes high for one cycle, indicating soft error correction is complete and CRAM is refreshed; if ERR is low, even if SEC_START is taken high, the soft error correction function will not be initiated. It should be noted that after soft error correction is completed, the readback CRC error flag must be cleared using RST. The timing diagram is shown in the figure below.

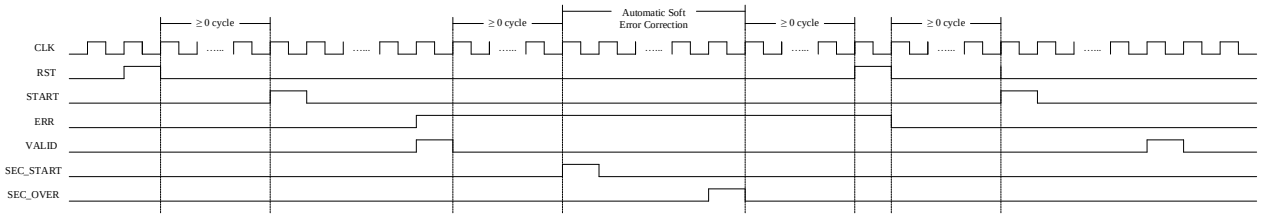

Figure 9-3 GTP_RBCRC Timing Diagram

9.6.4 Instantiation template

```
GTP_RBCRC GTP_RBCRC_inst(
    .CLK            (CLKCRC),
    .RST            (RST ),
    .START          (START),
    .ERR            (ERR),
    .VALID          (VALID),
    .SEC_START      (SEC_START),
    .SEC_OVER       (SEC_OVER)
);
```

9.7 GTP_APB

9.7.1 Description of Functionality

GTP_APB can be mapped as an APB bus interface within the chip, allowing the user to perform read and write operations on SPI core, I2C core, TIMER core, and embedded flash. The structure block diagram is shown below.

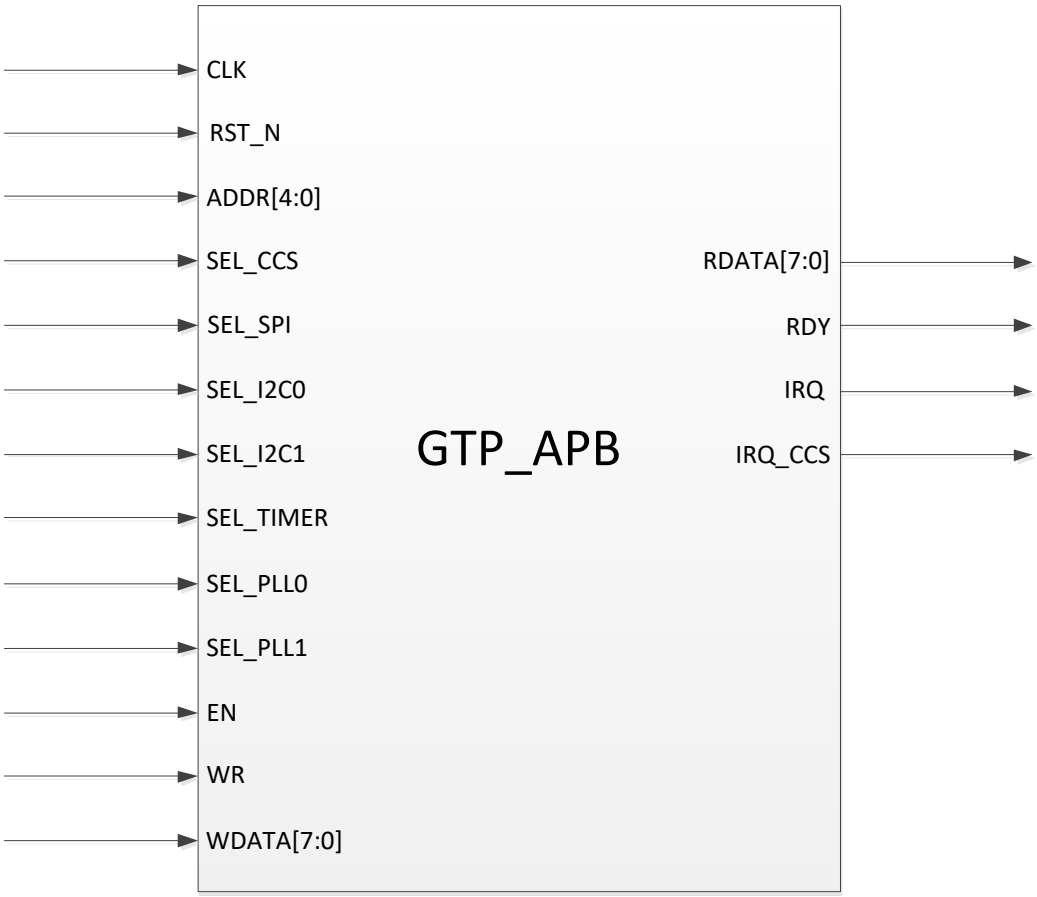

Figure 9-4 GTP_APB Structure Block Diagram

9.7.2 Port Description

Table 9-10 GTP_APB Port Description

Port	Direction	Function Description
CLK	Input	Clock, sampling on the rising edge, with a maximum frequency of 100MHz
RST_N	Input	Asynchronous reset, active low
ADDR[4:0]	Input	Address Bus
SEL_CCS	Input	Select CCS, active high
SEL_SPI	Input	Select SPI, active high
SEL_I2C0	Input	Select I2C0, active high
SEL_I2C1	Input	Select I2C1, active high
SEL_TIMER	Input	Select timer, active high
SEL_PLL0	Input	Select PLL0, active high
SEL_PLL1	Input	Select PLL1, active high
EN	Input	Enable, indicating the second and subsequent cycles of transmission, active high
WR	Input	Read/Write select. 1'b0: read; 1'b1: write
WDATA[7:0]	Input	Data bus input
RDATA[7:0]	Output	Data bus output

Port	Direction	Function Description
RDY	Output	Ready, indicating the end of a normal operation
IRQ	Output	Master interrupt
IRQ_CCS	Output	CCS interrupt

9.7.3 Functional Description

For detailed usage instructions and timing diagrams of GTP_APB, please refer to "***UG030007_Compa Family CPLD Embedded Hard Core User Guide***".

9.7.4 Instantiation template

Since the parameters of GTP_APB are only used for simulation, these parameters do not need to be invoked during instantiation of GTP_APB, nor do they affect actual function.

```
GTP_APB    GTP_APB_inst
(
        .CLK            (clk      ),
        .RST_N      (rst_sys_n    ),
        .ADDR           (addr         ),
        .SEL_CCS        (sel_ccs ),
        .SEL_SPI        (sel_spi  ),
        .SEL_I2C0       (sel_i2c0     ),
        .SEL_I2C1       (sel_i2c1     ),
        .SEL_TIMER      (sel_timer    ),
        .SEL_PLL0   (sel_pll0),
        .SEL_PLL1       (sel_pll1    ),
        .EN         (en       ),
        .WR             (wr       ),
        .WDATA          (wdata    ),
        .RDATA          (rdata        ),
        .RDY            (rdy          ),
        .IRQ            (irq      ),
        .IRQ_CCS        (irq_ccs      )
);
```

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