Logos Family PGL50G Device Configurable Multi-function PINs Application Guide

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.0	27.11.2022	Initial release.

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Chapter 1 Overview

A configurable Multi-function PIN can be used as a configuration interface during the configuration, and after the completion of the configuration, it can be used as a standard IO for the user in user mode. Some considerations on using a configurable Multi-function PIN as a user IO shall be taken into account in the single board design. The configurable multi-function PINs are all on Bank0, Bank1, or Bank2. See details in Table 2-1 and Table 2-2. So there is no need to consider the application of configurable multi-function IOs in other banks.

Configurable multi-function PINs must be used with the considerations in mind to avoid the following problem scenario: When reconfiguring the FPGA by resetting it in user mode and using a configurable multi-function PIN as an output for user logic, then after resetting, the multi-function PIN output will be in a non-high impedance state for a brief period (less than 100ns) (some PINs at a high level and some at a low level) and not controlled by IO_STATUS_C.

The process is shown in the following figure:

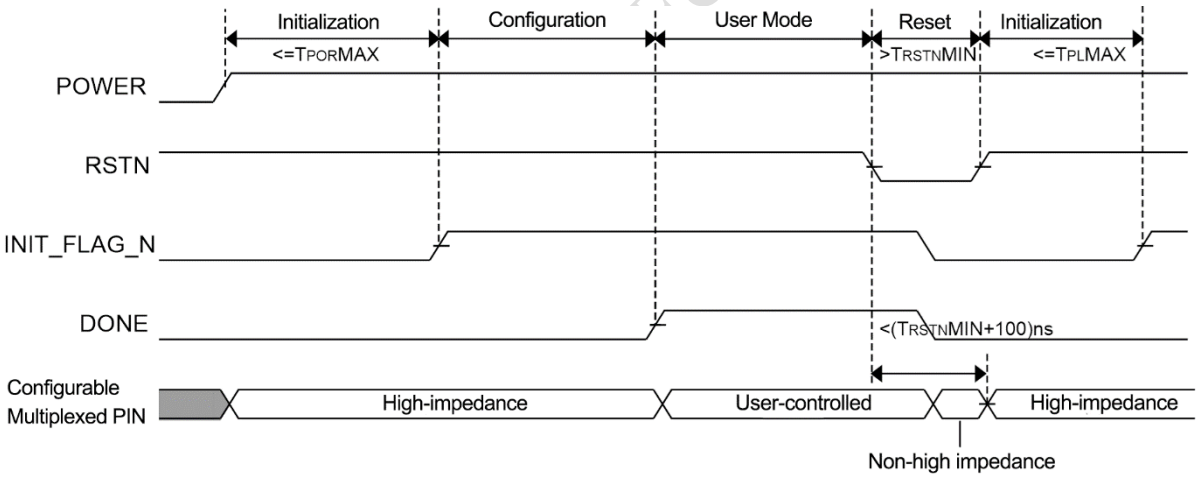

Figure 1-1 Non-High Impedance Process Diagram

For parameters in Figure 1-1, see "***DS02001_Logos Family FPGA Device Datasheet***" under the Chapter "Power-up Timing Characteristics".

This scenario mainly affects applications that require IO to maintain a fixed level during the reconfiguration process. For example, a configurable multi-function PIN is used as the enable or reset signal for other devices, and an external pull-up (or pull-down) of the FPGA is applied to keep the signal level stable during the configuration. In this case, it is expected that after the FPGA is reset, the configurable multi-function PIN output will be in a high impedance state, but the existence of the non-high impedance process may cause changes to the enable or reset signal, affecting the operation of other devices.

The possible triggers include:

1. Resetting FPGA in user mode
2. When resetting the FPGA, a configurable multi-function PIN is used as a user output.

The following solutions are provided for single board design for this scenario.

Chapter 2 Requirements for Single Board Design

The design requirements are the following:

1. If a configurable multi-function PIN is used as an input in user mode, it will not affect the design.
2. If a configurable multi-function PIN is used as an output in user mode, the following considerations shall be observed.
   1) Pin IO_STATUS_C requires an external pull-up.
   2) If the configurable multi-function PIN used needs to be maintained at a fixed level during the configuration, select a pin using the following method: For a fixed high level, choose a pin from Table 2-1 and apply an external pull-up (A pull-up resistor of 4.7K is recommended); for a fixed low level, choose one from Table 2-2 and apply an external pull-down (A pull-down resistor of 4.7K is recommended). If the rules of Table 1 and Table 2 are not followed, the configurable multi-function PIN output may be abnormal.
      For example: When using PGL50G-MBG324, if a signal needs to remain at a high level during the reconfiguration, users can choose pins such as L17(BFCS_N) and L18(BFOE_N) and apply an external pull-up; if a signal needs to remain at a low level during the reconfiguration, users can choose F15(ADR25), F16(ADR24), etc. and apply an external pull-down.
      If there is no need for the FPGA to maintain a fixed level during the reconfiguration, no action is required.

Table 2-1 Configurable Multi-function PINs that Can Remain at a High Level During Configuration

Bank Name	Pin Name (Function name)	Pin Number			
		MBG324	FBG484	MBG484	FBG676
B1	DIFFI_B1_31P/BFCS_N	L17	M21	N19	T24
B1	DIFFI_B1_31N/BFOE_N	L18	M22	M20	T26
B1	DIFFI_B1_32P/BFWE_N	M16	N20	N20	Y24
B1	DIFFI_B1_32N/BLDC	M18	N22	N22	Y26
B1	DIFFI_B1_33P/BHDC	N17	P21	P21	AD24
B2	DIFFIO_B2_1N/CSO_N	V3	T5	AB5	AF4
B2	DIFFIO_B2_15N/RWSEL/VREF_B2	T5	AB7	AB9	AF9
B2	DIFFIO_B2_26N/GCLK0/PLL4_CLK8/PLL5_CLK8/ECCLK	V10	AB13	AB12	AF13
B2	DIFFIO_B2_38P/MODE1	N12	U15	U15	AD16
B2	DIFFIO_B2_54N/MODE0/CMPMISO_2	T15	AA22	Y18	AF22
B2	DIFFIO_B2_54P/CFG_CLK	R15	Y21	W17	AD22

Table 2-2 Configurable Multi-function PINs that Can Remain at a Low Level During Configuration

Bank Name	Pin Name (Function name)	Pin Number			
		MBG324	FBG484	MBG484	FBG676
B1	DIFFI_B1_0P/ADR25	F15	C19	F15	B23
B1	DIFFI_B1_0N/ADR24/VREF_B1	F16	B20	F16	A23
B1	DIFFI_B1_14P/ADR23	C17	D19	F21	L23
B1	DIFFI_B1_14N/ADR22	C18	D20	F22	L24
B1	DIFFI_B1_15P/ADR21	F14	F18	H19	P20
B1	DIFFI_B1_15N/ADR20	G14	F19	H20	N21
B1	DIFFI_B1_16P/ADR19	D17	D21	E20	M23
B1	DIFFI_B1_16N/ADR18	D18	D22	E22	N24
B1	DIFFI_B1_17P/ADR17	H12	C20	G20	L17
B1	DIFFI_B1_17N/ADR16	G13	C22	G22	K18
B1	DIFFI_B1_18P/ADR15	E16	G19	D21	P24
B1	DIFFI_B1_18N/ADR14	E18	F20	D22	P26
B1	DIFFI_B1_19P/ADR13	K12	H19	H21	M19
B1	DIFFI_B1_19N/ADR12	K13	H18	H22	L18
B1	DIFFI_B1_20P/ADR11	F17	E20	C20	R25
B1	DIFFI_B1_20N/ADR10	F18	E22	C22	R26
B1	DIFFI_B1_21P/ADR9	H13	J17	K18	M18
B1	DIFFI_B1_21N/ADR8	H14	K17	K19	N19
B1	DIFFI_B1_22P/ADR7	H15	F21	B21	N22
B1	DIFFI_B1_22N/ADR6	H16	F22	B22	N23
B1	DIFFI_B1_23P/ADR5	G16	H20	J17	N17
B1	DIFFI_B1_23N/ADR4	G18	J19	J19	N18
B1	DIFFI_B1_29P/ADR3/XTAL_A	J16	K21	K21	W25
B1	DIFFI_B1_29N/ADR2/XTAL_B	J18	K22	K22	W26
B1	DIFFI_B1_30P/ADR1	K17	L20	M21	V24
B1	DIFFI_B1_30N/ADR0	K18	L22	M22	V26
B1	DIFFI_B1_55N/DOUT_BUSY	P16	T20	T20	AF24
B2	DIFFIO_B2_1P/INIT_FLAG_N	U3	T6	Y5	AE4
B2	DIFFIO_B2_2N/D9	P6	AB2	AB6	AF5
B2	DIFFIO_B2_2P/D8	N5	AA2	AA6	AE5
B2	DIFFIO_B2_4N/D6	T3	Y4	Y6	AF7
B2	DIFFIO_B2_4P/D5	R3	W4	W6	AE7
B2	DIFFIO_B2_14N/D4	V5	AB6	AB8	AF10
B2	DIFFIO_B2_14P/D3	U5	AA6	AA8	AD10
B2	DIFFIO_B2_15P/D7	R5	Y7	Y9	AE9
B2	DIFFIO_B2_25N/GCLK30/PLL4_CLK6/PLL5_CLK6/D15	T8	AB12	AB11	AD13
B2	DIFFIO_B2_25P/GCLK31/PLL4_CL	R8	AA12	Y11	AC13

Bank Name	Pin Name (Function name)	Pin Number			
		MBG324	FBG484	MBG484	FBG676
	K7/PLL5_CLK7/D14				
B2	DIFFIO_B2_26P/GCLK1/PLL4_CLK9/PLL5_CLK9/D13	U10	Y13	AA12	AE13
B2	DIFFIO_B2_37N/D12	V13	AB18	Y16	AF15
B2	DIFFIO_B2_37P/D11	U13	AA18	W15	AE15
B2	DIFFIO_B2_38N/D10	P12	V15	V15	AF16
B2	DIFFIO_B2_39N/D2	V14	U13	W13	AF17
B2	DIFFIO_B2_39P/D1	T14	U14	V13	AE17
B2	DIFFIO_B2_52N/CS_N	T13	AB20	AB17	AF20
B2	DIFFIO_B2_52P/D0	R13	AA20	Y17	AD20

Users must verify based on the application to ensure that the pin meets application requirements at each stage.

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