PG2L100H_MBG324

(PK04002, V1.3)

(07.13.2023)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.3	07.13.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Full Spelling
POD	Package Outline Drawing

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Chapter 1 Introduction to Packaging

PG2L100H_MBG324 uses a Wire-Bond BGA type of packaging. Package size: 15mmx15mm; Number of balls: 324; Ball pitch: 0.8mm; Maximum package thickness: 1.5mm.

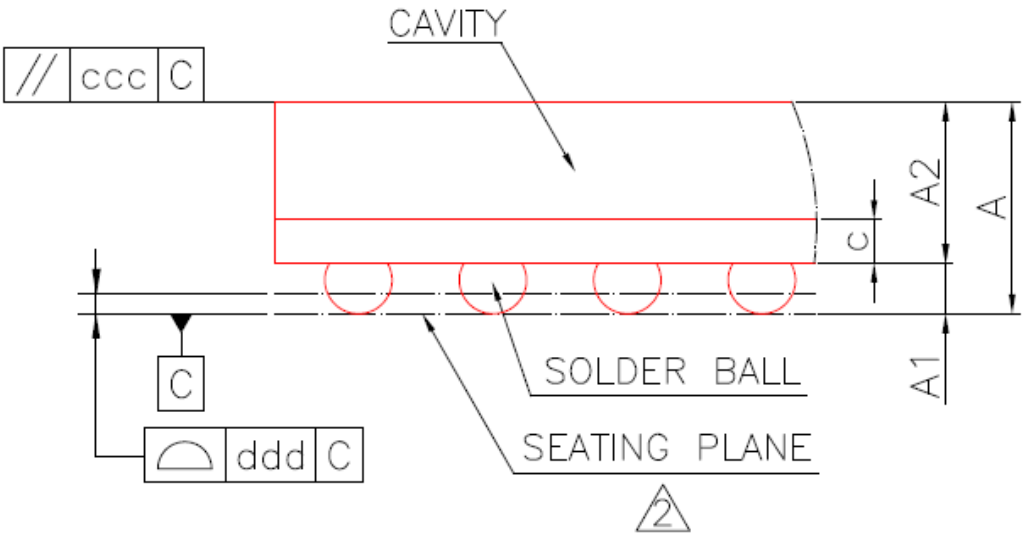
Chapter 2 Package Dimension and PIN Definitions

2.1 Package Dimension

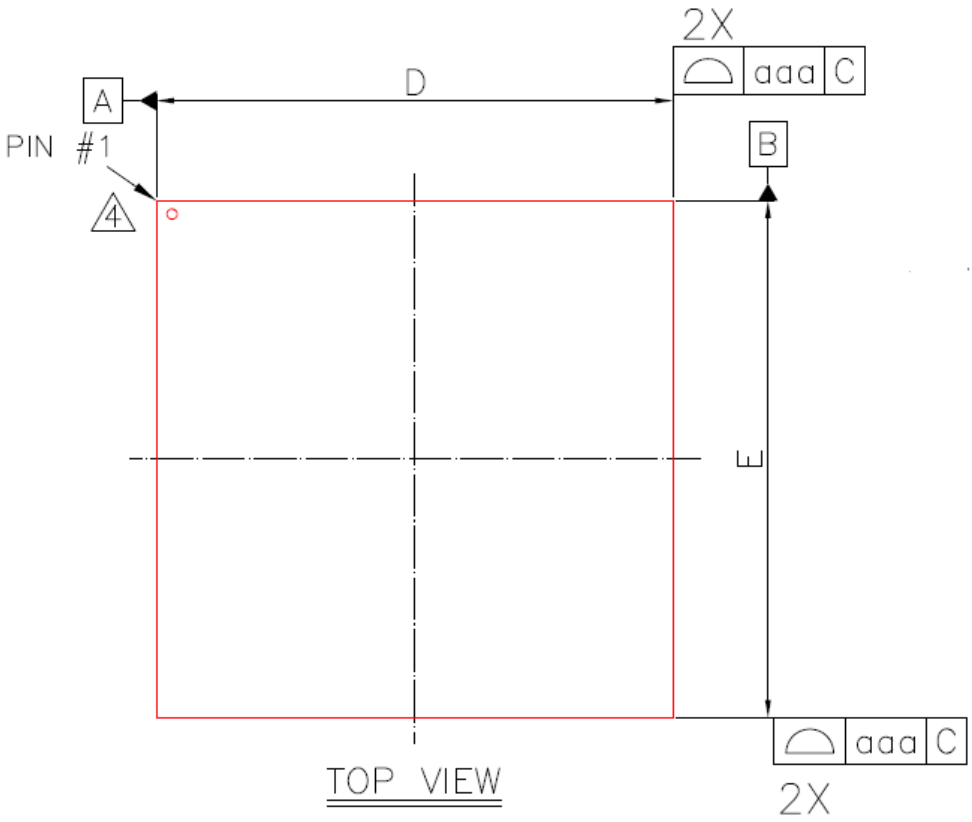
Table 2-1 Dimensional Values

Note: Unit in millimeter

Dimension Symbol	Value			Dimension Symbol	Value		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	-	-	1.5	c	0.22	0.26	0.30
A1	0.29	0.34	0.39	e	-	0.8	-
A2	0.91	0.96	1.01	b	0.40	0.45	0.50
D	14.9	15.0	15.1	aaa	-	-	0.15
E	14.9	15.0	15.1	ccc	-	-	0.15
D1	-	13.6	-	ddd	-	-	0.20
E1	-	13.6	-	eee	-	-	0.15


CAVITY
ccc C
A2
A
c
A1
C
SOLDER BALL
ddd C
SEATING PLANE
2

DETAIL : "A"


2X
aaa C
D
A
PIN #1
4
B
E
aaa C
2X
TOP VIEW

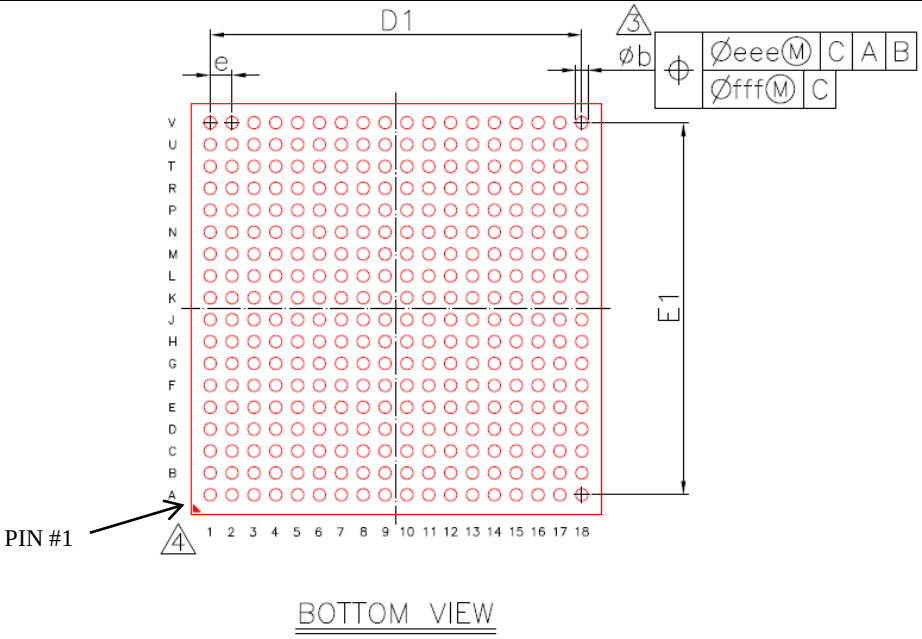


Figure 2-1 Package Outline Dimension (POD)

Note: Pin #1 is the pin 1 position of the chip.

2.2 Pin Definitions

PG2L100H_ MBG324 has 210 user IOs.

Table 2-1 Product Pin Definitions

PIN Name	PIN Type	PIN Direction	PIN Description
General PIN			
DIFFIO_XX_GY_NN[P,N]	General	Input/Output	General pin; (1) "DIFFIO" indicates the pin supports differential input/output and can be used for transmitting and receiving LVDS signals; (2) " XX " indicates bank numbers, which can be L3, L4, L5, R4, R5; (3) " G " indicates belonging to a memory group; (4) " Y " indicates the group number in a bank, each of which contains four groups; (5) "NN" indicates the sequence number of programmable IO pairs in a bank, increasing from 0, a bank contains 24 difference pairs; (6) In "[N,P]", "P" indicates the positive end of the differential pair and "N" indicates the negative end; (7) During initialization (clear configuration memory), all general pins remain in Tri-state, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors. (8) During configuration, all general pins remain in Tri-state except those need to be used for the multiplexed configuration IOs, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors.
SIO_XX_NN	General	Input/Output	General pin; (1) " SIO " indicates the pin only supports single ended input/output; (2) " XX " indicates bank numbers, which can be L3, L4, L5, R4, R5; (3) "NN" indicates the sequence number of programmable IO in a bank, increasing from 0, a bank contains 2 single ended IOs; (4) During initialization (clear configuration memory), all general pins remain in Tri-state, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors. (5) During configuration, all general pins remain in Tri- state except those need to be used for the multiplexed configuration IOs, if IO_STATUS_C pin is low level, enable internal weak pull-up resistors.
Configuration PIN			
INIT_FLAG_N	Dedicated	Bidirectional (open-drain)	(1)Initialization and configuration status dedicated pin. When it is low, it indicates that the FPGA is being initialized (clear configuration memory) or a configuration error has occurred. The pin has an internal weak pull-up resistor that is enabled during configuration;

PIN Name	PIN Type	PIN Direction	PIN Description
			(2) When the FPGA powers up completion, the pin is driven to low level. Once the FPGA completes initialization, the pin is released. During the power up and initialization process, this pin can accept an external low level input to delay the configuration process. When the FPGA detects high level input on this pin after initialization, the FPGA starts the configuration process.During configuration, this pin serves as an output for the configuration error indication state, low level indicates that an error occurred. (3) This pin should be connected to VCCIOCFG via an external weak pull-up resistor of no more than 4.7K.
CFG_DONE	Dedicated	Bidirectional (open-drain)	(1) Dedicated configuration status pin, built in weak pull-up resistor about 10K. (2) Output as the configuration completion indicator, high level indicates that the configuration is complete. This pin is an open-drain output. When the FPGA powers up completion, the pin is driven to low level before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released. (3) After the configuration is complete, the pin can be driven externally to low level to delay the chip wake up. (4) This pin should be connected to VCCIOCFG via an external weak pull-up resistor (recommended resistance value: 1KΩ~4.7KΩ).
RSTN	Dedicated	Input	(1).Dedicated configuration reset pin, built in weak pull-up resistor and always effective. (2) For restarting configuration logic and configuration memory, active-low. (3) This pin should be connected to VCCIOCFG via an external weak pull-up resistor (recommended resistance value: 1KΩ~4.7KΩ).
CFG_CLK	Dedicated	Input/Output	(1) Configuration clock pin. Except for the JTAG configuration mode, the configuration process of the FPGA is synchronize by this clock in other modes. (2) In the slave serial and slave parallel configuration modes, the pin serves as a clock input to obtain configuration data from external sources. (3) In the master SPI configuration mode, the pin serves as a clock output to obtain configuration data from external sources and an external pull-up resistor of 1K is required.
TCK	Dedicated	Input	(1) Dedicated JTAG test clock input pin. (2) Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TMS	Dedicated	Input	(1) Dedicated JTAG test mode selection input pin. (2) Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TDI	Dedicated	Input	(1) Dedicated JTAG test data input pin.

PIN Name	PIN Type	PIN Direction	PIN Description
			(2) Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
TDO	Dedicated	Output	(1) Dedicated JTAG test data output pin (2) Internal weak pull-up resistor is connected to VCCIOCFG and always effective.
MODE_2	Dedicated	Input	(1) Dedicated configuration pin, used for selecting configuration modes. (2) This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
MODE_1	Dedicated	Input	(1) Dedicated configuration pin, used for selecting configuration modes. (2) This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
MODE_0	Dedicated	Input	(1) Dedicated configuration pin, used for selecting configuration modes. (2) This pin should be connected to VCCIOCFG via an external pull-up resistor of no more than 1K, or connected to VSS via an external pull-down resistor of no more than 1K.
SCBV	Dedicated	Input	(1) The pin is always effective on BANKCFG, but only on BANK which the multiplexing configuration pins are located during configuration. (2) When the voltage of VCCIOCFG is 2.5V or 3.3V, the pin must be connected to high level and can be connected directly to the VCCIOCFG. When the voltage of VCCIOCFG is 1.8V or lower, the pin must be connected to low level and can be connected directly to the ground. Note: The pin must be used in conjunction with the software, and the SCBV selection in the bitstream setting must be consistent with the hardware setting. For details about the SCBV pin pull-up/pull-down level corresponds to the configured BANK power, see UG040012_Logos2 Family Hardware Design Guide.
FCS_N	Multiplexed	Output	Multi-function configuration pin, used for the Master SPI configuration mode. (1) In the Master SPI X1, X2 and X4 modes, this pin outputs a chip select signal to external flash, active-low. And should be connected to VCCIO via an external pull-up resistor of no more than 4.7K. (2) In the Master SPI X8 mode, this pin outputs a chip select signal to external low 4-bits data corresponding to the flash, active-low. And should be connected to VCCIO via an external pull-up resistor of no more than 4.7K. (3) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state.

PIN Name	PIN Type	PIN Direction	PIN Description
			(4) After the configuration is complete, the pin serves as a general pin.
MOSI_D0	Multiplexed	Input/Output	Multi-function configuration data pin. (1) "MOSI", in the master SPI X1 mode, this pin used for serial data output and connects to the data input pin of the external SPI flash (such as DQ0,D, SI,IO0, etc). After the command and address are sent to the external SPI flash, the pin output high-Z or weak pull-up, depending on the state of the IO_STATUS_C pin. (2) In the master SPI X2, X4 and X8 modes, the pin is bidirectional data port, as command and address output to the external SPI flash. Receive the lowest bit data from the external SPI flash. The pin connects to the bidirectional data pin of the external SPI flash (such as DQ0,D,SI,IO0, etc). (3) " D0", in the slave parallel mode, this pin serves as the D[0] bit of the data bus. (4) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state. (5) After the configuration is complete, the pin serves as a general pin.
MISO_D1_DI	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X1 mode, "MISO" serves as data input and connects to the data output pin of the external SPI flash (such as DQ1,Q,SO,IO1, etc). (2) In the master SPI X2, X4 and X8 modes, "D1" connects to the second serial data output pin of the external SPI flash (such as DQ1,Q,SO,IO1, etc). (3) In the slave parallel mode, this pin serves as the D[1] bit of the data bus. (4) In the slave serial mode, "D1" serves as data input pin . (5) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state. In the other configuration mode(such as JTAG), the state on the pin is ignored (6) After the configuration is complete, the pin serves as a general pin.
D[2, 3]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X4 and X8 modes, serve as data input and connects to the data output pin of the external SPI flash. "D2" connects to the third bit data output pin of the external SPI flash(such as DQ2,W#,WP#,IO2, etc). "D3" connects to the fourth bit data output pin of the external SPI flash(such as DQ3,HOLD#, IO3, etc). These pins should be connected to VCCIO via an external weak pull-up resistor of 4.7K. (2) In the slave parallel mode, these pins serve as the D[3:2] bits of the data bus. (3) In the other configuration modes or in initialization process, these pins act as general pins in a high-Z or weak pull-up state.

PIN Name	PIN Type	PIN Direction	PIN Description
			(4) After the configuration is complete, these pins serve as general pins.
D[4, 5, 6, 7]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the master SPI X8 mode, connect to the second flash in the same way as D[3:0]. (2) In the slave parallel mode, these pins serve as the D[7:4] bits of the data bus. (3) In the other configuration modes or in initialization process, these pins act as general pins in a high-Z or weak pull-up state. (4) After the configuration is complete, these pins serve as general pins.
D[8,…,15]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the slave parallel X16 and X32 modes, serve as the D[15:8] bits of the data bus. (2) In the other configuration modes, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (3) After the configuration is complete, these pins serve as general pins.
D[16,…,31]_A[0,…,15]	Multiplexed	Input/Output	Multi-function configuration data pin. (1) In the slave parallel X32 mode, serve as the D[31:16] bits of the data bus. (2) In the other configuration modes, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (3) After the configuration is complete, these pins serve as general pins.
A[16,…,28]	Multiplexed	Output	Multi-function configuration pin. (1) During initialization, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (2) After the configuration is complete, these pins serve as general pins.
CS_N	Multiplexed	Input	Multi-function configuration pin. For chip select input. Active low. (1) When it is low level, this pin enables the slave parallel mode configuration interface. In the slave parallel configuration mode, the external controller can select the slave parallel bus of the FPGA by controlling this pin. Or this pin connected to the previous FPGA CSO_DOUT pin in the slave parallel configuration chain. (2) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state. (3) After the configuration is complete, the pin serves as a general pin.
RWSEL	Multiplexed	Input	Multi-function configuration pin. For selecting the read/write input in the slave parallel configuration mode (high for read and low for write). (1) When it is high level, the slave parallel configuration mode reads data from the data bus. (2) When it is low level, the slave parallel configuration mode writes data to the data bus. (3) Read and write can be switched only when

PIN Name	PIN Type	PIN Direction	PIN Description
			CS_N is high level. (4) After the configuration is complete, the pin serves as a general pin. (5) In the other configuration modes or in initialization process, the pin act as a general pin in a high-Z or weak pull-up state.
CSO_DOUT	Multiplexed	Output	Multi-function configuration pin. Needed for cascade. (1) In the master SPI X1 mode, this pin serves as cascaded data output. (2) In the slave serial configuration mode, this pin serves as cascaded data output. (3) In the slave parallel cascade configuration mode, this pin serves as a chip select signal open-drain output, connects to downstream chip CS_N pin and should be connected to VCCIO via an external pull-up resistor of 330Ω. (4) In the other configuration modes, the pin act as a general pin.
VS[0, 1]	Multiplexed	Output	Multi-function configuration pin. (1) During initialization, these pins not be used and serve as general pins in a high-Z or weak pull-up state. (2)After the configuration is complete, these pins as general pins.
IO_STATUS_C	Multiplexed	Input	Multi-function configuration pin, used for controlling whether the weak pull-up resistors for all general pins are enabled during the configuration process. . (1) When it is set to "0", the internal pull-up resistors for all general pins are enabled. (2) When it is set to "1", the internal pull-up resistors for all general pins are disabled. (3) It is recommended that the pin connects to VCCIO or VSS via an external resistor of no more than 1K.. (5) This pin must not be left floating before or during configuration.
ECCLKIN	Multiplexed	Input	The external clock input for the Master configuration mode, which is an optional external clock input to the configuration logic. (1) In the master SPI mode, the FPGA can select this clock input as the configuration clock for the configuration logic. This clock can be divided (Depends on the settings in the bitstream) and output from the CFG_CLK pin. (2) In the other configuration modes, the pin act as a general pin.
BFOE_N	Multiplexed	Output	Multi-function configuration pin. (1) During initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (2)After the configuration is complete, the pin as a general pin.
BFWE_ FCS2_N	Multiplexed	Output	Multi-function configuration pin. (1) In the Master SPI X8 mode, this pin outputs a

PIN Name	PIN Type	PIN Direction	PIN Description
			chip select signal to external high 4-bits data corresponding to the flash, active-low. And should be connected to VCCIO via an external pull-up resistor of no more than 4.7K. (2) In the other configuration modes, the pin act as a general pin.
BADRVO_N	Multiplexed	Output	Multi-function configuration pin. (1) During initialization, the pin not be used and serves as a general pin in a high-Z or weak pull-up state. (2)After the configuration is complete, the pin as a general pin.
Clock PIN			
GMCLK	Multiplexed	Input	Multiplexing global multi-regional clock input pins. These pins can directly drive the regional clock buffer, IO clock buffer, global clock buffer, GPLL, PPLL, and also drive the multi-regional clock buffer. When not used as clock input, these pins serve as general pins, and when the differential pair is connected to a single ended clock source, only the positive end of the differential pair needs to be connected. When these pins serve as single regional clock sources, they are able to drive all the IO clock buffers and regional clock buffers of the BANK.
GSCLK	Multiplexed	Input	Multiplexing global single regional clock input pins. These pins can directly drive the regional clock buffer, IO clock buffer, global clock buffer, GPLL and PPLL. When not used as clock input, these pins serve as general pins, and when the differential pair is connected to a single ended clock source, only the positive end of the differential pair needs to be connected. They are able to drive all the IO clock buffers and regional clock buffers of the BANK.
Memory Interface PIN			
DQS	Multiplexed	N/A	DDR DQS PIN, each memory group contains two pins.
Reference PIN			
VREF	Multiplexed	N/A	Input reference voltage pins,. When not used as external reference voltage pins, these pins serve as general pins,
Power/ Ground PIN			
VCC	Dedicated	N/A	Core logic power, 1.0V. Power supply for core logic.
VCC_DRM	Dedicated	N/A	DRM power, 1.0V. Dedicated power supply for DRM. If the voltage is the same as VCC, it can be connected to VCC at the board.
VCCA	Dedicated	N/A	Analog power, 1.8V. Power supply for internal analog circuit.
VCCIO_[L3, L4, L5, R4, R5, CFG]	Dedicated	N/A	IO BANK power.
VCCB	Dedicated	N/A	Key memory backup battery power supply voltage, 1.0V~1.9V. When the key function is not used, the pin needs to

PIN Name	PIN Type	PIN Direction	PIN Description
			be connected to the VCCA or ground.
VSS	Dedicated	N/A	Ground
ADC PIN			
VCCADC	Dedicated	N/A	ADC analog power, 1.8V. Power supply for ADC analog circuit.
VSSADC	Dedicated	N/A	GND relative to VCCADC
VAADC_P	Dedicated	Input	ADC dedicated analog differential input (Positive).
VAADC_N	Dedicated	Input	ADC dedicated analog differential input (Negative).
VREFADC_P	Dedicated	N/A	1.255V ADC reference voltage pin.
VREFADC_N	Dedicated	N/A	ADC reference voltage ground.
VAA[0,..,15]P,VAA[0,..,15]N	Multiplexed	Input	ADC differential analog input signals.
TSDP	Dedicated	N/A	Positive pin of the temperature sensor diode. When not used temperature diode, the pin needs to be connected to the VSS. When temperature sensor diode is to be used, then appropriate external temperature monitoring chip is required.
TSDN	Dedicated	N/A	Negative pin of the temperature sensor diode.

2.2.1 Pin Name List

Table 2-2 Pin Name List

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L3	DIFFIO_L3_G0_05N_VREF	D9		112.061	
L3	DIFFIO_L3_G1_10P_GSCLK	C9	IO_11_P	134.168	
L3	DIFFIO_L3_G1_10N_GSCLK	B9	IO_11_N	132.238	
L3	DIFFIO_L3_G1_11P_GMCLK	B8	IO_12_P	108.662	
L3	DIFFIO_L3_G1_11N_GMCLK	A8	IO_12_N	103.828	
L3	DIFFIO_L3_G2_12P_GMCLK	C11	IO_13_P	100.877	
L3	DIFFIO_L3_G2_12N_GMCLK	C10	IO_13_N	99.0872	
L3	DIFFIO_L3_G2_13P_GSCLK	A10	IO_14_P	90.4016	
L3	DIFFIO_L3_G2_13N_GSCLK	A9	IO_14_N	92.0458	
L3	DIFFIO_L3_G3_18N_VREF	D10	IO_19_N	105.528	
L4	SIO_L4_00	G13		31.6097	
L4	DIFFIO_L4_G0_00P_VAA1P	D14	IO_25_P	79.5754	L4_G0
L4	DIFFIO_L4_G0_00N_VAA1N	C14	IO_25_N	81.825	L4_G0
L4	DIFFIO_L4_G0_01P_VAA2P	B13	IO_26_P	68.8907	L4_G0
L4	DIFFIO_L4_G0_01N_VAA2N	B14	IO_26_N	71.7473	L4_G0
L4	DIFFIO_L4_G0_02P_DQS_VAA3P	C12	IO_27_P	105.391	L4_G0_DQS
L4	DIFFIO_L4_G0_02N_DQS_VAA3N	B12	IO_27_N	108.819	L4_G0_DQS
L4	DIFFIO_L4_G0_03P	B11	IO_28_P	85.8649	L4_G0
L4	DIFFIO_L4_G0_03N	A11	IO_28_N	86.5368	L4_G0
L4	DIFFIO_L4_G0_04P_VAA5P	F13	IO_29_P	81.7682	L4_G0
L4	DIFFIO_L4_G0_04N_VAA5N	F14	IO_29_N	80.8126	L4_G0
L4	DIFFIO_L4_G0_05P	D12	IO_30_P	68.7368	L4_G0
L4	DIFFIO_L4_G0_05N_VREF	D13	IO_30_N	62.9635	L4_G0
L4	DIFFIO_L4_G1_06P_VAA7P	B16	IO_31_P	87.7328	L4_G1
L4	DIFFIO_L4_G1_06N_VAA7N	B17	IO_31_N	90.5677	L4_G1
L4	DIFFIO_L4_G1_07P_VAA8P	A15	IO_32_P	72.2239	L4_G1
L4	DIFFIO_L4_G1_07N_VAA8N	A16	IO_32_N	73.7992	L4_G1
L4	DIFFIO_L4_G1_08P_DQS_VAA9P	A13	IO_33_P	118.499	L4_G1_DQS
L4	DIFFIO_L4_G1_08N_DQS_VAA9N	A14	IO_33_N	118.225	L4_G1_DQS
L4	DIFFIO_L4_G1_09P_VAA10P	B18	IO_34_P	97.1573	L4_G1
L4	DIFFIO_L4_G1_09N_VAA10N	A18	IO_34_N	94.5929	L4_G1
L4	DIFFIO_L4_G1_10P_GSCLK	E15	IO_35_P	87.3126	L4_G1
L4	DIFFIO_L4_G1_10N_GSCLK	E16	IO_35_N	82.2688	L4_G1
L4	DIFFIO_L4_G1_11P_GMCLK	D15	IO_36_P	64.5261	L4_G1
L4	DIFFIO_L4_G1_11N_GMCLK	C15	IO_36_N	68.9786	L4_G1
L4	DIFFIO_L4_G2_12P_GMCLK	H16	IO_37_P	63.7261	L4_G2

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L4	DIFFIO_L4_G2_12N_GMCLK	G16	IO_37_N	63.1729	L4_G2
L4	DIFFIO_L4_G2_13P_GSCLK	F15	IO_38_P	58.3509	L4_G2
L4	DIFFIO_L4_G2_13N_GSCLK	F16	IO_38_N	53.4688	L4_G2
L4	DIFFIO_L4_G2_14P_DQS	H14	IO_39_P	84.6395	L4_G2_DQS
L4	DIFFIO_L4_G2_14N_DQS_BADRVO_N	G14	IO_39_N	83.729	L4_G2_DQS
L4	DIFFIO_L4_G2_15P_A28	E17	IO_40_P	68.0543	L4_G2
L4	DIFFIO_L4_G2_15N_A27	D17	IO_40_N	67.164	L4_G2
L4	DIFFIO_L4_G2_16P_A26	K13	IO_41_P	83.5663	L4_G2
L4	DIFFIO_L4_G2_16N_A25	J13	IO_41_N	83.8621	L4_G2
L4	DIFFIO_L4_G2_17P_A24	H17	IO_42_P	60.8562	L4_G2
L4	DIFFIO_L4_G2_17N_A23	G17	IO_42_N	62.4325	L4_G2
L4	DIFFIO_L4_G3_18P_A22	J14	IO_43_P	84.6986	L4_G3
L4	DIFFIO_L4_G3_18N_VREF_A21	H15	IO_43_N	90.0668	L4_G3
L4	DIFFIO_L4_G3_19P_A20	C16	IO_44_P	75.6686	L4_G3
L4	DIFFIO_L4_G3_19N_A19	C17	IO_44_N	75.1207	L4_G3
L4	DIFFIO_L4_G3_20P_DQS	E18	IO_45_P	83.161	L4_G3_DQS
L4	DIFFIO_L4_G3_20N_DQS_A18	D18	IO_45_N	85.9615	L4_G3_DQS
L4	DIFFIO_L4_G3_21P_A17	G18	IO_46_P	57.1071	L4_G3
L4	DIFFIO_L4_G3_21N_A16	F18	IO_46_N	60.8521	L4_G3
L4	DIFFIO_L4_G3_22P_BFOE_N	J17	IO_47_P	56.4323	L4_G3
L4	DIFFIO_L4_G3_22N_BFWE_FCS2_N	J18	IO_47_N	55.8313	L4_G3
L4	DIFFIO_L4_G3_23P_VS1	K15	IO_48_P	41.6973	L4_G3
L4	DIFFIO_L4_G3_23N_VS0	J15	IO_48_N	44.0118	L4_G3
L4	SIO_L4_01	K16		40.0028	
L5	SIO_L5_00	R11		79.206	
L5	DIFFIO_L5_G0_00P_MOSI_D0	K17	IO_49_P	53.9254	L5_G0
L5	DIFFIO_L5_G0_00N_MISO_D1_DI	K18	IO_49_N	55.133	L5_G0
L5	DIFFIO_L5_G0_01P_D2	L14	IO_50_P	52.9347	L5_G0
L5	DIFFIO_L5_G0_01N_D3	M14	IO_50_N	50.6691	L5_G0
L5	DIFFIO_L5_G0_02P_DQS_IO_STATUS_C	L15	IO_51_P	60.4504	L5_G0_DQS
L5	DIFFIO_L5_G0_02N_DQS_ECCLKIN	L16	IO_51_N	64.4349	L5_G0_DQS
L5	DIFFIO_L5_G0_03P_D4	L18	IO_52_P	53.6623	L5_G0
L5	DIFFIO_L5_G0_03N_D5	M18	IO_52_N	52.9668	L5_G0
L5	DIFFIO_L5_G0_04P_D6	R12	IO_53_P	102.337	L5_G0
L5	DIFFIO_L5_G0_04N_D7	R13	IO_53_N	102.835	L5_G0
L5	DIFFIO_L5_G0_05P_FCS_N	L13	IO_54_P	58.8273	L5_G0
L5	DIFFIO_L5_G0_05N_VREF_D8	M13	IO_54_N	56.4497	L5_G0
L5	DIFFIO_L5_G1_06P_D9	R18	IO_55_P	84.213	L5_G1
L5	DIFFIO_L5_G1_06N_D10	T18	IO_55_N	84.7207	L5_G1

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
L5	DIFFIO_L5_G1_07P_D11	N14	IO_56_P	58.1726	L5_G1
L5	DIFFIO_L5_G1_07N_D12	P14	IO_56_N	58.5154	L5_G1
L5	DIFFIO_L5_G1_08P_DQS_N	N17	IO_57_P	66.2576	L5_G1_DQS
L5	DIFFIO_L5_G1_08N_DQS_D13	P18	IO_57_N	65.5912	L5_G1_DQS
L5	DIFFIO_L5_G1_09P_D14	M16	IO_58_P	42.0641	L5_G1
L5	DIFFIO_L5_G1_09N_D15	M17	IO_58_N	46.3791	L5_G1
L5	DIFFIO_L5_G1_10P_GSCLK	N15	IO_59_P	71.6827	L5_G1
L5	DIFFIO_L5_G1_10N_GSCLK	N16	IO_59_N	71.2526	L5_G1
L5	DIFFIO_L5_G1_11P_GMCLK	P17	IO_60_P	50.7533	L5_G1
L5	DIFFIO_L5_G1_11N_GMCLK	R17	IO_60_N	52.9525	L5_G1
L5	DIFFIO_L5_G2_12P_GMCLK	P15	IO_61_P	75.7515	L5_G2
L5	DIFFIO_L5_G2_12N_GMCLK	R15	IO_61_N	78.2002	L5_G2
L5	DIFFIO_L5_G2_13P_GSCLK	T14	IO_62_P	64.3832	L5_G2
L5	DIFFIO_L5_G2_13N_GSCLK	T15	IO_62_N	65.167	L5_G2
L5	DIFFIO_L5_G2_14P_DQS_RWSEL	R16	IO_63_P	73.0403	L5_G2_DQS
L5	DIFFIO_L5_G2_14N_DQS_CSO_DOUT	T16	IO_63_N	71.3487	L5_G2_DQS
L5	DIFFIO_L5_G2_15P_CS_N	V15	IO_64_P	76.7472	L5_G2
L5	DIFFIO_L5_G2_15N_D31_A15	V16	IO_64_N	75.9603	L5_G2
L5	DIFFIO_L5_G2_16P_D30_A14	U17	IO_65_P	72.3321	L5_G2
L5	DIFFIO_L5_G2_16N_D29_A13	U18	IO_65_N	72.4011	L5_G2
L5	DIFFIO_L5_G2_17P_D28_A12	U16	IO_66_P	64.0738	L5_G2
L5	DIFFIO_L5_G2_17N_D27_A11	V17	IO_66_N	67.0525	L5_G2
L5	DIFFIO_L5_G3_18P_D26_A10	T11	IO_67_P	114.193	L5_G3
L5	DIFFIO_L5_G3_18N_VREF_D25_A9	U11	IO_67_N	115.766	L5_G3
L5	DIFFIO_L5_G3_19P_D24_A8	U12	IO_68_P	80.8451	L5_G3
L5	DIFFIO_L5_G3_19N_D23_A7	V12	IO_68_N	79.7261	L5_G3
L5	DIFFIO_L5_G3_20P_DQS	V10	IO_69_P	116.862	L5_G3_DQS
L5	DIFFIO_L5_G3_20N_DQS_D22_A6	V11	IO_69_N	119.601	L5_G3_DQS
L5	DIFFIO_L5_G3_21P_D21_A5	U14	IO_70_P	70.7302	L5_G3
L5	DIFFIO_L5_G3_21N_D20_A4	V14	IO_70_N	69.4537	L5_G3
L5	DIFFIO_L5_G3_22P_D19_A3	T13	IO_71_P	90.9777	L5_G3
L5	DIFFIO_L5_G3_22N_D18_A2	U13	IO_71_N	91.0005	L5_G3
L5	DIFFIO_L5_G3_23P_D17_A1	T9	IO_72_P	89.2385	L5_G3
L5	DIFFIO_L5_G3_23N_D16_A0	T10	IO_72_N	89.4551	L5_G3
L5	SIO_L5_01	R10		76.5904	
R4	SIO_R4_00	F5		26.7328	
R4	DIFFIO_R4_G0_00P_VAA4P	C6	IO_97_P	90.3097	R4_G0
R4	DIFFIO_R4_G0_00N_VAA4N	C5	IO_97_N	86.8476	R4_G0
R4	DIFFIO_R4_G0_01P_VAA6P	B7	IO_98_P	71.5097	R4_G0

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R4	DIFFIO_R4_G0_01N_VAA6N	B6	IO_98_N	74.0211	R4_G0
R4	DIFFIO_R4_G0_02P_DQS_VAA11P	A6	IO_99_P	95.8683	R4_G0_DQS
R4	DIFFIO_R4_G0_02N_DQS_VAA11N	A5	IO_99_N	97.229	R4_G0_DQS
R4	DIFFIO_R4_G0_03P	D8	IO_100_P	74.4627	R4_G0
R4	DIFFIO_R4_G0_03N	C7	IO_100_N	74.3004	R4_G0
R4	DIFFIO_R4_G0_04P_VAA12P	E6	IO_101_P	81.9312	R4_G0
R4	DIFFIO_R4_G0_04N_VAA12N	E5	IO_101_N	76.9545	R4_G0
R4	DIFFIO_R4_G0_05P	E7	IO_102_P	72.8724	R4_G0
R4	DIFFIO_R4_G0_05N_VREF	D7	IO_102_N	69.5204	R4_G0
R4	DIFFIO_R4_G1_06P_VAA13P	C4	IO_103_P	115.229	R4_G1
R4	DIFFIO_R4_G1_06N_VAA13N	B4	IO_103_N	115.835	R4_G1
R4	DIFFIO_R4_G1_07P_VAA14P	A4	IO_104_P	86.853	R4_G1
R4	DIFFIO_R4_G1_07N_VAA14N	A3	IO_104_N	85.8627	R4_G1
R4	DIFFIO_R4_G1_08P_DQS_VAA15P	B1	IO_105_P	82.8633	R4_G1_DQS
R4	DIFFIO_R4_G1_08N_DQS_VAA15N	A1	IO_105_N	86.1046	R4_G1_DQS
R4	DIFFIO_R4_G1_09P_VAA0P	B3	IO_106_P	81.5727	R4_G1
R4	DIFFIO_R4_G1_09N_VAA0N	B2	IO_106_N	83.8829	R4_G1
R4	DIFFIO_R4_G1_10P_GSCLK	D5	IO_107_P	104.498	R4_G1
R4	DIFFIO_R4_G1_10N_GSCLK	D4	IO_107_N	103.717	R4_G1
R4	DIFFIO_R4_G1_11P_GMCLK	E3	IO_108_P	56.3556	R4_G1
R4	DIFFIO_R4_G1_11N_GMCLK	D3	IO_108_N	62.5089	R4_G1
R4	DIFFIO_R4_G2_12P_GMCLK	F4	IO_109_P	62.8317	R4_G2
R4	DIFFIO_R4_G2_12N_GMCLK	F3	IO_109_N	65.4505	R4_G2
R4	DIFFIO_R4_G2_13P_GSCLK	E2	IO_110_P	65.9134	R4_G2
R4	DIFFIO_R4_G2_13N_GSCLK	D2	IO_110_N	65.9122	R4_G2
R4	DIFFIO_R4_G2_14P_DQS	H2	IO_111_P	52.9865	R4_G2_DQS
R4	DIFFIO_R4_G2_14N_DQS	G2	IO_111_N	51.9089	R4_G2_DQS
R4	DIFFIO_R4_G2_15P	C2	IO_112_P	70.6087	R4_G2
R4	DIFFIO_R4_G2_15N	C1	IO_112_N	70.8094	R4_G2
R4	DIFFIO_R4_G2_16P	H1	IO_113_P	52.6204	R4_G2
R4	DIFFIO_R4_G2_16N	G1	IO_113_N	54.577	R4_G2
R4	DIFFIO_R4_G2_17P	F1	IO_114_P	61.9541	R4_G2
R4	DIFFIO_R4_G2_17N	E1	IO_114_N	64.1385	R4_G2
R4	DIFFIO_R4_G3_18P	G6	IO_115_P	78.6893	R4_G3
R4	DIFFIO_R4_G3_18N_VREF	F6	IO_115_N	78.5718	R4_G3
R4	DIFFIO_R4_G3_19P	G4	IO_116_P	46.9769	R4_G3
R4	DIFFIO_R4_G3_19N	G3	IO_116_N	47.5756	R4_G3
R4	DIFFIO_R4_G3_20P_DQS	J4	IO_117_P	76.466	R4_G3_DQS
R4	DIFFIO_R4_G3_20N_DQS	H4	IO_117_N	76.3669	R4_G3_DQS

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R4	DIFFIO_R4_G3_21P	J3	IO_118_P	43.9863	R4_G3
R4	DIFFIO_R4_G3_21N	J2	IO_118_N	44.1721	R4_G3
R4	DIFFIO_R4_G3_22P	K2	IO_119_P	58.3157	R4_G3
R4	DIFFIO_R4_G3_22N	K1	IO_119_N	55.563	R4_G3
R4	DIFFIO_R4_G3_23P	H6	IO_120_P	52.7754	R4_G3
R4	DIFFIO_R4_G3_23N	H5	IO_120_N	55.3356	R4_G3
R4	SIO_R4_01	J5		29.1428	
R5	SIO_R5_00	K6		31.2098	
R5	DIFFIO_R5_G0_00P	L1	IO_121_P	58.7688	R5_G0
R5	DIFFIO_R5_G0_00N	M1	IO_121_N	58.9876	R5_G0
R5	DIFFIO_R5_G0_01P	K3	IO_122_P	41.1027	R5_G0
R5	DIFFIO_R5_G0_01N	L3	IO_122_N	38.052	R5_G0
R5	DIFFIO_R5_G0_02P_DQS	N2	IO_123_P	68.9569	R5_G0_DQS
R5	DIFFIO_R5_G0_02N_DQS	N1	IO_123_N	68.0922	R5_G0_DQS
R5	DIFFIO_R5_G0_03P	M3	IO_124_P	41.963	R5_G0
R5	DIFFIO_R5_G0_03N	M2	IO_124_N	47.3564	R5_G0
R5	DIFFIO_R5_G0_04P	K5	IO_125_P	72.6806	R5_G0
R5	DIFFIO_R5_G0_04N	L4	IO_125_N	70.8392	R5_G0
R5	DIFFIO_R5_G0_05P	L6	IO_126_P	50.4603	R5_G0
R5	DIFFIO_R5_G0_05N_VREF	L5	IO_126_N	51.1829	R5_G0
R5	DIFFIO_R5_G1_06P	U1	IO_127_P	93.3748	R5_G1
R5	DIFFIO_R5_G1_06N	V1	IO_127_N	92.3483	R5_G1
R5	DIFFIO_R5_G1_07P	U4	IO_128_P	79.0387	R5_G1
R5	DIFFIO_R5_G1_07N	U3	IO_128_N	78.435	R5_G1
R5	DIFFIO_R5_G1_08P_DQS	U2	IO_129_P	97.7884	R5_G1_DQS
R5	DIFFIO_R5_G1_08N_DQS	V2	IO_129_N	100.231	R5_G1_DQS
R5	DIFFIO_R5_G1_09P	V5	IO_130_P	86.9347	R5_G1
R5	DIFFIO_R5_G1_09N	V4	IO_130_N	83.4601	R5_G1
R5	DIFFIO_R5_G1_10P_GSCLK	R3	IO_131_P	79.9855	R5_G1
R5	DIFFIO_R5_G1_10N_GSCLK	T3	IO_131_N	81.1858	R5_G1
R5	DIFFIO_R5_G1_11P_GMCLK	T5	IO_132_P	68.0638	R5_G1
R5	DIFFIO_R5_G1_11N_GMCLK	T4	IO_132_N	66.2588	R5_G1
R5	DIFFIO_R5_G2_12P_GMCLK	N5	IO_133_P	84.3786	R5_G2
R5	DIFFIO_R5_G2_12N_GMCLK	P5	IO_133_N	82.6136	R5_G2
R5	DIFFIO_R5_G2_13P_GSCLK	P4	IO_134_P	47.9719	R5_G2
R5	DIFFIO_R5_G2_13N_GSCLK	P3	IO_134_N	45.7372	R5_G2
R5	DIFFIO_R5_G2_14P_DQS	P2	IO_135_P	69.9995	R5_G2_DQS
R5	DIFFIO_R5_G2_14N_DQS	R2	IO_135_N	71.9339	R5_G2_DQS
R5	DIFFIO_R5_G2_15P	M4	IO_136_P	42.2292	R5_G2

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
R5	DIFFIO_R5_G2_15N	N4	IO_136_N	40.6331	R5_G2
R5	DIFFIO_R5_G2_16P	R1	IO_137_P	79.8112	R5_G2
R5	DIFFIO_R5_G2_16N	T1	IO_137_N	78.3501	R5_G2
R5	DIFFIO_R5_G2_17P	M6	IO_138_P	55.0419	R5_G2
R5	DIFFIO_R5_G2_17N	N6	IO_138_N	55.1072	R5_G2
R5	DIFFIO_R5_G3_18P	R6	IO_139_P	84.2043	R5_G3
R5	DIFFIO_R5_G3_18N_VREF	R5	IO_139_N	81.5188	R5_G3
R5	DIFFIO_R5_G3_19P	V7	IO_140_P	103.91	R5_G3
R5	DIFFIO_R5_G3_19N	V6	IO_140_N	105.564	R5_G3
R5	DIFFIO_R5_G3_20P_DQS	U9	IO_141_P	119.461	R5_G3_DQS
R5	DIFFIO_R5_G3_20N_DQS	V9	IO_141_N	122.998	R5_G3_DQS
R5	DIFFIO_R5_G3_21P	U7	IO_142_P	75.9157	R5_G3
R5	DIFFIO_R5_G3_21N	U6	IO_142_N	70.7025	R5_G3
R5	DIFFIO_R5_G3_22P	R7	IO_143_P	89.1702	R5_G3
R5	DIFFIO_R5_G3_22N	T6	IO_143_N	83.725	R5_G3
R5	DIFFIO_R5_G3_23P	R8	IO_144_P	72.1066	R5_G3
R5	DIFFIO_R5_G3_23N	T8	IO_144_N	72.274	R5_G3
R5	SIO_R5_01	U8		73.0776	
	CFG_CLK	E9		42.4059	
	CFG_DONE	P10		41.2397	
	INIT_FLAG_N	P7		56.5652	
	MODE_0	P12		48.376	
	MODE_1	P13		56.1126	
	MODE_2	P11		41.5024	
	RSTN	P9		43.5425	
	SCBV	P8		54.9184	
	TCK	E10		46.9439	
	TDI	E11		43.8169	
	TDO	E13		61.9553	
	TMS	E12		46.5769	
	TSDN	L9	IO_165_N	109.893	
	TSDP	L10	IO_165_P	110.15	
	VAADC_N	K9	IO_166_N	97.2548	
	VAADC_P	J10	IO_166_P	98.2019	
	VREFADC_N	J9	IO_167_N	107.371	
	VREFADC_P	K10	IO_167_P	107.339	
	VCC	F8			
	VCC	G7			
	VCC	G9			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VCC	H8			
	VCC	J7			
	VCC	J11			
	VCC	K8			
	VCC	L7			
	VCC	L11			
	VCC	M8			
	VCC	M10			
	VCC	N7			
	VCC	N9			
	VCC	N11			
	VCC_DRM	F10			
	VCC_DRM	G11			
	VCCA	F12			
	VCCA	H12			
	VCCA	K12			
	VCCA	M12			
	VCCADC	H10			
	VCCB	E8			
	VCCIO_CFG	R9			
	VCCIO_L3	B10			
	VCCIO_L4	A17			
	VCCIO_L4	C13			
	VCCIO_L4	D16			
	VCCIO_L4	G15			
	VCCIO_L4	H18			
	VCCIO_L4	K14			
	VCCIO_L5	L17			
	VCCIO_L5	N13			
	VCCIO_L5	P16			
	VCCIO_L5	T12			
	VCCIO_L5	U15			
	VCCIO_L5	V18			
	VCCIO_R4	A7			
	VCCIO_R4	C3			
	VCCIO_R4	D6			
	VCCIO_R4	F2			
	VCCIO_R4	G5			
	VCCIO_R4	J1			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VCCIO_R5	K4			
	VCCIO_R5	N3			
	VCCIO_R5	P6			
	VCCIO_R5	T2			
	VCCIO_R5	U5			
	VCCIO_R5	V8			
	VSS	A2			
	VSS	A12			
	VSS	B5			
	VSS	B15			
	VSS	C8			
	VSS	C18			
	VSS	D1			
	VSS	D11			
	VSS	E4			
	VSS	E14			
	VSS	F7			
	VSS	F9			
	VSS	F11			
	VSS	F17			
	VSS	G8			
	VSS	G10			
	VSS	G12			
	VSS	H3			
	VSS	H7			
	VSS	H11			
	VSS	H13			
	VSS	J6			
	VSS	J8			
	VSS	J12			
	VSS	J16			
	VSS	K7			
	VSS	K11			
	VSS	L2			
	VSS	L8			
	VSS	L12			
	VSS	M5			
	VSS	M7			
	VSS	M9			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay(ps)	DQS Group
	VSS	M11			
	VSS	M15			
	VSS	N8			
	VSS	N10			
	VSS	N12			
	VSS	N18			
	VSS	P1			
	VSS	R4			
	VSS	R14			
	VSS	T7			
	VSS	T17			
	VSS	U10			
	VSS	V3			
	VSS	V13			
	VSSADC	H9			

2.2.2 Thermal Resistance

Table 2-2 Thermal Resistance

θJA(℃/W) (Flow: 0m/s)	θJB(℃/W)	θJC(℃/W)	θJA(℃/W) (Flow: 1m/s)	θJA(℃/W) (Flow: 2m/s)
17.0	8.0	3.6	14.8	13.4

2.2.3 Pressure Value

1. Short term pressure (within 5 minutes): 100g/ball, 324 balls, short term pressure can meet 32.4kg.
2. Long term pressure: 30g/ball, 324 balls, long term pressure can meet 9.72kg.

Chapter 3 Welding Requirements

Table 3-1 Welding Requirements

Preheat (150 ~200 ℃) time	60–120 S
Heating rate(T_L to T_P)	≤ 3 °C/S
Temperature above T_L(217℃) time	60-150 S
Package peak temperature/T_P	Reflow soldering:260℃ Rewelding:260℃
T_P -5℃ temperature range duration time	≤30 S
Rate of temperature fail (T_P to T_L)	≤ 6 °C/S
25℃ rise to T_P time	≤8 minutes

Note: Reference J-STD-020 standard.

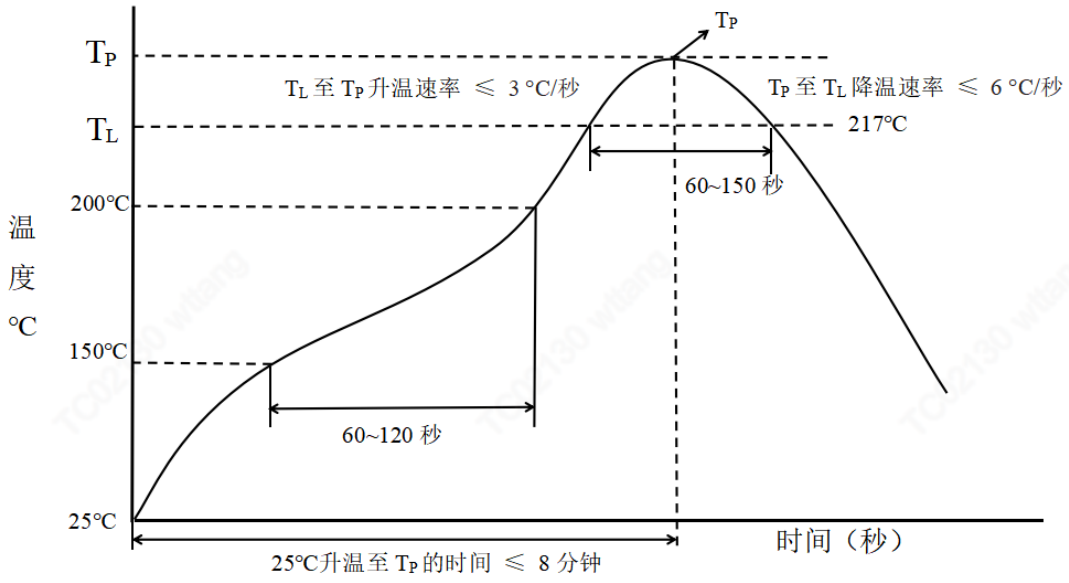


Figure 3-1 Welding Temperature Curve

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