PK03011_PGC7KD_MBG400

(V1.2)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.2	30.12.2020	Initial release

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
POD	Package Outline Drawing

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Chapter 1 Introduction to Packaging

The PGC7KD_MBG400 device is packaged with a Wire Bond BGA. Its package size is 17mmx17mm, with 400 solder balls, a pitch of 0.8mm, and a maximum package thickness of 1.55mm.

Chapter 2 Package Dimension and Pins

2.1 Package Outline Dimension

Table 2-1 Outline Dimensions

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	1.25	1.40	1.55	c	0.31	0.35	0.39
A1	0.30	0.35	0.40	e	-	0.8	-
A2	1.0	1.05	1.10	b	0.40	0.45	0.50
D	16.9	17.0	17.1	aaa	-	-	0.15
E	16.9	17.0	17.1	bbb	-	-	0.2
D1	-	15.2	-	ddd	-	-	0.2
E1	-	15.2	-	eee	-	-	0.15

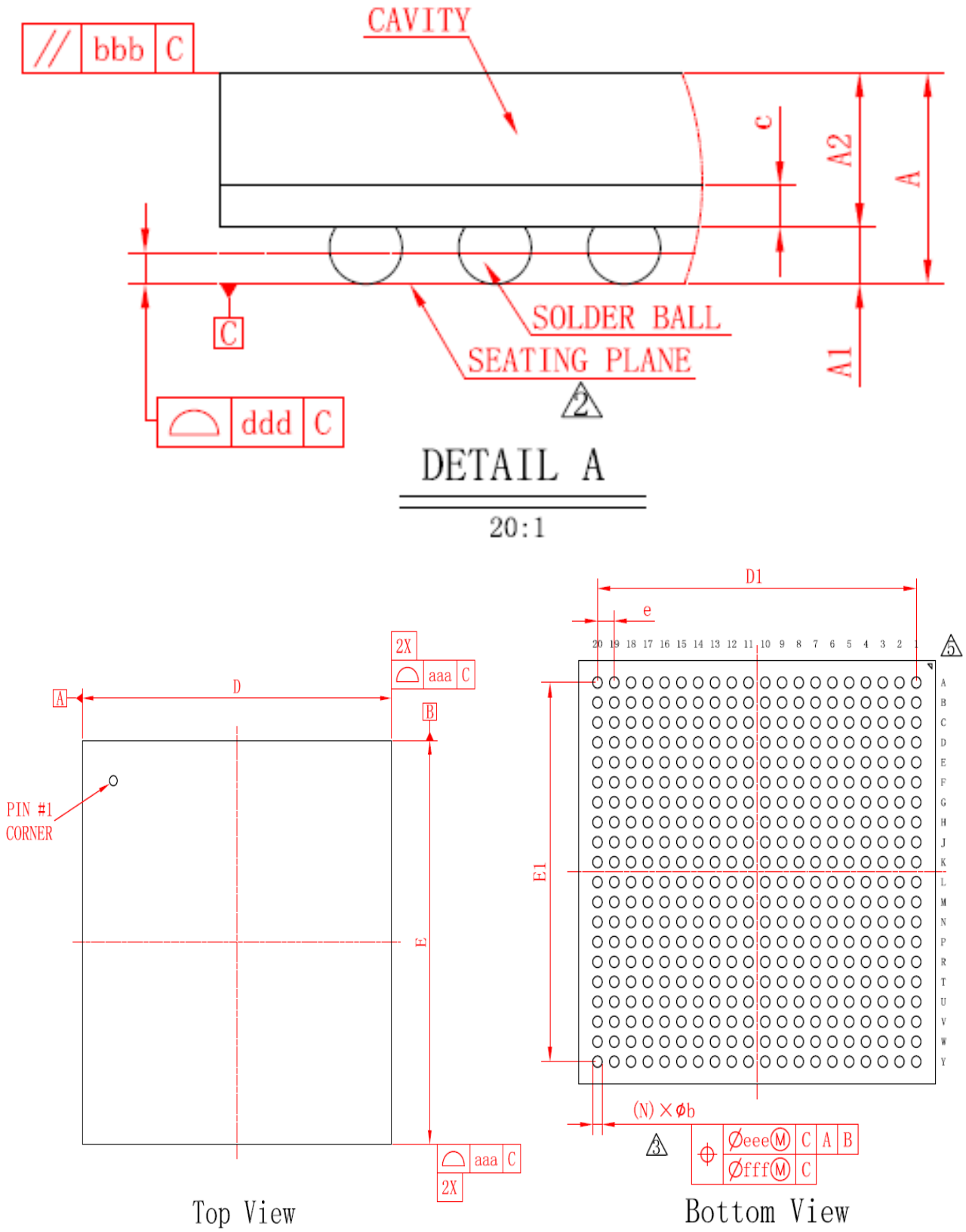

Figure 2-1 Package Outline Drawing (POD)

2.2 Pin Description

The PGC7KD_MBG400 device has 336 user I/Os.

Table 2-2 Device Pin Definitions

Pin Name	Pin Type	Direction	Pin Description
User I/O Pin			
DIFF[I,IO]_XX_NN[P,N]	User pin	Input/Output	User I/O. (1) DIFFI indicates support for differential signal input and pseudo-differential output; DIFFIO indicates support for differential signal input and true differential output, which can be used for transmitting and receiving LVDS signals; (2) “XX” denotes the Bank number, with possible values being B0, B1, B2, B3, B4, and B5; (3) “NN” denotes the sequence number of the programmable I/O group within the Bank, starting from 0 and increasing incrementally; (4) [P,N]: “P” denotes the positive side of the differential pair, and “N” denotes the negative side; During power-up, the user I/O is at a low voltage; After power-up is complete but before configuration, the general user I/O is at pull-down status; During configuration, the user I/O is at pull-down status;
Configuration[1]			
INIT_FLAG_N	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, with an internal weak pull-up resistor. When used as a configuration pin: During power-up, it is at a low voltage; After power-up is complete before configuration, it is open-drain at weak pull-up status; During configuration, it is open-drain at weak pull-up status; During initialization, the pin can be driven to a low voltage by an external input to indicate an error or to delay configuration. During configuration, the pin serves as an indicator output for configuration errors, where a low voltage indicates an error has occurred;
CFG_DONE	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, with an internal weak pull-up resistor. When it is used as configuration pin, it serves as an indicator output for configuration completion, where a high voltage indicates configuration is complete; Before or during configuration, the pin is driven to a low voltage; after configuration is complete, the pin can continue to be driven to a low voltage by an external source. If the internal start-up timing detects CFG_DONE at a low voltage, the internal start-up circuitry maintains its state until CFG_DONE goes high to continue the start-up process;
RSTN	Multi-function pin	Input	Configurable multiplexed reset pin, with an internal weak pull-up resistor. When it is used as a reset pin, it serves to restart the configuration process, active low. At this situation, it must be pulled up with an external resistor (internal weak pull-up resistor typically has a value of over 20kOhms, with a relatively weak pull-up strength); when the pin is at a low voltage, the CPLD enters reset state, with all I/Os in a weak pull-down status;

Pin Name	Pin Type	Direction	Pin Description
CFG_CLK	Multi-function pin	Input/Output	Configurable multiplexed clock pin, with an internal weak pull-up resistor. When it is used as a configuration pin: In slave SPI configuration mode, the pin serves as a clock input to acquire configuration data from an external source; In master SPI configuration mode, the pin serves as a clock output to acquire configuration data from an external source; in this mode, a 1kOhms pull-up resistor is needed; Master SPI mode and slave SPI mode are allowed to be enabled simultaneously, but using them at the same time is not permitted;
TCK	Multi-function pin	Input	Multiplexed JTAG test clock input pin; requires an external 4.7kOhms pull-down resistor;
TMS	Multi-function pin	Input	Multiplexed JTAG test mode select input pin; with an internal weak pull-up resistor, pulled up to VCCIO0;
TDI	Multi-function pin	Input	Multiplexed JTAG test data input pin; with an internal weak pull-up resistor, pulled up to VCCIO0;
TDO	Multi-function pin	Output	Multiplexed JTAG test data output pin; with an internal weak pull-up resistor, pulled up to VCCIO0.
JTAGEN	Multi-function pin	Input	Optional JTAG port behaviour control pin, usually used in user mode, when JTAG pins are configured as configuration I/Os, this pin is user I/O, with the state controlled by the user; when JTAG pins serve as user I/Os, JTAGEN serves as a dedicated input used to control the availability of JTAG pins; the default state is weak pull-down; when JTAGEN is configured as a dedicated I/O: (1) When at a low voltage, the JTAG pins function as user I/Os; (2) When at a high voltage, the JTAG pins function as JTAG configuration port.
FCS_N	Multi-function pin	Output	Configurable multiplexed pin, used for master SPI configuration mode, (1) In master SPI mode, outputs an active-low chip select signal to an external Flash; (2) After configuration is completed, it can be used as a user I/O.
MISO_SO	Multi-function pin	Input/Output	Configurable multiplexed pin; (1) MISO, serial data input in master SPI mode; (2) SO, serial data output in slave SPI mode; Master and slave SPI modes are allowed to be enabled simultaneously, but using them at the same time is not permitted.
MOSI_SI	Multi-function pin	Input/Output	Configurable multiplexed pin; (1) MOSI, serial data output in master SPI mode; (2) SI, serial data input in slave SPI mode; Master and slave SPI modes are allowed to be enabled simultaneously, but using them at the same time is not permitted.
FCSI_N	Multi-function pin	Input	Configurable multiplexed pin, with an internal weak pull-up resistor; In slave SPI mode, active-low chip select input.
SCL	Multi-function pin	Input (Open-drain)	Configurable multiplexed pin, clock input in slave I2C mode; requires an external weak pull-up resistor.

Pin Name	Pin Type	Direction	Pin Description
SDA	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, data input/output in I2C mode; requires an external weak pull-up resistor.
SPAL_CLK	Multi-function pin	Input	Clock input in slave parallel X16 configuration mode.
SPAL_CS_N	Multi-function pin	Input	Chip select input in slave parallel X16 configuration mode. Active-low
SPAL_RDWR_N	Multi-function pin	Input	Read/write control input in slave parallel X16 configuration mode; 1: read; 0: write.
SPAL_BUSY	Multi-function pin	Output	Busy indicator in slave parallel X16 configuration mode; During readback, if the data is not ready, SPAL_BUSY changes to high voltage.
SPAL_D15~SPAL_D0	Multi-function pin	Input/Output	Data bus in slave parallel X16 configuration mode.
Clock, PLL			
CLK[0,1,2][P,N]_[B0,B1,…,B5]	Multi-function pin	Input	Global clock input pin; can also be used as user I/O; (1) [0,1,2]: clock pin numbers; (2) [P,N]: positive and negative sides of the differential clock pins; (3) [B0,B1,…,B5]: bank numbers.
PLL[0,1]_CLKIN_[P,N]	Multi-function pin	Input	PLL input. PLL can choose to directly input a clock from these pins; they can also be used as user I/Os; (1) [0,1]: corresponds to PLL0 and PLL1; (2) [P,N]: positive and negative sides of the differential clock pins.
PLL[0,1]_CLKFB_[P,N]	Multi-function pin	Input	Optional PLL feedback clock input. PLL can select to feedback clock externally from these pins; they can also be used as user I/Os; (1) [0,1]: corresponds to PLL0 and PLL1; (2) [P,N]: positive and negative sides of the differential clock pins.
Power			
VCC		Power	External power supply of 2.5V or 3.3V, providing power to the core logic.
VCCIO[0,1,2,3,4,5]		Power	I/O Bank power.
VSS		Ground	Ground associated with VCC;

Note:

1. When the configured multi-function pin is used as a user I/O, its status is the same as the user I/O pin.

2.2.1 Pin Name list

Table 2-3 Pin Name List

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B0	DIFFI_B0_0N/CFG_DONE	A19	IO_1_N	59.0038
B0	DIFFI_B0_0P/INIT_FLAG_N	C17	IO_1_P	75.6012
B0	DIFFIO_B0_1N/SPAL_CLK	A20	IO_2_N	78.005
B0	DIFFIO_B0_1P/SPAL_CS_N	B19	IO_2_P	77.3725

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B0	DIFFI_B0_2N/SPAL_RDWR_N	F14	IO_3_N	51.2284
B0	DIFFI_B0_2P/SPAL_BUSY	G14	IO_3_P	52.0834
B0	DIFFIO_B0_3N/SPAL_D15	D16	IO_4_N	36.3023
B0	DIFFIO_B0_3P/SPAL_D14	E15	IO_4_P	33.1596
B0	DIFFI_B0_4N/SPAL_D13	D15	IO_5_N	32.4234
B0	DIFFI_B0_4P/SPAL_D12	E14	IO_5_P	41.1835
B0	DIFFIO_B0_5N/SPAL_D11	B18	IO_6_N	69.6435
B0	DIFFIO_B0_5P/SPAL_D10	A18	IO_6_P	71.2404
B0	DIFFI_B0_6N/SPAL_D9	F13	IO_7_N	36.0749
B0	DIFFI_B0_6P/SPAL_D8	G13	IO_7_P	39.3462
B0	DIFFIO_B0_7N/SPAL_D7	C16	IO_8_N	53.2012
B0	DIFFIO_B0_7P/SPAL_D6	C15	IO_8_P	52.8298
B0	DIFFI_B0_8N/SPAL_D5	D14	IO_9_N	48.7947
B0	DIFFI_B0_8P/SPAL_D4	C14	IO_9_P	46.7804
B0	DIFFIO_B0_9N/SPAL_D3	B17	IO_10_N	69.0779
B0	DIFFIO_B0_9P/SPAL_D2	A17	IO_10_P	70.3548
B0	DIFFI_B0_10N	F12	IO_11_N	55.7412
B0	DIFFI_B0_10P	G12	IO_11_P	55.6003
B0	DIFFIO_B0_11N	B16	IO_12_N	65.4932
B0	DIFFIO_B0_11P	A16	IO_12_P	69.2262
B0	DIFFI_B0_12N/RSTN	D13	IO_13_N	45.7414
B0	DIFFI_B0_12P/JTAGEN	C13	IO_13_P	50.5906
B0	DIFFIO_B0_13N/SPAL_D1	B15	IO_14_N	61.9752
B0	DIFFIO_B0_13P/SPAL_D0	A15	IO_14_P	63.6545
B0	DIFFI_B0_14N/EFB_CLK	C12	IO_15_N	37.4517
B0	DIFFI_B0_14P/EFB_STR	D12	IO_15_P	31.5222
B0	DIFFIO_B0_15N	B14	IO_16_N	64.005
B0	DIFFIO_B0_15P	A14	IO_16_P	67.3395
B0	DIFFI_B0_16N/EFB_D	F11	IO_17_N	48.3989
B0	DIFFI_B0_16P	G11	IO_17_P	49.2246
B0	DIFFIO_B0_17N	B13	IO_18_N	59.3683
B0	DIFFIO_B0_17P	A13	IO_18_P	62.5045
B0	DIFFI_B0_18N/SDA/CLK0N_B0	D11	IO_19_N	52.7662
B0	DIFFI_B0_18P/SCL/CLK0P_B0	C11	IO_19_P	54.3782
B0	DIFFIO_B0_19N	B12	IO_20_N	42.3232
B0	DIFFIO_B0_19P	A12	IO_20_P	42.3681
B0	DIFFI_B0_20N	C10	IO_21_N	43.0012
B0	DIFFI_B0_20P	D10	IO_21_P	40.32
B0	DIFFIO_B0_21N	A11	IO_22_N	44.9589

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B0	DIFFIO_B0_21P	B11	IO_22_P	39.8385
B0	DIFFI_B0_22N	F10	IO_23_N	47.3292
B0	DIFFI_B0_22P	G10	IO_23_P	49.916
B0	DIFFIO_B0_23N/CLK1N_B0	A10	IO_24_N	40.6266
B0	DIFFIO_B0_23P/CLK1P_B0	B10	IO_24_P	40.8588
B0	DIFFI_B0_24N/TMS	D9	IO_25_N	59.2921
B0	DIFFI_B0_24P/TCK	C9	IO_25_P	59.2403
B0	DIFFIO_B0_25N	A9	IO_26_N	47.5616
B0	DIFFIO_B0_25P	B9	IO_26_P	45.2439
B0	DIFFI_B0_26N	C8	IO_27_N	60.1174
B0	DIFFI_B0_26P	D8	IO_27_P	58.1349
B0	DIFFIO_B0_27N	A8	IO_28_N	61.3079
B0	DIFFIO_B0_27P	B8	IO_28_P	56.3648
B0	DIFFI_B0_28N	F9	IO_29_N	54.3992
B0	DIFFI_B0_28P	G9	IO_29_P	55.659
B0	DIFFIO_B0_29N	A7	IO_30_N	60.7191
B0	DIFFIO_B0_29P	B7	IO_30_P	57.6939
B0	DIFFI_B0_30N/TDI	C7	IO_31_N	47.9434
B0	DIFFI_B0_30P/TDO	E8	IO_31_P	48.398
B0	DIFFIO_B0_31N	A6	IO_32_N	64.2025
B0	DIFFIO_B0_31P	B6	IO_32_P	62.0442
B0	DIFFI_B0_32N	F8	IO_33_N	42.9616
B0	DIFFI_B0_32P	G8	IO_33_P	54.3276
B0	DIFFIO_B0_33N	A5	IO_34_N	66.1712
B0	DIFFIO_B0_33P	B5	IO_34_P	66.8552
B0	DIFFI_B0_34N	D7	IO_35_N	34.325
B0	DIFFI_B0_34P	C6	IO_35_P	38.9705
B0	DIFFIO_B0_35N	A4	IO_36_N	69.0688
B0	DIFFIO_B0_35P	B4	IO_36_P	65.3611
B0	DIFFI_B0_36N	E7	IO_37_N	57.0511
B0	DIFFI_B0_36P	D6	IO_37_P	55.1867
B0	DIFFIO_B0_37N	A3	IO_38_N	72.3203
B0	DIFFIO_B0_37P	B3	IO_38_P	70.5918
B0	DIFFI_B0_38N	D5	IO_39_N	37.0246
B0	DIFFI_B0_38P	E6	IO_39_P	31.4078
B0	DIFFIO_B0_39N	A2	IO_40_N	80.4998
B0	DIFFIO_B0_39P	B2	IO_40_P	74.5742
B0	DIFFI_B0_40N	F7	IO_41_N	38.2209
B0	DIFFI_B0_40P	G7	IO_41_P	51.9767

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B0	DIFFIO_B0_41N	A1	IO_42_N	82.0467
B0	DIFFIO_B0_41P	B1	IO_42_P	79.1705
B1	DIFFI_B1_0P/PLL1_CLKFB_P	D17	IO_43_P	47.2338
B1	DIFFI_B1_0N/PLL1_CLKFB_N	C18	IO_43_N	49.955
B1	DIFFI_B1_1P	F15	IO_44_P	34.7479
B1	DIFFI_B1_1N	G15	IO_44_N	34.2602
B1	DIFFI_B1_2P/PLL1_CLKIN_P	C19	IO_45_P	62.8574
B1	DIFFI_B1_2N/PLL1_CLKIN_N	E17	IO_45_N	61.2481
B1	DIFFI_B1_3P	F16	IO_46_P	52.911
B1	DIFFI_B1_3N	D18	IO_46_N	52.8442
B1	DIFFI_B1_4P	B20	IO_47_P	75.3497
B1	DIFFI_B1_4N	C20	IO_47_N	73.6439
B1	DIFFI_B1_5P	H14	IO_48_P	48.7473
B1	DIFFI_B1_5N	H15	IO_48_N	50.4892
B1	DIFFI_B1_6P	D19	IO_49_P	46.5915
B1	DIFFI_B1_6N	F17	IO_49_N	56.4831
B1	DIFFI_B1_7P	D20	IO_50_P	52.7496
B1	DIFFI_B1_7N	E19	IO_50_N	61.3383
B1	DIFFI_B1_8P	G16	IO_51_P	42.6528
B1	DIFFI_B1_8N	F18	IO_51_N	47.2395
B1	DIFFI_B1_9P	G17	IO_52_P	59.9872
B1	DIFFI_B1_9N	E20	IO_52_N	64.7321
B1	DIFFI_B1_10P	F19	IO_53_P	45.0248
B1	DIFFI_B1_10N	F20	IO_53_N	50.0356
B1	DIFFI_B1_11P	J14	IO_54_P	49.7462
B1	DIFFI_B1_11N	J15	IO_54_N	51.6688
B1	DIFFI_B1_12P	G19	IO_55_P	51.3711
B1	DIFFI_B1_12N	H17	IO_55_N	47.9279
B1	DIFFI_B1_13P	H16	IO_56_P	53.5323
B1	DIFFI_B1_13N	G20	IO_56_N	59.7791
B1	DIFFI_B1_14P	H18	IO_57_P	57.9641
B1	DIFFI_B1_14N	H19	IO_57_N	61.353
B1	DIFFI_B1_15P	J17	IO_58_P	53.0409
B1	DIFFI_B1_15N	H20	IO_58_N	57.7444
B1	DIFFI_B1_16P	J18	IO_59_P	30.6528
B1	DIFFI_B1_16N	J16	IO_59_N	40.5161
B1	DIFFI_B1_17P	K14	IO_60_P	47.2254
B1	DIFFI_B1_17N	K15	IO_60_N	47.4186
B1	DIFFI_B1_18P	J19	IO_61_P	40.3862

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B1	DIFFI_B1_18N	J20	IO_61_N	40.5282
B1	DIFFI_B1_19P	K17	IO_62_P	56.0441
B1	DIFFI_B1_19N	K18	IO_62_N	55.6504
B1	DIFFI_B1_20P/CLK0P_B1	K19	IO_63_P	42.9025
B1	DIFFI_B1_20N/CLK0N_B1	K20	IO_63_N	45.6561
B1	DIFFI_B1_21P	K16	IO_64_P	56.9036
B1	DIFFI_B1_21N	L17	IO_64_N	53.5599
B1	DIFFI_B1_22P	L19	IO_65_P	54.8089
B1	DIFFI_B1_22N	L20	IO_65_N	56.8799
B1	DIFFI_B1_23P	L14	IO_66_P	51.7799
B1	DIFFI_B1_23N	L15	IO_66_N	52.3219
B1	DIFFI_B1_24P	M20	IO_67_P	45.3009
B1	DIFFI_B1_24N	M19	IO_67_N	42.9957
B1	DIFFI_B1_25P	L16	IO_68_P	44.8948
B1	DIFFI_B1_25N	M18	IO_68_N	49.3473
B1	DIFFI_B1_26P	M17	IO_69_P	49.8066
B1	DIFFI_B1_26N	N20	IO_69_N	57.7585
B1	DIFFI_B1_27P	M16	IO_70_P	51.526
B1	DIFFI_B1_27N	N19	IO_70_N	53.7899
B1	DIFFI_B1_28P	N18	IO_71_P	30.5258
B1	DIFFI_B1_28N	N17	IO_71_N	30.7956
B1	DIFFI_B1_29P	P20	IO_72_P	58.0263
B1	DIFFI_B1_29N	P19	IO_72_N	56.3646
B1	DIFFI_B1_30P	P18	IO_73_P	54.0177
B1	DIFFI_B1_30N	R20	IO_73_N	58.5711
B1	DIFFI_B1_31P	M15	IO_74_P	50.71
B1	DIFFI_B1_31N	M14	IO_74_N	52.5096
B1	DIFFI_B1_32P	N16	IO_75_P	51.1756
B1	DIFFI_B1_32N	R19	IO_75_N	57.0589
B1	DIFFI_B1_33P	T20	IO_76_P	55.8178
B1	DIFFI_B1_33N	T19	IO_76_N	54.3593
B1	DIFFI_B1_34P	U20	IO_77_P	72.5648
B1	DIFFI_B1_34N	P17	IO_77_N	63.2768
B1	DIFFI_B1_35P	T18	IO_78_P	67.2318
B1	DIFFI_B1_35N	U19	IO_78_N	67.5821
B1	DIFFI_B1_36P	V20	IO_79_P	69.314
B1	DIFFI_B1_36N	P16	IO_79_N	64.3992
B1	DIFFI_B1_37P	N15	IO_80_P	55.1092
B1	DIFFI_B1_37N	N14	IO_80_N	56.8565

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B1	DIFFI_B1_38P	R17	IO_81_P	49.7581
B1	DIFFI_B1_38N	U18	IO_81_N	40.429
B1	DIFFI_B1_39P	P15	IO_82_P	37.5667
B1	DIFFI_B1_39N	R16	IO_82_N	44.7394
B1	DIFFI_B1_40P	V19	IO_83_P	46.7584
B1	DIFFI_B1_40N	T17	IO_83_N	45.9564
B1	DIFFI_B1_41P	U17	IO_84_P	47.6421
B1	DIFFI_B1_41N	V17	IO_84_N	44.7999
B2	DIFFI_B2_0N	R15	IO_85_N	45.5545
B2	DIFFI_B2_0P	T16	IO_85_P	46.8222
B2	DIFFI_B2_1N/MOSI_SI	W20	IO_86_N	77.3774
B2	DIFFI_B2_1P/FCSI_N	Y20	IO_86_P	80.9581
B2	DIFFI_B2_2N	R14	IO_87_N	39.5372
B2	DIFFI_B2_2P	P14	IO_87_P	43.9623
B2	DIFFI_B2_3N	W19	IO_88_N	71.4327
B2	DIFFI_B2_3P	Y19	IO_88_P	74.7696
B2	DIFFI_B2_4N	U15	IO_89_N	34.0302
B2	DIFFI_B2_4P	T14	IO_89_P	38.918
B2	DIFFI_B2_5N	W18	IO_90_N	70.1446
B2	DIFFI_B2_5P	Y18	IO_90_P	73.8507
B2	DIFFI_B2_6N	V16	IO_91_N	39.9795
B2	DIFFI_B2_6P	V15	IO_91_P	41.0551
B2	DIFFI_B2_7N	U14	IO_92_N	44.7548
B2	DIFFI_B2_7P	V14	IO_92_P	47.2679
B2	DIFFI_B2_8N	R13	IO_93_N	39.9777
B2	DIFFI_B2_8P	P13	IO_93_P	52.7425
B2	DIFFI_B2_9N	W17	IO_94_N	67.6572
B2	DIFFI_B2_9P	Y17	IO_94_P	71.6633
B2	DIFFI_B2_10N	T13	IO_95_N	52.8703
B2	DIFFI_B2_10P	T12	IO_95_P	53.5158
B2	DIFFI_B2_11N	W16	IO_96_N	71.4955
B2	DIFFI_B2_11P	Y16	IO_96_P	72.0293
B2	DIFFI_B2_12N	R12	IO_97_N	47.6058
B2	DIFFI_B2_12P	P12	IO_97_P	48.7781
B2	DIFFI_B2_13N	W15	IO_98_N	65.3385
B2	DIFFI_B2_13P	Y15	IO_98_P	69.5463
B2	DIFFI_B2_14N	T11	IO_99_N	51.9537
B2	DIFFI_B2_14P	U12	IO_99_P	52.0526
B2	DIFFI_B2_15N	W14	IO_100_N	59.3084

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B2	DIFFI_B2_15P	Y14	IO_100_P	62.8771
B2	DIFFI_B2_16N	V13	IO_101_N	51.6013
B2	DIFFI_B2_16P	V12	IO_101_P	51.6362
B2	DIFFI_B2_17N	W13	IO_102_N	45.6261
B2	DIFFI_B2_17P	Y13	IO_102_P	50.2937
B2	DIFFI_B2_18N	R11	IO_103_N	44.2149
B2	DIFFI_B2_18P	P11	IO_103_P	47.2975
B2	DIFFI_B2_19N/CLK1N_B2	W12	IO_104_N	68.4604
B2	DIFFI_B2_19P/CLK1P_B2	Y12	IO_104_P	67.9871
B2	DIFFI_B2_20N	T10	IO_105_N	65.1229
B2	DIFFI_B2_20P	U11	IO_105_P	62.565
B2	DIFFI_B2_21N	W11	IO_106_N	40.1824
B2	DIFFI_B2_21P	Y11	IO_106_P	44.15
B2	DIFFI_B2_22N	V10	IO_107_N	61.7829
B2	DIFFI_B2_22P	U10	IO_107_P	62.7775
B2	DIFFI_B2_23N	W10	IO_108_N	65.4543
B2	DIFFI_B2_23P	Y10	IO_108_P	62.779
B2	DIFFI_B2_24N	R10	IO_109_N	54.0055
B2	DIFFI_B2_24P	P10	IO_109_P	55.368
B2	DIFFI_B2_25N/CLK0N_B2	Y9	IO_110_N	66.5275
B2	DIFFI_B2_25P/CLK0P_B2	W9	IO_110_P	61.924
B2	DIFFI_B2_26N	T9	IO_111_N	43.4896
B2	DIFFI_B2_26P	V9	IO_111_P	42.4248
B2	DIFFI_B2_27N	Y8	IO_112_N	42.3234
B2	DIFFI_B2_27P	W8	IO_112_P	40.6435
B2	DIFFI_B2_28N	U9	IO_113_N	51.7145
B2	DIFFI_B2_28P	V8	IO_113_P	49.5172
B2	DIFFI_B2_29N	Y7	IO_114_N	61.5011
B2	DIFFI_B2_29P	W7	IO_114_P	58.6193
B2	DIFFI_B2_30N	R9	IO_115_N	47.3332
B2	DIFFI_B2_30P	P9	IO_115_P	51.0765
B2	DIFFI_B2_31N/MISO_SO	Y6	IO_116_N	66.3063
B2	DIFFI_B2_31P/CFG_CLK	W6	IO_116_P	63.5568
B2	DIFFI_B2_32N	T8	IO_117_N	51.9301
B2	DIFFI_B2_32P	T7	IO_117_P	51.954
B2	DIFFI_B2_33N	Y5	IO_118_N	66.0589
B2	DIFFI_B2_33P	W5	IO_118_P	63.1341
B2	DIFFI_B2_34N	R8	IO_119_N	33.0698
B2	DIFFI_B2_34P	P8	IO_119_P	37.6574

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B2	DIFFI_B2_35N	Y4	IO_120_N	68.1744
B2	DIFFI_B2_35P	W4	IO_120_P	67.0813
B2	DIFFI_B2_36N	U6	IO_121_N	48.4395
B2	DIFFI_B2_36P	V6	IO_121_P	50.034
B2	DIFFI_B2_37N	Y3	IO_122_N	71.8249
B2	DIFFI_B2_37P	W3	IO_122_P	69.2463
B2	DIFFI_B2_38N	R7	IO_123_N	33.1477
B2	DIFFI_B2_38P	P7	IO_123_P	36.8746
B2	DIFFI_B2_39N	Y2	IO_124_N	75.5243
B2	DIFFI_B2_39P/FCS_N	W2	IO_124_P	72.269
B2	DIFFI_B2_40N	T6	IO_125_N	52.5443
B2	DIFFI_B2_40P	R6	IO_125_P	51.5081
B2	DIFFI_B2_41N	Y1	IO_126_N	77.0558
B2	DIFFI_B2_41P	W1	IO_126_P	78.0026
B3	DIFFI_B3_0P	N3	IO_127_P	45.4414
B3	DIFFI_B3_0N	N4	IO_127_N	40.7281
B3	DIFFI_B3_1P	M6	IO_128_P	52.0002
B3	DIFFI_B3_1N	M7	IO_128_N	54.9056
B3	DIFFI_B3_2P	P3	IO_129_P	46.1111
B3	DIFFI_B3_2N	P4	IO_129_N	42.461
B3	DIFFI_B3_3P	R1	IO_130_P	67.9245
B3	DIFFI_B3_3N	R2	IO_130_N	64.1049
B3	DIFFI_B3_4P	T1	IO_131_P	66.4597
B3	DIFFI_B3_4N	T2	IO_131_N	64.4662
B3	DIFFI_B3_5P	N5	IO_132_P	24.0109
B3	DIFFI_B3_5N	N6	IO_132_N	27.7242
B3	DIFFI_B3_6P/CLK0P_B3	U1	IO_133_P	70.455
B3	DIFFI_B3_6N/CLK0N_B3	U2	IO_133_N	68.9611
B3	DIFFI_B3_7P	R3	IO_134_P	54.0627
B3	DIFFI_B3_7N	R4	IO_134_N	53.0425
B3	DIFFI_B3_8P	T3	IO_135_P	43.556
B3	DIFFI_B3_8N	T4	IO_135_N	51.4993
B3	DIFFI_B3_9P	V1	IO_136_P	75.45
B3	DIFFI_B3_9N	V2	IO_136_N	71.2947
B3	DIFFI_B3_10P	V3	IO_137_P	59.5463
B3	DIFFI_B3_10N	V4	IO_137_N	56.7444
B3	DIFFI_B3_11P	P5	IO_138_P	52.3338
B3	DIFFI_B3_11N	P6	IO_138_N	49.8374
B3	DIFFI_B3_12P	T5	IO_139_P	55.1502

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B3	DIFFI_B3_12N	R5	IO_139_N	56.4276
B3	DIFFI_B3_13P	U4	IO_140_P	41.0546
B3	DIFFI_B3_13N	U5	IO_140_N	34.085
B4	DIFFI_B4_0P	J2	IO_141_P	44.9492
B4	DIFFI_B4_0N	J1	IO_141_N	46.84
B4	DIFFI_B4_1P	K5	IO_142_P	58.5106
B4	DIFFI_B4_1N	K4	IO_142_N	58.2742
B4	DIFFI_B4_2P	K2	IO_143_P	54.0452
B4	DIFFI_B4_2N	K1	IO_143_N	55.8479
B4	DIFFI_B4_3P	K6	IO_144_P	44.0705
B4	DIFFI_B4_3N	K7	IO_144_N	45.4761
B4	DIFFI_B4_4P/CLK0P_B4	L1	IO_145_P	44.8707
B4	DIFFI_B4_4N/CLK0N_B4	L2	IO_145_N	43.1449
B4	DIFFI_B4_5P	L3	IO_146_P	54.1956
B4	DIFFI_B4_5N	L4	IO_146_N	52.0943
B4	DIFFI_B4_6P	M1	IO_147_P	50.1072
B4	DIFFI_B4_6N	M2	IO_147_N	46.0081
B4	DIFFI_B4_7P	M3	IO_148_P	33.9139
B4	DIFFI_B4_7N	M4	IO_148_N	35.7607
B4	DIFFI_B4_8P	L5	IO_149_P	36.6379
B4	DIFFI_B4_8N	M5	IO_149_N	35.2094
B4	DIFFI_B4_9P	L6	IO_150_P	45.8974
B4	DIFFI_B4_9N	L7	IO_150_N	43.6427
B4	DIFFI_B4_10P	N1	IO_151_P	60.7033
B4	DIFFI_B4_10N	N2	IO_151_N	56.248
B4	DIFFI_B4_11P	P1	IO_152_P	64.4123
B4	DIFFI_B4_11N	P2	IO_152_N	63.522
B5	DIFFI_B5_0P	C4	IO_153_P	54.8331
B5	DIFFI_B5_0N	C3	IO_153_N	57.7382
B5	DIFFI_B5_1P	F6	IO_154_P	33.9779
B5	DIFFI_B5_1N	G6	IO_154_N	33.6381
B5	DIFFI_B5_2P/PLL0_CLKFB_P	C2	IO_155_P	68.1783
B5	DIFFI_B5_2N/PLL0_CLKFB_N	C1	IO_155_N	69.8425
B5	DIFFI_B5_3P	E4	IO_156_P	41.4745
B5	DIFFI_B5_3N	E3	IO_156_N	42.273
B5	DIFFI_B5_4P/PLL0_CLKIN_P	D2	IO_157_P	66.5318
B5	DIFFI_B5_4N/PLL0_CLKIN_N	D1	IO_157_N	67.9032
B5	DIFFI_B5_5P	F5	IO_158_P	51.7208
B5	DIFFI_B5_5N	G5	IO_158_N	50.4867

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
B5	DIFFI_B5_6P	F4	IO_159_P	35.3938
B5	DIFFI_B5_6N	F3	IO_159_N	39.6328
B5	DIFFI_B5_7P	H6	IO_160_P	52.2951
B5	DIFFI_B5_7N	H7	IO_160_N	52.7337
B5	DIFFI_B5_8P/CLK0P_B5	E2	IO_161_P	64.0566
B5	DIFFI_B5_8N/CLK0N_B5	E1	IO_161_N	66.9745
B5	DIFFI_B5_9P	F2	IO_162_P	47.0553
B5	DIFFI_B5_9N	F1	IO_162_N	52.6575
B5	DIFFI_B5_10P	G4	IO_163_P	56.83
B5	DIFFI_B5_10N	G3	IO_163_N	59.6894
B5	DIFFI_B5_11P	H3	IO_164_P	48.3182
B5	DIFFI_B5_11N	H4	IO_164_N	45.8353
B5	DIFFI_B5_12P	G2	IO_165_P	58.4448
B5	DIFFI_B5_12N	G1	IO_165_N	59.3485
B5	DIFFI_B5_13P	J6	IO_166_P	33.3963
B5	DIFFI_B5_13N	J5	IO_166_N	31.7562
B5	DIFFI_B5_14P	H2	IO_167_P	56.1699
B5	DIFFI_B5_14N	H1	IO_167_N	61.003
B5	DIFFI_B5_15P	J4	IO_168_P	32.9632
B5	DIFFI_B5_15N	J3	IO_168_N	31.9668
	VSS	D3		
	VCC	H12		
	VCC	H13		
	VCC	J9		
	VCC	J10		
	VCC	J11		
	VCC	K12		
	VCC	L9		
	VCC	L12		
	VCC	M10		
	VCC	M12		
	VCCIO0	H8		
	VCCIO0	H9		
	VCCIO0	H10		
	VCCIO0	H11		
	VCCIO0	J12		
	VCCIO1	J13		
	VCCIO1	K13		
	VCCIO1	L13		

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
	VCCIO1	M13		
	VCCIO1	N13		
	VCCIO2	N8		
	VCCIO2	N9		
	VCCIO2	N10		
	VCCIO2	N11		
	VCCIO2	N12		
	VCCIO3	M8		
	VCCIO3	M9		
	VCCIO4	K8		
	VCCIO4	K9		
	VCCIO5	J7		
	VCCIO5	J8		
	VSS	C5		
	VSS	D4		
	VSS	E5		
	VSS	E9		
	VSS	E10		
	VSS	E11		
	VSS	E12		
	VSS	E13		
	VSS	E16		
	VSS	E18		
	VSS	G18		
	VSS	H5		
	VSS	K3		
	VSS	K10		
	VSS	K11		
	VSS	L8		
	VSS	L10		
	VSS	L11		
	VSS	L18		
	VSS	M11		
	VSS	N7		
	VSS	R18		
	VSS	T15		
	VSS	U3		
	VSS	U7		
	VSS	U8		

Bank Name	Pin Name	Pin Number	Differential Pair	Time Delay (ps)
	VSS	U13		
	VSS	U16		
	VSS	V5		
	VSS	V7		
	VSS	V11		
	VSS	V18		

2.2.2 Thermal Resistance

Table 2-4 Thermal Resistance Data

θJA(°C/W) (Flow: 0m/s)	θJB (°C/W)	θJC (°C/W)	θJA(°C/W) (Flow: 1m/s)	θJA(°C/W) (Flow: 2m/s)
22.0	13.5	10.4	18.5	17.5

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