SGMII 1GbE IP

User Guide

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Shenzhen Pango Microsystems Co., Ltd.

Revisions History

Document Revisions

Version	Date of Release	Revisions	Applicable IP and Corresponding Versions
V1.4	21.12.2023	Initial release.	V1.4

IP Revisions

IP Version	Date of Release	Revisions
V1.4	21.12.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
CTC	Clock Tolerance Compensation
CDR	Clock Data Recovery
GE	Gigabit Ethernet
GMII	Gigabit Media Independent Interface
HSSTLP	High Speed Serial Transceiver Low Performance
LH	Latching High
LL	Latching Low
MDIO	Management Data Input/Output
PCS	Physical Code Sublayer
PMA	Physical Media Attachment
SGMII	Serial Gigabit Media Independent Interface
IPC	IP Compiler
PDS	Pango Design Suite
UCE	User Constraint Editor

Related Documentation

The following documentation is related to this manual:

1. ***Pango_Design_Suite_Quick_Start_Tutorial***
2. ***Pango_Design_Suite_User_Guide***
3. ***IP_Compiler_User_Guide***
4. ***Simulation_User_Guide***
5. ***User_Constraint_Editor_User_Guide***
6. ***Physical_Constraint_Editor_User_Guide***
7. ***Route_Constraint_Editor_User_Guide***
8. ***UG040008_Logos2 Family FPGA High-Speed Serial Transceiver (HSSTLP) User Guide***
9. ***UG041004_HSSTLP_IP***
10. ***IEEE 802.3-2012 Specification***
11. ***Serial-GMII Specification-rev1.8***

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Chapter 1 Preface

This chapter describes the scope, structure, and writing standards of this manual to help users quickly find the information they need.

1.1 Introduction of the Manual

This manual serves as a user guide for the SGMII 1GbE IP product launched by Shenzhen Pango Microsystems Co., Ltd., mainly including IP usage guidelines and relevant information. Users can quickly understand the relevant features and methods of using the SGMII 1GbE IP through this manual.

1.2 Writing Standards of the Manual

Table 1-1 Description of Writing Standards

Text	**Rules**
Attention	If users ignore the attention contents, they may suffer adverse consequences or fail to operate successfully due to incorrect actions.
Description	Instructions and tips provided for users.
Recommendation	Recommended settings and instructions for users.

Chapter 2 IP User Guide

This chapter provides a usage guide for the SGMII 1GbE IP, including IP introduction, IP block diagram, IP generation process, Example Design, IP interface description, IP register description, typical applications, descriptions and considerations, and IP debugging methods. More details on the design process can be found in the following PDS help documentation.

- "***Pango_Design_Suite_Quick_Start_Tutorial***"
- "***Pango_Design_Suite_User_Guide***"
- "***IP_Compiler_User_Guide***"
- "***Simulation_User_Guide***"

2.1 IP Introduction

The SGMII 1GbE IP is designed by Shenzhen Pango Microsystems Co., Ltd. for realising the Ethernet SGMII interface. Users can configure and generate the IP module using the IPC (IP Compiler) tool within the PDS (Pango Design Suite).

2.1.1 Key Features

The SGMII 1GbE IP is designed by Pango Microsystems according to the "***IEEE802.3-2012 Specification and Serial-GMII Specification-rev1.8***", with the following main features.

- Supports GMII interface;
- Supports APB or MDIO for configuration management interface;
- Supports simple and fast configuration through ports;
- Supports auto-negotiation function;
- Supports GE mode and 10/100/1000Mbps SGMII mode;
- Supports dynamic switching between SGMII mode and GE mode;
- Supports clock frequency deviation correction to adapt to Ethernet's ±100ppm frequency difference;
- Supports Loopback function.

2.1.2 Applicable Devices and Packages

Table 2-1 SGMII 1GbE IP Applicable Devices and Package

Applicable Devices	**Supported Packages**
PG2L100H	ALL (except for MBG324)
PG2L50H	ALL (except for FBG256/MBG324)
PG2L25H	ALL
PG2L200H	ALL
PG2L100HX	ALL (except for MBG324)

2.2 IP Block Diagram

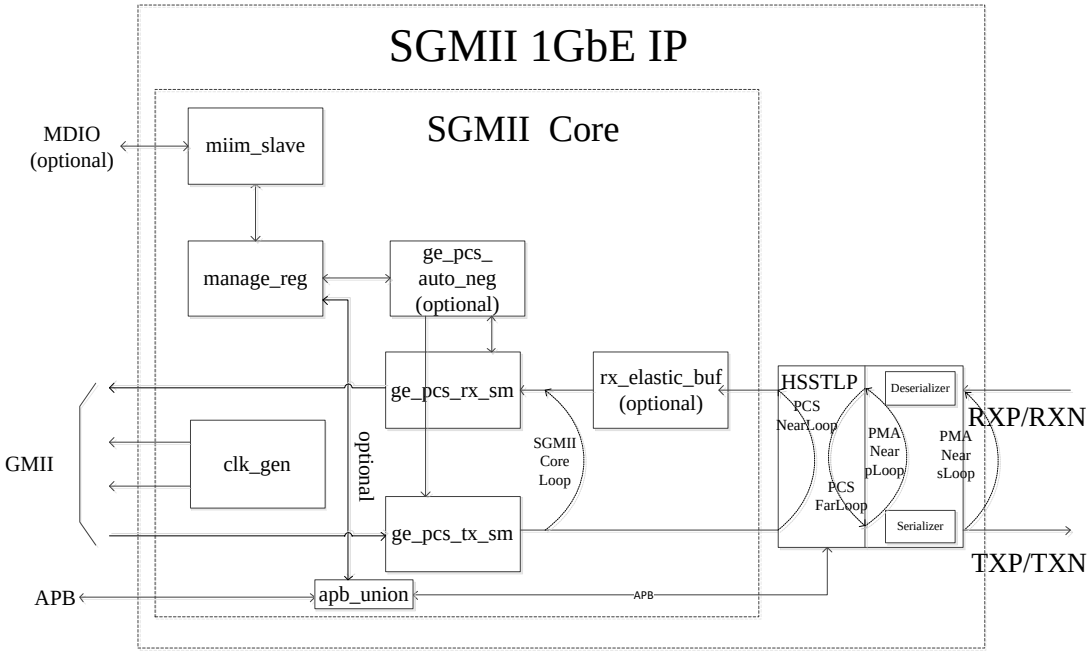

Figure 2-1 SGMII 1GbE IP System Block Diagram

The SGMII 1GbE IP consists of the SGMII Core and the HSSTLP IP, and the system block diagram is shown in Figure 2-1. Herein, the SGMII Core completes Auto-Negotiation and receiving/transmitting state machines among other functions; HSSTLP IP completes PCS encoding/decoding, PMA serial-to-parallel and parallel-to-serial conversion, and clock recovery among other functions. The dashed lines in the diagram indicate the data stream during loopback; for loopback configuration methods, please refer to "2.8.4 Loopback Mod".

2.3 IP Generation Process

2.3.1 Module Instantiation

Customised configurations of the SGMII 1GbE IP can be completed using the IPC tool, instantiating the required IP modules. For detailed instructions on using the IPC tool, please refer to "***IP_Compiler_User_Guide***".

The main operational steps for instantiating the SGMII 1GbE IP module are described as follows.

2.3.1.1 Selecting IP

Open IPC and click File > Update in the main window to open the Update IP dialog box, where you add the corresponding version of the IP model.

After selecting the FPGA device type, the Catalog interface can display all loaded IP models. Select the corresponding version of SGMII 1GbE under the System/Ethernet directory; the IP selection path interface is as shown in Figure 2-2. Then set the Pathname and Instance Name on the right side of the page. The project instantiation interface is shown in Figure 2-3.

Attention:

Be sure to use the software of version 2022.2 or above.

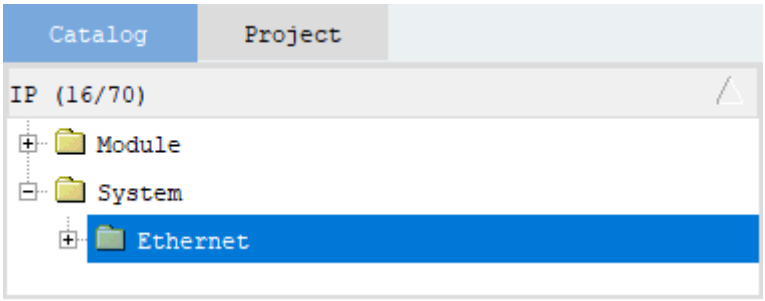

Figure 2-2 SGMII 1GbE IP Selection Path Interface

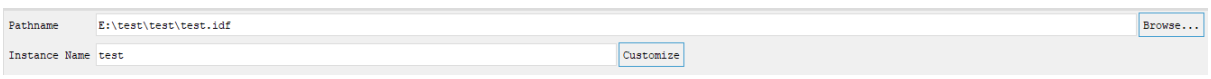

Figure 2-3 Project Instantiation Interface

2.3.1.2 IP Parameter Configuration

After selecting the IP, click <Customize> to enter the SGMII 1GbE IP parameter configuration interface. The left Symbol is the interface block diagram, as shown in Figure 2-4; the Parameter Configuration window is shown on the right side, as shown in Figure 2-5.

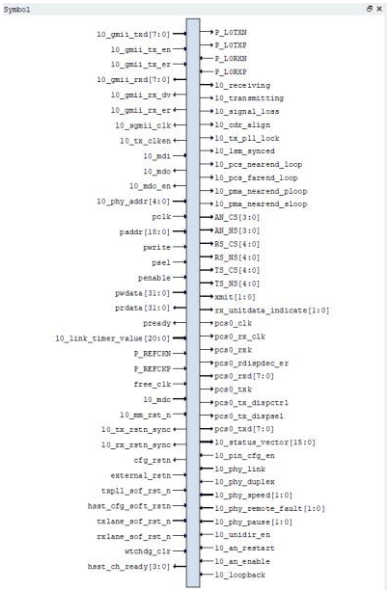

Figure 2-4 SGMII 1GbE IP Interface Block Diagram

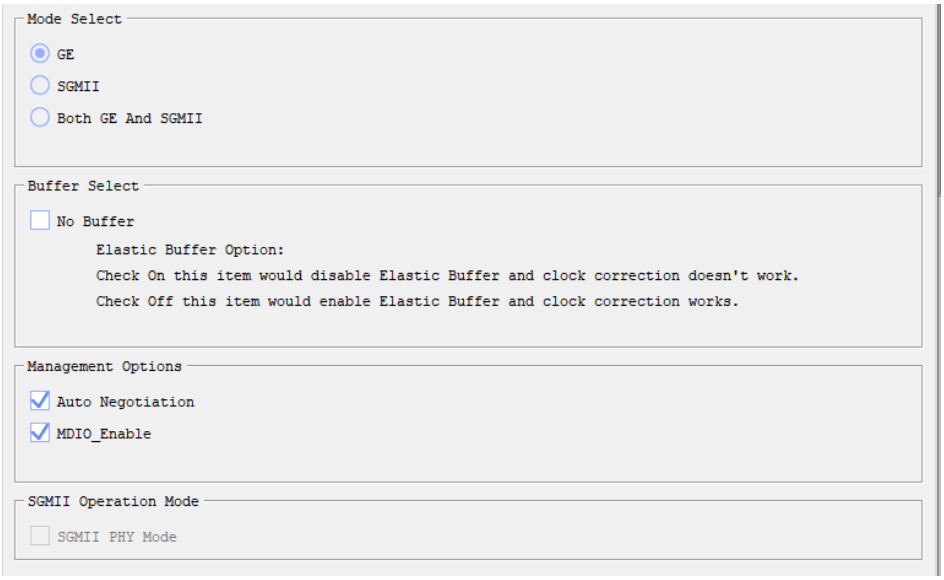

Figure 2-5 Configuration Interface for SGMII 1GbE IP Parameters

Table 2-2 SGMII 1GbE IP Configuration Parameter Explanation

Option Domain	Option Name/Parameter Name	Parameter Description	Default Value
Mode Select	GE	Select GE mode Check: IP operates in GE mode	Selected
	SGMII	SGMII mode selection Check: IP operates in SGMII mode	Cleared
	Both GE And SGMII	Select Both GE And SGMII Mode Check: IP operates in Both GE And SGMII mode	Cleared
Buffer Select	No Buffer	Frequency offset Buffer not enabled selection Check: IP Clock Skew Buffer is not enabled For detailed information please refer to "2.8.5 IP Clock Scheme"	Cleared
Management Options	Auto Negotiation	Select whether to enable auto-negotiation Check: IP enable Auto-Negotiation	Selected
	MDIO_Enable	Select MDIO Configuration Management Interface Enable Check: IP enables the MDIO Configuration Management Interface	Selected
SGMII Operation Mode	SGMII PHY Mode	Select SGMII PHY mode Selected: IP operates in PHY mode Cleared: IP operates in MAC mode	-

Note: "-" indicates that under GE mode, this option is invalid and there is no default value for it in the IP configuration interface.

2.3.1.3 Generating IP

After completing the parameter configuration, click the <Generate> button in the top left corner to produce the SGMII 1GbE IP code corresponding to the user specific settings. The information report interface for IP generation is shown in Figure 2-6.

Figure 2-6 SGMII 1GbE IP Generation Report Interface

After successful IP generation, it will output the files as shown in Table 2-3 under the project path specified in Figure 2-3.

Table 2-3 Output Files After SGMII 1GbE IP Generation

Output File[1]	**Description**
$instname.v	The top-level .v file of the generated IP.
$instname.idf	The Configuration file of the generated IP.
/rtl/*.v	The plaintext RTL files of the generated IP.
/rtl/common/*.v	The plaintext RTL files of the generated IP, where the folder contains some common modules.
/rtl/hsstlp/*	This folder contains the HSSTLP IP modules.
/rtl/synplify/*.vp	The nonplaintext RTL files of the generated IP, used for synthesis.
/sim_lib/modelsim/*.vp	The nonplaintext RTL files of the generated IP, which can be used for ModelSim or VCS simulation.
/sim/modelsim/*.f	The list of .v files required for ModelSim simulation of the generated Example Design.
/sim/modelsim/*.do	The .do script files and .do waveform files for ModelSim simulation of the generated Example Design.
/sim/modelsim/*.bat	The script for ModelSim simulation of the generated Example Design.
/example_design/bench/ *.v	The simulation stimulus files for the Example Design.
/example_design/rtl/*.v	The top-level file of the Example Design and some module files used in the design.
/pnr/core_only/*.pds	The project file of the generated IP core.
/pnr/core_only/*.fdc	The constraint file of the generated IP core.
/pnr/core_only/*.v	The top-level file of the generated IP core project.
/pnr/example_design/ *.pds	The project file of the Example Design.
/pnr/example_design/ *.fdc	The constraint file of the generated Example Design.
/rev_1	The default output path for synthesis reports. (This folder is generated only after specifying the synthesis tool)
/readme.txt	The readme file describes the structure of the generation directory after the IP is generated.

Attention:

The .pds and .fdc files generated with the IP are for reference only; please modify the pin constraints according to the actual pin connections when in use.

The *_vpAll.vp file in the *.vp file includes the contents of other *.vp files, selecting this file is equivalent to selecting all other *.vp files; users can choose based on their preferences, but both cannot be selected at the same time, otherwise, an error will occur. The same applies to _simvpAll.vp.

1 "$instname" is the instantiation name entered by the user; "*" is a wildcard character representing filenames of the same type.

2.3.2 Constraint Configuration

For the specific configuration method of constraint files, please refer to the relevant help documents in the PDS installation path: "***User_Constraint_Editor_User_Guide***", "***Physical_Constraint_Editor_User_Guide***", "***Route_Constraint_Editor_User_Guide***".

2.3.3 Simulation Runs

The simulation of the SGMII 1GbE IP is conducted using the Test Bench of the Example Design. For detailed information about Example Design, please refer to "2.4 Example Design".

For more details about the PDS simulation functions and third-party simulation tools, please consult the related help documents in the PDS installation path: "***Pango_Design_Suite_User Guide***", "***Simulation_User_Guide***".

2.3.4 Synthesis and Placement/Routing

The specific usage of PDS synthesis tools and placement/routing tools can be found in the help documents within the PDS installation path.

Attention:

The "Example Design" project files .pds and the pin constraint files .fdc generated with the IP are located in the "/pnr/example_design" directory. Physical constraints must be adjusted according to the actual device used and PCB board trace, for details, please refer to "2.8 Descriptions and Considerations".

2.3.5 Resources Utilization

Table 2-4 Typical Resource Utilization Values for the SGMII 1GbE IP Based on Applicable Devices

Device	IP Operating Mode (Parameter check options)	Typical Resource Utilization Values				
		LUT	FF	USCM	HSSTLP	DRM
PG2L100H	GE Auto Negotiation MDIO_Enable	814	864	3	1	0
	SGMII MDIO_Enable	764	822	4	1	0.5
	Both GE And SGMII	695	749	3	1	0.5
	Both GE And SGMII No Buffer	526	519	3	1	0
PG2L50H	GE Auto Negotiation MDIO_Enable	801	864	3	1	0
	SGMII MDIO_Enable	762	818	4	1	0.5
	Both GE And SGMII	692	748	3	1	0.5
	Both GE And SGMII No Buffer	527	522	3	1	0
PG2L25H	GE Auto Negotiation MDIO_Enable	812	865	3	1	0
	SGMII MDIO_Enable	764	821	4	1	0.5
	Both GE And SGMII	694	749	3	1	0.5
	Both GE And SGMII No Buffer	531	521	3	1	0
PG2L200H	GE Auto Negotiation MDIO_Enable	791	866	3	1	0
	SGMII MDIO_Enable	764	830	4	1	0.5
	Both GE And SGMII	694	755	3	1	0.5
	Both GE And SGMII No Buffer	509	523	3	1	0
PG2L100HX	GE Auto Negotiation MDIO_Enable	772	865	3	1	0
	SGMII MDIO_Enable	738	830	4	1	0.5
	Both GE And SGMII	677	755	3	1	0.5
	Both GE And SGMII No Buffer	496	523	3	1	0

2.4 Example Design

This section introduces the Example Design scheme for the SGMII 1GbE IP based on Both GE And SGMII modes[2]. The scheme instantiates both a MAC Side SGMII 1GbE IP and a PHY Side SGMII 1GbE IP, which negotiate automatically, then send data, and verify the correctness of the received data through CRC checks. The scheme performs read and write register operations on the SGMII Core via the MDIO interface.

Descirption:

The registers of HSSTLP IP can only be accessed through the APB interface.

2.4.1 Design Block Diagram

The system block diagram of the Example Design is as shown in Figure 2-7. Herein, Ⓜ denotes a selector, which according to the selection enable, transfers the output data of the respective test board to the host computer.

2 This Example Design scheme is only applicable to PG2L100H FBG676.

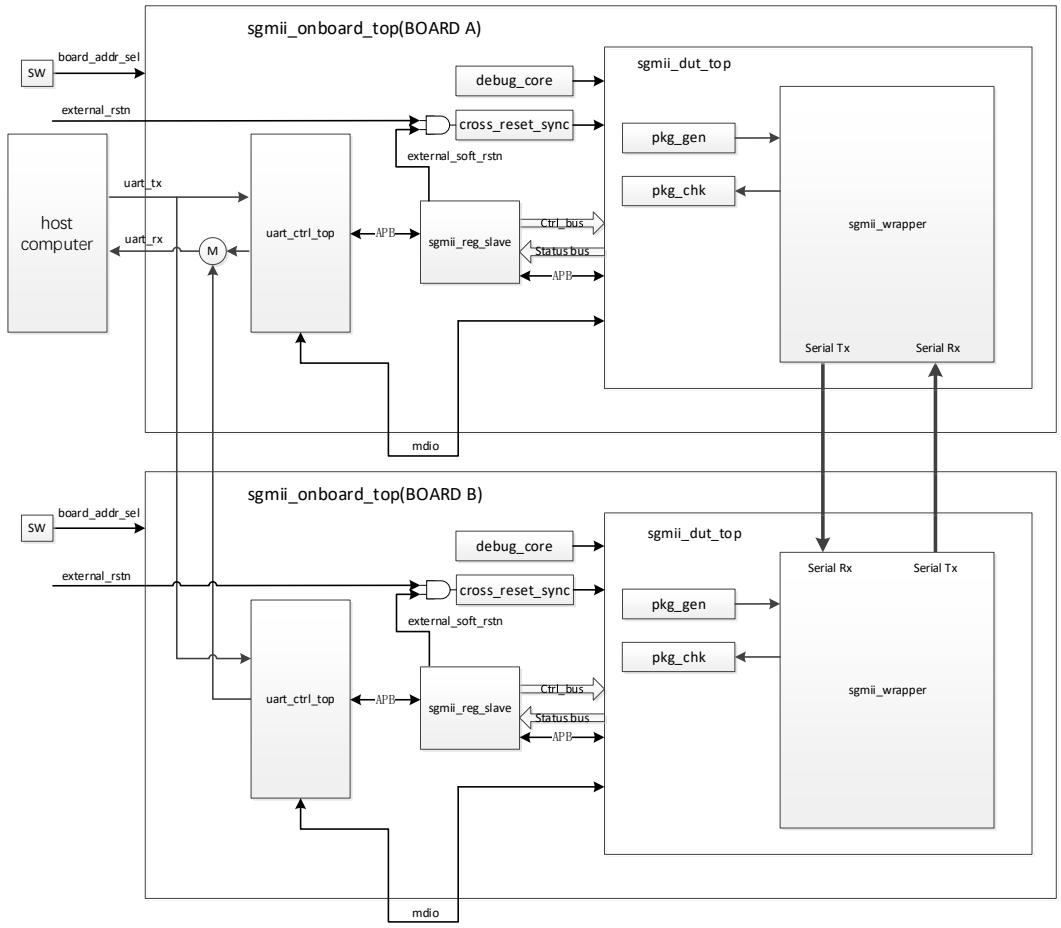

Figure 2-7 Both GE And SGMII mode Example Design Block Diagram

2.4.2 Module Description

2.4.2.1 uart_ctrl_top

A serial port module used for debugging, for receiving UART data with a fixed baud rate of 115200, outputting in data formats required by APB or MDIO protocols. For read and write operations, the address is 24 bits, and the data is 32 bits.

2.4.2.1.1 Read and Write Operation Description

- Read operation format: "0x72" + "address";
- Write operation format: "0x77" + "address" + "data".

For the read and write operation examples, please refer to "2.8.6 Example of read and write operations for the uart_ctrl_top module".

2.4.2.1.2 Address description

For information about the address for accessing registers through the uart_ctrl_top module, please refer to Table 2-5.

Table 2-5 uart_ctrl Module Address Description

Address bits	Description
23	Single board address (used only for debugging)
22	0: Access registers via the APB interface. 1: Access registers via the MDIO interface.
21	Select the access object via the APB interface (valid when accessing registers via the APB interface) 0: Access sgmii_reg_slave module register 1: Access IP register
20:19	Not used (set to 0)
18:0	IP register address[3]

2.4.2.2 sgmii_reg_slave

For the custom register module used for debugging, please refer to Table 2-6 for relevant register descriptions.

Table 2-6 sgmii_reg_slave Register Description

Register address (16bit)	R/W	Description	Default value (32 bits)
0x0000	W	bit0: ge_or_sgmii 1'b0: GE mode 1'b1: SGMII mode The remaining bits are non-functional	0x10

3 For addresses of IP registers, please refer to "2.6 Description of the IP Register", and for register addresses within the sgmii_reg_slave module, please refer to Table 2-6.

Register address (16bit)	R/W	Description	Default value (32 bits)
0x0001	W	bit28: pin_cfg_en 1'b0: Fast port configuration invalid 1'b1: Enable fast port configuration bit26: phy_duplex bit[25:24]: phy_pause bit22: phy_link bit [17:16]: phy_speed (valid under SGMII mode) 2'b11: Reserved 2'b10: SGMII 1000Mbps 2'b01: SGMII 100Mbps 2'b00: SGMII 10Mbps bit4: an_enable 1'b0: Disable auto-negotiation 1'b1: Enable auto-negotiation bit0: an_restart 1'b0: Disable auto-negotiation restart 1'b1: Enable auto-negotiation restart	0x07420010
0x0004	W	bit0: start_test 1'b0: Disable packet transmission 1'b1: Enable packet transmission	0x0

2.4.2.3 debug_core

PDS includes IP modules for debugging, which allows waveform capture and viewing of specific signals in certain modules via the Fabric Debugger tool. Specific usage can be found in the help documentation under the PDS installation path.

2.4.2.4 cross_reset_sync

Asynchronous signal synchronisation module, used for synchronising and debouncing externally input asynchronous signals.

2.4.2.5 pkg_gen

Data generation module, used for producing transmission data.

2.4.2.6 pkg_chk

Data detection module, used for CRC verification of received data.

2.4.2.7 sgmii_wrapper

SGMII 1GbE IP top layer.

2.4.3 Descriptions of Ports

Refer to Table 2-7 for the interface description of Example Design.

Table 2-7 Example Design Interface List

Port Name	Bit width	I/O	PORT Description	Pin constraints
free_clk	1	I	External reference clock[4] Frequency: 50MHz	G5
external_rstn	1	I	System reset signal 0: Reset 1: Reset release	AA23
hsst_cfg_soft_rstn	1	I	HSSTLP IP configuration parameter reset signal 0: Reset 1: Reset release	AA22
P_REFCKN	1	I	HSSTLP IP differential reference clock input N-terminal Frequency: 125MHz	E13
P_REFCKP	1	I	HSSTLP IP differential reference clock input P-terminal Frequency: 125MHz	F13
P_L0TXN	1	O	HSSTLP IP differential serial output signal N-terminal	-
P_L0TXP	1	O	HSSTLP IP differential serial output signal P-terminal	-
P_L0RXN	1	I	HSSTLP IP differential serial input signal N-terminal	-
P_L0RXP	1	I	HSSTLP IP differential serial input signal P-terminal	-
LED50M1S	1	O	free_clk clock indicator[5]	V24
LED125M1S	1	O	125MHz differential clock indicator[5]	AA25
ok_led	1	O	Packet reception verification correct indicator 0: Light off (verification error) 1: Light on (verification correct)	W25
cfg_uart_txd	1	O	Local port for sending data to the host computer	C24
cfg_uart_rxd	1	I	Local port for receiving data from the host computer	D24
uart_rxd_to_partner	1	O	Port for sending data from local side to remote side	B19
uart_txd_from_partner	1	I	Port for receiving data sent from remote side to local side	B20

4 Used as the APB pclk and the HSSTHP reset clock in this Example Design.

5 blinks once every second under normal conditions.

Port Name	Bit width	I/O	PORT Description	Pin constraints
l0_cdr_align	1	O	HSSTLP IP PMA CDR lock indicator (connected to l0_cdr_align port) 0: Light off (unlocked) 1: Light on (locked)	W24
l0_tx_pll_lock	1	O	HSSTLP IP PLL lock indicator (connected to l0_tx_pll_lock port) 0: Light off (unlocked) 1: Light on (locked)	AA24
l0_lsm_synced	1	O	HSSTLP IP Word Align alignment indicator (connected to l0_lsm_synced port) 0: Light off (not aligned) 1: Light on (aligned)	AC24
l0_an_status	1	O	SGMII 1GbE IP link status indicator 0: Light off (link issue) 1: Light on (link normal)	AB25
master_mdc_o	1	O	MDIO output clock (generated by the serial port module)	D4
master_mdio	1	IO	MDIO data signal	A20
slave_l0_mdc	1	I	MDIO input clock (connected to master_mdc_o)	E5
slave_l0_mdio	1	IO	MDIO data signal (connected to master_mdio)	A19
l0_ctrl3	1	I	Single board serial port address control signal 0: Board A 1: Board B	T24

Note: "-" indicates location constraint has been applied through HSSTLP-related constraints.

2.4.4 Test Method

Generate the bitstream by instantiating the SGMII 1GbE IP of corresponding mode[6], using the IP built-in Example Design project[7]. Use two test boards[8]for docking tests; one with the MAC Side bitstream programmed, and the other with the PHY Side bitstream programmed; evaluate the test results based on the link indicators and CRC verification.

The debug_core module has been included in Example Design; board-to-board docking tests can be performed using the Fabric Debuggertool in the PDS software to capture PCS transmitter/receiver data and to tally packet transmission information, as shown in screenshots Figure 2-8, Figure 2-9, and Figure 2-10. Users may add or remove signals to be captured according to actual needs. For the

6 For details, please refer to "2.4.5 Instance Configuration" and "2.3.1 Module Instantiation".

7 For the Example Design project path, see Table 2-3.

8 The model number of the PG2L100H test board is P04I100RD04_A2.

description of debug_core signals, please refer to Table 2-8.

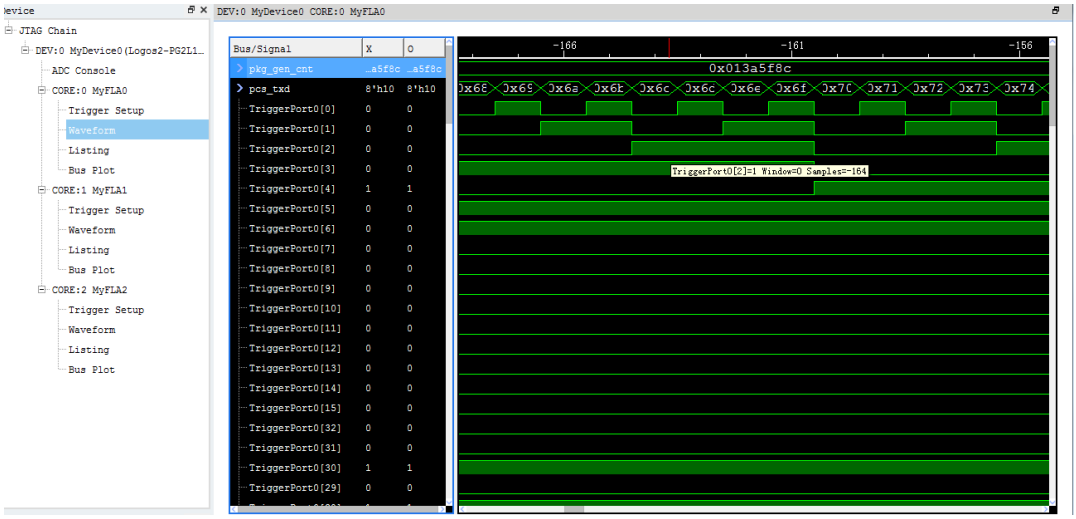

Figure 2-8 Data at PCS Transmitter

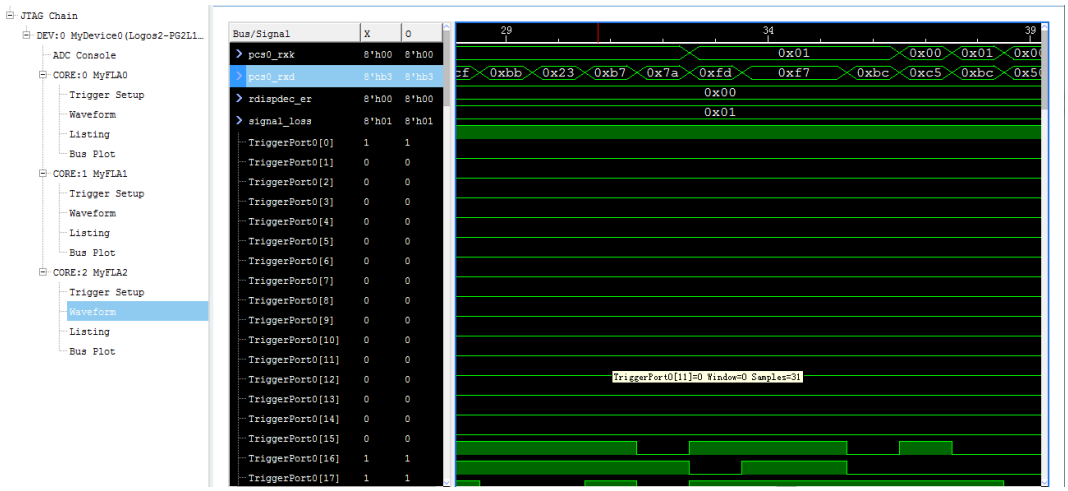

Figure 2-9 Data at PCS Receiver

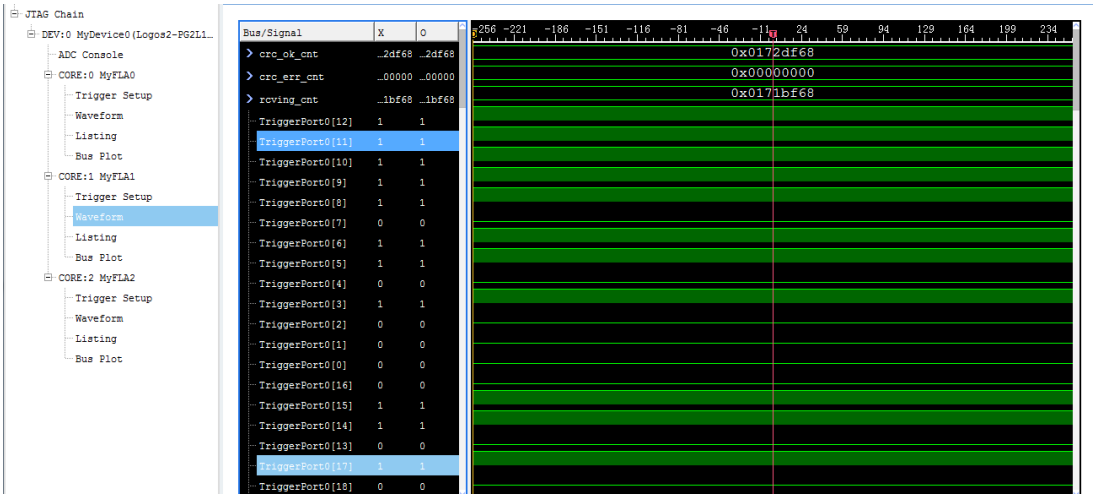

Figure 2-10 GMII-side Packet Reception Statistics

Table 2-8 debug_core Signal Explanation

debug_core numbering	**TriggerPort**	**Signal Name**
debug_core0	TriggerPort0[0]~ TriggerPort0[7]	pcs0_txd[0]~ pcs0_txd[7]
	TriggerPort0[8]	pcs0_txk
	TriggerPort0[9]~ TriggerPort0[15]	7'h0
	TriggerPort0[16]~ TriggerPort0[47]	pkg_gen_cnt[0]~ pkg_gen_cnt[31]
	TriggerPort0[48]~ TriggerPort0[127]	80'h0
debug_core1	TriggerPort0[0]~ TriggerPort0[31]	rcving_cnt[0]~ rcving_cnt[31]
	TriggerPort0[32]~ TriggerPort0[63]	crc_err_cnt[0]~ crc_err_cnt[31]
	TriggerPort0[64]~ TriggerPort0[95]	crc_ok_cnt[0]~ crc_ok_cnt[31]
	TriggerPort0[96]~ TriggerPort0[127]	32'h0
debug_core2	TriggerPort0[0]	signal_loss
	TriggerPort0[1]~ TriggerPort0[7]	7'h0
	TriggerPort0[8]	rdispdec_er
	TriggerPort0[9]~ TriggerPort0[15]	7'h0
	TriggerPort0[16]~ TriggerPort0[23]	pcs0_rxd[0]~ pcs0_rxd[7]
	TriggerPort0[24]	pcs0_rxk
	TriggerPort0[25]~ TriggerPort0[127]	103'h0

2.4.5 Instance Configuration

2.4.5.1 MAC Side

Figure 2-11 Both GE And SGMII Mode MAC Side Configuration

2.4.5.2 PHY Side

Figure 2-12 Both GE and SGMII Mode PHY Side Configuration

2.4.6 Instance Simulation

Under the Windows operating system, after the IP is generated, simulation can be run by double-clicking the "*.bat file[9]" in the <project_path>/sim/modelsim directory.

2.5 Descriptions of IP Interfaces

This section provides an overview of the SGMII 1GbE IP interface descriptions and timing diagram.

9 For the output files after IP generation, please refer to Table 2-3.

2.5.1 IP Interface Description

2.5.1.1 IP Interface Block Diagram

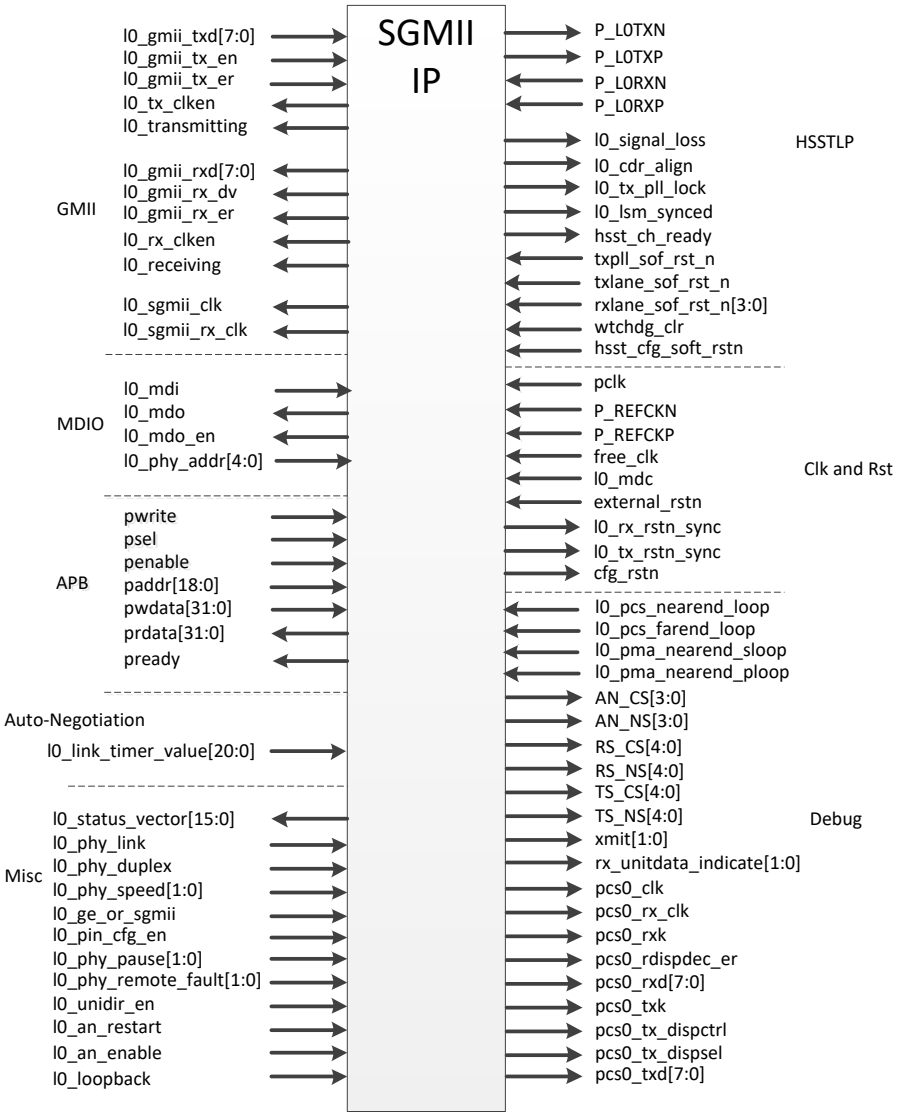

Figure 2-13 SGMII 1GbE IP Interface

2.5.1.2 IP Interface List

Table 2-9 SGMII 1GbE IP Interface Signal List

Port	I/O	Bit width	Description
Clock Signal			
l0_mdc	Input	1	Management Data Clock (for MDIO interface clock) This port must have a clock input when MDIO is enabled Frequency: 2.5MHz
pclk	Input	1	APB Clock (for APB interface clock) Frequency: 50MHz~100MHz
P_REFCKN	Input	1	Differential Clock N-terminal used for HSSTLP IP Frequency: 125MHz
P_REFCKP	Input	1	Differential Clock P-terminal used for HSSTLP IP Frequency: 125MHz
free_clk	Input	1	Reset sequence reference clock for HSSTLP IP Frequency: 10MHz~100MHz
Reset signal			
external_rstn	Input	1	Global asynchronous reset signal (free_clk clock domain) 0: Reset 1: Reset release
l0_rx_rstn_sync	Output	1	HSSTLP IP RX end reset signal 0: Reset 1: Reset release Note: HSSTLP IP RX side reset completion indication (consistent with the receive-side data clock domain)
l0_tx_rstn_sync	Output	1	HSSTLP IP TX end reset signal 0: Reset 1: Reset release Note: HSSTLP IP TX side reset completion indication (consistent with the transmit-side data clock domain)
cfg_rstn	Output	1	Configuration reset signal output by SGMII Core (free_clk clock domain) 0: Reset 1: Reset release
HSSTLP IP Side Signals			
P_L0TXN	Output	1	HSSTLP IP transmission differential signal N-terminal
P_L0TXP	Output	1	HSSTLP IP transmission differential signal P-terminal
P_L0RXN	Input	1	HSSTLP IP reception differential signal N-terminal
P_L0RXP	Input	1	HSSTLP IP reception differential signal P-terminal
l0_signal_loss	Output	1	Invert the "P_RX_SIGDET_STATUS"[10] value corresponding to HSSTLP IP 0: Indicates a valid signal was detected from the port P_L*RXP/ P_L*RXN 1: Indicates no valid signal was detected from the port P_L*RXP/ P_L*RXN Note: This is an asynchronous signal.

10 Please refer to "***UG041004_HSSTLP_IP***"

Port	I/O	Bit width	Description
l0_cdr_align	Output	1	Corresponding to "P_RX_READY" for HSSTLP IP[10] 0: Indicates CDR lock signal not established 1: Indicates CDR lock signal successfully established Note: This is an asynchronous signal.
l0_tx_pll_lock	Output	1	Corresponding to "P_PLL_READY" for HSSTLP IP[10] 0: PLL not locked 1: PLL locked Note: This is an asynchronous signal.
l0_lsm_synced	Output	1	Synchronization status signal, corresponding to "P_PCS_LSM_SYNCED" for HSSTLP IP[10], 0: Word Align unsuccessful 1: Word Align successful Note: This is an asynchronous signal.
hsst_ch_ready[3:0]	Output	4	HSSTLP IP Serdes RX channel reset completion flag (free_clk clock domain) 0: Incomplete: 1: complete: Bit0~Bit3 correspond to Lane0~Lane3 respectively
txpll_sof_rst_n	Input	1	HSSTLP IP PLL soft reset (free_clk clock domain) 0: Reset 1: Reset release
txlane_sof_rst_n	Input	1	HSSTLP IP Serdes TX channel soft reset (free_clk clock domain) 0: Reset 1: Reset release For debugging use only, and RX reset is required after TX reset
rxlane_sof_rst_n[3:0]	Input	4	HSSTLP IP Serdes RX channel soft reset (free_clk clock domain) 0: Reset 1: Reset release Bit0~Bit3 correspond to Lane0~Lane3 respectively For debugging use only (IP defaults to Lane0)
wtchdg_clr	Input	1	HSSTLP IP reset sequence watchdog clear signal (free_clk clock domain) 0: Normal Operation 1: Watchdog counter zero For debugging use only
hsst_cfg_soft_rstn	Input	1	HSSTLP IP configuration module soft reset signal (free_clk clock domain) 0: Reset 1: Reset release A global reset is required after enabling this reset
GMII Signals			
l0_gmii_txd[7:0]	Input	8	GMII TXD[7:0] signal
l0_gmii_tx_en	Input	1	GMII TX_EN signal
l0_gmii_tx_er	Input	1	GMII TX_ER signal
l0_transmitting	Output	1	PCS transmits status signal 1: PCS signal transmission in progress 0: No PCS signal transmission
l0_gmii_rxd[7:0]	Output	8	GMII RXD[7:0] signal
l0_gmii_rx_dv	Output	1	GMII RX_DV signal
l0_gmii_rx_er	Output	1	GMII RX_ER signal

Port	I/O	Bit width	Description
l0_receiving	Output	1	PCS recives status signal 1: PCS signal reception in progress 0: No PCS signal reception
l0_sgmii_clk	Output	1	GMII operating clock Frequency: 125MHz
l0_sgmii_rx_clk	Output	1	GMII receives working clock (used in No_Buffer mode) Frequency: 125MHz
l0_tx_clken	Output	1	GMII TXD clock enable signal (active high) GE mode: full high level SGMII mode: (related to PHY Device Speed) Speed=11: Reserved Speed=10: SGMII 1000Mbps (full high level) Speed =01: SGMII 100 Mbps (generates a pulse every 10 clock cycles) Speed =00: SGMII 10 Mbps(generates a pulse every 100 clock cycles)
l0_rx_clken	Output	1	GMII RXD clock enable signal (Used in No_Buffer mode, active high) GE mode: full high level SGMII mode: (related to PHY Device Speed) Speed=11: Reserved Speed =10: SGMII 1000 Mbps (full high level) Speed =01: SGMII 100 Mbps (generates a pulse every 10 clock cycles) Speed =00: SGMII 10 Mbps (generates a pulse every 100 clock cycles)
Status Signals			
l0_status_vector [15:0]	Output	16	Output state statistical vector Bit[15]:Resolve Priority: Controls the Invocation of the Priority Resolution Function. This signal is pulled high in the Auto-Negotiation IDLE_DETECT and LINK_OK states, and low in other states Bit[14]:an_complete: Auto-negotiation completion indication: 1: complete: 0: Not completed Bit[13]:an_page_rx: Indication of new configuration data received by Auto-Negotiation 1: New configuration data received 0: New configuration data not received Bit[12]:rxdisp_er: 10B/8B decoding polarity error indication 1: Incorrect polarity 0: Correct polarity Bit[11]:rxdec_er: 10B/8B decoding data error indication 1: Data error 0: Data correct Bit[10:9]:Remote Fault Encode: Link status passed by Link Partner received from auto-negotiation SGMII MAC mode: 10: Link abnormal 00: Link normal

Port	I/O	Bit width	Description
			In SGMII PHY mode: Fixed to 0: Under GE mode: 00:No Error, Link OK. 01:Offline 10:Link Failure 11:Auto-Negotiation_Error Bit[8:7]:Pause: Pause capability of Link Partner received from Auto-Negotiation (valid in GE mode) Bit[6]: elastic Buffer state: 1: Overflow 0 : No overflow Bit[5]: Indication for half-duplex/full-duplex: 1: Full duplex 0: Half duplex Bit[4:3]: SGMII rate indication: 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps Bit[2:1]:RUDI: 00: Reserved 01: Invalid (an error occurred while receiving C-code or I-code) 10: /C/ (receiving C-code) 11: /I/ (receiving I-code) Bit[0]: Auto-Negotiation related port, Link Status When auto-negotiation is enabled: 1: Synchronization successful and auto-negotiation completed 0: Synchronization failed or Auto-Negotiation incomplete When auto-negotiation is disabled: 1: Synchronization successful 0: Synchronization failed
Fast Configuration Interface[11]			
l0_pin_cfg_en	Input	1	Fast configuration enable signal[12] 1: Fast configuration interface valid 0: Fast configuration interface invalid
l0_phy_link	Input	1	PHY Link status (meaningful in SGMII PHY mode) 1:Link Up 0:Link Down Corresponding to register Reg4.15
l0_phy_duplex	Input	1	PHY duplex status (meaningful in SGMII PHY mode) 1: Full duplex 0: Half duplex Corresponding to register Reg4.12

11 This group of signals needs to be generated in the clock domain (mdc/free_clk) of the management interface (MDIO/APB).

12 Fast configuration of registers only affects Reg0 and Reg4, and does not affect other registers. Please refer to "2.5.3 Fast Configuration Interface" for details.

Port	I/O	Bit width	Description
l0_phy_speed	Input	2	PHY operational speed (meaningful in SGMII PHY mode) 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps Under SGMII PHY mode Corresponding to registers Rg4.11:10 when Auto-Negotiation is enabled Corresponding to registers {Reg0.6,Reg0.13} when Auto-Negotiation is disabled Under SGMII MAC mode Meaningless when auto-negotiation is enabled Corresponding to registers {Reg0.6,Reg0.13} when Auto-Negotiation is disabled
l0_phy_remote_fault	Input	2	Remote Fault (meaningful in GE mode) 11:Auto-Negotiation_Error 10:Link Failure 01:Off Line 00:No Error(Link Ok) Corresponding to register Reg4.13:12
l0_phy_pause	Input	2	Pause (meaningful in GE mode) 11:Both Symmetric PAUSE and Asymmetric PAUSE toward Local Device 10:Symmetric PAUSE 01:Asymmetric PAUSE toward Link Partner 00:No PAUSE Corresponding to register Reg4.8:7
l0_unidir_en	Input	1	Undirectional mode enable control 0: Not enabled 1: Enabled Corresponding to register Reg0.5
l0_an_restart	Input	1	Auto-negotiation restart control 0: Normal operation 1: Restart auto-negotiation Corresponding to register Reg0.9
l0_an_enable	Input	1	Auto-negotiation enable control 0: Not enabled 1: Enabled Corresponding to register Reg0.12
l0_loopback	Input	1	SGMII Core Loopback control[13] 0: Not enabled 1: Enabled Corresponding to register Reg0.14

13 Loopback functions cannot be used when frequency bias Buffer is not enabled.

Port	I/O	Bit width	Description
Operating Mode Configuration			
l0_ge_or_sgmii	Input	1	GE and SGMII mode selection (Both GE And SGMII modes) 0: GE mode 1:SGMII mode
MDIO Signals[14]			
l0_mdi	Input	1	Management Data In
l0_mdo	Output	1	Management Data Out
l0_mdo_en	Output	1	Output enable control signal 0: mdo invalid 1: mdo valid
l0_phy_addr	Input	5	Input MDIO PHY address[15]
APB Signals[16]			
pwrite	Input	1	APB write enable signal 0: Read data 1: Write data
psel	Input	1	APB interface Chip Select signal 0: Cleared 1: Selected
penable	Input	1	APB interface access enable 0: Not enabled 1: Enabled
paddr[18:0]	Input	19	APB interface read/write address bus
pwdata[31:0]	Input	32	APB interface write data bus
prdata[31:0]	Output	32	APB interface read data bus
pready	Output	1	APB interface read/write Ready signal For write operation: 0: Data has not been successfully written to the register 1: Data has been successfully written to the register For read operation: 0: Read data is not yet ready 1: Read data is now ready

14 Valid when configuring the management interface as MDIO (check "MDIO_Enable"), please refer to "2.3.1.2 IP Parameter Configuration".

15 MDIO read/write operations are valid if they match the PHY address on mdio; if not, invalid.

16 Valid when configuring the management interface as APB (uncheck "MDIO_Enable"), please refer to "2.3.1.2 IP Parameter Configuration".

Port	I/O	Bit width	Description
Auto-Negotiation			
l0_link_timer_value [20:0]	Input	21	link_timer_valve setting Under GE mode Set to: 10ms/8ns = 1250000 Under SGMII mode Set to: 1.6ms/8ns = 200000 For simulation Set to: 2us/8ns = 250
Debug Signal			
l0_pcs_nearend_loop	Input	1	PCS parallel near-end loopback enable 0: Not enabled 1: Enabled
l0_pcs_farend_loop	Input	1	PCS parallel far-end loopback enable 0: Not enabled 1: Enabled
l0_pma_nearend_sloop	Input	1	PMA serial near-end loopback enable 0: Not enabled 1: Enabled
l0_pma_nearend_ploop	Input	1	PMA parallel near-end loopback enable 0: Not enabled 1: Enabled
AN_CS[3:0]	Output	4	Current state of the Auto-Negotiation state machine (l0_sgmii_clk clock domain)
AN_NS[3:0]	Output	4	Next state of the Auto-Negotiation state machine (l0_sgmii_clk clock domain)
RS_CS[4:0]	Output	5	Current state of receive state machine[17]
RS_NS[4:0]	Output	5	Next state of receive state machine[17]
TS_CS[4:0]	Output	5	Current state of the transmit state machine (l0_sgmii_clk clock domain)
TS_NS[4:0]	Output	5	Next state of the transmit state machine (l0_sgmii_clk clock domain)
xmit[1:0]	Output	2	xmit signal output by the Auto-Negotiation state machine (l0_sgmii_clk clock domain) 00: Reserved 01: CONFIGURATION 10: DATA 11: IDLE
rx_unitdata_indicate [1:0]	Output	2	Data type indication received by PCS[17] (output to the Auto-Negotiation module) 00: Reserved 01: Invalid 10: /C/ 11: /I/
pcs_clk	Output	1	Corresponds to HSSTLP "P_TCLK2FABRIC_0"[18]

17 Operates in l0_sgmii_rx_clk clock domain under No Buffer mode, enables frequency offset Buffer mode operation in l0_sgmii_clk clock domain.

18 Please refer to "UG041004_HSSTLP_IP".

Port	I/O	Bit width	Description
pcs0_txk	Output	1	Corresponds to HSSTLP "P_TDATA_0[10]"[18]
pcs0_txd	Output	8	Corresponds to HSSTLP "P_TDATA_0 [7:0]"[18]
pcs0_tx_dispctrl	Output	1	Corresponds to HSSTLP "P_TDATA_0 [9]"[18]
pcs0_tx_dispsel	Output	1	Corresponds to HSSTLP "P_TDATA_0 [8]"[18]
pcs_rx_clk	Output	1	Corresponds to HSSTLP "P_RCLK2FABRIC_0"[18]
pcs0_rxk	Output	1	Corresponds to HSSTLP "P_RDATA_0[10]"[18]
pcs0_rxd	Output	8	Corresponds to HSSTLP "P_RDATA_0[7:0]"[18]
pcs0_rdispdec_er	Output	1	Result of the "OR" operation between HSSTLP "P_RDATA_0[8]" and "P_RDATA_0[9]"[18]

2.5.2 Configuration Management Interface

SGMII 1GbE IP provides two types of register configuration management interfaces—APB and MDIO interfaces. The "MDIO_Enable" in the interface configuration determines whether to enable the MDIO interface. For detailed descriptions, please refer to "2.3.1.2 IP Parameter Configuration".

- When the MDIO interface is disabled, SGMII 1GbE IP operates the registers of HSSTLP IP and SGMII Core through the APB interface.
- When the MDIO interface is enabled, SGMII 1GbE IP operates the registers of HSSTLP IP via the APB interface, and the registers of SGMII Core via the MDIO interface.

2.5.2.1 APB Interface Timing Description

2.5.2.1.1 APB Write Timing

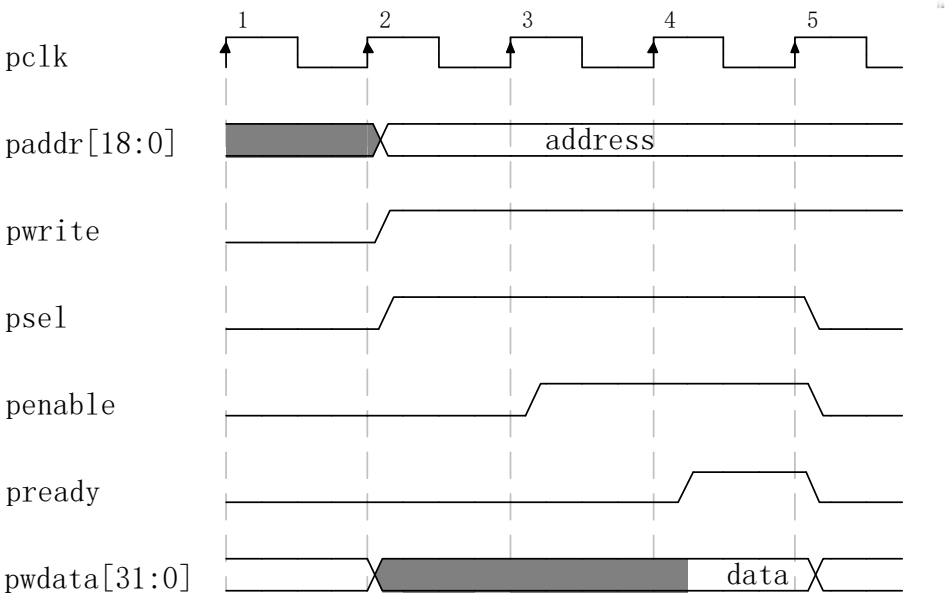

Figure 2-14 Basic APB Write Timing

2.5.2.1.2 APB Read Timing

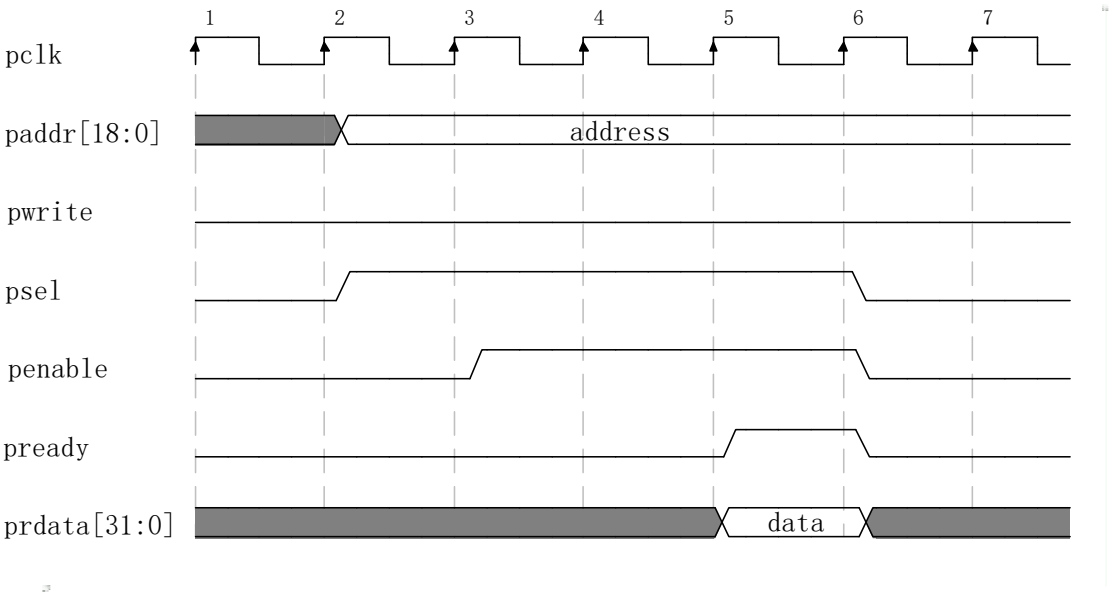

Figure 2-15 Basic APB Read Timing

2.5.2.2 MDIO Interface Timing Description

2.5.2.2.1 MDIO Write Timing

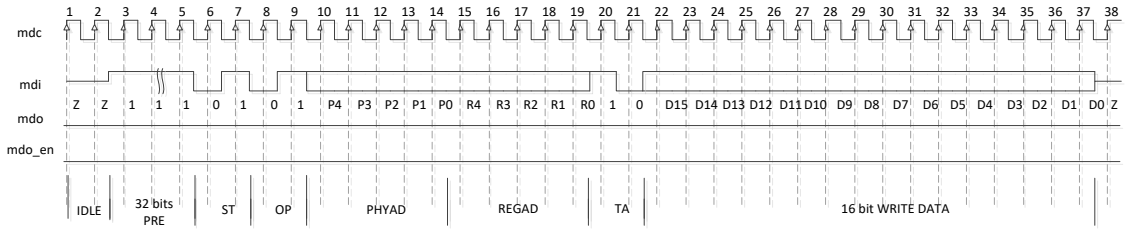

Figure 2-16 MDIO Write Timing

2.5.2.2.2 MDIO Write Timing

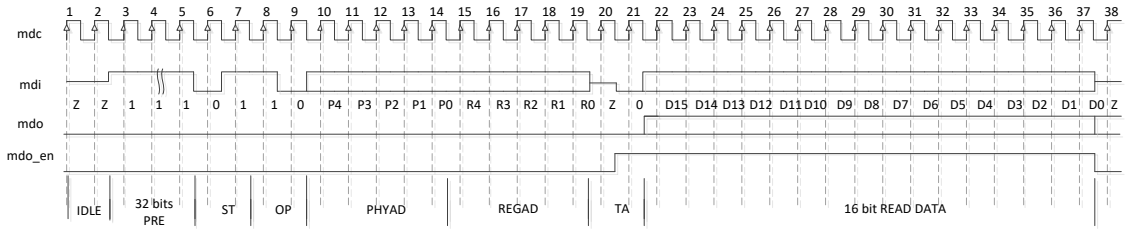

Figure 2-17 MDIO Write Timing

2.5.3 Fast Configuration Interface

The fast configuration interface allows for quick configuration of registers Reg0 and Reg4. When the fast configuration enable signal is active, the configuration information can be written directly to the corresponding configuration registers. Timing requirements are as follows:

- The fast configuration enable signal must be kept high for at least one configuration management interface clock cycle;
- The configuration information must remain stable for at least one configuration management interface clock cycle.

When the fast configuration enable signal is valid, registers other than Reg0 and Reg4 are written via the configuration management interface, and all registers are read via the configuration management interface; when the fast configuration interface enable signal is not valid, all registers are read and written via the configuration management interface.

2.5.4 GMII Interface

2.5.4.1 GE Mode

2.5.4.1.1 GMII Transmit Timing

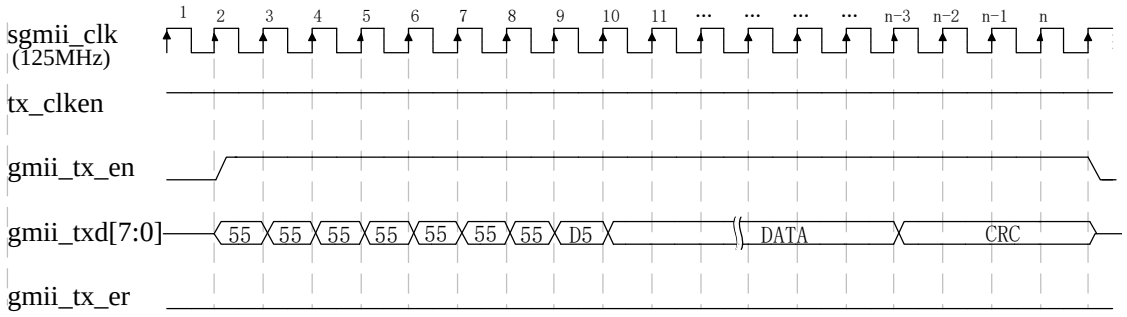

Figure 2-18 GE Mode GMII Transmit Timing

2.5.4.1.2 GMII Receive Timing

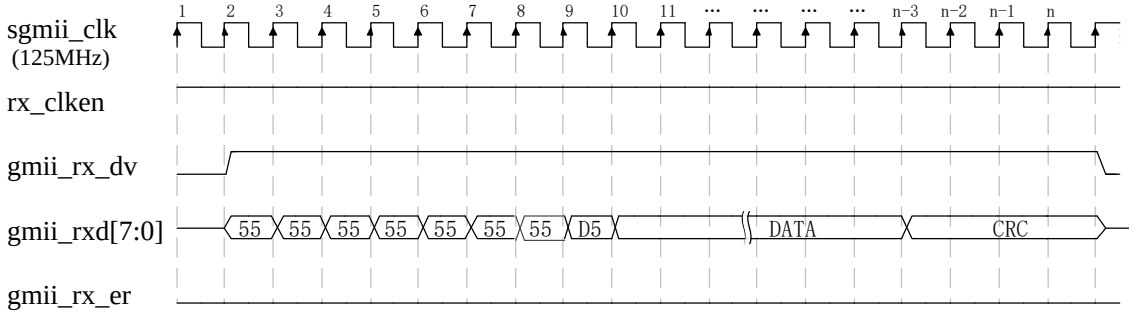

Figure 2-19 GE Mode GMII Receive Timing

2.5.4.2 SGMII Mode

2.5.4.2.1 GMII Transmit Timing

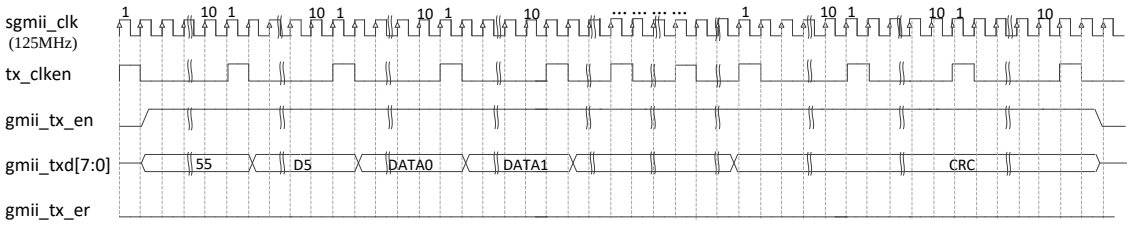

Figure 2-20 GMII Transmission Timing at 100Mbps in SGMII Mode

Attention:

In SGMII mode, at a rate of 10Mbps, tx_clken is pulled high once every 100 cycles of the 125MHz clock, with each data bit lasting 100 cycles of the 125MHz clock;

In SGMII mode, at a rate of 100Mbps, tx_clken is pulled high once every 10 cycles of the 125MHz clock, with each data bit lasting 10 cycles of the 125MHz clock;

In SGMII mode, at a rate of 1000Mbps, tx_clken remains continuously high, with each data bit lasting 1 cycle of the 125MHz clock.

2.5.4.2.2 GMII Receive Timing

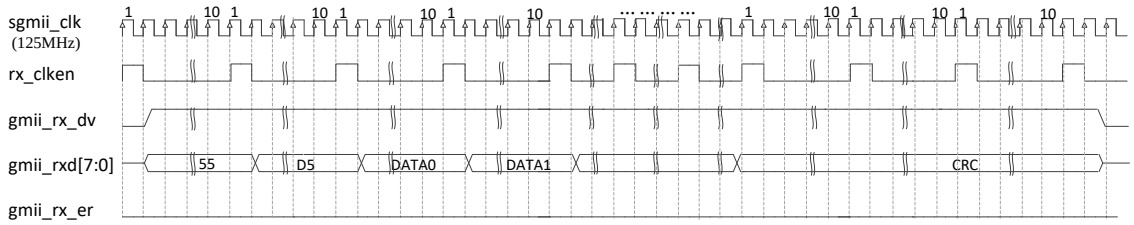

Figure 2-21 GMII Receive Timing at 100Mbps in SGMII Mode

Attention:

In SGMII mode, at a rate of 10Mbps, rx_clken is pulled high once every 100 cycles of the 125MHz clock, with each data bit lasting 100 cycles of the 125MHz clock;

In SGMII mode, at a rate of 100Mbps, rx_clken is pulled high once every 10 cycles of the 125MHz clock, with each data bit lasting 10 cycles of the 125MHz clock;

In SGMII mode, at a rate of 1000Mbps, rx_clken remains continuously high, with each data bit lasting 1 cycle of the 125MHz clock.

2.6 Description of the IP Register

The contents of the register depend on the IP configuration method[19], with different definitions for registers under various operating modes, detailed as follows. Registers can be configured through

19 Please refer to "2.3.1.2 IP Parameter Configuration".

the Configuration Management Interface MDIO or APB interface[20], and also via the Simple Fast Interface[21].

2.6.1 SGMII Core Register Descriptions

Descirption:

Rest will reset all registers to default values

The register features include "self-clearing" registers, which, after being configured via the management configuration interface, will automatically reset to zero after one clock cycle of the management configuration interface. When configuring self-clearing registers via the Fast Configuration port, the self-clear function does not operate, requiring manual cancellation of the port configuration.

The register features include "read-to-clear" registers, which immediately reset to zero after their value is read through the management configuration interface.

2.6.1.1 GE Mode

2.6.1.1.1 Auto-Negotiation Enabled

Table 2-10 Register Definitions when GE Mode Auto-Negotiation Feature is Enabled

Address	Register	Description
0	Control Register (Register 0)	Parameters for Configuring SGMII Module Functionality
1	Status Register (Register 1)	SGMII Module Status Parameters
2	PHY Identifier Register (Register 2 and 3)	PHY ID
3	PHY Identifier Register (Register 2 and 3)	PHY ID
4	Auto-Negotiation Advertisement Register (Register 4)	Local Devices Auto-Negotiation Capability
5	Auto-Negotiation Link Partner Ability Base Register (Register 5)	Remote Devices Auto-Negotiation Capability
6	Auto-Negotiation Expansion Register (Register 6)	Auto-Negotiation Expansion Register
15	Extended Status Register (Register 15)	Extended Status Register

20 Please refer to "2.6.3 Register Access".

21 Please refer to "Fast Configuration Interface" in Table 2-9.

Address	Register	Description
16	Vender_spc Register (Register 16)	Buffer Control Register
17	Vender_spc_1 Register (Register 17)	Loopback Control Register

Recommendation:

It is recommended that Register 5 is read via the MDIO or APB interface only after Auto-Negotiation is complete.

Table 2-11 Control Register (Register 0)

Bits	Item	Description	Access Type	Reset Values
0.15	Reserved	Reserved Field	Read Only	0
0.14	Loopback	Loopback Mode Enable 1: Enabled 0: Not enabled	Read /Write	0
0.13	Speed Selection(LSB)	0: Speed is 1000Mbps	Read Only	0
0.12	Auto-Negotiation Enable	Auto-negotiation enable control[22] 1: Enabled 0: Not enabled	Read /Write	1
0.11:10	Reserved	Reserved Field	Read Only	01
0.9	Restart Auto-Negotiation	Auto-Negotiation Restart Enable Control[22] 1: Restart 0: Normal operation	Read /Write/Self-cleaning	0
0.8	Duplex Mode	1: Full duplex	Read Only	1
0.7	Reserved	Reserved Field	Read Only	0
0.6	Speed Selection(MSB)	1: Speed is 1000Mbps	Read Only	1
0.5	Unidirectional Enable	Undirectional mode enable control 0: Not enabled 1: Enabled (the state of reception will not affect the operation of transmission)	Read /Write	0
0.4:0	Reserved	Reserved Field	Read Only	000000

22 When Auto-Negotiation is disabled, this register is ignored.

Table 2-12 Status Register (Register 1)

Bits	Item	Description	Access Type	Reset Values
1.15:9	Reserved	Reserved Field	Read Only	0000000
1.8	Extended Status	States Supported by Extended Status Register (Reg15)	Read Only	1
1.7	Unidirectional Ability	States Supported by Unidirectional Mode	Read Only	1
1.6	Reserved	Reserved Field	Read Only	0
1.5	Auto-Negotiation Complete	Auto-negotiation completion indication[22] 1: complete: 0: Incomplete:	Read Only	0
1.4	Remote Fault	Remote Fault reception indication 1: Received 0: Not received	Read-Only/Read-to-Clear/LH	0
1.3	Auto-Negotiation Ability	States of auto-negotiation capability supported[22]	Read Only	1
1.2	Link Status	When auto-negotiation is enabled: 1: Synchronization successful and auto-negotiation completed 0: Synchronization failed or Auto-Negotiation incomplete When auto-negotiation is disabled: 1: Synchronization successful 0: Synchronization failed	Read-Only/Read-to-Clear/LL	0
1.1:0	Reserved	Reserved Field	Read Only	00

Table 2-13 PHY Identifier Register (Register 2 and 3)

Bits	Item	Description	Access Type	Reset Values
2.15:0	Organizationally Unique Identifier	Undefined	Read /Write	0000000000000000
3.15:10			Read /Write	000000
3.9:4	Manufacturer's Model Number	Undefined	Read /Write	000000
3.3:0	Revision Number	Undefined	Read /Write	00000

Table 2-14 Auto-Negotiation Advertisement Register (Register 4)

Bits	Item	Description	Access Type	Reset Values
4.15:14	Reserved	Reserved Field	Read Only	00
4.13:12	Remote Fault	00:No Error(Link OK) 01:Offline 10:Link Failure 11:Auto-Negotiation_Error	Read /Write	00

Bits	Item	Description	Access Type	Reset Values
4.11:9	Reserved	Reserved Field	Read Only	000
4.8:7	Pause	00:No PAUSE 01:Asymmetric PAUSE toward Link Partner 10:Symmetric PAUSE 11:Both Symmetric PAUSE and Asymmetric PAUSE toward Local Device	Read /Write	11
4.6	Half Duplex	Half-Duplex Capability Indicator: 1: Supported 0: Not supported	Read Only	0
4.5	Full Duplex	Full-Duplex Capability Indicator: 1: Supported 0: Not supported	Read Only	1
4.4:0	Reserved	Reserved Field	Read Only	0

Table 2-15 Auto-Negotiation Link Partner Ability Base Register (Register 5)

Bits	Item	Description	Access Type	Reset Values
5.15	Reserved	Reserved Field	Read Only	0
5.14	Acknowledge	1: Acknowledge (remote end has received information) 0: No Acknowledge (remote end has not received information)	Read Only	0
5.13:12	Remote Fault	00:No Error(Link OK) 01:Offline 10:Link Failure 11:Auto-Negotiation_Error	Read Only	00
5.11:9	Reserved	Reserved Field	Read Only	100
5.8:7	PAUSE	00:No PAUSE 01:Asymmetric PAUSE toward Link Partner 10:Symmetric PAUSE 11:Both Symmetric PAUSE and Asymmetric PAUSE toward Local Device	Read Only	00
5.6	Half Duplex	Half-Duplex Capability Indicator: 1: Supported 0: Not supported	Read Only	0
5.5	Full Duplex	Full-Duplex Capability Indicator: 1: Supported 0: Not supported	Read Only	0
5.4:0	Reserved	Reserved Field	Read Only	00000

Table 2-16 Auto-Negotiation Expansion Register (Register 6)

Bits	Item	Description	Access Type	Reset Values
6.15:2	Reserved	Reserved Field	Read Only	0000000000 0000
6.1	Page Received	1: A new Page message received 0: No new Page message received	Read-Only/Read-to-Clear/ LH	0
6.0	Reserved	Reserved Field	Read Only	0

Table 2-17 Extended Status Register (Register 15)

Bits	Item	Description	Access Type	Reset Values
15.15	1000BASE-X Full Duplex	1000BASE-X Full Duplex (Supported)	Read Only	1
15.14	1000BASE-X Half Duplex	1000BASE-X Half Duplex (Not Supported)	Read Only	0
15.13	1000BASE-T Full Duplex	1000BASE-T Full Duplex (Not Supported)	Read Only	0
15.12	1000BASE-T Half Duplex	1000BASE-T Half Duplex (Not Supported)	Read Only	0
15.11:0	Reserved	Reserved Field	Read Only	000000000000

Table 2-18 Vender_spc Register (Register 16)

Bits	Item	Description	Access Type	Reset Values
16.15:8	Reserved	Reserved Field	Read Only	00000000
16.7:4	Min_ipg	Minimum Frame Interval Configuration[23]	Read/Write	0110
16.3:0	Reserved	Reserved Field	Read Only	0001

Attention:

In SGMII mode or Both GE And SGMII mode, with No Buffer option cleared, an offset correction Buffer is instantiated within the SGMII Core, capable of transferring the received data from the recovered data clock domain to the local clock domain; when there is an offset between the recovered data clock and the local clock, the Buffer corrects the frequency offset by deleting or inserting Idle frames.

Should frequency offset be corrected by deleting Idle frames, which reduces the number of bytes in the frame interval, this can be managed by configuring the Min_ipg register to ensure Buffer deletes Idle frames only when the byte count in the frame interval exceeds the Min_ipg configured value, and the resulting byte count after Idle deletion is still not less than the Min_ipg configured value.

23 When operating in SGMII mode or Both GE And SGMII mode, and the "No Buffer" option is cleared, the appropriate minimum frame interval must be configured according to the actual application. Please refer to "2.3.1.2 IP Parameter Configuration" for operating mode selection.

Table 2-19 Vendor-specific 1 Register (Register 17)

Bits	Item	Description	Access Type	Reset Values
17.15:12	Reserved	Reserved Field	Read Only	0000
17.11:8	mr_rstfsm_lsm_force	In HSSTLP IP loopback, corresponding loopback signals 17.8 corresponds to HSSTLP IP Lane0 17.9 corresponds to HSSTLP IP Lane1 17.10 corresponds to HSSTLP IP Lane2 17.11 corresponds to HSSTLP IP Lane3	Read/Write	0000
17.7:4	mr_rstfsm_cdr_force[24]	17.4 corresponds to HSSTLP IP Lane0 17.5 corresponds to HSSTLP IP Lane1 17.6 corresponds to HSSTLP IP Lane2 17.7 corresponds to HSSTLP IP Lane3	Read/Write	0000
17.3:0	mr_rstfsm_los_force[25]	17.0 corresponds to HSSTLP IP Lane0 17.1 corresponds to HSSTLP IP Lane1 17.2 corresponds to HSSTLP IP Lane2 17.3 corresponds to HSSTLP IP Lane3	Read/Write	1111

2.6.1.1.2 Auto-Negotiation Disabled

Auto-negotiation is disabled, indicating the "Auto Negotiation" parameter is cleared.

Table 2-20 Register Definitions when Auto-negotiation is Disabled in GE Mode

Address	Register[26]	Description
0	Control Register (Register 0)	Configure SGMII Module Functional Parameters
1	Status Register (Register 1)	SGMII Module Status Parameters
2	PHY Identifier Register (Register 2 and 3)	PHY ID
3	PHY Identifier Register (Register 2 and 3)	PHY ID
15	Extended Status Register (Register 15)	Extended Status Register
16	Vender_spc Register (Register 16)	Buffer Control Register
17	Vender_spc_1 Register (Register 17)	Loopback Control Register

24 For PCS near-end parallel loopback and PMA near-end parallel loopback, configure the corresponding Bit for the Lane in use by the current SGMII Core as 1'b1.

25 For PCS near-end parallel loopback and PMA near-end parallel loopback, configure the corresponding Bit for the Lane in use by the current SGMII Core as 1'b0.

26 The field definitions for each register are the same as those in the corresponding registers in Table 2-10.

2.6.1.2 SGMII Mode

2.6.1.2.1 Auto-Negotiation Enabled

Table 2-21 Register Definitions when Auto-negotiation Feature is Enabled in SGMII Mode

Address	Register[27]	Description
0	SGMII Control (Register 0)	Parameters for Configuring SGMII Module Functionality
1	SGMII Status Register (Register 1)	SGMII Module Status Parameters
2	PHY Identifier Register (Register 2 and 3)	PHY ID
3	PHY Identifier Register (Register 2 and 3)	PHY ID
4	SGMII Auto-Negotiation Advertisement in MAC Mode (Register 4) SGMII Auto-Negotiation Advertisement in PHY Mode (Register4)	Auto-negotiation Capability Value of Local Device
5	SGMII Auto-Negotiation Link Partner Ability Base (Register 5)	Auto-negotiation Capability Value of Remote Device
6	Auto-Negotiation Expansion Register (Register 6)	Auto-Negotiation Expansion Register
15	Extended Status Register (Register 15)	Extended Status Register
16	Vender_spc Register (Register 16)	Buffer Control Register
17	Vender_spc_1 Register (Register 17)	Loopback Control Register

Table 2-22 SGMII Control (Register 0)

Bits	Item	Description	Access Type	Reset Values
0.15	Reserved	Reserved Field	Read Only	0
0.14	Loopback	Loopback Mode Enable 1: Enabled 0: Not enabled	Read/Write	0
0.13	Speed Selection(LSB)	0.6:0.13:speed[1:0] 11: Reserved 10: 1000 Mbps 01: 100 Mbps 00: 10 Mbps	Read/Write	0
0.12	Auto-Negotiation Enable	Auto-Negotiation enable control[22] 1: Enable auto-negotiation 0: Diable auto-negotiation	Read/Write	1
0.11:10	Reserved	Reserved Field	Read Only	01
0.9	Restart Auto-Negotiation	Auto-Negotiation Restart Enable Control[22] 1: Restart 0: Normal operation	Read /Write/Self-cleaning	0

27 The field definitions for Register 2 and 3, Register 6, Register 15, Register 16, and Register 17 are identical to those in the corresponding registers in Table 2-10.

Bits	Item	Description	Access Type	Reset Values
0.8	Duplex Mode	1: Full duplex	Read Only	1
0.7	Reserved	Reserved Field	Read Only	0
0.6	Speed Selection(MSB)	0.6:0.13:speed[1:0] 11: Reserved 10: 1000 Mbps 01: 100 Mbps 00: 10 Mbps	Read/Write	1
0.5	Unidirectional Enable	Undirectional mode enable control 0: Not enabled 1: Enabled (the state of reception will not affect the operation of transmission)	Read/Write	0
0.4:0	Reserved	Reserved Field	Read Only	000000

Table 2-23 SGMII Status Register (Register 1)

Bits	Item	Description	Access Property	Reset Values
1.15:9	Reserved	Reserved Field	Read Only	0000000
1.8	Extended Status	AN Extended Status Register (Reg15) supported status	Read Only	1
1.7	Unidirectional ability	States Supported by Unidirectional Mode	Read Only	1
1.6	Reserved	Reserved Field	Read Only	0
1.5	Auto-Negotiation Complete	Auto-negotiation completion indication[22] 1: Auto-negotiation completed 0: Auto-negotiation not completed	Read Only	0
1.4	Remote Fault	SGMII MAC Side[22] 1: PHY Link Status received as 0 0: PHY Link Status received as 1 SGMII PHY Side Constantly 0	Read-Only/Read-to-Clear/LH	SGMII MAC Side: 1 SGMII PHY Side: 0
1.3	Auto-Negotiation Ability	States supported by auto-negotiation capability	Read Only	1
1.2	SGMII Link Status	When auto-negotiation is enabled: 1: SGMII synchronisation successful and auto-negotiation complete 0: SGMII synchronisation failed or auto-negotiation incomplete When auto-negotiation is disabled: 1: SGMII synchronisation successful 0: SGMII synchronisation failed	Read Only	1

Bits	Item	Description	Access Property	Reset Values
1.1:0	Reserved	Reserved Field	Read Only	00

Table 2-24 SGMII Auto-Negotiation Advertisement MAC Mode(Register 4)

Bit	Field description	Description	Property	Defaults
4.15:0	All bits	MAC Side is a fixed value	Read Only	0100000000000001

Attention:

SGMII MAC Side speed uses the speed of the remote side, with the default speed being 1000Mbps.

Table 2-25 SGMII Auto-Negotiation Advertisement in PHY Mode (Register 4)

Bits	Item	Description	Access Type	Reset Values
4.15	PHY Link Status	phy_link control 1: Connection done 0: Connection fails	Read/Write	0
4.14	Acknowledge	Local side response bit	Read Only	0
4.13	Reserved	Reserved Field	Read Only	0
4.12	Duplex Mode	phy_duplex control 1: Full duplex 0: Half duplex	Read/Write	0
4.11:10	Speed	phy_speed control 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps	Read/Write	00
4.9:1	Reserved	Reserved Field	Read Only	000000000
4.0	Reserved	Reserved Field	Read Only	1

Table 2-26 SGMII Auto-Negotiation Link Partner Ability Base (Register 5)

Bit	Field description	Description	Property	Defaults
5.15	PHY Link Status	1: Connection done 0: Connection fails	Read Only	0
5.14	Acknowledge	1: Acknowledgement (indicates the remote side has received the information) 0: No Acknowledge (remote end has not received information)	Read Only	0
5.13	Reserved	Reserved Field	Read Only	0

Bit	Field description	Description	Property	Defaults
5.12	Duplex Mode	1: Full duplex 0: Half duplex	Read Only	0
5.11:10	Speed	Remote speed 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps	Read Only	10
5.9:1	Reserved	Reserved Field	Read Only	000000000
5.0	Reserved	Reserved Field	Read Only	0

2.6.1.2.2 Auto-Negotiation Disabled

Table 2-27 Definition of Registers when SGMII Mode Auto-Negotiation is Disabled

Address	Register[28]	Description
0	SGMII Control (Register 0)	Parameters for Configuring SGMII Module Functionality
1	SGMII Status Register (Register 1)	SGMII Module Status Parameters
2	PHY Identifier Register (Register 2 and 3)	PHY ID
3	PHY Identifier Register (Register 2 and 3)	PHY ID
15	Extended Status Register (Register 15)	Extended Status Register
16	Vender_spc Register (Register 16)	Buffer Control Register
17	Vender_spc_1 Register (Register 17)	Loopback Control Register

2.6.1.3 Both GE and SGMII Mode

In this mode, SGMII 1GbE IP dynamically switches between GE and SGMII modes online using the l0_ge_or_sgmii signal.

- When the l0_ge_or_sgmii signal is 0, switch to GE mode and use GE mode register definitions;
- When the l0_ge_or_sgmii signal is 1, switch to SGMII mode and use SGMII mode register definitions.

28 The field definitions for each register are the same as those in the corresponding registers in Table 2-21.

2.6.2 HSSTLP IP Register Description

For HSSTLP IP register descriptions, please refer to "***UG040008_Logos2 Family FPGA High-Speed Serial Transceiver (HSSTLP) User Guide***" and "***UG041004_HSSTLP_IP***".

2.6.3 Register Access

SGMII 1GbE IP provides two types of register configuration management interfaces – APB interface and MDIO interface. Configure whether the MDIO interface is enabled through the "MDIO_Enable" interface option, for detailed description please refer to "2.3.1.2 IP Parameter Configuration".

2.6.3.1 MDIO Interface Disable

If the MDIO interface is not configured as enabled, SGMII 1GbE IP operates HSSTLP IP and SGMII Core registers through the APB interface.

2.6.3.1.1 HSSTLP IP Register Access

When paddr[18] is 0, operate the HSSTLP IP registers.

- paddr[17:2] is the valid address for HSSTLP IP registers;
- prdata[7:0] and pwdata[7:0] are the valid data for the HSSTLP IP registers.

2.6.3.1.2 SGMII Core Register Access

When paddr[18] is 1, operate the read and write registers of the SGMII Core.

- paddr[6:2] is the valid address for SGMII Core registers;
- prdata[15:0] and pwdata[15:0] are the valid data for the SGMII Core registers;
- paddr[20:19] is the chip select signal for the SGMII Core.

2.6.3.2 MDIO Interface Enable

If the MDIO interface is configured as enabled, SGMII 1GbE IP accesses HSSTLP IP registers via

the APB interface and SGMII Core registers via the MDIO interface.

2.6.3.2.1 HSSTLP IP Register Access

When MDIO interface is enabled, SGMII 1GbE IP operates HSSTLP IP registers via the APB interface.

- The highest bit of the address paddr[18] is invalid;
- paddr[17:2] is the valid address for HSSTLP IP registers;
- prdata[7:0] and pwdata[7:0] are the valid data for the HSSTLP IP registers.

2.6.3.2.2 SGMII Core Register Access

When MDIO interface is enabled, SGMII 1GbE IP operates SGMII Core registers via the MDIO interface.

2.7 Typical Applications

2.7.1 Single Lane Typical Applications

For typical applications of single lane in SGMII 1GbE IP, please refer to "2.4 Example Design".

2.7.2 Multi Lane Typical Applications

This section describes the Multi Lane typical applications of SGMII 1GbE IP, that is, to create a Multi Lane project with 4 lanes based on the single lane SGMII 1GbE IP by certain modifications. Users can refer to this Multi Lane scheme to modify the designs to meet actual needs.

In the Multi Lane project, similar to the single lane SGMII 1GbE IP, only one HSSTLP IP and one PLL are used. The modification process for the entire Multi Lane project is briefly introduced as follows.

- Step One: Instantiate the 4-lane HSSTLP IP;

- Step Two: Instantiate the other 3 SGMII 1GbE IPs and add the associated files of the 3 SGMII 1GbE IPs to the project;
- Step Three: Add the APB chip select module — bus_allocator to the existing project;
- Step Four: Modify the top level of the Multi Lane project;
- Step Five: Modify the clock constraints and physical location constraints to complete the changes.

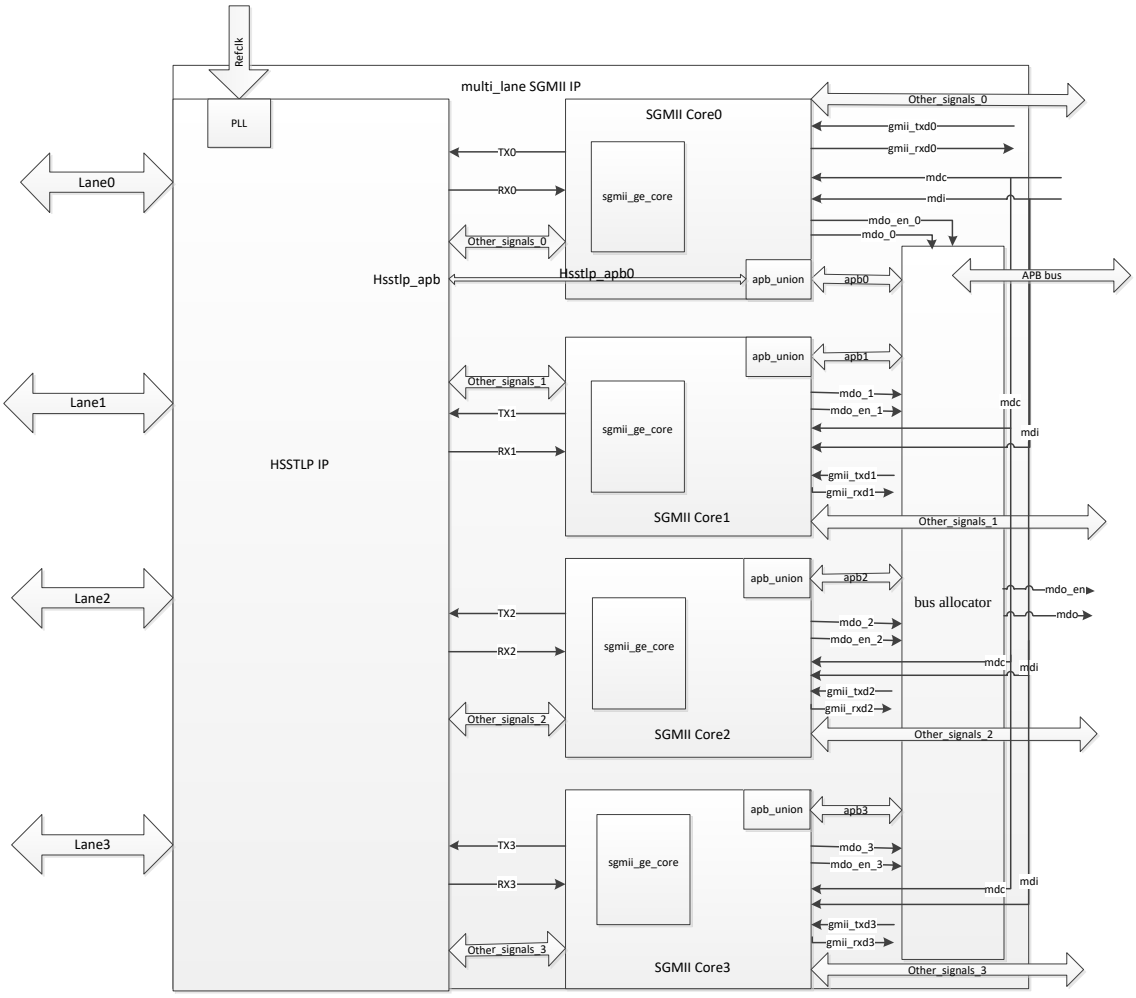

Figure 2-22 ulti_lane Design Block Diagram

The Multi Lane design block diagram is as shown in Figure 2-22. As can be seen from the figure, the four SGMII 1GbE IPs share a single HSSTLP IP. The APB interface of the HSSTLP IP is connected to the APB interface of the SGMII Core0; the APB and MDIO interfaces of the 4 SGMII 1GbE IPs are connected to the bus allocator module, which in turn is connected to the external inputs. The selected mode of the Multi Lane project and the correspondence with the 4 Serdes channels of the HSSTLP IP can be found in Table 2-28.

Table 2-28 Correspondence between Multi Lane Project and HSSTLP IP Serdes Channels

HSSTLP IP Serdes Channel Number	SGMII Core Number	SGMII 1GbE IP Configuration
Lane0	SGMII Core0	GE, AN, with Frequency Offset Buffer, MDIO.
Lane1	SGMII Core1	Both, AN, with Frequency Offset Buffer, MDIO, PHY Side.
Lane2	SGMII Core2	Both, AN, with Frequency Offset Buffer, MDIO, MAC Side.
Lane3	SGMII Core3	Both, AN, without Frequency Offset Buffer, APB, PHY Side.

2.7.2.1 Instantiation of HSSTLP IP

For the instantiation steps of the HSSTLP IP, please refer to "***UG041004_HSSTLP_IP***". Here, only the instantiation of the HSSTLP IP for SGMII Multi Lane is taken as an example, introducing the relevant parameter configurations, with the parameter configuration interface shown below.

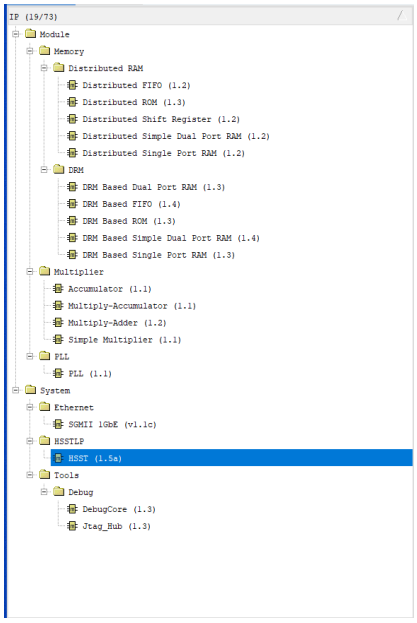

Figure 2-23 HSSTLP IP Selection Interface

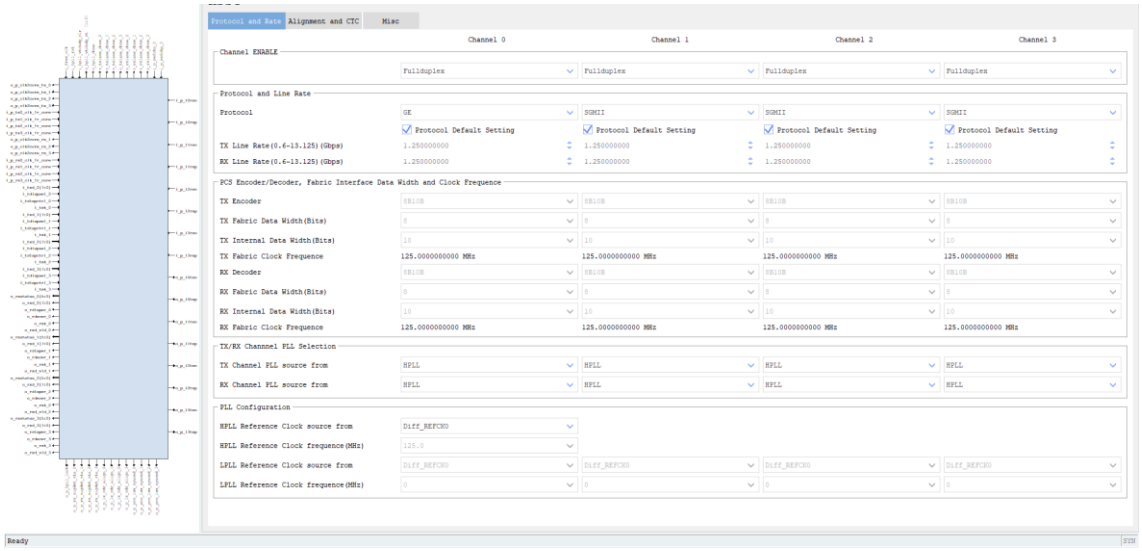

Figure 2-24 HSSTLP IP Protocol and Rate Interface

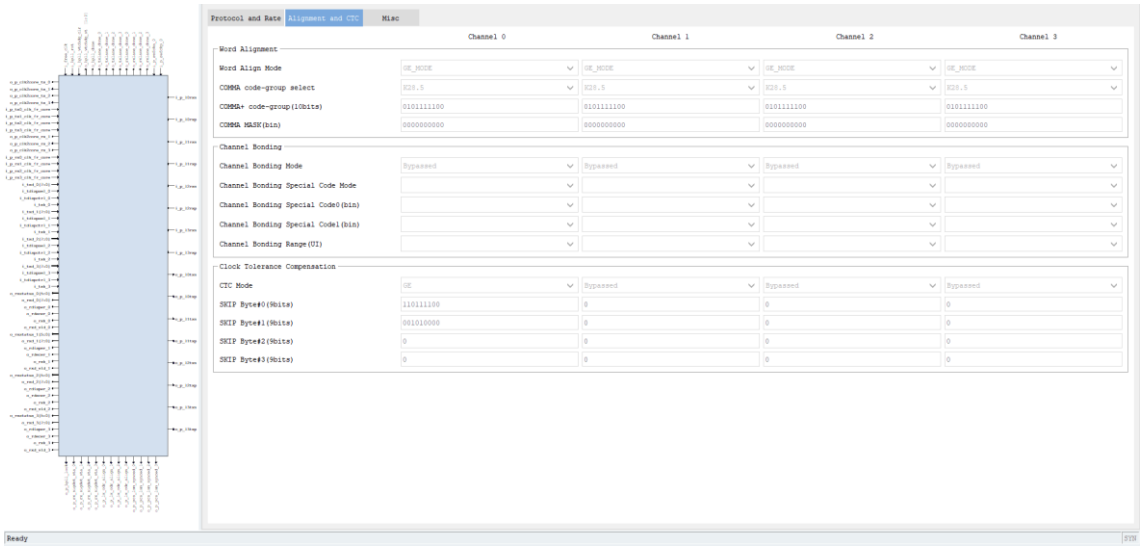

Figure 2-25 HSSTLP IP Alignment and CTC Interface

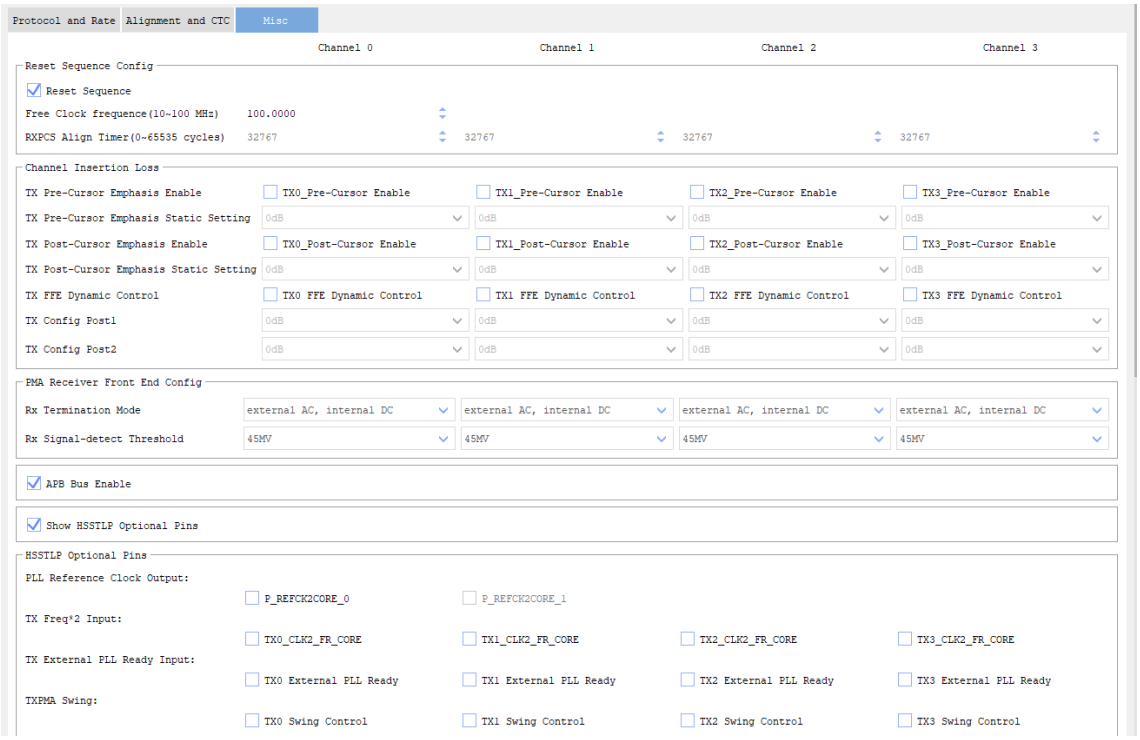

Figure 2-26 HSSTLP IP Misc part a Interface

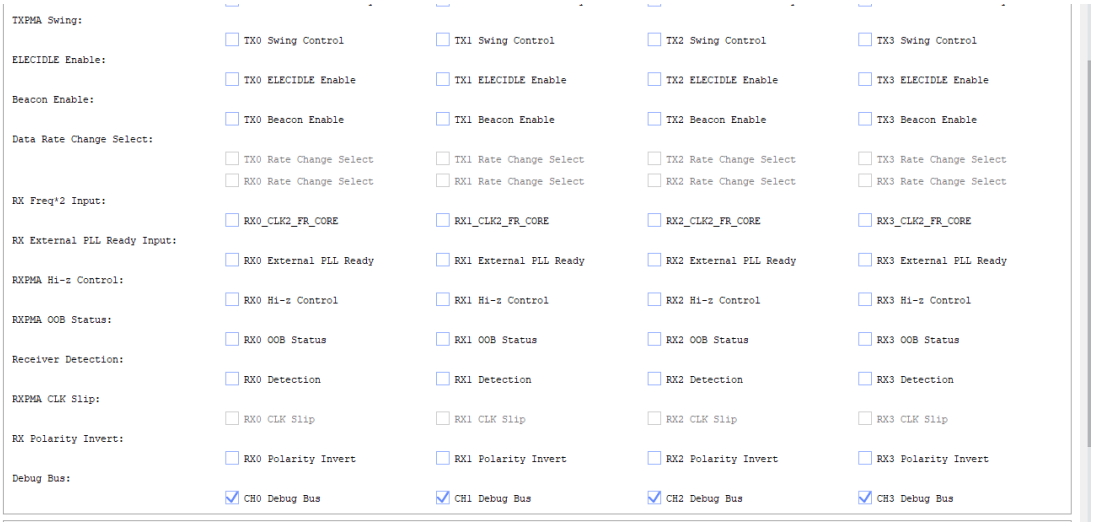

Figure 2-27 HSSTLP IP Misc part b Interface

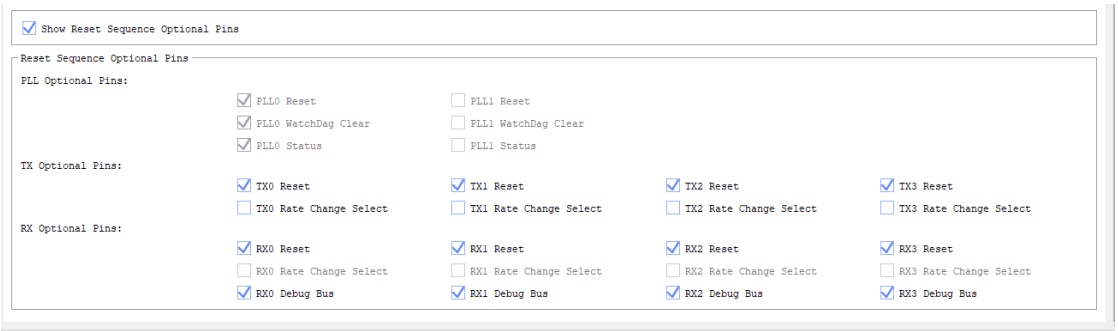

Figure 2-28 HSSTLP IP Misc part c Interface

The mode correspondence between HSSTLP IP and SGMII 1GbE IP is shown in , which customers can configure according to their own needs.

Table 2-29 Correspondence between HSSTLP IP and SGMII 1GbE IP Modes

HSSTLP IP	**SGMII 1GbE IP Mode**
GE	GE mode with enabled Frequency Offset Buffer
SGMII	All modes other than the above

2.7.2.2 Instantiation of SGMII 1GbE IP

For the instantiation steps of the SGMII 1GbE IP, please refer to "2.3.1 Module Instantiation". Instantiate and generate 3 SGMII 1GbE IPs, and add the SGMII soft core files of these 3 SGMII 1GbE IPs to the project. The files that need to be added are shown in Table 2-30.

Table 2-30 SGMII Soft Core Files

File paths	**Description**
< project_path >/rtl/*.v	The plaintext RTL files of the generated IP.
< project_path >/rtl/common/*.v	The plaintext RTL files of the generated IP, where the folder contains some common modules.
<project_path>/rtl/synplify/*.vp	The nonplaintext RTL files of the generated IP, used for synthesis. (When invoking, you may only call *_vpALL.vp or other *.vp files excluding *_vpALL.vp)

2.7.2.3 Add the bus_allocator module

The bus_allocator module is used for the input and output selection of the APB bus and the output selection of the MDIO bus. The APB bus uses reserved addr[20:19] for identifying multiple Cores. This module is instantiated at the top level of the Multi Lane project, located in the [<project_path>/example_design/rtl] directory, added using the Add Source command. The input and output signal mapping of the bus_allocator module is shown in Table 2-31, which users can configure according to their needs.

Table 2-31 bus_allocator Signal Mapping Description

bus_allocator Signal	**Multi Lane Project Top-Level Signals**
paddr	paddr
pwrite	pwrite
psel	psel
penable	penable
pwdata	pwdata
prdata	prdata
pready	pready
paddr_*	paddr_*
pwrite_*	pwrite_*
psel_*	psel_*
penable_*	penable_*
pwdata_*	pwdata_*
prdata_*	prdata_*
pready_*	pready_*
mdo_*	mdo_*
mdo_en_*	mdo_en_*
mdo	mdo
mdo_en	mdo_en

2.7.2.4 Modify the Multi Lane Project Top-Level

After the instantiation of HSSTLP IP, instantiation of SGMII 1GbE IP, and addition of the bus_allocator module, modify the Multi Lane project top-level according to the newly generated IP ports and the ports of bus_allocator to complete the invocation of HSSTLP IP, SGMII Core, and bus_allocator. During project invocation, the mapping relationships for some signals are as shown in Table 2-32.

Table 2-32 SGMII Core Signal Mapping Explanation

SGMII_Core Top-Level Signals	Multi Lane Project Top-Level Signals	Description
inst*.mdo	mdo_*	-
inst*.mdo_en	mdo_en_*	-
inst*.phy_addr	l*_phy_addr	Connect to 0 when the MDIO interface is not enabled.
inst*.mm_rst_n	l*_mm_rst_n	Leave open when the MDIO interface is not enabled.
inst*.paddr	paddr_*	-
inst*.pwrite	pwrite_*	-
inst*.psel	psel_*	-
inst*.penable	penable_*	-
inst*.pwdata	pwdata_*	-
inst*.prdata	prdata_*	-
inst*.pready	pready_*	-
inst*.status_vector	l*_status_vector	-
inst*.pin_cfg_en	l*_pin_cfg_en	-
inst*.phy_link	l*_phy_link	-
inst*.phy_duplex	l*_phy_duplex	-
inst*.phy_speed	l*_phy_speed	-
inst*.phy_remote_fault	l*_phy_remote_fault	-
inst*.phy_pause	l*_phy_pause	-
inst*.unidir_en	l*_unidir_en	-
inst*.an_restart	l*_an_restart	-
inst*.an_enable	l*_an_enable	-
inst*.loopback	l*_loopback	-
inst*.link_timer_value	l*_link_timer_value	-
inst*.tx_clken	l*_tx_clken	-
inst*.sgmii_clk	l*_sgmii_clk	-
inst*.tx_rstn_sync	l*_tx_rstn_sync	-
inst*.rx_rstn_sync	l*_rx_rstn_sync	-
inst*.gmii_rxd	l*_gmii_rxd	-
inst*.gmii_rx_dv	l*_gmii_rx_dv	-
inst*.gmii_rx_er	l*_gmii_rx_er	-
inst*.receiving	l*_receiving	-
inst*.gmii_txd	l*_gmii_txd	-
inst*.gmii_tx_en	l*_gmii_tx_en	-
inst*.gmii_tx_er	l*_gmii_tx_er	-
inst*.transmitting	l*_transmitting	-
inst*.i_txlane_done_0	o_txlane_done_*	-
inst*.i_rxlane_done_0	o_rxlane_done_*	-

SGMII_Core Top-Level Signals	Multi Lane Project Top-Level Signals	Description
inst*.i_rxk_0	o_rxk_*	-
inst*.i_rxd_0	o_rxd_*	-
inst*.i_rdisper_0	o_rdisper_*	-
inst*.i_rdecer_0	o_rdecer_*	-
inst*.i_p_pcs_lsm_synced_0	l*_lsm_synced	-
inst*.i_p_clk2core_rx_0	o_p_clk2core_rx_*	-
inst*.i_p_clk2core_tx_0	o_p_clk2core_tx_*	-
inst*.o_p_tx0_clk_fr_core	i_p_tx*_clk_fr_core	-
inst*.o_p_rx0_clk_fr_core	i_p_rx*_clk_fr_core	-
inst*.o_txk_0	i_txk_*	-
inst*.o_txd_0	i_txd_*	-
inst*.o_tdispctrl_0	i_tdispctrl_*	-
inst*.o_tdispsel_0	i_tdispsel_*	-
inst*.o_loop_dbg_0	i_loop_dbg_*	-
inst*.AN_CS	l*_AN_CS	-
inst*.AN_NS	l*_AN_NS	-
inst*.TS_CS	l*_TS_CS	-
inst*.TS_NS	l*_TS_NS	-
inst*.RS_CS	l*_RS_CS	-
inst*.RS_NS	l*_RS_NS	-
inst*.xmit	l*_xmit	-
inst*.rx_unitdata_indicate	l*_rx_unitdata_indicate	-
inst*.pcs0_rdispdec_er	pcs*_rdispdec_er	-
inst*.ge_or_sgmii	l*_ge_or_sgmii	The signal is hidden in GE mode.
inst*.mdc	mdc	Shared across 4 Lanes, set to 1 when the MDIO interface is not enabled.
inst*.mdi	mdi	Shared across 4 Lanes, set to 0 when the MDIO interface is not enabled.
inst*.cfg_rstn	cfg_rstn	Shared across 4 Lanes.
inst*.pclk	pclk	Shared across 4 Lanes.
inst0.o_p_cfg_addr	i_p_cfg_addr	Only connected to SGMII Core0, other Cores left open.
inst0.o_p_cfg_write	i_p_cfg_write	Only connected to SGMII Core0, other Cores left open.
inst0.o_p_cfg_psel	i_p_cfg_psel	Only connected to SGMII Core0, other Cores left open.
inst0.o_p_cfg_enable	i_p_cfg_enable	Only connected to SGMII Core0, other Cores left open.
inst0.o_p_cfg_wdata	i_p_cfg_wdata	Only connected to SGMII Core0, other Cores left open.
inst0.i_p_cfg_rdata	o_p_cfg_rdata	Only connected to SGMII Core0, other Cores left open.

SGMII_Core Top-Level Signals	Multi Lane Project Top-Level Signals	Description
inst0.i_p_cfg_ready	o_p_cfg_ready	Only connected to SGMII Core0, other Cores left open.
inst*.external_rstn	external_rstn	Shared across 4 Lanes.
inst*.cfg_soft_rstn	hsst_cfg_soft_rstn	Shared across 4 Lanes.
inst*.MANAGEMENT_INTERFACE	L*_MANAGEMENT_INTERFACE	Parameter, its value remains consistent with the original top-level.
inst*.AUTO_NEGOTIATION	L*_AUTO_NEGOTIATION	Parameter, its value remains consistent with the original top-level.
inst*.CLOCKING_LOGIC	L*_CLOCKING_LOGIC	Parameter, its value remains consistent with the original top-level.
inst*.CLOCKEN	L*_CLOCKEN	Parameter, its value remains consistent with the original top-level.

Note: The signal type remains consistent with the original top-level; "*" corresponds to 0, 1, 2, 3; "-" indicates none.

Table 2-33 HSSTLP IP Signal Mapping Explanation

HSSTLP IP Signals	Multi Lane Project Top-Level Signals	Description
i_free_clk	free_clk	-
i_wtchdg_clr_0	wtchdg_clr	-
i_txlane_rst_*	~txlane_sof_rst_n[*]	-
i_rxlane_rst_*	~rxlane_sof_rst_n[*]	-
i_pcs_cb_rst_*	1'b0	-
i_hsst_fifo_clr_*	1'b0	-
i_loop_dbg_*	i_loop_dbg_*	-
o_wtchdg_st_0	Float	-
o_pll_done_0	Float	-
o_txlane_done_*	o_txlane_done_*	-
o_rxlane_done_*	o_rxlane_done_*	-
i_p_refckn_0	P_REFCKN	-
i_p_refckp_0	P_REFCKP	-
o_p_clk2core_tx_*	o_p_clk2core_tx_*	-
i_p_tx*_clk_fr_core	i_p_tx*_clk_fr_core	-
o_p_clk2core_rx_*	o_p_clk2core_rx_*	-
i_p_rx*_clk_fr_core	i_p_rx*_clk_fr_core	-
o_p_pll_lock_0	l0_tx_pll_lock	-
o_p_rx_sigdet_sta_*	l*_signal_detect	-
o_p_lx_cdr_align_*	l*_cdr_align	-
o_p_pcs_lsm_synced_*	l*_lsm_synced	-
i_p_pcs_nearend_loop_*	l*_pcs_nearend_loop	-

HSSTLP IP Signals	Multi Lane Project Top-Level Signals	Description
i_p_pcs_farend_loop_*	l*_pcs_farend_loop	-
i_p_pma_nearend_ploop_*	l*_pma_nearend_ploop	-
i_p_pma_nearend_sloop_*	l*_pma_nearend_sloop	-
i_p_pma_farend_ploop_*	1'b0	-
i_p_cfg_clk	pclk	-
i_p_cfg_rst	~hsst_cfg_soft_rstn	-
i_p_cfg_psel	i_p_cfg_psel	-
i_p_cfg_enable	i_p_cfg_enable	-
i_p_cfg_write	i_p_cfg_write	-
i_p_cfg_addr	i_p_cfg_addr	-
i_p_cfg_wdata	i_p_cfg_wdata	-
o_p_cfg_rdata	o_p_cfg_rdata	-
o_p_cfg_int	Float	-
o_p_cfg_ready	o_p_cfg_ready	-
i_p_l*rxn	P_L*RXN	-
i_p_l*rxp	P_L*RXP	-
i_txd_*	i_txd_*	-
i_tdispsel_*	i_tdispsel_*	-
i_tdispctrl_*	i_tdispctrl_*	-
i_txk_*	i_txk_*	-
o_rxstatus_*	Float	-
o_rxd_*	o_rxd_*[7:0]	-
o_rdisper_*	o_rdisper_*	-
o_rdecer_*	o_rdecer_*	-
o_rxk_*	o_rxk_*	-
i_pll_rst_0	i_pll_rst_0	-

Note: The signal type remains consistent with the original top-level; "*" corresponds to 0, 1, 2, 3; "-" indicates none.

After completing the mapping of top-level signals, customers need to process some logics as per the Example Design.

Attention:

hsst_ch_ready[3:0] is composed of four o_rxlane_done_* signals.

2.7.2.5 Clock Constraints and HSSTLP Physical Location Constraints

In the generated individual SGMII Core, there are corresponding clock constraints and HSSTLP physical location constraints. Users need to consolidate the clock constraints of the 4 SGMII Cores into one. The clock constraints and HSSTLP physical location constraints generated by this Multi Lane project are shown in the Figure 2-30 and Figure 2-29, which users need to modify according to actual application conditions.

```
define_attribute {t:u_hsstlp_ch0.o_p_clk2core_tx_0} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}

define_attribute {t:u_hsstlp_ch0.o_p_clk2core_tx_1} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}
define_attribute {t:u_hsstlp_ch0.o_p_clk2core_rx_1} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}

define_attribute {t:u_hsstlp_ch0.o_p_clk2core_tx_2} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}
define_attribute {t:u_hsstlp_ch0.o_p_clk2core_rx_2} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}

define_attribute {t:u_hsstlp_ch0.o_p_clk2core_tx_3} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}
define_attribute {t:u_hsstlp_ch0.o_p_clk2core_rx_3} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}
```

Figure 2-29 Multi Lane Project Clock Constraints

```
define_attribute {i:u_hsstlp_ch0.U_GTP_HSSTLP_WRAPPER.CHANNEL0_ENABLE.U_GTP_HSSTLP_LANE0} {PAP_LOC} {HSSTLP_364_918:U0_HSSTLP_LANE}
define_attribute {i:u_hsstlp_ch0.U_GTP_HSSTLP_WRAPPER.CHANNEL1_ENABLE.U_GTP_HSSTLP_LANE1} {PAP_LOC} {HSSTLP_364_918:U1_HSSTLP_LANE}
define_attribute {i:u_hsstlp_ch0.U_GTP_HSSTLP_WRAPPER.CHANNEL2_ENABLE.U_GTP_HSSTLP_LANE2} {PAP_LOC} {HSSTLP_364_918:U2_HSSTLP_LANE}
define_attribute {i:u_hsstlp_ch0.U_GTP_HSSTLP_WRAPPER.CHANNEL3_ENABLE.U_GTP_HSSTLP_LANE3} {PAP_LOC} {HSSTLP_364_918:U3_HSSTLP_LANE}
```

Figure 2-30 Multi Lane Project Physical Constraints

2.8 Descriptions and Considerations

2.8.1 Clock Constraints

In the generated Example Design project constraint file ips2l_sgmii_top.fdc, the output clock of HSSTLP IP has been constrained to the global clock. Taking the Example Design project as an example:

```
define_attribute {t:U_ips2l_sgmii_dut.U_sgmii_inst01.u_hsstlp_ch0.o_p_clk2core_tx_0} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}
define_attribute {t:U_ips2l_sgmii_dut.U_sgmii_inst01.u_hsstlp_ch0.o_p_clk2core_rx_0} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}
```

2.8.2 HSSTLP Physical Location Constraints

In the generated Example Design project constraint file ips2l_sgmii_top.fdc, physical constraints have been applied to the HSSTLP IP's Serdes channels and reference clock input locations. Taking Example Design as an example:

```
define_attribute {i:U_ips2l_sgmii_dut.U_sgmii_inst01.u_hsstlp_ch0.U_GTP_HSSTLP_WRAPPER.CHANNEL0_ENABLE.U_GTP_HSSTLP_LANE0} {PAP_LOC} {HSSTLP_364_918:U0_HSSTLP_LANE}
define_attribute {i:U_ips2l_sgmii_dut.U_sgmii_inst01.u_hsstlp_ch0.U_GTP_HSSTLP_WRAPPER.PLL0_ENABLE.U_GTP_HSSTLP_PLL0} {PAP_LOC} {HSSTLP_364_918:U0_HSSTLP_PLL}
```

Wherein:

- HSSTLP_364_918:U0_HSSTLP_LANE indicates that the Serdes channels will use the Q3_Lane0 of the chip for data communication.
- HSSTLP_364_918:U0_HSSTLP_PLL indicates that the input differential clock will use the Q3_PLL0 of the chip for locking.

Users can modify the constraints according to the actual situation of the single board by referring to "***UG041004_HSSTLP_IP***". to meet practical usage requirements.

2.8.3 Operating Modes

2.8.3.1 GE Mode

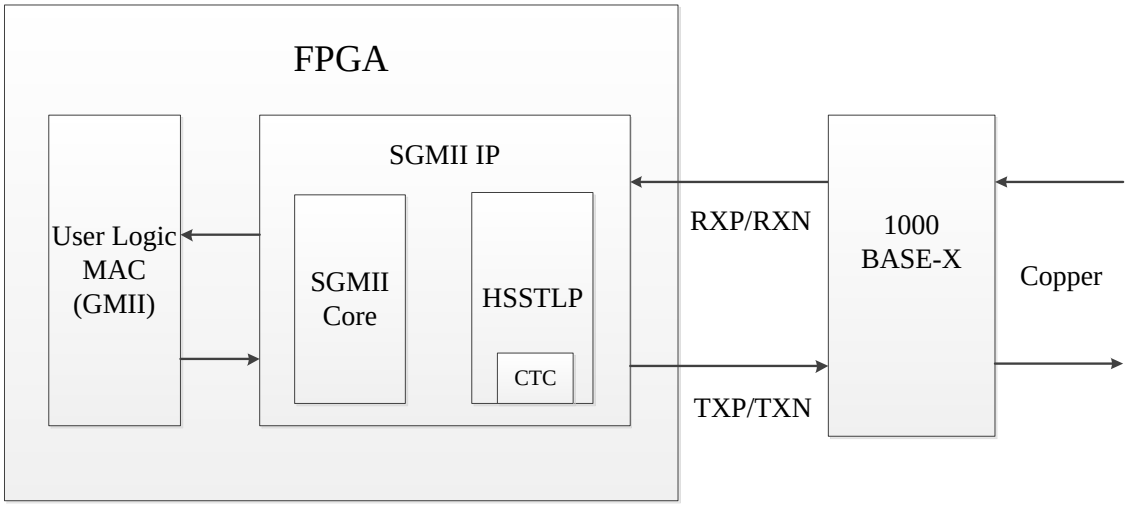

Figure 2-31 GE mode schematic

2.8.3.2 SGMII Mode

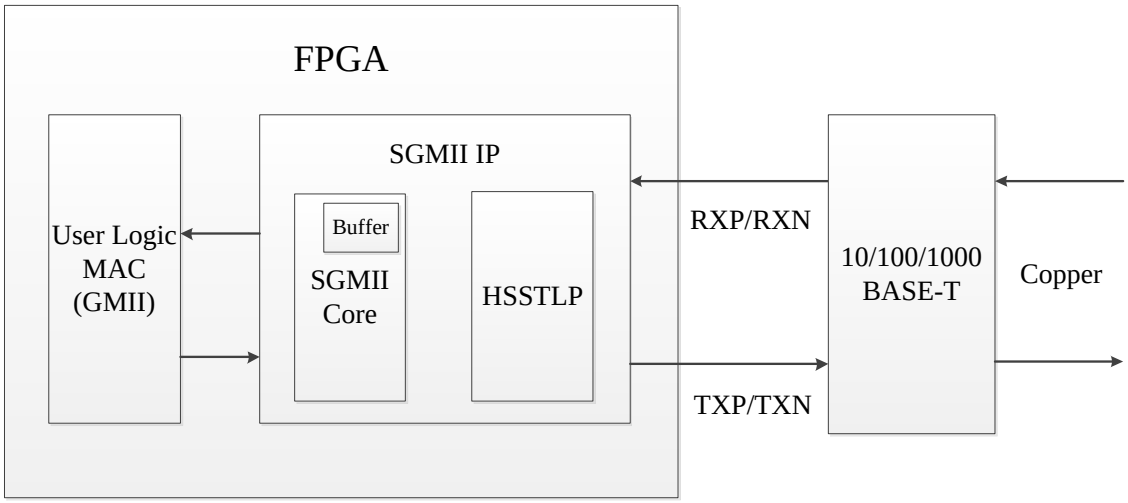

Figure 2-32 SGMII mode schematic

2.8.3.3 Both GE and SGMII Mode

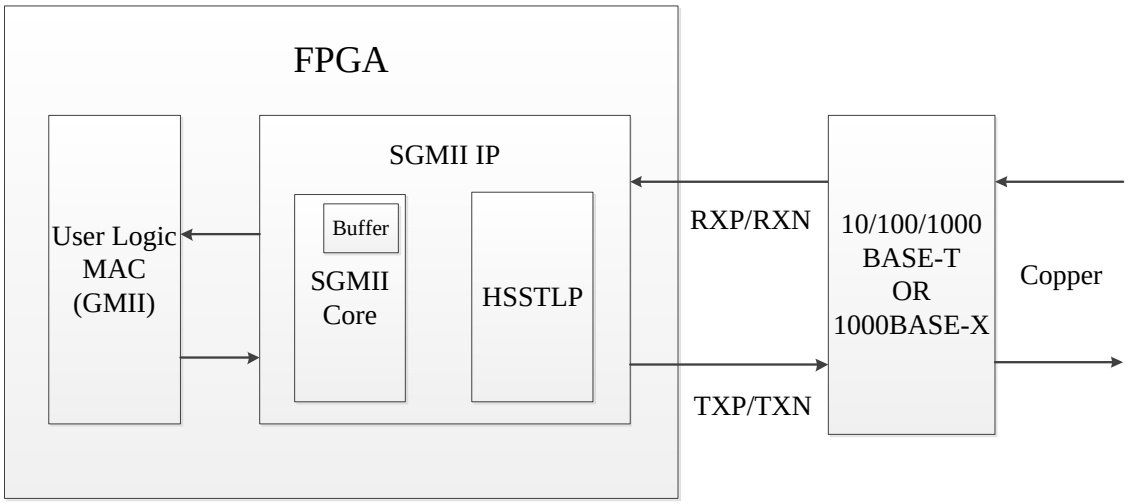

Figure 2-33 Both GE And SGMII mode schematic

2.8.4 Loopback Mod

The SGMII 1GbE IP supports five types of loopback modes, as shown in Figure 2-1:

- SGMII Core Loopback
- PMA Near-End Parallel Loopback[29]
- PMA near-end serial loopback[29]
- PCS near-end parallel loopback[29]
- PCS far-end parallel loopback[29]

2.8.4.1 SGMII Core Loopback

This loopback mode supports two types of configuration: port configuration and register configuration.

Table 2-34 SGMII Core Loopback Port Configuration

Configuration Item	Configuration Descriptions
Port enable	l0_pin_cfg_en=1, to enable port configuration.
Loopback configuration	l0_loopback=1.
Non-Loopback configuration	l0_loopback=0.

Table 2-35 SGMII Core Loopback Register Configuration

Configuration Item	Configuration Descriptions
Register enable	l0_pin_cfg_en=0, to enable register configuration.
Loopback configuration	reg0.14 Loopback == 1'b1.
Non-Loopback configuration	reg0.14 Loopback == 1'b0.

29 For detailed introduction about loopback, please refer to:

"***UG040008_Logos2 Family FPGA High-Speed Serial Transceiver (HSSTLP) User Guide***" and "***UG041004_ HSSTLP_IP***".

Attention:

SGMII Core Loopback is not available when the "No Buffer" option is selected.

2.8.4.2 PMA Near-End Parallel Loopback

Attention:

PMA near-end parallel loopback mode requires the corresponding register values to be set correctly before enabling the loopback port.

Table 2-36 PMA Near-End Parallel Loopback

Configuration Item	Configuration Descriptions
Register Configuration	reg17.0 mr_rstfsm_los_force == 1'b0; reg17.4 mr_rstfsm_cdr_force == 1'b1. Following the above configuration, the SGMII register reg17 Vendor_spc_1 is set to 0x0010.
Port Configuration	When pma_nearend_ploop=1, PMA near-end parallel loopback is enabled.

2.8.4.3 PMA Near-End Serial Loopback

Attention:

PMA near-end serial loopback mode requires the corresponding register values to be set correctly before enabling the loopback port.

Table 2-37 PMA Near-End Serial Loopback

Configuration Item	Configuration Descriptions
Register Configuration	reg17.0 mr_rstfsm_los_force == 1'b1. Following the above configuration, the SGMII register reg17 Vendor_spc_1 is set to 0x0001.
Port Configuration	When pma_nearend_sloop=1, PMA near-end serial loopback is enabled.

2.8.4.4 PCS near-end parallel loopback

Attention:

PCS near-end parallel loopback mode requires the corresponding register values to be set correctly before enabling the loopback port.

Table 2-38 PCS Near-End Parallel Loopback

Configuration Item	Configuration Descriptions
Register Configuration	reg17.0 mr_rstfsm_los_force == 1'b0; reg17.4 mr_rstfsm_cdr_force == 1'b1. Following the completion of the above configuration, the SGMII register reg17 Vendor_spc_1 is set to 0x0010.
Port Configuration	When pcs_nearend_loop=1, PCS near-end parallel loopback is enabled.

2.8.4.5 PCS far-end parallel loopback

Attention:

PCS far-end loopback mode first requires ensuring the corresponding register values are set correctly, then enabling the loopback port.

Table 2-39 PCS Far-End Parallel Loopback

Configuration Item	Configuration Descriptions
Register Configuration	reg17.0 mr_rstfsm_los_force == 1'b1. Following the above configuration, the SGMII register reg17 Vendor_spc_1 is set to 0x0001. Configure HSSTLP IP registers: Offset 0x824.2 PMA_REG_PLPBK_TXPCLK_EN ==1 Offset 0x00c.4:3PCS_RX_CLK_SEL ==2'b01 After configuration, the HSSTLP IP register 0x824 is set to 0x4 After configuration, the HSSTLP IP register 0x00c is set to 0x8
Port Configuration	When pcs_farend_loop=1, PCS far-end parallel loopback is enabled.

Attention:

Under this loopback mode, if the value of HSSTLP IP register 0x824 is not configured to 0x4, the clocks at both ends of the link must share the same source.

2.8.5 IP Clock Scheme

2.8.5.1 Frequency Offset Adjustment Buffer located within the HSSTLP IP

In GE mode, when the Frequency Offset Buffer is enabled (i.e., the "No Buffer" option is not chosen), this clock scheme is applicable.

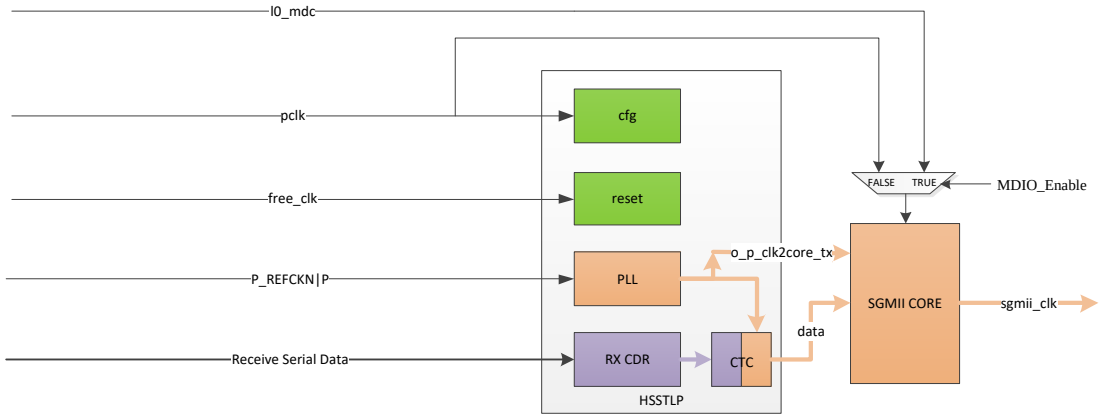

Figure 2-34 Schematic of Clock Scheme with Frequency Offset Adjustment Buffer in HSSTLP IP

2.8.5.1.1 Data Path Clock

- In the transmit direction, a pair of 125MHz differential input clocks provide the clock source for the HSSTLP IP which, after passing through PLL in the HSSTLP IP, provides the SGMII Core with the transmit clock o_p_clk2core_tx. Ultimately serves as the clock sgmii_clk for the GMII side.
- In the receive direction, the RX_CDR in the HSSTLP IP recovers the clock from serial differential data, and in the CTC within the HSSTLP IP, it unifies the clock domain to o_p_clk2core_tx.

2.8.5.1.2 Free Run Clock

- free_clk is a clock independent of the data path clock, providing a clock for the HSSTLP IP reset sequence, with a frequency range of 10MHz to 100MHz in this scheme.

2.8.5.1.3 Configuration clock

- l0_mdc—MDIO interface clock, 2.5MHz. When "MDIO_Enable" is selected, it provides the clock for the SGMII Core configuration logic.
- pclk—APB interface clock, 50MHz~100MHz. When "MDIO_Enable" is selected, it provides the clock for HSSTLP IP configuration logic; when "MDIO_Enable" is cleared, it provides the clock for both HSSTLP IP and SGMII Core configuration logics.

2.8.5.2 Frequency Offset Adjustment Buffer located within the SGMII Core

Under SGMII mode or Both GE And SGMII modes, when the Frequency Offset Buffer is enabled (i.e., the "No Buffer" option is not chosen), this clock scheme is applicable.

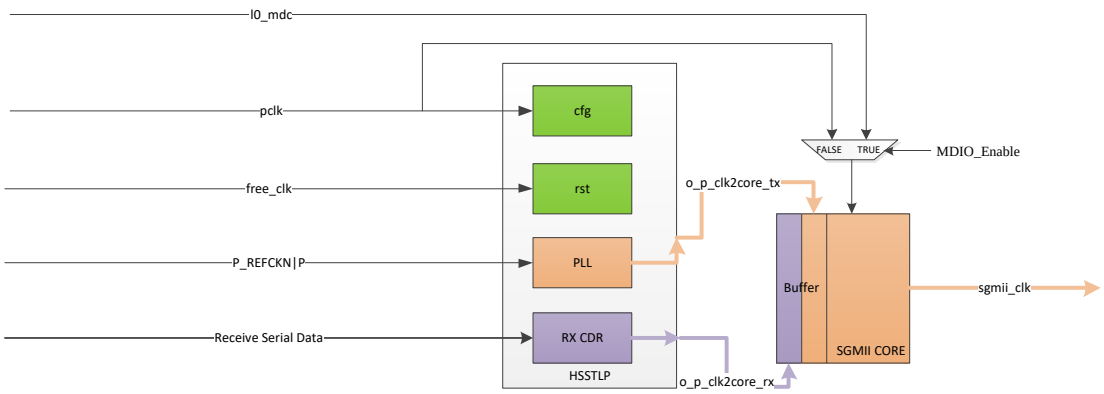

Figure 2-35 Schematic of Clock Scheme with Frequency Offset Adjustment Buffer in SGMII Core

2.8.5.2.1 Data Path Clock

- In the transmit direction, a pair of 125MHz differential input clocks provide the clock source for the HSSTLP IP which, after passing through PLL in the HSSTLP IP, provides the SGMII Core with the transmit clock o_p_clk2core_tx.

- In the receive direction, the RX_CDR in the HSSTLP IP recovers the clock from serial differential data, providing the SGMII Core with the receive clock o_p_clk2core_rx.
- Through the Elastic Buffer in the SGMII Core, the clock domain is unified to o_p_clk2core_tx, eventually generating the clock sgmii_clk for the GMII side.

2.8.5.2.2 Free Run Clock

- free_clk is a clock independent of the data path clock, providing a clock for the HSSTLP IP reset sequence, with a frequency range of 10MHz to 100MHz in this scheme.

2.8.5.2.3 Configuration clock

- l0_mdc—MDIO interface clock, 2.5MHz. When "MDIO_Enable" is selected, it provides the clock for the SGMII Core configuration logic.
- pclk—APB interface clock, 50MHz~100MHz. When the "MDIO_Enable" option is selected, it provides a clock for the HSSTLP IP configuration logic; when the "MDIO_Enable" option is cleared, it provides a clock for both HSSTLP IP configuration logic and SGMII Core configuration logic.

2.8.5.3 Without Frequency Offset Adjustment Buffer

In GE mode, SGMII mode, or Both GE And SGMII modes, when the Frequency Offset Buffer is not enabled (i.e., the "No Buffer" option is chosen), this clock scheme is applicable.

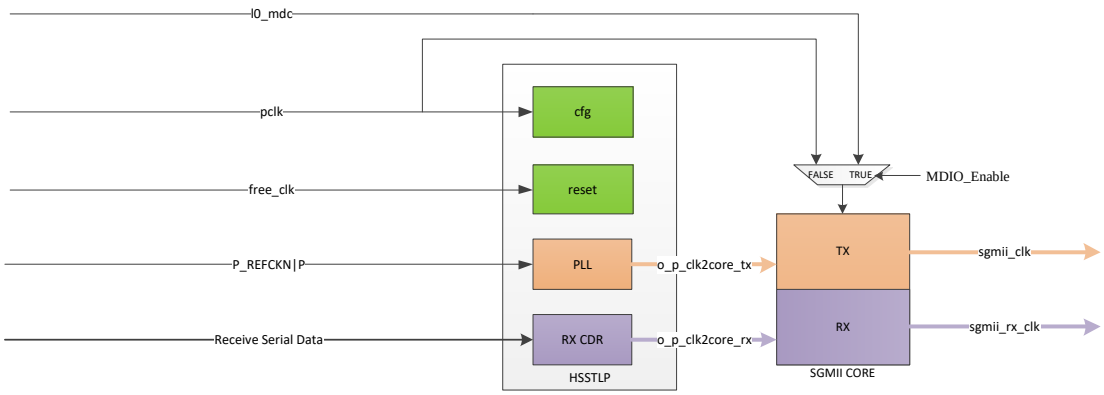

Figure 2-36 Schematic of Clock Scheme without Frequency Offset Adjustment Buffer

2.8.5.3.1 Data Path Clock

- In the transmit direction, a pair of 125MHz differential input clocks provide the clock source for the HSSTLP IP which, after passing through PLL in the HSSTLP IP, provides the SGMII Core with the transmit clock o_p_clk2core_tx, ultimately generating the transmit direction clock sgmii_clk for the GMII side.
- In the RX direction, the RX_CDR in HSSTLP IP recovers the clock from the serial differential data, providing the capture clock o_p_clk2core_rx for SGMII Core, and ultimately generating the clock sgmii_rx_clk for the GMII receive side.

2.8.5.3.2 Free Run Clock

- free_clk is a clock independent of the data path clock, providing a clock for the HSSTLP IP reset sequence, with a frequency range of 10MHz to 100MHz in this scheme.

2.8.5.3.3 Configuration clock

- l0_mdc—MDIO interface clock, 2.5MHz. Selecting the "MDIO_Enable" parameter provides a clock for the SGMII Core configuration logic.
- pclk—APB interface clock, 50MHz~100MHz. When the "MDIO_Enable" option is selected, it provides a clock for the HSSTLP IP configuration logic; when the "MDIO_Enable" option is cleared, it provides a clock for both HSSTLP IP configuration logic and SGMII Core configuration logic.

2.8.6 Example of read and write operations for the uart_ctrl_top module

2.8.6.1 Read Operation

Reading data from address 0x000001: 0x72+0x000001, which is 0x72000001.

2.8.6.2 Write Operation

Writing 0x02 to address 0x000001: 0x77+0x000001+0x00000002, which is 0x7700000100000002.

2.8.7 IP Invocation Method

The SGMII 1GbE IP supports invocation by adding an idf file. For the specific method of adding an idf file, please refer to the relevant help documentation in the PDS installation path: "***Pango_Design_Suite_User_Guide***".

2.9 IP Debugging Method

In the Example Design, DebugCore and LED can monitor the link status of the SGMII 1GbE IP; for the DebugCore signal list and LED indicator signal list, please refer to "2.4.4 Test Method", "2.4.3 Descriptions of Ports".

In the Example Design, the UART can read the values of the status registers in the IP to monitor the link status. For the use of the UART module, please refer to "2.4.2.1 uart_ctrl_top".

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