Logos Family SDRAM User Guide

(V1.0)

(02.12.2019)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.0	02.12.2019	Initial release;

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
SDRAM	Synchronous Dynamic Random Access Memory

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Chapter 1 Overall Introduction

Logos Family FPGAs products provide SDRAM resources, with a size of 512K * 32bit * 4 banks, supporting up to 200MHz frequency.

Below are some parameters of the SDRAM:

- Row address: 11bit; column address: 8bit
- Maximum data width: 32bit
- 4-Banks
- CAS Latency of 2 and 3
- Burst length: 1, 2, 3, 8 and full page
- The input is sampled on the rising edge of the clock
- DQM masking supported
- Auto or manual refresh supported

For detailed information, please refer to "M12L64322A(2S)".

Chapter 2 Pin Mapping

The pin correspondence of the SDRAM in the constraint file is shown in Table 2-1 and Figure 2-1, Figure 2-2.

Table 2-1 SDRAM Pin Correspondence List of Constraints

SDRAM Pin Name	**Corresponding Pin Name in Constraint File**
SDRAM_CLK	CLK
SDRAM_CS	CS
SDRAM_CKE	CKE
SDRAM_ADDR0~10	A0~10
SDRAM_BA0~1	BA0~1
SDRAM_RAS	RAS
SDRAM_CAS	CAS
SDRAM_WE	WE
SDRAM_DQM0~3	DQM0~3
SDRAM_DQ0~31	DQ0~31

sdram_dq[31]	Inout	DQ31	BANKR1
sdram_dq[30]	Inout	DQ30	BANKR1
sdram_dq[29]	Inout	DQ29	BANKR1
sdram_dq[28]	Inout	DQ28	BANKR1
sdram_dq[27]	Inout	DQ27	BANKR1
sdram_dq[26]	Inout	DQ26	BANKR1
sdram_dq[25]	Inout	DQ25	BANKR1
sdram_dq[24]	Inout	DQ24	BANKR1
sdram_dq[23]	Inout	DQ23	BANKL1
sdram_dq[22]	Inout	DQ22	BANKL1
sdram_dq[21]	Inout	DQ21	BANKL1
sdram_dq[20]	Inout	DQ20	BANKL1
sdram_dq[19]	Inout	DQ19	BANKL1
sdram_dq[18]	Inout	DQ18	BANKL1
sdram_dq[17]	Inout	DQ17	BANKL1
sdram_dq[16]	Inout	DQ16	BANKL1
sdram_dq[15]	Inout	DQ15	BANKR1
sdram_dq[14]	Inout	DQ14	BANKR1
sdram_dq[13]	Inout	DQ13	BANKR1
sdram_dq[12]	Inout	DQ12	BANKR1
sdram_dq[11]	Inout	DQ11	BANKR1
sdram_dq[10]	Inout	DQ10	BANKR1
sdram_dq[9]	Inout	DQ9	BANKR1
sdram_dq[8]	Inout	DQ8	BANKR1

Figure 2-1 SDRAM Pins Constraints in PDS

sdram_dq[7]	Inout	DQ7	BANKL1
sdram_dq[6]	Inout	DQ6	BANKL1
sdram_dq[5]	Inout	DQ5	BANKL1
sdram_dq[4]	Inout	DQ4	BANKL1
sdram_dq[3]	Inout	DQ3	BANKL1
sdram_dq[2]	Inout	DQ2	BANKL1
sdram_dq[1]	Inout	DQ1	BANKL1
sdram_dq[0]	Inout	DQ0	BANKL1
sdram_addr[1…	Output	A10	BANKR1
sdram_addr[9]	Output	A9	BANKL1
sdram_addr[8]	Output	A8	BANKL1
sdram_addr[7]	Output	A7	BANKL1
sdram_addr[6]	Output	A6	BANKL1
sdram_addr[5]	Output	A5	BANKL1
sdram_addr[4]	Output	A4	BANKL1
sdram_addr[3]	Output	A3	BANKR1
sdram_addr[2]	Output	A2	BANKR1
sdram_addr[1]	Output	A1	BANKR1
sdram_addr[0]	Output	A0	BANKR1
sdram_bank[1]	Output	BA1	BANKR1
sdram_bank[0]	Output	BA0	BANKR1
sdram_dqm[3]	Output	DQM3	BANKR1
sdram_dqm[2]	Output	DQM2	BANKL1
sdram_dqm[1]	Output	DQM1	BANKR1
sdram_dqm[0]	Output	DQM0	BANKL1
check_err	Output	4	BANKR0
clk_out_indi…	Output	100	BANKL2
sdram_cas_n	Output	CAS	BANKL1
sdram_cke	Output	CKE	BANKL1
sdram_clk	Output	CLK	BANKR1
sdram_cs_n	Output	CS	BANKL1
sdram_ras_n	Output	RAS	BANKL1
sdram_we_n	Output	WE	BANKL1

Figure 2-2 SDRAM Pins Constraints in PDS

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