Compa Family CPLDs Device Support Input of 1.0V Application Guide

(AN03019, V1.0)

(02.03.2022)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.0	02.03.2022	Initial release.

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Figures

Chapter 1 Overview

The I/Os in Compa device support the input of 1.0V level signals. This document describes how to configure I/O attribute using PDS software.

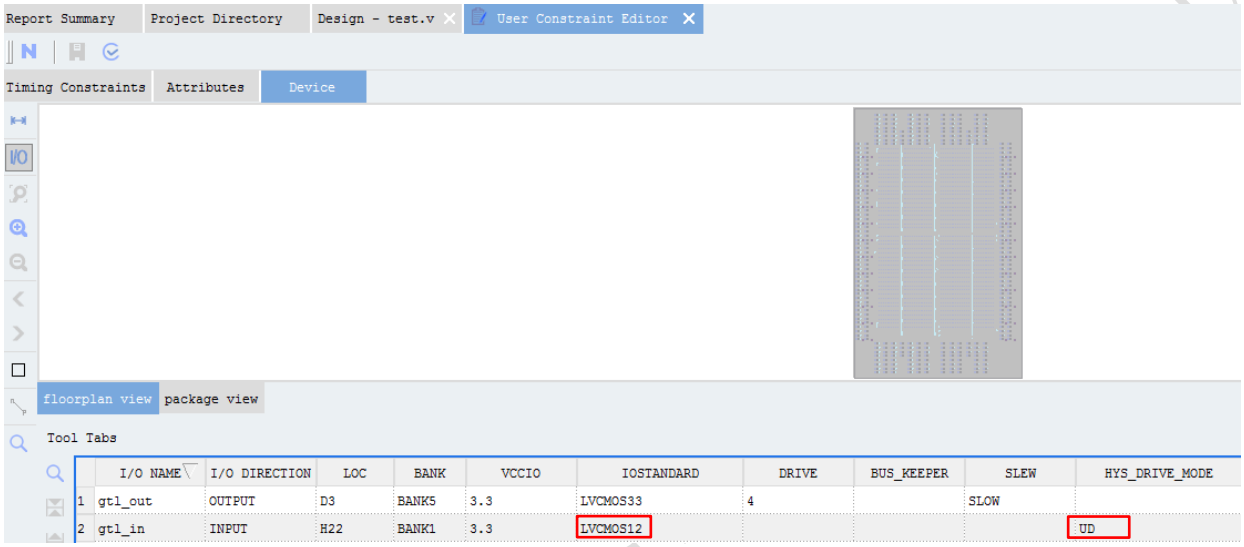
Chapter 2 Features

- When VCCIO of input bank is 1.5V, 1.8V, 2.5V, or 3.3V, and the input signal is 1.0V, the input should be set to "UD"
- Every I/O which is used as an input in each bank supports "UD"
- All Compa devices support this application

Chapter 3 Software Configuration

Software: supported in all versions.

Open PDS software and click on [User Constraint Editor] to do physical constraints on the input I/O. This is shown in the following figure.



	I/O NAME	I/O DIRECTION	LOC	BANK	VCCIO	IOSTANDARD	DRIVE	BUS_KEEPER	SLEW	HYS_DRIVE_MODE
1	gtl_out	OUTPUT	D3	BANK5	3.3	LVCMOS33	4		SLOW	
2	gtl_in	INPUT	H22	BANK1	3.3	LVCMOS12				UD

Figure 3-1 Software Configuration

- For the output "gtl_out" that needs to output an 1.0V signal, users should set "OPEN_DRAIN" to "ON" and add an external pull-up resistor to the pin to pull it up to 1.0V, as shown in the circuit diagram below:

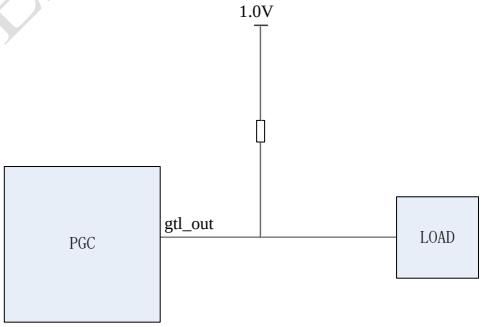


Figure 3-2 Open-drain Output Circuit Diagram

"IOSTANDARD" should be set to the LVCMOS standard, and other properties remain the default values.

- For the input "gtl_in", "VCCIO" can be configured as 1.5, 1.8, 2.5, or 3.3, "IOSTANDARD" is set to "LVCMOS12", and "HYS_DRIVE_MODE" is set to "UD".

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