QSGMII IP

User Guide

(UG042007, V1.4)

(30.04.2024)

Shenzhen Pango Microsystems Co., Ltd.

Revisions History

Document Revisions

Version	Date of Release	Revisions	Applicable IP and Corresponding Versions
V1.4	30.04.2024	Initial release.	V1.4

IP Revisions

IP Version	Date of Release	Revisions
V1.4	30.04.2024	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
APB	Advanced Peripheral Bus
PCS	Physical Code Sublayer
PHY	Physical
PMA	Physical Media Attachment
QSGMII	Quad Serial Gigabit Media Independent Interface
SerDes	Serializer Deserializer
SGMII	Serial Gigabit Media Independent Interface
IPC	IP Compiler
PDS	Pango Design Suite

Related Documentation

The following documentation is related to this manual:

1. ***Pango_Design_Suite_Quick_Start_Tutorial***
2. ***Pango_Design_Suite_User_Guide***
3. ***IP_Compiler_User_Guide***
4. ***Simulation_User_Guide***
5. ***User_Constraint_Editor_User_Guide***
6. ***Physical_Constraint_Editor_User_Guide***
7. ***Route_Constraint_Editor_User_Guide***
8. ***IEEE802.3-2012 Specification***
9. ***Cisco Systems, Serial-GMII Specification-rev1.8***
10. ***Cisco Systems, QSGMII Specification-rev1.2***
11. ***Fabric_Debugger_User_Guide***
12. ***UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide***
13. ***UG041004 _HSSTLP_IP***

Table of Contents

Tables

Figures

Chapter 1 Preface

This chapter describes the scope, structure, and writing standards of this manual to help users quickly find the information they need.

1.1 Introduction of the Manual

This manual serves as a user guide for the QSGMII IP launched by Pango Microsystems, primarily including the IP user guide and related information. This manual helps users quickly understand the QSGMII IP features and usage.

1.2 Writing Standards of the Manual

Table 1-1 Description of Writing Standards

Text	**Rules**
Attention	If users ignore the attention contents, they may suffer adverse consequences or fail to operate successfully due to incorrect actions.
Description	Instructions and tips provided for users.
Recommendation	Recommended settings and instructions for users.

Chapter 2 IP User Guide

This chapter provides a guide on the use of QSGMII IP, including an introduction to IP, block diagram, IP generation process, Example Design, IP interface description, IP register description, typical applications, instructions and considerations, and IP debugging methods. More details on the design process can be found in the following PDS help documentation.

- "***Pango_Design_Suite_Quick_Start_Tutorial***"
- "***Pango_Design_Suite_User_Guide***"
- "***IP_Compiler_User_Guide***"
- "***Simulation_User_Guide***"

2.1 IP Introduction

The QSGMII IP is an Ethernet interface IP launched by Pango Microsystems, connecting the data link layer and physical layer to enable the efficient transmission of 4 Ethernet data streams (10/100/1000Mbps) over a single SerDes channel. Users can configure and generate the IP module using the IPC (IP Compiler) tool within the PDS (Pango Design Suite).

2.1.1 Key Features

The QSGMII IP is designed according to the "***IEEE802.3-2012 Specification***", "***Cisco Systems, Serial-GMII Specification-rev1.8***", "***Cisco Systems, and QSGMII Specification-rev1.2***" standards, with the following main features.

- Supports GMII data interface;
- Supports APB or MDIO for configuration management interface;
- Supports simple and fast configuration through ports;
- Supports clock frequency deviation correction to adapt to the ±100ppm frequency difference of Ethernet;
- Supports 4 SGMII Cores transmitting at different rates;
- Supports reset operation for a single SGMII Core;
- Supports auto-negotiation function;
- Supports loopback function.

2.1.2 Applicable Devices and Packages

Table 2-1 QSGMII IP Applicable Devices and Packages

Applicable Devices	**Supported Packages**
PG2L100H	ALL (except for MBG324)
PG2L50H	ALL (except for FBG256/MBG324)
PG2L25H	ALL
PG2L200H	ALL
PG2L100HX	ALL (except for MBG324)

2.2 IP Block Diagram

The QSGMII IP consists of HSSTLP and QSGMII Core, as shown in the system block diagram Figure 2-1. The dotted lines show the data stream during loopback. For loopback configuration methods, please refer to "2.8.4 Loopback Mode".

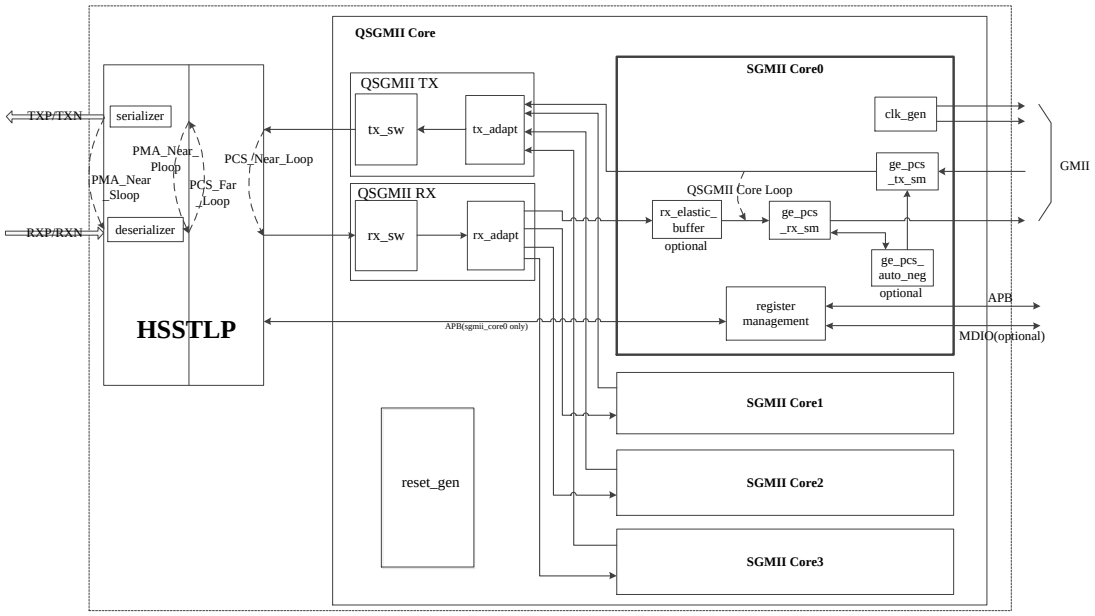

Figure 2-1 QSGMII IP System Block Diagram

2.2.1 HSSTLP

HSSTLP is instantiated from the HSSTLP, including HSSTLP_PLL, HSSTLP_APB_Bridge and HSSTLP IP hard core resources. It mainly implements PCS encoding/decoding, PMA serial/parallel conversion, and clock recovery functions. The HSSTLP IP registers can only be accessed through the APB interface of SGMII Core0, as shown in Figure 2-1.

2.2.2 QSGMII Core

The QSGMII Core is the soft core logic of the QSGMII IP, including QSGMII TX, QSGMII RX, reset_gen, and 4 SGMII Cores[1]. It mainly implements auto-negotiation, frequency offset handling, data transmission, data reception, and register management functions. Each SGMII Core has its own set of registers that can be accessed through the APB or MDIO interfaces. For detailed information, please refer to "2.6 Description of the IP Register".

1 corresponds to SGMII Core0, SGMII Core1, SGMII Core2, SGMII Core3 in Figure 2-1.

2.3 IP Generation Process

2.3.1 Module Instantiation

Customized configurations of QSGMII IP can be completed through the IPC tool, instantiating the required IP modules. For detailed instructions on using the IPC tool, please refer to "***IP_Compiler_User_Guide***".

The main steps for instantiating the QSGMII IP module are described below.

2.3.1.1 Selecting IP

Open IPC and click File > Update in the main window to open the Update IP dialog box, where you add the corresponding version of the IP model.

After selecting the FPGAs device type, the Catalog interface displays the loaded IP models. Select the corresponding version of QSGMII under the "System/Ethernet" directory. The IP selection path is shown in Figure 2-2. Then set the Pathname and Instance Name on the right side of the page. The project instantiation interface is shown in Figure 2-3.

Attention:

Be sure to use the software of version 2022.2 or above.

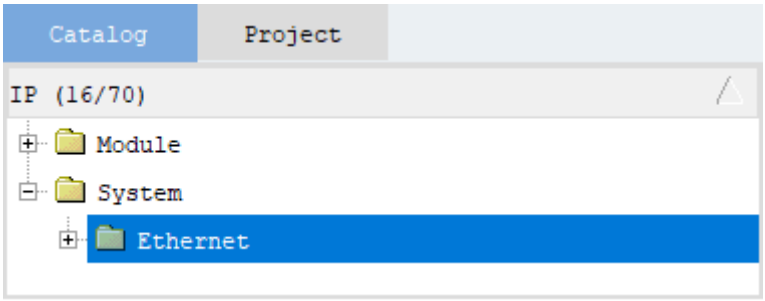

Figure 2-2 QSGMII IP Selection Path Interface

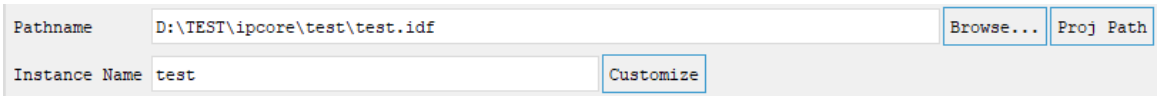

Figure 2-3 Project Instantiation Interface

2.3.1.2 IP Parameter Configuration

After selecting the IP, click <Customize> to enter the QSGMII IP parameter configuration interface. The left Symbol is the interface block diagram, as shown in Figure 2-4; the Parameter Configuration window is shown on the right side, as shown in Figure 2-5.

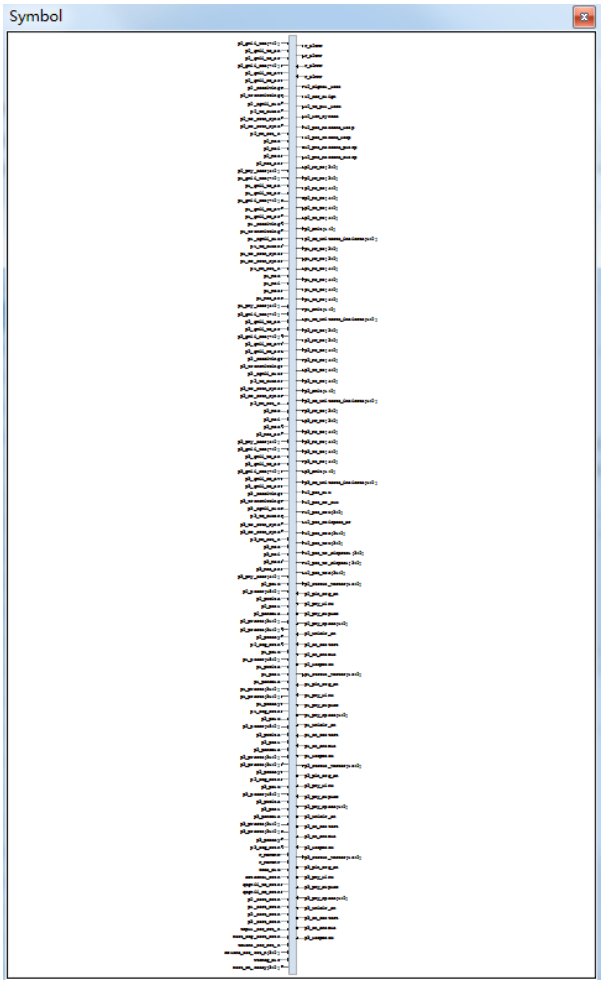

Figure 2-4 QSGMII IP Interface Block Diagram

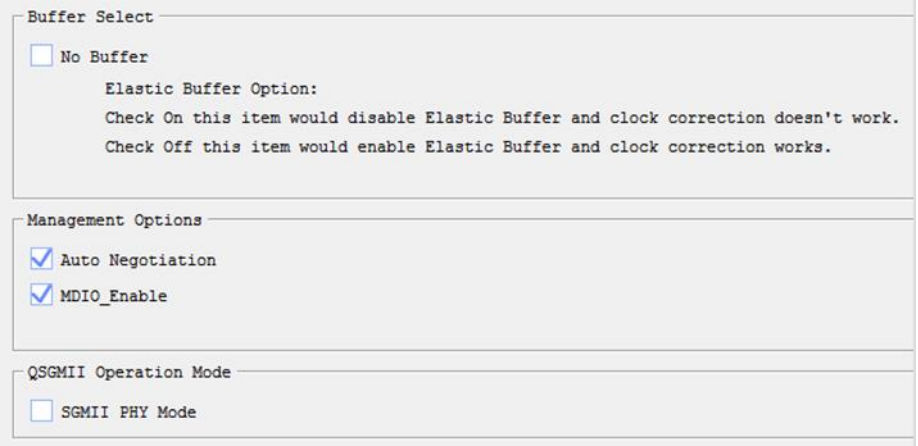

Figure 2-5 QSGMII IP Parameter Configuration Interface

For QSGMII IP configuration parameter description, please refer to Table 2-2.

Table 2-2 QSGMII IP Configuration Parameter Description

Option Domain	**Option Name/Parameter Name**	**Parameter Description**	**Default Value**
Buffer Select	No Buffer	Frequency offset Buffer not enabled selection Check: IP Clock Skew Buffer is not enabled	Cleared
Management Options	Auto Negotiation	Select whether to enable auto-negotiation Check: IP enable Auto-Negotiation	Selected
	MDIO_Enable	Select MDIO Configuration Management Interface Enable Check: IP enables the MDIO Configuration Management Interface	Selected
QSGMII Operation Mode	SGMII PHY Mode	QSGMII PHY mode selection Selected: IP operates in PHY mode Cleared: IP operates in MAC mode	Cleared

2.3.1.3 Generating IP

Upon completion of parameter configuration, click the <Generate> button in the top left corner to generate the QSGMII IP code according to the user-specific settings. The information report interface for IP generation is shown in Figure 2-6.

Figure 2-6 QSGMII IP Generation Report Interface

Upon successful IP generation, the files indicated in Table 2-3 will be output to the Project path specified in Figure 2-3.

Table 2-3 Output Files after IP Generation

Output File[2]	**Description**
$instname.v	The top-level .v file of the generated IP.
$instname.idf	The Configuration file of the generated IP.
/rtl/*.v	The plaintext RTL files of the generated IP.
/rtl/common/*.v	The plaintext RTL files of the generated IP, where the folder contains some common modules.
/rtl/hsstlp/ *	This folder contains the HSSTLP IP modules.
/rtl/synplify/*.vp	The nonplaintext RTL files of the generated IP, used for synthesis.
/sim_lib/modelsim/*.vp	The nonplaintext RTL files of the generated IP, which can be used for ModelSim or VCS simulation.
/sim/modelsim/*.f	The list of .v files required for ModelSim simulation of the generated Example Design.
/sim/modelsim/*.do	The .do script files and .do waveform files for ModelSim simulation of the generated Example Design.
/sim/modelsim/*.bat	The script for ModelSim simulation of the generated Example Design.
/example_design/bench/*.v	The simulation stimulus files for the Example Design.
/example_design/rtl/*.v	The top-level file of the Example Design and some module files used in the design.
/pnr/core_only/*.pds	The project file of the generated IP core.
/pnr/core_only/*.fdc	The constraint file of the generated IP core.
/pnr/core_only/*.v	The top-level file of the generated IP core project.
/pnr/example_design/*.pds	The project file of the Example Design.
/pnr/example_design/*.fdc	The constraint file of the generated Example_Design.
/rev_1	The default output path for synthesis reports. (This folder is generated only after specifying the synthesis tool)
/readme.txt	The readme file describes the structure of the generation directory after the IP is generated.

2 "$instname" is the instantiation name entered by the user; "*" is a wildcard character representing filenames of the same type.

Attention:

The .pds and .fdc files generated with the IP are for reference only; please modify the pin constraints according to the actual pin connections when in use.

The *_vpAll.vp file in the *.vp file includes the contents of other *.vp files, selecting this file is equivalent to selecting all other *.vp files; users can choose based on their preferences, but both cannot be selected at the same time, otherwise, an error will occur. The same applies to _simvpAll.vp.

2.3.2 Constraint Configuration

For the specific configuration method of constraint files, please refer to the relevant help documents in the PDS installation path: "***User_Constraint_Editor_User_Guide***", "***Physical_Constraint_Editor_User_Guide***", and "***Route_Constraint_Editor_User_Guide***".

2.3.3 Simulation Runs

The simulation of QSGMII IP is based on the Test Bench of the Example Design. For detailed information about Example Design, please refer to "2.4 Example Design".

For more details about the PDS simulation functions and third-party simulation tools, please consult the related help documents in the PDS installation path: "***Pango_Design_Suite_User Guide***", "***Simulation_User_Guide***".

2.3.4 Synthesis and Placement/Routing

The specific usage of PDS synthesis tools and placement/routing tools can be found in the help documents within the PDS installation path.

Attention:

Example Design project files .pds and pin constraint files .fdc generated with the IP are located in the "/pnr/example_design" directory, and physical constraints need to be modified according to the actual devices and PCB trace routing. For details, please refer to "2.8 Descriptions and Considerations".

2.3.5 Resources Utilization

Table 2-4 Typical Resource Utilization Values for QSGMII IP Based on Applicable Devices

Device	IP Operating Mode (Parameter check options)	Typical Resource Utilization Values				
		LUT	FF	HSSTLP	USCM	DRM
PG2L100H	Auto Negotiation MDIO_Enable SGMII PHY Mode	3290	4274	1	4	2
	Auto Negotiation MDIO_Enable SGMII PHY Mode No Buffer	2604	3396	1	4	0
	Auto Negotiation SGMII PHY Mode	2949	3945	1	3	2
	MDIO_Enable SGMII PHY Mode No Buffer	1686	1966	1	4	0
PG2L50H	Auto Negotiation MDIO_Enable SGMII PHY Mode	3302	4269	1	4	2
	Auto Negotiation MDIO_Enable SGMII PHY Mode No Buffer	2617	3389	1	4	0
	Auto Negotiation SGMII PHY Mode	2947	3943	1	3	2
	MDIO_Enable SGMII PHY Mode No Buffer	1696	1961	1	4	0
PG2L25H	Auto Negotiation MDIO_Enable SGMII PHY Mode	3298	4271	1	4	2
	Auto Negotiation MDIO_Enable SGMII PHY Mode No Buffer	2613	3393	1	4	0
	Auto Negotiation SGMII PHY Mode	2951	3946	1	3	2
	MDIO_Enable SGMII PHY Mode No Buffer	1686	1962	1	4	0
PG2L200H	Auto Negotiation MDIO_Enable SGMII PHY Mode	3428	4285	1	4	2
	Auto Negotiation MDIO_Enable SGMII PHY Mode No Buffer	2612	3394	1	4	0
	Auto Negotiation SGMII PHY Mode	3029	3956	1	3	2
	MDIO_Enable SGMII PHY Mode No Buffer	1670	1974	1	4	0

Device	IP Operating Mode (Parameter check options)	Typical Resource Utilization Values				
		LUT	FF	HSSTLP	USCM	DRM
PG2L100HX	Auto Negotiation MDIO_Enable SGMII PHY Mode	3388	4284	1	4	2
	Auto Negotiation MDIO_Enable SGMII PHY Mode No Buffer	2575	3394	1	4	0
	Auto Negotiation SGMII PHY Mode	3028	3956	1	3	2
	MDIO_Enable SGMII PHY Mode No Buffer	1620	1794	1	4	0

2.4 Example Design

This section mainly introduces the Example Design scheme based on QSGMII IP[3]. This scheme involves instantiating a MAC Side QSGMII IP and a PHY Side QSGMII IP that interface with each other to perform auto-negotiation, followed by data transmission, and using CRC to verify the accuracy of the data at the receive side. The scheme also includes the use of the MDIO interface to perform read and write operations on the registers of the QSGMII Core.

Descirption:

The HSSTLP IP register interface can only be accessed through the APB interface of SGMII Core0.

3 This Example Design scheme is only applicable to PG2L100H FBG676.

2.4.1 Design Block Diagram

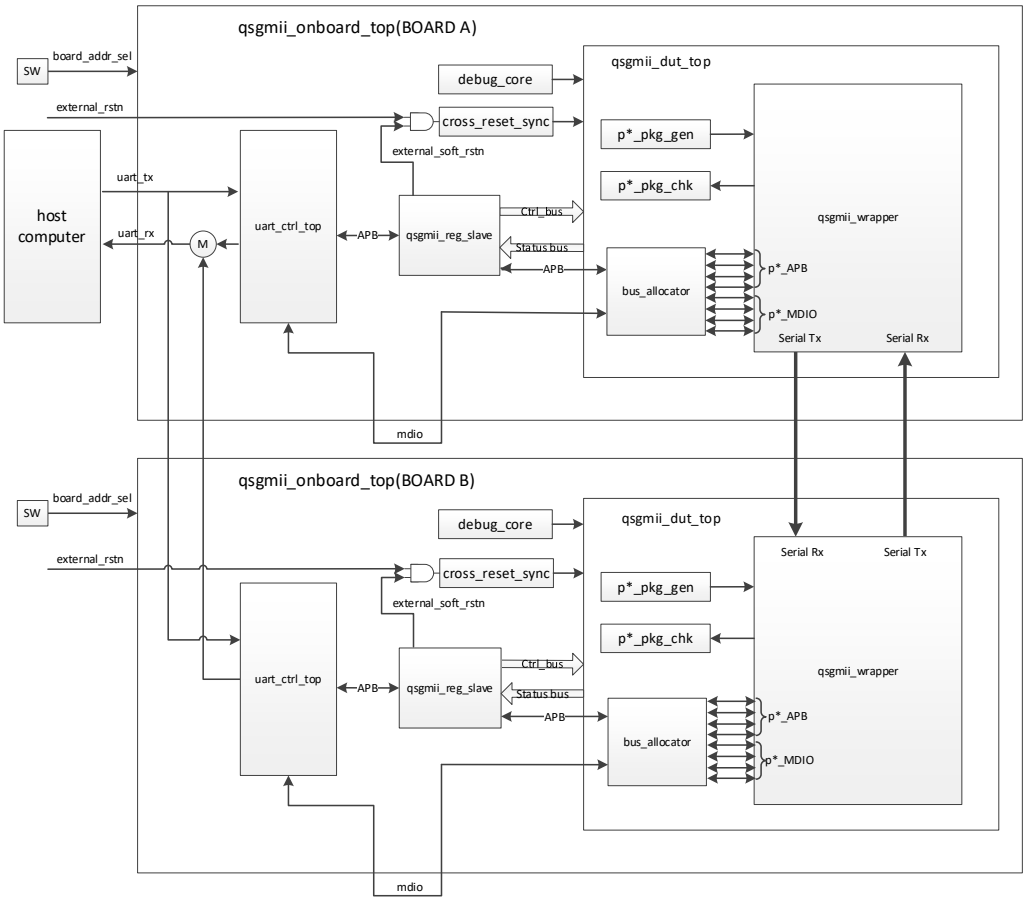

Figure 2-7 Example Design System Block Diagram

The system block diagram of Example Design is shown in Figure 2-7, where the uart_ctrl_top module completes the conversion between UART and the MDIO and APB interfaces. Control signals for the qsgmii_dut_top module are uniformly output by the uart_ctrl_top module and control the qsgmii_dut_top module after conversion by the qsgmii_reg_slave module. The status signals of the qsgmii_dut_top module are converted by the qsgmii_reg_slave module and output to the uart_ctrl_top module. Ⓜ indicates the selector that, according to the selection enable, transfers output data from the corresponding test board to the host computer.

2.4.2 Module Description

2.4.2.1 uart_ctrl_top

This is a serial port module used for debugging. This module receives UART data and then outputs the data in the format as per the APB or MDIO protocol, achieving data conversion between the serial port and the APB and MDIO interfaces. The serial port baud rate is fixed at 115200, with the read/write operation address being 32bit and the data 32bit.

2.4.2.1.1 Read and Write Operation Description

- Read operation format: "0x72" + "address";
- Write operation format: "0x77" + "address" + "data".

For the read and write operation examples, please refer to "2.8.6 Example of read and write operations for the uart_ctrl_top module".

2.4.2.1.2 Address description

For information about the address for accessing registers through the uart_ctrl_top module, please refer to Table 2-5.

Table 2-5 uart_ctrl_top Module Address Description

Address bits	Description
31:29	Not used, set to 0.
28	Single board address, used only for debugging.
27:25	Not used, set to 0.
24	Set to 0 when accessing registers via the APB interface; set to 1 when accessing through the MDIO interface.
23	Valid when accessing registers through the APB interface; Set to 0 when accessing the qsgmii_reg_slave module; set to 1 when accessing IP.
22:21	Not used, set to 0.
20:19	Used to differentiate the 4 SGMII Cores in the bus_allocator module; 2'b00: Operates SGMII Core0; 2'b01: Operates SGMII Core1; 2'b10: Operates SGMII Core2; 2'b11: Operates SGMII Core3.
18:0	IP register address (refer to "2.6 Description of the IP Register") or the register address within the qsgmii_reg_slave module (refer to Table 2-6).

2.4.2.2 qsgmii_reg_slave

For the custom register module used for debugging, please refer to Table 2-6 for relevant register descriptions.

Table 2-6 qsgmii_reg_slave Register Description

Register address (16bit)	**R/W**	**Description**	**Default value (32 bits)**
0x0041	W	This register configures all the 4 SGMII Cores simultaneously; bit 28: pin_cfg_en fast port configuration enable 0: Fast port configuration is invalid 1: Enable fast port configuration bit24: phy_duplex bit20: phy_link bit[17:16]: phy_speed 2'b11: Reserved 2'b10: SGMII 1000M 2'b01: SGMII 100M 2'b00: SGMII 10M bit4: an_enable 1'b0: Disable auto-negotiation 1'b1: Enable auto-negotiation bit0: an_restart 1'b 0: disable Auto-Negotiation restart; 1'b 1: auto-negotiation restart enabled.	0x01120010
0x0002	W	bit0: start_test 1'b0: Disable packet transmission 1'b1: Enable packet transmission	0x0

2.4.2.3 debug_core

PDS includes IP modules for debugging, which allows waveform capture and viewing of specific signals in certain modules via the Fabric Debugger tool. Specific usage can be found in the help documentation under the PDS installation path.

2.4.2.4 cross_reset_sync

Asynchronous signal synchronisation module, used for synchronising and debouncing externally input asynchronous signals.

2.4.2.5 qsgmii_dut_top[4]

The qsgmii_dut_top module includes the p*_pkg_gen module, p*_pkg_chk module, bus_allocator module, and qsgmii_wrapper module.

2.4.2.5.1 p*_pkg_gen

Data generation module, used for producing transmission data.

2.4.2.5.2 p*_pkg_chk

Data detection module, used for CRC verification of received data.

2.4.2.5.3 bus_allocator

The bus allocator module, which divides a single APB/MDIO into 4 paths, facilitates the input and output selection of the APB bus as well as the output selection of the MDIO bus. The APB bus of the this module reserves two bits [20:19] to identify multiple SGMII Cores in QSGMII IP. For specific address allocation, please refer to Table 2-5.

2.4.2.5.4 qsgmii_wrapper

QSGMII IP layer. For related interfaces, please refer to Table 2-9.

4 "*" represents 0, 1, 2, or 3, corresponding to the 4 SGMII Cores in QSGMII Core: SGMII Core0, SGMII Core1, SGMII Core2, and SGMII Core3.

2.4.3 Descriptions of Ports

Refer to Table 2-7 for the interface description of Example Design.

Table 2-7 Example Design Interface List

Port Name	Bit width	I/O	PORT Description	Pin constraints
free_clk	1	I	External reference clock[5] Frequency: 50MHz	G5
external_rstn	1	I	System reset signal 0: Reset 1: Reset release	AA23
hsst_cfg_soft_rstn	1	I	HSSTLP IP configuration parameter reset signal 0: Reset 1: Reset release	AA22
P_REFCKN	1	I	HSSTLP IP differential reference clock input N-terminal Frequency: 125MHz	E13
P_REFCKP	1	I	HSSTLP IP differential reference clock input P-terminal Frequency: 125MHz	F13
P_L0TXN	1	O	HSSTLP IP differential serial output signal N-terminal	-
P_L0TXP	1	O	HSSTLP IP differential serial output signal P-terminal	-
P_L0RXN	1	I	HSSTLP IP differential serial input signal N-terminal	-
P_L0RXP	1	I	HSSTLP IP differential serial input signal P-terminal	-
LED50M1S	1	O	free_clk clock indicator[6]	V24
LED125M1S	1	O	125M differential clock indication[6]	AA25
ok_led	1	O	Packet reception verification correct indicator 0: Light off (verification error) 1: Light on (verification correct)	W25
cfg_uart_txd	1	O	Local port for sending data to the host computer	C24
cfg_uart_rxd	1	I	Local port for receiving data from the host computer	D24
uart_rxd_to_partner	1	O	Port for sending data from local side to remote side	B19
uart_rxd_from_partner	1	I	Port for receiving data sent from remote side to local side	B20
l0_cdr_align	1	O	HSSTLP IP PMA CDR lock indicator (connected to l0_cdr_align port) 0: Light off (unlocked) 1: Light on (locked)	W24

5 Used as the APB pclk and the HSSTLP IP reset clock in this Example Design

6 Flashes once every 1 second under normal conditions

Port Name	Bit width	I/O	PORT Description	Pin constraints
l0_tx_pll_lock	1	O	HSSTLP IP PLL lock indicator (connected to l0_tx_pll_lock port) 0: Light off (unlocked) 1: Light on (locked)	AA24
l0_lsm_synced	1	O	HSSTLP IP Word Align alignment indicator (connected to l0_lsm_synced port) 0: Light off (not aligned) 1: Light on (aligned)	AC24
l0_an_status	1	O	QSGMII IP link status indicator 0: Light off (link issue) 1: Light on (link normal)	AB25
master_mdc_o	1	O	MDIO output clock, generated by the serial port module	D4
master_mdio	1	IO	MDIO data signal	A20
slave_l0_mdc	1	I	MDIO input clock (connected to master_mdc_o)	E5
slave_l0_mdio	1	IO	MDIO data signal (connected to master_mdio)	A19
l0_ctr13	1	I	Single board serial port address control signal 0: Board A 1: Board B	T24

Note: "-" indicates location constraint has been applied through HSSTLP-related constraints.

2.4.4 Test Method

Instantiate the QSGMII IP in the corresponding mode[7] to generate the bitstream using the IP's own Example Design project[8]. Use two test boards[9]for docking tests; one with the MAC Side bitstream programmed, and the other with the PHY Side bitstream programmed; evaluate the test results based on the link indicators and CRC verification.

7 For details, please refer to "2.4.5 Instance Configuration" and "2.3.1 Module Instantiation".

8 For the Example Design project path, see Table 2-3.

9 The model number of the PG2L100H test board is P04I100RD04_A2.

In the Example Design, a debug_core module has been added. Through board-to-board connection tests, data can be captured from the PCS transmitter and receiver using the Fabric Debugger tool in the PDS software. This tool also allows for the collection of statistics on the number of packets transmitted and received. The relevant screenshots are shown below. Users may add or remove signals to be captured according to actual needs. For the description of debug_core signals, please refer to Figure 2-8.

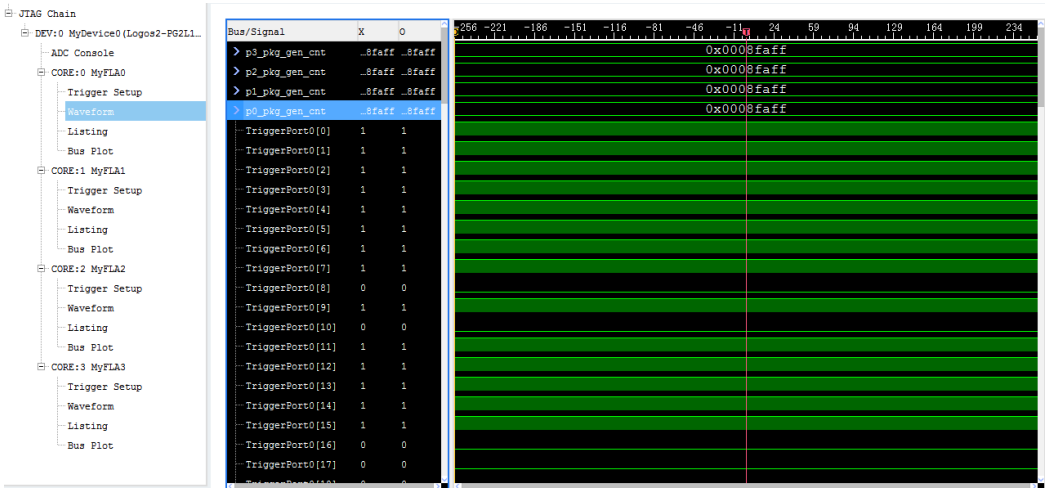

Figure 2-8 Packet Transmission Statistics at the GMII Side

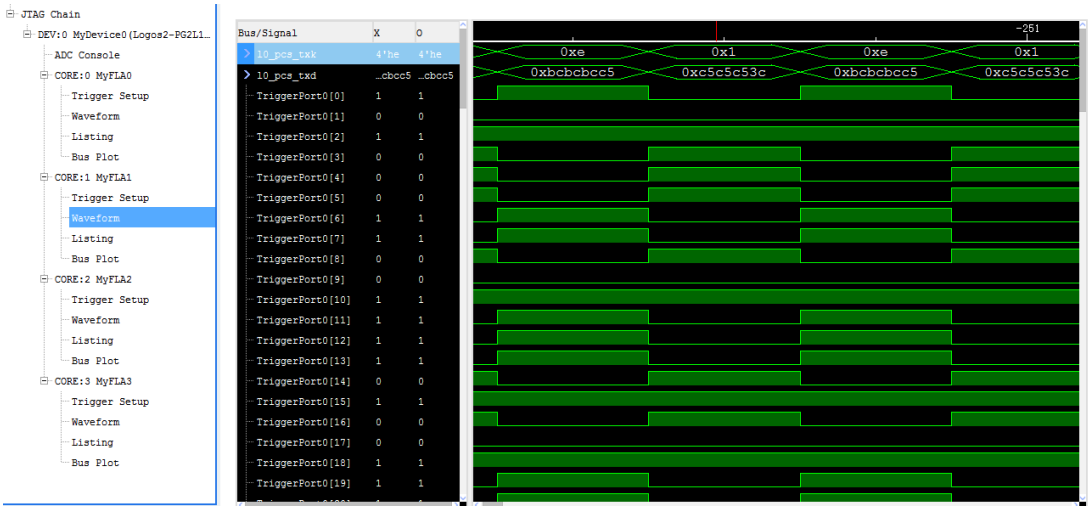

Figure 2-9 Data at PCS Transmitter

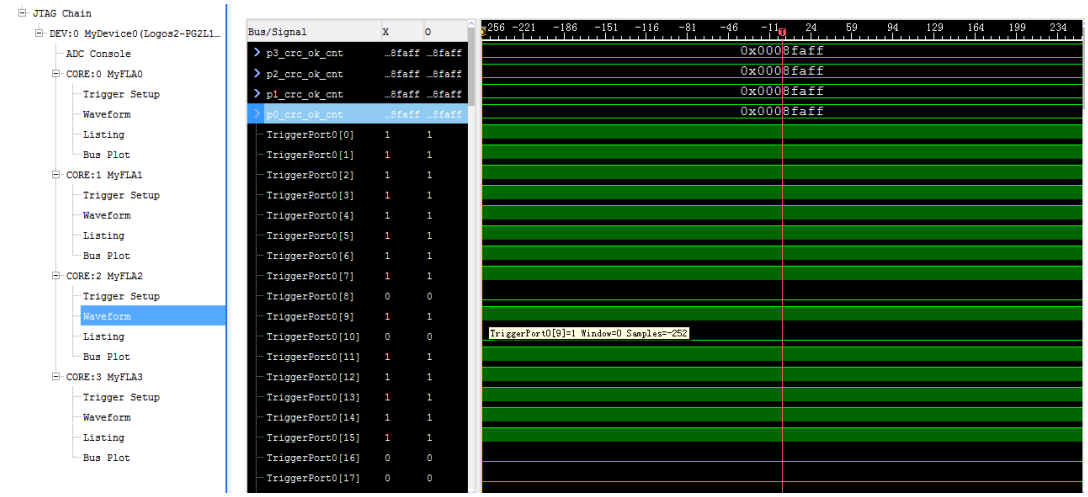

Figure 2-10 Packet Reception Statistics at the GMII Side

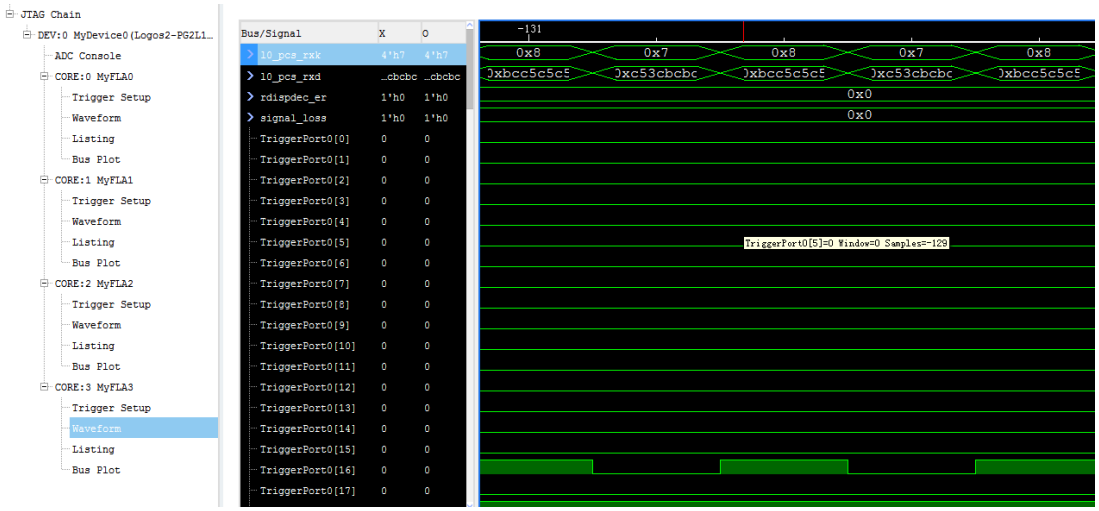

Figure 2-11 Data at PCS Receiver

Table 2-8 debug_core Signal Explanation

debug_core numbering	TriggerPort	Signal Name
debug_core0	TriggerPort[0]~TriggerPort[31]	p0_pkg_gen_cnt[31:0]
	TriggerPort[32]~TriggerPort[63]	p1_pkg_gen_cnt[31:0]
	TriggerPort[64]~TriggerPort[95]	p2_pkg_gen_cnt[31:0]
	TriggerPort[96]~TriggerPort[127]	p3_pkg_gen_cnt[31:0]
debug_core1	TriggerPort[0]~TriggerPort[31]	l0_pcs_txd[31:0]
	TriggerPort[32]~TriggerPort[35]	l0_pcs_txk[3:0]
	TriggerPort[36]~TriggerPort[127]	92'b0

debug_core numbering	TriggerPort	Signal Name
debug_core2	TriggerPort[0]~TriggerPort[31]	p0_crc_ok_cnt[31:0]
	TriggerPort[32]~TriggerPort[63]	p1_crc_ok_cnt[31:0]
	TriggerPort[64]~TriggerPort[95]	p2_crc_ok_cnt[31:0]
	TriggerPort[96]~TriggerPort[127]	p3_crc_ok_cnt[31:0]
debug_core3	TriggerPort[0]	signal_loss
	TriggerPort[1]~TriggerPort[7]	7'b0
	TriggerPort[8]	rdispdec_er
	TriggerPort[9]~TriggerPort[15]	7'b0
	TriggerPort[16]~TriggerPort[47]	l0_pcs_rxd[31:0]
	TriggerPort[48]~TriggerPort[51]	l0_pcs_rxk[4:0]
	TriggerPort[52]~TriggerPort[127]	76'b0

2.4.5 Instance Configuration

2.4.5.1 MAC Side

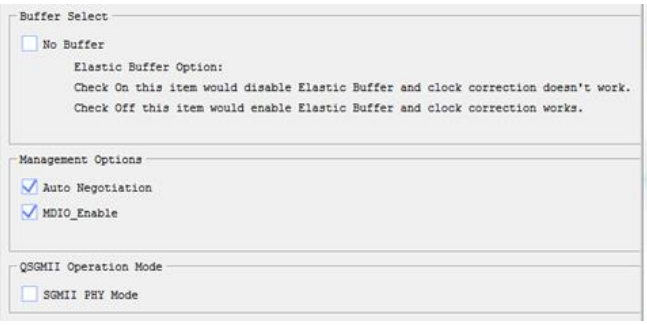

Figure 2-12 QSGMII MAC Side Configuration Diagram

2.4.5.2 PHY Side

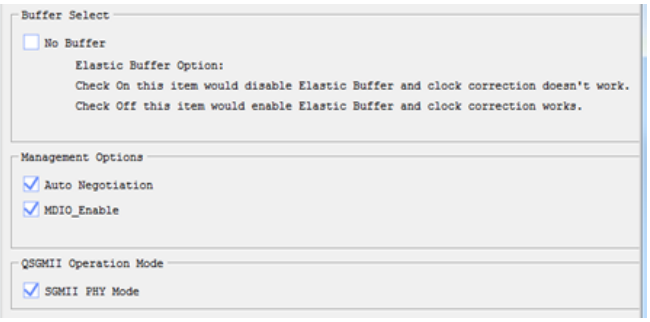

Figure 2-13 QSGMII PHY Side Configuration Diagram

2.4.6 Instance Simulation

In the Windows system, after IP generation, double-click the *.bat file [10] under the "<project_path>/sim/modelsim" path to run simulation.

Attention:

Do not directly use the Example Design generated by the IP for Flow on-board testing; Modify physical constraints according to the devices and the PCB traces used, then proceed with Flow on-board testing. For details, please refer to "2.8 Descriptions and Considerations".

2.5 Descriptions of IP Interfaces

This section provides the QSGMII IP related interface instructions and timing descriptions.

10 For the output files after IP generation, please refer to Table 2-3.

2.5.1 IP Interface Description

2.5.1.1 Port Block Diagram

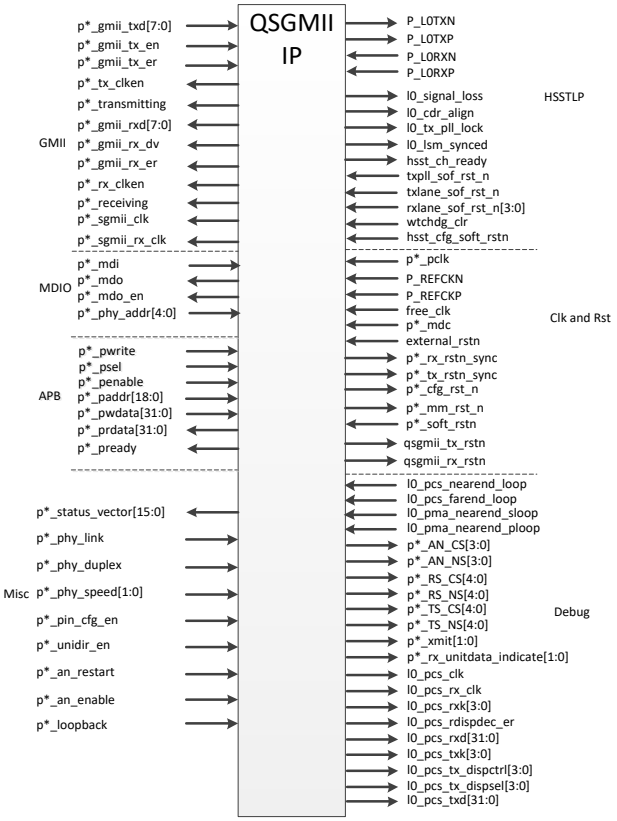

Figure 2-14 QSGMII IP Interface

Descirption:

"*" in "p*" represents 0, 1, 2 or 3, corresponding to the interface signal of SGMII Core0, SGMII Core1, SGMII Core2, and SGMII Core3 respectively.

2.5.1.2 Port List

Table 2-9 QSGMII IP Interface Signal List

Port[11]	I/O	Bit width	Description
Clock and Reset Signals			
free_clk	I	1	Reset sequence reference clock for HSSTLP IP Frequency: 10MHz~100MHz
external_rstn	I	1	Global asynchronous reset signal (free_clk clock domain) 0: Reset 1: Reset release
p*_soft_rstn	I	1	SGMII Core global asynchronous reset signal (free_clk clock domain) 0: Reset 1: Reset release
qsgmii_tx_rstn	O	1	QSGMII logical reset in TX direction (l0_pcs_clk clock domain) 0: Reset 1: Reset release
qsgmii_rx_rstn	O	1	QSGMII logical reset in RX direction (l0_pcs_rx_clk clock domain) 0: Reset; 1: Reset release
MDIO Interface[12]			
p*_mdc	I	1	Management Data Clock (for MDIO interface clock) This port must have a clock input when MDIO is enabled Frequency: 2.5MHz
p*_mdi	I	1	Management Data In
p*_mdo	O	1	Management Data Out
p*_mdo_en	O	1	Output enable control signal 0: mdo invalid 1: mdo valid
p*_phy_addr	I	5	MDIO PHY Address
p*_mm_rst_n	O	1	Global asynchronous reset 0: Reset 1: Reset release Note: In the management interface clock domain

11 Throughout this document, the "*" in p* represents 0, 1, 2 or 3, corresponding to the 4 SGMII Cores used in the QSGMII Core. Signals with "p*", "l0", or "L0" in their names are related to Lane0; signals without "p*" or "l0" are applicable to Lanes 0~3.

12 Valid when configuring the management interface as MDIO (check "MDIO_Enable"), please refer to "2.3.1.2 IP Parameter Configuration".

Port[11]	I/O	Bit width	Description
APB Interface[13]			
p*_cfg_rst_n	O	1	SGMII Core configuration logic reset output, operating in the free_clk clock domain 0: Reset 1: Reset release
p*_pclk	I	1	APB Clock (for APB interface clock) Frequency: 50MHz~100MHz
p*_paddr[18:0]	I	19	APB interface read/write address bus
p*_pwrite	I	1	APB write enable signal 1: Write data 0: Read data
p*_psel	I	1	APB interface Chip Select signal 1: Selected 0: Cleared
p*_penable	I	1	APB interface access enable 1: Enabled 0: Not enabled
p*_wdata[31:0]	I	32	APB interface write data bus
p*_prdata[31:0]	O	32	APB interface read data bus
p*_pready	O	1	APB interface read/write Ready signal For write operation: 0: Data has not been successfully written to the register 1: Data has been successfully written to the register For read operation: 0: Read data is not yet ready 1: Read data is now ready
Fast Configuration Interface[14]			
p*_pin_cfg_en	I	1	Fast configuration enable signal[15] 1: Fast configuration interface valid 0: Fast configuration interface invalid
p*_phy_link	I	1	PHY Link status (meaningful in QSGMII PHY mode) 1:Link Up 0:Link Down Corresponding to register Reg4.15
p*_phy_duplex	I	1	PHY duplex status (meaningful in QSGMII PHY mode) 1: Full duplex 0: Half duplex Corresponding to register Reg4.12

13 Valid when configuring the management interface as APB (uncheck "MDIO_Enable"), please refer to "2.3.1.2 IP Parameter Configuration".

14 This group of signals needs to be generated in the clock domain (mdc/free_clk) of the management interface (MDIO/APB).

15 Fast configuration of registers only affects Reg0 and Reg4, and does not affect other registers. For details, please refer to "2.5.3 Fast Configuration Interface".

Port[11]	I/O	Bit width	Description
p*_phy_speed[1:0]	I	2	PHY operational speed (meaningful in QSGMII PHY mode) 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps Under QSGMII PHY mode Corresponding to registers Rg4.11:10 when Auto-Negotiation is enabled Corresponding to registers {Reg0.6,Reg0.13} when Auto-Negotiation is disabled Under QSGMII MAC mode Meaningless when auto-negotiation is enabled Corresponding to registers {Reg0.6,Reg0.13} when Auto-Negotiation is disabled
p*_unidir_en	I	1	Undirectional mode enable control 0: Not enabled 1: Enabled Corresponding to register Reg0.5
p*_an_restart	I	1	Auto-negotiation restart control 0: Normal operation 1: Restart auto-negotiation Corresponding to register Reg0.9
p*_an_enable	I	1	Auto-negotiation enable control 0: Not enabled 1: Enabled Corresponding to register Reg0.12
p*_loopback	I	1	SGMII Core internal loopback enable[16] 0: Disabled 1: Internal loop enabled at the interface between the SGMII Core and QSGMII Core Corresponding to register Reg0.14
Status Indicator			
p*_status_vector[15:0]	O	16	Output state statistical vector Bit[15]:Resolve Priority: Controls the Invocation of the Priority Resolution Function. This signal is pulled high in the Auto-Negotiation IDLE_DETECT and LINK_OK states, and low in other states Bit[14]:an_complete: Auto-negotiation completion indication: 1: complete: 0: Not completed Bit[13]:an_page_rx: Indication of new configuration data received by Auto-Negotiation 1: New configuration data received 0: New configuration data not received Bit[12]:rxdisp_er: 10B/8B decoding polarity error indication

16 Loopback functions cannot be used when frequency bias Buffer is not enabled.

Port[11]	I/O	Bit width	Description
			1: Incorrect polarity 0: Correct polarity Bit[11]:rxdec_er: 10B/8B decoding data error indication 1: Data error 0: Data correct Bit[10:9]:Remote Fault Encode: Link status passed by Link Partner received from auto-negotiation SGMII MAC mode: 10: Link abnormal 00: Link normal In SGMII PHY mode: Fixed to 0: Under GE mode: 00:No Error, Link OK. 01:Offline 10:Link Failure 11:Auto-Negotiation_Error Bit[8:7]:Pause: Pause capability of Link Partner received from Auto-Negotiation (valid in GE mode) Bit[6]: elastic Buffer state: 1: Overflow 0 : No overflow Bit[5]: Indication for half-duplex/full-duplex: 1: Full duplex 0: Half duplex Bit[4:3]: SGMII rate indication: 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps Bit[2:1]:RUDI: 00: Reserved 01: Invalid (an error occurred while receiving C-code or I-code) 10: /C/ (receiving C-code) 11: /I/ (receiving I-code) Bit[0]: Auto-Negotiation related port, Link Status When auto-negotiation is enabled: 1: Synchronization successful and auto-negotiation completed 0: Synchronization failed or Auto-Negotiation incomplete When auto-negotiation is disabled: 1: Synchronization successful 0: Synchronization failed
GMII Interface			
p*_sgmii_clk	O	1	SGMII operating clock Frequency: 125MHz
p*_tx_clken	O	1	sgmii_clk clock enable signal, active high
p*_tx_rstn_sync	O	1	Reset signal sent by GMII to Fabric in TX direction 0: Reset 1: Reset release
p*_sgmii_rx_clk	O	1	SGMII logic operating clock in receive direction Frequency: 125MHz

Port[11]	I/O	Bit width	Description
p*_rx_clken	O	1	sgmii_rx_clk clock enable signal, active high
p*_rx_rstn_sync	O	1	Reset signal sent by GMII to Fabric in RX direction 0: Reset 1: Reset release
p*_gmii_rxd[7:0]	O	8	GMII RXD[7:0] signal
p*_gmii_rx_dv	O	1	GMII RX_DV signal
p*_gmii_rx_er	O	1	GMII RX_ER signal
p*_receiving	O	1	PCS recives status signal 1: PCS signal reception in progress 0: No PCS signal reception
p*_gmii_txd[7:0]	I	8	GMII TXD[7:0] signal
p*_gmii_tx_en	I	1	GMII TX_EN signal
p*_gmii_tx_er	I	1	GMII TX_ER signal
p*_transmitting	O	1	PCS transmits status signal 1: PCS signal transmission in progress 0: No PCS signal transmission
HSSTLP IP Interface			
P_L0TXN	O	1	HSSTLP IP differential serial output signal N-terminal
P_L0TXP	O	1	HSSTLP IP differential serial output signal P-terminal
P_L0RXN	I	1	HSSTLP IP differential serial input signal N-terminal
P_L0RXP	I	1	HSSTLP IP differential serial input signal P-terminal
P_REFCKN	I	1	HSSTLP IP differential reference clock input signal N-terminal
P_REFCKP	I	1	HSSTLP IP differential reference clock input signal Pterminal
l0_signal_loss	O	1	Port valid signal detection: 1: No valid signal was detected from port P_L0RXP/ P_L0RXN 0: Valid signal was detected from port P_L0RXP/ P_L0RXN Note: This is an asynchronous signal.
l0_cdr_align	O	1	CDR lock flag signal 0: CDR is not locked 1: CDR is locked successfully Note: This is an asynchronous signal.
l0_tx_pll_lock	O	1	TX PLL lock status flag signal 0: PLL not locked 1: PLL is locked; Note: This is an asynchronous signal.
l0_lsm_synced	O	1	Word Alignment successful, state machine lock flag 0: Word Align unsuccessful 1: Word Align successful Note: This is an asynchronous signal.
hsst_ch_ready[3:0]	O	4	HSSTLP IP reset sequence completion indicator (free_clk clock domain) 1: complete: 0: Incomplete: Bit0~Bit3 correspond to Lane0~Lane3 respectively
txpll_sof_rst_n	I	1	PLL soft reset signal (free_clk clock domain) 1: Reset release 0: Reset

Port[11]	I/O	Bit width	Description
txlane_sof_rst_n	I	1	TX Lane soft reset signal (free_clk clock domain) 1: Reset release 0: Reset
rxlane_sof_rst_n[3:0]	I	4	RX Lane soft reset signal (free_clk clock domain) 1: Reset release 0: Reset Bit0~Bit3 correspond to Lane0~Lane3 respectively
wtchdg_clr	I	1	Watchdog clear signal (free_clk clock domain) 1: All watchdog counters cleared 0: Normal Operation
hsst_cfg_soft_rstn	I	1	HSSTLP IP configuration module soft reset signal (free_clk clock domain) 1: Reset release 0: Reset Perform one external_rstn after enabling this reset
Debug Interface			
l0_pcs_farend_loop	1	I	PCS parallel far-end loopback enable 0: Not enabled 1: Enabled
l0_pcs_nearend_loop	I	1	PCS parallel near-end loopback enable 0: Not enabled 1: Enabled
l0_pma_nearend_ploop	I	1	PMA parallel near-end loopback enable 0: Not enabled 1: Enabled
l0_pma_nearend_sloop	I	1	PMA serial near-end loopback enable 0: Not enabled 1: Enabled
p*_AN_CS[3:0]	O	4	Current state of Auto-Negotiation module (p*_sgmii_clk clock domain)
p*_AN_NS[3:0]	O	4	Next state of Auto-Negotiation module (p*_sgmii_clk clock domain)
p*_RS_CS[4:0]	O	5	Current state of soft core receive module (p*_sgmii_clk clock domain)
p*_RS_NS[4:0]	O	5	Next state of soft core receive module (p*_sgmii_clk clock domain)
p*_TS_CS[4:0]	O	5	Current state of soft core transmission module (p*_sgmii_clk clock domain)
p*_TS_NS[4:0]	O	5	Next state of soft core transmission module (p*_sgmii_clk clock domain)
p*_xmit[1:0]	O	2	xmit signal output by Auto-Negotiation state machine (p*_sgmii_clk clock domain) 00: Reserved 01: CONFIGURATION 10: DATA 11: IDLE

Port[11]	I/O	Bit width	Description
p*_rx_unitdata_indicate [1:0]	O	2	rx_sm output data type signal[17] 00: Reserved 01: Invalid 10: /C/ 11: /I/
l0_pcs_clk	O	1	PCS transmit data clock
l0_pcs_rx_clk	O	1	PCS receive data clock
l0_pcs_rxk[3:0]	O	4	Indicates current pcs data type (pcs0_rx_clk clock domain) 1: pcs_rxd is a PCS control signal 0: pcs_rxd is a PCS data signal
l0_pcs_rdispdec_er[3:0]	O	4	Decode polarity error indication (pcs0_rx_clk clock domain) 1: 10b/8b decoding polarity error or data error 0: 10b/8b decoding normal
l0_pcs_rxd[31:0]	O	32	Data signal received by pcs_rx_sm (pcs0_rx_clk clock domain)
l0_pcs_txk[3:0]	O	4	Indicates current pcs data type (pcs0_rx_clk clock domain) 1: pcs_txd is a PCS control signal 0: pcs_txd is a PCS data signal
l0_pcs_tx_dispctrl[3:0]	O	4	disparity control signal, used for forcing 8b10b polarity and the mandatory replacement from I2 to I1 tx_dispctrl, tx_dispsel: 00: Normal data transmission 01: I2 replaced with I1 10: Disparity forced to be negative 11: Disparity forced to be positive
l0_pcs_tx_dispsel[3:0]	O	4	Please refer to pcs0_tx_dispctrl signal description (pcs0_rx_clk clock domain)
l0_pcs_txd[31:0]	O	32	Data signal transmitted by PCS (pcs0_rx_clk clock domain)

2.5.2 Register Management Interface

QSGMII IP provides two types of register configuration management interfaces — APB interface and MDIO interface. Users can enable/disable the MDIO interface using the MDIO_Enable option. For detailed descriptions, please refer to "2.3.1.2 IP Parameter Configuration".

Both the APB and MDIO interfaces include 4 independent sets of interface signals (refer to Table 2-9 for details), which correspond to the 4 SGMII Cores within the QSGMII Core and can be used for accessing the separate configuration registers of each SGMII Core.

17 It operates in the p*_sgmii_rx_clk clock domain under the No Buffer mode, and in the p*_sgmii_clk clock domain when the frequency offset Buffer is enabled.

- When the MDIO interface is disabled, the QSGMII IP operates the registers of the HSSTLP IP and QSGMII Core through the APB interface.
- When the MDIO interface is enabled, the QSGMII IP operates the registers of HSSTLP IP through the APB interface and the registers of QSGMII Core through the MDIO interface.

Descirption:

The QSGMII IP can only operate the registers of HSSTLP IP through the APB interface of SGMII Core0, as shown in the figure Figure 2-1.

2.5.2.1 APB Interface Timing Description

2.5.2.1.1 APB Write Timing

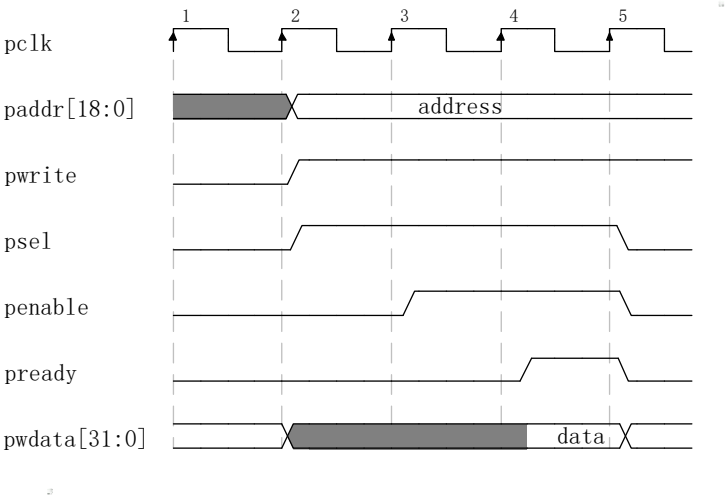

Figure 2-15 Basic APB Write Timing

2.5.2.1.2 APB Read Timing

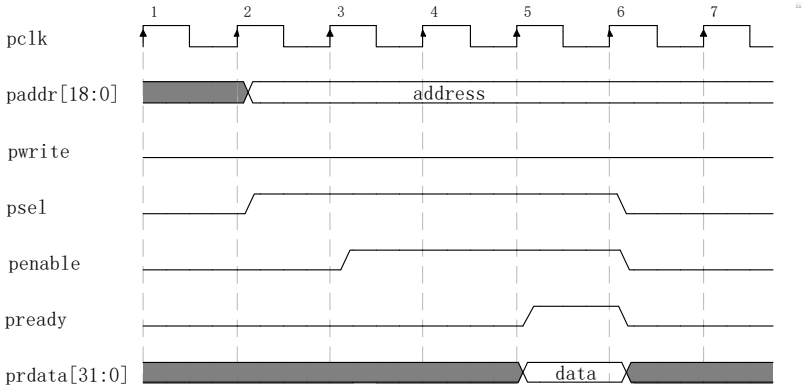

Figure 2-16 Basic APB Read Timing

2.5.2.2 MDIO Interface Timing Description

2.5.2.2.1 MDIO Write Timing

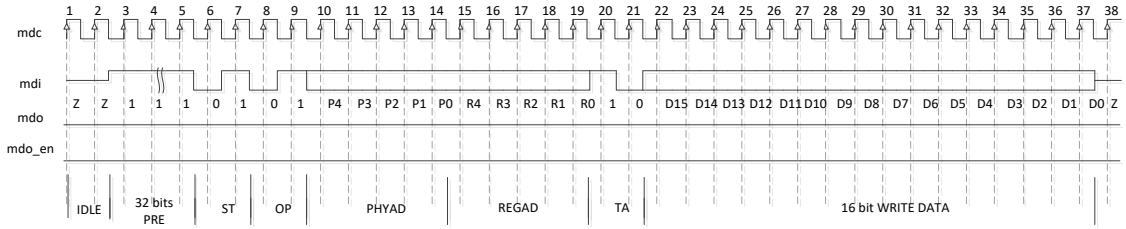

Figure 2-17 MDIO Write Timing

2.5.2.2.2 MDIO Write Timing

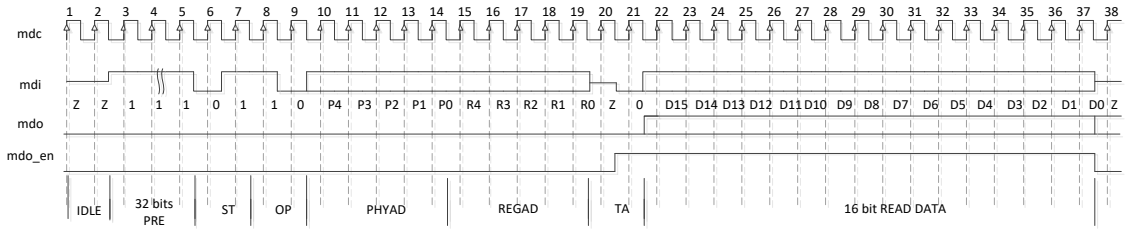

Figure 2-18 MDIO Write Timing

2.5.3 Fast Configuration Interface

The fast configuration interface allows for quick configuration of registers Reg0 and Reg4. When the fast configuration enable signal is active, the configuration information can be written directly to the corresponding configuration registers. Timing requirements are as follows:

- The fast configuration enable signal must be kept high for at least one configuration management interface clock cycle;
- The configuration information must remain stable for at least one configuration management interface clock cycle.

When the fast configuration enable signal is valid, registers other than Reg0 and Reg4 are written via the configuration management interface, and all registers are read via the configuration management interface; when the fast configuration interface enable signal is not valid, all registers are read and written via the configuration management interface.

2.5.4 GMII Interface

2.5.4.1 GMII Transmit Timing

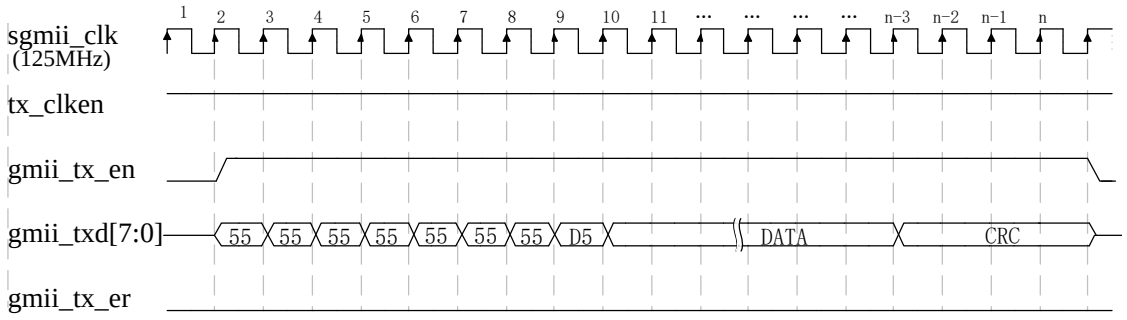

Figure 2-19 GMII Transmit Timing at a Rate of 1000Mbps

Attention:

At a rate of 10Mbps, tx_clken is pulled high every 100 cycles of the 125MHz clock, with each data lasting for 100 cycles of the 125MHz clock;

At a rate of 100Mbps, tx_clken is pulled high every 10 cycles of the 125MHz clock, with each data lasting for 10 cycles of the 125MHz clock;

At a rate of 1000Mbps, tx_clken is high throughout, with each data lasting for 1 cycle of the 125MHz clock.

2.5.4.2 GMII Receive Timing

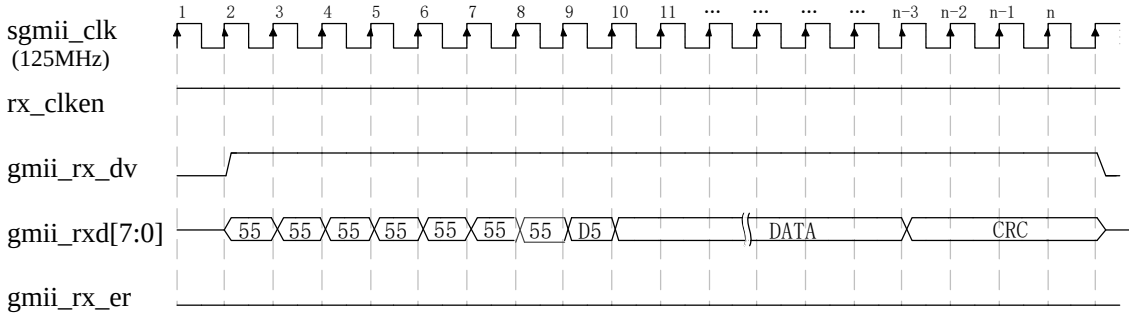

Figure 2-20 GMII Receive Timing at a Rate of 1000Mbps

Attention:

At a rate of 10Mbps, rx_clken is pulled high every 100 cycles of the 125MHz clock, with each data lasting for 100 cycles of the 125MHz clock;

At a rate of 100Mbps, rx_clken is pulled high every 10 cycles of the 125MHz clock, with each data lasting for 10 cycles of the 125MHz clock;

At a rate of 1000Mbps, rx_clken is high throughout, with each data lasting for 1 cycle of the 125MHz clock.

2.6 Description of the IP Register

This section provides the QSGMII IP related register description and access methods.

2.6.1 SGMII Core Register Descriptions

Descirption:

Rest will reset all registers to default values

The register features include "self-clearing" registers, which, after being configured via the management configuration interface, will automatically reset to zero after one clock cycle of the management configuration interface. When configuring self-clearing registers via the Fast Configuration port, the self-clear function does not operate, requiring manual cancellation of the port configuration.

The register features include "read-to-clear" registers, which immediately reset to zero after their value is read through the management configuration interface.

Each SGMII Core has a set of registers that are identically defined and independently accessible, which can be accessed through their management configuration interfaces.

2.6.1.1 Auto-Negotiation Enabled

Table 2-10 Register Definitions When Auto-negotiation Function is Enabled

Address	Register	Description
0	Control Register (Register 0)	Parameters for Configuring SGMII Module Functionality
1	Status Register (Register 1)	SGMII Module Status Parameters
2	PHY Identifier Register (Register 2 and 3)	PHY ID
3	PHY Identifier Register (Register 2 and 3)	PHY ID
4	Auto-Negotiation Advertisement Register (Register 4)	Local Devices Auto-Negotiation Capability
5	Auto-Negotiation Link Partner Ability Base Register (Register 5)	Remote Devices Auto-Negotiation Capability
6	Auto-Negotiation Expansion Register (Register 6)	Auto-Negotiation Expansion Register
15	Extended Status Register (Register 15)	Extended Status Register
16	Vender_spc Register (Register 16)	Buffer Control Register
17	Vender_spc_1 Register (Register 17)	Loopback Control Register

Table 2-11 SGMII Control (Register 0)

Bits	Item	Description	Access Type	Reset Values
0.15	Reserved	Reserved Field	Read Only	0
0.14	Loopback	Loopback Mode Enable 1: Enabled 0: Not enabled	Read/Write	0
0.13	Speed Selection(LSB)	0: Speed is 1000Mbps	Read Only	0
0.12	Auto-Negotiation Enable	Auto-Negotiation enable control[18] 1: Enabled 0: Not enabled	Read/Write	1
0.11:10	Reserved	Reserved Field	Read Only	01
0.9	Restart Auto-Negotiation	Auto-Negotiation Restart Enable Control[18] 1: Restart 0: Normal operation	Read /Write/Self-cleaning	0
0.8	Duplex Mode	1: Full duplex	Read Only	1
0.7	Reserved	Reserved Field	Read Only	0
0.6	Speed Selection(MSB)	1: Speed is 1000Mbps	Read Only	1
0.5	Unidirectional Enable	Undirectional mode enable control 0: Not enabled 1: Enabled (the state of reception will not affect the operation of transmission)	Read/Write	0
0.4:0	Reserved	Reserved Field	Read Only	000000

Table 2-12 SGMII Status Register (Register 1)

Bits	Item	Description	Access Type	Reset Values
1.15:9	Reserved	Reserved Field	Read Only	0000000
1.8	Extended Status	States Supported by Extended Status Register (reg15)	Read Only	1
1.7	Unidirectional Ability	States Supported by Unidirectional Mode	Read Only	1
1.6	Reserved	Reserved Field	Read Only	0
1.5	Auto-Negotiation Complete	Auto-negotiation completion indication[18] 1: complete: 0: Incomplete:	Read Only	0
1.4	Remote Fault	Remote Fault reception indication 1: Received 0: Not received	Read-Only/Read-to-Clear/LH	0

18 When Auto-Negotiation is disabled, this register is ignored.

Bits	Item	Description	Access Type	Reset Values
1.3	Auto-Negotiation Ability	States of auto-negotiation capability supported[18]	Read Only	1
1.2	Link Status	When auto-negotiation is enabled: 1: Synchronization successful and auto-negotiation completed 0: Synchronization failed or Auto-Negotiation incomplete When auto-negotiation is disabled: 1: Synchronization successful 0: Synchronization failed	Read-Only/Read-to-Clear/LL	0
1.1:0	Reserved	Reserved Field	Read Only	00

Table 2-13 PHY Identifier Register (Register 2 and 3)

Bits	Item	Description	Access Type	Reset Values
2.15:0	Organizationally Unique Identifier	Undefined	Read/Write	0000000000000000
3.15:10			Read/Write	000000
3.9:4	Manufacturer's Model Number	Undefined	Read/Write	000000
3.3:0	Revision Number	Undefined	Read/Write	00000

Table 2-14 SGMII Auto-Negotiation Advertisement MAC Mode(Register 4)

Bits	Item	Description	Access Type	Reset Values
4.15:0	All bits	MAC Side is a fixed value	Read Only	0100000000000001

Attention:

SGMII MAC Side speed uses the remote speed, default speed is 1000M.

Table 2-15 SGMII Auto-Negotiation Advertisement in PHY Mode (Register 4)

Bits	Item	Description	Access Type	Reset Values
4.15	PHY Link Status	When pin_cfg_en=0, it is controlled by the management configuration interface; When pin_cfg_en=1, it is controlled by l0_phy_link; phy_link control: 1: Connection done 0: Connection fails	Read/Write	0

Bits	Item	Description	Access Type	Reset Values
4.14	Acknowledge	Local side response bit	Read Only	0
4.13	Reserved	Reserved Field	Read Only	0
4.12	Duplex Mode	When pin_cfg_en=0, it is controlled by the management configuration interface; When pin_cfg_en=1, it is controlled by l0_phy_duplex; phy_duplex control: 1: Full duplex 0: Half duplex	Read/Write	0
4.11:10	Speed	When pin_cfg_en=0, it is controlled by the management configuration interface; When pin_cfg_en=1, it is controlled by l0_phy_speed; phy_speed control: 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps	Read/Write	00
4.9:1	Reserved	Reserved Field	Read Only	000000000
4.0	Reserved	Reserved Field	Read Only	1

Table 2-16 SGMII Auto-Negotiation Link Partner Ability Base (Register 5)

Bits	Item	Description	Access Type	Reset Values
5.15	PHY Link Status	1: Connection done 0: Connection fails	Read Only	0
5.14	Acknowledge	1: Acknowledge (remote end has received information) 0: No Acknowledge (remote end has not received information)	Read Only	0
5.13	Reserved	Reserved Field	Read Only	0
5.12	Duplex Mode	1: Full duplex 0: Half duplex	Read Only	0
5.11:10	Speed	Remote speed 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps	Read Only	10
5.9:1	Reserved	Reserved Field	Read Only	000000000
5.0	Reserved	Reserved Field	Read Only	0

Table 2-17 Auto-Negotiation Expansion Register (Register 6)

Bits	Item	Description	Access Type	Reset Values
6.15:2	Reserved	Reserved Field	Read Only	0000000000000
6.1	Page Received	1: A new Page message received 0: No new Page message received	Read-Only/Read-to-Clear/LH	0
6.0	Reserved	Reserved Field	Read Only	0

Table 2-18 Extended Status Register (Register 15)

Bits	Item	Description	Access Type	Reset Values
15.15	1000BASE-X Full Duplex	1000BASE-X Full Duplex (Supported)	Read Only	1
15.14	1000BASE-X Half Duplex	1000BASE-X Half Duplex (Not Supported)	Read Only	0
15.13	1000BASE-T Full Duplex	1000BASE-T Full Duplex (Not Supported)	Read Only	0
15.12	1000BASE-T Half Duplex	1000BASE-T Half Duplex (Not Supported)	Read Only	0
15.11:0	Reserved	Reserved Field	Read Only	000000000000

Table 2-19 Vender_spc Register (Register 16)

Bits	Item	Description	Access Type	Reset Values
16.15:8	Reserved	Reserved Field	Read Only	00000000
16.7:4	Min_ipg	Minimum Frame Interval Configuration[19]	Read/Write	0110
16.3:0	Reserved	Reserved Field	Read Only	0001

19 When the "No Buffer" option is cleared, configure the appropriate minimum frame interval based on the actual application.

Attention:

When the No Buffer parameter is cleared, a frequency offset correction Buffer is instantiated within the SGMII Core, which can transfer received data from the recovered clock domain to the local clock domain. When there is a frequency offset between the clock recovered from received data and the local clock, the Buffer corrects the frequency offset by inserting or deleting Idle.

Should frequency offset be corrected by deleting Idle frames, which reduces the number of bytes in the frame interval, this can be managed by configuring the Min_ipg register to ensure Buffer deletes Idle frames only when the byte count in the frame interval exceeds the Min_ipg configured value, and the resulting byte count after Idle deletion is still not less than the Min_ipg configured value.

Table 2-20 Vendor-specific 1 Register (Register 17)

Bits	Item	Description	Access Type	Reset Values
17.15:12	Reserved	Reserved field.	Read Only	0000
17.11:8	mr_rstfsm_lsm_force	In HSSTLP IP loopback, corresponding loopback signals 17.8 corresponds to HSSTLP IP Lane0 17.9 corresponds to HSSTLP IP Lane1 17.10 corresponds to HSSTLP IP Lane2 17.11 corresponds to HSSTLP IP Lane3	Read/Write	0000
17.7:4	mr_rstfsm_cdr_force[20]	17.4 corresponds to HSSTLP IP Lane0 17.5 corresponds to HSSTLP IP Lane1 17.6 corresponds to HSSTLP IP Lane2 17.7 corresponds to HSSTLP IP Lane3	Read/Write	0000
17.3:0	mr_rstfsm_los_force[21]	17.0 corresponds to HSSTLP IP Lane0 17.1 corresponds to HSSTLP IP Lane1 17.2 corresponds to HSSTLP IP Lane2 17.3 corresponds to HSSTLP IP Lane3	Read/Write	1111

20 For PCS near-end parallel loopback and PMA near-end parallel loopback, configure the corresponding Bit for the Lane in use by the current SGMII Core as 1'b1.

21 For PCS near-end parallel loopback and PMA near-end parallel loopback, configure the corresponding Bit for the Lane in use by the current SGMII Core as 1'b0.

2.6.1.2 Auto-Negotiation Disabled

Table 2-21 Definition of Registers when SGMII Mode Auto-Negotiation is Disabled

Address	Register[22]	Description
0	SGMII Control (Register 0)	Parameters for Configuring SGMII Module Functionality
1	SGMII Status Register (Register 1)	SGMII Module Status Parameters
2	PHY Identifier Register (Register 2 and 3)	PHY ID
3	PHY Identifier Register (Register 2 and 3)	PHY ID
15	Extended Status Register (Register 15)	Extended Status Register
16	Vender_spc Register (Register 16)	Buffer Control Register
17	Vender_spc_1 Register (Register 17)	Loopback Control Register

2.6.2 Register Access

QSGMII IP provides two types of register configuration management interfaces — APB and MDIO interfaces. The MDIO interface can be enabled/disabled via the MDIO_Enable option. For detailed information, please refer to "2.3.1.2 IP Parameter Configuration".

2.6.2.1 MDIO Interface Disable

If the MDIO interface is disabled, the QSGMII IP operates the registers of the HSSTLP IP and SGMII Core through the APB interface. In this case, the registers of HSSTLP IP can only be operated through the APB interface of SGMII Core0; the registers of each SGMII Core can be operated through their respective independent APB interfaces (for details on the interface signals, please refer to Table 2-9).

2.6.2.1.1 HSSTLP IP Register Access

When paddr[18] is 0, operate the HSSTLP IP registers.

- paddr[17:2] is the valid address for HSSTLP IP registers;
- prdata[7:0] and pwdata[7:0] are the valid data for the HSSTLP IP registers.

22 The field definitions for each register are the same as those in the corresponding registers in Table 2-10.

2.6.2.1.2 SGMII Core Register Access

When paddr[18] is 1, operate the read and write registers of the SGMII Core.

- paddr[6:2] is the valid address for SGMII Core registers;
- prdata[15:0] and pwdata[15:0] are the valid data for the SGMII Core registers;

2.6.2.2 MDIO Interface Enable

If the MDIO interface is enabled, the QSGMII IP operates the registers of HSSTLP IP through the APB interface of SGMII Core0 and operates the registers of the 4 SGMII Cores through 4 independent sets of MDIO interfaces.

2.6.2.2.1 HSSTLP IP Register Access

When the MDIO interface is enabled, the QSGMII IP operates the registers of the HSSTLP IP through the APB interface of SGMII Core0.

- The highest bit of the address paddr[18] is invalid;
- paddr[17:2] is the valid address for HSSTLP IP registers;
- prdata[7:0] and pwdata[7:0] are the valid data for the HSSTLP IP registers.

2.6.2.2.2 SGMII Core Register Access

When the MDIO interface is enabled, the QSGMII IP operates the registers of the 4 SGMII Cores through 4 independent sets of MDIO interfaces (for details on the interface signals, please refer to Table 2-9).

2.7 Typical Applications

For typical applications of QSGMII IP, please refer to "2.4 Example Design".

2.8 Descriptions and Considerations

2.8.1 Clock Constraints

In the generated Example Design project constraint file ipsxd_qsgmii_onboard.fdc, the output clock of HSSTLP IP has been constrained to the global clock. Taking the Example Design project as an example:

```
define_attribute {t:U_ipsxd_qsgmii_dut.U_inst1111.U_hsstlp_ch0.o_p_clk2core_tx_0} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}
define_attribute {t:U_ipsxd_qsgmii_dut.U_inst1111.U_hsstlp_ch0.o_p_clk2core_rx_0} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}
```

2.8.2 HSSTLP Physical Location Constraints

In the generated Example Design project constraint file ipsxd_qsgmii_onboard.fdc, physical constraints have been applied to the SerDes channels of HSSTLP IP and the positions of reference clock inputs. Taking Example Design as an example:

```
define_attribute {i:U_ipsxd_qsgmii_dut.U_inst1111.U_hsstlp_ch0.U_GTP_HSSTLP_WRAPPER.CHANNEL0_ENABLE.U_GTP_HSSTLP_LANE0} {PAP_LOC} {HSSTLP_364_918:U0_HSSTLP_LANE}
define_attribute {i:U_ipsxd_qsgmii_dut.U_inst1111.U_hsstlp_ch0.U_GTP_HSSTLP_WRAPPER.PLL0_ENABLE.U_GTP_HSSTLP_PLL0} {PAP_LOC} {HSSTLP_364_918:U0_HSSTLP_PLL}
```

```
define_attribute {p:P_REFCKN} {PAP_IO_DIRECTION} {INPUT}
define_attribute {p:P_REFCKN} {PAP_IO_LOC} {E13}
define_attribute {p:P_REFCKN} {PAP_IO_VCCIO} {3.3}
define_attribute {p:P_REFCKN} {PAP_IO_STANDARD} {LVCMOS33}
define_attribute {p:P_REFCKN} {PAP_IO_UNUSED} {TRUE}
define_attribute {p:P_REFCKP} {PAP_IO_DIRECTION} {INPUT}
define_attribute {p:P_REFCKP} {PAP_IO_LOC} {F13}
define_attribute {p:P_REFCKP} {PAP_IO_VCCIO} {3.3}
define_attribute {p:P_REFCKP} {PAP_IO_STANDARD} {LVCMOS33}
define_attribute {p:P_REFCKP} {PAP_IO_UNUSED} {TRUE}
```

Users can modify the constraints according to the actual situation of the single board to meet practical usage requirements.

2.8.3 Operating Modes

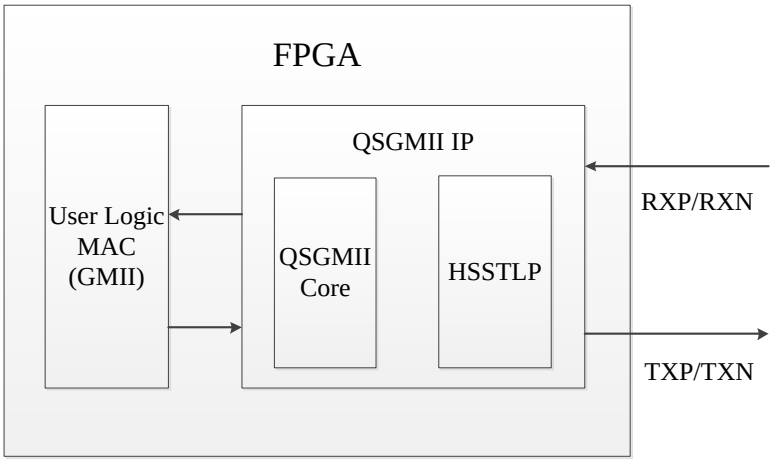

Figure 2-21 QSGMII IP Operating Mode Diagram

2.8.4 Loopback Mode

QSGMII IP supports five types of loopback modes. The data stream during loopback is shown in Figure 2-1:

- SGMII Core Loopback
- PMA Near-End Parallel Loopback
- PMA Near-End Serial Loopback
- PCS near-end parallel loopback
- PCS far-end parallel loopback

2.8.4.1 SGMII Core Loopback

This loopback mode supports two types of configuration: port configuration and register configuration.

Attention:

SGMII Core Loopback is not available when the "No Buffer" option is selected, and the loopback is independent for each SGMII Core.

Table 2-22 SGMII Core Loopback Port Configuration

Configuration Item	Configuration Descriptions
Port enable	When p*_pin_cfg_en=1, port configuration is enabled.
Loopback configuration	p*_loopback=1.
Non-Loopback configuration	p*_loopback=0.

Table 2-23 SGMII Core Loopback Register Configuration

Configuration Item	Configuration Descriptions
Register enable	When p*_pin_cfg_en=0, register configuration is enabled.
Loopback configuration	reg0.14 Loopback == 1'b1.
Non-Loopback configuration	reg0.14 Loopback == 1'b0.

2.8.4.2 PMA Near-End Parallel Loopback

Attention:

PMA near-end parallel loopback mode requires the corresponding register values to be set correctly before enabling the loopback port.

Table 2-24 PMA Near-End Parallel Loopback

Configuration Item	Configuration Descriptions

Register Configuration	reg17.0 mr_rstfsm_los_force == 1'b0;
	reg17.4 mr_rstfsm_cdr_force == 1'b1;
	Following the above configuration, the SGMII register reg17 Vendor_spc_1 is set to 0x0010.
	(For a detailed introduction to PMA Near-End Parallel Loopback, please refer to *"**UG040008_Logos2 Family FPGA High-Speed Serial Transceiver (HSSTLP) User Guide**"* and *"**UG041004_HSSTLP_IP**"*)

Port Configuration	When pma_nearend_ploop=1, PMA near-end parallel loopback is enabled.

2.8.4.3 PMA Near-End Serial Loopback

Attention:

PMA near-end serial loopback mode requires the corresponding register values to be set correctly before enabling the loopback port.

Table 2-25 PMA Near-End Serial Loopback

Configuration Item	Configuration Descriptions
Register Configuration	reg17.0 mr_rstfsm_los_force == 1'b1; Following the above configuration, the SGMII register reg17 Vendor_spc_1 is set to 0x0001. (For a detailed introduction to PMA Near-End Serial Loopback, please refer to *"**UG040008_Logos2 Family FPGA High-Speed Serial Transceiver (HSSTLP) User Guide**"* and *"**UG041004_HSSTLP_IP**"*)
Port Configuration	When pma_nearend_sloop=1, PMA near-end serial loopback is enabled.

2.8.4.4 PCS near-end parallel loopback

Attention:

PCS near-end parallel loopback mode requires the corresponding register values to be set correctly before enabling the loopback port.

Table 2-26 PCS Near-End Parallel Loopback

Configuration Item	Configuration Descriptions

Register Configuration	reg17.0 mr_rstfsm_los_force == 1'b0;
	reg17.4 mr_rstfsm_cdr_force == 1'b1;
	Following the completion of the above configuration, the SGMII register reg17 Vendor_spc_1 is set to 0x0010.
	(For a detailed introduction to PCS Near-End Parallel Loopback, please refer to *"**UG040008_Logos2 Family FPGA High-Speed Serial Transceiver (HSSTLP) User Guide**"* and *"**UG041004_HSSTLP_IP**"*)

Port Configuration	When pcs_nearend_loop=1, PCS near-end parallel loopback is enabled.

2.8.4.5 PCS far-end parallel loopback

Attention:

PCS far-end loopback mode first requires ensuring the corresponding register values are set correctly, then enabling the loopback port.

Under this loopback mode, if the value of HSSTLP IP register 0x824 is not configured to 0x4, the clocks at both ends of the link must share the same source.

Table 2-27 PCS Far-End Parallel Loopback

Configuration Item	Configuration Descriptions
Register Configuration	reg17.0 mr_rstfsm_los_force == 1'b1; After the configuration is complete, SGMII register reg17 Vender_spc_1 == 0x0001; Configure HSSTLP IP registers: Offset 0x824.2 PMA_REG_PLPBK_TXPCLK_EN ==1; Offset 0x00c.4:3 PCS_RX_CLK_SEL==2'b01; After configuration, the HSSTLP IP register 0x824 is set to 0x4; After configuration, the HSSTLP IP register 0x00c is set to 0x8. (For a detailed introduction to PCS far-end parallel loopback, please refer to ***"UG040008_Logos2 Family FPGA High-Speed Serial Transceiver (HSSTLP) User Guide"*** and ***"UG041004_HSSTLP_IP"***)
Port Configuration	When pcs_farend_loop=1, PCS far-end parallel loopback is enabled.

2.8.5 IP Clock Scheme

2.8.5.1 Clock Scheme with Frequency Offset Buffer Enabled

This clock scheme is applicable when the frequency offset Buffer is enabled for QSGMII IP (i.e., the "No_Buffer" option is cleared).

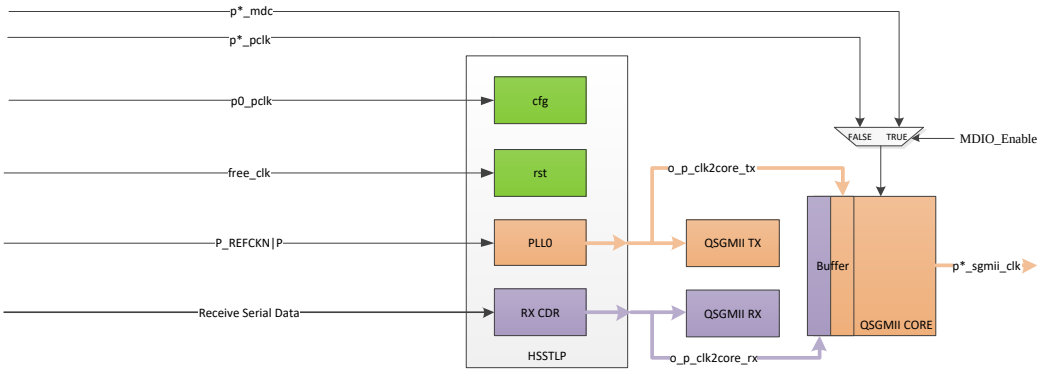

Figure 2-22 Diagram of Clock Scheme with Frequency Offset Buffer Enabled

2.8.5.1.1 Data Path Clock

- In the transmit direction, a pair of 125MHz differential input clocks is used to provide a clock source for the HSSTLP IP. After passing through PLL0 in the HSSTLP IP, it provides the transmit clock o_p_clk2core_tx for QSGMII TX and QSGMII Core.
- In the receive direction, RX_CDR within the HSSTLP IP recovers the clock from the serial differential data, providing the capture clock o_p_clk2core_rx for QSGMII RX and QSGMII Core.
- Through the elasticity Buffer in QSGMII Core, the clock domains are aligned to o_p_clk2core_tx, ultimately generating the clock p*_sgmii_clk provided to the GMII side.

2.8.5.1.2 Free Run Clock

- free_clk is a clock independent of the data path clock, providing a clock for the HSSTLP IP reset sequence, with a frequency of 50MHz in this scheme.

2.8.5.1.3 Configuration clock

- p*_mdc — The MDIO interface clock, 2.5MHz. When the MDIO_Enable parameter is selected, it provides the clock for QSGMII Core configuration logic. The 4 MDIO interface clocks at this location operate independently.
- p*_pclk — The APB interface clock, 50MHz~100MHz. p0_pclk provides the clock for HSSTLP IP configuration logic. When the "MDIO_Enable" option is cleared, it provides the clock for QSGMII Core configuration logic.

2.8.5.2 Clock Scheme with Frequency Offset Buffer Disabled

This clock scheme is applicable when the frequency offset Buffer is disabled (i.e., the "No_Buffer" option is selected).

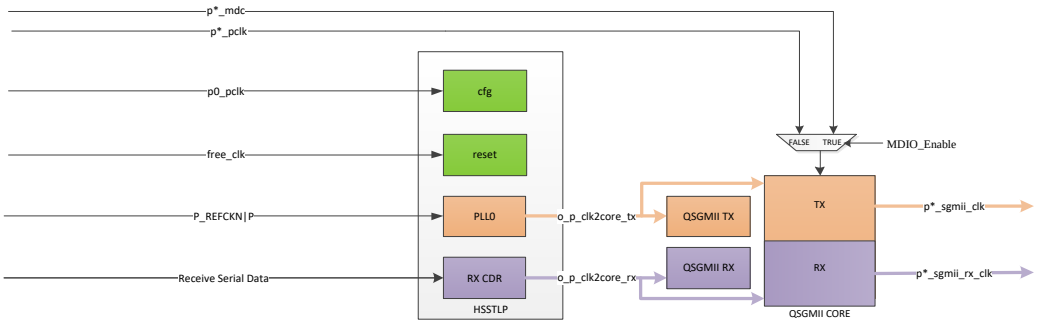

Figure 2-23 Diagram of Clock Scheme with Frequency Offset Buffer Disabled

2.8.5.2.1 Data Path Clock

- In the TX direction, a pair of 125MHz differential input clocks is used to provide a clock source for the HSSTLP IP. After passing through PLL0 in the HSSTLP IP, it provides the transmit clock o_p_clk2core_tx for QSGMII Core, ultimately generating the clock p*_sgmii_clk for the TX direction at the GMII side.
- In the RX direction, the RX_CDR in HSSTLP IP recovers the clock from the serial differential data, providing the capture clock o_p_clk2core_rx for QSGMII Core, and ultimately generating the clock p*_sgmii_rx_clk for the GMII receive side.

2.8.5.2.2 Free Run Clock

- free_clk is a clock independent of the data path clock, providing a clock for the HSSTLP IP reset sequence, with a frequency of 50MHz in this scheme.

2.8.5.2.3 Configuration clock

- p*_mdc — The MDIO interface clock, 2.5MHz. When the MDIO_Enable parameter is selected, it provides the clock for QSGMII Core configuration logic. The 4 MDIO interface clocks at this location operate independently.

- p*_pclk — The APB interface clock, 50MHz~100MHz. p0_pclk provides the clock for HSSTLP IP configuration logic. When the "MDIO_Enable" option is cleared, it provides the clock for QSGMII Core configuration logic. The 4 APB interface clocks at this location operate independently.

2.8.6 Example of read and write operations for the uart_ctrl_top module

2.8.6.1.1 Read Operation

To read data from address 0x00000001, the read operation format is "0x72"+"0x00000001", which is 0x0000000172.

2.8.6.1.2 Write Operation

To write data 0x02 to address 0x00000001, the write operation format is "0x77"+"0x00000001"+"0x00000002", which is 0x770000000100000002.

2.8.7 IP Invocation Method

Users can directly add the IP by adding the idf of the QSGMII IP generated by the IPC instantiation through PDS.

2.9 IP Debugging Method

In the Example Design, DebugCore and LED can monitor the link status of QSGMII IP. For the DebugCore signal list and LED indicator list, please refer to "2.4.3 Descriptions of Ports" and "2.4.4 Test Method".

In the Example Design, the UART can read the values of the status registers in the IP to monitor the link status. For the use of the UART module, please refer to "2.4.2.1 uart_ctrl_top".

Disclaimer

Copyright Notice

Disclaimer

1. This document only provides information in stages and may be updated at any time based on the actual situation of the products without further notice. The Company assumes no legal responsibility for any direct or indirect losses caused by improper use of this document.
2. This document is provided "as is" without any warranties, including but not limited to warranties of merchantability, fitness for a particular purpose, non-infringement, or any other warranties mentioned in proposals, specifications, or samples. This document does not grant any explicit or implied intellectual property usage license, whether by estoppel or otherwise.
3. The Company reserves the right to modify any documents related to its family's products at any time without prior notice.