pg2l_lvds8to1_and_4to1 Application Guide

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Shenzhen Pango Microsystems Co., Ltd.

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.2	31.03.2022	Initial release.

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Chapter 1 Overview

1.1 Introduction

This document is an application document for FPGA products LVDS8:1 and LVDS4:1 launched by Shenzhen Pango Microsystems Co., Ltd. This document mainly introduces the function list, design architecture, interface definitions, interface timing, supported devices, and reference design of LVDS4to1 and LVDS8to1.

1.2 Main Functions

- The main functions supported include:
- Double-edge transmit and receive (LVDS8:1);
- Double-edge transmit and receive (LVDS4:1);
- Automatic and manual alignment;
- Line rate of 1250 Mbps;
- Each clock group supports 16 pairs of data

1.3 Design Information

Table 1-1 Design Information

LVDS8TO1_AND_LVDS4TO1	
Supported Devices	Logos2 family FPGA products
Supported User Interface	Custom
Provided Design Files	
Design File	Verilog files
Reference Designs	Verilog files
Simulation File	Verilog files
Constraint File	fdc file
Development Tools	
Design Tools	PDS Development Suite PDS_2022.2-sp6.8-PG2L50H-Beta1-ads version

1.4 Resource Usage

Table 1-2 Resource Usage Rate

Project Type	Device	DRM	FF	LUT	PLL
LVDS8:1 8-channel, enables auto training	PG2L50H	0	2181	1781	1
LVDS4:1 8-channel, enables auto training	PG2L50H	0	1762	1523	1

Chapter 2 Function Description

LVDS8TO1/LVDS4TO1 mainly includes transmit and receive modules. The transmit module transmits LVDS and implements parallel-to-serial conversion. The receive module receives data compliant with LVDS level standards and implements serial-to-parallel conversion and byte alignment. SOC, LVDS display, etc. can serve as the receive device, while a camera, SOC, etc. can serve as the transmit device.

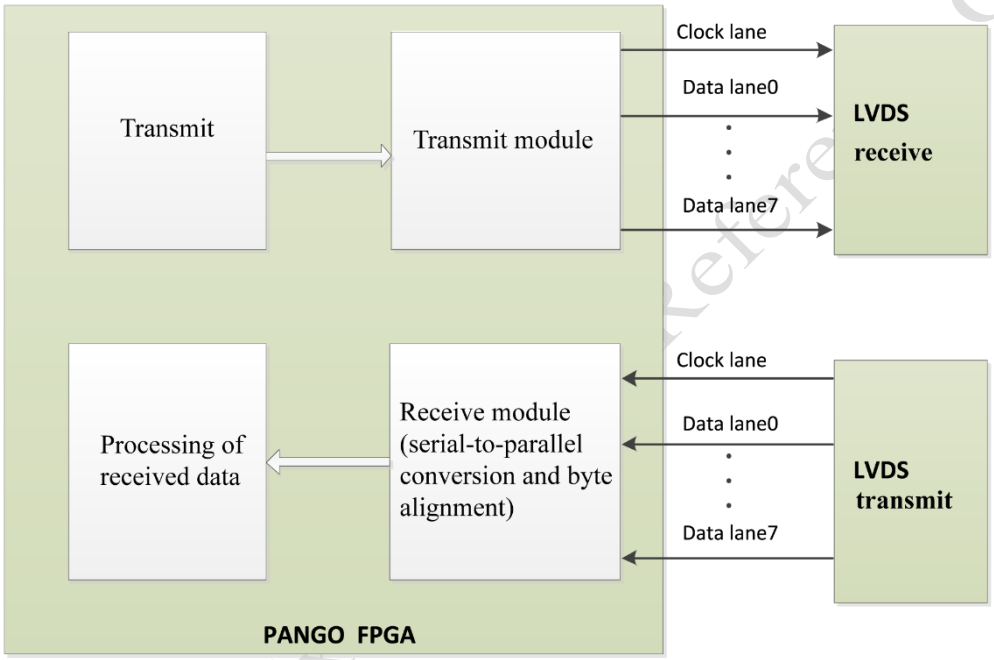

Figure 2-1 LVDS8TO1/LVDS4TO1 Application Introduction

2.1 Clock Module Design

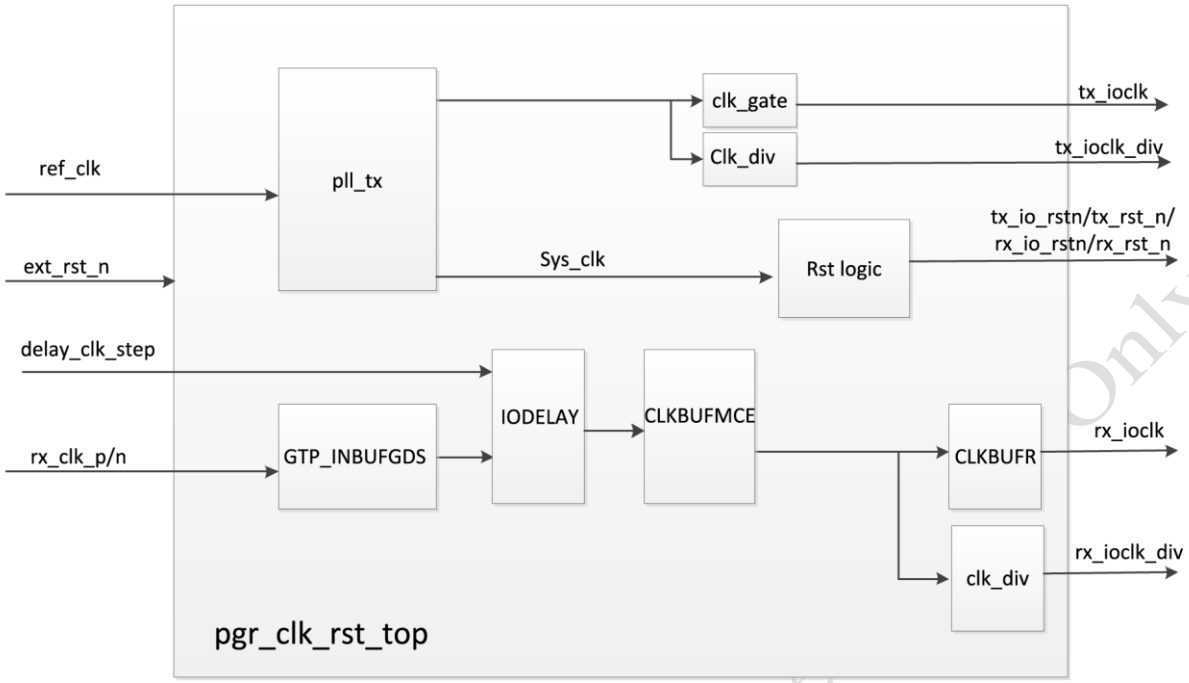

Figure 2-2 Clock Architecture Block Diagram

The pgr_clk_rst_top module mainly provides system clocks and reset signals. The high-speed transmit clock is generated by the local crystal oscillator through PLL frequency multiplication. The high-speed receive clock, after being converted from differential to single-ended via the internal INBUFGDS, enters IODELAY and then the regional clock. The parallel receive clock is generated from the high-speed clock through the division unit.

Note: Connect the differential receive clock to the GMCLK clock pin, and use the gate function of the PLL output on the transmitter.

2.2 Transmit Module Design

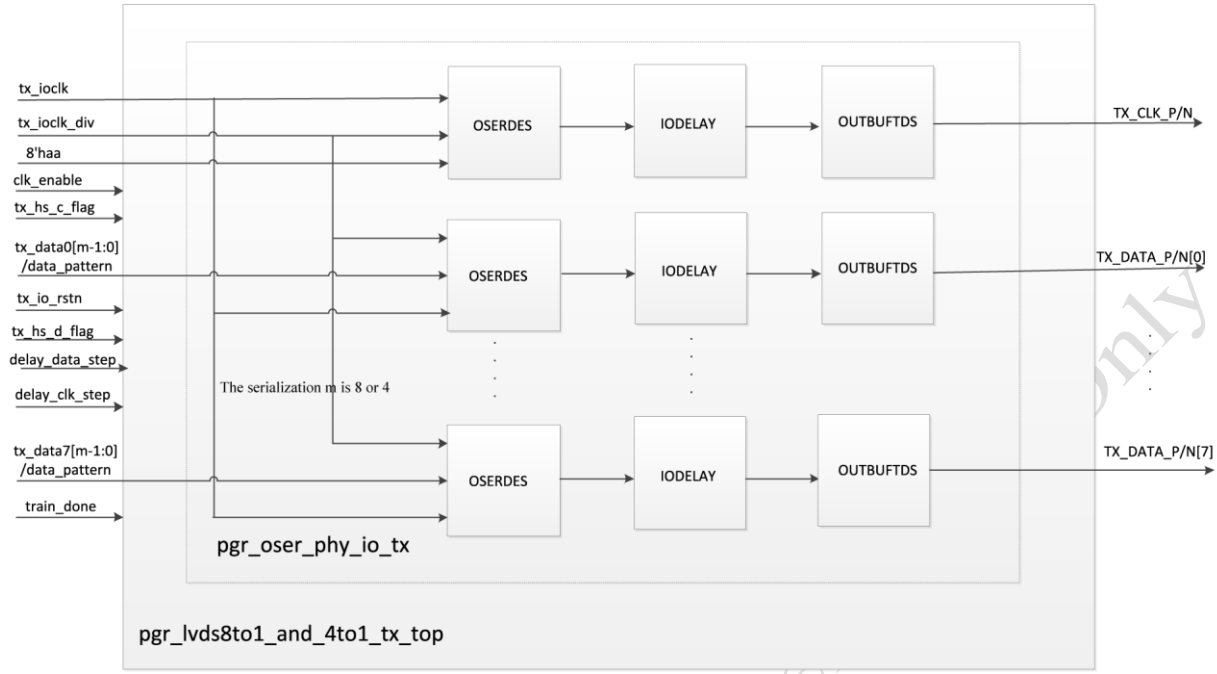

Figure 2-3 Transmit Function Block Diagram

The lvds8to1 / 4to1_tx_top module implements parallel-to-serial data conversion and supports independent delay adjustment for clock and data channels.

Transmitted parallel data achieve parallel-to-serial conversion through OSERDES and delay adjustment through IODELAY. OUTBUFTDS outputs the serial data in the differential form.

2.3 Receive Module Design

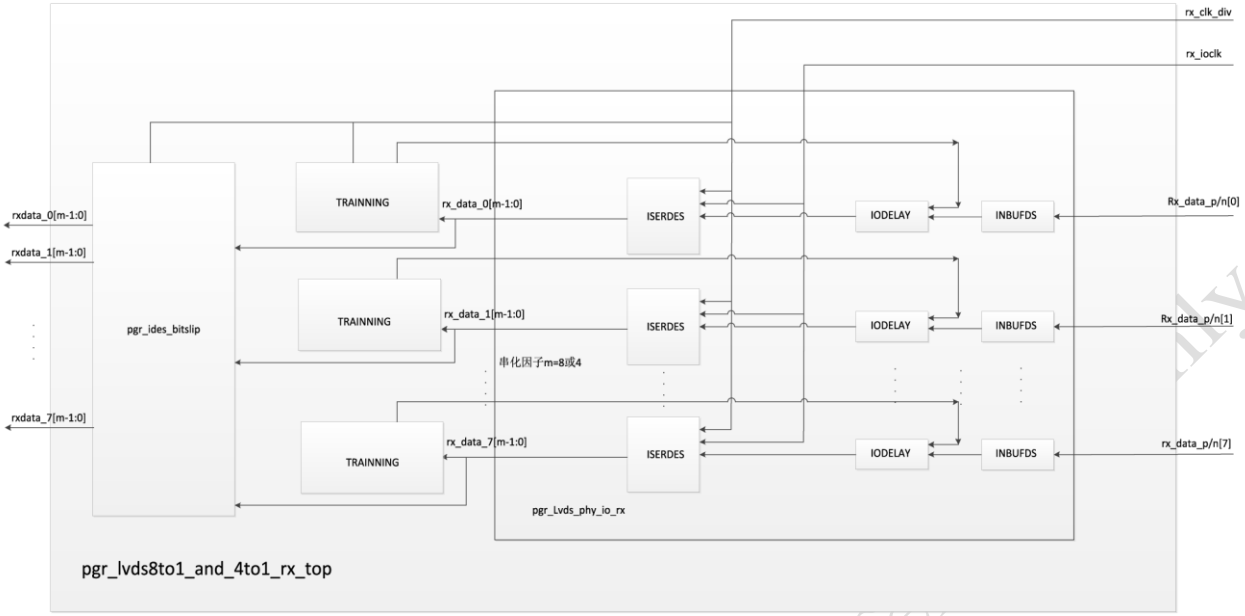

Figure 2-4 Receive Function Block Diagram

The pgr_lvds8to1 / 4to1_rx_top module implements serial-to-parallel data conversion and byte alignment. The differential data signal is converted to a single-end signal by the INBUFDS unit, then passes through the IODELAY unit and enters ISERDES. Use the TRAINING module to adjust the iodelay value of each data channel to obtain their optimal sampling windows. After the training is completed, use the bitslip module to shift bits of the ISERDES module for byte alignment.

2.4 List of Interfaces

Table 2-1 List of Clock Module Interfaces

Signal Name	Input / Output	Bit width	Description
Global signals			
ref_clk	Input	1	System clock signal, 50MHz
ext_rst_n	Input	1	System reset signal, active-low
rx_clk_p	Input	1	Differential clock input, P side, connected to p side of pin GMCLK
rx_clk_n	Input	1	Differential clock input, n side, connected to pin GMCLK of port N
delay_clk_step	Input	8	Input clock channel iodelay, 0–247 steps, each step is about10ps
tx_ioclk	Output	1	High-speed clock of output channel, used for driving OSERDES
tx_ioclk_div	Output	1	Division clock for the high-speed clock of output channel

Signal Name	Input / Output	Bit width	Description
tx_io_rstn	Output	1	IOL reset signal of output channel, active-low
tx_rstn	Output	1	Logic reset signal of transmit module, active-low
rx_ioclk	Output	1	High-speed clock of input channel, used for driving ISERDES
rx_ioclk_div	Output	1	Division clock for the high-speed clock of input channel
rx_io_rstn	Output	1	IOL reset signal of input channel, active-low
rx_rstn	Output	1	Logic reset signal of receive module, active-low

Table 2-2 List of Transmit Module Interfaces

Signal Name	Input / Output	Bit width	Description
Global signals			
tx_ioclk	Input	1	High-speed clock of output channel, used for driving OSERDES
tx_ioclk_div	Input	1	Division clock for the high-speed clock of output channel
clk_enable	Input	1	Clock channel data enable signal, active-high
tx_io_rstn	Input	1	IOL reset signal of output channel, active-low
tx_rstn	Input	1	Logic reset signal of output channel, active-low
train_done	Input	1	Transmitter sends the user data enable signal; Sends user data at a high level; Sends fixed data PATTERN (4'h9/8'h2c) at a low level.
tx_hs_c_flag	Input	1	Output clock channel high-speed mode enable, 1: High-speed mode enabled 0: High-impedance
tx_hs_d_flag	Input	1	Output data channel high-speed mode enable, 1: High-speed mode enabled 0: High-impedance
delay_data_step	Input	8*CHANNEL	IODELAY value of the output data channel. Each channel is independently adjustable and uses 8 bits. 0–127 for each channel, each step delay is 5ps, and the inherent delay of the IODELAY device is about 0.6ns.
delay_clk_step	Input	8	IODELAY value of the output clock channel, adjustable within 0–127, each step delay is 5ps, and the inherent delay of the IODELAY device is about 0.6ns.
tx_data	Input	CHANNEL*DATA_WIDTH	Transmits parallel high-speed user data, transmits tx_data when train_done is high, and transmits PATTERN (4'h9/8'h2c) when train_done is low.
tx_data_p	Output	CHANNEL	High-speed data port of output channel, p side
tx_data_n	Output	CHANNEL	High-speed data port of output channel, n side
tx_clk_p	Output	1	High-speed clock port of output channel, p side
tx_clk_n	Output	1	High-speed clock port of output channel, n side

Table 2-3 List of Interfaces of the Receive Top-level Module

Signal Name	Input / Output	Bit width	Description
Global signals			
dly_key_n	Input	1	Debugging button, reserved
rx_io_rstn	Input	1	IOL reset signal of input channel, active-low
rx_ioclk	Input	1	High-speed clock of input channel
rx_ioclk_div	Input	1	Division clock for the high-speed clock of input channel
rx_data_p	Input	CHANNEL	High-speed data port of input channel, p side
rx_data_n	Input	CHANNEL	High-speed data port of input channel, n side
rx_hs_data	Output	CHANNEL*DATA_WIDTH	Desterilized and byte-aligned parallel data
sync_done	Output	1	Reserved
rx_train_done	Output	1	Byte alignment complete flag signal: High indicates that bytes are aligned, low indicates that bytes are not aligned

2.5 Parameter Definitions

Table 2-4 Definitions of Top-level Parameters

Parameter	Description
CHANNEL	Number of channels, with a optional range of 1–16 Default value = 8;
DES_MODE	Serialisation ratio mode: "DES4": The serialisation ratio is 1:4; "DES8": The serialization ratio is 1:8; Default value = "DES8".
AUTO_TRAINING	Auto training enable, with “TRUE” and “FALSE” optional When it is "TRUE": Auto training is enabled, the fixed PATTERN is used for verification, each data channel is automatically scanned for the maximum continuous correct window, and the middle value of the window is used as the optimal data sampling window value. If the scanned values of step 50–100 are all correct IODELAY values, then set the IODELAY value of that data channel to 75. When it is "FALSE": Manually adjust the IODELAY value of the clock channel or data channel to obtain the correct sampling window. Default value = "TRUE".
DELAY_D_VALUE	The static delay value of the data receive channel, effective when AUTO_TRAINING is "FALSE"; Each data channel is independently adjustable, with a value range of 0–247, and each step is approximately 10ps. Default value = {CHANNEL{8'h30}};

2.6 Interface Timing

The reset timing of the receive module: First release rx_io_rstn (ISERDES reset), then release rx_gate_rstn (high-speed serial clock and division clock reset), to ensure all ISERDES work simultaneously. Finally, release rx_rstn(logic reset). The reset timing of the transmit module is similar: First, release OSERDES reset, then release the clock reset, and finally release the logic reset.

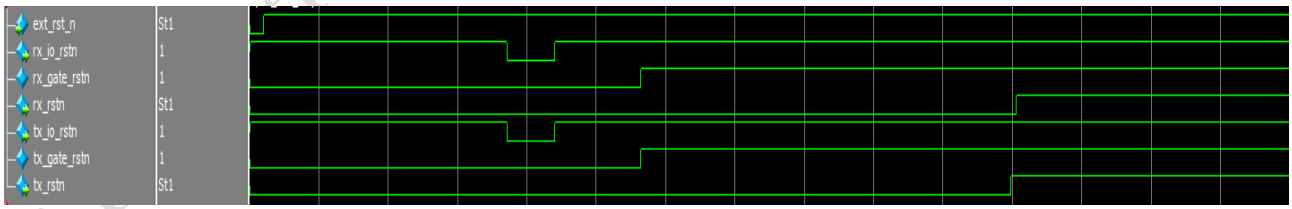

Figure 2-5 Typical Reset Timing

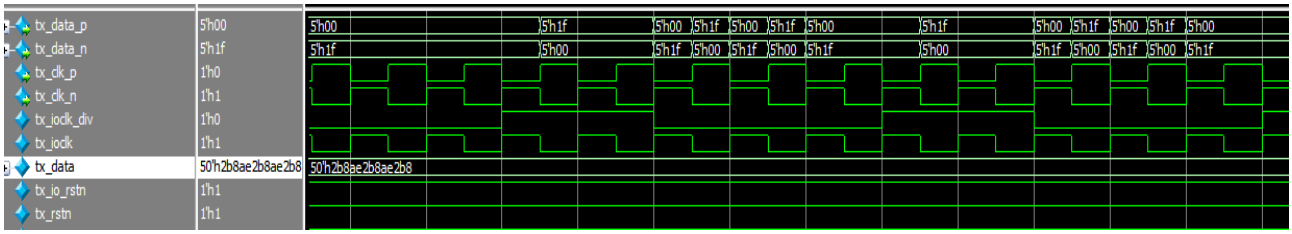

Figure 2-6 Typical Transmit Timing

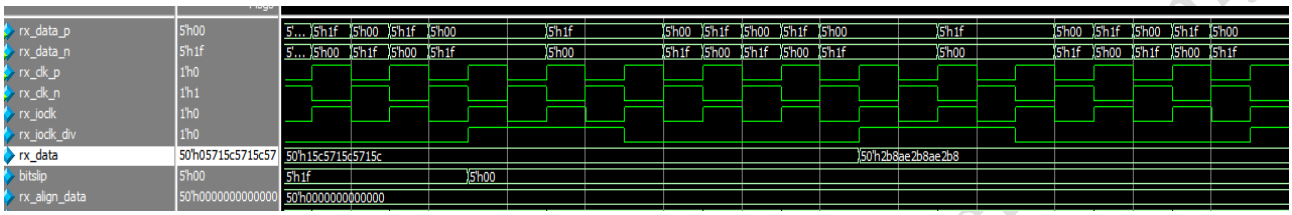

Figure 2-7 Typical Receive Timing

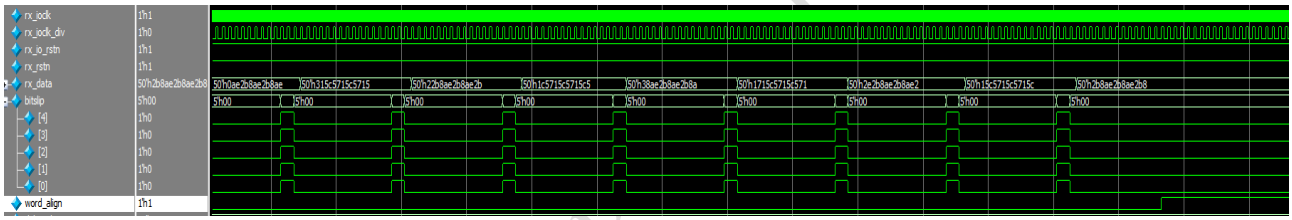

Figure 2-8 Typical Bitslip Timing

Chapter 3 Reference Design

3.1 Reference Function Design

To simplify the verification environment for the reference design, PG2L50H is used simultaneously as both the transmitter and receiver, which are connected with an SMA cable. The design function block diagram is shown in Figure 3-1.

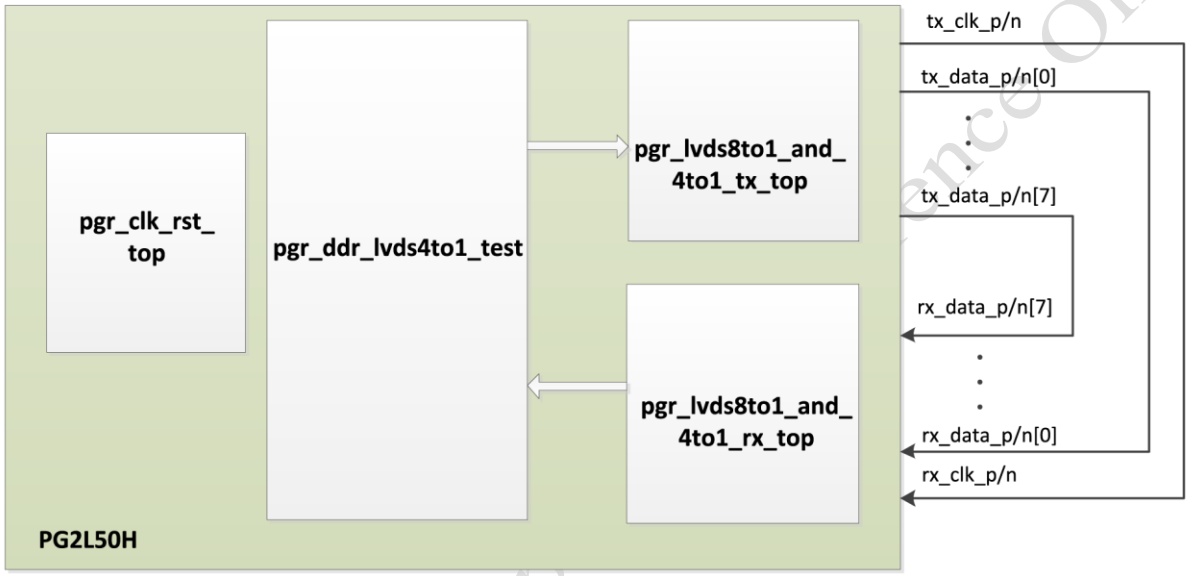

Figure 3-1 Reference Design Function Block Diagram

pgr_clk_rst_top module: generates the clock and reset signals required by the system.

pgr_ddr_lvds4to1_test module: generates parallel high-speed transmission data and verifies the correctness of the received data.

pgr_lvds8to1_and_4to1_tx_top module: serves as the data transmit module and implements data parallel-to-serial conversion.

Pgr_lvds8to1_and_4to1_rx_top module: implements data serial-to-parallel conversion and byte alignment.

3.2 Reference Design Interface List

Table 3-1 Reference Design Interface List

Signal Name	I/O	Bit width	Description
Global signals			
ref_clk	I	1	System clock signal, 50MHz
ext_rst_n	I	1	System reset signal, active-low
dly_key_n	I	1	Debugging button, reserved
tx_mode	I	2	Test data mode selection signal, selected via a DIP switch 2'b00: pattern (4'h9/ 8'h2c) 2'b01: fixed number (4'ha/ 8'h3a) 2'b10: counter (incremental number) 2'b11: prbs (pseudo-random number)
err_flag	O	1	Bit error indicator: High indicates a bit error
train_done_led	O	1	Test signal: A low level indicates alignment of received bytes
High-speed serial interfaces			
tx_data_p	O	8	Transmitter high-speed data port, p side;
tx_data_n	O	8	Transmitter high-speed data port, n side;
tx_clk_p	O	1	Transmitter high-speed clock port, p side;
tx_clk_n	O	1	Transmitter high-speed clock port, n side;
rx_data_p	I	8	Receiver high-speed data port, p side;
rx_data_n	I	8	Receiver high-speed data port, n side;
rx_clk_p	I	1	Receiver high-speed clock port, p side;
rx_clk_n	I	1	Receiver high-speed clock port, n side;

3.3 Reference Design File Directory

pgr_pg2l_lvds8to1_and_4to1_eval Design Example Directory Structure Diagram:

```
pgr_pg2l_lvds8to1_and_4to1_eval
|
├─bench                  // Example simulation test bench
├─docs                   // Design document
├─ip                     // Relevant IP called by the design
├─pnr                    // Example project directory
|  ├─ipcore              // IP CORE files generated by PDS
|  |  └─pll_tx           // PLL IP CORE used in the example
|  ├─P04I50RD02_A1.fdc   // Example project constraint reference files
|  ├─top_inserter.fic    // Debug Core debugging files
|  └─project.pds         // PDS project file
├─simulation             // Simulation project directory
|  ├─file_list.f         // Design file list
|  ├─sim.bat             // Simulation scripts
|  ├─sim.tcl             // Simulation TCL scripts
|  └─wave.do             // Simulation waveform scripts
├─src                    // RTL files included in the design example
```

Figure 3-2 File Directory

3.4 Reference Design Simulation

Run the sim.bat script in the reference design file directory, or run the sim.tcl script in the simulation software to start the simulation. The simulation waveform is shown in Figure 3-3.

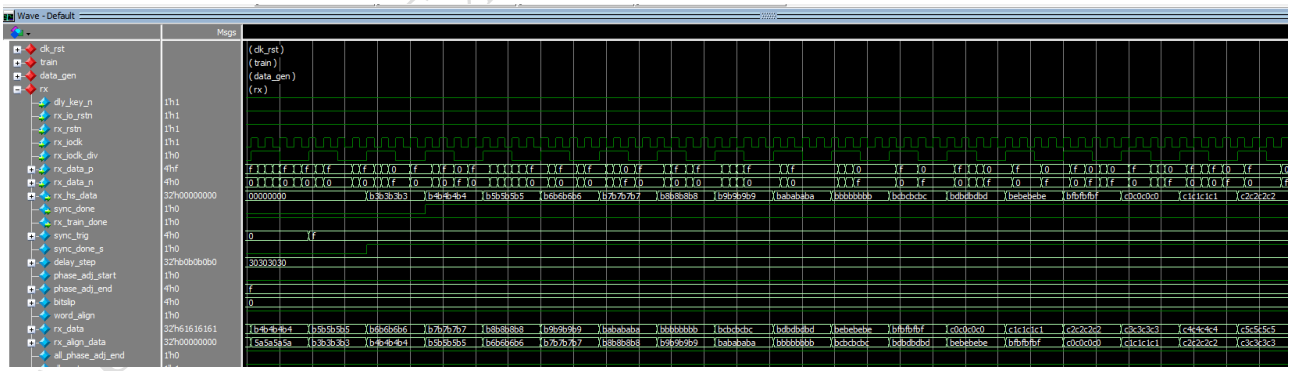

Figure 3-3 Simulation Waveform

3.5 Reference Design On-board Verification

The on-board verification environment is shown in Figure 3-4. The P04I50RD02_A0 board is used for self-transmission and reception tests. The voltages of BANK R4 and BANK L3 are adjusted to 2.5V

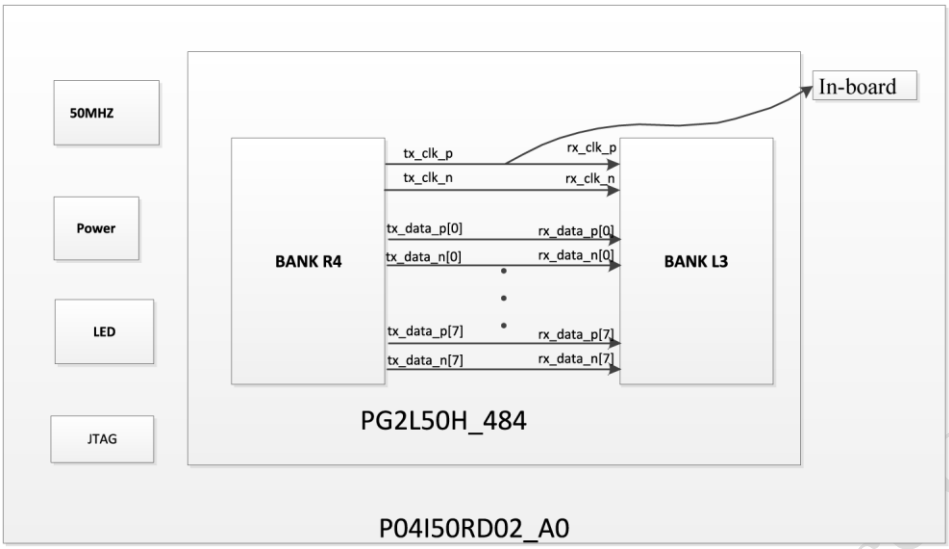

Figure 3-4 Reference Design On-board Environment

On-board precautions:

1. Connect the receiver to an external termination resistor of 100ohm, or enable the termination resistor in the UCE interface.
2. The receiver can sample the data correctly only after obtaining the correct IODELAY value. Enable auto training, or manually scan the correct data channel for the IODELAY value and set the parameter DELAY-D-VALUE.
3. For the reset timing of the receive module, release the IOL reset and then the high-speed serial clock reset, otherwise receive channel misalignment may occur.
4. For the reset timing of the transmit module. Release the IOL reset and then the high-speed serial clock reset, otherwise transmit channel misalignment may occur.
5. To use the transmitter, enable the termination resistor in the UCE interface.

Connect the 12V DC power supply, set the lower 2 bits of DIP switch SW9 to 2'b10 (incremental number mode), set top-level parameter DES_MODE to "DES4", set the project to LVDS4:1 mode, program the bitstream, and use the debugcore tool to capture the waveform. As shown in Figure 3-5, the correct incremental number is captured by the receiver.

When the top-level parameter AUTO_TRAINING is set to "TRUE", the data sampling window is scanned automatically. Users can use debugcore to capture the optimal delay chain window delay_step, and fill the value of delay_step into parameter DELAY_D_VALUE. Then set the parameter AUTO_TRAINING to "FALSE" to use static sampling, which can save resources.

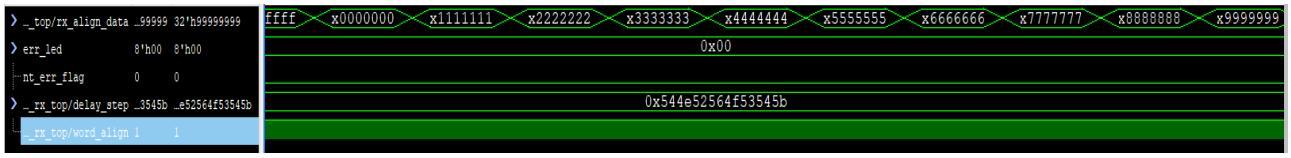

Figure 3-5 LVDS4:1 On-board Verification Waveform

To verify the transmission and reception of LVDS8:1, set top-level parameter DES_MODE to "DES8"Select the data to be captured in the fic file, and generate the bitstream for programming. The captured waveform is shown in Figure 3-6.

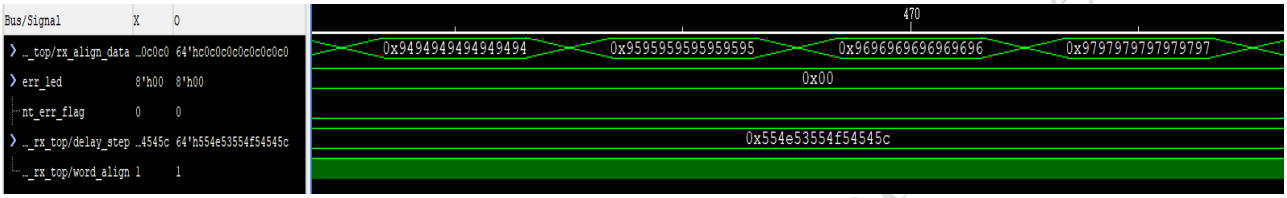

Figure 3-6 LVDS8:1 On-board Verification Waveform

	I/O NAME	I/O DIRECTION	LOC	BANK	VCCIO	IOSTANDARD	DRIVE	DIFF_IN_TERM_MODE
40	ext_rst_n	INPUT	K21	BANKL4	2.5	LVCMOS25		
41	ref_clk	INPUT	J19	BANKL4	2.5	LVCMOS25		
42	rx_clk_n	INPUT	C19	BANKL3	2.5	LVDS25		OFF(default)
43	rx_clk_p	INPUT	C18	BANKL3	2.5	LVDS25		OFF(default)
24	rx_data_n[0]	INPUT	E17	BANKL3	2.5	LVDS25		OFF(default)
23	rx_data_n[1]	INPUT	G22	BANKL3	2.5	LVDS25		OFF(default)
22	rx_data_n[2]	INPUT	C15	BANKL3	2.5	LVDS25		OFF(default)
21	rx_data_n[3]	INPUT	D15	BANKL3	2.5	LVDS25		OFF(default)
20	rx_data_n[4]	INPUT	D16	BANKL3	2.5	LVDS25		OFF
19	rx_data_n[5]	INPUT	B16	BANKL3	2.5	LVDS25		OFF
18	rx_data_n[6]	INPUT	B13	BANKL3	2.5	LVDS25		OFF
17	rx_data_n[7]	INPUT	A16	BANKL3	2.5	LVDS25		OFF
32	rx_data_p[0]	INPUT	F16	BANKL3	2.5	LVDS25		OFF(default)
31	rx_data_p[1]	INPUT	G21	BANKL3	2.5	LVDS25		OFF(default)
30	rx_data_p[2]	INPUT	C14	BANKL3	2.5	LVDS25		OFF(default)
29	rx_data_p[3]	INPUT	D14	BANKL3	2.5	LVDS25		OFF(default)
28	rx_data_p[4]	INPUT	E16	BANKL3	2.5	LVDS25		OFF(default)
27	rx_data_p[5]	INPUT	B15	BANKL3	2.5	LVDS25		OFF(default)
26	rx_data_p[6]	INPUT	C13	BANKL3	2.5	LVDS25		OFF(default)
25	rx_data_p[7]	INPUT	A15	BANKL3	2.5	LVDS25		OFF(default)
36	train_done_led	OUTPUT	K17	BANKL4	2.5	LVCMOS25	4	
37	tx_clk_n	OUTPUT	D1	BANKR4	2.5	LVDS25	3.5	ON
38	tx_clk_p	OUTPUT	E1	BANKR4	2.5	LVDS25	3.5	ON
8	tx_data_n[0]	OUTPUT	P1	BANKR4	2.5	LVDS25	3.5	ON
7	tx_data_n[1]	OUTPUT	J1	BANKR4	2.5	LVDS25	3.5	ON
6	tx_data_n[2]	OUTPUT	L4	BANKR4	2.5	LVDS25	3.5	ON
5	tx_data_n[3]	OUTPUT	P4	BANKR4	2.5	LVDS25	3.5	ON
4	tx_data_n[4]	OUTPUT	N2	BANKR4	2.5	LVDS25	3.5	ON
3	tx_data_n[5]	OUTPUT	H5	BANKR4	2.5	LVDS25	3.5	ON
2	tx_data_n[6]	OUTPUT	M5	BANKR4	2.5	LVDS25	3.5	ON
1	tx_data_n[7]	OUTPUT	J4	BANKR4	2.5	LVDS25	3.5	ON
16	tx_data_p[0]	OUTPUT	R1	BANKR4	2.5	LVDS25	3.5	ON
15	tx_data_p[1]	OUTPUT	K1	BANKR4	2.5	LVDS25	3.5	ON
14	tx_data_p[2]	OUTPUT	L5	BANKR4	2.5	LVDS25	3.5	ON
13	tx_data_p[3]	OUTPUT	P5	BANKR4	2.5	LVDS25	3.5	ON
12	tx_data_p[4]	OUTPUT	P2	BANKR4	2.5	LVDS25	3.5	ON
11	tx_data_p[5]	OUTPUT	J5	BANKR4	2.5	LVDS25	3.5	ON
10	tx_data_p[6]	OUTPUT	M6	BANKR4	2.5	LVDS25	3.5	ON

Figure 3-7 UCE Constraints

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