Logos Family FPGAs High-Speed Serial Transceiver (HSST) User Guide

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.4	04.08.2022	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
HSST	High Speed Serial Transceiver
PCS	Physical Code Sublayer
PMA	Physical Media Attachment
XAUI	10 Gigabit Attachment Unit interface
CPRI	Common Public Radio Interface
SRIO	Serial Rapid IO
CTC	Clock Tolerance Compensation
PRBS	Pseudo-Random Binary Sequence
APB	Advanced Peripheral Bus
UI	Unit Internal
CDR	Clock Data Recovery
LEQ	Linear Equalizer
CTLE	Continuous Time Linear Equalizer
PCIE	Peripheral Component Interconnect Express
RX	Receiver
TX	Transmitter
CML	Current Mode Logic
PI	Phase Interpolator
OOB	Out of band

Related Documentation

The following documentation is related to this manual:

1. ***DS02001_Logos Family FPGAs Datasheet***

Table of Contents

Tables

Figures

Chapter 1 General Introduction to HSST

The Logos Family products have built-in high-speed serial interface module, i.e. HSST. In addition to the PMA, HSST also integrates a rich set of PCS functions, which can be flexibly applied to various serial protocol standards. Within the Logos Family products, each HSST supports 1 to 4 full-duplex transceiver LANEs, see pin locations at Appendix A: HSST Pin Location Description. The key features of HSST include:

- Supported line rates: Refer to the "AC Electrical Characteristics of the High-Speed Serial Transceiver HSST" section in the "***DS02001_Logos Family FPGAs Datasheet***".
- Flexible reference clock selection
- Configurable output swing and de-emphasis
- Adaptive equalizer at receiver side
- Data channels support following modes: 8bit only, 10bit only, 8B10B 8bit, 16bit only, 20bit only, 8B10B 16bit, 32bit only, 40bit only, 8B10B 32bit, 64B66B/64B67B 16bit, 64B66B/64B67B 32bit
- Flexibly configurable PCS
- Supports protocols such as PCI Express GEN1, PCI Express GEN2, XAUI, Gigabit Ethernet, CPRI, SRIO, etc.
- Flexible byte alignment function
- RX Clock Slip function to ensure a fixed receive delay supported
- Protocol standard 8B10B encoding/decoding supported
- Protocol standard 64B66B/64B67B data adaptation function supported
- Flexible CTC scheme
- x2 and x4 channel bonding
- HSST configuration supports dynamic modification
- Near-end loopback and far-end loopback
- Built-in PRBS Function

PGL50H contains 1 HSST with a total of 4 full-duplex transmit and receive LANEs; PGL100H contains 2 HSSTs with a total of 8 full-duplex transmit and receive LANEs.

HSST consists of two PLLs and four transmit and receive LANEs, each LANE comprising four components: PCS Transmitter, PMA Transmitter, PCS Receiver, PMA Receiver. The PCS Transmitter and PMA Transmitter make up the transmit path, and the PCS Receiver and PMA Receiver make up the receive path. The structure of HSST is shown in Figure 1-1:

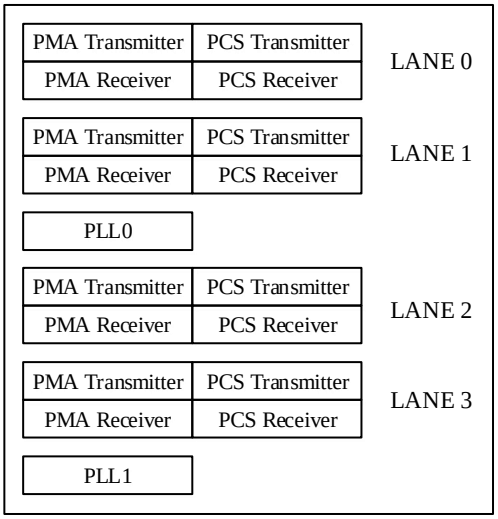

Figure 1-1 HSST Structure Diagram

For the four transmit and receive LANEs in HSST, LANEs 0/1 can only be clocked by PLL0, and LANEs 2/3 can be clocked by either PLL0 or PLL1. PLL0/1 each correspond to a pair of external differential reference clock inputs, and each PLL can also select a reference clock from another PLL or from the Fabric clock as the reference clock input (Fabric logic clock as reference clock is only for internal testing and not recommended); PLL output frequency supports dynamic re-division to accommodate a range of line rates.

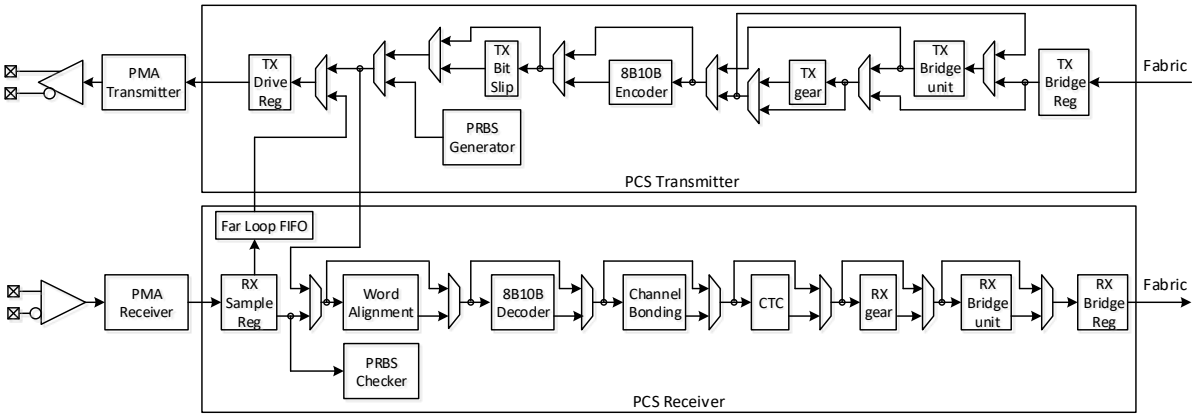

Figure 1-2 Schematic Diagram of PCS Transmitter and Receiver Structure

As shown in Figure 1-2, each PCS Transmitter mainly includes the following modules:

- TX Bridge Reg module: Used for data bridging from Fabric to PCS Transmitter
- TX Bridge unit module: Used for phase compensation for the internal clock domain of PCS Transmitter and the Fabric clock domain
- TX gear module: Completes data integration (encoding) in 64B66B/64B67B format
- 8B10B Encoder module: Completes 8B10B encoding compliant with IEEE 802.3 1000BASE-X specification

- TX Bit Slip module: The main function is to perform bit slip on the transmitted data according to configuration
- PRBS Generator module: Generates PRBS test data
- TX Drive Reg module: Used for data bridging from PCS Transmitter to PMA Transmitter

The TX Bridge unit, TX gear, 8B10B Encoder, and TX Bit Slip modules can be bypassed to meet the application requirements of different protocols. Users can flexibly choose the interface bit width between HSST and Fabric according to protocol requirements, with supported bit width modes including 8bit only, 10bit only, 8B10B 8bit (using 8B10B encoding, with 10bits of effective data after encoding), 16bit only, 20bit only, 8B10B 16bit, 32bit only, 40bit only, 8B10B 32bit, 64B66B/64B67B 16bit, and 64B66B/64B67B 32bit (where the bit width mode refers to effective data bits, with actual data interface bit count being extended). The higher the line rate, the wider the selected interface bit width, so that the timing requirements for the internal logic of the Fabric is reduced. When the data width is set to 32bit only, 40bit only, 8B10B 32bit, and 64B66B/64B67B 32bit, the PCS Transmitter converts the data to 16bits or 20bits before transferring it to the PMA Transmitter.

As shown in Figure 1-2, each PCS Receiver mainly includes the following functional modules:

- RX Sample Reg module: Used for data bridging from PMA Receiver to PCS Receiver
- Word Alignment module: Supports flexible byte alignment
- 8B10B Decoder module: Completes 8B10B decoding compliant with IEEE 802.3 1000BASE-X Specification
- Channel Bonding module: Used for channel bonding
- CTC module: Used for compensating the slight frequency error between the transmit clock and receive clock
- RX gear module: Completes data integration (decoding) in 64B66B/64B67B format
- RX Bridge unit module: Used for phase compensation for the internal clock domain of PCS Receiver and the Fabric clock domain
- RX Bridge Reg module: Used for data bridging from PCS Receiver to Fabric
- PRBS Checker module: Used for verifying PRBS sequences

Word Alignment, 8B10B Decoder, Channel Bonding, CTC, RX gear, RX Bridge unit modules can be bypassed by the user to meet the application requirements of different protocols. Users can also flexibly choose the interface bit width between HSST and Fabric according to protocol requirements, with supported bit width modes including 8bit only, 10 bit only, 8B10B 8bit (using 8B10B encoding, with 10bits of effective data before decoding), 16bit only, 20bit only, 8B10B 16bit, 32bit only, 40bit only, 8B10B 32bit, 64B66B/64B67B 16bit, and 64B66B/64B67B 32bit. Bit

width modes 32bit only, 40bit only, 8B10B 32bit, and 64B66B/64B67B 32bit are suitable for applications with higher line rates, where the PCS Receiver converts the 16bits or 20bits data from the PMA Receiver to 32bits or 40bits before transferring it to the Fabric.

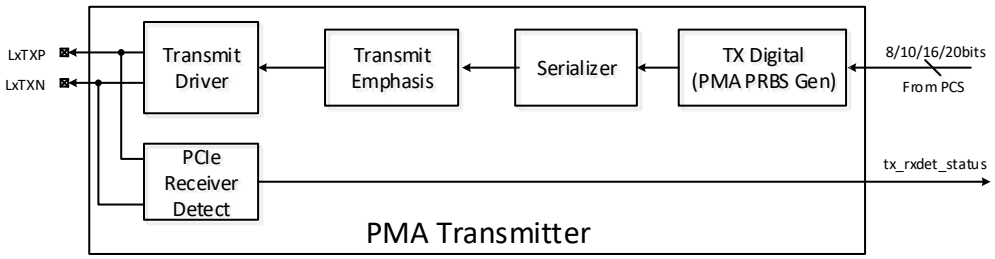

Figure 1-3 PMA Transmitter Functional Diagram

As shown in Figure 1-3, each PMA Transmitter mainly includes the following functional modules:

- TX Digital (PMA PRBS Gen) module: Completes data bridging from PCS Transmitter to PMA Transmitter, as well as PMA PRBS Generator
- Serializer module: Completes the conversion of parallel data to serial data
- Transmit Emphasis module: Supports adjustable de-emphasis function
- Transmit Driver module: Supports adjustable transmit driver
- PCIe Receiver Detect module: Supports PCI Express-based receive detection function

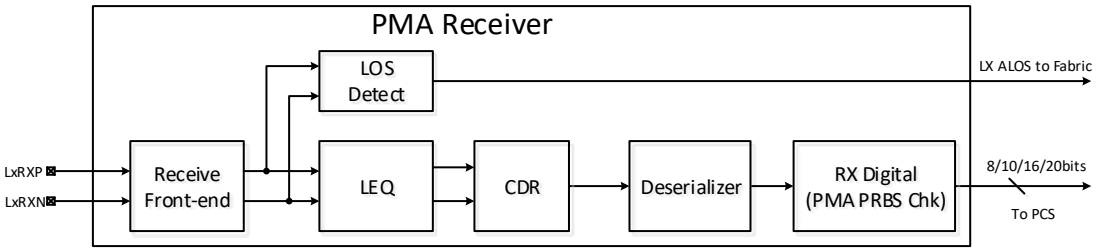

Figure 1-4 PMA Receiver Functional Diagram

As shown in Figure 1-4, each PMA Receiver mainly includes the following functional modules:

- Receive Front-end module: Supports multiple receive termination modes
- LEQ module: Supports linear equalization
- CDR module: Data and clock recovery
- LOS Detect module: Used for detecting if the receive signal is valid
- Deserializer module: Converts serial data to 8-bit, 10-bit, 16-bit, and 20-bit parallel data
- RX Digital (PMA PRBS Chk) module: Completes data bridging from PMA Receiver to PCS Receiver, and PMA PRBS Checker

Chapter 2 HSST Interface Description

Table 2-1 HSST LANE Clock-Related Ports

Port Naming	Input/ Output	Clock Domain	Description
P_RCLK2FABRIC	Output	-	Receive clock sent to Fabric
P_TCLK2FABRIC	Output	-	Transmit clock sent to Fabric
P_RX_CLK_FR_CORE	Input	-	Receive clock from Fabric, serving as the RX interface data clock
P_RCLK2_FR_CORE	Input	-	Receive clock from Fabric, which is generated by P_REFCK2CORE through PLL frequency multiplication and twice the frequency of P_RX_CLK_FR_CORE
P_TX_CLK_FR_CORE	Input	-	Transmit clock from Fabric, serving as the TX interface data clock
P_TCLK2_FR_CORE	Input	-	Transmit clock from Fabric, which is generated by P_REFCK2CORE through PLL frequency multiplication and twice the frequency of P_TX_CLK_FR_CORE
P_CA_ALIGN_RX	Output	Asynchronous Signal	Receiving LANE CLK Aligner dynamic state output, a 0-to-1 transition indicates aligner success, an asynchronous signal
P_CA_ALIGN_TX	Output	Asynchronous Signal	Transmitting LANE CLK Aligner dynamic state output, a 0-to-1 transition indicates aligner success, an asynchronous signal
P_CIM_CLK_ALIGNER_RX[7:0]	Input	Asynchronous Signal	CLK Aligner delay step selection at receive side, an asynchronous signal
P_CIM_CLK_ALIGNER_TX[7:0]	Input	Asynchronous Signal	CLK Aligner delay step selection at transmit side, an asynchronous signal
P_CIM_DYN_DLY_SEL_RX	Input	Asynchronous Signal	Receive LANE's CLK Aligner enable, an asynchronous signal, 1: Enabled; 0: Disabled
P_CIM_DYN_DLY_SEL_TX	Input	Asynchronous Signal	Transmit LANE's CLK Aligner enable, an asynchronous signal, 1: Enabled; 0: Disabled
P_CIM_START_ALIGN_RX	Input	Asynchronous Signal	Input source for generating receive LANE CLK Aligner pulse, the setting value is triggered once on rising edge, an asynchronous signal
P_CIM_START_ALIGN_TX	Input	Asynchronous Signal	Input source for generating transmit LANE CLK Aligner pulse, the setting value is triggered once on rising edge, an asynchronous signal

Table 2-2 HSST LANE Reset-Related Ports

Port Naming	Input/ Output	Clock Domain	Description
P_PCS_TX_RST	Input	Asynchronous Signal	Reset PCS Transmitter, 1: Reset; 0: Not reset
P_PCS_RX_RST	Input	Asynchronous Signal	Reset PCS Receiver, 1: Reset; 0: Not reset
P_LANE_PD	Input	Asynchronous Signal	Reserved, fixed to value 0

Port Naming	Input/ Output	Clock Domain	Description
P_LANE_RST	Input	Asynchronous Signal	Lane reset, includes: RX LANE and TX LANE; 1: reset; 0: not reset
P_RX_LANE_PD	Input	Asynchronous Signal	RX LANE power control, includes: RX PMA and RX PCS; 1: Powered off; 0: Not powered off
P_RX_PMA_RST	Input	Asynchronous Signal	Reset PMA Receiver, an asynchronous signal, 1: reset; 0: not reset
P_TX_PMA_RST	Input	Asynchronous Signal	Reset PMA Transmitter, an asynchronous signal, 1: reset; 0: not reset
P_TX_LANE_PD	Input	Asynchronous Signal	TX LANE power control, includes: TX PMA and TX PCS; 1: Powered off; 0: Not powered off
P_PCS_CB_RST	Input	Asynchronous Signal	Reset module after Channel bonding, 1: Reset; 0: Not reset;
P_CTLE_ADP_RST	Input	Asynchronous Signal	Reset the linear equalizer of the PMA receiver, 1: Reset; 0: Not reset;

Table 2-3 Transmitting Ports between HSST LANE and Fabric

Port Naming	Input/ Output	Clock Domain	Description
P_TDATA[45:0]	Input	P_TX_CLK_FR_CORE	Transmit data
P_TX_LS_DATA	Input	P_TX_CLK_FR_CORE	Transmitted low-frequency signal
P_TX_BEACON_EN	Input	Asynchronous Signal	TX beacon enable signal, 1: Enabled; 0: Disabled
P_TX_DEEMP[1:0]	Input	Asynchronous Signal	Transmitter de-emphasis control
P_TX_SWING	Input	Asynchronous Signal	Transmitter output swing value for half-swing control 1’b0: Full swing (default); 1'b1: Half swing
P_TX_MARGIN[2:0]	Input	Asynchronous Signal	Transmitter output swing DAC source selection. Default value 3'b000 3'b000: Swing source register PMA_CH_REG_TX_AMP_DAC0; 3'b001: Swing source register PMA_CH_REG_TX_AMP_DAC1; 3'b010: Swing source register PMA_CH_REG_TX_AMP_DAC2; 3'b011: Swing source register PMA_CH_REG_TX_AMP_DAC3; Other value: reserved
P_TX_RXDET_REQ	Input	Asynchronous Signal	Receiver Detection request signal
P_TX_RXDET_STATUS	Output	Asynchronous Signal	Receiver Detection result, an asynchronous signal,1: Receiver detected
P_TX_RATE[2:0]	Input	Asynchronous Signal	TX line rate control signal 3’b000: The line rate is 1/8 of the maximum data rate; 3’b001: The line rate is 1/4 of the maximum data rate; 3’b010: The line rate is half of the maximum data rate; 3’b011: The line rate is equal to the maximum data rate; Other value: reserved
P_TX_BUSWIDTH[2:0]	Input	Asynchronous Signal	Bit width selection from TX PCS to TX PMA 3’b000: 8bit; 3’b001:10bit;

Port Naming	Input/ Output	Clock Domain	Description
			3'b010:16bit; 3'b011:20bit; Other value: reserved

Table 2-4 Receiving Ports between HSST LANE and Fabric

Port Naming	Input/ Output	Clock Domain	Description
P_RDATA[46:0]	Output	P_RX_CLK_FR_CORE	Receive data
P_RX_SIGDET_STATUS	Output	Asynchronous Signal	Port valid signal detection, an asynchronous signal: 0: No valid signal detected from port P_RX_SDP/P_RX_SDN 1: Valid signal detected from port P_RX_SDP/P_RX_SDN
P_RX_SATA_COMINIT	Output	Asynchronous Signal	SATA COMINIT status, 1: Detected; 0: Not detected
P_RX_SATA_COMWAKE	Output	Asynchronous Signal	SATA COMWAKE status, 1: Detected; 0: Not detected
P_RX_LS_DATA	Output	P_RX_CLK_FR_CORE	Low-frequency signal output to Fabric
P_RX_READY	Output	Asynchronous Signal	CDR has successfully locked the flag signal, an asynchronous signal, 1: Locked; 0: Unlocked
P_TEST_STATUS[19:0]	Output	Asynchronous Signal	RX output test status register, internal test signal
P_PCS_WORD_ALIGN_EN	Input	Asynchronous Signal	When configured as effective control by the RX CLK Slip port control method, it serves as the RX CLK Slip control signal, an asynchronous signal, A rising edge from 0 to 1 causes the PMA RX's Deserializer module to slip one bit When configured for an external state machine, serves as the Word Alignment enable signal, an asynchronous signal, 1: Enabled; 0: Disabled
P_PCS_LSM_SYNCED	Output	Asynchronous Signal	Word Alignment successful, state machine lock flag, an asynchronous signal, 1: Word Alignment successful; 0: Word Alignment unsuccessful;
P_PCS_MCB_EXT_EN	Input	Asynchronous Signal	Channel bonding enable under external state machine mode, an asynchronous signal, 1: Enabled; 0: Disabled
P_PCS_RX_MCB_STATUS	Output	Asynchronous Signal	Channel Bonding control state machine lock signal, an asynchronous signal, 1: Bonded; 0: Not bonded
P_RXGEAR_SLIP	Input	Asynchronous Signal	Slip indication to RX gearbox with 64B66B/67B decoder mode, edge-triggered, detection of either a rising or falling edge will cause a slip of 1 bit, asynchronous signal, internally synchronized by the PCS
P_RX_POLARITY_INVERT	Input	Asynchronous Signal	RX Sample Reg's polarity inversion enable, an asynchronous signal, 1: Polarity inverted; 0: Polarity not inverted
P_CEB_ADETECT_EN[3:0]	Input	Asynchronous Signal	Test signal, set externally to 4'b1111' in normal mode
P_RX_RATE[2:0]	Input	Asynchronous Signal	RX line rate control signal 3'b000: The line rate is 1/8 of the maximum data rate;

Port Naming	Input/ Output	Clock Domain	Description
			3'b001: The line rate is 1/4 of the maximum data rate; 3'b010: The line rate is half of the maximum data rate; 3'b011: The line rate is equal to the maximum data rate; Other value: reserved
P_RX_BUSWIDTH[2:0]	Input	Asynchronous Signal	Bit width selection from RX PMA to RX PCS 3'b000: 8bit; 3'b001:10bit; 3'b010:16bit; 3'b011:20bit; Other value: reserved
P_RX_HIGHZ	Input	Asynchronous Signal	RX input high impedance control signal, 0: Not at high impedance; 1: At high impedance

Table 2-5 Other Ports between HSST LANE and Fabric

Port Naming	Input/ Output	Clock Domain	Description
P_PCS_NEAREND_LOOP	Input	Asynchronous Signal	PCS near-end loopback control signal, 1: Enabled; 0: Disabled
P_PCS_FAREND_LOOP	Input	Asynchronous Signal	PCS far-end loopback control signal, 1: Enabled; 0: Disabled
P_PMA_NEAREND_PLOOP	Input	Asynchronous Signal	PMA near-end parallel loopback control signal, 1: Enabled; 0: Disabled
P_PMA_NEAREND_SLOOP	Input	Asynchronous Signal	PMA near-end serial loopback control signal, 1: Enabled; 0: Disabled
P_PMA_FAREND_PLOOP	Input	Asynchronous Signal	PMA far-end parallel loopback control signal, 1: Enabled; 0: Disabled
P_CFG_READY	Output	P_CFG_CLK	Dynamic configuration interface read and write ready output, 1: Valid; 0: Invalid
P_CFG_RDATA[7:0]	Output	P_CFG_CLK	Read data for the dynamic configuration interface
P_CFG_INT	Output	P_CFG_CLK	Dynamic configuration interface interrupt output, 1: Valid; 0: Invalid
P_CFG_CLK	Input	-	Dynamically configure the clock input of the interface
P_CFG_RST	Input	P_CFG_CLK	Dynamic configuration interface reset signal, 1: Reset; 0: Not reset. All registers revert to the initial values set by the Parameter after reset
P_CFG_PSEL	Input	P_CFG_CLK	Dynamic configuration interface selection signal, 1: Selected; 0: Not selected
P_CFG_ENABLE	Input	P_CFG_CLK	Dynamic configuration interface access enable, 1: Enabled; 0: Disabled
P_CFG_WRITE	Input	P_CFG_CLK	Dynamic configuration interface read or write select signal, 1: Write; 0: Read
P_CFG_ADDR[15:0]	Input	P_CFG_CLK	Dynamic configuration interface read and write address
P_CFG_WDATA[7:0]	Input	P_CFG_CLK	Dynamic configuration interface write data

Table 2-6 HSST PLL Ports

Port Naming	Input/Output	Clock Domain	Description
P_REFCK2CORE	Output	-	Pin input reference clock output to Fabric
P_PLL_REF_CLK	Input	-	PLL reference clock from Fabric

Port Naming	Input/Output	Clock Domain	Description
P_PLL_READY	Output	Asynchronous Signal	PLL lock status, an asynchronous signal, 1: Locked; 0: Unlocked
P_PLLPOWERDOWN	Input	Asynchronous Signal	PLL powered-off control 0: Not powered off (default); 1: Powered off
P_PLL_RST	Input	Asynchronous Signal	PLL reset control, 0: Not reset (default); 1: Reset
P_RESCAL_RST_I	Input	Asynchronous Signal	Resistor calibration reset, 1: Reset; 0: Not reset, Internal test signal, connected to a fixed value of 0.
P_RESCAL_I_CODE_I[5:0]	Input	Asynchronous Signal	PMA manual configuration of resistance value, default value 6'b101110, internal test signal
P_RESCAL_I_CODE_O[5:0]	Output	Asynchronous Signal	The resistor control output code when invalid, default value 6'b101110 internal test signal
P_LANE_SYNC	Input	Asynchronous Signal	Synchronization signal of the transmit channel
P_RATE_CHANGE_TXPCLK_ON	Input	Asynchronous Signal	Synchronization control signal enable for dynamic switching

Table 2-7 HSST External Ports

Port Naming	Input/Output	Clock Domain	Description
P_TX_SDN	Output	-	Differential output data negative end, HSST dedicated pin
P_TX_SDP	Output	-	Differential output data positive end, HSST dedicated pin
P_RX_SDN	Input	-	Differential input data negative end, HSST dedicated pin
P_RX_SDP	Input	-	Differential input data positive end, HSST dedicated pin
P_REFCLKN	Input	-	Differential input reference clock negative end, HSST dedicated pin
P_REFCLKP	Input	-	Differential input reference clock positive end, HSST dedicated pin

Chapter 3 HSST Functional Description

3.1 HSST Clock Structure

3.1.1 Reference Clock Selection

HSST supports flexible selection of PLL0 and PLL1 reference clocks: each HSST has two pairs of dedicated differential reference clock input pins P_REFCLKP_0/P_REFCLKN_0 and P_REFCLKP_1/P_REFCLKN_1. The PLL can also select clocks from the Fabric P_PLL_REF_CLK_0, P_PLL_REF_CLK_1 (Fabric logic clock as reference clock, only for internal testing, not recommended); dedicated clock input pins P_REFCLKP_0/P_REFCLKN_0 and P_REFCLKP_1/P_REFCLKN_1 can also be output to the Fabric through ports P_REFCK2CORE_0 and P_REFCK2CORE_1. The structural diagram of the reference clock selection is shown in Figure 3-1:

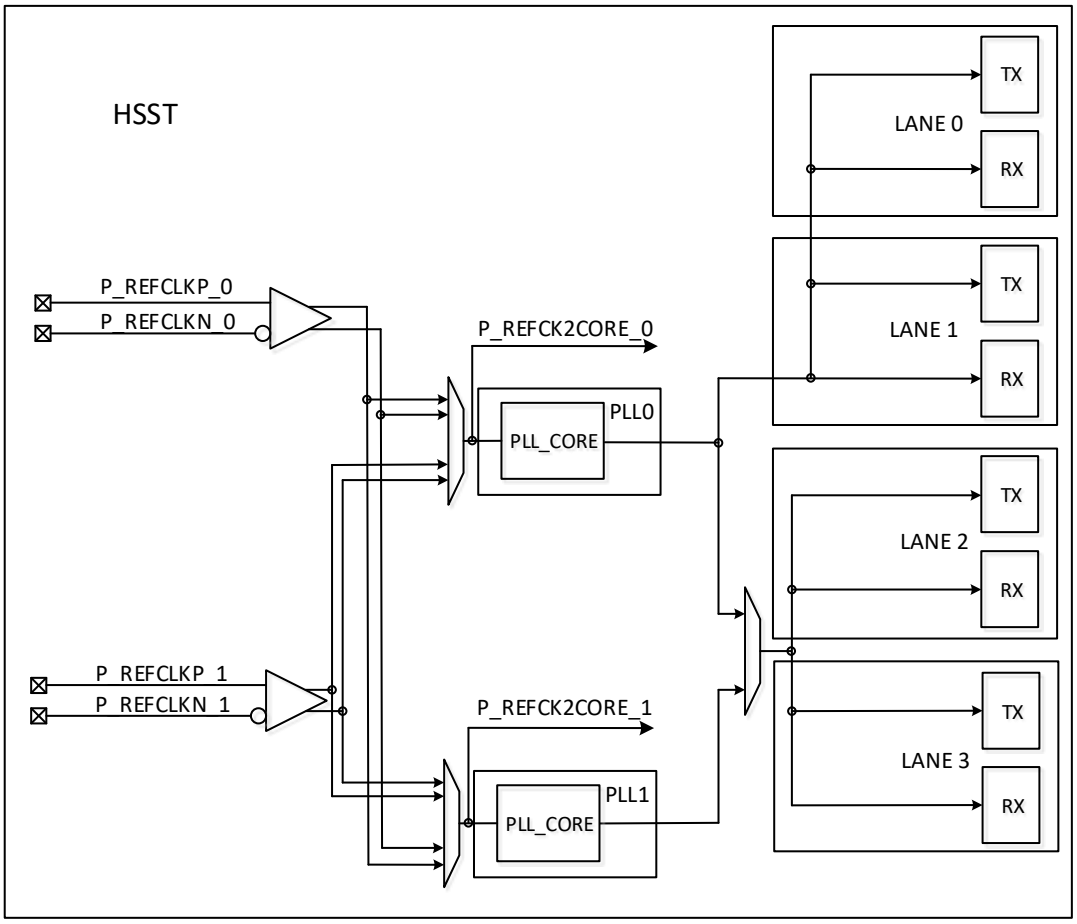

Figure 3-1 Reference Clock Source Selection Structure Diagram

The reference clock input circuit is shown in Figure 3-1. Wherein, PLL0 can be assigned to

LANE0-LANE3, and PLL1 can be assigned to LANE2 and LANE3.

Please note, as shown in Figure 3-1, the clock sources for LANE0 and LANE1 can be only derived from the same PLL, and the clock sources for LANE2 and LANE3 can be only derived from the same PLL.

Matching resistors are connected on the clock input ports P and N, for resistance values, please refer to the "HSST Hard IP DC Electrical Characteristics" section in the "***DS02001_Logos Family FPGAs Datasheet***"; the middle virtual ground can be left floating or connected to the internal common-mode voltage. The reference clock is connected to the buffer after passing through the AC coupling capacitor and then output to the internal PLL loop.

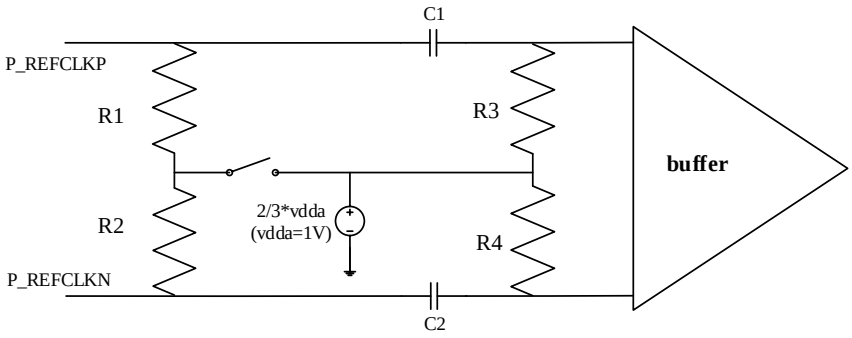

Figure 3-2 Reference Clock Input Circuit

3.1.2 Clock Structure of the Transmit Path

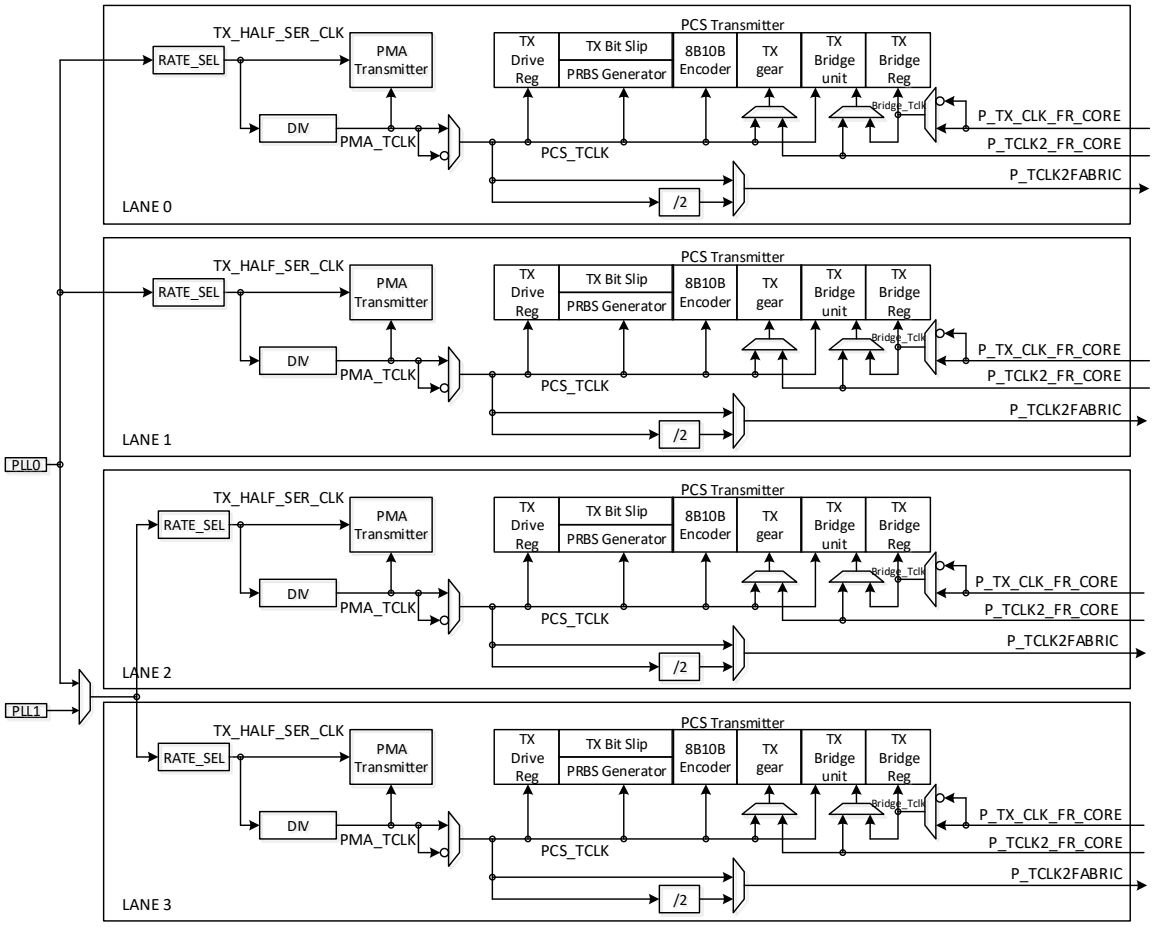

Figure 3-3 Transmit Path Clock Structure Diagram

As shown in Figure 3-3, HSST shares PLL0 and PLL1, with the high-speed clock output of PLL0 distributed to four LANEs, and that of PLL1 distributed to LANE2 and LANE3. Users can independently generate TX_HALF_SER_CLK for each LANE based on the PLL output, using a division factor, with the line rate being twice the frequency of TX_HALF_SER_CLK. Here, the frequency of TX_HALF_SER_CLK is derived by dividing the PLL output frequency by RATE_SLE.

The channel rate supports dynamic configuration, suitable for dynamic rate selection in applications such as PCI Express.

PMA_TCLK is generated by further dividing the TX_SER_CLK, supporting multiple division ratios to accommodate the 8/10/16/20 bits data width interface between PMA and PCS. PMA_TCLK, once passed to the PCS Transmitter, is referred to as PCS_TCLK.

The clock output P_TCLK2FABRIC can be used for Fabric internal processing; at lower Data Rates (e.g., 3Gbps), its frequency is consistent with PCS_TCLK; at higher Data Rates, it can be reduced to half the frequency of PCS_TCLK.

The clock input P_TX_CLK_FR_CORE is the transmit clock fed back from the Fabric, P_TX_CLK2_FR_CORE is twice the frequency of P_TX_CLK_FR_CORE and phase-aligned, P_TX_CLK_FR_CORE and P_TX_CLK2_FR_CORE can be generated by the PLL in the Fabric from the refclk output by the PCS.

3.1.3 Clock Structure of the Receive Path

Each HSST receiving LANE has an RX CDR with integrated PLL function; after division by RATE_SEL, the generated clock signal RX_HALF_SER_CLK has a frequency that is half of the channel's line rate. The clock structure diagram of the receiving LANE is shown in Figure 3-4:

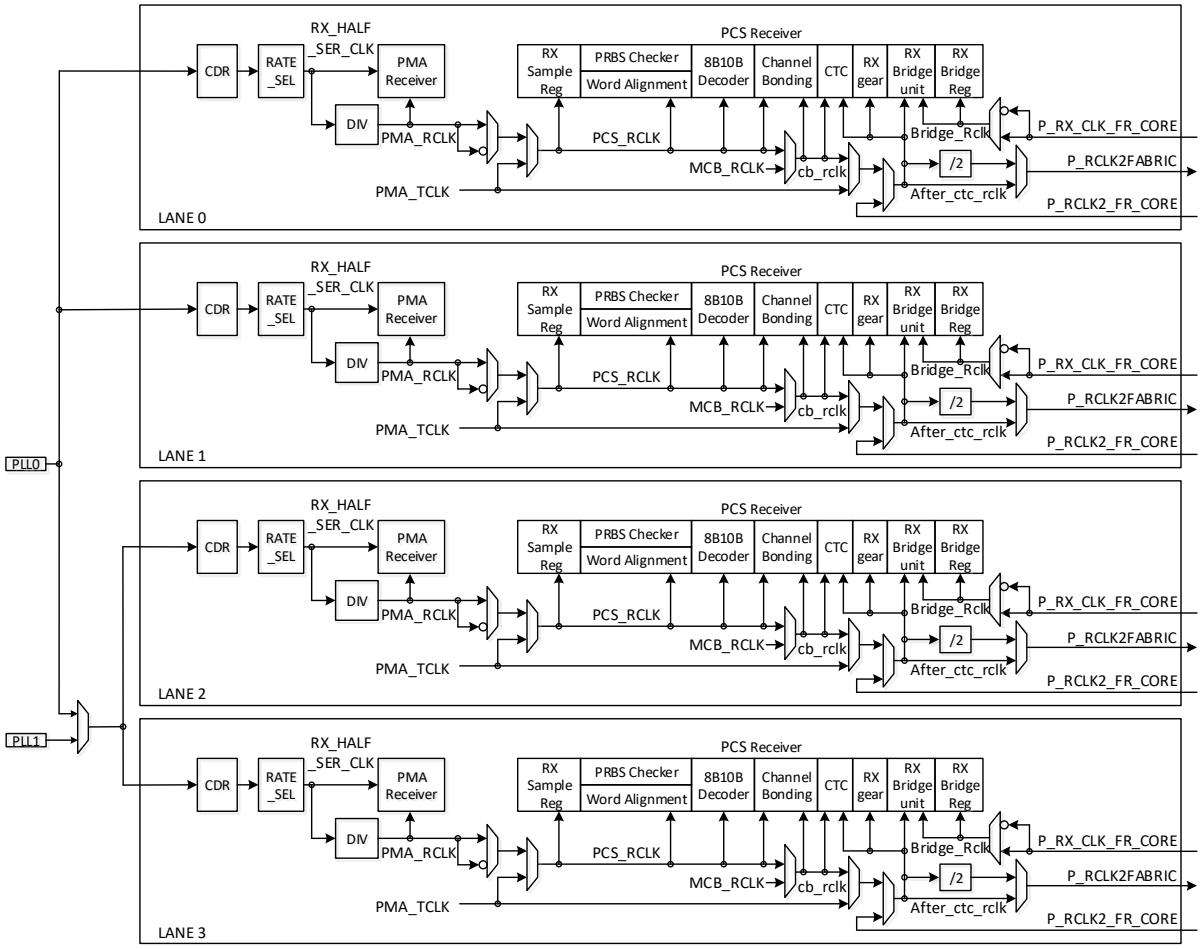

Figure 3-4 Receiving LANE Clock Structure Diagram

PMA_RCLK is generated by further dividing RX_HALF_SER_CLK, supporting multiple division ratios to accommodate the 8/10/16/20 bits data width interface between PMA and PCS. Once PMA_RCLK is passed to the PCS Receiver, it is referred to as PCS_RCLK.

When channel bonding is enabled, the data from each LANE is synchronized to the same clock MCB_RCLK after passing through the channel bonding module. Here, MCB_RCLK is derived

from the Bonding Master's PMA_RCLK; in a 4-channel bonding, it comes from LANE 0's PMA_RCLK; in a 2-channel bonding, it comes from either LANE 0 or LANE 2's PMA_RCLK.

When the CTC is enabled, the data processed through the CTC module will transfer to the PMA_TCLK clock domain, where PMA_TCLK is derived from the PMA Transmitter of the respective LANE.

The clock output P_RCLK2FABRIC can be used for Fabric received data processing. At lower Data Rates (e.g., 3Gbps), its frequency is consistent with PMA_RCLK; at higher Data Rates, the frequency of P_RCLK2FABRIC can be reduced to half of PMA_RCLK.

3.2 PLL Function

Each HSST contains four LANEs, with TX and RX sharing PLL0 and PLL1. PLL0 can provide clocks for all four LANEs, while PLL1 can only provide clocks for LANEs 2/3. The functional structure diagram is shown in Figure 3-5.

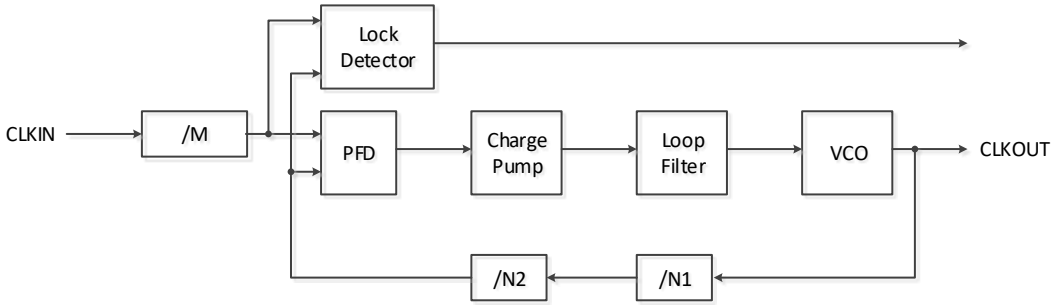

Figure 3-5 PLL Structure Schematic

The input clock and feedback clock pass through the Phase Frequency Detector (PFD), Charge Pump and Loop Filter in sequence. For VCO frequency and PLL input clock frequency range, refer to the "AC Characteristics of High-Speed Serial Transceiver HSST" section in the "***DS02001_Logos Family FPGAs Datasheet***". The PLL output frequency is determined by the input clock CLKIN frequency, input division factor M, and feedback division factors N1 and N2, with the calculation method as follows:

$$\mathrm{CLKOUT} = \frac{\mathrm{CLKIN}}{\mathrm{M}} \times \mathrm{N1} \times \mathrm{N2}$$

Requirements for Phase Frequency Detector port input clock frequency range ($\frac{CLKIN}{M}$): 60MHz~312.5MHz.

When the Phase Frequency Detector port input clock frequency is between 60MHz~70MHz, the register REG_QPCURRENT should be configured to 4'b0011; when the frequency is between 70MHz~312.5MHz, REG_QPCURRENT should be configured to 4'b0100.

The relationship between PMA line rate and PLL output is calculated as follows:

$$\text{PMA Line Rate} = 2 \times \frac{\text{CLKOUT}}{D}$$

Where D represents the division ratio on the TX or RX clock path.

Note: When both PLL0 and PLL1 are in use, if there is a need to power down or reset one of the PLLs individually, a separate reference clock must be provided for PLL0 and PLL1 respectively. If using the shared reference clock REFCLK0, powering down or resetting PLL0 will affect PLL1; conversely, powering down or resetting PLL1 will not affect PLL0. Similarly, if using the shared reference clock REFCLK1, powering down or resetting PLL1 will affect PLL0; conversely, powering down or resetting PLL0 will not affect PLL1.

The PLL division factor M corresponds to PLL register address 0x017 bit[0], N1 corresponds to PLL register address 0x00a bit[1], N2 corresponds to PLL register address 0x00a bit[3:2]; after modification, it is necessary to first reset the PLL, then reset the relevant TX or RX channels;

The TX clock division ratio D corresponds to PMA register address 0x00c bit[1:0]; when dynamic rate switching in transmit direction is performed via the register, it is necessary to set PMA register address 0x00c bit[3] to 1, and after modification, reset the corresponding TX channel;

The RX clock division ratio D corresponds to PMA register address 0x004 bit[5:4]; when dynamically switching the reception rate via the register, it is necessary to set PMA register address 0x004 bit[7] to 1, and after modification, reset the corresponding RX channel;

See the description of the corresponding register parameters for details.

Table 3-1 Supported Range for PLL Division Factors

Division Factor	**Supported Values**
M	1, 2
N1	4, 5
N2	2, 4, 5

3.3 PCS Transmitter Function

3.3.1 TX Bridge Reg Module

Completes the transmission data bridging from Fabric to HSST, ensuring interface timing. Each LANE has 46 bits of transmission data, with definitions varying according to different bit width modes, see Table 3-2 for details:

Table 3-2 LANE Transmission Data Definitions

	P_TDATA_x Data Bit																		
Data Width Mode	[45:44]	[43]	[42]	[41]	[40:39]	[38:33]	[32]	[31]	[30]	[29:22]	[21]	[20]	[19]	[18:17]	[16:11]	[10]	[9]	[8]	[7:0]
8bit only	PCIe_EI	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	TXD [7:0]
10bit only	PCIe_EI	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	TXD [9:0]		
8b10b 8bit	PCIe_EI	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	TXK	TDISPCTRL	TDISPSEL	TXD [7:0]
16bit only	PCIe_EI	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	TXD [15:10]	NA	TXD [9:0]		
20bit only	PCIe_EI	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	TXD [19:10]				NA	TXD [9:0]		
8b10b 16bit	PCIe_EI	NA	NA	NA	NA	NA	NA	NA	NA	NA	TXK [1]	TDISPCTRL [1]	TDISPSEL [1]	TXD [15:8]		TXK [0]	TDISPCTRL [0]	TDISPSEL [0]	TXD [7:0]
32bit only	PCIe_EI	NA	NA	NA	NA	TXD [31:26]	NA	TXD [25:16]			NA	NA	NA	NA	TXD [15:10]	NA	TXD [9:0]		
40bit only	PCIe_EI	NA	TXD [39:30]				NA	TXD [29:20]			NA	TXD [19:10]				NA	TXD [9:0]		
8b10b 32bit	PCIe_EI	TXK [3]	TDISPCTRL [7:6]		TXD [31:24]		TXK [2]	TDISPCTRL [2]	TDISPSEL [2]	TXD [23:16]	TXK [1]	TDISPCTRL [1]	TDISPSEL [1]	TXD [15:8]		TXK [0]	TDISPCTRL [0]	TDISPSEL [0]	TXD [7:0]
64b 66b 16bit	PCIe_EI	TXH[2:0]			TXQ [6:5]	NA	NA	NA	NA	NA	TXQ[4:0]				TXD [15:10]	NA	TXD[9:0]		
64b 66b 32bit	PCIe_EI	TXH[2:0]			TXQ [6:5]	TXD [31:26]	NA	TXD[25:16]			TXQ[4:0]				TXD [15:10]	NA	TXD[9:0]		

The definitions of the data bits are shown in the following table:

Table 3-3 Definitions of Data Bits in P_TDATA

Data Bit Name	**Description**
TXK	1 indicates that TXD is the 8B10B Special Code-groups according to the IEEE 802.3 1000BASE-X Specification; 0 indicates that TXD is the 8B10B Data Code-groups according to the IEEE 802.3 1000BASE-X Specification;
TXD	code-groups
TDISPCTRL	Used for forcing the 8B10B polarity and the mandatory replacement from I2 to I1, {TDISCTRL, TDISPSEL} can be: 2'b00: Normal Data Transmission 2'b01: According to the IEEE 802.3 1000BASE-X specification protocol, it implements the selection of the first I1/I2 at the frame trailer, and automatically accomplishes the replacement from I2 to I1 under the right conditions. 2'b10: Forces the 8B10B encoding polarity to be negative 2'b11: Forces the 8B10B encoding polarity to be positive
TDISPSEL	
PCIe_EI	PCI Express electrical_idle indication, including PCIe_E1_H and PCIe_E1_L
TXH	Transmitted message header for 64B66B mode
TXQ	Sequence number for 64B66B mode

3.3.2 TX Bridge Unit Module

The TX Bridge unit module completes phase compensation from BRIDGE_TCLK to PCS_TCLK, with a FIFO depth of 8.

3.3.3 TX Gear Module

The TX gear module completes the interface rate adaptation for 64B66B or 64B67B in the TX direction. Supports two bit width modes for PCS and Fabric interfaces: 64B66B_16bit and 64B66B_32bit.

64B66B_16bit: Corresponds to 64B66B or 64B67B encoded data, with Fabric interface width TX_DATA being 16bit;

64B66B_32bit: Corresponds to 64B66B or 64B67B encoded data, with Fabric interface width TX_DATA being 32bit.

3.3.4 8B10B Encoder Module

Implements the 8B10B Encode function in accordance with the IEEE 802.3 1000BASE-X Specification, see IEEE Std802.3 36.2 Physical Coding Sublayer (PCS) for details.

3.3.5 TX Bit Slip Module

The main function is to perform bit slip on transmitted data according to configuration, to implement data transmission and reception delay consistency in applications such as CPRI. The number of Bits for Slip is set through the Parameter PCS_TX_BIT_SLIP_CYCLES.

The Slip function of the TX Bit Slip can operate under various bit width modes. In 20bit only, 8B10B 16bit, 40bit only, and 8B10B 32bit modes, the TX Bit Slip can implement a 0~19bit slip, as shown in Figure 3-6:

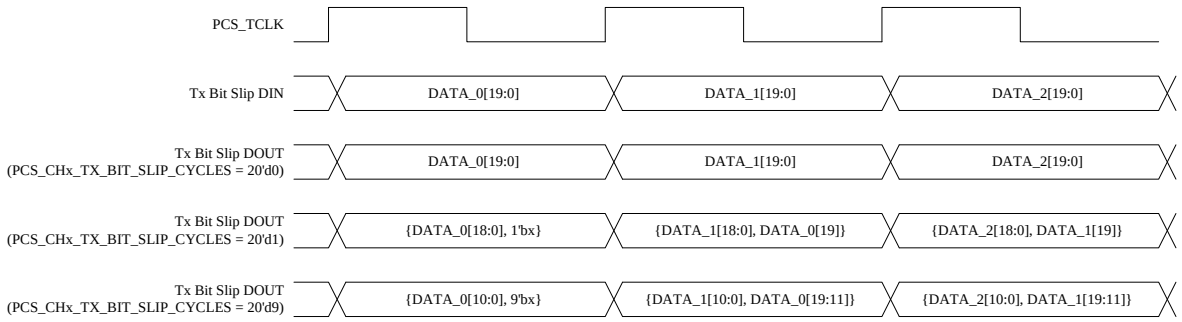

Figure 3-6 TX Bit Slip Module's 0~19bit Slip Functional Diagram

In 10bit only and 8B10B 8bit modes, the TX Bit Slip can implement a 0~9bit slip, as shown in Figure 3-7:

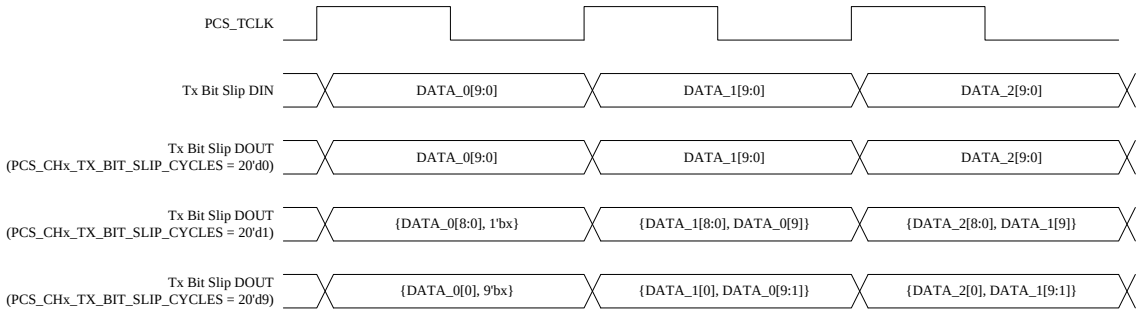

Figure 3-7 TX Bit Slip Module's 0~9bit Slip Functional Diagram

3.3.6 PRBS Generator Module

The PRBS Generator module is responsible for generating various feature code streams, commonly used for PMA testing; users can select the required feature code stream by the Parameter PCS_TX_PRBS_MODE. The PRBS Generator module can operate in internal bit width modes of 8bit, 10bit, 16bit, and 20bit only.

Table 3-4 PRBS Generation Patterns

PCS_TX_PRBS_MODE Value	**Feature Code Stream**
"PRBS_7"	Generates random numbers based on the polynomial 1 + X6 + X7
"PRBS_15"	Generates random numbers based on the polynomial 1 + X14 + X15
"PRBS_23"	Generates random numbers based on the polynomial 1 + X18 + X23
"PRBS_31"	Generates random numbers based on the polynomial 1 + X28 + X31
"LONG_1"	Output all 1 signal
"LONG_0"	Output all 0 signal
"20UI"	Alternating transmission of 20bit 1s and 20bit 0s
"D10_2"	Outputs the sequence 20'b0101010101_0101010101; corresponding to D10.2 in 8B10B encoding
"PCIE"	Outputs PCI Express Compliance Pattern; i.e., alternating transmission of the sequence 20'b001111_1010_101010_1010 and the sequence 20'b110000_0101_010101_0101

Users can dynamically modify the PCS channel configuration Parameter PCS_TX_INSERT_ER to insert error codes into the generated test code stream. With each transition of PCS_TX_INSERT_ER from 0 to 1, an error injection operation is performed, with the number of error bits injected being variable.

3.3.7 TX Drive Reg Module

Completes data bridging from the PCS Transmitter to the PMA Transmitter, ensuring interface timing. The TX Drive Reg module can implement polarity inversion of transmitted serial data, and

bit order inversion of parallel data based on the PCS and PMA interfaces, through Parameter PCS_TX_DRIVE_REG_MODE.

When polarity inversion is enabled, the data ports P_TX_SDP and P_TX_SDN transmitted from the HSST are exchanged with each other. When bit order inversion is enabled, the transmitted data from the PCS Transmitter to the PMA Transmitter is inverted in bit order, that is:

For valid data of 8 bits, the inverted bit order data is

data_out[7:0]={data_in[0],data_in[1]...,data_in[7]}

3.4 PMA Transmitter Function

3.4.1 TX Digital Module

The TX Digital module mainly implements data bridging from PCS to PMA, including the following functions:

- Processes control signals related to transmission;
- PRBS generator;
- Implements PMA far-end parallel loopback;
- Selectable parallel data types to be transmitted to PMA;
- Data error injection;

3.4.2 Serializer Module

The main function of the Serializer is to convert the 20bits parallel data from TX Digital into serial data. Here, the 20bits refer to the parallel bit width between PCS and PMA, which is part of the HSST internal bit width, with the lower bits first out during parallel-to-serial conversion. The effective bit width of TX parallel data is controlled by the register PMA_REG_TX_BUSWIDTH, and the correspondence is as follows:

Table 3-5 Correspondence between TX Parallel Data Effective Bit Width and PMA_REG_TX_BUSWIDTH Register

PMA_REG_TX_BUSWIDTH	TX Parallel Data Effective Bit Width	Output data
2'b00	8bit	pma_txd<7:0> serialized output, higher bits discarded
2'b01	10bit	pma_txd<9:0> serialized output, higher bits discarded
2'b10	16bit	pma_txd<17:10>, pma_txd<7:0> serialized output, other bits discarded
2'b11	20bit	pma_txd<19:0> serialized output

3.4.3 Configurable TX Output Module

The output stage of TX adopts current mode to accommodate the needs of different protocols and scenarios, and it includes the following features:

- High-Speed Differential Current Mode Output;
- Configurable Output Amplitude;
- Configurable Post-Cursor De-emphasis;
- Correctable Output Impedance;

The circuit architecture of the output stage is as follows:

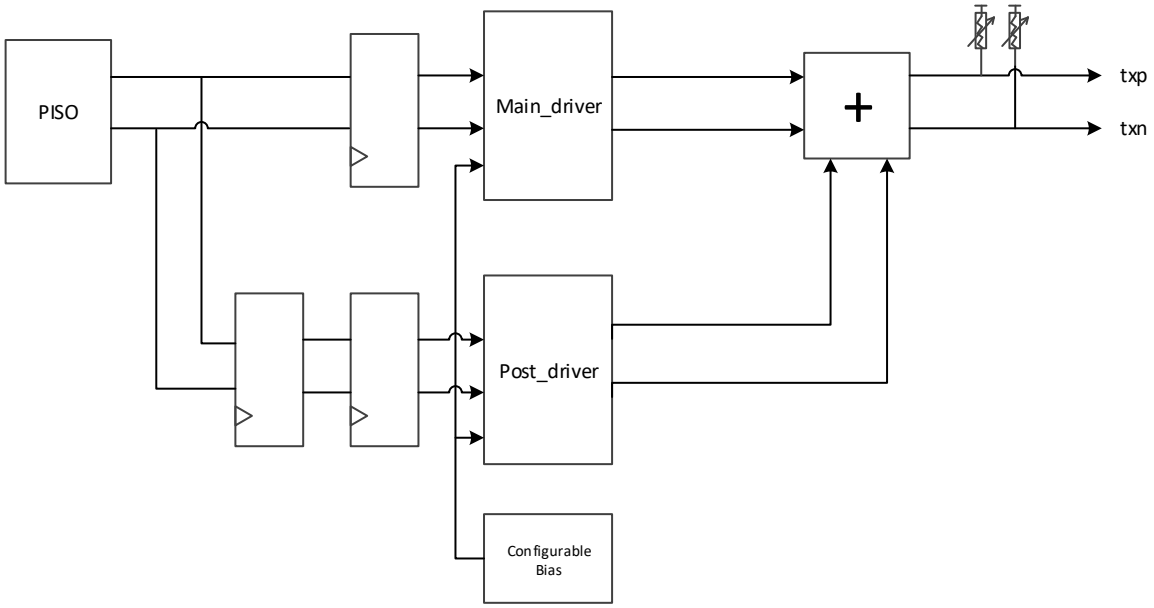

Figure 3-8 Architecture Diagram of TX Output Stage Circuit

3.4.4 PCI Express Receiver Detect Module

The PCIE protocol requires the PMA to be able to detect the receiver load from transmitter to verify whether the link is established. The principle of load detection at transmitter is based on the rise time of the output signal, as shown in Figure 3-9. During load detection, a capacitor greater than 100nF needs to be externally connected between TX output and RX input, and the RX input must be pulled down to ground through a matching resistor. At the start of detection, TX output is first placed on the common-mode output, then the bias current of the TX drive stage is cut off. After 1.8μs, the TX output voltage is compared with the corresponding threshold voltage. If it is less than the threshold voltage, it indicates that the link is established; otherwise, the link is not established.

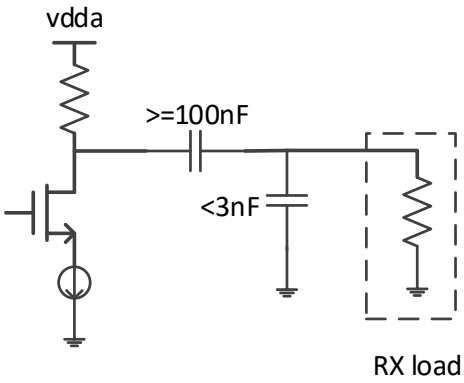

Figure 3-9 Schematic of Load Detection at Transmitter

Receiver detection is controlled by the register signal P_TX_RXDET_REQ, and the detection result is reflected by P_TX_RXDET_STATUS. The timing relationship between them is as follows.

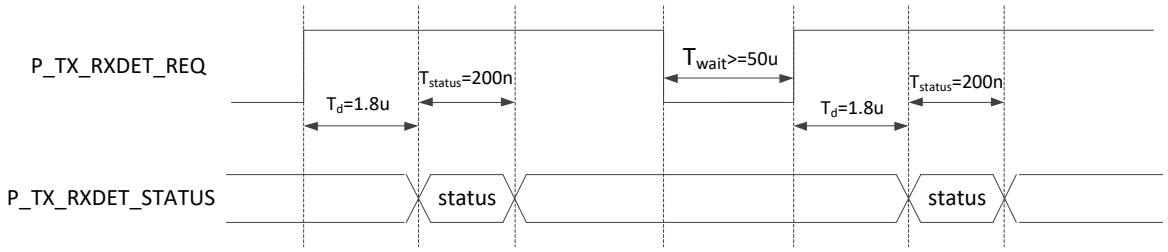

Figure 3-10 Timing Diagram of Load Detection at Transmitter

3.5 PCS Receiver Function

3.5.1 RX Sample Reg Module

Completes the data bridging from PMA Receiver to PCS Receiver, ensuring interface timing.

The RX Sample Reg module can implement polarity inversion of the received serial data through the configuration port signal PCS_RX_POLARITY_INV[0]. Enabling polarity inversion can compensate for the defect where HSST data receiving ports P_RX_SDP and P_RX_SDN are incorrectly swapped in the PCB.

Through the parameter PCS_RX_POLARITY_INV[1], the RX Sample Reg module also supports bit order inversion of parallel data based on the PMA and PCS interfaces. When bit order inversion is enabled, the received data from PMA Receiver to PCS Receiver is inverted in bit order, that is:

For valid data of 8 bits, the inverted bit order data is

"data_out[7:0]={data_in[0],data_in[1]...,data_in[7]} "

3.5.2 Word Alignment Module

The main function of the Word Alignment module is to implement byte alignment according to a predefined pattern. For example, with a 10-bit data width, the parallel data of transmitter is treated as one byte of 10 bits. After serial transmission, its byte boundary information is lost, so the parallel data produced after serial-to-parallel conversion in the PMA does not follow byte boundary rules. As shown in the following figure, before byte alignment, the default bytes of parallel data (Before Word Alignment) may be in a form where several bits of the source data have been slipped, with the number of slipped bits being random. The Word Alignment module utilizes certain characteristics of the data stream itself to implement byte alignment, reverting it to the boundary consistent with the transmitter (see After Word Alignment in the figure).

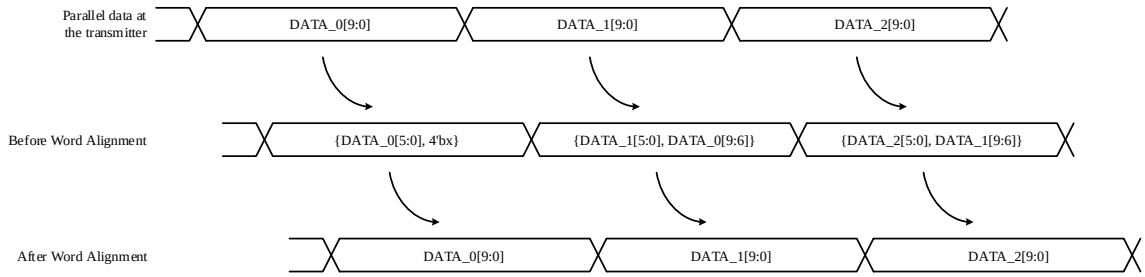

Figure 3-11 Description of Word Alignment Function

HSST supports two byte alignment modes: a Comma-based detection byte alignment mode and an RX CLK Slip-based byte alignment mode. User logic selects the byte alignment mode through the Parameter PCS_COMMA_DET_MODE.

In the Comma-based detection byte alignment mode, Parameter PCS_COMMA_REG0 and PCS_COMMA_REG1 are used to specify the Comma detection pattern. For example, for K28.5 in the 8B10B Special Data Group, PCS_COMMA_REG0/1 can be set to 10'b0101_1111_00 and 10'b1010_0000_11. The Parameter PCS_COMMA_MASK is used to mask the corresponding bits of Parameter PCS_COMMA_REG0/1, thereby generating a Comma of less than 10 bits. In this mode, once the specified Comma is detected, the byte boundary adjustment is automatically completed.

In the RX CLK Slip-based byte alignment mode, the byte boundary adjustment is implemented in the PMA Deserializer.

Byte alignment often requires a state machine to control the byte boundary adjustment to avoid incorrect adjustments due to line error code. HSST supports internal Link State Machine or external Link State Machine. The supported internal Link State Machines include:

- 1Gb Ethernet Link State Machine (802.3 "Figure 36–9—Synchronization state diagram")
- 10Gb Ethernet Link State Machine (802.3 "Figure 48–7—PCS synchronization state diagram")

- RapidIO Interconnect Specification Part 6 (Figure 4-15. LaneAlignment State Machine)

The byte alignment state machine is selected by configuring the Parameter PCS_ALIGN_MODE. In the Comma-based detection byte alignment mode: If the internal Link State Machine is chosen, HSST will automatically complete the byte alignment, and the result of the alignment is output through the port signal P_PCS_LSM_SYNCED; if the external Link State Machine is chosen, user logic can customize the Link State Machine, and enable byte realignment through the port P_PCS_WORD_ALIGN_EN.

3.5.3 8B10B Decoder Module

Implements the 8B10B Decode function in accordance with the IEEE 802.3 1000BASE-X specification, see IEEE Std802.3 36.2 Physical Coding Sublayer (PCS) for details.

3.5.4 Channel Bonding Module

The main function of the Channel Bonding module is to implement byte alignment among multiple channels according to a predefined pattern. When using the Bonding function, HSST needs to be able to transmit and receive data properly.

When multi-channel data is transmitted, the bytes between its channels are aligned. After parallel-to-serial conversion at the transmit side, serial transmission on the board, serial-to-parallel conversion at the receive side, and being processed by the Word Alignment module, the bytes between channels are no longer aligned. As shown in the figure below, before channel bonding, there may be a skew of several bytes between the data of the channels. The Channel Bonding module leverages certain characteristics of the data stream itself to implement byte alignment between channels, reverting it to the boundary consistent with the transmitter (see After Channel Bonding in the figure).

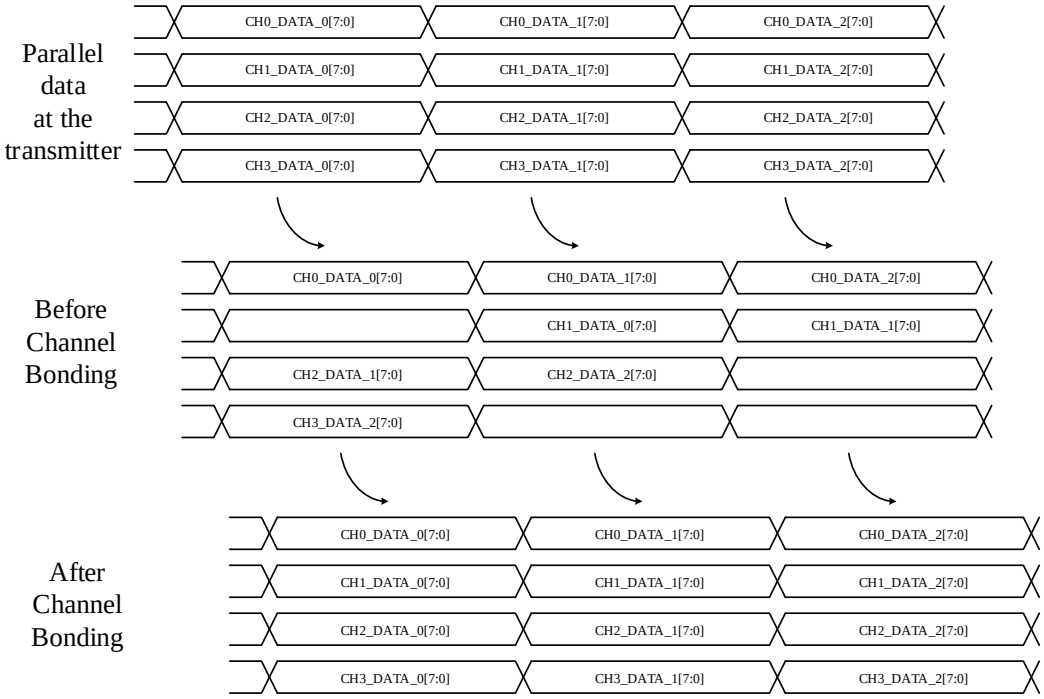

Figure 3-12 Channel Bonding Functional Diagram

Channel bonding is implemented by inserting the Special Codes into the data stream according to protocol requirements. Different protocols specify different Special Codes, which users can set by the Parameter PCS_A_REG.

The Logos HSST's channel bonding can implement bonding between 2 Channels or 4 Channels, with a maximum Deskew capability of +/-80 bits, meeting the requirements of the supported protocols. When two channels are bonded, only the bonding between Channel 0 and Channel 1 or between Channel 2 and Channel 3 is supported.

In order to avoid incorrect bonding adjustments due to line errors, channel bonding often requires a state machine to control. The HSST supports internal Bonding State Machine, or external Bonding State Machine. The supported internal Bonding State Machines include:

- Internal 10Gb XAUI Channel Bonding State Machine ("Figure 48–8 - PCS deskew state diagram")
- Internal Rapid IO Channel Bonding State Machine ("Figure 4-15. Lane Alignment State Machine")

The channel bonding state machine is selected via the Parameter PCS_CEB_MODE. If the internal Bonding State Machine is chosen, the HSST will automatically complete the related channel bonding, and the results will be output through the Bonding Master Channel signal P_PCS_RX_MCB_STATUS (with Channel 0/2 as the Bonding Master Channel for two-channel bonding; Channel 0 for four-channel bonding). If the external Bonding State Machine is chosen, user logic can customize control of the state machine; enable the bonding process through the port

P_PCS_MCB_EXT_EN.

3.5.5 CTC Module

The function of CTC (Clock Tolerance Compensation) module is to compensate for minor frequency difference between the far-end clock and the local clock according to a predefined pattern (the frequency error specified by the PCI Express protocol is +/-300ppm, and for other protocols, the number is typically +/-100ppm). The CTC module includes an asynchronous FIFO with a depth of 32, as shown in Figure 3-13, with the FIFO's write clock being CB_RCLK, which is derived from PMA_RCLK and has been synchronized to the far-end transmit clock in the CDR module; the FIFO's read clock is AFTER_CTC_RCLK, which is derived from the local clock.

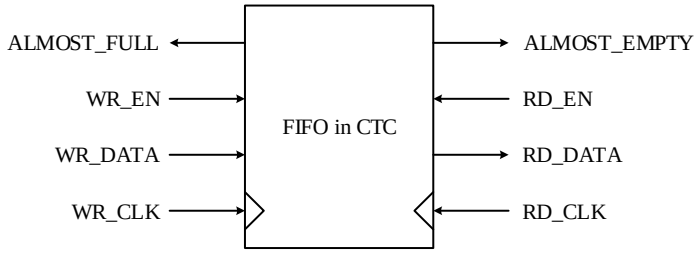

Figure 3-13 CTC Internal FIFO Diagram

When the write clock is faster than the read clock, the FIFO level will gradually rise, and once it reaches a certain level, the level flag signal ALMOST_FULL will be set high. At this point, the CTC will discard certain specific characters (or character sequences) before writing to the FIFO, thus preventing FIFO write full. The specific characters (or character sequences) referred to here are called SKIP. The details are shown in Figure 3-14.

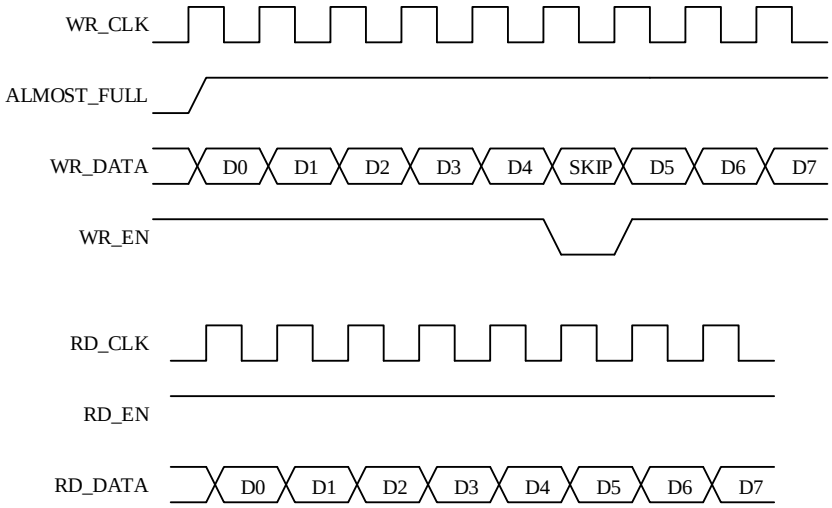

Figure 3-14 SKIP Delete Timing Diagram

When the write clock is slower than the read clock, the FIFO level will gradually decrease, and once it reaches a certain level, the level flag signal ALMOST_EMPTY will be set high. At this point, the CTC will pause FIFO reading upon detecting a specific character (or sequence of characters) and automatically insert a SKIP character to prevent FIFO read empty. The details are shown in Figure 3-15.

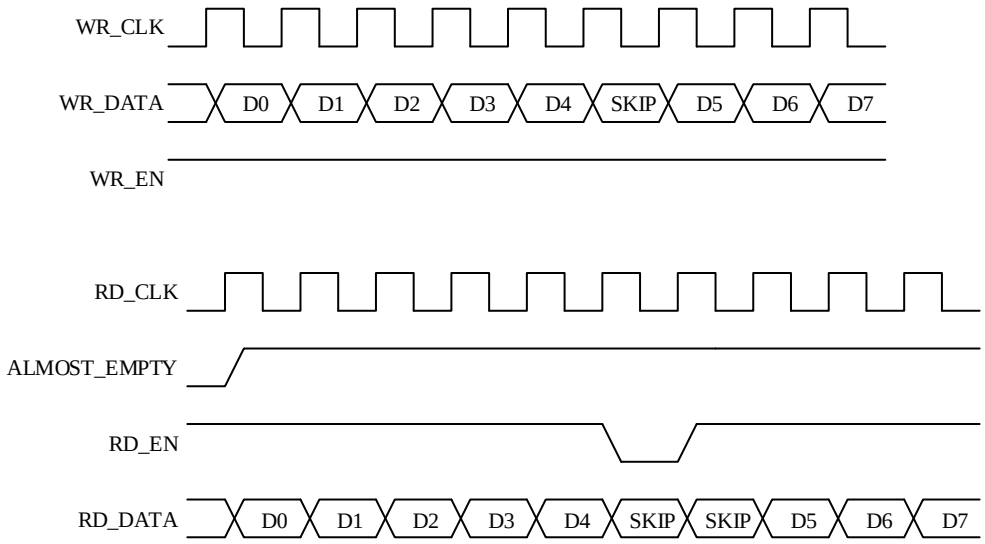

Figure 3-15 SKIP Add Timing Diagram

Different protocols define SKIP differently, and the CTC module in HSST supports three types of SKIP lengths (selected by the Parameter PCS_CTC_MODE):

- 1SKIP mode, set by Parameter PCS_SKIP_REG0, inserts/deletes a SKIP character of 1 byte;
- 2SKIP mode, set by Parameter PCS_SKIP_REG0 and PCS_SKIP_REG1, inserts/deletes SKIP characters of 2 bytes;
- PCIE_2BYTE mode, set by Parameter PCS_SKIP_REG0 and PCS_SKIP_REG1, only adds or deletes the subsequent SKIP;
- 4SKIP (PCIE_4BYTE) mode, set by Parameter PCS_SKIP_REG0, PCS_SKIP_REG1, PCS_SKIP_REG2, and PCS_SKIP_REG3. At this time, only the last byte of the SKIP sequence is inserted or deleted;

The Almost Full/Empty thresholds of the CTC FIFO can be modified according to application requirements, where: the Almost Full threshold is set by Parameter PCS_CTC_AFULL, to 5'd20 by default; the Almost Empty threshold is set by Parameter PCS_CTC_AEMPTY, to 5'd12 by default.

During the auto-negotiation of 1G Ethernet, both communicating parties continuously send /C/ characters, and no SKIP characters appear. Therefore, HSST will automatically replace some /C/ characters with two /I2/ characters before the CTC operation to facilitate the CTC process. Here, /I2/ will be used as the CTC's SKIP character, for detailed functions of /C/ and /I2/, please refer to

IEEE Std 802.3 36.2 Physical Coding Sublayer (PCS).

3.5.6 RX Gear Module

The RX gear module completes the interface rate adaptation in RX direction 64B66B or 64B67B. Supports two bit width modes for PCS and Fabric interfaces: 64B66B_16bit and 64B66B_32bit.

64B66B_16bit: Corresponds to 64B66B or 64B67B encoded data, with the Fabric interface width P_RDATA being 16bit;

64B66B_32bit: Corresponds to 64B66B or 64B67B encoded data, with the Fabric interface width P_RDATA being 32bit.

3.5.7 RX Bridge Unit Module

The RX Bridge unit module completes phase compensation from AFTER_CTC_RCLK to BRIDGE_RCLK, with a FIFO depth of 8.

3.5.8 RX Bridge Reg Module

Completes the receipt data bridging from HSST to Fabric, ensure interface timing. Each Lane's data receiving port P_RDATA has 47 bits, with definitions varying according to different bit width modes, see Table 3-6:

Table 3-6 Lane Receipt Data Definitions

	P_RDATA_x Data Bit																				
Data Width Mode	[46:44]	[43]	[42]	[41]	[40:39]	[38]	[37:33]	[32]	[31]	[30]	[29:22]	[21]	[20]	[19]	[18:17]	[16]	15:11	[10]	[9]	[8]	[7:0]
8bit only	RX STATUS	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	RXD [7:0]
10bit only	RX STATUS	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	RXD [9:0]		
8b10b 8bit	RX STATUS	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	RXK	RDEC_ER	RDISP_ER	RXD [7:0]
16bit only	RX STATUS	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	RXD [15:10]		NA	RXD [9:0]		
20bit only	RX STATUS	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	RXD [19:10]					NA	RXD [9:0]		
8b10b 16bit	RX STATUS	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	RXK [1]	RDEC_ER [1]	RDISP_ER [1]	RXD [15:8]			RXK [0]	RDEC_ER [0]	RDISP_ER [0]	RXD [7:0]
32bit only	RX STATUS	NA	NA	NA	NA	RXD [31:26]		NA	RXD [25:16]			NA	NA	NA	NA	RXD [15:10]		NA	RXD [9:0]		
40bit only	RX STATUS	NA	RXD [39:30]					NA	RXD [29:20]			NA	RXD [19:10]					NA	RXD [9:0]		
8b10b 32bit	RX STATUS	RXK [3]	RDEC_ER [3]	RDISP_ER [3]	RXD [31:24]			RXK [2]	RDEC_ER [2]	RDISP_ER [2]	RXD [23:16]	RXK [1]	RDEC_ER [1]	RDISP_ER [1]	RXD [15:8]			RXK [0]	RDEC_ER [0]	RDISP_ER [0]	RXD [7:0]
64b 66b 16bit	RX STATUS	NA										RXQ_START	RXH VLD	RXH[2:0]		RXD VLD	RXD[15:0]				
64b 66b 32bit	RX STATUS	NA					RXD[31:16]					RXQ_START	RXH VLD	RXH[2:0]		RXD VLD	RXD[15:0]				

Wherein, the definition of the data bits is shown in Table 3-6:

Table 3-7 Definitions of Data Bits in P_RDATA_x

Data Bit Name	Description
RXK	1 indicates that RXD is the 8B10B Special Code-Groups according to IEEE 802.3 1000BASE-X Specification; 0 indicates that RXD is the 8B10B Data Code-Groups according to IEEE 802.3 1000BASE-X Specification;
RXD	Code-Groups
RDEC_ER	A high level indicates that the 8B10B Decoder has detected an invalid code
RDISP_ER	A high level indicates that the 8B10B Decoder has detected an Invalid Disparity
RXSTATUS	Reception status encoding for the PCI Express PHY Interface (PIPE) 3'b000: Normal 3'b001: The CTC module executed a SKIP add operation 3'b010: The CTC module executed a SKIP delete operation 3'b011: PCIe 4byte mode, perform continuous deletion 3'b101: CTC FIFO write full 3'b110: CTC FIFO read empty 3'b100, 3'b111: Reserved
RXQ_START	RXsequence start indicator in 64B66B mode
RXH	RX_header Sync header in 64B66B/64B67B mode
RXHVLD	Valid indicator of RX_header Sync header in 64B66B/64B67B mode
RXDVLD	Valid indicator of RX_data reception data in 64B66B/64B67B mode

3.5.9 PRBS Checker Module

The PRBS Checker module is responsible for the automated detection of various feature code streams, commonly used for HSST line error code testing. Users can select the required feature code stream by the Parameter PCS_RX_PRBS_MODE. The supported options include:

Table 3-8 PRBS Checker Pattern

PCS_RX_PRBS_MODE	**Feature Code Stream**
"PRBS_7"	Generates random numbers based on the polynomial 1 + X6 + X7
"PRBS_15"	Generates random numbers based on the polynomial 1 + X14 + X15
"PRBS_23"	Generates random numbers based on the polynomial 1 + X18 + X23
"PRBS_31"	Generates random numbers based on the polynomial 1 + X28 + X31

The error count detected by the PRBS Checker can be obtained by reading the configuration register PCS_ERR_CNT, and user logic can clear the error counter by the register PCS_RX_ERRCNT_CLR.

3.6 PMA Receiver Function

3.6.1 Receiver Front-end Module

The RX receiver is a differential current mode input, including the following features:

- Configurable AC or DC coupling.
- Configurable RX termination voltage;
- Adjustable matching resistor;

HSST can be configured in four modes: external AC/internal DC (default mode), external AC/internal AC, external DC/internal AC, external DC/internal DC. It is recommended to use external AC coupling (externally connected coupling capacitor)/internal DC coupling. For the RX side, pins not used in the external AC/internal DC mode should be left floating, pins not used in the external DC/internal DC mode should be connected to an external grounding resistor, and pins not used in external AC/internal AC and external DC/internal AC modes can be connected to a grounding resistor or left floating;

Note: When using external DC coupling, the TX voltage at opposite side should be 1.2V.

The structure is shown in Figure 3-16.

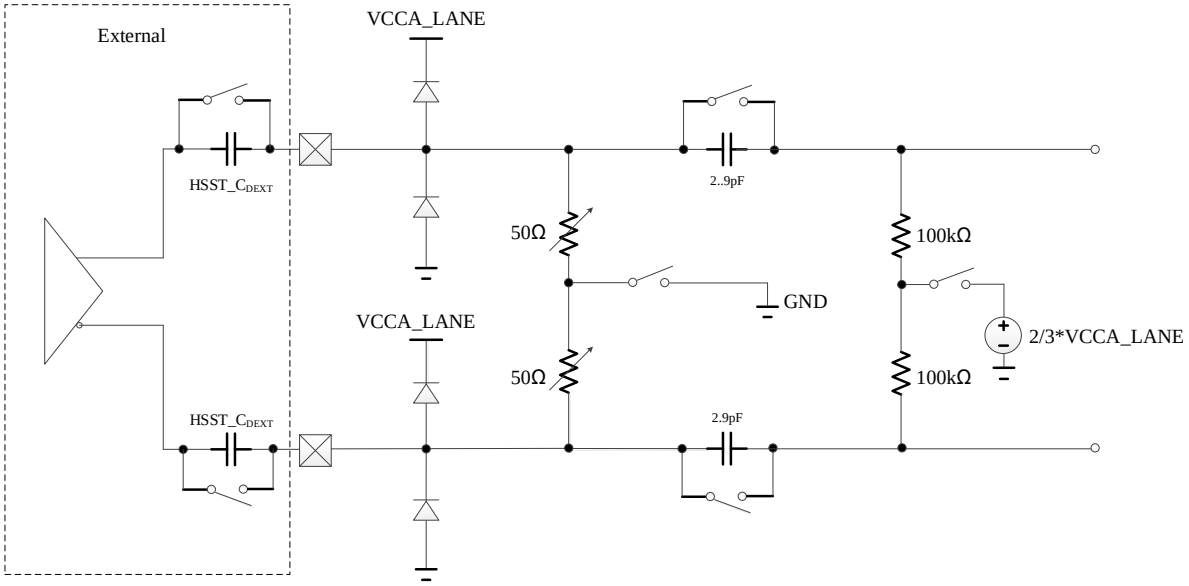

Figure 3-16 RX Receiver Structure Diagram

The RX termination voltage is automatically configured according to the coupling method, see Figure 3-17, Figure 3-18, Figure 3-19, Figure 3-20 for specific forms; users need to choose the coupling method according to the actual scenario.

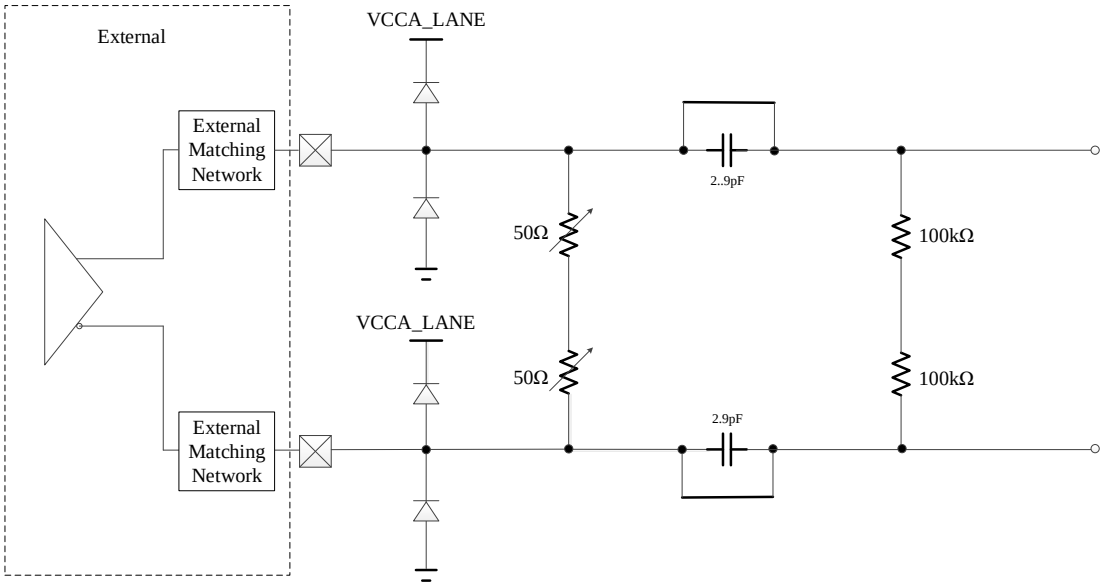

Figure 3-17 External DC/Internal DC Mode Diagram

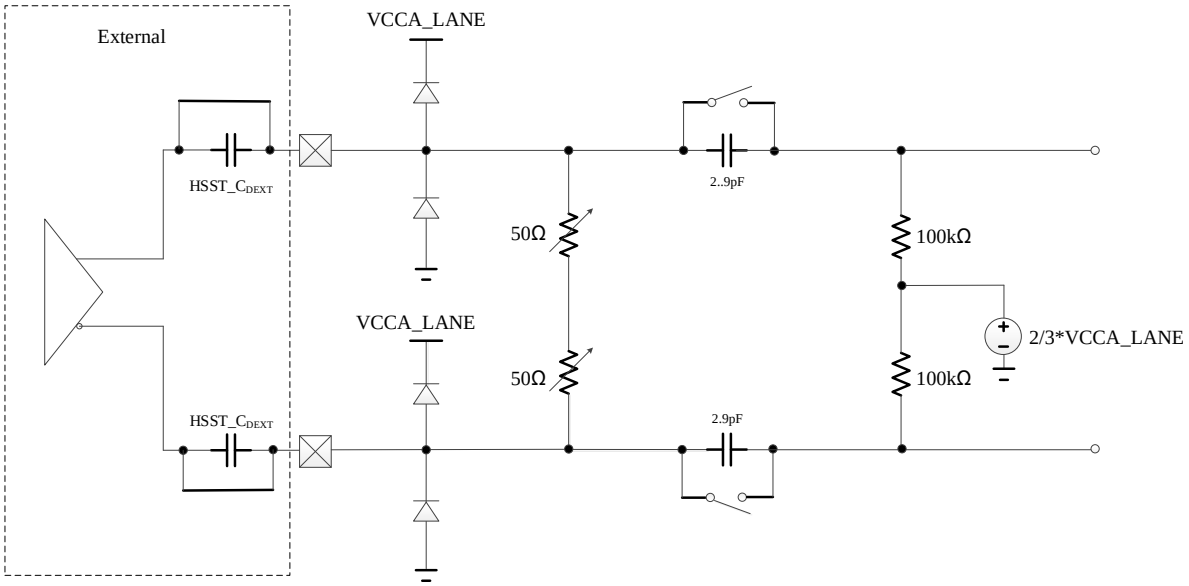

Figure 3-18 External DC/Internal AC Mode Diagram

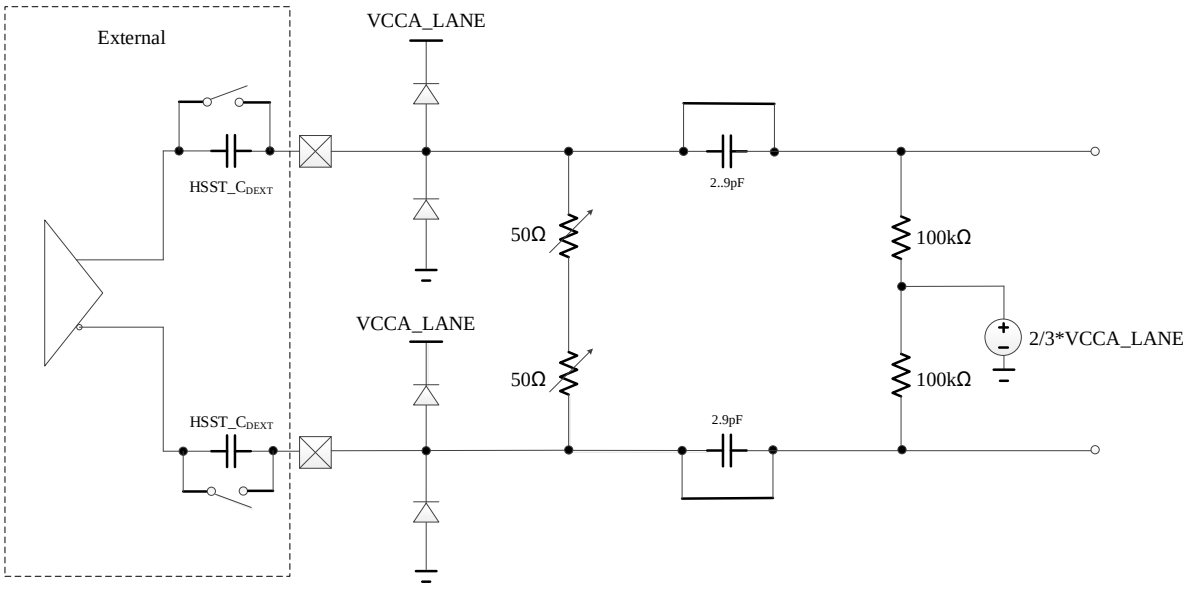

Figure 3-19 External AC/Internal DC Mode Diagram

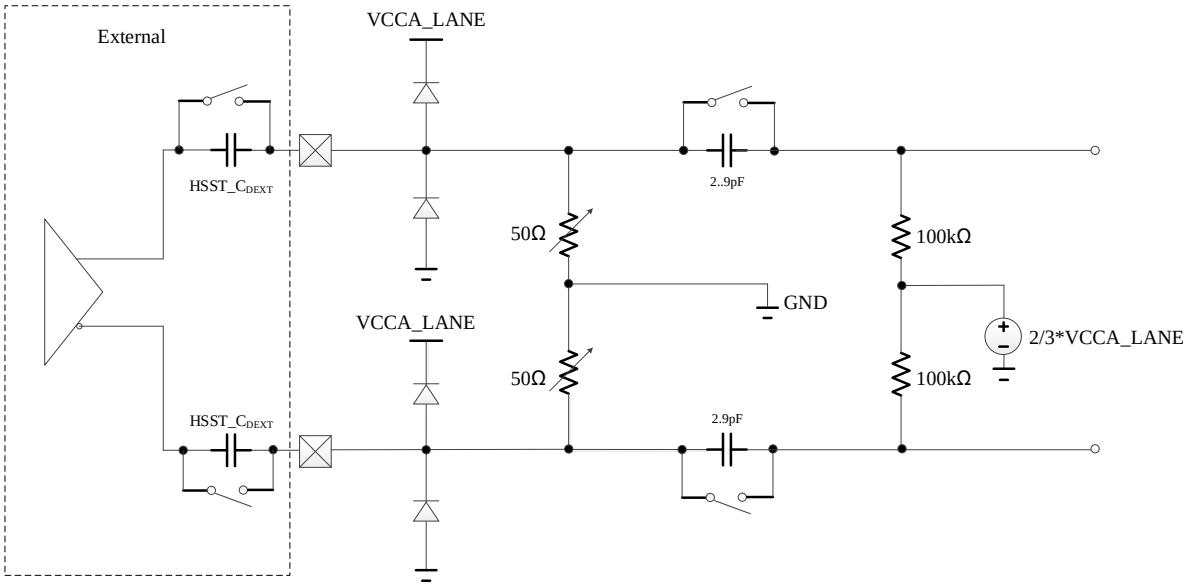

Figure 3-20 External AC/Internal AC Mode Diagram

3.6.2 LEQ Module

The LEQ (Linear Equalizer) module is an adaptive linear equalizer at the receiver, used to compensate for high-frequency losses in the received signal. For 3.125Gbps and below, the LEQ can support approximately 6dB of channel attenuation compensation (at the Nyquist frequency point). Above 3.125Gbps, the LEQ can support approximately 5dB of channel attenuation compensation (at the Nyquist frequency point).

3.6.3 CDR Module

The main function of the CDR is to recover clock information from the data, thereby restoring the correct data. The RX's CDR is based on a phase interpolation architecture, with its clock source being derived from the common PLL. After passing through the LEQ, the data goes through edge samplers and data samplers, with the sampler's clock being derived from the PI's output. The two sets of data are then processed in the CDR state machine after DEMUX processing. The CDR state machine determines the phase information by comparing the edge signal and the data signal, and then outputs control signals to control the clock, ultimately aligning the sampling clock of the data signal to the middle of the data.

3.6.4 LOS Detect Module

LOS Detect is used to detect whether there is a valid signal at the receiving port, and the result is

transmitted to the Fabric through the P_RX_SIGDET_STATUS port.

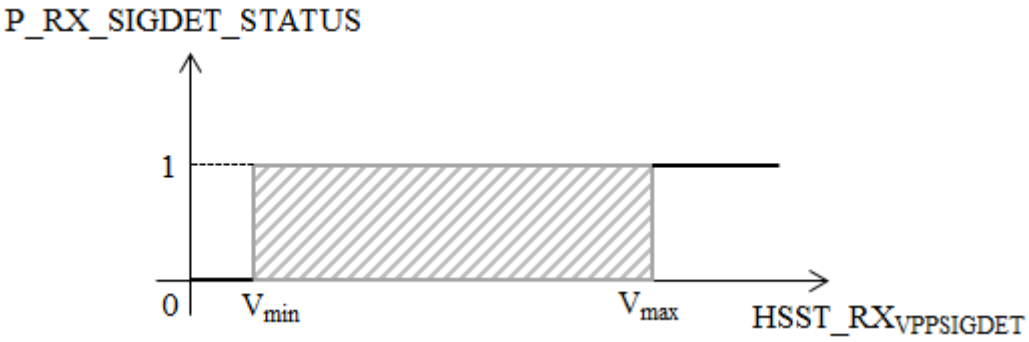

Figure 3-21 P_RX_SIGDET_STATUS Signal Diagram

As shown in Figure 3-21, when the voltage of the received signal is lower than V_{min}, P_RX_SIGDET_STATUS is low, indicating that the LOS Detect module has not detected a valid signal from the port; when the voltage of the received signal is higher than V_{min} and less than V_{max}, P_RX_SIGDET_STATUS is in a indeterminate state; when the voltage of the received signal is greater than V_{max}, P_RX_SIGDET_STATUS is high, indicating that the LOS Detect module has detected a valid signal from the port. It is necessary to control the link noise not to exceed V_{min}. If the link noise exceeds V_{min}, it may cause the noise to be recognized as a valid signal, thus affecting the application.

For specific values of V_{max} and V_{min}, please refer to the "High-Speed Serial Transceiver (HSST) AC Characteristics" section in the ***"DS02001_Logos Family FPGAs Datasheet"***, under the "$HSST\_RX_{VPPSIGDET}$" parameter.

3.6.5 Deserializer Module

The main function of the Deserializer is to convert PMA's high-speed serial data into 20 bits of parallel data to be sent to RX Digital. Here, the 20 bits refer to the parallel bit width between the PMA Receiver and the PCS Receiver, which is part of the HSST internal interface, with lower bits first out during the serial-to-parallel conversion. The effective bit width of the RX parallel data is controlled by the parameter PMA_REG_RX_BUSWIDTH, and their correspondence is as follows:

Table 3-9 Correspondence between RX Parallel Data Effective Bit Width and Register PMA_REG_RX_BUSWIDTH

PMA_REG_RX_BUSWIDTH	**RX Parallel Data Effective Bit Width**	**Output data**
2'b00	8bit	pma_rxd<7:0> parallel output, higher data bits invalid
2'b01	10bit	pma_rxd<9:0> parallel output, higher data bits invalid

PMA_REG_RX_BUSWIDTH	RX Parallel Data Effective Bit Width	Output data
2'b10	16bit	pma_rxd<17:10>, pma_rxd<7:0> parallel output, other data bits invalid
2'b11	20bit	pma_rxd<19:0> parallel output

Additionally, the Deserializer module supports the RX CLK Slip function to ensure a fixed receive delay. In the circuit, this is achieved through the PMA_REG_RXPCLK_SLIP register. Each time there is a rising edge of the PMA_REG_RXPCLK_SLIP signal, the PMA's parallel output clock PMA_RCLK will be delayed one UI. If multiple UIs need to be delayed, there must be an equivalent number of rising edges on the PMA_REG_RXPCLK_SLIP signal. The maximum UI delay depends on the bit width of the parallel data (for example, if the bit width is N, then the parallel clock can move by up to N-1 UIs). The pulse duration of PMA_REG_RXPCLK_SLIP must be at least 20 UIs to ensure the correct response of the circuit.

3.6.6 RX Digital Module

The RX Digital module mainly completes the data bridging from the PMA Receiver to the PCS Receiver, including the following functions:

- Processing of the received control signals;
- PRBS checker;
- Implements PMA far-end parallel loopback;
- Reception data error injection;
- Signal detect, OOB detect;

3.7 Loopback Function

HSST supports multiple loopback modes for testing, including PCS near-end loopback, PMA near-end parallel loopback, PMA near-end serial loopback, PMA far-end parallel loopback, and PCS far-end loopback.

Both the PCS layer and the PMA layer have PRBS code transmission and verification modules, with the transmission modules supporting error injection functions. Note that the PRBS code transmission and verification modules should be used in conjunction, otherwise the verification results may not match the actual values. That is, if the transmission occurs at PCS layer, then verify at the PCS layer; if the transmission occurs at PMA layer, then verify at the PMA layer; the same rules apply to error injection.

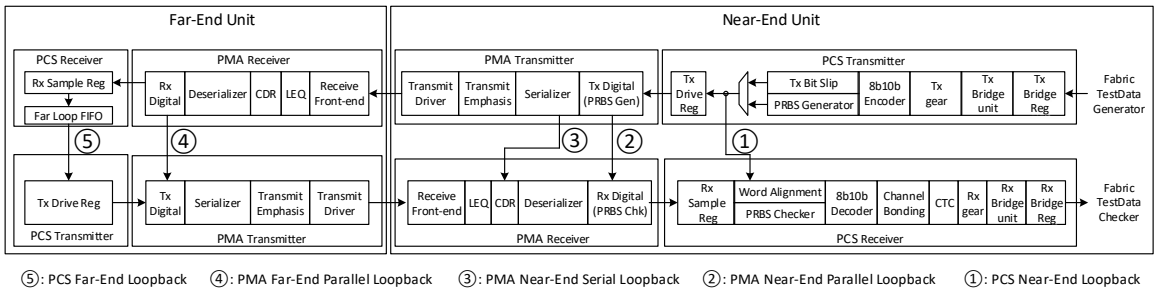

Figure 3-22 HSST Loopback Mode Data Path Overview

3.7.1 PCS Near-End Loopback

PCS near-end loopback is implemented within the PCS, where data transmitted from the Fabric passes through the TX Bit Slip module in the PCS Transmitter, loops back to the Word Alignment module, and then loops back out to the Fabric through the PCS Receiver's RX Bridge Reg module, as shown in Figure 3-23.

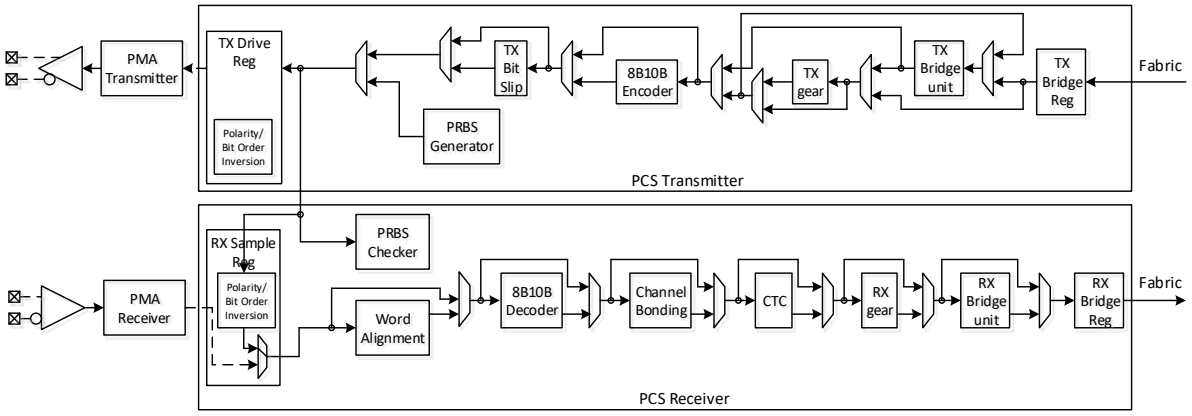

Figure 3-23 PCS Near-End Loopback Data Path Diagram

The register configuration method for PCS near-end loopback is as follows:

- PCS_NEAR_LOOP="TRUE"

3.7.2 PMA Near-End Parallel Loopback

PMA near-end parallel loopback is implemented in the PMA, where parallel data from the PCS Transmitter passes through the PMA TX Digital module, loops back to the PMA RX Digital module, and finally loops back to the PCS, as shown in Figure 3-24.

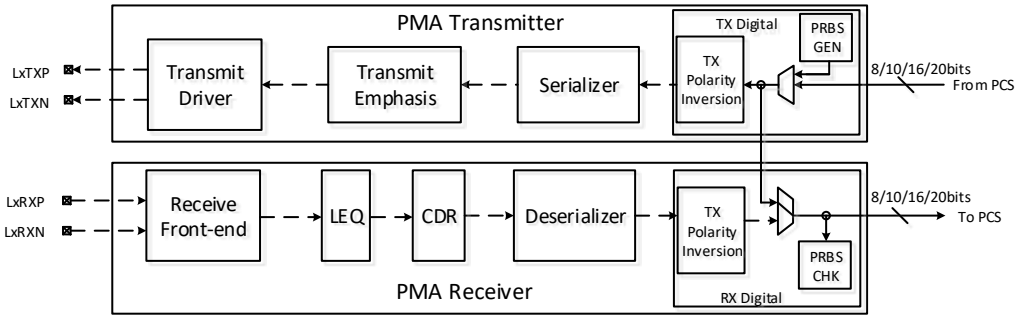

Figure 3-24 PMA Near-End Parallel Loopback Data Path Diagram

The register configuration method for PMA near-end parallel loopback is as follows:

- PMA_REG_RX_TX2RX_PLPBK_EN="TRUE"

3.7.3 PMA Near-End Serial Loopback

PMA near-end serial loopback is implemented in the PMA, where parallel data from the PCS Transmitter goes through parallel-to-serial conversion, loops back to the PMA Receiver's CDR module, and finally loops back to the PCS through serial-to-parallel conversion, as shown in Figure 3-25.

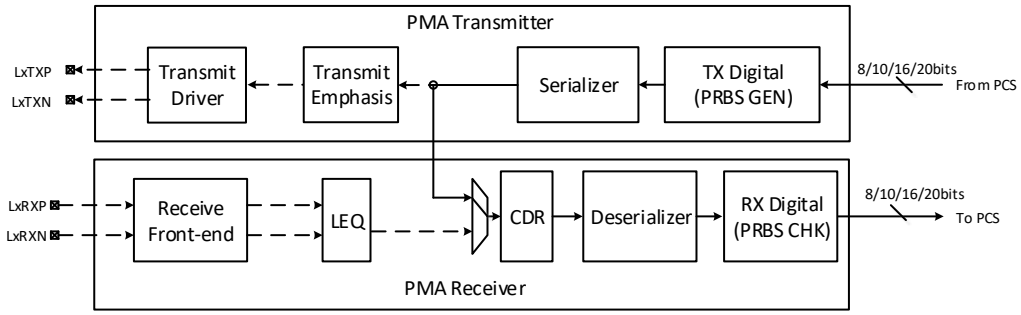

Figure 3-25 PMA Near-End Serial Loopback Data Path Diagram

The register configuration method for PMA near-end serial loopback is as follows:

- PMA_REG_TX_TX2RX_SLPBACK_EN="TRUE"

3.7.4 PMA Far-End Parallel Loopback

PMA far-end parallel loopback is implemented in the PMA, where the received data is sampled and converted to parallel data, then passes through the PMA RX Digital module, loops back to the PMA TX Digital module, and finally loops back out through PMA, as shown in Figure 3-26.

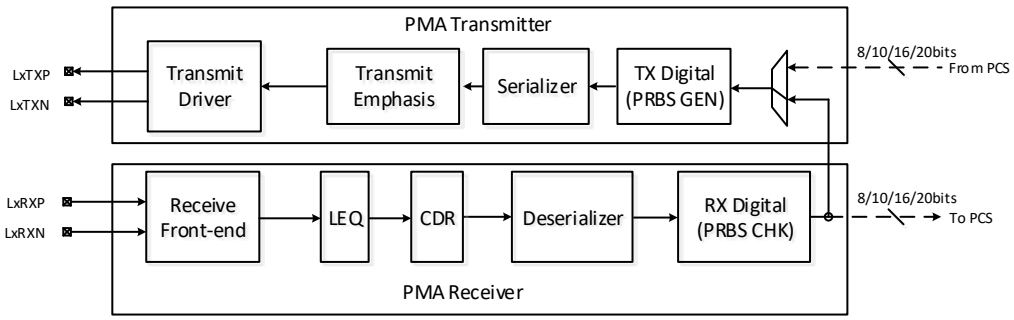

Figure 3-26 PMA Far-End Parallel Loopback Data Path Diagram

The register configuration method for PMA far-end parallel loopback is as follows:

- PMA_REG_TX_DATA_MUX_SEL=3
- PMA_REG_TX_FIFO_EN="TRUE"
- PMA_REG_PLPBK_TXPCLK_EN="FALSE"

3.7.5 PCS Far-End Loopback

PCS far-end parallel loopback is implemented within the PCS. In this mode, the received data is sampled by the PMA and converted into parallel data. After passing through the RX Sample Reg module, it loops back to the TX Drive Reg module via an asynchronous FIFO with a depth of 8 (used to compensate for phase differences between PCS_RCLK and PCS_TCLK), and then loops back out through the PMA. The data path is shown in Figure 3-27.

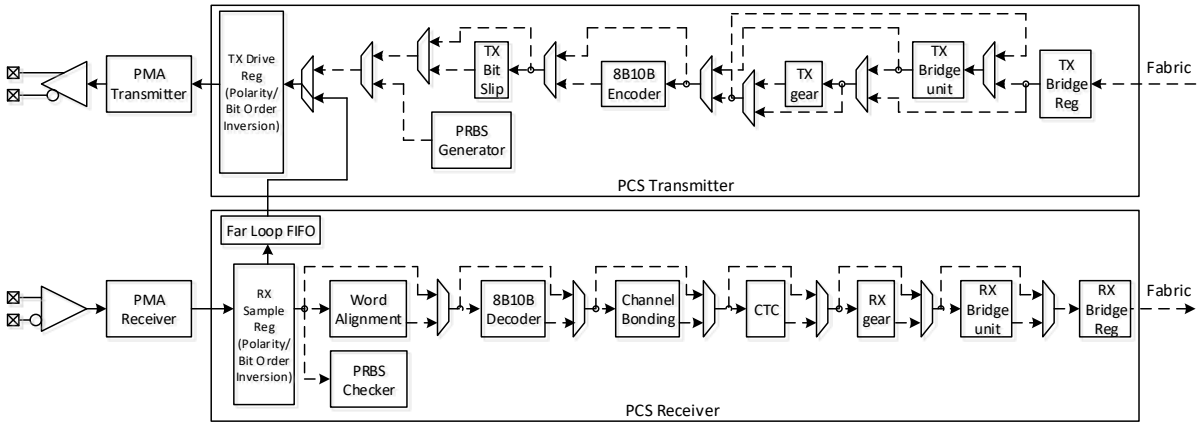

Figure 3-27 PCS Far-End Loopback Data Path Diagram

The register configuration method for PCS far-end loopback is as follows:

- PCS_FAR_LOOP="TRUE"
- PMA_REG_PLPBK_TXPCLK_EN="FALSE"
- PCS_CB_RCLK_SEL="PMA_TCLK"

Chapter 4 Power-Up Reset Timing of HSST

This chapter provides Power-up Reset timing diagrams for the PLL, transmit direction, and receive direction. Users can use the reset module code provided in the IP to meet the Power-up Reset timing requirements. When directly calling GTP_HSST_E2, users need to design the reset module themselves.

4.1 PLL Power-up Reset Timing Diagram

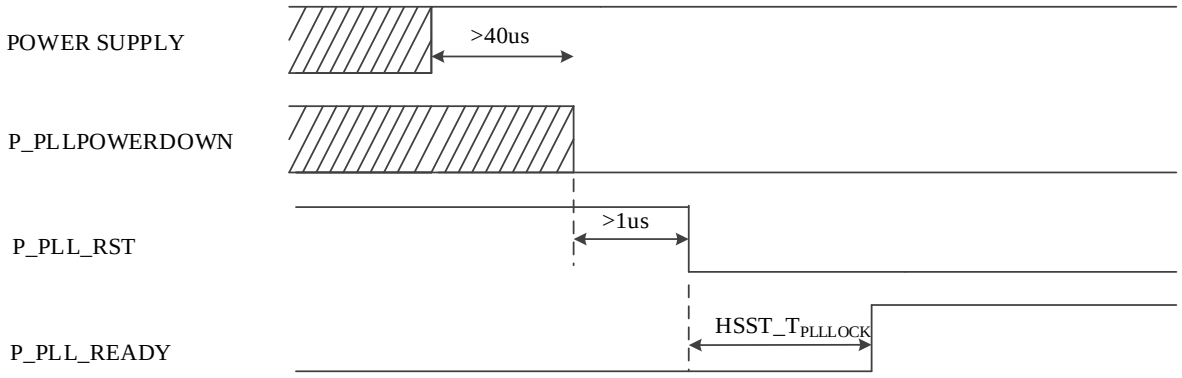

Figure 4-1 PLL Power-up Reset Timing Diagram

In the first stage, after the power stabilizes for more than 40μs, P_PLLPOWERDOWN must remain low.

In the second stage, wait for at least 1μs, then unreset the P_PLL_RST port.

In the third stage, wait for the P_PLL_READY port to become high, which indicates the PLL is phase-locked. The maximum PLL lock time is HSST_$T_{PLLLOCK}$.

For specific values and descriptions of HSST_$T_{PLLLOCK}$, please refer to the "High-Speed Serial Transceiver HSST AC Characteristics" section in the ***"DS02001_Logos Family FPGAs Datasheet"***.

During normal operation, if P_PLLPOWERDOWN is kept low, only P_PLL_RST needs to be operated to reset the PLL.

4.2 Timing Diagram of Power-up Reset in Transmit Direction

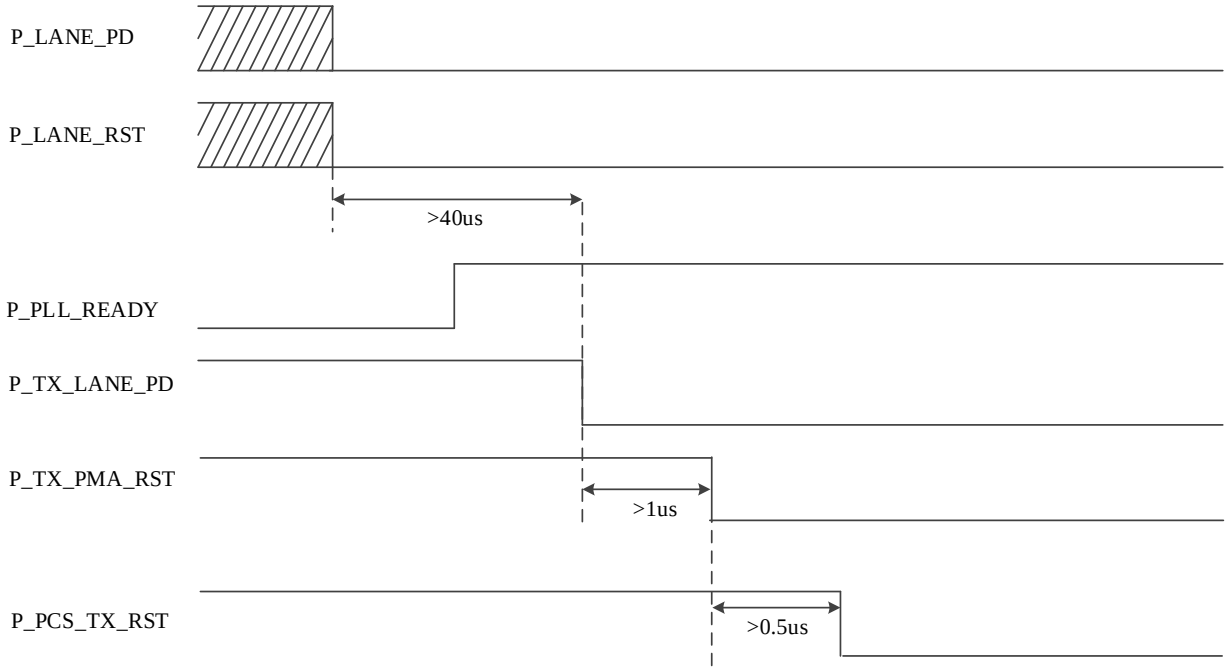

Figure 4-2 Timing Diagram of Power-up Reset in Transmit Direction

In the first stage, when P_LANE_PD and P_LANE_RST are low and last for at least 40μs, control whether P_TX_LANE_PD transitions from high to low based on the state of P_PLL_READY; if P_PLL_READY is high, then P_TX_LANE_PD transitions from high to low; if it is low, then wait.
In the second stage, after P_TX_LANE_PD becomes low, P_TX_PMA_RST needs to wait for more than 1μs before releasing (i.e., transitioning from high to low).
In the third stage, after P_TX_PMA_RST becomes low, P_PCS_TX_RST needs to wait for more than 0.5μs before releasing (i.e., transitioning from high to low).

4.3 Timing Diagram of Dynamic Rate Switching in Transmit Direction

The synchronous timing for dynamic rate switching in transmit direction by changing P_TX_RATE is as shown in Figure 4-3. In the diagram, PCIe_EI is the indicator of PCI Express electrical_idle, which includes PCIe_EI_H and PCIe_E1_L, defined by bits P_TDATA[45:44]. During synchronous timing control, PCIe_E1_H and PCIe_E1_L both produce the same PCIe_EI control timing.

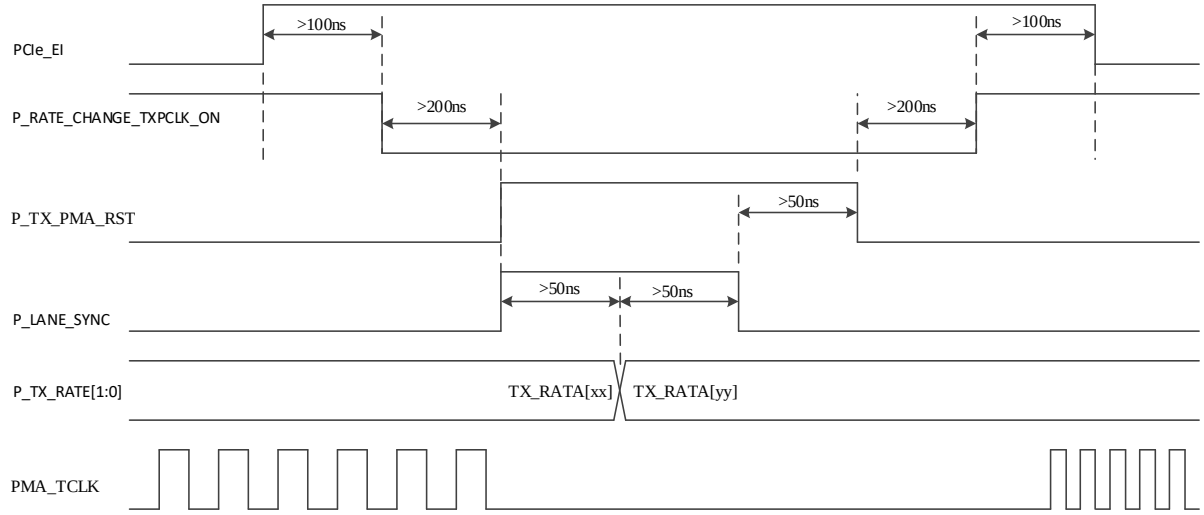

Figure 4-3 Timing Diagram of Dynamic Rate Switching in Transmit Direction

PMA_TCLK is the parallel clock of the PMA TX output.

When the dynamic rate switching in transmit direction is performed by changing P_TX_RATE, the PLL will not be out of lock, so there is no need to reset P_PCS_TX_RST again.

If it is necessary to implement transmit direction rate switching by modifying PLL configuration parameters (changing VCO frequency), then the PLL must be reset first, followed by resetting the transmitter.

For the content about dynamic rate switching, please refer to Section 3.2 PLL Function.

4.4 Timing Diagram of Power-up Reset in Receive Direction

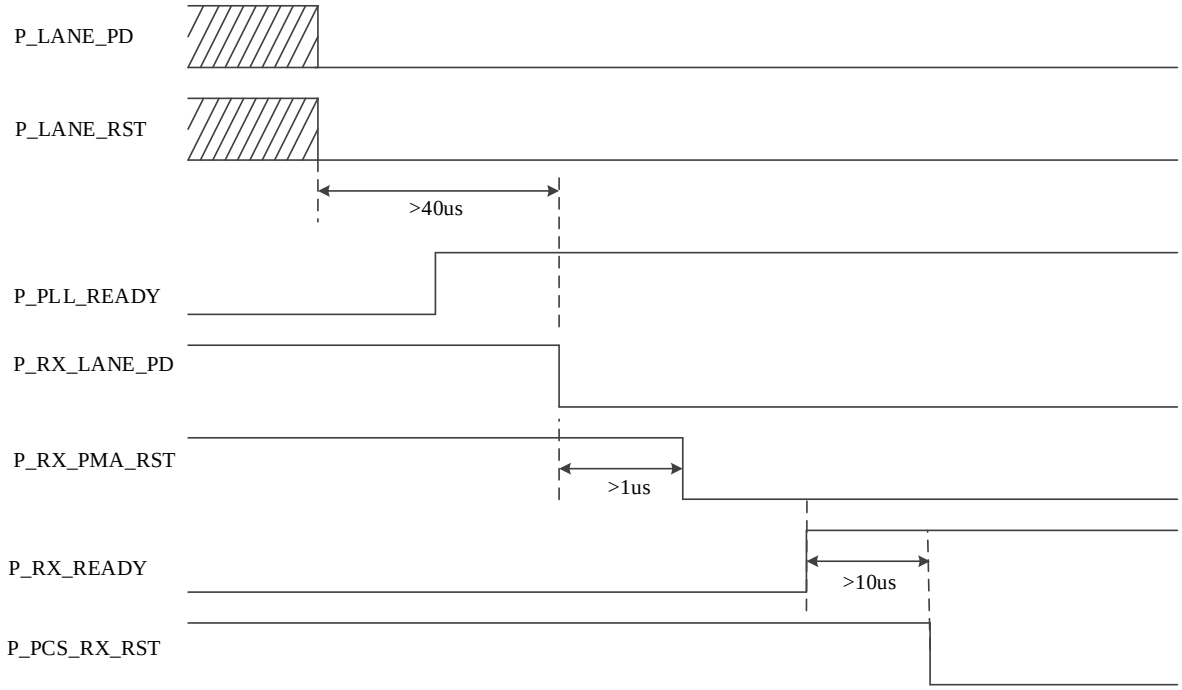

Figure 4-4 Timing Diagram of Power-up Reset in Receive Direction

In the first stage, when P_LANE_PD and P_LANE_RST are low and last for at least 40μs, control whether P_RX_LANE_PD transitions from high to low based on the state of P_PLL_READY; if P_PLL_READY is high, then P_RX_LANE_PD transitions from high to low; if it is low, then wait.

In the second stage, after P_RX_LANE_PD becomes low, P_RX_PMA_RST needs to wait for more than 1μs before releasing (i.e., transitioning from high to low).

In the third stage, after P_RX_READY becomes low, P_PCS_RX_RST needs to wait for more than 10μs before releasing (i.e., transitioning from high to low).

When RX is powered down during normal operation, it requires at least 40μs to ensure all modules are turned off.

4.5 Timing Diagram of Dynamic Rate Switching in Receive Direction

The synchronous timing for dynamic rate switching in receive direction by changing P_RX_RATE is as shown in Figure 4-5.

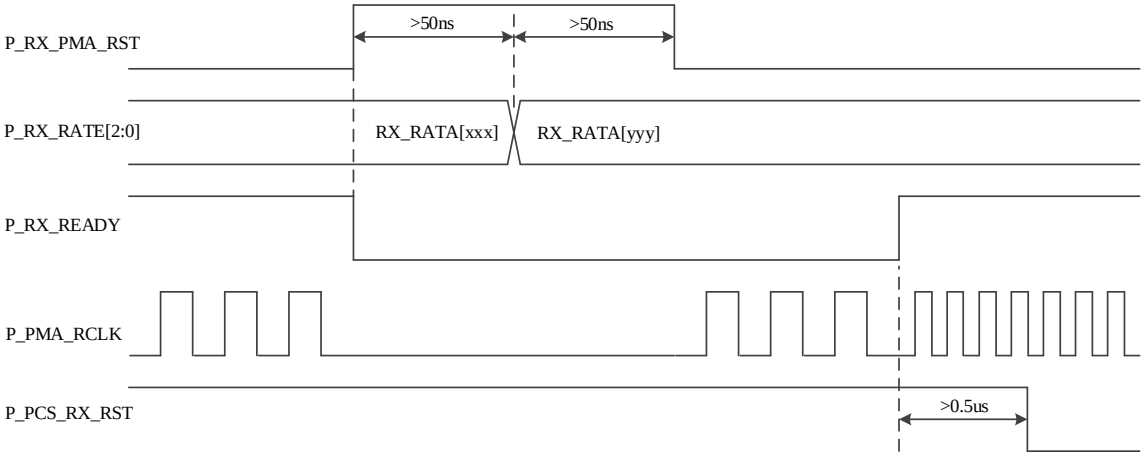

Figure 4-5 Timing Diagram of Dynamic Rate Switching in Receive Direction

PMA_RCLK is the parallel clock of PMA RX output.

When the dynamic rate switching in receive direction is performed by changing P_RX_RATE, it involves CDR re-locking, so P_PCS_RX_RST needs to be reset again.

If it is also necessary to switch the receiver direction rate by modifying PLL configuration parameters (changing the VCO frequency), then the PLL must be reset before resetting the receiver.

For the content about dynamic rate switching, please refer to Section 3.2 PLL Function.

Chapter 5 HSST Register Description

Use APB bus to configure the registers of HSST, and the configuration registers can support read-back. The bus data width is 8 bits, and the bus address width is 16 bits. Register default values are based on IP parameters, and the register descriptions are for reference only.

Note: Do not modify the Reserved parameter values in the registers.

Each HSST contains 2 sets of PMA PLLs, 4 PCS LANEs, and 4 PMA LANEs, with the register address allocation for each channel as in the following table:

Table 5-1 HSST Configuration Register Address Allocation

Channel Module	Configuration Register Address Range
PMA PLL0	0x0000——0x0fff
PMA PLL1	0x1000——0x1fff
PCS LANE0	0x8000——0x8fff
PMA LANE0	0x9000——0x9fff
PCS LANE1	0xa000——0xafff
PMA LANE1	0xb000——0xbfff
PCS LANE2	0xc000——0xcfff
PMA LANE2	0xd000——0xdfff
PCS LANE3	0xe000——0xefff
PMA LANE3	0xf000——0xffff

5.1 PLL Configuration Register Descriptions

Table 5-2 PLL Configuration Register Description: pma_pll_reg0, Offset Address 0x000

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	LANE_SYNC	Reserved
6	R/W	LANE_SYNC_OW	Reserved
5	R/W	PLL_READY	1'b0: PLL not locked; 1'b1: PLL locked
4	R/W	PLL_READY_OW	1'b0: PLL ready controlled by port P_PLL_READY 1'b1: PLL ready controlled by register PLL_READY
3	R/W	PLL_RESET_N	1'b0: PLL reset; 1'b1: PLL not Reset
2	R/W	PLL_RESET_N_OW	1'b0: PLL reset controlled by internal circuit 1'b1: PLL reset controlled by register PLL_RESET_N
1	R/W	PLL_POWERDOWN	1'b0: Not powered off; 1'b1: Powered off
0	R/W	PLL_POWERDOWN_OW	1'b0: PLL power-off is controlled by port P_PMA_PLL_POWERDOWN 1'b1: PLL power-off is controlled by register PLL_POWERDOWN

Table 5-3 PLL Configuration Register Description: pma_pll_reg1, Offset Address 0x001

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R/W	RESCAL_DONE	Reserved
4	R/W	RESCAL_DONE_OW	Reserved
3	R/W	RESCAL_RESET_N	Reserved
2	R/W	RESCAL_RESET_N_OW	Reserved
1	R/W	RESCAL_I_CODE_PMA	Reserved
0	R/W	LOCKDET_REPEAT	Reserved

Table 5-4 PLL Configuration Register Description: pma_pll_reg2, Offset Address 0x002

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved
4:3	R/W	REG_BIAS_VCOREP_C	Reserved
2:1	R/W	REG_LDO_VREF_SEL	Reserved
0	R/W	REG_RESCAL_CODE_OW	Reserved

Table 5-5 PLL Configuration Register Description: pma_pll_reg3, Offset Address 0x003

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	REG_RESCAL_ONCHIP_SMALL	Reserved
6	R/W	REG_RESCAL_ONCHIP_SMALL_OW	Reserved
5:0	R/W	REG_RESCAL_I_CODE	Reserved

Table 5-6 PLL Configuration Register Description: pma_pll_reg4, Offset Address 0x004

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved
4:2	R/W	REG_JTAG_VHYSTSEL	Reserved
1	R/W	REG_JTAG_AC_MODE	Reserved
0	R/W	REG_JTAG_OE	Reserved

Table 5-7 PLL Configuration Register Description: pma_pll_reg5, Offset Address 0x005

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PLL_UNLOCKED_STICKY_CLEAR	Reserved
6	R/W	PLL_LOCKED_STICKY_CLEAR	Reserved
5	R/W	PLL_LOCKED	Reserved
4	R/W	PLL_LOCKED_OW	Reserved
3	R/W	PLL_LOCKDET_RESET_N	Reserved
2	R/W	PLL_LOCKDET_RESET_N_OW	Reserved
1	R/W	PLL_LOCKDET_EN	Reserved

Bits	R/W	Corresponding Parameter Name	Description
0	R/W	PLL_LOCKDET_EN_OW	Reserved

Table 5-8 PLL Configuration Register Description: pma_pll_reg6, Offset Address 0x006

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved
6:4	R/W	PLL_LOCKDET_FBCT	Reserved
3:1	R/W	PLL_LOCKDET_REFCT	Reserved
0	R/W	NOFBCLK_STICKY_CLEAR	Reserved

Table 5-9 PLL Configuration Register Description: pma_pll_reg7, Offset Address 0x007

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	PLL_UNLOCKDET_ITER	Reserved
5:3	R/W	PLL_LOCKDET_ITER	Reserved
2:0	R/W	PLL_LOCKDET_LOCKCT	Reserved

Table 5-10 PLL Configuration Register Description: pma_pll_reg8, Offset Address 0x008

Bits	R/W	Corresponding Parameter Name	Description
7:3	R/W	TEST_SEL	Reserved
2	R/W	REFCLK_TEST_EN	Reserved
1	R/W	FBCLK_TEST_EN	Reserved
0	R/W	PD_VCO	Reserved

Table 5-11 PLL Configuration Register Description: pma_pll_reg9, Offset Address 0x009

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PD_BGR	Reserved
6	R/W	BGR_STARTUP	Reserved
5	R/W	BGR_STARTUP_EN	Reserved
4	R/W	REFCLK_OUT_PD	1’b0: Enable refclk output buffer 1’b1: Disable refclk output buffer
3:2	R/W	TEST_FSM	Reserved
1	R/W	TEST_SIG_HALF_EN	Reserved
0	R/W	TEST_V_EN	Reserved

Table 5-12 PLL Configuration Register Description: pma_pll_reg10, Offset Address 0x00a

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R/W	RESET_N_PFDQP	Reserved
4	R/W	RESET_N_PFDQP_OW	Reserved
3:2	R/W	FBDIVB	Feedback divider B, corresponding to parameter

Bits	R/W	Corresponding Parameter Name	Description
			N2 in Section 3.2 "PLL Functions" 2’b00: 1/2; 2’b01: 1/5; 2’b10: 1/4
1	R/W	FBDIVA_5_EN	Feedback divider A div-5 enable, corresponding to parameter N1 in Section 3.2 "PLL Functions" 1'b0: 1/4; 1'b1: 1/5
0	R/W	REFCLK_TERM_VCM_EN	refclk terminal common-mode voltage selection register 1’b0: refclk terminal common-mode voltage selection input DC coupling 1’b1: refclk terminal common-mode voltage selection internal vcm

Table 5-13 PLL Configuration Register Description: pma_pll_reg11, Offset Address 0x00b

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved
4	R/W	VC_FORCE_EN	Reserved
3:0	R/W	QPCURRENT	Reserved

Table 5-14 PLL Configuration Register Description: pma_pll_reg12, Offset Address 0x00c

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved
4:0	R/W	VCRESET_C_RING	Reserved

Table 5-15 PLL Configuration Register Description: pma_pll_reg13, Offset Address 0x00d

Bits	R/W	Corresponding Parameter Name	Description
7:4	R/W	LPF_TR_C	Reserved
3:0	R/W	LPF_R_C	Reserved

Table 5-16 PLL Configuration Register Description: pma_pll_reg14, Offset Address 0x00e

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved
6:5	R/W	BIAS_LANE_SYNC	Reserved
4:3	R/W	BIAS_QP	Reserved
2:1	R/W	ICTRL_PLL	Reserved
0	R/W	PD_BIAS	Reserved

Table 5-17 PLL Configuration Register Description: pma_pll_reg15, Offset Address 0x00f

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	LANE_SYNC_EN_OW	Reserved
6	R/W	LANE_SYNC_EN	Reserved
5:4	R/W	BIAS_CLKBUFS3	Reserved

Bits	R/W	Corresponding Parameter Name	Description
3:2	R/W	TXPCLK_SEL	Reserved
1:0	R/W	BIAS_CLKBUFS1	Reserved

Table 5-18 PLL Configuration Register Description: pma_pll_reg16, Offset Address 0x010

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	BIAS_REFBUF_C	Reserved
5:4	R/W	BIAS_VCRST_C	Reserved
3:2	R/W	BIAS_REFD2S_C	Reserved
1:0	R/W	BIAS_D2S	Reserved

Table 5-19 PLL Configuration Register Description: pma_pll_reg17, Offset Address 0x011

Bits	R/W	Corresponding Parameter Name	Description
7:5	R/W	CLKBUFS3_C	Reserved
4:2	R/W	CLKBUFS2_C	Reserved
1:0	R/W	CLKBUFS1_C	Reserved

Table 5-20 PLL Configuration Register Description: pma_pll_reg18, Offset Address 0x012

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PLL_UNLOCKED	Register controls PLL lock status 1'b0:' PLL locked; 1'b1: PLL not locked
6	R/W	PLL_UNLOCKED_OW	1'b0: pll_unlocked is controlled by internal circuit 1'b1: pll_unlocked is controlled by register PLL_UNLOCKED
5	R/W	RESCAL_R_CODE_SIGN	Reserved
4	R/W	REFCLK_SEL	1'b0: refclk is derived from dedicated clock pin; 1'b1: refclk is derived from Fabric logic
3:2	R/W	PLL_REFCLK_CML_SEL	2’b00: refclk is derived from local pin, PLL0 corresponds to reference clock 0 pin, PLL1 corresponds to reference clock 1 pin 2’b01: refclk is derived from another PLL's dedicated clock pin within the same HSST, PLL0 corresponds to reference clock 1 pin, PLL1 corresponds to reference clock 0 pin 2’b10, 2’b11: Reserved
1:0	R/W	CLKBUFS4_C	Reserved

Table 5-21 PLL Configuration Register Description: pma_pll_reg19, Offset Address 0x013

Bits	R/W	Corresponding Parameter Name	Description
7:4	R/W	RESCAL_I_CODE_VAL_0TO3	Reserved
3	R/W	RESCAL_EN	Reserved
2	R/W	PLL_CLKBUF_PD_RIGHT	Reserved
1	R/W	PLL_CLKBUF_PD_LEFT	Reserved
0	R/W	PLL_LOCKDET_MODE	Reserved

Table 5-22 PLL Configuration Register Description: pma_pll_reg20, Offset Address 0x014

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R/W	RESCAL_WAIT_SEL	Reserved
4:3	R/W	RESCAL_ITER_VALID_SEL	Reserved
2	R/W	RESCAL_I_CODE_OW	Reserved
1:0	R/W	RESCAL_I_CODE_VAL_4TO5	Reserved

Table 5-23 PLL Configuration Register Description: pma_pll_reg21, Offset Address 0x015

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:0	R/W	I_CTRL_MAX	Reserved

Table 5-24 PLL Configuration Register Description: pma_pll_reg22, Offset Address 0x016

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:0	R/W	I_CTRL_MIN	Reserved

Table 5-25 PLL Configuration Register Description: pma_pll_reg23, Offset Address 0x017

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	pma_quadreg_txpll_160to167	[7:1]: Reserved [0]: pll_refclk_div2_en_o, PLL reference clock divide-by-two enable, corresponding to parameter M in Section 3.2 PLL Functions

Table 5-26 PLL Configuration Register Description: pma_pll_reg24, Offset Address 0x018

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	pma_quadreg_txpll_168to175	Reserved

Table 5-27 PLL Configuration Register Description: pma_pll_reg25, Offset Address 0x019

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	pma_quadreg_txpll_176to183	Reserved

Table 5-28 PLL Configuration Register Description: pma_pll_reg26, Offset Address 0x01a

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	pma_quadreg_txpll_184to191	Reserved

Table 5-29 PLL Configuration Register Description: pma_pll_reg27, Offset Address 0x01b

Bits	R/W	Corresponding Parameter Name	Description
7	R	pma_pll_status_7	Reserved
6:1	R	pma_pll_status_6_1	Reserved
0	R	pma_pll_status_0	Reserved

Table 5-30 PLL Configuration Register Description: pma_pll_reg28, Offset Address 0x01c

Bits	R/W	Corresponding Parameter Name	Description
7	R	pma_pll_status_15	Reserved
6	R	pma_pll_status_14	pll_unlocked state
5	R	pma_pll_status_13	pll_locked state
4	R	pma_pll_status_12	Reserved
3	R	pma_pll_status_11	Reserved
2	R	pma_pll_status_10	Reserved
1:0	R	pma_pll_status_9_8	Reserved

Table 5-31 PLL Configuration Register Description: pma_pll_reg29, Offset Address 0x01d

Bits	R/W	Corresponding Parameter Name	Description
7:2	R	pma_pll_status_23_18	Reserved
1	R	pma_pll_status_17	Reserved
0	R	pma_pll_status_16	Reserved

Table 5-32 PLL Configuration Register Description: pma_pll_reg30, Offset Address 0x01e

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	pma_pll_status_31_24	Reserved

Table 5-33 PLL Configuration Register Description: pma_pll_reg31, Offset Address 0x01f

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		Reserved
2	R/W	cfg_pll_rstn	Configuring PLL's cfg_pll_rstn 1'b0: Reset; 1'b1: Not reset
1	R/W	cfg_pllpowerup	Configuring PLL's cfg_pllpowerup 1'b0: ON; 1'b1: OFF
0	R/W	cfg_hsst_rstn	Configuring PLL's cfg_hsst_rstn 1'b0: Reset; 1'b1: Not reset

5.2 PCS Channel Configuration Register Description

Table 5-34 PCS Channel Configuration Register Description: Offset Address 0x000

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PCS_BYPASS_BRIDGE_FIFO	Active-high Bypass module RX Bridge FIFO,

Bits	R/W	Corresponding Parameter Name	Description
			related to IP configuration 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"
6	R/W	PCS_BYPASS_BRIDGE	Active-high Bypass module RX Bridge unit, related to IP configuration 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"
5	R/W	PCS_BYPASS_GEAR	Active-high Bypass module RX Gear, related to IP configuration 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"
4	R/W	PCS_BYPASS_CTC	Active-high Bypass module CTC, related to IP configuration 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"
3	R/W	PCS_BYPASS_BONDING	Active-high Bypass module Channel Bonding, related to IP configuration 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"
2	R/W	PCS_BYPASS_DENC	Active-high Bypass module 8B10B Decoder, related to IP configuration 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"
1	R/W	PCS_BYPASS_WORD_ALIGN	Active-high Bypass module Word Alignment, related to IP configuration 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"
0	R		Reserved

Table 5-35 PCS Channel Configuration Register Description: Offset Address 0x001

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved
6	R/W	PCS_FARLP_PWR_REDUCTION	Active-high, disable PCS far-end loopback FIFO, reducing power consumption 1'b0: Corresponds to parameter value "FALSE", enable PCS far-end loopback FIFO when conducting PCS far-end loopback test 1'b1: Corresponds to parameter value "TRUE", disable PCS far-end loopback FIFO when not conducting PCS far-end loopback test, reducing power consumption
5	R/W	PCS_SAMP_16B	One of the PCS Receiver module bit width selections, related to IP configuration 1'b0: Corresponds to parameter value "X20"; used for bit width modes other than 8/16/32 bits only 1'b1: Corresponds to parameter value "X16"; used for 8/16/32 bits only bit width modes
4:3	R/W	PCS_ALIGN_MODE	Word Alignment Link State Machine selection, related to IP configuration 2'b00: Corresponds to parameter value "1GB", select Link State Machine based on Gig Ethernet 2'b01: Corresponds to parameter value "10GB", select Link State Machine based on 10G Ethernet 2'b10: Corresponds to parameter value

Bits	R/W	Corresponding Parameter Name	Description
			"RAPIDIO", select Link State Machine based on RapidIO 2'b11: Corresponds to parameter value "OUTSIDE", select External State Machine control
2:1	R/W	PCS_RX_POLARITY_INV	RX Sample Reg module polarity inversion and bit order inversion 2'b00: Corresponds to parameter value "DELAY", no inversion 2'b01: Corresponds to parameter value "BIT_POLARITY_INVERSION", enable polarity inversion 2'b10: Corresponds to parameter value "BIT_REVERSAL", enable bit order inversion 2'b11: Corresponds to parameter value "BOTH", enable both polarity inversion and bit order inversion
0	R/W	PCS_DATA_MODE	One of the PCS Receiver module bit width selections, related to IP configuration 1'b0: Corresponds to parameter values "X8", "X10", used for 8bit only, 10bit only, or 8B10B 8bit width modes 1'b1: Corresponds to parameter values "X16", "X20", used for width modes other than 8bit only, 10bit only, or 8B10B 8bit

Table 5-36 PCS Channel Configuration Register Description: Offset Address 0x002

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PCS_COMMA_REG0[7:0]	Word Alignment Comma Byte 0 Definition, lower 8bits Related to IP configuration

Table 5-37 PCS Channel Configuration Register Description: Offset Address 0x003

Bits	R/W	Corresponding Parameter Name	Description
7:2	R/W	PCS_COMMA_MASK[5:0]	Word Alignment Comma Mask bit definition, lower 6bits Related to IP configuration
1:0	R/W	PCS_CHx_COMMA_REG0[9:8]	Word Alignment Comma Byte 0 Definition, upper 2bits Related to IP configuration

Table 5-38 PCS Channel Configuration Register Description: Offset Address 0x004

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	PCS_CTC_MODE	CTC mode selection, related to IP configuration 2'b00: Corresponds to parameter value "1SKIP", the inserted/deleted SKIP character is 1 byte 2'b01: Corresponds to parameter value "2SKIP", the inserted/deleted SKIP characters are 2 bytes 2'b10: Corresponds to parameter value "PCIE_2BYTE", PCIe's 2-byte mode, only adds or deletes the subsequent skip 2'b11: Corresponds to parameter value "4SKIP",

Bits	R/W	Corresponding Parameter Name	Description
			PCIe's 4-byte mode, the SKIP bytes are 4 bytes, but only the last byte of the SKIP characters is inserted/deleted
5:4	R/W	PCS_CEB_MODE	Channel Bonding State Machine selection, related to IP configuration 2'b00: Corresponds to parameter value "10GB", selects the Channel Bonding State Machine based on XAUI 2'b01: Corresponds to parameter value "RAPIDIO", selects the Channel Bonding State Machine based on RapidIO 2'b10: Corresponds to parameter value "OUTSIDE", selects External State Machine control 2’b11: Reserved
3:0	R/W	PCS_COMMA_MASK[9:6]	Word Alignment Comma Mask bit definition, upper 4 bits Related to IP configuration

Table 5-39 PCS Channel Configuration Register Description: Offset Address 0x005

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PCS_A_REG	Definition of Align Pattern used for channel bonding, related to IP configuration

Table 5-40 PCS Channel Configuration Register Description: Offset Address 0x006

Bits	R/W	Corresponding Parameter Name	Description
7:2	R/W	PCS_SKIP_REG0[5:0]	SKIP character Byte 0 used by CTC, lower 6bits, related to IP configuration
1	R/W	PCS_GE_AUTO_EN	Active-high, enable automatic replacement from /C/ to /I2/ based on 1 Gig Ethernet, related to IP configuration 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"
0	R		Reserved

Table 5-41 PCS Channel Configuration Register Description: Offset Address 0x007

Bits	R/W	Corresponding Parameter Name	Description
7:4	R/W	PCS_SKIP_REG1[3:0]	SKIP character Byte 1 used by CTC, lower 4bits, related to IP configuration
3	R		Reserved
2:0	R/W	PCS_SKIP_REG0[8:6]	SKIP character Byte 0 used by CTC, upper 3bits, related to IP configuration

Table 5-42 PCS Channel Configuration Register Description: Offset Address 0x008

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	PCS_SKIP_REG2[1:0]	SKIP character Byte 2 used by CTC, lower 2bits, related to IP configuration
5	R		Reserved

Bits	R/W	Corresponding Parameter Name	Description
4:0	R/W	PCS_SKIP_REG1[8:4]	SKIP character Byte 1 used by CTC, upper 5bits, related to IP configuration

Table 5-43 PCS Channel Configuration Register Description: Offset Address 0x009

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved
6:0	R/W	PCS_SKIP_REG2[8:2]	SKIP character Byte 2 used by CTC, upper 7bits, related to IP configuration

Table 5-44 PCS Channel Configuration Register Description: Offset Address 0x00a

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PCS_SKIP_REG3[7:0]	SKIP character Byte 3 used by CTC, lower 8 bits, related to IP configuration

Table 5-45 PCS Channel Configuration Register Description: Offset Address 0x00b

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved
6	R/W	PCS_ERRDETECT_SILENCE	Active-high, report an error when K-code encoding is incorrect 1'b0: Corresponds to parameter value "FALSE"; 1"b1:" Corresponds to parameter value "TRUE"
5	R/W	PCS_COMMA_DET_MODE	Alignment mode selection in Word Alignment module, related to IP configuration 1'b0: Corresponds to parameter value "COMMA_PATTERN", select Comma Alignment mode 1'b1: Corresponds to parameter value "RX_CLK_SLIP", select RX CLK Slip mode
4	R/W	PCS_FIFOFLAG_CTC	CTC priority encoding flag signal in RXstatus encoding, configured as 1 indicates high priority signal in CTC 1"b0: Corresponds to parameter value "FALSE"; 1"b1: Corresponds to parameter value "TRUE"
3	R/W	PCS_SPLIT	One of the PCS Receiver module bit width selections, related to IP configuration 1'b0: Corresponds to parameter value "FALSE"; for bit width modes other than 8bit only, 10bit only, or 8B10B 8bit 1'b1: Corresponds to parameter value "TRUE"; for 8bit only, 10bit only, or 8B10B 8bit bit width modes
2	R/W	PCS_DEC_DUAL	One of the PCS Receiver module bit width selections, related to IP configuration 1'b1: Corresponds to parameter value "TRUE"; 1"b0:" Corresponds to parameter value "FALSE"
1	R		Reserved
0	R/W	PCS_SKIP_REG3[8]	SKIP character Byte 3 used by CTC, upper 1bit, related to IP configuration

Table 5-46 PCS Channel Configuration Register Description: Offset Address 0x00c

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PCS_RCLK_POLINV	RCLK clock source selection 1'b0: Corresponds to parameter value "RCLK" 1'b1: Corresponds to parameter value "REVERSE_OF_RCLK"
6:5	R/W	PCS_AFTER_CTC_RCLK_SEL	AFTER_CTC_RCLK clock source selection, related to IP configuration 2'b00: Corresponds to parameter value "PMA_RCLK" 2'b01: Corresponds to parameter value "PMA_TCLK" 2'b10: Corresponds to parameter value "MCB_RCLK" 2'b11: Corresponds to parameter value "RCLK2"
4:3	R/W	PCS_CB_RCLK_SEL	CB_RCLK clock source selection, related to IP configuration 2'b00: Corresponds to parameter value "PMA_RCLK" 2'b01: Corresponds to parameter value "PMA_TCLK" 2'b10: Corresponds to parameter value "MCB_RCLK" 2'b11: Corresponds to parameter value "RCLK"
2:1	R/W	PCS_PCS_RCLK_SEL	PCS_RCLK clock source selection, related to IP configuration 2'b00: Corresponds to parameter value "PMA_RCLK" 2'b01: Corresponds to parameter value "PMA_TCLK" 2'b10: reserved 2'b11: Corresponds to parameter value "RCLK"
0	R/W	PCS_PMA_RCLK_POLINV	1"b0: Corresponds to parameter value "PMA_RCLK"; 1"b1:" reserved

Table 5-47 PCS Channel Configuration Register Description: Offset Address 0x00d

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	CFG_AFTER_CTC_RCLK_SEL_1	Select after_ctc_rclk2fabric source, 2'b00:pma_rclk; 2'b01:pma_tclk; 2'b10:mcb_rclk; 2'b11:rclk2
5	R/W	PCS_AFTER_CTC_RCLK_EN_GB	One of the PCS Receiver module bit width selections, related to IP configuration 1'b0: Corresponds to parameter value "FALSE", for bit width modes other than 32bit only, 40bit only, or 8B10B 32bit 1'b1: Corresponds to parameter value "TRUE", for 32bit only, 40bit only, or 8B10B 32bit bit width modes
4	R/W	PCS_AFTER_CTC_RCLK_EN	One of the PCS Receiver module bit width selections, related to IP configuration 1'b0: Corresponds to parameter value "FALSE", for bit width modes other than 8bit only, 10bit only, or 8B10B 8bit 1'b1: Corresponds to parameter value "TRUE", for 8bit only, 10bit only, or 8B10B 8bit bit width modes

Bits	R/W	Corresponding Parameter Name	Description
3	R/W	PCS_CB_RCLK_EN	One of the PCS Receiver module bit width selections, related to IP configuration 1'b0: Corresponds to parameter value "FALSE", for bit width modes other than 8bit only, 10bit only, or 8B10B 8bit 1'b1: Corresponds to parameter value "TRUE", for 8bit only, 10bit only, or 8B10B 8bit bit width modes
2	R/W	PCS_PCS_RCLK_EN	One of the PCS Receiver module bit width selections, related to IP configuration 1"b0: Corresponds to parameter value "FALSE", for bit width modes other than 8bit only, 10bit only, or 8B10B 8bit 1"b1: Corresponds to parameter value "TRUE", for 8bit only, 10bit only, or 8B10B 8bit bit width modes
1:0	R/W	PCS_BRIDGE_RCLK_SEL	CB_RCLK clock source selection 2’b00: Corresponds to parameter value "PMA_RCLK" 2’b01: Corresponds to parameter value "PMA_TCLK" 2’b10: Corresponds to parameter value "MCB_RCLK" 2’b11: Corresponds to parameter value "RCLK"

Table 5-48 PCS Channel Configuration Register Description: Offset Address 0x00e

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved
6	R/W	CFG_AFTER_CTC_RCLK_EN_GB_1	PCS Receiver module bit width selection 1"b0: Output after_ctc_rclkfabric 1'b1: after_ctc_rclkfabric output divided by 2
5	R/W	PCS_RX_BRIDGE_CLK_POLINV	1"b0: Corresponds to parameter value "RX_BRIDGE_CLK"; 1"b1:" Reserved
4:3	R/W	PCS_RX_64B66B_67B	64B66B_67B selection, related to IP configuration 2’b00: Corresponds to parameter value "NORMAL" 2’b01: Corresponds to parameter value "64B_66B" 2’b11: Corresponds to parameter value "64B_67B"
2	R/W	PCS_PCIE_SLAVE	PCI Express-based channel bonding settings, related to IP configuration 1"b0: Corresponds to parameter value "MASTER"; 1"b1: Corresponds to parameter value "SLAVE"
1	R/W	PCS_SLAVE	Channel bonding settings other than PCI Express, related to IP configuration 1"b0: Corresponds to parameter value 0, indicating MASTER 1"b1: Corresponds to parameter value 1, indicating SLAVE
0	R/W	PCS_PCS_RX_RSTN	Reset register for the PCS Receiver, active-low 1'b0: Reset; 1'b1: Not reset

Table 5-49 PCS Channel Configuration Register Description: Offset Address 0x00f

Bits	R/W	Corresponding Parameter Name	Description
7:1	R		Reserved
0	R/W	PCS_PCS_CB_RSTN	PCS CB reset register, active-low 1'b0: Reset; 1'b1: Not reset

Table 5-50 PCS Channel Configuration Register Description: Offset Address 0x010

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R/W	PCS_TX_BYPASS_BIT_SLIP	Bypass TX BitSlip module, active-high 1"b0: Corresponds to parameter value "FALSE"; 1"b1: Corresponds to parameter value "TRUE"
4	R/W	PCS_TX_BYPASS_ENC	Bypass 8B10B Encoder module, active-high, related to IP configuration 1"b0: Corresponds to parameter value "FALSE"; 1"b1: Corresponds to parameter value "TRUE"
3	R/W	PCS_TX_BYPASS_GEAR	One of the PCS Transmitter module data width selections, related to IP configuration 1"b0: Corresponds to parameter value "FALSE", for 32bit only, 40bit only, or 8B10B 32bit width modes 1"b1: Corresponds to parameter value "TRUE", for width modes other than 32bit only, 40bit only, or 8B10B 32bit
2	R/W	PCS_TX_BYPASS_BRIDGE_FIFO	Bypass module TX Bridge unit/TX Bridge FIFO control, [2:1]=2"b00: TX Bridge unit effective [2:1]=2'b01:bypass TX Bridge unit [2:1]=2'b10: bypass TX Bridge FIFO [2] or [1]=1"b0: Corresponds to parameter value "FALSE" [2] or [1]=1"b1: Corresponds to parameter value "TRUE"
1	R/W	PCS_TX_BYPASS_BRIDGE_UINT	
0	R/W	PCS_TX_BRIDGE_GEAR_SEL	Configuration selection for the order of bridge unit and gear modules in TX direction, related to IP configuration 1'b0: Corresponds to parameter value "FALSE", bridge unit first 1'b1: Corresponds to parameter value "TRUE", gear module first

Table 5-51 PCS Channel Configuration Register Description: Offset Address 0x011

Bits	R/W	Corresponding Parameter Name	Description
7:3	R/W	PCS_TX_BIT_SLIP_CYCLES	Determine the number of bits for Slip in the TX Bit Slip module
2:1	R/W	PCS_TX_DRIVE_REG_MODE	TX Drive Reg module polarity inversion and bit order inversion 2"b00: Corresponds to parameter value "NO_CHANGE", no inversion 2"b01: Corresponds to parameter value "EN_POLARIY_REV", enable polarity inversion 2"b10: Corresponds to parameter value "EN_BIT_REV", enable bit order inversion

Bits	R/W	Corresponding Parameter Name	Description
			2"b11: Corresponds to parameter value "EN_BOTH", enable both polarity inversion and bit order inversion
0	R/W	PCS_TX_GEAR_SPLIT	One of the PCS Transmitter module data width selections, related to IP configuration 1"b0: Corresponds to parameter value "FALSE", for other modes 1"b1: Corresponds to parameter value "TRUE", for 32bit only, 40bit only, or 8B10B 32bit width modes

Table 5-52 PCS Channel Configuration Register Description: Offset Address 0x012

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		Reserved
2	R/W	PCS_INT_TX_MASK_2	Active-high Mask transmit channel interrupt status register (offset address 0x27) bit 2 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
1	R/W	PCS_INT_TX_MASK_1	Active-high Mask transmit channel interrupt status register (offset address 0x27) bit 1 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
0	R/W	PCS_INT_TX_MASK_0	Active-high Mask transmit channel interrupt status register (offset address 0x27) bit 0 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"

Table 5-53 PCS Channel Configuration Register Description: Offset Address 0x013

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		Reserved
2	R/W	PCS_INT_TX_CLR_2	Active-high clear transmit channel interrupt status register (offset address 0x27) bit 2 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
1	R/W	PCS_INT_TX_CLR_1	Active-high clear transmit channel interrupt status register (offset address 0x27) bit 1 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
0	R/W	PCS_INT_TX_CLR_0	Active-high clear transmit channel interrupt status register (offset address 0x27) bit 0 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"

Table 5-54 PCS Channel Configuration Register Description: Offset Address 0x014

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PCS_TX_GEAR_CLK_EN_SEL	One of the PCS Transmitter module data width selections, related to IP configuration 1"b0: Corresponds to parameter value "FALSE", for other modes 1"b1: Corresponds to parameter value "TRUE", for scenarios where one of the width modes (32bit only, 40bit only, or 8B10B 32bit) is selected in conjunction with the Bypass TX Bridge FIFO mode

Bits	R/W	Corresponding Parameter Name	Description
6	R/W	PCS_TX_SLAVE	Channel bonding settings at transmit side, related to IP configuration 1"b0: Corresponds to parameter value "MASTER"; 1"b1: Corresponds to parameter value "SLAVE"
5	R/W	PCS_TX_PCS_TX_RSTN	Reset register for the PCS Transmitter, active-low 1'b0: Reset; 1'b1: Not reset
4	R/W	PCS_PCS_TCLK_SEL	PCS_TCLK selection, related to IP configuration 1"b0: Corresponds to parameter value "PMA_TCLK"; 1"b1: Corresponds to parameter value "TCLK"
3	R/W	PCS_TX_TCLK_POLINV	1"b0: Corresponds to parameter value "TCLK"; 1"b1: Reserved
2	R/W	PCS_TX_BRIDGE_TCLK_SEL	TCLK clock source selection, related to IP configuration 1"b0: Corresponds to parameter value "PCS_TCLK"; 1"b1: Corresponds to parameter value "TCLK"
1	R/W	PCS_TX_PCS_CLK_EN_SEL	One of the PCS Transmitter module data width selections, related to IP configuration 1"b0: Corresponds to parameter value "FALSE", for other modes 1"b1: Corresponds to parameter value "TRUE", for 32bit only, 40bit only, or 8B10B 32bit width modes
0	R/W	PCS_TX_PMA_TCLK_POLINV	1"b0: Corresponds to parameter value "PMA_TCLK"; 1"b1: Reserved

Table 5-55 PCS Channel Configuration Register Description: Offset Address 0x015

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved
4	R/W	PCS_GEAR_TCLK_SEL	GEAR_TCLK selection, related to IP configuration 1"b0: Corresponds to parameter value "PMA_TCLK"; 1"b1: Corresponds to parameter value "TCLK2"
3:2	R/W	PCS_TX_64B66B_67B	TX 64B66B_67B selection, related to IP configuration 2'b00: Corresponds to parameter value "NORMAL" 2'b01: Corresponds to parameter value "64B_66B" 2'b11: Corresponds to parameter value "64B_67B"
1:0	R/W	PCS_DATA_WIDTH_MODE	One of the PCS Transmitter module data width selections, related to IP configuration 2"b00: Corresponds to parameter value "X20", for 20bit only, 8B10B 16bit, 8B10B 32bit, and 40bit only modes 2"b01: Corresponds to parameter value "X16", for 16bit only and 32bit only modes 2"b10: Corresponds to parameter value "X10", for 10bit only and 8B10B 8bit modes 2"b11: Corresponds to parameter value "X8", for 8bit only mode

Table 5-56 PCS Channel Configuration Register Description: Offset Address 0x016

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved
4	R/W	PCS_TX_BRIDGE_CLK_POLINV	TX_BRIDGE_CLK clock selection 1'b0: Select TX_BRIDGE_CLK 1'b1: Select the inverted clock of TX_BRIDGE_CLK

Bits	R/W	Corresponding Parameter Name	Description
3	R		Reserved
2	R/W	PCS_ENC_DUAL	One of the PCS Transmitter module data width selections, related to IP configuration 1"b0: Corresponds to parameter value "FALSE", for modes other than 8B10B 16bit and 8B10B 32bit 1"b1: Corresponds to parameter value "TRUE", for 8B10B 16bit and 8B10B 32bit modes
1	R/W	PCS_TX_OUTZZ	Reserved
0	R/W	PCS_TX_TCLK2FABRIC_SEL	One of the PCS Transmitter module data width selections, related to IP configuration 1"b0: Corresponds to parameter value "FALSE", for modes other than 32bit only, 40bit only, and 8B10B 32bit 1"b1: Corresponds to parameter value "TRUE", for 32bit only, 40bit only, and 8B10B 32bit modes

Table 5-57 PCS Channel Configuration Register Description: Offset Address 0x017

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PCS_COMMA_REG1	Word Alignment Comma Byte 1 Definition, lower 8 bits, related to IP configuration

Table 5-58 PCS Channel Configuration Register Description: Offset Address 0x018

Bits	R/W	Corresponding Parameter Name	Description
7:2	R		Reserved
1:0	R/W	PCS_COMMA_REG1	Word Alignment Comma Byte 1 Definition, upper 2 bits, related to IP configuration

Table 5-59 PCS Channel Configuration Register Description: Offset Address 0x019

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		Reserved
2:0	R/W	PCS_RAPID_IMAX	Number of bytes for lock state detection in Rapid IO Link State Machine, Related to IP configuration

Table 5-60 PCS Channel Configuration Register Description: Offset Address 0x01a

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PCS_RAPID_VMIN_1	Number of bytes for exit state detection in Rapid IO Link State Machine, lower 8 bits, related to IP configuration

Table 5-61 PCS Channel Configuration Register Description: Offset Address 0x01b

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PCS_RAPID_VMIN_2	Number of bytes for exit state detection in Rapid IO Link State Machine, upper 8 bits, related to IP configuration

Table 5-62 PCS Channel Configuration Register Description: Offset Address 0x01c

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R/W	PCS_PRBS_ERR_LPBK	PRBS_ERR_LPBK enable 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"
4	R/W	PCS_RX_ERRCNT_CLR	PCS_ERR_CNT counter clear, high level clear 1"b0: Corresponds to parameter value "FALSE"; 1"b1: Corresponds to parameter value "TRUE", counter cleared
3:0	R/W	PCS_RX_PRBS_MODE	PRBS Checker mode selection at the receive side 4'd0: Corresponds to parameter value "DISABLE"; 4'd1: Corresponds to parameter value "PRBS_7"; 4'd2: Corresponds to parameter value "PRBS_15"; 4'd3: Corresponds to parameter value "PRBS_23"; 4'd4: Corresponds to parameter value "PRBS_31"

Table 5-63 PCS Channel Configuration Register Description: Offset Address 0x01d

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R/W	PCS_ENABLE_PRBS_GEN	PCS PRBS Generator enable, high level enable 1'b0: Corresponds to parameter value "FALSE", disable PRBS 1'b1: Corresponds to parameter value "TRUE", enable PRBS
4	R/W	PCS_TX_INSERT_ER	PRBS error code injection For each transition from 0 to 1, one error injection operation is performed, with the number of injected error bits being variable 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"
3:0	R/W	PCS_TX_PRBS_MODE	PCS PRBS Generator mode selection at the transmit side 4'd0: Corresponds to parameter value "DISABLE"; 4'd1: Corresponds to parameter value "PRBS_7"; 4'd2: Corresponds to parameter value "PRBS_15"; 4'd3: Corresponds to parameter value "PRBS_23"; 4'd4: Corresponds to parameter value "PRBS_31"; 4'd5: Corresponds to parameter value "LONG_1"; 4'd6: Corresponds to parameter value "LONG_0"; 4'd7: Corresponds to parameter value "20UI"; 4'd8: Corresponds to parameter value "D10_2"; 4'd9: Corresponds to parameter value "PCIE"

Table 5-64 PCS Channel Configuration Register Description: Offset Address 0x01e

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	PCS_ERR_CNT	Checking error counter in PCS PRBS checker, which remains at 0xFF after reaching its maximum value 0xFF and will not increment with further link errors until the counter is cleared

Table 5-65 PCS Channel Configuration Register Description: Offset Address 0x01f

Bits	R/W	Corresponding Parameter Name	Description
7:4	R/W	PCS_MASTER_CHECK_OFFSET	Used for channel bonding, related to IP configuration
3:0	R/W	PCS_DEFAULT_RADDR	Used for channel bonding, related to IP configuration

Table 5-66 PCS Channel Configuration Register Description: Offset Address 0x020

Bits	R/W	Corresponding Parameter Name	Description
7	R	NA	Reserved
6:4	R/W	PCS_SEACH_OFFSET	Channel Bonding range settings, related to IP configuration 4'd0: Corresponds to parameter value "20BIT"; 4'd1: Corresponds to parameter value "30BIT" 4'd2: Corresponds to parameter value "40BIT"; 4'd3: Corresponds to parameter value "50BIT" 4'd4: Corresponds to parameter value "60BIT"; 4'd5: Corresponds to parameter value "70BIT" 3'd6: Corresponds to parameter value "80BIT"
3:0	R/W	PCS_DELAY_SET	Used for Channel Bonding, related to IP configuration

Table 5-67 PCS Channel Configuration Register Description: Offset Address 0x021

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		Reserved
2:0	R/W	PCS_CEB_RAPIDLS_MMAX	The MMAX value used by the Channel Bonding RapidIO state machine, Related to IP configuration

Table 5-68 PCS Channel Configuration Register Description: Offset Address 0x022

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved
4:0	R/W	PCS_CTC_AFULL	CTC FIFO Almost Full Threshold

Table 5-69 PCS Channel Configuration Register Description: Offset Address 0x023

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R/W	PCS_CTC_CONTI_SKP_SET	1’b0: Disable continuous SKIP deletion 1’b1: Enable continuous SKIP deletion
4:0	R/W	PCS_CTC_AEMPTY	CTC FIFO Almost Empty Threshold

Table 5-70 PCS Channel Configuration Register Description: Offset Address 0x024

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved
4	R/W	PCS_PMA_RX2TX_PLOOP_EN	PMA far-end parallel loopback enable, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"

Bits	R/W	Corresponding Parameter Name	Description
3	R/W	PCS_PMA_TX2RX_SLOOP_EN	PMA near-end serial loopback enable, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
2	R/W	PCS_PMA_TX2RX_PLOOP_EN	PMA near-end parallel loopback enable, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
1	R/W	PCS_NEAR_LOOP	PCS near-end loopback enable, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
0	R/W	PCS_FAR_LOOP	PCS far-end loopback enable, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"

Table 5-71 PCS Channel Configuration Register Description: Offset Address 0x025

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PCS_INT_RX_MASK_7	Receive channel interrupt status register (offset address 0x28) bit 7 mask, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
6	R/W	PCS_INT_RX_MASK_6	Receive channel interrupt status register (offset address 0x28) bit 6 mask, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
5	R/W	PCS_INT_RX_MASK_5	Receive channel interrupt status register (offset address 0x28) bit 5 mask, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
4	R/W	PCS_INT_RX_MASK_4	Receive channel interrupt status register (offset address 0x28) bit 4 mask, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
3	R/W	PCS_INT_RX_MASK_3	Receive channel interrupt status register (offset address 0x28) bit 3 mask, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
2	R/W	PCS_INT_RX_MASK_2	Receive channel interrupt status register (offset address 0x28) bit 2 mask, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
1	R/W	PCS_INT_RX_MASK_1	Receive channel interrupt status register (offset address 0x28) bit 1 mask, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
0	R/W	PCS_INT_RX_MASK_0	Receive channel interrupt status register (offset address 0x28) bit 0 mask, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"

Table 5-72 PCS Channel Configuration Register Description: Offset Address 0x026

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PCS_INT_RX_CLR_7	Clear receive channel interrupt status register (offset address 0x28) bit 7, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1:

Bits	R/W	Corresponding Parameter Name	Description
			Corresponds to parameter value "TRUE"
6	R/W	PCS_INT_RX_CLR_6	Clear receive channel interrupt status register (offset address 0x28) bit 6, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
5	R/W	PCS_INT_RX_CLR_5	Clear receive channel interrupt status register (offset address 0x28) bit 5, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
4	R/W	PCS_INT_RX_CLR_4	Clear receive channel interrupt status register (offset address 0x28) bit 4, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
3	R/W	PCS_INT_RX_CLR_3	Clear receive channel interrupt status register (offset address 0x28) bit 3, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
2	R/W	PCS_INT_RX_CLR_2	Clear receive channel interrupt status register (offset address 0x28) bit 2, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
1	R/W	PCS_INT_RX_CLR_1	Clear receive channel interrupt status register (offset address 0x28) bit 1, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"
0	R/W	PCS_INT_RX_CLR_0	Clear receive channel interrupt status register (offset address 0x28) bit 0, active-high 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"

Table 5-73 PCS Channel Configuration Register Description: Offset Address 0x027

Bits	R/W	Corresponding Parameter Name	Description
7:3	R	NA	Reserved
2	R	NA	1'b1: Illegal character had been detected in 8B10B encoding (This state is the historical status)
1	R	NA	1'b1: TX Bridge FIFO was read empty (This state is the historical status)
0	R	NA	1'b1: TX Bridge FIFO was write full (This state is the historical status)

Table 5-74 PCS Channel Configuration Register Description: Offset Address 0x028

Bits	R/W	Corresponding Parameter Name	Description
7	R	NA	1'b1: RX Bridge FIFO was read empty (This state is the historical status)
6	R	NA	1'b1: RX Bridge FIFO was write full (This state is the historical status)
5	R	NA	1'b1: CTC FIFOwas read empty (This state is the historical status)
4	R	NA	1'b1: CTC FIFO was write full (This state is the historical status)
3	R	NA	1'b1: Channel Bonding FIFO was read empty (This state is the historical status)

Bits	R/W	Corresponding Parameter Name	Description
2	R	NA	1'b1: Channel Bonding FIFO was write full (This state is the historical status)
1	R	NA	1'b1: Channel Bonding state machine was out of lock (This state is the historical status)
0	R	NA	1'b1: Word Alignment state machine was out of lock (This state is the historical status)

Table 5-75 PCS Channel Configuration Register Description: Offset Address 0x029

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		Reserved
2	R/W	PCS_CA_DYN_DLY_SEL_RX	Active-high, enables the CLK Aligner function of the corresponding receive channel 1'b0: Corresponds to parameter value "FALSE", bypass CLK Aligner 1'b1: Corresponds to parameter value "TRUE", enable CLK Aligner
1	R/W	PCS_CA_DYN_DLY_EN_RX	Active-high, enable the CLK Aligner delay step of the receive channel 1'b0: Corresponds to parameter value "FALSE", CLK Aligner delay step is 0 1'b1: Corresponds to parameter value "TRUE", CLK Aligner delay step determined by CLK_ALIGNER_RXx or P_CIM_CLK_ALIGNER_RXx [7:0]
0	R/W	PCS_CA_RSTN_RX	RX CLK Aligner reset, active-low 1"b0: Corresponds to parameter value "FALSE "; 1"b1: Corresponds to parameter value "TRUE"

Table 5-76 PCS Channel Configuration Register Description: Offset Address 0x02a

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PCS_CA_RX	Static setting of the CLK Aligner delay step for the corresponding receive channel, Used when P_CIM_CLK_DYN_DLY_SEL_RX[x] is invalid

Table 5-77 PCS Channel Configuration Register Description: Offset Address 0x02b

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		Reserved
2	R/W	PCS_CA_DYN_DLY_SEL_TX	Active-high, enable the CLK Aligner function of the corresponding transmit channel 1'b0: Corresponds to parameter value "FALSE", bypass CLK Aligner 1'b1: Corresponds to parameter value "TRUE", enable CLK Aligner
1	R/W	PCS_CA_DYN_DLY_EN_TX	Active-high, enable the CLK Aligner delay step of the transmit channel 1'b0: Corresponds to parameter value "FALSE", CLK Aligner delay step is 0 1'b1: Corresponds to parameter value "TRUE", CLK Aligner delay step is determined by CLK_ALIGNER_TXx or P_CIM_CLK_ALIGNER_TXx [7:0]

Bits	R/W	Corresponding Parameter Name	Description
0	R/W	PCS_CA_RSTN_TX	TX CLK Aligner reset, active-low 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"

Table 5-78 PCS Channel Configuration Register Description: Offset Address 0x02c

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PCS_CA_TX	Static setting for the CLK Aligner delay step of the corresponding transmission channel, Used when P_CIM_CLK_DYN_DLY_SEL_TX[x] is invalid

Table 5-79 PCS Channel Configuration Register Description: Offset Address 0x02d

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PCS_RXTEST_PWR_REDUCTION	Active high to disable RX test_status function, reducing power 1'b0: Corresponds to parameter value "NORMAL" 1'b1: Corresponds to parameter value "POWER_REDUCTION"
6	R/W	PCS_RXBRG_PWR_REDUCTION	Active high to disable RX bridge function, reducing power 1'b0: Corresponds to parameter value "NORMAL" 1'b1: Corresponds to parameter value "POWER_REDUCTION"
5	R/W	PCS_RXGEAR_PWR_REDUCTION	Active high to disable RX GEAR function, reducing power 1'b0: Corresponds to parameter value "NORMAL" 1'b1: Corresponds to parameter value "POWER_REDUCTION"
4	R/W	PCS_RXCTC_PWR_REDUCTION	Active high to disable RX CTC function, reducing power 1'b0: Corresponds to parameter value "NORMAL" 1'b1: Corresponds to parameter value "POWER_REDUCTION"
3	R/W	PCS_RXCB_PWR_REDUCTION	Active high to disable RX channel bonding function, reducing power 1'b0: Corresponds to parameter value "NORMAL" 1'b1: Corresponds to parameter value "POWER_REDUCTION"
2	R/W	PCS_RXDEC_PWR_REDUCTION	Active high to disable RX decoder function, reducing power 1'b0: Corresponds to parameter value "NORMAL" 1'b1: Corresponds to parameter value "POWER_REDUCTION"
1	R/W	PCS_WDALIGN_PWR_REDUCTION	Active high to disable RX wordalign function, reducing power 1'b0: Corresponds to parameter value "NORMAL" 1'b1: Corresponds to parameter value "POWER_REDUCTION"
0	R/W	PCS_RXPRBS_PWR_REDUCTION	Active high to disable RX PRBS function, reducing power 1'b0: Corresponds to parameter value "NORMAL" 1'b1: Corresponds to parameter value "POWER_REDUCTION"

Table 5-80 PCS Channel Configuration Register Description: Offset Address 0x02e

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved
6	R/W	CFG_TXBRG_EMPTY_CHK_EN	TX bridge unit FIFO empty detection enable 1'b1: Corresponds to parameter value "TRUE"; 1'b0: Corresponds to parameter value "FALSE"
5	R/W	CFG_TXBRG_FULL_CHK_EN	TX bridge unit FIFO full detection enable 1'b1: Corresponds to parameter value "TRUE"; 1'b0: Corresponds to parameter value "FALSE"
4	R/W	PCS_TXPRBS_PWR_REDUCTION	Active high to disable TX PRBS function, reducing power consumption 1'b0: Corresponds to parameter value "NORMAL" 1'b1: Corresponds to parameter value "POWER_REDUCTION"
3	R/W	PCS_TXBSLP_PWR_REDUCTION	Active high to disable TX bitslip function, reducing power consumption 1'b0: Corresponds to parameter value "NORMAL" 1'b1: Corresponds to parameter value "POWER_REDUCTION"
2	R/W	PCS_TXENC_PWR_REDUCTION	Active high to disable TX encoder function, reducing power consumption 1'b0: Corresponds to parameter value "NORMAL" 1'b1: Corresponds to parameter value "POWER_REDUCTION"
1	R/W	PCS_TXGEAR_PWR_REDUCTION	Active high to disable TX GEAR function, reducing power consumption 1'b0: Corresponds to parameter value "NORMAL" 1'b1: Corresponds to parameter value "POWER_REDUCTION"
0	R/W	PCS_TXBRG_PWR_REDUCTION	Active high to disable TX bridge function, reducing power consumption 1'b0: Corresponds to parameter value "NORMAL" 1'b1: Corresponds to parameter value "POWER_REDUCTION"

Table 5-81 PCS Channel Configuration Register Description: Offset Address 0x02f

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	CFG_FLP_EMPTY_CHK_EN	Far-end loopback FIFO read empty detection enable 1'b1: Corresponds to parameter value "TRUE"; 1'b0: Corresponds to parameter value "FALSE"
6	R/W	CFG_FLP_FULL_CHK_EN	Far-end loopback FIFO write full detection enable 1'b1: Corresponds to parameter value "TRUE"; 1'b0: Corresponds to parameter value "FALSE"
5	R/W	CFG_CEB_EMPTY_CHK_EN	Receive side channel bonding unit FIFO read empty detection enable 1'b1: Corresponds to parameter value "TRUE"; 1'b0: Corresponds to parameter value "FALSE"
4	R/W	CFG_CEB_FULL_CHK_EN	Receive side channel bonding unit FIFO write full detection enable 1'b1: Corresponds to parameter value "TRUE"; 1'b0: Corresponds to parameter value "FALSE"
3	R/W	CFG_CTC_EMPTY_CHK_EN	Receive side CTC unit FIFO read empty detection enable 1'b1: Corresponds to parameter value "TRUE"; 1'b0: Corresponds to parameter value "FALSE"

Bits	R/W	Corresponding Parameter Name	Description
2	R/W	CFG_CTC_FULL_CHK_EN	Receive side CTC unit FIFO write full detection enable 1'b1: Corresponds to parameter value "TRUE"; 1'b0: Corresponds to parameter value "FALSE"
1	R/W	CFG_RXBRG_EMPTY_CHK_EN	Receive side bridge unit FIFO read empty detection enable 1'b1: Corresponds to parameter value "TRUE"; 1'b0: Corresponds to parameter value "FALSE"
0	R/W	CFG_RXBRG_FULL_CHK_EN	Receive side bridge unit FIFO write full detection enable 1'b1: Corresponds to parameter value "TRUE"; 1'b0: Corresponds to parameter value "FALSE"

5.3 PMA Channel Configuration Register Discription

5.3.1 PMA RX Section

Table 5-82 PMA Channel Configuration Register Description: pma_rx_reg0, Offset Address 0x000

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_RX_SIGDET_PD_EN	enable RX signal detect power down control from register 1'b0: Corresponds to parameter value "FALSE", controlled by the internal circuit 1'b1: Corresponds to parameter value "TRUE", controlled by the register PMA_REG_RX_SIGDET_PD
6	R/W	PMA_REG_RX_SIGDET_PD	1'b0: Enable receiver signal detection; 1'b1: Disable receiver signal detection
5	R/W	PMA_REG_RX_DATAPATH_PD_EN	enable the RX data path power down control from register 1'b0: Corresponds to parameter value "FALSE", controlled by the internal circuit 1'b1: Corresponds to parameter value "TRUE", controlled by the register PMA_REG_RX_DATAPATH_PD
4	R/W	PMA_REG_RX_DATAPATH_PD	1'b0: Enable receiver data path; 1'b1: Disable receiver data path;
3	R/W	PMA_REG_RX_CLKPATH_PD_EN	enable the RX clk path power down control from register 1'b0: Corresponds to parameter value "FALSE", controlled by internal circuit 1'b1: Corresponds to parameter value "TRUE", controlled by the register PMA_REG_RX_CLKPATH_PD
2	R/W	PMA_REG_RX_CLKPATH_PD	1'b0: Enable receiver clock path; 1'b1: Disable receiver clock path
1	R/W	PMA_REG_RX_PD_EN	enable RX power down control from register 1'b0: Corresponds to parameter value "FALSE", controlled by internal circuit 1'b1: Corresponds to parameter value "TRUE", controlled by the register PMA_REG_RX_PD
0	R/W	PMA_REG_RX_PD	1'b0: Enable receiver; 1'b1: Disable receiver

Table 5-83 PMA Channel Configuration Register Description: pma_rx_reg1, Offset Address 0x001

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_RXPCLK_SLIP_OW	enable rxpclk slip control from register 1'b0: Corresponds to parameter value "DISABLE", controlled by internal circuit 1'b1: Corresponds to parameter value "ENABLE", controlled by the register PMA_REG_RXPCLK_SLIP
6	R/W	PMA_REG_RXPCLK_SLIP	When the register changes from 0 to 1, rxpclk delays one UI 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"
5	R/W	PMA_REG_RX_SIGDET_RST_N_EN	Reserved
4	R/W	PMA_REG_RX_SIGDET_RST_N	Reserved
3	R/W	PMA_REG_RX_CDR_RST_N_EN	enable the CDR reset control from register 1'b0: Corresponds to parameter value "FALSE", controlled by the internal circuit 1'b1: Corresponds to parameter value "TRUE", controlled by the register PMA_REG_RX_CDR_RST_N
2	R/W	PMA_REG_RX_CDR_RST_N	Active-low 1'b0: reset CDR; 1'b1:normal operation of CDR
1	R/W	PMA_REG_RX_DCC_RST_N_EN	Reserved
0	R/W	PMA_REG_RX_DCC_RST_N	Reserved

Table 5-84 PMA Channel Configuration Register Description: pma_rx_reg2, Offset Address 0x002

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R/W	PMA_REG_RX_HIGHZ_EN	Reserved
4	R/W	PMA_REG_RX_HIGHZ	Reserved
3	R/W	PMA_REG_RX_PCLKSWITCH_EN	Reserved
2	R/W	PMA_REG_RX_PCLKSWITCH	Reserved
1	R/W	PMA_REG_RX_PCLKSWITCH_RST_N_EN	Reserved
0	R/W	PMA_REG_RX_PCLKSWITCH_RST_N	Reserved

Table 5-85 PMA Channel Configuration Register Description: pma_rx_reg3, Offset Address 0x003

Bits	R/W	Corresponding Parameter Name	Description
7:4	R/W	REG_RX_EQ_R_SET	Reserved
3:0	R/W	REG_RX_EQ_C_SET	Reserved

Table 5-86 PMA Channel Configuration Register Description: pma_rx_reg4, Offset Address 0x004

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_RX_RATE_EN	enable the RX rate control from register 1'b0: Corresponds to parameter value "FALSE", controlled by internal circuit 1'b1: Corresponds to parameter value "TRUE", controlled by the register PMA_REG_RX_RATE
6	R		Reserved
5:4	R/W	PMA_REG_RX_RATE	RX clock path division ratio, corresponding to parameter D in Section 3.2 PLL Functions 2'b00: Corresponds to parameter value "DIV8", 1/8 of the maximum data rate 2'b01: Corresponds to parameter value "DIV4", 1/4 of the maximum data rate 2'b10: Corresponds to parameter value "DIV2", 1/2 of the maximum data rate 2'b11: Corresponds to parameter value "DIV1", the maximum data rate
3	R/W	PMA_REG_RX_BUSWIDTH_EN	enable the RX datawidth control from register 1'b0: Corresponds to parameter value "FALSE", controlled by internal circuit 1'b1: Corresponds to parameter value "TRUE", controlled by the register PMA_REG_RX_BUSWIDTH
2:0	R/W	PMA_REG_RX_BUSWIDTH	bit[2] is reserved Value of bit[1:0] is determined by IP configuration 2'b00: Corresponds to parameter value "8BIT", 8-bit 2'b01: Corresponds to parameter value "10BIT", 10-bit 2'b10: Corresponds to parameter value "16BIT", 16-bit 2'b11: Corresponds to parameter value "20BIT", 20-bit

Table 5-87 PMA Channel Configuration Register Description: pma_rx_reg5, Offset Address 0x005

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved
6	R/W	PMA_REG_RX_RES_TRIM_EN	Reserved
5:0	R/W	PMA_REG_RX_RES_TRIM	Reserved

Table 5-88 PMA Channel Configuration Register Description: pma_rx_reg6, Offset Address 0x006

Bits	R/W	Corresponding Parameter Name	Description
7:4	R/W	PMA_REG_RX_ICTRL_SIGDET	Reserved
3:0	R		Reserved

Table 5-89 PMA Channel Configuration Register Description: pma_rx_reg7, Offset Address 0x007

Bits	R/W	Corresponding Parameter Name	Description
7:1	R/W	PMA_REG_RX_PREAMP_IC_0_6	Reserved
0	R/W	PMA_REG_ RX_EQ_OFF	1'b0: Enable receiver equalization; 1'b1: Disable receiver equalization

Table 5-90 PMA Channel Configuration Register Description: pma_rx_reg8, Offset Address 0x008

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R/W	PMA_REG_RX_PCLK_EDGE_SEL	1'b0: Corresponds to parameter value "POS_EDGE", rx_pdata latches to the transmit side on the rising edge of rxpclk 1'b1: Corresponds to parameter value "NEG_EDGE", rx_pdata latches to the transmit side on the falling edge of rxpclk
4:0	R/W	PMA_REG_RX_PREAMP_IC_7_11	Reserved

Table 5-91 PMA Channel Configuration Register Description: pma_rx_reg9, Offset Address 0x009

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved
6:5	R/W	PMA_REG_RX_DCC_IC_TX	Reserved
4:3	R/W	PMA_REG_RX_DCC_IC_RX	Reserved
2	R		Reserved
1:0	R/W	PMA_REG_RX_PIBUF_IC	Reserved

Table 5-92 PMA Channel Configuration Register Description: pma_rx_reg10, Offset Address 0x00a

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	PMA_REG_RX_ICTRL_SLICER	Reserved
5:4	R/W	PMA_REG_RX_ICTRL_PREAMP	Reserved
3:2	R		Reserved
1:0	R/W	PMA_REG_RX_ICTRL_TRX	Reserved

Table 5-93 PMA Channel Configuration Register Description: pma_rx_reg11, Offset Address 0x00b

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	PMA_REG_RX_ICTRL_PREDRV	Reserved
5:4	R/W	PMA_REG_RX_ICTRL_DCC	Reserved
3:2	R/W	PMA_REG_RX_ICTRL_PI	Reserved
1:0	R/W	PMA_REG_RX_ICTRL_PIBUF	Reserved

Table 5-94 PMA Channel Configuration Register Description: pma_rx_reg12, Offset Address 0x00c

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_TXCLK_SEL	1"b0: Corresponds to parameter value "PLL" 1"b1: Corresponds to parameter value "RXCLK"
6	R/W	PMA_REG_RX_TX2RX_PLPBK_EN	PMA parallel loopback enable 1"b0: Corresponds to parameter value "FALSE" 1"b1: Corresponds to parameter value "TRUE"

Bits	R/W	Corresponding Parameter Name	Description
5	R/W	PMA_REG_RX_TX2RX_PLPBK_RST_N_EN	enable the TX2RX parallel loop back reset control from register 1"b0: Corresponds to parameter value "FALSE" 1"b1: Corresponds to parameter value "TRUE"
4	R/W	PMA_REG_RX_TX2RX_PLPBK_RST_N	1"b0: Reset parallel loopback module; 1"b1: Normal operation
3	R/W	PMA_REG_TX_RATE_EN	enable the TX rate control from register 1'b0: Corresponds to parameter value "FALSE", controlled by internal circuit 1"b1: Corresponds to parameter value "TRUE", Controlled by the register PMA_REG_TX_RATE
2	R		Reserved
1:0	R/W	PMA_REG_TX_RATE	TX clock path division ratio, corresponding to parameter D in Section 3.2 PLL Functions 2’b00: Corresponds to Parameter Value "DIV8", line rate is 1/8 of the maximum data rate 2’b01: Corresponds to parameter value "DIV4", line rate is 1/4 of the maximum data rate 2’b10: Corresponds to parameter value "DIV2", line rate is 1/2 of the maximum data rate 2’b11: Corresponds to parameter value "DIV", line rate is equal to the maximum data rate

Table 5-95 PMA Channel Configuration Register Description: pma_rx_reg13, Offset Address 0x00d

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	PMA_REG_PRBS_CHK_WIDTH_SEL	Selection of width for PRBS check 2’b00: Corresponds to parameter value "8BIT", 8bit 2’b01: Corresponds to parameter value "10BIT", 10bit 2’b10: Corresponds to parameter value "16BIT", 16bit 2’b11: Corresponds to parameter value "20BIT", 20bit
5	R/W	PMA_REG_PRBS_CHK_EN	PMA RX PRBS check enable 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"
4:3	R/W	PMA_REG_PRBS_SEL	PMA RX PRBS Mode Selection 2’b00: Corresponds to parameter value "PRBS7" 2’b01: Corresponds to parameter value "PRBS15" 2’b10: Corresponds to parameter value "PRBS23" 2’b11: Corresponds to parameter value "PRBS31"
2	R/W	PMA_REG_UDP_CHK_EN	BIST UDP check enable 1"b0: Corresponds to parameter value "FALSE" 1"b1: Corresponds to parameter value "TRUE"
1	R/W	PMA_REG_RX_ERR_INSERT	Insertion error on the rising edge 1"b0: Corresponds to parameter value "FALSE" 1"b1: Corresponds to parameter value "TRUE"
0	R/W	PMA_REG_RX_DATA_POLARITY	Receive data polarity inversion control register 1"b0: Corresponds to parameter value "NORMAL" 1"b1: Corresponds to parameter value "REVERSE"

Table 5-96 PMA Channel Configuration Register Description: pma_rx_reg14, Offset Address 0x00e

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:3	R/W	PMA_REG_CDR_PROP_GAIN	CDR proportional gain control: 3’b000: 1/2^12; 3’b001: 1/2^11; 3’b010: 1/2^10

Bits	R/W	Corresponding Parameter Name	Description
			3’b011: 1/2^9; 3’b100: 1/2^8; 3’b101: 1/2^7 3’b110: 1/2^6; 3’b111: 1/2^5
2	R/W	PMA_REG_CHK_COUNTER_EN	Checking error detection count enable/clear control 1"b0: Clear counter value; 1"b1: Enable counter
1	R/W	PMA_REG_LOAD_ERR_CNT	enable to load BIST checker error counter to 32bit status 1'b0: Status retains the previous counter value, error counter counts normally 1'b1: Error counter value loaded to status, counter cleared
0	R/W	PMA_REG_BIST_CHK_PAT_SEL	BIST Constant Pattern or PRBS Pattern Selection 1’b0: Corresponds to parameter value "PRBS" 1’b1: Corresponds to parameter value "CONSTANT"

Table 5-97 PMA Channel Configuration Register Description: pma_rx_reg15, Offset Address 0x00f

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:3	R/W	PMA_REG_CDR_INT_GAIN	CDR integral gain control 3’b000: 1/2^17; 3’b001: 1/2^16; 3’b010: 1/2^15 3’b011: 1/2^14; 3’b100: 1/2^13; 3’b101: 1/2^12 3’b110: 1/2^11; 3’b111: 1/2^10
2:0	R/W	PMA_REG_CDR_PROP_TURBO_GAIN	Reserved

Table 5-98 PMA Channel Configuration Register Description: pma_rx_reg16, Offset Address 0x010

Bits	R/W	Corresponding Parameter Name	Description
7:3	R/W	PMA_REG_CDR_INT_SAT_MAX [4:0]	Reserved
2:0	R/W	PMA_REG_CDR_INT_TURBO_GAIN	Reserved

Table 5-99 PMA Channel Configuration Register Description: pma_rx_reg17, Offset Address 0x011

Bits	R/W	Corresponding Parameter Name	Description
7:5	R/W	PMA_REG_CDR_INT_SAT_MIN [2:0]	Reserved
4:0	R/W	PMA_REG_CDR_INT_SAT_MAX [9:5]	Reserved

Table 5-100 PMA Channel Configuration Register Description: pma_rx_reg18, Offset Address 0x012

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved
6:0	R/W	PMA_REG_CDR_INT_SAT_MIN [9:3]	Reserved

Table 5-101 PMA Channel Configuration Register Description: pma_rx_reg19, Offset Address 0x013

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved

Bits	R/W	Corresponding Parameter Name	Description
6	R/W	PMA_REG_CDR_RX_PI_FORCE_SEL	CDR RX PI control force value selection. 1'b0: RX pi ctrl using the accumulator output 1'b1: RX pi ctrl using the force data(bypass CDR) When this bit is set to 1, i.e., after bypassing CDR, a global reset of HSST or reset of RX LANE is required
5	R/W	PMA_REG_CDR_LOCK_RST_OW	Reserved
4	R/W	PMA_REG_CDR_LOCK_RST	Reserved
3	R/W	PMA_REG_CDR_PROP_RST_OW	Reserved
2	R/W	PMA_REG_CDR_PROP_RST	Reserved
1	R/W	PMA_REG_CDR_INT_RST_OW	Reserved
0	R/W	PMA_REG_CDR_INT_RST	Reserved

Table 5-102 PMA Channel Configuration Register Description: pma_rx_reg20, Offset Address 0x014

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_CDR_RX_PI_FORCE_D	CDR RX PI control force data

Table 5-103 Description of PMA Channel Configuration Register: pma_rx_reg21, Offset Address 0x015

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_CDR_INT_SAT_DET_EN	Reserved
6	R/W	PMA_REG_CDR_LOCK_OW	Reserved
5	R/W	PMA_REG_CDR_LOCK	Reserved
4:3	R/W	PMA_REG_CDR_TURBO_MODE_TIMER	Reserved
2:0	R/W	PMA_REG_CDR_LOCK_TIMER	Reserved

Table 5-104 Description of PMA Channel Configuration Register: pma_rx_reg22, Offset Address 0x016

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved

Table 5-105 Description of PMA Channel Configuration Register: pma_rx_reg23, Offset Address 0x017

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_CDR_PI_CTRL_RST_OW	Reserved
6	R/W	PMA_REG_CDR_PI_CTRL_RST	Reserved
5	R/W	PMA_REG_CDR_SAT_DET_STATUS_RESET_EN	Reserved
4	R/W	PMA_REG_CDR_SAT_DET_STATUS_EN	Reserved
3:0	R		Reserved

Table 5-106 Description of PMA Channel Configuration Register: pma_rx_reg24, Offset Address 0x018

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved
6:5	R/W	PMA_REG_CDR_SAT_DET_TIMER	Reserved
4	R/W	PMA_REG_CDR_SIGDET_STATUS_DIS	Reserved
3	R/W	PMA_REG_CDR_SAT_DET_STICKY_RST_OW	Reserved
2	R/W	PMA_REG_CDR_SAT_DET_STICKY_RST	Reserved
1	R/W	PMA_REG_CDR_SAT_DET_RST_OW	Reserved
0	R/W	PMA_REG_CDR_SAT_DET_RST	Reserved

Table 5-107 Description of PMA Channel Configuration Register: pma_rx_reg25, Offset Address 0x019

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_CDR_STATUS_FIFO_EN	Reserved
6:4	R	MA_REG_CDR_STATUS_RADDR_INIT	Reserved
3	R		Reserved
2	R/W	PMA_REG_CDR_TURBO_MODE_EN	Reserved
1	R/W	PMA_REG_CDR_SAT_DET_STATUS_OW	Reserved
0	R/W	PMA_REG_CDR_SAT_DET_STATUS	Reserved

Table 5-108 Description of PMA Channel Configuration Register: pma_rx_reg26, Offset Address 0x01a

Bits	R/W	Corresponding Parameter Name	Description
7:3	R/W	PMA_REG_OOB_COMWAKE_GAP_MIN[4:0]	Reserved
2:0	R/W	PMA_REG_PMA_TEST_SEL	Reserved

Table 5-109 Description of PMA Channel Configuration Register: pma_rx_reg27, Offset Address 0x01b

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved
6:1	R/W	PMA_REG_OOB_COMWAKE_GAP_MAX	Reserved
0	R/W	PMA_REG_OOB_COMWAKE_GAP_MIN[5]	Reserved

Table 5-110 Description of PMA Channel Configuration Register: pma_rx_reg28, Offset Address 0x01c

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_OOB_COMINIT_GAP_MIN	Reserved

Table 5-111 Description of PMA Channel Configuration Register: pma_rx_reg29, Offset Address 0x01d

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_OOB_COMINIT_GAP_MAX	Reserved

Table 5-112 Description of PMA Channel Configuration Register: pma_rx_reg30, Offset Address 0x01e

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R/W	PMA_REG_RX_SYNC_RST_N	Reserved
4	R/W	PMA_REG_RX_SYNC_RST_N_EN	Reserved
3	R/W	PMA_REG_COMINIT_STATUS_CLEAR	Reserved
2	R/W	PMA_REG_COMWAKE_STATUS_CLEAR	Reserved
1:0	R/W	PMA_REG_RX_PIBUF_IC_TX	Reserved

Table 5-113 Description of PMA Channel Configuration Register: pma_rx_reg31, Offset Address 0x01f

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R/W	PMA_REG_RX_SATA_COMWAKE	Reserved
4	R/W	PMA_REG_RX_SATA_COMWAKE_OW	Reserved
3	R/W	PMA_REG_RX_SATA_COMINIT	Reserved
2	R/W	PMA_REG_RX_SATA_COMINIT_OW	Reserved
1:0	R		Reserved

Table 5-114 Description of PMA Channel Configuration Register: pma_rx_reg32, Offset Address 0x020

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_RX_SLIP_EN	1'b0: Corresponds to parameter value "FALSE", CDR demux works normally 1'b1: Corresponds to parameter value "TRUE", bypass CDR demux
6:3	R/W	PMA_REG_RX_SLIP_SEL	slip output selection signal based on counter value of slip control
2	R/W	PMA_REG_RX_SLIP_SEL_EN	Overwrite of enable signal of reg_rx_slip_sel 1'b0: Corresponds to parameter value "FALSE", controlled by internal circuit 1'b1: Corresponds to parameter value "TRUE", controlled by register PMA_REG_RX_SLIP_SEL
1	R/W	PMA_REG_TX_DCC_DISABLE	Reserved
0	R/W	PMA_REG_RX_DCC_DISABLE	Reserved

Table 5-115 Description of PMA Channel Configuration Register: pma_rx_reg33, Offset Address 0x021

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R/W	PMA_REG_RX_SIGDET_STATUS	Receive signal detection status: 1'b0: Corresponds to parameter value "FALSE", no signal detected 1'b1: Corresponds to parameter value "TRUE", input signal detected
4	R/W	PMA_REG_RX_SIGDET_STATUS_OW	Overwrite of RX signal detection status 1'b0: Corresponds to parameter value "DISABLE", controlled by internal circuit 1'b1: Corresponds to parameter value "ENABLE", controlled by register PMA_REG_RX_SIGDET_STATUS
3	R/W	PMA_REG_RX_SIGDET_FSM_RST_N	Reserved
2:0	R/W	PMA_REG_RX_SIGDET_STATUS_SEL	Reserved

Table 5-116 Description of PMA Channel Configuration Register: pma_rx_reg34, Offset Address 0x022

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_RX_SIGDET_CH2_SEL	Reserved
6	R/W	PMA_REG_RX_SIGDET_PULSE_EXT	Reserved
5:4	R/W	PMA_REG_RX_SIGDET_GRM	Reserved
3:0	R/W	PMA_REG_RX_SIGDET_VTH	Reserved

Table 5-117 Description of PMA Channel Configuration Register: pma_rx_reg35, Offset Address 0x023

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R/W	PMA_REG_RX_SIGDET_CHK_WINDOW_EN	Reserved
4:0	R/W	PMA_REG_RX_SIGDET_CH2_CHK_WINDOW	Reserved

Table 5-118 Description of PMA Channel Configuration Register: pma_rx_reg36, Offset Address 0x024

Bits	R/W	Corresponding Parameter Name	Description
7:5	R/W	PMA_REG_RX_SIGDET_OOB_DET_COUNT_VAL[2:0]	Reserved
4	R/W	PMA_REG_SLIP_FIFO_INV	Reserved
3	R/W	PMA_REG_SLIP_FIFO_INV_EN	Reserved
2:0	R/W	PMA_REG_RX_SIGDET_NOSIG_COUNT_SETTING	Reserved

Table 5-119 Description of PMA Channel Configuration Register: pma_rx_reg37, Offset Address 0x025

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved
4:2	R/W	PMA_REG_RX_SIGDET_4OOB_DET_SEL	Reserved
1:0	R/W	PMA_REG_RX_SIGDET_OOB_DET_COUNT_VAL[4:3]	Reserved

Table 5-120 Description of PMA Channel Configuration Register: pma_rx_reg38, Offset Address 0x026

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_RX_OOB_DETECTOR_PD_OW	Reserved
6	R/W	PMA_REG_RX_OOB_DETECTOR_RESET_N	Reserved
5	R/W	PMA_REG_RX_OOB_DETECTOR_RESET_N_OW	Reserved
4:1	R/W	PMA_REG_RX_SIGDET_IC_I	Reserved
0	R		Reserved

Table 5-121 Description of PMA Channel Configuration Register: pma_rx_reg39, Offset Address 0x027

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved
4	R/W	REG_CTLE_CTRL[0]	Reserved
3:2	R/W	REG_RX_TERM_CM_CTRL	Reserved
1	R		Reserved
0	R/W	PMA_REG_RX_OOB_DETECTOR_PD	Reserved

Table 5-122 Description of PMA Channel Configuration Register: pma_rx_reg40, Offset Address 0x028

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	pma_lane_reg_status_0to7	RX BIST error count PMA_CHx_REG_RX_ERR_COUNTER[7:0]

Table 5-123 Description of PMA Channel Configuration Register: pma_rx_reg41, Offset Address 0x029

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	pma_lane_reg_status_8to15	RX BIST error count PMA_CHx_REG_RX_ERR_COUNTER[15:8]

Table 5-124 Description of PMA Channel Configuration Register: pma_rx_reg42, Offset Address 0x02a

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	pma_lane_reg_status_16to23	RX BIST error count PMA_CHx_REG_RX_ERR_COUNTER[23:16]

Table 5-125 Description of PMA Channel Configuration Register: pma_rx_reg43, Offset Address 0x02b

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	pma_lane_reg_status_24to31	RX BIST error count PMA_CHx_REG_RX_ERR_COUNTER[31:24]

Table 5-126 Description of PMA Channel Configuration Register: pma_rx_reg44, Offset Address 0x02c

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	pma_lane_reg_status_39to32	Reserved

Table 5-127 Description of PMA Channel Configuration Register: pma_rx_reg45, Offset Address 0x02d

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	pma_lane_reg_status_47to40	Reserved

Table 5-128 Description of PMA Channel Configuration Register: pma_rx_reg46, Offset Address 0x02e

Bits	R/W	Corresponding Parameter Name	Description
7:4	R/W	PMA_REG_RX_RESERVED	Reserved
3:0	R	pma_lane_reg_status_48to51	Reserved

Table 5-129 Description of PMA Channel Configuration Register: pma_rx_reg47, Offset Address 0x02f

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	pma_lane_reg_status_52to59	Receiver CDR PI Value Under the scenario with no frequency difference, the CDR converges when this parameter stabilizes around a certain value PMA_CHx_REG_PICTRL_STATUS[7:0]

Table 5-130 Description of PMA Channel Configuration Register: pma_rx_reg48, Offset Address 0x030

Bits	R/W	Corresponding Parameter Name	Description
7:2	R	pma_lane_reg_status_62to67	Reserved
1	R	pma_lane_reg_status_61	Receiver Signal Detection Status PMA_CHx_REG_RX_SIGDET_STATUS
0	R	pma_lane_reg_status_60	Receiver CDR READY Status PMA_CHx_REG_RX_CDR_READY

Table 5-131 Description of PMA Channel Configuration Register: pma_rx_reg49, Offset Address 0x031

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	pma_lane_reg_status_68to75	Reserved

Table 5-132 Description of PMA Channel Configuration Register: pma_rx_reg50, Offset Address 0x032

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:0	R	pma_lane_reg_status_76to81	Reserved

Table 5-133 Description of PMA Channel Configuration Register: pma_rx_reg51, Offset Address 0x033

Bits	R/W	Corresponding Parameter Name	Description
7:1	R		Reserved
0	R	pma_lane_reg_status_82	Reserved

Table 5-134 Description of PMA Channel Configuration Register: pma_rx_reg52, Offset Address 0x034

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	pma_lane_reg_status_90to97	Reserved

Table 5-135 Description of PMA Channel Configuration Register: pma_rx_reg53, Offset Address 0x035

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	pma_lane_reg_status_98to105	Reserved

Table 5-136 Description of PMA Channel Configuration Register: pma_rx_reg54, Offset Address 0x036

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	pma_lane_reg_status_106to113	Reserved

Table 5-137 Description of PMA Channel Configuration Register: pma_rx_reg55, Offset Address 0x037

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	pma_lane_reg_status_114to121	Reserved

Table 5-138 Description of PMA Channel Configuration Register: pma_rx_reg56, Offset Address 0x038

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:0	R	pma_lane_reg_status_122to127	Reserved

5.3.2 PMA TX Section

Table 5-139 Description of PMA Channel Configuration Register: pma_tx_reg0, Offset Address 0x039

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_TX_RXDET_REQ	Reserved
6	R/W	PMA_TX_RXDET_REQ_OW	Reserved
5:4	R/W	PMA_REG_TX_BEACON_TIMER_SEL	Reserved
3	R/W	PMA_TX_CLKPATH_PD_OW	enable the clock path power down control from register 1'b0: Corresponds to parameter value "DISABLE", controlled by internal circuit 1"b1: Corresponds to parameter value "ENABLE", controlled by the register PMA_TX_CLKPATH_PD
2	R/W	PMA_TX_CLKPATH_PD	1"b0: Transmitter clock path power is on; 1"b1: Transmitter clock path power is off

Bits	R/W	Corresponding Parameter Name	Description
1	R/W	PMA_TX_PD_OW	enable TX power down control from register 1'b0: Corresponds to parameter value "DISABLE", controlled by internal circuit 1"b1: Corresponds to parameter value "ENABLE", controlled by the register PMA_TX_PD
0	R/W	PMA_TX_PD	1"b0: Transmitter power is on; 1"b1: Transmitter power is off

Table 5-140 Description of PMA Channel Configuration Register: pma_tx_reg1, Offset Address 0x03a

Bits	R/W	Corresponding Parameter Name	Description
7:4	R		Reserved
3	R/W	PMA_REG_TX_EI_EN	register Electric Ideal enable 1'b0: no EI; 1'b1: EI mode
2	R/W	PMA_REG_TX_EI_EN_OW	Overwrite of Electric Ideal enable register 1'b0: Corresponds to parameter value "FALSE", controlled by internal circuit 1"b1: Corresponds to parameter value "TRUE", controlled by the register PMA_REG_TX_EI_EN
1	R/W	PMA_REG_TX_BEACON_EN	Reserved
0	R/W	PMA_REG_TX_BEACON_EN_OW	Reserved

Table 5-141 Description of PMA Channel Configuration Register: pma_tx_reg2, Offset Address 0x03b

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_TX_ BIAS_CAL_EN	Reserved
6:1	R/W	PMA_REG_TX_RES_CAL	Reserved
0	R/W	PMA_REG_TX_ RES_CAL_EN	Reserved

Table 5-142 Description of PMA Channel Configuration Register: pma_tx_reg3, Offset Address 0x03c

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:0	R/W	PMA_REG_TX_BIAS_CTRL	Reserved

Table 5-143 Description of PMA Channel Configuration Register: pma_tx_reg4, Offset Address 0x03d

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved

Table 5-144 Description of PMA Channel Configuration Register: pma_tx_reg5, Offset Address 0x03e

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	PMA_REG_TX_RESERVED	Reserved

Table 5-145 Description of PMA Channel Configuration Register: pma_tx_reg6, Offset Address 0x03f

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	PMA_REG_TX_RESERVED	Reserved

Table 5-146 Description of PMA Channel Configuration Register: pma_tx_reg7, Offset Address 0x040

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	PMA_REG_TX_RXDET_TIMER_SEL	Reserved
5;0	R		Reserved

Table 5-147 Description of PMA Channel Configuration Register: pma_tx_reg8, Offset Address 0x041

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_TX_DCC_RESET_N	Reserved
6	R/W	PMA_REG_TX_DCC_RESET_N_OW	Reserved
5	R/W	PMA_REG_TX_ RESET_N	TX reset enable, active Low 1'b0: TX reset; 1'b1: TX not reset
4	R/W	PMA_REG_TX_RESET_N_OW	Overwrite of TX reset n register 1'b0: Corresponds to parameter value "FALSE", controlled by internal circuit 1'b1: Corresponds to parameter value "TRUE", controlled by register PMA_REG_TX_RESET_N
3	R/W	PMA_REG_TX_PD_POST_OW	Overwrite of REG_TX_PD_POSE 1'b0: Corresponds to parameter value "DISABLE", controlled by internal circuit 1'b1: Corresponds to parameter value "ENABLE", controlled by register PMA_REG_TX_PD_POST
2	R/W	PMA_REG_TX_PD_POST	Post-cursor de-emphasis enable 1'b0: Corresponds to parameter value "ON", enabled 1'b1: Corresponds to parameter value "OFF", disabled
1	R/W	PMA_REG_TX_SYNC	Reserved
0	R/W	PMA_REG_TX_SYNC_OW	Reserved

Table 5-148 Description of PMA Channel Configuration Register: pma_tx_reg9, Offset Address 0x042

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R/W	PMA_REG_PLL_READY	register pll ready enable 1'b0: pll not ready; 1'b1: pll ready
4	R/W	PMA_REG_PLL_READY_OW	Overwrite of pll ready register 1'b0: Corresponds to parameter value "FALSE", controlled by port P_PLL_READY 1'b1: Corresponds to parameter value "TRUE", controlled by register PMA_REG_PLL_READY
3:1	R/W	PMA_REG_TX_BUSWIDTH	bit[2] is reserved bit[1:0]TX buswidth control 2’b00: 8bit;2’b01:10bit;2’b10:16bit;2’b11:20bit

Bits	R/W	Corresponding Parameter Name	Description
0	R/W	PMA_REG_TX_BUSWIDTH_OW	Overwrite of TX buswidth register 1'b0: Corresponds to parameter value "DISABLE", controlled by internal circuit 1'b1: Corresponds to parameter value "ENABLE", controlled by the register PMA_REG_TX_BUSWIDTH

Table 5-149 Description of PMA Channel Configuration Register: pma_tx_reg10, Offset Address 0x043

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R		Reserved
4:3	R/W	PMA_REG_EI_PCLK_DELAY_SEL	Reserved
2	R		Reserved
1	R/W	PMA_REG_EI_PCLK_SW	Reserved
0	R/W	PMA_REG_EI_PCLK_SW_OW	Reserved

Table 5-150 Description of PMA Channel Configuration Register: pma_tx_reg11, Offset Address 0x044

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:0	R/W	PMA_REG_TX_DRV01_DAC0	The correspondence between post-cursorde-emphasis configuration value and gain

Setting	Gain(dB)
6’b00_0000	0.01
6’b00_0001	0.14
6’b00_0010	0.27
6’b00_0011	0.38
6’b00_0100	0.50
6’b00_0101	0.63
6’b00_0110	0.75
6’b00_0111	0.88
6’b00_1000	1.02
6’b00_1001	1.13
6’b00_1010	1.27
6’b00_1011	1.40
6’b00_1100	1.54
6’b00_1101	1.67
6’b00_1110	1.83
6’b00_1111	1.95
6’b01_0000	2.00
6’b01_0001	2.13
6’b01_0010	2.28

Bits	R/W	Corresponding Parameter Name	Description	
			6’b01_0011	2.42
			6’b01_0100	2.56
			6’b01_0101	2.70
			6’b01_0110	2.85
			6’b01_0111	2.99
			6’b01_1000	3.14
			6’b01_1001	3.27
			6’b01_1010	3.41
			6’b01_1011	3.56
			6’b01_1100	3.70
			6’b01_1101	3.85
			6’b01_1110	4.02
			6’b01_1111	4.19
			6’b10_0000	4.30
			6’b10_0001	4.46
			6’b10_0010	4.61
			6’b10_0011	4.77
			6’b10_0100	4.93
			6’b10_0101	5.10
			6’b10_0110	5.28
			6’b10_0111	5.45
			6’b10_1000	5.62
			6’b10_1001	5.80
			6’b10_1010	5.99
			6’b10_1011	6.17
			6’b10_1100	6.35
			6’b10_1101	6.53
			6’b10_1110	6.72
			6’b10_1111	6.92
			6’b11_0000	6.98
			6’b11_0001	7.17
			6’b11_0010	7.36
			6’b11_0011	7.56
			6’b11_0100	7.77
			6’b11_0101	7.97
			6’b11_0110	8.19
			6’b11_0111	8.40
			6’b11_1000	8.63
			6’b11_1001	8.83

Bits	R/W	Corresponding Parameter Name	Description
			6'b11_1010 9.05 6'b11_1011 9.27 6'b11_1100 9.49 6'b11_1101 9.69 6'b11_1110 9.97 6'b11_1111 10.18 Note: The values of post-cursorde-emphasis levels in the table are typical values

Table 5-151 Description of PMA Channel Configuration Register: pma_tx_reg12, Offset Address 0x045

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:0	R/W	PMA_REG_TX_DRV01_DAC1	Reserved

Table 5-152 Description of PMA Channel Configuration Register: pma_tx_reg13, Offset Address 0x046

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:0	R/W	PMA_REG_TX_DRV01_DAC2	Reserved

Table 5-153 Description of PMA Channel Configuration Register: pma_tx_reg14, Offset Address 0x047

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:0	R/W	PMA_REG_TX_DRV00_DAC0	main cursor TX bias ctrl code setting

Table 5-154 Description of PMA Channel Configuration Register: pma_tx_reg15, Offset Address 0x048

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:0	R/W	PMA_REG_TX_DRV00_DAC1	Reserved

Table 5-155 Description of PMA Channel Configuration Register: pma_tx_reg16, Offset Address 0x049

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:0	R/W	PMA_REG_TX_DRV00_DAC2	Reserved

Table 5-156 Description of PMA Channel Configuration Register: pma_tx_reg17, Offset Address 0x04a

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:0	R/W	PMA_REG_TX_AMP0	TX swing source register AMP0 When the post-cursorde-emphasis

<table>
<tr><th>Bits</th><th>R/W</th><th>Corresponding Parameter Name</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>PMA_REG_TX_DRV01_DAC0 is configured to 0, the corresponding values of (Vp-Vn)p2p are as follows:
<table>
<tr><th>Setting</th><th>$(V_p - V_n)_{p2p}$(mV)</th></tr>
<tr><td>5’b0_0101</td><td>370.8</td></tr>
<tr><td>5’b0_0110</td><td>437.5</td></tr>
<tr><td>5’b0_0111</td><td>498.2</td></tr>
<tr><td>5’b0_1000</td><td>543.5</td></tr>
<tr><td>5’b0_1001</td><td>601.1</td></tr>
<tr><td>5’b0_1010</td><td>655.5</td></tr>
<tr><td>5’b0_1011</td><td>704.9</td></tr>
<tr><td>5’b0_1100</td><td>762.3</td></tr>
<tr><td>5’b0_1101</td><td>805.9</td></tr>
<tr><td>5’b0_1110</td><td>847.8</td></tr>
<tr><td>5’b0_1111</td><td>880.5</td></tr>
<tr><td>5’b1_0000</td><td>906.9</td></tr>
<tr><td>5’b1_0001</td><td>924.0</td></tr>
<tr><td>5’b1_0010</td><td>932.2</td></tr>
<tr><td>5’b1_0011</td><td>935.1</td></tr>
<tr><td>others</td><td>Reserved</td></tr>
</table>
Note: The values of voltage levels in the table are typical values</td></tr>
</table>

Table 5-157 Description of PMA Channel Configuration Register: pma_tx_reg18, Offset Address 0x04b

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:0	R/W	PMA_REG_TX_AMP1	Reserved

Table 5-158 Description of PMA Channel Configuration Register: pma_tx_reg19, Offset Address 0x04c

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:0	R/W	PMA_REG_TX_AMP2	Reserved

Table 5-159 Description of PMA Channel Configuration Register: pma_tx_reg20, Offset Address 0x04d

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:0	R/W	PMA_REG_TX_AMP3	Reserved

Table 5-160 Description of PMA Channel Configuration Register: pma_tx_reg21, Offset Address 0x04e

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5:0	R/W	PMA_REG_TX_AMP4	Reserved

Table 5-161 Description of PMA Channel Configuration Register: pma_tx_reg22, Offset Address 0x04f

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved
6	R/W	PMA_REG_TX_DEEMP_OW	Reserved
5:4	R/W	PMA_REG_TX_DEEMP	Reserved
3	R/W	PMA_REG_TX_MARGIN_OW	Reserved
2:0	R/W	PMA_REG_TX_MARGIN	Reserved

Table 5-162 PMA Channel Configuration Register Description: pma_tx_reg23, Offset Address 0x050

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_TX_BEACON_OSC_CTRL	Reserved
6:5	R		Reserved
4:3	R/W	PMA_REG_TX_RXDET_THRESHOLD	Reserved
2	R		Reserved
1	R/W	PMA_REG_TX_SWING_OW	Overwrite of signal of TX_swing 1"b0: Corresponds to parameter value "FALSE", controlled by internal circuit 1"b1: Corresponds to parameter value "TRUE", controlled by the register PMA_REG_TX_SWING
0	R/W	PMA_REG_TX_SWING	1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"

Table 5-163 PMA Channel Configuration Register Description: pma_tx_reg24, Offset Address 0x051

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_TX_RXDET_STATUS	RX detect status force value 1'b0: RX not detected, floating 1'b1: RX detected, 50-ohm termination
6	R/W	PMA_REG_TX_RXDET_STATUS_OW	register RX detect status force enable 1'b0: Corresponds to parameter value "FALSE", controlled by internal circuit 1'b1: Corresponds to parameter value "TRUE", controlled by the register PMA_REG_TX_RXDET_STATUS
5	R/W	PMA_REG_TX_PCLK_EDGE_SEL	1"b0: Corresponds to parameter value "POS_EDGE" 1"b1: Corresponds to parameter value "NEG_EDGE"
4	R/W	PMA_REG_TX_TX2RX_SLPBACK_EN	PMA serial loopback enable, active-high 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"
3:2	R/W	PMA_REG_TX_PREDRV_CM_CTRL	Reserved
1:0	R/W	PMA_REG_TX_PREDRV_DAC	Reserved

Table 5-164 PMA Channel Configuration Register Description: pma_tx_reg25, Offset Address 0x052

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved
4:3	R/W	PMA_REG_TX_PRBS_SEL	PMA TX PRBS mode selection 2'b00:PRBS7; 2'b01:PRBS15 2'b10:PRBS23; 2'b11:PRBS31
2:1	R/W	PMA_REG_TX_PRBS_GEN_WIDTH_SEL	PMA TX PRBS width select 2'b00:8 bit; 2'b01:10 bit; 2'b10:16 bit; 2'b11:20 bit
0	R/W	PMA_REG_TX_PRBS_GEN_EN	PMA TX PRBS generator enable, active-high 1"b0: Corresponds to parameter value "FALSE"; 1"b1: Corresponds to parameter value "TRUE"

Table 5-165 PMA Channel Configuration Register Description: pma_tx_reg26, Offset Address 0x053

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_TX_UDP_DATA_7_TO_0	Reserved

Table 5-166 PMA Channel Configuration Register Description: pma_tx_reg27, Offset Address 0x054

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_TX_UDP_DATA_15_TO_8	Reserved

Table 5-167 PMA Channel Configuration Register Description: pma_tx_reg28, Offset Address 0x055

Bits	R/W	Corresponding Parameter Name	Description
7:5	R/W	PMA_REG_TX_FIFO_WP_CTRL	Reserved
4	R		Reserved
3:0	R/W	PMA_REG_TX_UDP_DATA_19_TO_16	Reserved

Table 5-168 PMA Channel Configuration Register Description: pma_tx_reg29, Offset Address 0x056

Bits	R/W	Corresponding Parameter Name	Description
7:4	R		Reserved
3	R/W	PMA_REG_TX_ERR_INSERT	PRBS error code injection For each transition from 0 to 1, one error injection operation is performed, with the number of injected error bits being variable 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"
2:1	R/W	PMA_REG_TX_DATA_MUX_SEL	Data selection control signal 2'b00: data from pcs; 2'b01: prbs data 2'b10: udp data; 2'b11: RX loopback data
0	R/W	PMA_REG_TX_FIFO_EN	Register configuration TX_fifo_en enable, 1"b0: Corresponds to parameter value "FALSE", disable 1"b1: Corresponds to parameter value "TRUE", enable When TX PMA PRBS function or PMA far-end parallel loopback is used, it is necessary to set to 1, and the default value under normal conditions is 0

Table 5-169 PMA Channel Configuration Register Description: pma_tx_reg30, Offset Address 0x057

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R/W	PMA_REG_RATE_CHANGE_TXPCLK_ON	Reserved
4	R/W	PMA_REG_RATE_CHANGE_TXPCLK_ON_OW	Reserved
3:2	R		Reserved
1	R/W	PMA_CH_REG_TX_SATA_EN	Reserved
0	R		Reserved

Table 5-170 PMA Channel Configuration Register Description: pma_tx_reg31, Offset Address 0x058

Bits	R/W	Corresponding Parameter Name	Description
7:5	R/W	PMA_REG_TX_PULLUP_DAC1_0TO2	Reserved
4:0	R/W	PMA_REG_TX_PULLUP_DAC0_0TO4	Reserved

Table 5-171 PMA Channel Configuration Register Description: pma_tx_reg32, Offset Address 0x059

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_TX_PULLUP_DAC3_0	Reserved
6:2	R/W	PMA_REG_TX_PULLUP_DAC2_0TO4	Reserved
1:0	R/W	PMA_REG_TX_PULLUP_DAC1_3TO4	Reserved

Table 5-172 PMA Channel Configuration Register Description: pma_tx_reg33, Offset Address 0x05a

Bits	R/W	Corresponding Parameter Name	Description
7:4	R/W	PMA_REG_TX_OOB_DELAY_SEL	Reserved
3:0	R	PMA_REG_TX_PULLUP_DAC3_1TO4	Reserved

Table 5-173 PMA Channel Configuration Register Description: pma_tx_reg34, Offset Address 0x05b

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_RX_JTAG_MODE_EN	Reserved
6	R/W	PMA_REG_RX_JTAG_MODE_EN_OW	Reserved
5	R	PMA_REG_TX_JTAG_MODE_EN	Reserved
4	R/W	PMA_REG_TX_JTAG_MODE_EN_OW	Reserved
3	R/W	PMA_REG_TX_LS_MODE_EN	Reserved
2:1	R/W	PMA_REG_TX_SLPBK_AMP	Reserved
0	R/W	PMA_REG_TX_POLARITY	PMA TX polarity inversion 1"b0: Corresponds to parameter value "NORMAL", txpdata_out[19:0] = txpdata_in[19:0] 1"b1: Corresponds to parameter value "REVERSE",

Bits	R/W	Corresponding Parameter Name	Description
			txpdata_out[19:0] = ~txpdata_in[19:0]

Table 5-174 PMA Channel Configuration Register Description: pma_tx_reg35, Offset Address 0x05c

Bits	R/W	Corresponding Parameter Name	Description
7:5	R/W	PMA_REG_RX_TERM_MODE_CTRL	Related to IP configuration 3'b010: external DC, internal DC 3'b100: external DC, internal AC 3'b101: external AC, internal AC 3'b110: external AC, internal DC
4	R/W	PMA_REG_TX_FBCLK_FAR_EN	Reserved
3:1	R/W	PMA_REG_RX_ACJTAG_VHYSTSEL	Reserved
0	R/W	PMA_REG_RX_JTAG_OE	Reserved

Table 5-175 PMA Channel Configuration Register Description: pma_tx_reg36, Offset Address 0x05d

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		Reserved
2	R/W	PMA_REG_PLPBK_TXPCLK_EN	1"b0: Corresponds to parameter value "FALSE", parallel loopback mode, using rxpclk. 1"b1: Corresponds to parameter value "TRUE", normal working mode, using txpclk When in PMA and PCS far-end loopback mode, it is necessary to set to 1, and the default value under normal working mode is 0
1:0	R		Reserved

Table 5-176 PMA Channel Configuration Register Description: pma_tx_reg37, Offset Address 0x05e

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved

Table 5-177 PMA Channel Configuration Register Description: pma_tx_reg38, Offset Address 0x05f

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved

Table 5-178 PMA Channel Configuration Register Description: pma_tx_reg39, Offset Address 0x060

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved

Table 5-179 PMA Channel Configuration Register Description: pma_tx_reg40, Offset Address 0x061

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved

Table 5-180 PMA Channel Configuration Register Description: pma_tx_reg41, Offset Address 0x062

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved

Table 5-181 PMA Channel Configuration Register Description: pma_tx_reg42, Offset Address 0x063

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved

Table 5-182 PMA Channel Configuration Register Description: pma_tx_reg43, Offset Address 0x064

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved

Table 5-183 PMA Channel Configuration Register Description: pma_tx_reg44, Offset Address 0x065

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved

Table 5-184 PMA Channel Configuration Register Description: pma_tx_reg45, Offset Address 0x066

Bits	R/W	Corresponding Parameter Name	Description
7:5	R/W	PMA_REG_CTLE_INIT_DAC[2:0]	Reserved
4	R/W	PMA_REG_CTLE_HOLD	Reserved
3	R/W	PMA_REG_CTLE_FORCE_SEL	Reserved
2:0	R/W	PMA_REG_CTLE_CTRL[3:1]	Reserved

Table 5-185 PMA Channel Configuration Register Description: pma_tx_reg46, Offset Address 0x067

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R/W	PMA_REG_CTLE_THRESHOLD[0]	Reserved
4:2	R/W	PMA_REG_CTLE_SHIFTER_GAIN	Reserved
1	R/W	PMA_REG_CTLE_POLARITY	Reserved
0	R/W	PMA_REG_CTLE_INIT_DAC[3]	Reserved

Table 5-186 PMA Channel Configuration Register Description: pma_tx_reg47, Offset Address 0x068

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_CTLE_THRESHOLD [8:1]	Reserved

Table 5-187 PMA Channel Configuration Register Description: pma_tx_reg48, Offset Address 0x069

Bits	R/W	Corresponding Parameter Name	Description
7:5	R/W	PMA_REG_CDR_READY_THD [2:0]	Reserved

Bits	R/W	Corresponding Parameter Name	Description
4:3	R/W	PMA_REG_CDR_READY_CHECK_CTRL	Reserved
2:0	R/W	PMA_REG_CTLE_THRESHOLD [11:9]	Reserved

Table 5-188 PMA Channel Configuration Register Description: pma_tx_reg49, Offset Address 0x06a

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_CDR_READY_THD [10:3]	Reserved

Table 5-189 PMA Channel Configuration Register Description: pma_tx_reg50, Offset Address 0x06b

Bits	R/W	Corresponding Parameter Name	Description
7:2	R/W	PMA_REG_EQ_DAC	Reserved
1	R/W	PMA_REG_EQ_DAC_OW	Reserved
0	R/W	PMA_REG_CDR_READY_THD[11]	Reserved

Table 5-190 PMA Channel Configuration Register Description: pma_tx_reg51, Offset Address 0x06c

Bits	R/W	Corresponding Parameter Name	Description
7:4	R		Reserved
3	R/W	PMA_REG_ANA_RX_EQ_R_SET_OW	Reserved
2	R/W	PMA_REG_EQ_DC_CALIB_SEL	Reserved
1	R/W	PMA_REG_EQ_DC_CALIB_SEL_OW	Reserved
0	R/W	PMA_REG_EQ_DC_CALIB_EN	Reserved

Table 5-191 PMA Channel Configuration Register Description: pma_tx_reg52, Offset Address 0x06d

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved
6	R/W	PMA_REG_CTLE_ADP_RSTN	Reset of CTLE adapter module for the channel 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"
5	R/W	PMA_REG_TX_PMA_RSTN	Lane's TX channel reset configuration 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"
4	R/W	PMA_REG_TX_LANE_POWERUP	Lane's TX channel power-up configuration 1'b0: Corresponds to parameter value "OFF"; 1'b1: Corresponds to parameter value "ON"
3	R/W	PMA_REG_RX_PMA_RSTN	Lane's RX channel reset configuration 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"
2	R/W	PMA_REG_RX_LANE_POWERUP	Lane's RX channel power-up configuration 1'b0: Corresponds to parameter value "OFF"; 1'b1: Corresponds to parameter value "ON"
1	R/W	PMA_REG_PMA_POR_N	Lane reset configuration 1'b0: Corresponds to parameter value "FALSE"; 1'b1: Corresponds to parameter value "TRUE"

Bits	R/W	Corresponding Parameter Name	Description
0	R/W	PMA_REG_LANE_POWERUP	Lane power-up configuration 1'b0: Corresponds to parameter value "OFF"; 1'b1: Corresponds to parameter value "ON"

Appendix A: HSST Pin Location Description

Table A-1 HSST Pin Locations

Device Model/Package	Constrained Location	Corresponding Pin: P/N
PGL50H FBG484	HSST_88_340	LANE0 TX:B6/A6
		LANE0 RX:D7/C7
		LANE1 TX:B8/A8
		LANE1 RX:D9/C9
		LANE2 TX:B14/A14
		LANE2 RX:D13/C13
		LANE3 TX:B16/A16
		LANE3 RX:D15/C15
		REFCLK0:A10/B10
		REFCLK1:A12/B12
PGL100H FBG900	HSST_120_588	LANE0 TX:B9/A9
		LANE0 RX:D10/C10
		LANE1 TX:B11/A11
		LANE1 RX:D12/C12
		LANE2 TX:B21/A21
		LANE2 RX:D20/C20
		LANE3 TX:B23/A23
		LANE3 RX:D22/C22
		REFCLK0:B13/A13
		REFCLK1:C18/D18
	HSST_120_0	LANE0 TX:AJ9/AK9
		LANE0 RX:AG10/AH10
		LANE1 TX:AJ11/AK11
		LANE1 RX:AG12/AH12
		LANE2 TX:AJ21/AK21
		LANE2 RX:AG20/AH20
		LANE3 TX:AJ23/AK23
		LANE3 RX:AG22/AH22
		REFCLK0:AJ13/AK13
		REFCLK1:AG18/AH18

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