# Logos Family PGL12G and PGL22G Device Configurable Multi-function IOs Application Guide

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**Shenzhen Pango Microsystems Co., Ltd.**

# Revisions History

## Document Revisions

| Version | Date of Release | Revisions |
|---|---|---|
| V1.0 | 13.12.2021 | Initial release. |
| | | |

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# Chapter 1 Overview

A configurable multi-function PIN can be used as a configuration interface during the configuration, and after the completion of the configuration, it can be used as a standard IO for the user in user mode. Some considerations on using a configurable multi-function IO as a user IO shall be taken into account in the single board design. The configurable multi-function IOs for PGL12G and PGL22G devices are all on BANKL0, BANKR0, or BANKR1. See details in Table 2-1 and Table 2-2. So there is no need to consider the application of configurable multi-function IOs in other banks.

Configurable multi-function IOs must be used with the considerations in mind to avoid the following problem scenario: In user mode, resetting should be used to reconfigure the FPGA, and use a configurable multi-function IO as an output for user logic, then after resetting, the multi-function IO output will be in a non-high impedance state for a brief period (less than 100ns) (some IOs at a high level and some at a low level) and not controlled by IO_STATUS_C.

The process is shown in the following figure.

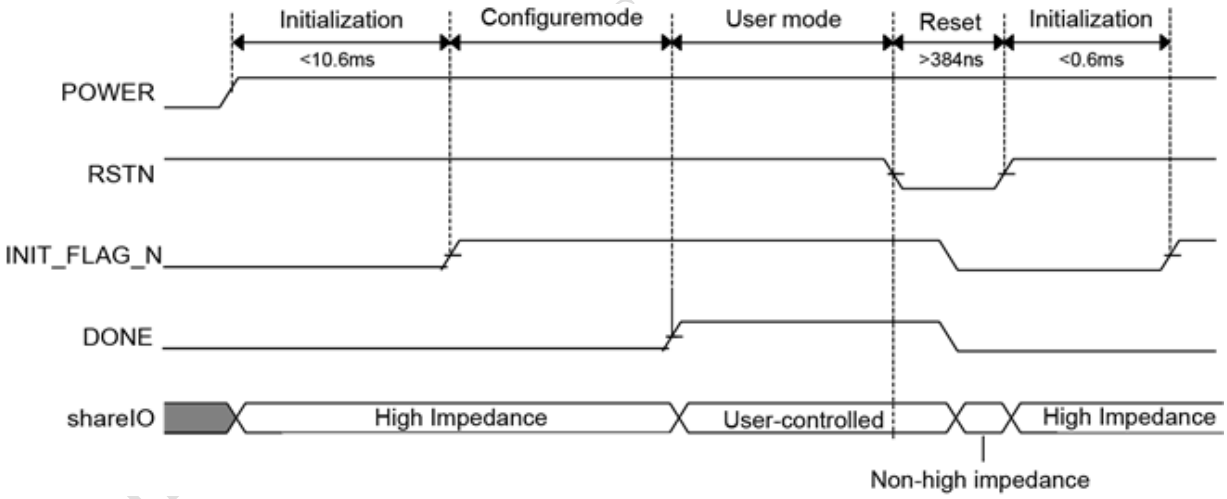


Figure 1-1 Non-High Impedance Process Diagram

This scenario mainly affects applications that require IO to maintain a fixed level during the reconfiguration process. For example, use a configurable multi-function IO as the enable or reset signal for other devices and keep the signal at a fixed level during the configuration by applying an external pull-up (or pull-down) of the FPGA. In this case, it is expected that after the FPGA is reset, the configurable multi-function IO output will be in a high impedance state, but the existence of the non-high impedance process may cause changes to the enable or reset signal, affecting the operation of other devices.

The possible triggers include:

1. Resetting FPGA in user mode
2. When resetting FPGA, a configurable multi-function IO is used as user output.

The following solutions are provided for user single board design for this scenario.

# Chapter 2 Configurable Multi-function IOs User Guide

For configurable multi-function IOs, the following considerations shall be taken into account during the board design.

1. If a configurable multi-function IO is used as an input in user mode, it will not affect the design.
2. If a configurable multi-function IO is used as an output in user mode, the following considerations shall be observed.
    1) Pin IO_STATUS_C requires an external pull-up.
    2) If the configurable multi-function IO used needs to be maintained at a fixed level during the configuration, select a pin using the following method: For a fixed high level of IO, choose a pin from Table 2-1 and apply an external pull-up (A pull-up resistor of 4.7K is recommended); for a fixed low level of IO, choose one from Table 2-2 and apply an external pull-down (A pull-down resistor of 4.7K is recommended).
3. If there is no need for the IO to maintain at a fixed level, no action is required.

Table 2-1 Configurable Multi-function IOs that Can Remain at a High Level during Configuration

| Bank Name | Pin Name (Function name) | Pin Number | | | | |
|---|---|---|---|---|---|---|
| | | PGL12G | | PGL22G(S) | | |
| | | LPG144 | FBG256 | LPG176 | FBG256 | MBG324 |
| L0 | DIFFIO_L0_3_N/CFG_CLK | 31 | A8 | 34 | A8 | C9 |
| L0 | DIFFIO_L0_4_P/FCS_N | 34 | D10 | 37 | D10 | B8 |
| L0 | DIFFIO_L0_4_N/CS_N | 35 | C10 | 38 | C10 | A8 |
| L0 | DIFFIO_L0_5_P/MODE_0 | 32 | B7 | 36 | B7 | B9 |
| L0 | DIFFIO_L0_5_N/MODE_1 | 33 | A7 | | A7 | A9 |
| L0 | DIFFIO_L0_6_P/MODE_2 | 37 | B10 | | B10 | C4 |
| L0 | DIFFIO_L0_6_N/VREF_L0/CSO_DOUT | 39 | A10 | | A10 | D4 |
| L0 | DIFFIO_L0_7_P/RWSEL | 36 | B6 | | B6 | B7 |
| R0 | DIFFIO_R0_3_N/ECCLKIN | 4 | E13 | 8 | E13 | C11 |
| R0 | DIFFIO_R0_4_P/FCS2_N | 3 | B12 | 3 | B12 | B10 |
| R0 | DIFFIO_R0_4_N/BFCE_N | | A12 | 2 | A12 | A10 |
| R0 | DIFFIO_R0_5_P/BFOE_N | | G11 | 7 | | B11 |
| R0 | DIFFIO_R0_5_N/BADRVO_N | | G10 | 6 | | A11 |
| R0 | DIFFIO_R0_6_P/BFWE_N | | C16 | 176 | | B12 |
| R0 | DIFFIO_R0_7_P/VS1 | 2 | B14 | 175 | B14 | B13 |
| R0 | DIFFIO_R0_7_N/VS0 | 1 | A14 | 173 | A14 | A13 |

Table 2-2 Configurable Multi-function IOs that Can Remain at a Low Level during Configuration

| Bank Name | Pin Name (Function name) | Pin Number | | | | |
|---|---|---|---|---|---|---|
| | | PGL12G | | PGL22G(S) | | |
| | | LPG144 | FBG256 | LPG176 | FBG256 | MBG324 |
| L0 | DIFFIO_L0_0_P/BUSY | 28 | E7 | 29 | E7 | E8 |
| L0 | DIFFIO_L0_7_N/INIT_FLAG_N | 38 | A6 | 40 | A6 | A7 |
| L0 | DIFFIO_L0_12_P/D0 | 48 | B3 | 49 | B3 | B4 |
| L0 | DIFFIO_L0_12_N/RRN_L0/D1 | 49 | A3 | 50 | A3 | A4 |
| L0 | DIFFIO_L0_13_P/RRP_L0/D2 | 50 | D5 | 51 | D5 | B3 |
| L0 | DIFFIO_L0_13_N/D3 | 51 | D6 | 52 | D6 | A3 |
| L0 | DIFFIO_L0_14_P/D4 | 52 | B2 | 53 | B2 | B2 |
| L0 | DIFFIO_L0_14_N/D5 | 53 | A2 | 54 | A2 | A2 |
| L0 | DIFFIO_L0_15_P/D6 | 54 | D4 | 55 | D4 | B1 |
| L0 | DIFFIO_L0_15_N/D7 | 55 | C4 | 56 | C4 | A1 |
| L0 | DIFFIO_L0_16_P/D8 | | B1 | 57 | B1 | C1 |
| L0 | DIFFIO_L0_16_N/D9 | | A1 | 59 | A1 | C2 |
| L0 | DIFFIO_L0_17_P/D10 | | E4 | 60 | E4 | G4 |
| L0 | DIFFIO_L0_17_N/D11 | | E3 | 61 | E3 | F4 |
| L0 | DIFFIO_L0_18_P/D12 | | C1 | 62 | C1 | D1 |
| L0 | DIFFIO_L0_18_N/D13 | | C2 | 63 | C2 | D2 |
| L0 | DIFFIO_L0_19_P/D14 | | F4 | 64 | F4 | E1 |
| L0 | DIFFIO_L0_19_N/D15 | | F3 | 65 | F3 | E2 |
| R0 | DIFFIO_R0_12_P/D16/ADR0 | 135 | E16 | 164 | | B17 |
| R0 | DIFFIO_R0_12_N/RRN_R0/D17/ADR1 | 133 | E15 | 163 | E14 | A17 |
| R0 | DIFFIO_R0_13_P/RRP_R0/D18/ADR2 | 132 | H13 | 162 | E12 | F11 |
| R0 | DIFFIO_R0_13_N/D19/ADR3 | 131 | H14 | 161 | | G11 |
| R0 | DIFFIO_R0_14_P/D20/ADR4 | 130 | F16 | | | E15 |
| R0 | DIFFIO_R0_14_N/D21/ADR5 | 129 | F15 | | | E16 |
| R0 | DIFFIO_R0_15_P/D22/ADR6 | 128 | J14 | | | F12 |
| R0 | DIFFIO_R0_15_N/D23/ADR7 | 127 | J13 | | | G12 |
| R0 | DIFFIO_R0_16_P/D24/ADR8 | | G16 | | | B18 |
| R0 | DIFFIO_R0_16_N/D25/ADR9 | | G15 | | | A18 |
| R0 | DIFFIO_R0_17_P/D26/ADR10 | | H10 | | | C18 |
| R0 | DIFFIO_R0_17_N/D27/ADR11 | | J10 | | | C17 |
| R0 | DIFFIO_R0_18_P/D28/ADR12 | | H16 | | | D18 |
| R0 | DIFFIO_R0_18_N/D29/ADR13 | | H15 | | | D17 |
| R0 | DIFFIO_R0_19_P/D30/ADR14 | | J12 | | | E18 |
| R0 | DIFFIO_R0_19_N/D31/ADR15 | | J11 | | | E17 |
| R1 | DIFFIO_R1_0_P/ADR16 | | K14 | | | F14 |

| Bank Name | Pin Name (Function name) | Pin Number | | | | |
|---|---|---|---|---|---|---|
| | | PGL12G | | PGL22G(S) | | |
| | | LPG144 | FBG256 | LPG176 | FBG256 | MBG324 |
| R1 | DIFFIO_R1_1_P/ADR17 | | J16 | | | F18 |
| R1 | DIFFIO_R1_1_N/ADR18 | | J15 | | | F17 |
| R1 | DIFFIO_R1_2_P/ADR19 | 123 | K11 | | | G14 |
| R1 | DIFFIO_R1_2_N/ADR20 | 122 | K12 | | | G13 |
| R1 | DIFFIO_R1_3_P/ADR21 | | K16 | | | F16 |
| R1 | DIFFIO_R1_3_N/ADR22 | | K15 | | | G16 |
| R1 | DIFFIO_R1_4_P/ADR23 | 121 | L15 | | | H14 |
| R1 | DIFFIO_R1_4_N/ADR24 | 120 | L16 | | | H13 |
| R1 | DIFFIO_R1_5_P/ADR25 | | L11 | | | G18 |

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