XAUI IP

User Guide

(UG042006, V1.5)

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Revisions History

Document Revisions

Version	Date of Release	Revisions	Applicable IP and Corresponding Versions
V1.5	19.12.2023	Initial release.	V1.5

IP Revisions

IP Version	Date of Release	Revisions
V1.5	19.12.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
APB	Advanced Peripheral Bus
CDR	Clock Data Recovery
CTC	Clock Tolerance Compensation
HSSTLP	High Speed Serial Transceiver Low Performance
MDIO	Management Data Input/Output
PCS	Physical Code Sublayer
PMA	Physical Media Attachment
XAUI	10 Gigabit Attachment Unit Interface
XGMII	10 Gigabit Media Independent Interface
IPC	IP Compiler
PDS	Pango Design Suite

Related Documentation

The following documentation is related to this manual:

1. ***Pango_Design_Suite_Quick_Start_Tutorial***
2. ***Pango_Design_Suite_User_Guide***
3. ***IP_Compiler_User_Guide***
4. ***Simulation_User_Guide***
5. ***User_Constraint_Editor_User_Guide***
6. ***Physical_Constraint_Editor_User_Guide***
7. ***Route_Constraint_Editor_User_Guide***
8. ***UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide***
9. ***UG041004_HSSTLP_IP***
10. ***IEEE 802.3-2012 Specification***

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Chapter 1 Preface

This chapter describes the scope, structure, and writing standards of this manual to help users quickly find the information they need.

1.1 Introduction of the Manual

This manual serves as a user guide for the XAUI (10 Gigabit Attachment Unit Interface) IP product launched by Pango Microsystems, primarily including the IP user guide and related information. This manual helps users quickly understand the features and usage of XAUI IP.

1.2 Writing Standards of the Manual

Table 1-1 Description of Writing Standards

Text	**Rules**
Attention	If users ignore the attention contents, they may suffer adverse consequences or fail to operate successfully due to incorrect actions.
Description	Instructions and tips provided for users.
Recommendation	Recommended settings and instructions for users.

Chapter 2 IP User Guide

This chapter provides a guide on the use of XAUI IP, including an introduction to IP, IP block diagram, IP generation process, Example Design, IP interface description, IP register description, typical applications, instructions and considerations, and IP debugging methods. More details on the design process can be found in the following PDS help documentation.

- "***Pango_Design_Suite_Quick_Start_Tutorial***"
- "***Pango_Design_Suite_User_Guide***"
- "***IP_Compiler_User_Guide***"
- "***Simulation_User_Guide***"

2.1 IP Introduction

XAUI IP is designed by Pango Microsystems for implementing high-speed communications at 10Gbps. In a 10G Ethernet system, users can connect the data link layer with the physical layer via the XAUI interface. Users can configure and generate the IP module using the IPC (IP Compiler) tool within the PDS (Pango Design Suite).

2.1.1 Key Features

XAUI IP is designed in accordance with the IEEE802.3-2012 standard, with main features as follows:

- Supports XGMII Style user interface supported;
- Supports a line rate of 4×3.125Gbps;
- Supports byte synchronization for independent channels;
- Supports byte alignment between four channels;
- Supports clock tolerance compensation within the protocol-specified frequency offset range (±100ppm);
- Supports APB or MDIO management interfaces supported;
- Supports loopback and test patterns supported;
- Supports link status reporting.

2.1.2 Applicable Devices and Packages

Table 2-1 XAUI IP Applicable Devices and Packages

Applicable Devices	**Supported Packages**
PG2L100H	ALL (except for MBG324)
PG2L100HX	ALL (except for MBG324)
PG2L50H	ALL (except for FBG256/MBG324)
PG2L25H	ALL
PG2L200H	ALL

2.2 IP Block Diagram

The XAUI IP system block diagram is shown in Figure 2-1, where the dashed lines indicate the data stream direction during loopback. For loopback configuration methods, please refer to "2.8.3.1 Loopback Mode".

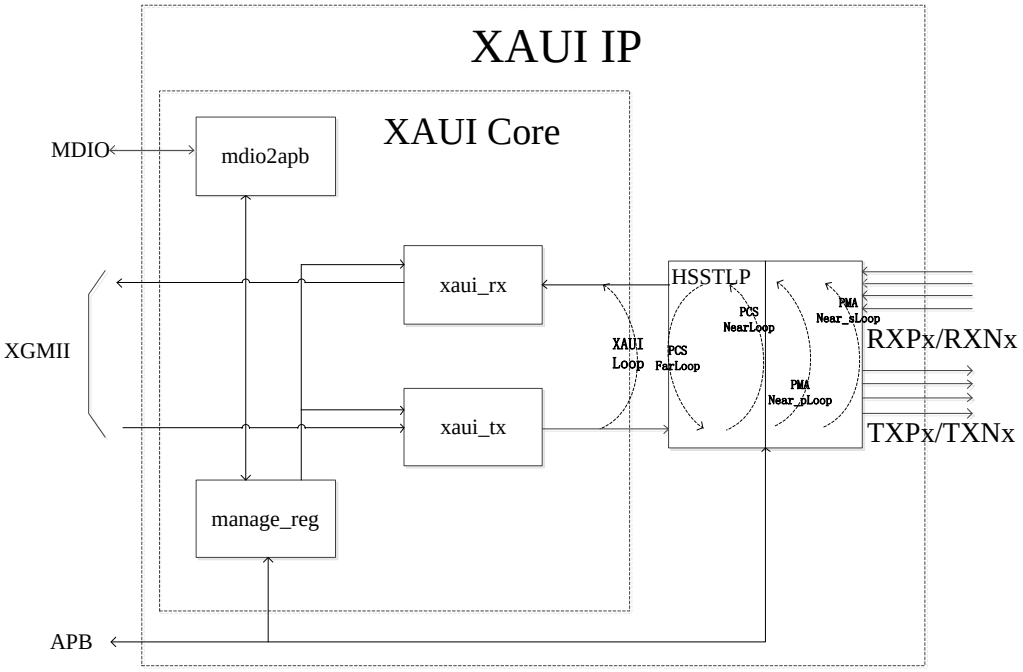

Figure 2-1 XAUI IP System Block Diagram

XAUI IP consists of the XAUI Core and HSSTLP, divided into transmission and reception directions. The XAUI Core performs functions such as conversion between XGMII data and PCS Code-Groups, and implementation of management interfaces. The HSSTLP handles encoding/decoding, serial-to-parallel conversion, parallel-to-serial conversion, clock and data

recovery, byte alignment, channel alignment, and clock tolerance compensation.

2.3 IP Generation Process

2.3.1 Module Instantiation

Users can customise the configuration of XAUI IP through the IPC tool to instantiate the required IP modules. For detailed instructions on using the IPC tool, please refer to *"**IP_Compiler_User_Guide**"*.

The main steps for instantiating the XAUI IP module are described as follows.

2.3.1.1 Selecting IP

Open IPC and click File > Update in the main window to open the Update IP dialogue box, where users add the corresponding version of the IP model.

After selecting the FPGA device type, the Catalog interface can display loaded IP models. Select the corresponding version of XAUI under the System/Ethernet directory. The IP selection path is shown in Figure 2-2. Then set the Pathname and Instance Name on the right side of the page. The project instantiation interface is shown in Figure 2-3.

Attention:

Be sure to use the software of version 2022.2 or above.

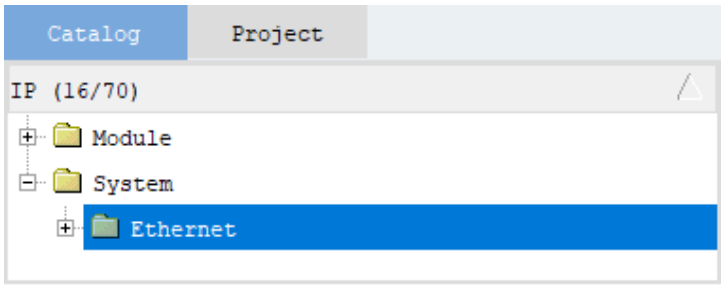

Figure 2-2 XAUI IP Selection Path

Figure 2-3 Project Instantiation Interface

2.3.1.2 IP Parameter Configuration

After selecting the IP, click <Customize> to enter the XAUI IP parameter configuration interface, with the left Symbol representing the interface block diagram, as shown in Figure 2-4; the right side is the parameter configuration window, as shown in Figure 2-5.

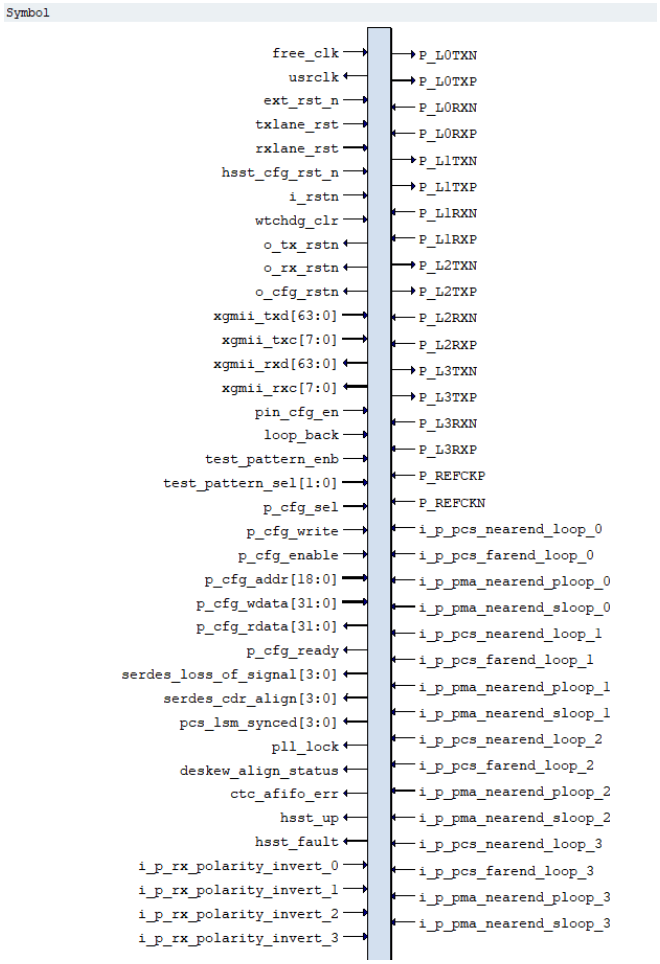

Figure 2-4 XAUI IP Interface Block Diagram

Figure 2-5 XAUI IP Parameter Configuration Interface

For XAUI IP configuration parameter descriptions, please refer to Table 2-2.

Table 2-2 Descriptions of XAUI IP Configuration Parameters

Option Domain	Parameter/Configuration Options	Parameter Description	Default Value
Data Rate	10Gbps	The data rate is 10Gbps.	Selected
Management Options	MDIO Enable	Enable the MDIO interface management channel.	Cleared

2.3.1.3 Generating IP

Upon completion of parameter configuration, click the <Generate> button in the top left corner to generate the XAUI IP and the IP code according to user-specific settings. The information report interface for IP generation is shown in Figure 2-6.

Figure 2-6 XAUI IP Generation Report Interface

Upon successful IP generation, the files indicated in Table 2-3 will be output to the project path specified in Figure 2-3.

Table 2-3 Output Files after IP Generation

Output File[1]	Description
<instance_name>.v	The top-level .v file of the generated IP.
<instance_name>.idf	The Configuration file of the generated IP.
/rtl/*.v	The plaintext RTL files of the generated IP.
/rtl/ipm2l_hsstlp_xaui/	The plaintext RTL files of the generated IP; this folder contains related files of the HSSTLP module.
/rtl/synplify/*.vp	The non-plaintext RTL files of the generated IP.
/sim_lib/ModelSim/*_sim.vp	The non-plaintext RTL files of the generated IP, which can only be used for ModelSim simulation.
/sim/modelsim/*.f	The list of .v and .vp files required for ModelSim simulation of the generated Example Design.

1 <instance_name> is the instantiation name entered by the user; "*" is a wildcard character that replaces files of the same type.

Output File[1]	Description
/sim/modelsim/*.do	The .do script files and .do waveform files for ModelSim simulation of the generated Example Design.
/sim/modelsim/*.bat	The script for ModelSim simulation of the generated Example Design.
/example_design/bench/ips2l_xaui_dut_top_sim.v	Configurations of the DUT layer simulation, such as clock, and reset.
/example_design/bench/ips2l_xaui_dut_top_tb.v	DUT layer simulation test bench.
/example_design/rtl/	The top-level file of the Example Design, DUT layer files and other used module files. For specific details, please refer to the module description of the Example Design in this chapter.
/pnr/core_only/<instance_name>.pds	The project file of the generated IP core.
/pnr/core_only/<instance_name>.fdc	The constraint file of the generated IP core.
/pnr/core_only/*.v	The top-level file for Core only.
/pnr/example_design/pango_xaui_top.pds	The project file of the Example Design.
/pnr/example_design/pango_xaui_top.fdc	The constraint file of the Example Design.
/rev_1	The default output path for synthesis reports (this folder is generated only after specifying the synthesis tool).
readme.txt	The readme file describes the structure of the generation directory after the IP is generated.

2.3.2 Constraint Configuration

For the specific configuration method of constraint files, please refer to the relevant help documents in the PDS installation path: "***User_Constraint_Editor_User_Guide***", "***Physical_Constraint_Editor_User_Guide***", "***Route_Constraint_Editor_User_Guide***".

2.3.3 Simulation Runs

The simulation of XAUI IP is based on the Test Bench of the Example Design. For detailed information about Example Design, please refer to "2.4 Example Design".

For more details about the PDS simulation functions and third-party simulation tools, please consult the related help documents in the PDS installation path: "***Pango_Design_Suite_User_Guide***", "***Simulation_User_Guide***".

2.3.4 Synthesis and Placement/Routing

The specific usage of PDS synthesis tools and placement/routing tools can be found in the help documents within the PDS installation path.

Attention:

The .pds and .fdc files generated by the IP are for reference only, please modify constraints according to the actual device used and pin connections. Refer to "2.8 Descriptions and Considerations" for details.

2.3.5 Resources Utilization

Table 2-4 Typical Resource Utilization Values for XAUI IP Based on Applicable Devices

Device	Configuration Mode	Typical Resource Utilization Values			
		LUT	FF	HSSTLP	USCM
PG2L100H	MDIO Disable	1554	1713	1	2
	MDIO Enable	1621	1819	1	3
PG2L100HX	MDIO Disable	1555	1713	1	2
	MDIO Enable	1645	1819	1	3
PG2L50H	MDIO Disable	1557	1713	1	2
	MDIO Enable	1623	1819	1	3
PG2L25H	MDIO Disable	1554	1713	1	2
	MDIO Enable	1622	1820	1	3
PG2L200H	MDIO Disable	1554	1713	1	2
	MDIO Enable	1625	1820	1	3

2.4 Example Design

This section mainly introduces the Example Design scheme of XAUI IP. This scheme transmits data through the XAUI IP of two test boards, verifying the correctness of the received data based on link indications and cyclic redundancy check results.

2.4.1 Design Block Diagram

The system block diagram of the Example Design is as shown in Figure 2-7.

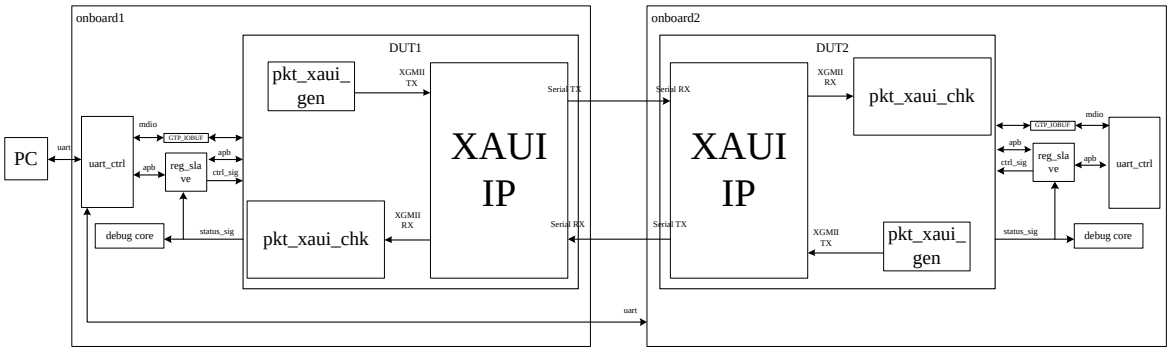

Figure 2-7 Example Design System Block Diagram

2.4.2 Descriptions of Ports

The interface descriptions of the Example Design are shown in Table 2-5.

Table 2-5 Example Design Interface List

Port	Pin constraints	I/O	Description
Clock and reset			
free_clk	G5	In	Input clock, which acts on initialization logic and configuration interface with a frequency of 100MHz, and also serves as the clock for APB.
ext_rst_n	AA23	In	Reset signal. 0: Reset; 1: Reset release.
hsst_cfg_rst_n	AA22	In	Dynamic configuration interface signal of HSSTLP. 0: Reset (all registers of HSSTLP revert to the initial values set by the Parameter after reset); 1: Reset release.
i_rstn	Y20	In	Logical reset of HSSTLP. 0: Reset; 1: Reset release.
MDIO Clock and Data			
mdc_xaui	E5	In	The MDIO's clock input when "MDIO Enable" is selected, 2MHz.
mdc_uart	D4	Out	The MDIO clock generated by the serial port module when "MDIO Enable" is selected.
mdio_xaui	G26	Inout	The MDIO data port when "MDIO Enable" is selected.
mdio_uart	G25	Inout	The MDIO data port of the serial port module when "MDIO Enable" is selected.
UART Module			
txd	C24	Out	UART sends data.
rxd	D24	In	UART receives data.
i_txd_b	B20	In	For debugging use only (default: 1).
o_rxd_b	B19	Out	For debugging use only.
uart_ctrl_sel	M24	In	It should be set to "0".

Port	Pin constraints	I/O	Description
User-side signal			
pin_cfg_en	T24	In	User-configured port. When MDIO is enabled, it operates under the mdc clock domain; When MDIO is disabled, it operates under the free_clk clock domain. 1: Configuration port valid (loop_back, test_pattern_enb, test_pattern_sel[1:0]); 0: Configuration port invalid, mode configuration is done using internal registers.
loop_back	P24	In	Loopback mode control. When MDIO is enabled, it operates under the mdc clock domain; When MDIO is disabled, it operates under the free_clk clock domain. 1: operate in the loopback mode; 0: operate in the normal mode.
test_pattern_enb	N24	In	Testpattern enable port. Testpattern testing can be performed after successfully establishing the link and completing relevant configurations. When MDIO is enabled, it operates under the mdc clock domain; When MDIO is disabled, it operates under the free_clk clock domain. 1: Operate in the testpattern mode; 0: operate in the normal mode.
test_pattern_sel[1:0]	1:F25 0:F24	In	Testpattern selection, Testpattern testing can be performed after successfully establishing the link and completing relevant configurations. When MDIO is enabled, it operates under the mdc clock domain; When MDIO is disabled, it operates under the free_clk clock domain. 11: Reserved; 10: Mix Frequency test pattern; 01: Low Frequency test pattern; 00: High Frequency test pattern.
HSSTLP-end Signal			
refclkp	CLK_0_P	In	Reference clock differential input positive end, HSSTLP dedicated pin, with a frequency of 156.25MHz.
refclkn	CLK_0_N	In	Reference clock differential input negative end, HSSTLP dedicated pin, with a frequency of 156.25MHz.
P_L0RXP	R0_P	In	Channel 0 differential input positive end, HSSTLP dedicated pin.
P_L0RXN	R0_N	In	Channel 0 differential input negative end, HSSTLP dedicated pin.
P_L1RXP	R1_P	In	Channel 1 differential input positive end, HSSTLP dedicated pin.
P_L1RXN	R1_N	In	Channel 1 differential input negative end, HSSTLP dedicated pin.
P_L2RXP	R2_P	In	Channel 2 differential input positive end, HSSTLP dedicated pin.
P_L2RXN	R2_N	In	Channel 2 differential input negative end, HSSTLP dedicated pin.

Port	Pin constraints	I/O	Description
P_L3RXP	R3_P	In	Channel 3 differential input positive end, HSSTLP dedicated pin.
P_L3RXN	R3_N	In	Channel 3 differential input negative end, HSSTLP dedicated pin.
P_L0TXP	T0_P	Out	Channel 0 differential output positive end, HSSTLP dedicated pin.
P_L0TXN	T0_N	Out	Channel 0 differential output negative end, HSSTLP dedicated pin.
P_L1TXP	T1_P	Out	Channel 1 differential output positive end, HSSTLP dedicated pin.
P_L1TXN	T1_N	Out	Channel 1 differential output negative end, HSSTLP dedicated pin.
P_L2TXP	T2_P	Out	Channel 2 differential output positive end, HSSTLP dedicated pin.
P_L2TXN	T2_N	Out	Channel 2 differential output negative end, HSSTLP dedicated pin.
P_L3TXP	T3_P	Out	Channel 3 differential output positive end, HSSTLP dedicated pin.
P_L3TXN	T3_N	Out	Channel 3 differential output negative end, HSSTLP dedicated pin.
Debug LED Indicator Signals			
led0	V24	Out	The Debug signal is used for easy observation, indicating whether the HSSTLP link is abnormal. 1: Light on, HSSTLP link abnormal; 0: Light off, HSSTLP link normal.
led1	AA25	Out	The Debug signal is used for easy observation, indicating whether the HSSTLP link is abnormal. 1: Light on, HSSTLP link normal; 0: Light off, HSSTLP link abnormal.
led2	W25	Out	The Debug signal is used for easy observation, indicating whether the HSSTLP link has received data. 1: Light on, HSSTLP link abnormal, at least one lane has lost data; 0: Light off, HSSTLP link normal.
led3	W24	Out	The Debug signal is used for easy observation, indicating whether the CDR in the HSSTLP link is abnormal. 1: Light on, HSSTLP link CDR normal; 0: Light off, HSSTLP link CDR abnormal.
led4	AA24	Out	Indicates whether the HSSTLP link sync is abnormal. 1: Light on, HSSTLP link sync normal; 0: Light off, HSSTLP link sync abnormal.
led5	AC24	Out	The Debug signal is used for easy observation, indicating whether the HSSTLP link deskew is abnormal. 1: Light on, HSSTLP link deskew normal; 0: Light off, HSSTLP link deskew abnormal.
led6	AB25	Out	The Debug signal is used for easy observation, indicating whether the HSSTLP link CTC is abnormal and FIFO is full or empty. 1: Light on, HSSTLP link CTC abnormal; 0: Light off, HSSTLP link CTC normal.
led7	AB24	Out	The Debug signal is used for easy observation, indicating whether a CRC error occurred for the XAUI IP reception. 1: Light on, a CRC error occurred for the XAUI IP reception; 0: Light off, a CRC error didn't occur for the XAUI IP reception.

Attention:

The MDIO clock and data are only effective when "MDIO Enable" (refer to "2.3.1.2 IP Parameter Configuration") is selected in the parameter configuration interface. Connect mdc_xaui to mdc_uart, and mdio_xaui to mdio_uart for usage;

The UART interface is for debugging use only. Please operate according to the relevant descriptions in this document. For more details, please refer to "2.4.3 Module Description";

In the Example Design, the clock frequency of free_clk is fixed at 100MHz.

2.4.3 Module Description

The modules in the Example Design are described as follows.

2.4.3.1 GTP_IOBUF Module

Converts mdi, mdo to bidirectional IO port MDIO.

2.4.3.2 Debug_core Module

Samples the status signals of HSSTLP, facilitating the observation of HSSTLP's status.

2.4.3.3 pkg_gen Module

Generates MAC frames whose Payload is of the Counter data type.

2.4.3.4 pkg_chk Module

Performs cyclic redundancy check on the received data.

2.4.3.5 uart_ctrl module

The serial port module, used during debugging with a fixed baud rate of 115200, receives UART data and outputs data in the data format required by the APB protocol or the MDIO protocol. For

read and write operations, the address width is 24 bits, and the data width is 32 bits.

2.4.3.5.1 Read and Write Operation Description

- Read operation format: "0x72" + "address";
- Write operation format: "0x77" + "address" + "data".

For the read and write operation examples, please refer to "2.8.4 Read and Write Operation Examples of the uart_ctrl Module".

2.4.3.5.2 Address description

The address when accessing registers through the uart_ctrl module is described in Table 2-6.

Table 2-6 uart_ctrl Module Address Description

Address bits	Description
23	Only for debugging, set to 0.
22	Set to 0 when accessing registers via the APB interface; set to 1 when accessing through the MDIO interface.
21	Valid when accessing registers via the APB interface. Set to 0 when accessing the reg_slave module; set to 1 when accessing IP.
20:19	Not used, set to 0.
18:0	The address of the IP register (refer to "2.6 Description of the IP Register") or the register address within reg_slave (refer to Table 2-7).

2.4.3.6 reg_slave Module

The register module used during debugging is for observing link status and generating some control signals. It can be accessed via the APB interface. The register address is described in Table 2-7.

Table 2-7 reg_slave Module Register Description

Register address	R/W	Description	Defaults
0x8000	W	Enable the pkg_gen module packet transmission control. 0x80: Start packet transmission (default); 0x00: Stop packet transmission.	0x80
others	-	For debugging use only.	-

Note: "-" indicates that this parameter does not exist.

Descirption:

When using the serial port module from this document's Example Design to access the reg_slave register for packet transmission control, to start transmission: write 0x7700800000000080 to the serial port; to stop transmission: write 0x7700800000000000 to the serial port.

2.4.3.7 XAUI IP Module

The XAUI IP module includes the XAUI Core and HSSTLP.

2.4.4 Directory Description

Taking the Example Design with MDIO disabled as an example, the project directory is shown in Figure 2-8.

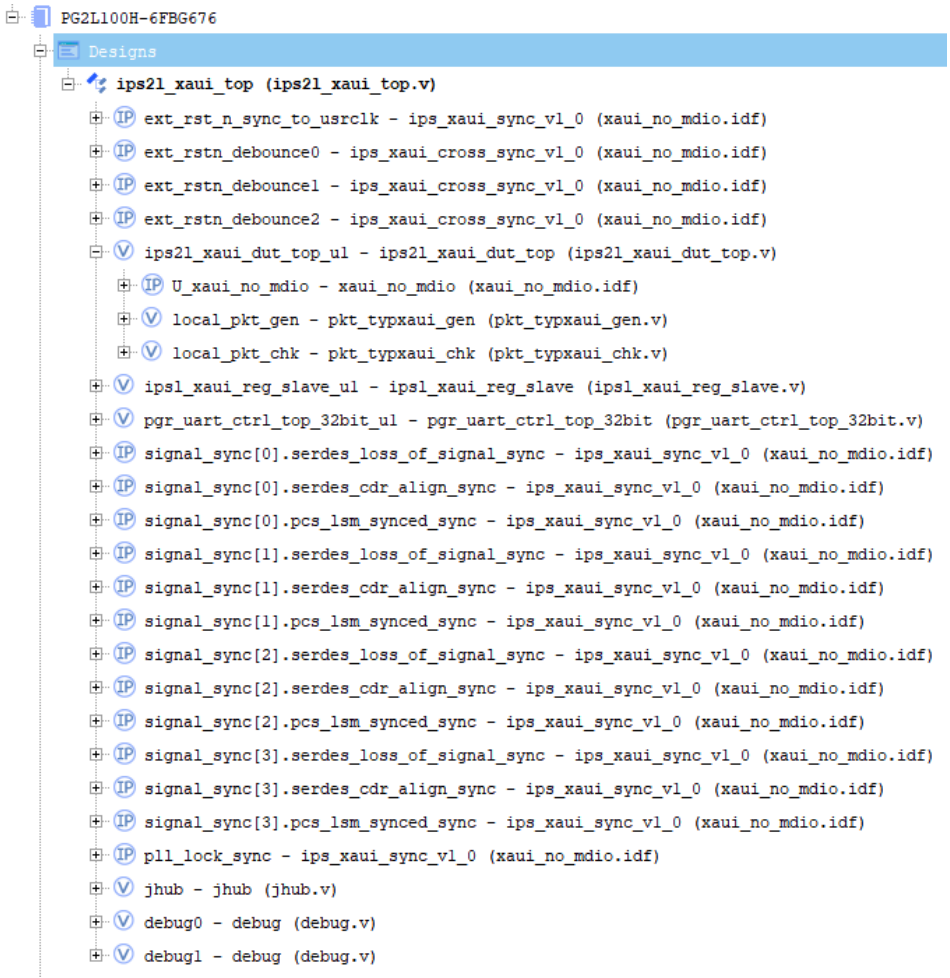

Figure 2-8 File Directory in MDIO Disable Mode

- ips2l_xaui_top: top-level file;
- ips2l_xaui_dut_top_u1: DUT layer, facilitates simulation testing;
- U_xaui_no_mdio: XAUI IP;
- local_pkt_gen: packet generator;
- local_pkt_chk: packet receiver;
- pgr_uart_ctrl_top_32bit_u1: serial port module;
- ipsl_xaui_reg_slave_u1: register module;
- The rest are debouncing, synchronisation, and debug modules.

2.4.5 Test Method

Perform the docking test using two test boards[2], judge test results according to cyclic redundancy check results, and monitor the link status through DebugCore and LEDs. For XAUI IP configuration methods, please refer to "2.4.6 Instance Configuration".

The Example Design includes a Debug_core module, which allows capturing transmitter and receiver data[3] using the Fabric Debugger tool within PDS software, as illustrated by screenshots in Figure 2-9 and Figure 2-10. Users may add or remove signals to be captured as needed; the Debug Core signal list is shown in Table 2-8.

Table 2-8 Debug Core Signal List

DEBUG CORE signal	**Project Signal Name**	**Meaning**
CORE:0 MyFAL0		
TriggerPort0[0]	ctc_afifo_err	1: The fifo of CTC is empty or full; 0: The fifo of CTC is not empty or full.
TriggerPort0[1]	deskew_align_status	1: channel bounding aligned; 0: channel bounding not aligned.
TriggerPort0[2]	s_pll_lock	1: PLL locked; 0: PLL not locked.
TriggerPort0[6:3]	s_pcs_lsm_synced[3:0]	Corresponding to 4 lanes, bit[0] represents lane0, and so on. 1: lane synchronisation normal; 0: lane synchronisation abnormal.

2 The model number of the test board is P04I100RD04_A2.

3 Capture the corresponding signals to form a waveform based on the assignment conditions in the Example Design.

DEBUG CORE signal	Project Signal Name	Meaning
TriggerPort0[10:7]	s_serdes_cdr_align[3:0]	Corresponding to 4 lanes, bit[0] represents lane0, and so on. 1: CDR locked; 0: CDR not locked.
TriggerPort0[14:11]	s_serdes_loss_of_signal[3:0]	Corresponding to 4 lanes, bit[0] represents lane0, and so on. 1: serdes signal lost; 0: serdes signal normal.
TriggerPort0[15]	hsst_up	1: link normal; 0: link abnormal.
TriggerPort0[16]	hsst_fault	1: link abnormal; 0: link normal.
TriggerPort0[255:17]	Not connected to a project signal	0.
CORE:1 MyFAL1		
TriggerPort0[0]	crc_ok	CRC passed, real-time signal.
TriggerPort0[1]	crc_err	CRC failed, real-time signal.
TriggerPort0[2]	rcving_data	Data indication. 1: Indicates data.
TriggerPort0[3]	crc_err_record	CRC record. 1: A CRC error occurred; 0: No CRC error occurred.
TriggerPort0[35:4]	rcving_cnt[31:0]	Received packet count.
TriggerPort0[67:36]	err_cnt[31:0]	CRC error packet count.
TriggerPort0[75:68]	xgmii_rxc[7:0]	Data reception control signal indication.
TriggerPort0[139:76]	xgmii_rxd[63:0]	Receive data.
TriggerPort0[147:140]	xgmii_txc[7:0]	Data transmission control signal indication.
TriggerPort0[211:148]	xgmii_txd[63:0]	Transmit data.
TriggerPort0[243:212]	tx_cnt[31:0]	Transmitted packet count.
TriggerPort0[255:244]	Not connected to a project signal	0.

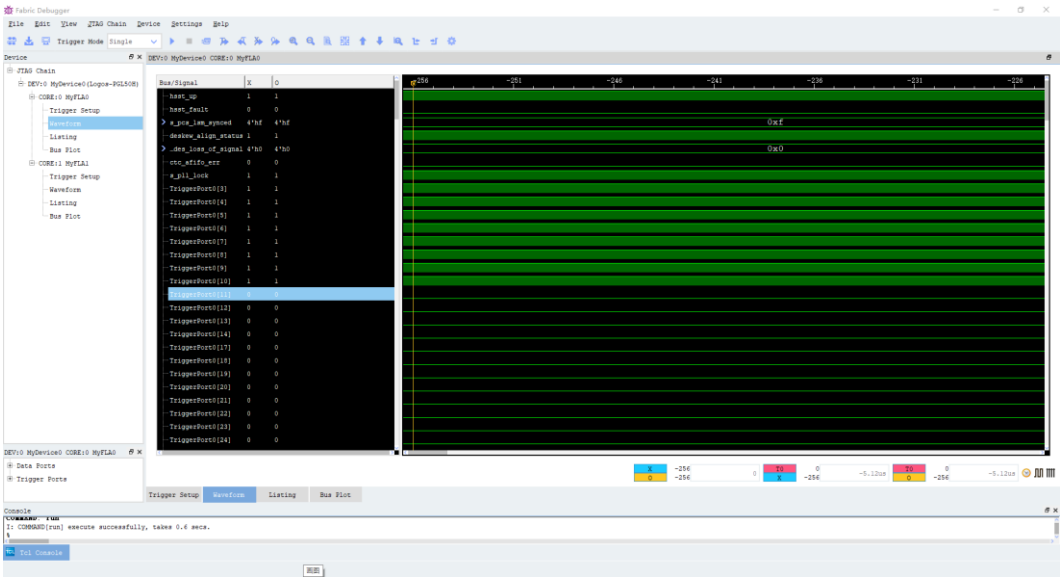

Figure 2-9 Debug Core0 Waveform Capture

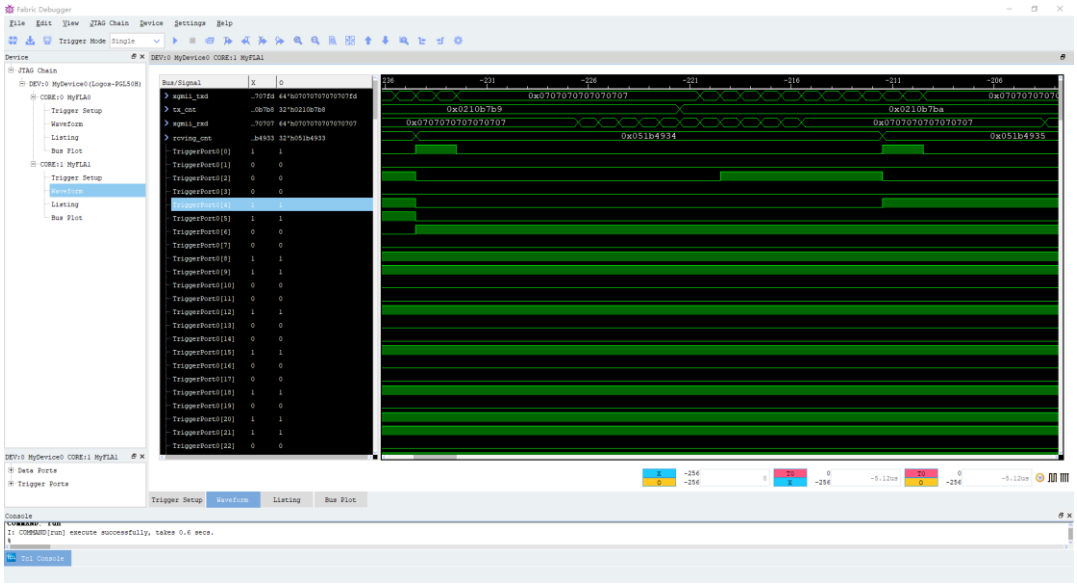

Figure 2-10 Debug Core1 Waveform Capture

2.4.6 Instance Configuration

- Users can perform register read and write access to the XAUI Core via APB. Configuration method: Do not check "MDIO Enable" in the IP parameter configuration interface. Please refer to "2.3.1.2 IP Parameter Configuration".
- Users can enable and disable loopback via the APB online configuration register. For the configuration method, please refer to "2.8.3.1 Loopback Mode".

- Other parameters follow the default configurations.

2.4.7 Instance Simulation

In the Windows system, after IP generation, double-click the *.bat file [4] under the <project_path>/sim/modelsim directory to run the simulation using ModelSim10.1a.

2.5 Descriptions of IP Interfaces

2.5.1 XAUI IP Interface Descriptions

Table 2-9 XAUI Interface Signal List

Port	I/O	Description
Clock and reset		
free_clk	In	Input clock, which acts on initialization logic and configuration interface with a frequency of 10–100MHz, and also serves as the clock for APB.
usrclk	Out	User clock, with a frequency of 156.25M, sourced from HSSTLP_XAUI.
ext_rst_n	In	Reset signal. 0: Reset; 1: Reset release.
txlane_rst	In	HSSTLP TX lane soft reset, for debugging use only, which operates under the free_clk clock domain. 0: Reset release; 1: Reset.
rxlane_rst	In	HSSTLP RX lane soft reset, for debugging use only, which operates under the free_clk clock domain. 0: Reset release; 1: Reset.
hsst_cfg_rst_n	In	Dynamic configuration interface signal of HSSTLP. 0: Reset (all registers of HSSTLP revert to the initial values set by the Parameter after reset); 1: Reset release.
wtchdg_clr	In	Watchdog counter clear signal, which operates under the free_clk clock domain. 1: Clear.
i_rstn	In	Logical reset of HSSTLP. 0: Reset; 1: Reset release.
o_tx_rstn	Out	When it is high, it indicates HSSTLP TX direction reset is complete and can be used for user base reset in the TX direction, active-low, asynchronous signal.

4 For the output files after IP generation, please refer to Table 2-3.

Port	I/O	Description
o_rx_rstn	Out	When it is high, it indicates HSSTLP RX direction reset is complete and can be used for user base reset in the RX direction, active-low, asynchronous signal.
o_cfg_rstn	Out	XAUI core reg reset output, asynchronous signal.
User-side signal		
xgmii_txd[63:0]	In	XGMII data transmission signal, from the user side, which operates within the usrclk clock domain.
xgmii_txc[7:0]	In	XGMII transmission control signal, from the user side, which operates within the usrclk clock domain.
xgmii_rxd[63:0]	Out	XGMII interface data reception character, to the user side, which operates within the usrclk clock domain.
xgmii_rxc[7:0]	Out	XGMII reception control signal, to the user side, which operates within the usrclk clock domain.
pin_cfg_en	In	User-configured port. When MDIO is enabled, it operates under the mdc clock domain; When MDIO is disabled, it operates under the free_clk clock domain. 1: Configuration port valid (loop_back, test_pattern_enb, test_pattern_sel[1:0]); 0: Configuration port invalid, mode configuration is done using internal registers.
loop_back	In	Loopback mode control. When MDIO is enabled, it operates under the mdc clock domain; When MDIO is disabled, it operates under the free_clk clock domain. 1: operate in the loopback mode; 0: operate in the normal mode.
test_pattern_enb	In	Testpattern enable port. When MDIO is enabled, it operates under the mdc clock domain; When MDIO is disabled, it operates under the free_clk clock domain. 1: Operate in the testpattern mode; 0: operate in the normal mode.
test_pattern_sel[1:0]	In	Testpattern selection. When MDIO is enabled, it operates under the mdc clock domain; When MDIO is disabled, it operates under the free_clk clock domain. 11: Reserved; 10: Mix Frequency test pattern; 01: Low Frequency test pattern; 00: High Frequency test pattern.
HSSTLP-end Signal		
P_REFCKP	In	Reference clock differential input positive end, HSSTLP dedicated pin, with a frequency of 156.25MHz.
P_REFCKN	In	Reference clock differential input negative end, HSSTLP dedicated pin, with a frequency of 156.25MHz.
P_L0RXP	In	Channel 0 differential input positive end, HSSTLP dedicated pin.
P_L0RXN	In	Channel 0 differential input negative end, HSSTLP dedicated pin.
P_L1RXP	In	Channel 1 differential input positive end, HSSTLP dedicated pin.
P_L1RXN	In	Channel 1 differential input negative end, HSSTLP dedicated pin.
P_L2RXP	In	Channel 2 differential input positive end, HSSTLP dedicated pin.
P_L2RXN	In	Channel 2 differential input negative end, HSSTLP dedicated pin.
P_L3RXP	In	Channel 3 differential input positive end, HSSTLP dedicated pin.
P_L3RXN	In	Channel 3 differential input negative end, HSSTLP dedicated pin.
P_L0TXP	Out	Channel 0 differential output positive end, HSSTLP dedicated pin.

Port	I/O	Description
P_L0TXN	Out	Channel 0 differential output negative end, HSSTLP dedicated pin.
P_L1TXP	Out	Channel 1 differential output positive end, HSSTLP dedicated pin.
P_L1TXN	Out	Channel 1 differential output negative end, HSSTLP dedicated pin.
P_L2TXP	Out	Channel 2 differential output positive end, HSSTLP dedicated pin.
P_L2TXN	Out	Channel 2 differential output negative end, HSSTLP dedicated pin.
P_L3TXP	Out	Channel 3 differential output positive end, HSSTLP dedicated pin.
P_L3TXN	Out	Channel 3 differential output negative end, HSSTLP dedicated pin.
Status Information		
hsst_fault	Out	Link status signal, active-high, which is asynchronous and indicates local line status is unstable.
hsst_up	Out	Link status signal, active-high, which is asynchronous and indicates HSSTLP is operating properly.
serdes_loss_of_signal[3:0]	Out	This signal is asynchronous and indicates whether the lane serial receiver signal is lost. 1: Signal lost; 0: Signal normal. bit[0] represents lane0, and so on.
serdes_cdr_align[3:0]	Out	Active-high. This signal is asynchronous and indicates whether the CDR of the lane is locked. 1: CDR locked; 0: CDR not locked. bit[0] represents lane0, and so on.
pll_lock	Out	This signal is asynchronous and indicates whether the PLL within HSSTLP is locked. 1: PLL locked; 0: PLL not locked. This signal is asynchronous.
pcs_lsm_synced[3:0]	Out	This signal is asynchronous and indicates whether the lane of HSSTLP has completed synchronization. 1: The lane has completed synchronization; 0: The lane has not completed synchronization. bit[0] represents lane0, and so on.
deskew_align_status	Out	This signal is asynchronous and indicates whether the 4 channels are aligned. 1: 4 channels aligned; 0: 4 channels not aligned.
ctc_afifo_err	Out	This signal is asynchronous and indicates whether the CTC AFIFO of HSSTLP is empty or full. 1: The AFIFO of CTC is empty/full; 0: The AFIFO of CTC is not empty/full.
APB Bus		
p_cfg_enable	In	APB interface access enable signal, which operates within the free_clk clock domain. 1: Enabled; 0: Disabled.
p_cfg_write	In	APB interface read/write select signal, which operates within the free_clk clock domain. 1: Write operation; 0: Read operation.
p_cfg_addr[18:0]	In	APB interface read/write address signal, which operates within the free_clk clock domain.

Port	I/O	Description
p_cfg_wdata[31:0]	In	APB interface write data signal, which operates within the free_clk clock domain.
p_cfg_rdata[31:0]	Out	APB interface read data signal, which operates within the free_clk clock domain.
p_cfg_ready	Out	APB interface read/write ready output signal, which operates within the free_clk clock domain. 1: Data valid; 0: Data invalid.
p_cfg_sel	In	APB interface chip select signal, which operates within the free_clk clock domain. Once selected, APB data transfer can be performed. 1: Selected; 0: Cleared.
MDIO Bus[5]		
mdc	In	MDIO interface clock signal, with a frequency of 2MHz.
mdi	In	MDIO input data.
phy_addr[4:0]	In	PHY address configuration bus.
mdo	Out	MDIO output data.
mdo_en	Out	MDIO output data enable signal.
Loopback Enable		
i_p_pcs_nearend_loop_0	In	Corresponds to the P_PCS_NEAREND_LOOP_0 interface and controls lane0. 1: Enabled; 0: Disabled.
i_p_pcs_farend_loop_0	In	Corresponds to the P_PCS_FAREND_LOOP_0 interface and controls lane0. 1: Enabled; 0: Disabled.
i_p_pma_nearend_ploop_0	In	Corresponds to the P_PMA_NEAREND_PLOOP_0 interface and controls lane0. 1: Enabled; 0: Disabled.
i_p_pma_nearend_sloop_0	In	Corresponds to the P_PMA_NEAREND_SLOOP_0 interface and controls lane0. 1: Enabled; 0: Disabled.
i_p_pcs_nearend_loop_1	In	Corresponds to the P_PCS_NEAREND_LOOP_1 interface and controls lane1. 1: Enabled; 0: Disabled.
i_p_pcs_farend_loop_1	In	Corresponds to the P_PCS_FAREND_LOOP_1 interface and controls lane1. 1: Enabled; 0: Disabled.
i_p_pma_nearend_ploop_1	In	Corresponds to the P_PMA_NEAREND_PLOOP_1 interface and controls lane1. 1: Enabled; 0: Disabled.

5 The MDIO interface is only displayed when "MDIO Enable" is selected in the parameter configuration interface (refer to "2.3.1.2 IP Parameter Configuration").

Port	I/O	Description
i_p_pma_nearend_sloop_1	In	Corresponds to the P_PMA_NEAREND_SLOOP_1 interface and controls lane1. 1: Enabled; 0: Disabled.
i_p_pcs_nearend_loop_2	In	Corresponds to the P_PCS_NEAREND_LOOP_2 interface and controls lane2. 1: Enabled; 0: Disabled.
i_p_pcs_farend_loop_2	In	Corresponds to the P_PCS_FAREND_LOOP_2 interface and controls lane2. 1: Enabled; 0: Disabled.
i_p_pma_nearend_ploop_2	In	Corresponds to the P_PMA_NEAREND_PLOOP_2 interface and controls lane2. 1: Enabled; 0: Disabled.
i_p_pma_nearend_sloop_2	In	Corresponds to the P_PMA_NEAREND_SLOOP_2 interface and controls lane2. 1: Enabled; 0: Disabled.
i_p_pcs_nearend_loop_3	In	Corresponds to the P_PCS_NEAREND_LOOP_3 interface and controls lane3, 1: Enabled; 0: Disabled.
i_p_pcs_farend_loop_3	In	Corresponds to the P_PCS_FAREND_LOOP_3 interface and controls lane3. 1: Enabled; 0: Disabled.
i_p_pma_nearend_ploop_3	In	Corresponds to the P_PMA_NEAREND_PLOOP_3 interface and controls lane3. 1: Enabled; 0: Disabled.
i_p_pma_nearend_sloop_3	In	Corresponds to the P_PMA_NEAREND_SLOOP_3 interface and controls lane3. 1: Enabled; 0: Disabled.
i_p_rx_polarity_invert_0	In	Corresponds to the P_RX_POLARITY_INVERT_0 interface and controls lane0. 1: Polarity inversed; 0: Polarity normal.
i_p_rx_polarity_invert_1	In	Corresponds to the P_RX_POLARITY_INVERT_0 interface and controls lane1. 1: Polarity inversed; 0: Polarity normal.
i_p_rx_polarity_invert_2	In	Corresponds to the P_RX_POLARITY_INVERT_0 interface and controls lane2. 1: Polarity inversed; 0: Polarity normal.
i_p_rx_polarity_invert_3	In	Corresponds to the P_RX_POLARITY_INVERT_0 interface and controls lane3. 1: Polarity inversed; 0: Polarity normal.

Port	I/O	Description
Debug Signals[6]		
rxd_no_k_l[3:0]	Out	No |K| indicator within low 32bits; each bit corresponds to 8bits, 1 indicates the current 32bits contains |T| and the corresponding 8bits is not |K| or has a polarity error; this signal operates within the free_clk clock domain.
rxd_no_k_h[3:0]	Out	No |K| indicator within high 32bits; each bit corresponds to 8bits, 1 indicates the current 32bits contains |T| and the corresponding 8bits is not |K| or has a polarity error; this signal operates within the free_clk clock domain.
pcs_eop_l[3:0]	Out	End of packet indicator within low 32 bit; 1 indicates the current is ||T||; this signal operates within the free_clk clock domain.
pcs_eop_h[3:0]	Out	End of packet indicator within high 32bit; 1 indicates the current is ||T||; this signal operates within the free_clk clock domain.
rxd_is_ak_l[3:0]	Out	An error occurs in the lower 32bit where ||T|| is not followed by |A| or |K|, with 1 indicating an error; this signal operates under the free_clk clock domain.
rxd_is_ak_h[3:0]	Out	An error occurs in the upper 32bit where ||T|| is not followed by |A| or |K|, with 1 indicating an error; this signal operates under the free_clk clock domain.
ctc0_status[2:0][7]	Out	The status of Lane0 CTC AFIFO.
ctc1_status[2:0][7]	Out	The status of Lane1 CTC AFIFO.
ctc2_status[2:0][7]	Out	The status of Lane2 CTC AFIFO.
ctc3_status[2:0][7]	Out	The status of Lane3 CTC AFIFO.
pcs_txd[63:0]	Out	XAUI TX data signal, which operates within the usrclk clock domain.
pcs_txk[7:0]	Out	XAUI TX control signal transmission indicator, which operates within the usrclk clock domain.
pcs_tx_dispsel[7:0]	Out	XAUI TX direction data polarity mode selection signal; the low bit controls the lower 8 bits, and the high bit controls the upper 8 bits; this signal operates within the usrclk clock domain. {pcs_tx_dispctrl[0], pcs_tx_dispsel[0]} are a set of signals controlling the lower 8bits, other bits are similar. 2'b00: Data transmission normal; 2'b01: Select the first I1/I2 at the end of frame according to the IEEE 802.3 1000BASE-X specification, with automatic replacement of I2 by I1 under the right conditions; 2'b10: Force the 8b10b encoding polarity to be negative; 2'b11: Force the 8b10b encoding polarity to be positive.
pcs_tx_dispctrl[7:0]	Out	
pcs_rxd_dly[63:0]	Out	RX direction data reception character, which operates within the usrclk clock domain.
pcs_rxk_dly[7:0]	Out	RX direction control signal indicator, which operates within the usrclk clock domain.

6 For the |K|, |T|, ||T||, |A| in the Debug signal descriptions, please refer to the "***IEEE 802.3-2012 Specification***".

7 A status indicator signal output by the HSSTLP. Please refer to the "***UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide***".

Port	I/O	Description
pcs_rdispdec_er_dly[7:0]	Out	This signal indicates whether a polarity error or invalid character occurred in the RX direction; 1 indicates a polarity error or invalid character occurred; this signal operates within the usrclk clock domain.
s_xaui_core_rx_rst_n	Out	Synchronized to xaui core rx reset of usrclk.
s_xaui_core_tx_rst_n	Out	Synchronized to xaui core tx reset of usrclk.

2.5.2 XAUI IP Interface Timing Description

XAUI IP uses a 64-bit width user data interface that maps to the 32-bit XGMII as specified in the IEEE 802.3-2012 specification, as shown in Figure 2-11, which lists two mapping cases A and B.

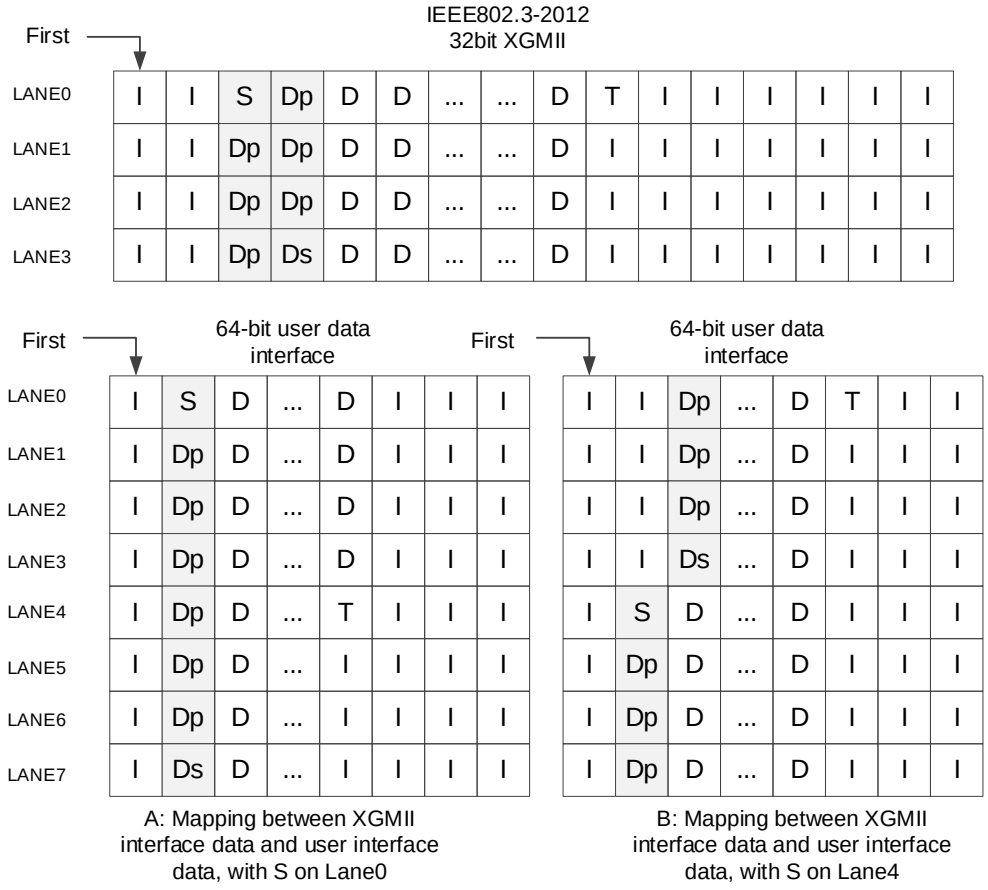

Figure 2-11 User Data Interface Mapping Diagram

The rules for encoding from the XGMII interface to the PCS interface in the XAUI IP are shown in Table 2-10 and Table 2-11.

Table 2-10 XGMII Character to PCS Code-Groups Mapping

XGMII TXC	XGMII TXD	PCS Code-Groups 8-bit value	Description
0	0x00 through 0xFF	0xXX	Normal data transmission.
1	0x07	0xBC or 0x1C or 0x7C	Idle character in the Idle sequence.
1	0x07	0xBC	Idle character in Terminate.
1	0xFB	0xFB	Start character.
1	0xFD	0xFD	Termination character.
1	0xFE	0xFE	Error character.
1	0x9C	0x9C	Sequency.

Table 2-11 PCS Code-Groups to XGMII Character Mapping

XGMII RXC	XGMII RXD	PCS Code-Groups 8-bit value	Description
0	0x00 through 0xFF	0xXX	Normal data transmission.
1	0x07	0xBC	/K/ (Sync), used for Word Alignment.
1	0x07	0x7C	/A/ (Align), used for Channel Bonding.
1	0x07	0x1C	/R/ (Skip), used for CTC.
1	0xFB	0xFB	Start character.
1	0xFD	0xFD	Termination character.
1	0xFE	0xFE	Error character.
1	0x9C	0x9C	Sequency.

2.5.2.1 Data Transmission Timing of the User

2.5.2.1.1 Normal data

When the user transmits normal data, /S/ must be on Lane0 or Lane4, /T/ can be on any channel, followed by channels filled with XGMII Idle. For a detailed description, please refer to "***IEEE 802.3-2012 specification (section 46.3.1)***". Timing diagram examples when transmitting normal data are shown in Figure 2-12 and Figure 2-13.

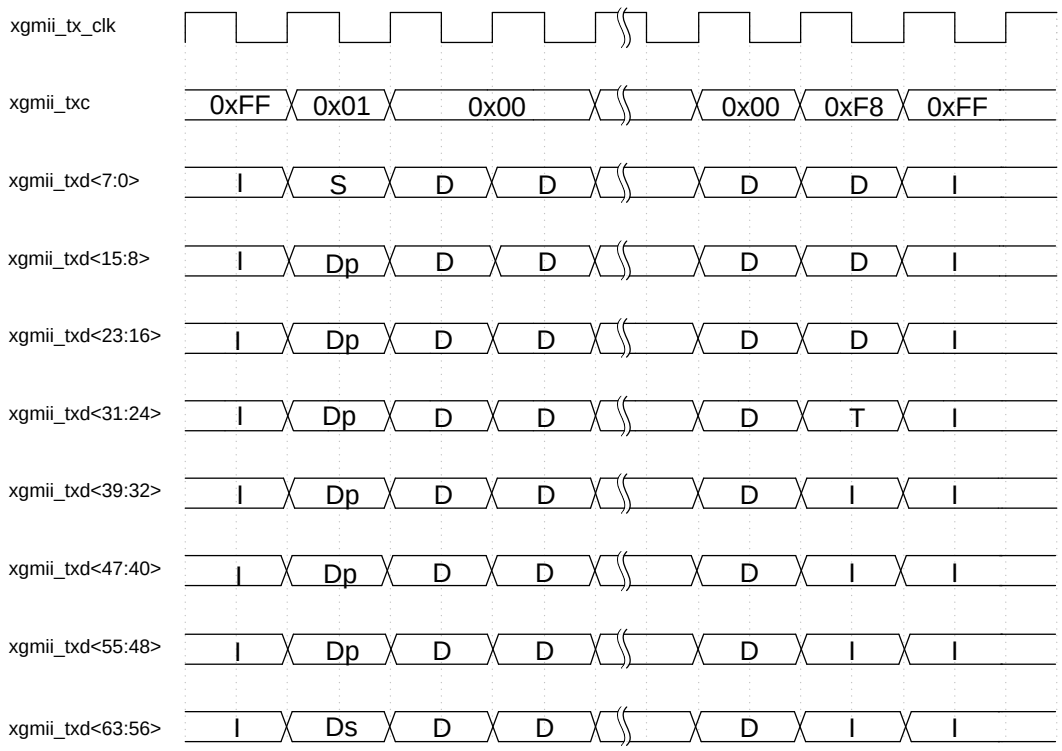

Figure 2-12 Example of User Transmitting Normal Data (/S/ on Lane0)

Descirption:

S: Start, indicating the start character.

Dp: Data Preamble, indicating the data in the form of a preamble.

Ds: SFD (Start Frame Delimiter).

D: Data, indicating a piece of data.

T: Terminate, indicating the termination character.

I: Idle, indicating the Idle character.

Figure 2-13 Example of User Sending Normal Data (/S/ on Lane4)

2.5.2.1.2 Error Data

When the user transmits error data, the error character /E/ can be on any Lane. The timing diagram example is shown in Figure 2-14, with /E/ on Lane1.

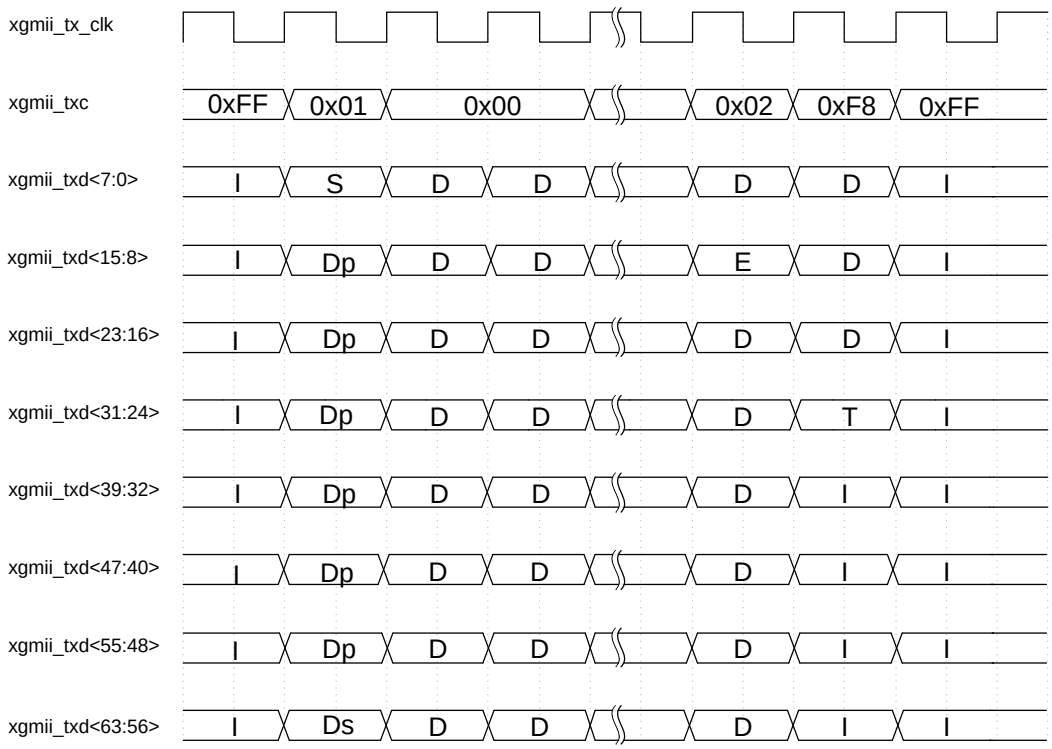

Figure 2-14 Example of User Sending Error Code (/E/ on Lane1)

Descirption:

E: Error, indicating the error character.

2.5.2.2 Data Reception Timing of the User

2.5.2.2.1 Normal data

The timing of receiving normal data is similar to that of transmitting normal data, starting with the Start Character (S), /S/ on Lane0 or Lane4, and ending with /T/, where /T/ can be on any Lane. For a detailed description, please refer to "***IEEE 802.3-2012 specification (section 46.3.2)***". The timing diagram example when receiving normal data is shown in Figure 2-15.

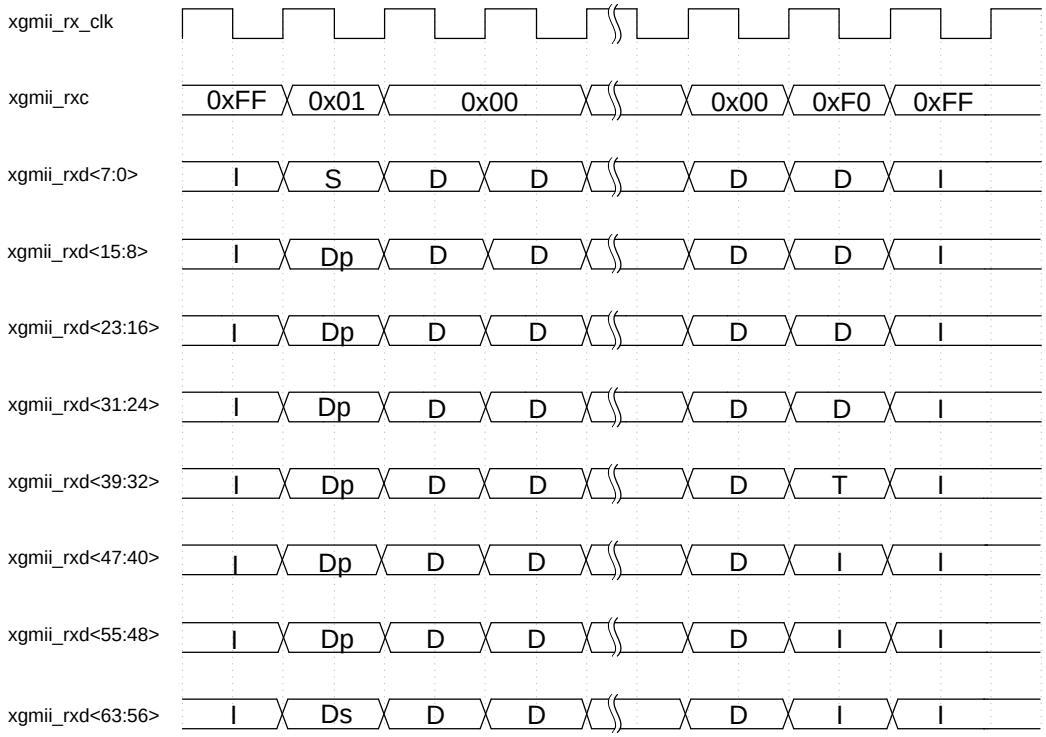

Figure 2-15 Example of User Receiving Normal Data (/S/ on Lane0)

2.5.2.2.2 Error Data

When receiving error data, the error character /E/ can be on any Lane. Figure 2-16 shows a timing example for receiving error data, with /E/ on Lane 1.

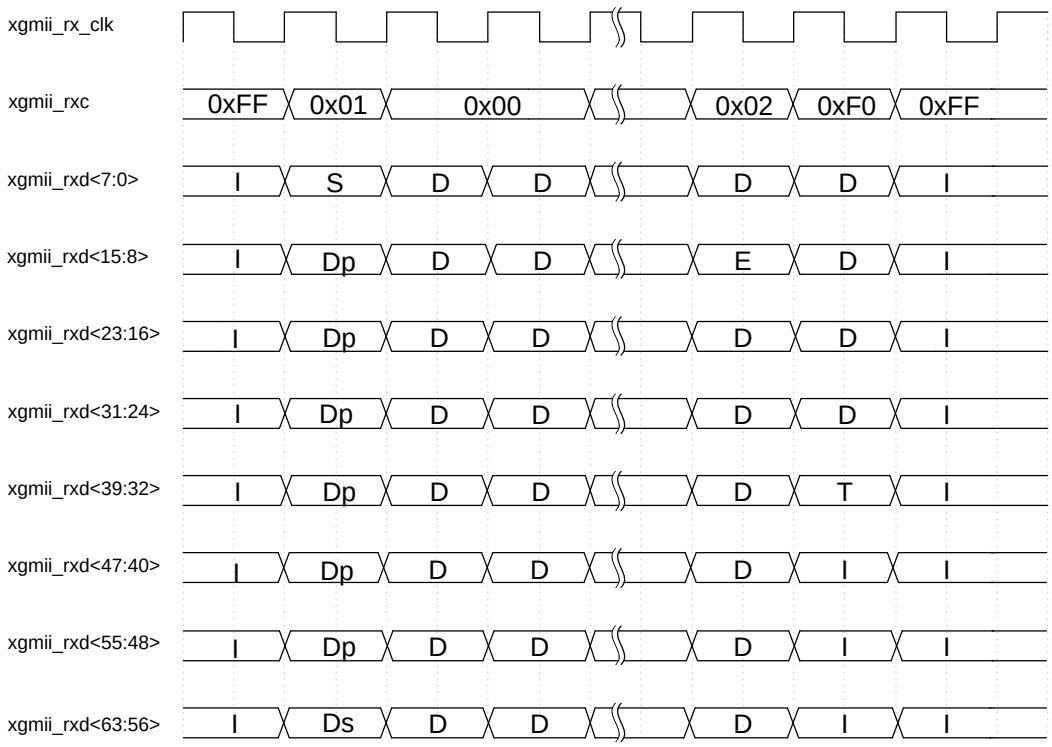

Figure 2-16 Example of User Receiving Error Data (/E/ on Lane1)

2.5.3 Register Management Interface

2.5.3.1 APB Operating Timing

2.5.3.1.1 APB Read Timing

To perform a read operation through APB, first pull high p_cfg_sel to select the APB interface, simultaneously pull high p_cfg_enable and pull down p_cfg_write. Then enter the valid address p_cfg_addr to request data reading. After 3 Cycles of maintaining the above signal, p_cfg_ready is pulled high, and the valid data is read out, then p_cfg_enable is pulled low, completing a read operation.

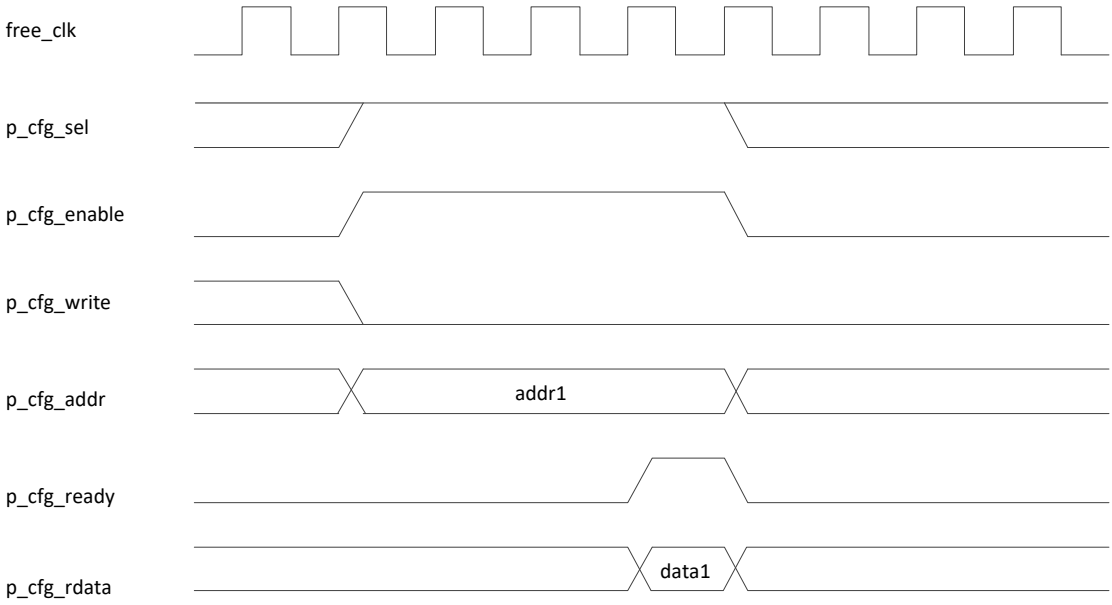

Figure 2-17 Basic APB Read Timing

2.5.3.1.2 APB Write Timing

To perform a write operation through APB, first pull high p_cfg_sel to select the APB interface, simultaneously pull high p_cfg_enable and pull high p_cfg_write. Then enter the valid address p_cfg_addr to request data writing. After 1 Cycle of maintaining the above signal, p_cfg_ready is pulled high, and the valid data is written, then p_cfg_enable is pulled low, completing a write operation.

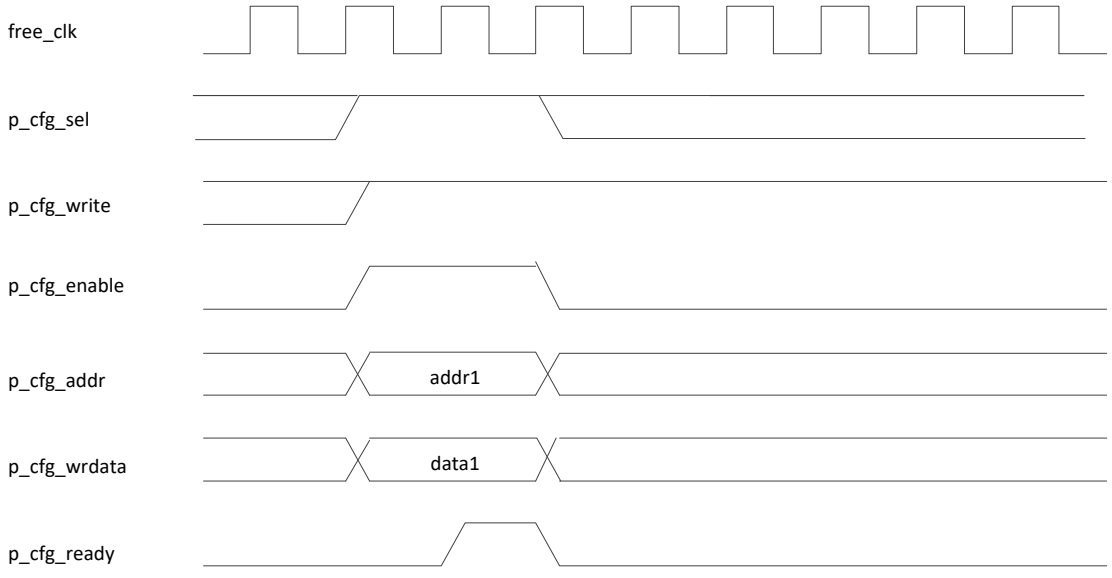

Figure 2-18 Basic APB Write Timing

2.5.3.2 MDIO Operating Timing

2.5.3.2.1 MDIO Write Timing

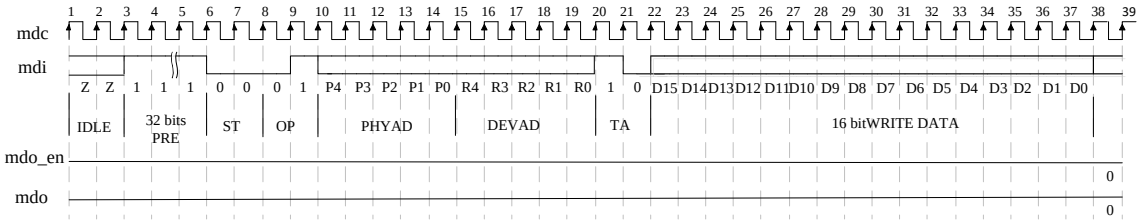

Figure 2-19 MDIO Write Timing

2.5.3.2.2 MDIO Write Timing

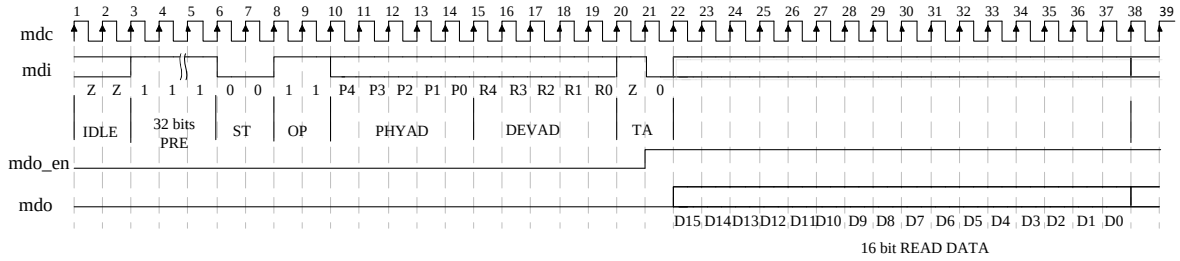

Figure 2-20 MDIO Write Timing

2.5.3.2.3 MDIO Address Setting Timing

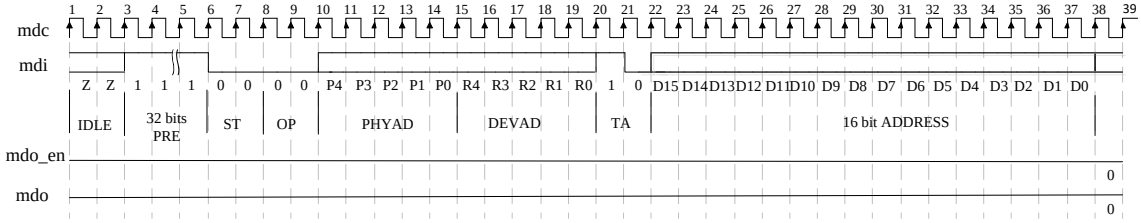

Figure 2-21 MDIO Address Setting Timing

2.5.3.2.4 MDIO Post-read Address Auto-increment Timing

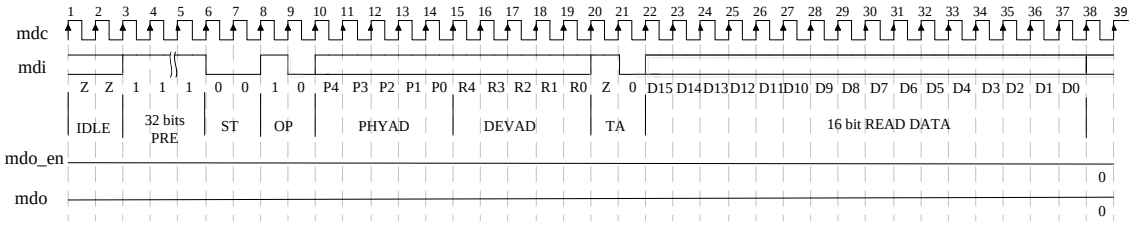

Figure 2-22 MDIO Post-read Address Auto-increment Timing

2.6 Description of the IP Register

2.6.1 XAUI CORE Register Description

XAUI Core registers can be selected and configured via the MDIO or APB interface. The register address mapping will change with the management interface. The definition of the registers is as follows, and a reset will restore all register values back to their default values.

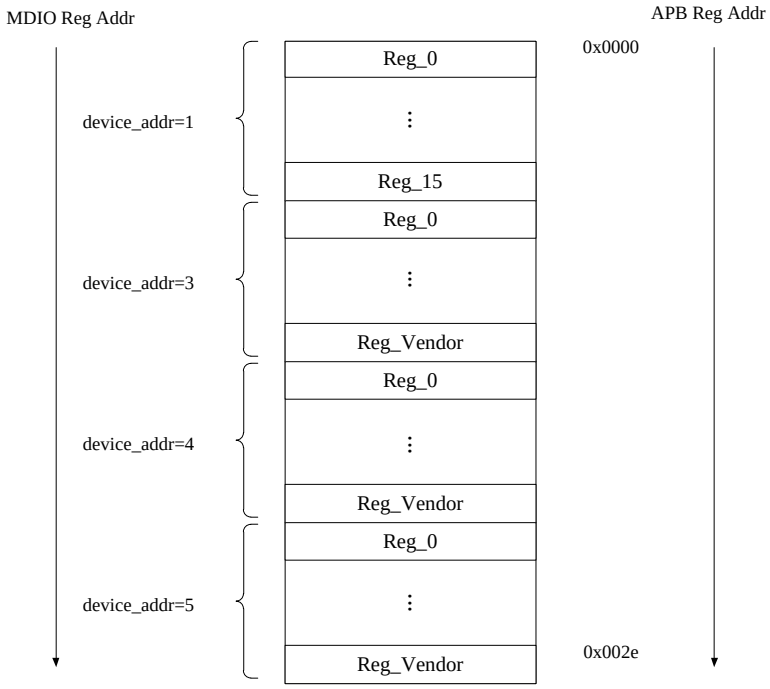

Figure 2-23 XAUI Core Register Address Allocation

Table 2-12 XAUI Core Register Address Allocation

Interface Type	Address Allocated
APB interface	The operating range of register addresses is 0x0000–0x002e.
MDIO interface	Consistent with IEEE 802.3-2012 clause 45.

2.6.1.1 MDIO Management Interface

When MDIO serves as a management interface, the corresponding registers are identified by device_addr, as shown below.

2.6.1.1.1 10GBASE-X

When XAUI operates in the 10GBASE-X PCS/PMA mode, i.e., when device_addr equals 1 and 3, the detailed register list is shown in Table 2-13.

Table 2-13 List of 10GBASE-X PCS/PMA Registers

Address	Register
1.0	Physical Medium Attachment/Physical Medium Dependent (PMA/PMD) Control 1
1.1	PMA/PMD Status 1
1.2,1.3	PMA/PMD Device Identifier
1.4	PMA/PMD Speed Ability
1.5, 1.6	PMA/PMD Devices in Package
1.7	10G PMA/PMD Control 2
1.8	10G PMA/PMD Status 2
1.9	Reserved
1.10	10G PMD Receive Signal OK
1.11 TO 1.13	Reserved
1.14, 1.15	PMA/PMD Package Identifier
1.16 to 1.65535	Reserved
3.0	PCS Control 1
3.1	PCS Status 1
3.2, 3.3	PCS Device Identifier
3.4	PCS Speed Ability
3.5, 3.6	PCS Devices in Package
3.7	10G PCS Control 2
3.8	10G PCS Status 2
3.9 to 3.13	Reserved

Address	Register
3.14, 3.15	Package Identifier
3.16 to 3.23	Reserved
3.24	10GBASE-X PCS Status
3.25	10GBASE-X Test Control
3.26 to 3.32767	Reserved
3.32768	Vendor Specific
3.32769 to 3.65535	Reserved

Table 2-14 PMA/PMD Control 1 Registers

Bit	Register	Description	Property	Defaults
1.0.15:14	Reserved	Reserved field.	RO	0
1.0.13	Speed Selection	1.0.6 1.0.13 11 = bits 5:2 select speed 10 = 1000 Mb/s 01 = 100 Mb/s 00 = 10 Mb/s	RO	1
1.0.12:11	Reserved	Reserved field.	RO	0
1.0.11	Power down(NA)	Power down by configuring the HSSTLP register via APB, and this register does not operate.	RW	0
1.0.10:7	Reserved	Reserved field.	RO	0
1.0.6	Speed Selection	1.0.6 1.0.13 11 = bits 5:2 select speed 10 = 1000 Mb/s 01 = 100 Mb/s 00 = 10 Mb/s	RO	1
1.0.5:2	Speed Selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved 0 0 1 1 = 100Gb/s 0 0 1 0 = 40Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10Gb/s	RO	0
1.0.1:0	Reserved	Reserved field.	RO	0
1.0.0	Loopback	1 = Enable loopback mode 0 = Disable loopback mode It has the same function as port loop_back.	RW	0

Table 2-15 PMA/PMD Status 1 Registers

Bit	Register	Description	Property	Defaults
1.1.15:8	Reserved	Reserved Field	RO	0
1.1.7	Local Fault	1 = Fault condition detected 0 = Fault condition not detected Maintain the fixed value 0.	RO	0

Bit	Register	Description	Property	Defaults
1.1.6:3	Reserved	Reserved field.	RO	0
1.1.2	Receive Link Status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down Maintain the fixed value 1.	RO	1
1.1.1	Power Down Ability	1 = PMA/PMD supports low-power mode 0 = PMA/PMD does not support low-power mode Maintain the fixed value 1.	RO	1
1.1.0	Reserved	Reserved field.	RO	0

Table 2-16 PMA/PMD Identifier Registers

Bit	Register	Description	Property	Defaults
1.2.15:0	PMA/PMD Identifier	Organizationally Unique Identifier[3:18]	RO	0
1.3.15:10	PMA/PMD Identifier	Organizationally Unique Identifier[19:24]	RO	0
1.3.9:4	PMA/PMD Identifier	Manufacturer's Model Number	RO	0
1.3.3:0	PMA/PMD Identifier	Revision Number	RO	0

Table 2-17 PMA/PMD Speed Ability Registers

Bit	Register	Description	Property	Defaults
1.4.15:1	Reserved	1 = PMA/PMD is capable of operating as 2BASE-TL 0 = PMA/PMD is not capable of operating as 2BASE-TL Maintain the fixed value 0.	RO	0
1.4.0	10G Capable	1 = PMA/PMD is capable of operating at 10 Gb/s 0 = PMA/PMD is not capable of operating at 10 Gb/s Maintain the fixed value 1.	RO	1

Table 2-18 PMA/PMD Devices in Package Registers

Bit	Register	Description	Property	Defaults
1.5.15:6	Reserved	Reserved field.	RO	0
1.5.5	DTE Extender Sublayer (XS) Present	1 = DTE XS present in package 0 = DTE XS not present in package	RO	0
1.5.4	PHY XS Present	1 = PHY XS present in package 0 = PHY XS not present in package	RO	0
1.5.3	PCS Present	1 = PCS present in package 0 = PCS not present in package	RO	1
1.5.2	WIS Present	1 = WIS present in package 0 = WIS not present in package	RO	0
1.5.1	PMA/PMD Present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO	1
1.5.0	Clause 22 Device Present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO	0

Bit	Register	Description	Property	Defaults
1.6.15	Vendor- specific Device 2 Present	1 = Vendor-specific device 2 present in package 0 = Vendor-specific device 2 not present in package	RO	0
1.6.14	Vendor-specific Device 1 Present	1 = Vendor-specific device 1 present in package 0 = Vendor-specific device 1 not present in package	RO	0
1.6.13:0	Reserved	Reserved field.	RO	0

Table 2-19 10G PMA/PMD Control 2 Registers

Bit	Register	Description	Property	Defaults
1.7.15:3	Reserved	Reserved field.	RO	0
1.7.2:0	PMA/PMD Type Selection	The block always returns 100 for these bits and ignores writes. 10GBASE-X PMA/PMD.	RO	100

Table 2-20 10G PMA/PMD Status 2 Registers

Bit	Register	Description	Property	Defaults
1.8.15:14	Device Present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO	10
1.8.13	Transmit Local Fault Ability	1 = PMA/PMD has the ability to detect a fault condition on the transmit path 0 = PMA/PMD does not have the ability to detect a fault condition on the transmit path	RO	0
1.8.12	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO	0
1.8.11	Transmit Fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO	0
1.8.10	Receive Fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO	0
1.8.9	Reserved		RO	0
1.8.8	PMD transmit disable ability	1 = PMD has the ability to disable the transmit path 0 = PMD does not have the ability to disable the transmit path	RO	0
1.8.7	10GBASE-SR Ability	1 = PMA/PMD is able to perform 10GBASE-SR 0 = PMA/PMD is not able to perform 10GBASE-SR	RO	0
1.8.6	10GBASE-LR ability	1 = PMA/PMD is able to perform 10GBASE-LR 0 = PMA/PMD is not able to perform 10GBASE-LR	RO	0
1.8.5	10GBASE-ER ability	1 = PMA/PMD is able to perform 10GBASE-ER 0 = PMA/PMD is not able to perform 10GBASE-ER	RO	0

Bit	Register	Description	Property	Defaults
1.8.4	10GBASE-LX4 ability	1 = PMA/PMD is able to perform 10GBASE-LX4 0 = PMA/PMD is not able to perform 10GBASE-LX4	RO	1
1.8.3	10GBASE-SW ability	1 = PMA/PMD is able to perform 10GBASE-SW 0 = PMA/PMD is not able to perform 10GBASE-SW	RO	0
1.8.2	10GBASE-LW ability	1 = PMA/PMD is able to perform 10GBASE-LW 0 = PMA/PMD is not able to perform 10GBASE-LW	RO	0
1.8.1	10GBASE-EW Ability	1 = PMA/PMD is able to perform 10GBASE-EW 0 = PMA/PMD is not able to perform 10GBASE-EW	RO	0
1.8.0	PMA Loopback Ability	1 = PMA has the ability to perform a local loopback function 0 = PMA does not have the ability to perform a local loopback function	RO	1

Table 2-21 10GPMD Signal Receive OK Registers

Bit	Register	Description	Property	Defaults
1.10.15:5	Reserved	Reserved field.	RO	0
1.10.4	PMD receive signal detect 3	1 = Signal detected on receive lane 3 0 = Signal not detected on receive lane 3 It has the same function as port serdes_loss_of_signal[3].	RO	0
1.10.3	PMD receive signal detect 2	1 = Signal detected on receive lane 2 0 = Signal not detected on receive lane 2 It has the same function as port serdes_loss_of_signal[2].	RO	0
1.10.2	PMD receive signal detect 1	1 = Signal detected on receive lane 1 0 = Signal not detected on receive lane 1 It has the same function as port serdes_loss_of_signal[1].	RO	0
1.10.1	PMD receive signal detect 0	1 = Signal detected on receive lane 0 0 = Signal not detected on receive lane 0 It has the same function as port serdes_loss_of_signal[0].	RO	0
1.10.0	Global PMD receive signal detect	1 = Signal detected on receive 0 = Signal not detected on receive	RO	0

Table 2-22 PMA/PMD Package Identifier Registers

Bit	Register	Description	Property	Defaults
1.15.15:0	PMA/PMD Package Identifier	The block always returns 0 for these bits.	RO	0
1.14.15:0	PMA/PMD Package Identifier	The block always returns 0 for these bits.	RO	0

Table 2-23 PCS Control 1 Registers

Bit	Register	Description	Property	Defaults
3.0.15:14	Reserved	Reserved field.	RO	0
3.0.13	Speed Selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	RO	1
3.0.12:7	Reserved	Reserved field.	RO	0
3.0.6	Speed Selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	RO	1
3.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved 0 1 1 x = Reserved 0 1 0 1 = Reserved 0 1 0 0 = 100Gb/s 0 0 1 1 = 40Gb/s 0 0 1 0 = 10/1Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10Gb/s	RO	0
3.0.1:0	Reserved	Reserved field.	RO	0

Table 2-24 PCS Status 1 Registers

Bit	Register	Description	Property	Defaults
3.1.15:8	Reserved	Reserved field.	RO	0
3.1.7	Local Fault	1 = Fault condition detected 0 = No fault condition detected This bit is set to 1 whenever either of the bits 3.8.11, 3.8.10 are set to 1.	RO	0
3.1.6:3	Reserved	Reserved field.	RO	0
3.1.2	PCS Receive Link Status	1 = The PCS receive link is up 0 = The PCS receive link is down Latch the low level, and restore to the current link status after a read operation.	RO LL	0
3.1.1	Power Down Ability	1 = PCS supports low-power mode 0 = PCS does not support low-power mode	RO	1
3.1.0	Reserved	Reserved field.	RO	0

Note: "LL" indicates latching the low level.

Table 2-25 PCS Device Identifier Registers

Bit	Register	Description	Property	Defaults
3.2.15:0	PCS Identifier	The block always returns 0 for these bits.	RO	0
3.3.15:0	PCS Identifier	The block always returns 0 for these bits.	RO	0

Table 2-26 PCS Devices in Package Registers

Bit	Register	Description	Property	Defaults
3.2.15:0	PCS Identifier	The block always returns 0 for these bits.	RO	0
3.3.15:0	PCS Identifier	The block always returns 0 for these bits.	RO	0

Table 2-27 PCS Speed Ability Registers

Bit	Register	Description	Property	Defaults
3.4.15:1	Reserved	Reserved field.	RO	0
3.4.0	10G Capable	1 = PCS is capable of operating at 10 Gb/s 0 = PCS is not capable of operating at 10 Gb/s	RO	1

Table 2-28 PCS Devices in Package Registers

Bit	Register	Description	Property	Defaults
3.6.15	Vendor-specific Device 2 Present	The block always returns 0 for these bits.	RO	0
3.6.14	Vendor-specific Device 1 Present	The block always returns 0 for these bits.	RO	0
3.6.13:0	Reserved	Reserved field.	RO	0
3.5.15:6	Reserved	Reserved field.	RO	0
3.5.5	DTE XS Present	1 = DTE XS present in package 0 = DTE XS not present in package	RO	0
3.5.4	PHY XS Present	1 = PHY XS present in package 0 = PHY XS not present in package	RO	0
3.5.3	PCS Present	1 = PCS present in package 0 = PCS not present in package	RO	1
3.5.2	WIS Present	1 = WIS present in package 0 = WIS not present in package	RO	0
3.5.1	PMA/PMD Present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO	1
3.5.0	Clause 22 device present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO	0

Table 2-29 10G PCS Control 2 Registers

Bit	Register	Description	Property	Defaults
3.7.15:2	Reserved	Reserved field.	RO	0
3.7.1:0	PCS Type Selection	The block always returns 01 for these bits and ignores writes.	RO	01

Table 2-30 PCS Status 2 Registers

Bit	Register	Description	Property	Defaults
3.8.15:14	Device present	The block always returns 10.	RO	10
3.8.13:12	Reserved	Reserved field.	RO	0
3.8.11	Transmit local fault	1 = Fault condition on Transmit path 0 = No fault condition on Transmit path Maintain the fixed value 0.	RO	0
3.8.10	Receive local fault	1 = Fault condition on receive path 0 = No fault condition on receive path Latch the high level, and clear after a read operation.	RO LH	0
3.8.9:3	Reserved	Reserved field.	RO	0
3.8.2	10GBASE-W Capable	The block always returns 0 for this bit.	RO	0
3.8.1	10GBASE-X capable	1 = PCS is able to support 10GBASE-X PCS type 0 = PCS is not able to support 10GBASE-X PCS type	RO	1
3.8.0	10GBASE-R capable	The block always returns 0 for this bit.	RO	0

Table 2-31 PCS Package Identifier Registers

Bit	Register	Description	Property	Defaults
3.14.15:0	Package Identifier	The block always returns 0 for these bits.	RO	0
3.15.15:0	Package Identifier	The block always returns 0 for these bits.	RO	0

Table 2-32 10GBASE-X Status Registers

Bit	Register	Description	Property	Defaults
3.24.15:13	Reserved	The block always returns 0 for these bits.	RO	0
3.24.12	10GBASE-X Lane Alignment Status	1 = 10GBASE-X PCS receive lanes aligned 0 = 10GBASE-X PCS receive lanes not aligned	RO	0
3.24.11	Pattern Testing Ability	1 = 10GBASE-X PCS is able to generate test patterns 0 = 10GBASE-X PCS is not able to generate test patterns	RO	1
3.24.10:4	Reserved		RO	0
3.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO	0
3.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO	0
3.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO	0
3.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO	0

Table 2-33 10GBASE-X Test Control Registers

Bit	Register	Description	Property	Defaults
3.25.15:3	Reserved		RO	0
3.25.2	Transmit Test Pattern Enable	1 = Transmit test pattern enable 0 = Transmit test pattern disabled	RW	0
3.25.1:0	Test pattern select	1 0 1 1 = Reserved 1 0 = Mixed-frequency test pattern 0 1 = Low-frequency test pattern 0 0 = High-frequency test pattern	RW	00

Table 2-34 Vendor Specific Registers[8]

Bit	Register	Description	Property	Defaults
3.32768.15:3	Reserved		RO	0
3.32768.2	Force sync	XAUI Core loopback, used when PCS far-end parallel loopback mode is enabled, for testing purposes only. 1: Force word align locking; 0: Use P_PCS_LSM_SYNCED[3:0] of HSSTLP.	RW	0
3.32768.1	Force cdr	XAUI Core loopback, used when PCS near-end parallel loopback mode is enabled, for testing purposes only. 1: Force CDR align locking; 0: Use P_RX_READY of HSSTLP.	RW	0
3.32768.0	Force loss signal	XAUI Core loopback, used when PCS near-end parallel loopback and PMA near-end serial loopback modes are enabled, for testing purposes only. 0: Force signal detect to high; 1: Use P_RX_SIGDET_STATUS of HSSTLP for signal detect.	RW	1

2.6.1.1.2 DTE XGXS

When XAUI operates in the DTE XGXS mode, i.e., when device_addr equals 5, the detailed list is shown in Table 2-35.

Table 2-35 DTE XGXS Register List

Address	Register
5.0	DTE XS Control 1
5.1	DTE XS Status 1
5.2,5.3	DTE XS Device Identifier

8 For detailed descriptions of HSSTLP related signals, please refer to the "***UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide***".

Address	Register
5.4	DTE XS Speed Ability
5.5,5.6	DTE XS Devices in Package
5.7	Reserved
5.8	DTE XS Status 2
5.9 to 5.13	Reserved
5.14, 5.15	DTE XS Package Identifier
5.16 to 5.23	Reserved
5.24	10G DTE XGXS Lane Status
5.25	10G DTE XGXS Test Control
5.26 to 5.32767	Reserved
5.32768	Vendor Specific
5.32769 to 5.65535	Reserved

Table 2-36 DTE XS Control 1 Registers

Bit	Register	Description	Property	Defaults
5.0.15	Reserved	Reserved field.	RO	0
5.0.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode It has the same function as port loop_back.	RW	0
5.0.13	Speed Selection	1 = Operation at 10 Gbp/s and above 0 = Unspecified	RO	1
5.0.12	Reserved	Reserved field.	RO	0
5.0.11	Power down(NA)	Power down by configuring the HSSTLP register via APB, and this register does not operate.	RW	0
5.0.10:7	Reserved	Reserved field.	RO	0
5.0.6	Speed Selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	RO	1
5.0.5:2	Speed Selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10Gb/s	RO	0
5.0.1:0	Reserved	Reserved field.	RO	0

Table 2-37 DTE XS Status 1 Registers

Bit	Register	Description	Property	Defaults
5.1.15:8	Reserved	Reserved field.	RO	0
5.1.7	Local Fault	1 = Local fault detected 0 = No Local Fault detected This bit is set to 1 whenever either of the bits 5.8.11,5.8.10 are set to 1.	RO	0
5.1.6:3	Reserved	Reserved field.	RO	0
5.1.2	DTE XS Receive Link Status	1 = The DTE XS receive link is up. 0 = The DTE XS receive link is down. Latch the low level, and restore to the current Link status after read.	RO LL	0
5.1.1	Power Down Ability	Maintain the fixed value 1.	RO	1
5.1.0	Reserved	Reserved field.	RO	0

Note: "LL" indicates latching the low level, and "LH" indicates latching the high level.

Table 2-38 DTE XS Device Identifier Registers

Bit	Register	Description	Property	Defaults
5.2.15:0	DTE XS Identifier	Maintain the fixed value 0.	RO	0
5.3.15:0	DTE XS Identifier	Maintain the fixed value 0.	RO	0

Table 2-39 DTE XS Speed Ability Registers

Bit	Register	Description	Property	Defaults
5.4.15:1	Reserved	Reserved field.	RO	0
5.4.0	10G Capable	Maintain the fixed value 0.	RO	1

Table 2-40 DTE XS Devices in Package Registers

Bit	Register	Description	Property	Defaults
5.6.15	Vendor-specific Device 2 Present	Maintain the fixed value 0.	RO	0
5.6.14	Vendor-specific Device 1 Present	Maintain the fixed value 0.	RO	0
5.6.13:0	Reserved	Reserved field.	RO	0
5.5.15:6	Reserved	Reserved field.	RO	0
5.5.5	DTE XS Present	1 = DTE XS present in package 0 = DTE XS not present in package	RO	1
5.5.4	PHY XS Present	1 = PHY XS present in package 0 = PHY XS not present in package	RO	0
5.5.3	PCS Present	1 = PCS present in package 0 = PCS not present in package	RO	0

Bit	Register	Description	Property	Defaults
5.5.2	WIS Present	1 = WIS present in package 0 = WIS not present in package	RO	0
5.5.1	PMA/PMD Present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO	1
5.5.0	Clause 22 device present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO	0

Table 2-41 DTE XS Status 2 Registers

Bit	Register	Description	Property	Defaults
5.8.15:14	Device Present	Maintain the fixed value 10.	RO	10
5.8.13:12	Reserved	Reserved field.	RO	0
5.8.11	Transmit Local Fault	1 = Fault condition on Transmit path 0 = No fault condition on Transmit path Maintain the fixed value 0.	RO	0
5.8.10	Receive Local Fault	1 = Fault condition on receive path 0 = No fault condition on receive path Latch the high level, and clear after a read operation.	RO LH	0
5.8.9:0	Reserved	Reserved field.	RO	0

Table 2-42 DTE XS Package Identifier Registers

Bit	Register	Description	Property	Defaults
5.15.15:0	DTE XS Package Identifier	Maintain the fixed value 0.	RO	0
5.14.15:0	DTE XS Package Identifier	Maintain the fixed value 0.	RO	0

Table 2-43 DTE XS Lane Status Registers

Bit	Register	Description	Property	Defaults
5.24.15:13	Reserved	Reserved field.	RO	0
5.24.12	DTE XGXS Lane Alignment Status	1 = DTE XGXS receive lanes aligned 0 = DTE XGXS receive lanes not aligned	RO	0
5.24.11	Pattern testing ability	Maintain the fixed value 1.	RO	1
5.24.10:4	Reserved	Reserved field.	RO	0
5.24.3	Lane 3 Sync	1 = Lane 3 is synchronized; 0 = Lane 3 is not synchronized.	RO	0
5.24.2	Lane 2 Sync	1 = Lane 2 is synchronized; 0 = Lane 2 is not synchronized.	RO	0
5.24.1	Lane 1 Sync	1 = Lane 1 is synchronized; 0 = Lane 1 is not synchronized.	RO	0
5.24.0	Lane 0 Sync	1 = Lane 0 is synchronized; 0 = Lane 0 is not synchronized.	RO	0

Table 2-44 10G DTE XGXS Test Control Registers

Bit	Register	Description	Property	Defaults
5.25.15:3	Reserved	Reserved field.	RO	0
5.25.2	Transmit Test Pattern Enable	1 = Transmit test pattern enable 0 = Transmit test pattern disabled	RW	0
5.25.1:0	Test Pattern Select	11 = Reserved 10 = Mixed frequency test pattern 01 = Low frequency test pattern 00 = High frequency test pattern	RW	00

Table 2-45 Vendor Specific Registers[9]

Bit	Register	Description	Property	Defaults
5.32768.15:3	Reserved	Reserved field.	RO	0
5.32768.2	Force sync	XAUI Core loopback, used when PCS far-end parallel loopback mode is enabled, for testing purposes only. 1: Force word align locking; 0: Use P_PCS_LSM_SYNCED[3:0] of HSSTLP.	RW	0
5.32768.1	Force cdr	XAUI Core loopback, used when PCS near-end parallel loopback mode is enabled, for testing purposes only. 1: Force CDR align locking; 0: Use P_RX_READY of HSSTLP.	RW	0
5.32768.0	Force loss signal	XAUI Core loopback, used when PCS near-end parallel loopback and PMA near-end serial loopback modes are enabled, for testing purposes only. 0: Force signal detect to high; 1: Use P_RX_SIGDET_STATUS of HSSTLP for signal detect.	RW	1

2.6.1.1.3 PHY XS

When XAUI operates in the PHY XS mode, i.e., device_addr equals 4, the detailed list is shown in Table 2-46.

Table 2-46 List of PHY XS Registers

Address	Register
4.0	PHY XS Control 1
4.1	PHY XS Status 1
4.2,4.3	PHY XS Device Identifier

9 For detailed descriptions of HSSTLP-related signals, please refer to the "***UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide***".

Address	Register
4.4	PHY XS Speed Ability
4.5,4.6	PHY XS Devices in Package
4.7	Reserved
4.8	PHY XS Status 2
4.9 to 4.13	Reserved
4.14, 4.15	PHY XS Package Identifier
4.16 to 4.23	Reserved
4.24	10G PHY XGXS Lane Status
4.25	10G PHY XGXS Test Control
4.26 to 4.32767	Reserved
4.32768	Vendor Specific
4.32769 to 4.65535	Reserved

Table 2-47 PHY XS Control 1 Registers

Bit	Register	Description	Property	Defaults
4.0.15	Reserved	Reserved field.	RO	0
4.0.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode It has the same function as port loop_back.	RW	0
4.0.13	Speed Selection	1 = Operation at 10 Gbp/s and above 0 = Unspecified	RO	1
4.0.12	Reserved	Reserved field.	RO	0
4.0.11	Power down(NA)	Power down by configuring the HSSTLP register via APB, and this register does not operate.	RW	0
4.0.10:7	Reserved	Reserved field.	RO	0
4.0.6	Speed Selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	RO	1
4.0.5:2	Speed Selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10Gb/s	RO	0
4.0.1:0	Reserved	Reserved field.	RO	0

Table 2-48 PHY XS Status 1 Registers

Bit	Register	Description	Property	Defaults
4.1.15:8	Reserved	Reserved field.	RO	0
4.1.7	Local Fault	1 = Local fault detected 0 = No Local Fault detected This bit is set to 1 whenever either of the bits 4.8.11,4.8.10 are set to 1.	RO	0
4.1.6:3	Reserved	Reserved field.	RO	0
4.1.2	PHY XS Receive Link Status	1 = The PHY XS receive link is up 0 = The PHY XS receive link is down Latch the low level, and restore to the actual Link state after read.	RO LL	0
4.1.1	Power Down Ability	Maintain the fixed value 1.	RO	1
4.1.0	Reserved	Reserved field.	RO	0

Note: "LL" indicates latching the low level.

Table 2-49 PHY XS Device Identifier Registers

Bit	Register	Description	Property	Defaults
4.2.15:0	PHY XS Identifier	Maintain the fixed value 0.	RO	0
4.3.15:0	PHY XS Identifier	Maintain the fixed value 0.	RO	0

Table 2-50 PHY XS Speed Ability Registers

Bit	Register	Description	Property	Defaults
4.4.15:1	Reserved	Reserved field.	RO	0
4.4.0	10G Capable	Maintain the fixed value 0.	RO	1

Table 2-51 PHY XS Devices in Package Registers

Bit	Register	Description	Property	Defaults
4.6.15	Vendor-specific Device 2 Present	Maintain the fixed value 0.	RO	0
4.6.14	Vendor-specific Device 1 Present	Maintain the fixed value 0.	RO	0
4.6.13:0	Reserved	Reserved field.	RO	0
4.5.15:6	Reserved	Reserved field.	RO	0
4.5.5	DTE XS Present	1 = DTE XS present in package 0 = DTE XS not present in package	RO	0
4.5.4	PHY XS Present	1 = PHY XS present in package 0 = PHY XS not present in package	RO	1
4.5.3	PCS Present	1 = PCS present in package 0 = PCS not present in package	RO	0

Bit	Register	Description	Property	Defaults
4.5.2	WIS Present	1 = WIS present in package 0 = WIS not present in package	RO	0
4.5.1	PMA/PMD Present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO	1
4.5.0	Clause 22 device present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO	0

Table 2-52 PHY XS Status 2 Registers

Bit	Register	Description	Property	Defaults
4.8.15:14	Device Present	Maintain the fixed value 10.	RO	10
4.8.13:12	Reserved	Reserved field.	RO	0
4.8.11	Transmit Local Fault	1 = Fault condition on Transmit path 0 = No fault condition on Transmit path Maintain the fixed value.	RO LH	0
4.8.10	Receive Local Fault	1 = Fault condition on receive path 0 = No fault condition on receive path Latch the high level, and clear after read.	RO LH	0
4.8.9:0	Reserved	Reserved field.	RO	0

Table 2-53 PHY XS Package Identifier Registers

Bit	Register	Description	Property	Defaults
4.15.15:0	PHY XS Package Identifier	Maintain the fixed value 0.	RO	0
4.14.15:0	PHY XS Package Identifier	Maintain the fixed value 0.	RO	0

Table 2-54 PHY XS Lane Status Registers

Bit	Register	Description	Property	Defaults
4.24.15:13	Reserved	Reserved field.	RO	0
4.24.12	PHY XGXS Lane Alignment Status	1 = PHY XGXS receive lanes aligned 0 = PHY XGXS receive lanes not aligned	RO	0
4.24.11	Pattern testing ability	Maintain the fixed value 1.	RO	1
4.24.10:4	Reserved	Reserved field.	RO	0
4.24.3	Lane 3 Sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO	0
4.24.2	Lane 2 Sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO	0
4.24.1	Lane 1 Sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO	0
4.24.0	Lane 0 Sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO	0

Table 2-55 10G PHY XGXS Test Control Registers

Bit	Register	Description	Property	Defaults
4.25.15:3	Reserved	Reserved field.	RO	0
4.25.2	Transmit Test Pattern Enable	1 = Transmit test pattern enable 0 = Transmit test pattern disabled	RW	0
4.25.1:0	Test Pattern Select	11 = Reserved 10 = Mixed frequency test pattern 01 = Low frequency test pattern 00 = High frequency test pattern	RW	00

Table 2-56 Vendor Specific Registers[10]

Bit	Register	Description	Property	Defaults
4.32768.15:3	Reserved		RO	0
4.32768.2	Force sync	XAUI Core loopback, used when PCS far-end parallel loopback mode is enabled, for testing purposes only. 1: Force word align locking; 0: Use P_PCS_LSM_SYNCED[3:0] of HSSTLP.	RW	0
4.32768.1	Force cdr	XAUI Core loopback, used when PCS near-end parallel loopback mode is enabled, for testing purposes only. 1: Force CDR align locking; 0: Use P_RX_READY of HSSTLP.	RW	0
4.32768.0	Force loss signal	XAUI Core loopback, used when PCS near-end parallel loopback and PMA near-end serial loopback modes are enabled, for testing purposes only. 0: Force signal detect to high; 1: Use P_RX_SIGDET_STATUS of HSSTLP for signal detect.	RW	1

2.6.1.2 APB Management Interface

When APB serves as a management interface, register address mapping is shown in Table 2-57.

Table 2-57 APB Interface Mapping Addresses

APB Address Signal	MDIO Address	Register
0x0000	1.0	Physical Medium Attachment/Physical Medium Dependent (PMA/PMD) Control 1
0x0001	1.1	PMA/PMD Status 1
0x0002	1.2,1.3	PMA/PMD Device Identifier
0x0003	1.4	PMA/PMD Speed Ability

10 For detailed descriptions of HSSTLP-related signals, please refer to the "***UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide***".

APB Address Signal	MDIO Address	Register
0x0004	1.5	PMA/PMD Devices in Package
0x0005	1.6	PMA/PMD Devices in Package
0x0006	1.7	10G PMA/PMD Control 2
0x0007	1.8	10G PMA/PMD Status 2
0x0008	1.9	Reserved
0x0009	1.10	10G PMD Receive Signal OK
Reserved	1.11 to 1.13	Reserved
0x000a	1.14, 1.15	PMA/PMD Package Identifier
Reserved	1.16 to 1.65535	Reserved
0x000b	3.0	PCS Control 1
0x000c	3.1	PCS Status 1
0x000d	3.2, 3.3	PCS Device Identifier
0x000e	3.4	PCS Speed Ability
0x000f	3.5,	PCS Devices in Package
0x0010	3.6	PCS Devices in Package
0x0011	3.7	10G PCS Control 2
0x0012	3.8	10G PCS Status 2
Reserved	3.9 to 3.13	Reserved
0x0013	3.14, 3.15	Package Identifier
Reserved	3.16 to 3.23	Reserved
0x0014	3.24	10GBASE-X PCS Status
0x0015	3.25	10GBASE-X Test Control
Reserved	3.26 to 3.32767	Reserved
0x0016	3.32768	Vendor Specific
Reserved	3.32769 to 3.65535	Reserved
0x0017	4.0	PHY XS Control 1
0x0018	4.1	PHY XS Status 1
0x0019	4.2,4.3	PHY XS Device Identifier
0x001a	4.4	PHY XS Speed Ability
0x001b	4.5	PHY XS Devices in Package
0x001c	4.6	PHY XS Devices in Package
0x001d	4.7	Reserved
0x001e	4.8	PHY XS Status 2
Reserved	4.9 to 4.13	Reserved
0x001f	4.14, 4.15	PHY XS Package Identifier
Reserved	4.16 to 4.23	Reserved
0x0020	4.24	10G PHY XGXS Lane Status
0x0021	4.25	10G PHY XGXS Test Control
Reserved	4.26 to 4.32767	Reserved

APB Address Signal	MDIO Address	Register
0x0022	4.32768	Vendor Specific
Reserved	4.32769 to 4.65535	Reserved
0x0023	5.0	DTE XS Control 1
0x0024	5.1	DTE XS Status 1
0x0025	5.2,5.3	DTE XS Device Identifier
0x0026	5.4	DTE XS Speed Ability
0x0027	5.5	DTE XS Devices in Package
0x0028	5.6	DTE XS Devices in Package
0x0029	5.7	Reserved
0x002a	5.8	DTE XS Status 2
Reserved	5.9 to 5.13	Reserved
0x002b	5.14, 5.15	DTE XS Package Identifier
Reserved	5.16 to 5.23	Reserved
0x002c	5.24	10G DTE XGXS Lane Status
0x002d	5.25	10G DTE XGXS Test Control
Reserved	5.26 to 5.32767	Reserved
0x002e	5.32768	Vendor Specific
Reserved	5.32769 to 5.65535	Reserved

2.6.2 HSSTLP Register Description

For HSSTLP IP register descriptions, please refer to "***UG040008_Logos2 Family FPGAs High-Speed Serial Transceiver (HSSTLP) User Guide***" and "***UG041004 _HSSTLP_IP***".

2.6.3 Register Access

XAUI IP provides two types of register management interfaces—APB and MDIO interfaces. Users can enable/disable the MDIO interface through the "MDIO Enable" interface configuration. For detailed descriptions, please refer to "2.3.1.2 IP Parameter Configuration".

2.6.3.1 MDIO Interface Disable

If the MDIO interface is disabled, XAUI IP operates the HSSTLP and XAUI Core registers through the APB interface.

2.6.3.1.1 HSSTLP Register Access

When p_cfg_addr[18] is 0, XAUI IP operates the HSSTLP registers.

- p_cfg_addr[17:2] is the valid address for the HSSTLP registers;
- p_cfg_rdata[7:0] and p_cfg_wdata[7:0] are the valid data for the HSSTLP registers.

2.6.3.1.2 XAUI Core Register Access

When p_cfg_addr[18] is 1, XAUI IP reads and writes the XAUI Core registers.

- p_cfg_addr[17:2] is the valid address for the XAUI Core registers;
- p_cfg_rdata[15:0] and p_cfg_wdata[15:0] are the valid data for the XAUI Core registers.

2.6.3.2 MDIO Interface Enable

If the MDIO interface is enabled, XAUI IP accesses the HSSTLP registers through the APB interface and the XAUI Core registers through the MDIO interface.

2.6.3.2.1 HSSTLP Register Access

XAUI IP operates the HSSTLP registers through the APB interface.

- The highest bit of the address, p_cfg_addr[18], is invalid;
- p_cfg_addr[17:2] is the valid address for the HSSTLP registers;
- p_cfg_rdata[7:0] and p_cfg_wdata[7:0] are the valid data for the HSSTLP registers.

2.6.3.2.2 XAUI Core Register Access

XAUI IP operates the XAUI Core registers through the MDIO interface.

2.6.3.3 Operating the Register Address Mapping Algorithm via the APB Interface

Address mapping is illustrated as follows:

- If the user operates the HSSTLP register at address 0x8001, then p_cfg_addr[18] is 0, p_cfg_addr[17:2] is 0x8001, p_cfg_addr[1:0] is 00, resulting in the mapped address p_cfg_addr[18:0] of 0x020004.
- If a user operates the XAUI Core register at address 0x0003, then p_cfg_addr[18] is 1, p_cfg_addr[17:2] is 0x0003, p_cfg_addr[1:0] is 00, resulting in the mapped address p_cfg_addr[18:0] of 0x04000c.

Table 2-58 XAUI IP Register Address Allocation After Mapping

Register		**Start Address**	**Address Offset**	**Address Offset Unit**
XAUI Core Register		0x040000	0x0~0xb8	0x4
HSSTLP Register	LANE0 PCS	0x000000	0x0~0xffc	0x4
	LANE0 PMA RX	0x001000	0x0~0xffc	0x4
	LANE0 PMA TX	0x002000	0x0~0xffc	0x4
	Reserved	0x003000	0x0~0xffc	0x4
	LANE1 PCS	0x004000	0x0~0xffc	0x4
	LANE1 PMA RX	0x005000	0x0~0xffc	0x4
	LANE1 PMA TX	0x006000	0x0~0xffc	0x4
	Reserved	0x007000	0x0~0xffc	0x4
	LANE2 PCS	0x008000	0x0~0xffc	0x4
	LANE2 PMA RX	0x009000	0x0~0xffc	0x4
	LANE2 PMA TX	0x00a000	0x0~0xffc	0x4
	Reserved	0x00b000	0x0~0xffc	0x4
	LANE3 PCS	0x00c000	0x0~0xffc	0x4
	LANE3 PMA RX	0x00d000	0x0~0xffc	0x4
	LANE3 PMA TX	0x00e000	0x0~0xffc	0x4
	Reserved	0x00f000	0x0~0xffc	0x4
	PLL0	0x010000	0x0~0x3ffc	0x4

2.7 Typical Applications

For typical applications of XAUI IP, please refer to "2.4 Example Design".

2.8 Descriptions and Considerations

2.8.1 Clock Constraints

In applications, the PDS software will automatically constrain the clock o_p_clk2core_tx_0 output by HSSTLP to a regional clock or a global clock. Please note whether the clock path of

o_p_clk2core_tx_0 meets the design intent after PDS routing. Clock attributes can be constrained through the PDS software or by editing the clock properties in the .fdc file, with the method for editing .fdc constraints as follows. Where, $nameInst is the instantiation name when the IP is actually instantiated.

Constrain the clock pcs0_clk to the global clock:

```
define_attribute {t:ips2l_xaui_dut_top_u1.U_$nameInst.ipm2l_xaui_hsstlp_u1.o_p_clk2core_tx_0} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}
```

Constrain the clock pcs0_clk to the regional clock:

```
define_attribute {t:ips2l_xaui_dut_top_u1.U_$nameInst.ipm2l_xaui_hsstlp_u1.o_p_clk2core_tx_0} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFR}
```

2.8.2 HSSTLP Physical Location Constraints

In applications, it is necessary to physically constrain HSSTLP in the .fdc file through PDS according to the actual single board. Physical locations can be constrained through the PDS software or by editing the physical locations in the .fdc file, with the method for editing .fdc constraints as follows. Where, $nameInst is the instantiation name when the IP is actually instantiated.

```
define_attribute {i:ips2l_xaui_dut_top_u1.U_$nameInst.ipm2l_xaui_hsstlp_u1.U_GTP_HSSTLP_WRAPPER.CHANNEL0_ENABLE.U_GTP_HSSTLP_LANE0} {PAP_LOC} {HSSTLP_364_918:U0_HSSTLP_LANE}
define_attribute {i:ips2l_xaui_dut_top_u1.U_$nameInst.ipm2l_xaui_hsstlp_u1.U_GTP_HSSTLP_WRAPPER.CHANNEL1_ENABLE.U_GTP_HSSTLP_LANE1} {PAP_LOC} {HSSTLP_364_918:U1_HSSTLP_LANE}
define_attribute {i:ips2l_xaui_dut_top_u1.U_$nameInst.ipm2l_xaui_hsstlp_u1.U_GTP_HSSTLP_WRAPPER.CHANNEL2_ENABLE.U_GTP_HSSTLP_LANE2} {PAP_LOC} {HSSTLP_364_918:U2_HSSTLP_LANE}
define_attribute {i:ips2l_xaui_dut_top_u1.U_$nameInst.ipm2l_xaui_hsstlp_u1.U_GTP_HSSTLP_WRAPPER.CHANNEL3_ENABLE.U_GTP_HSSTLP_LANE3} {PAP_LOC} {HSSTLP_364_918:U3_HSSTLP_LANE}
define_attribute {i:ips2l_xaui_dut_top_u1.U_$nameInst.ipm2l_xaui_hsstlp_u1.U_GTP_HSSTLP_WRAPPER.PLL0_ENABLE.U_GTP_HSSTLP_PLL0} {PAP_LOC} {HSSTLP_364_918:U0_HSSTLP_PLL}
```

2.8.3 Operating Modes

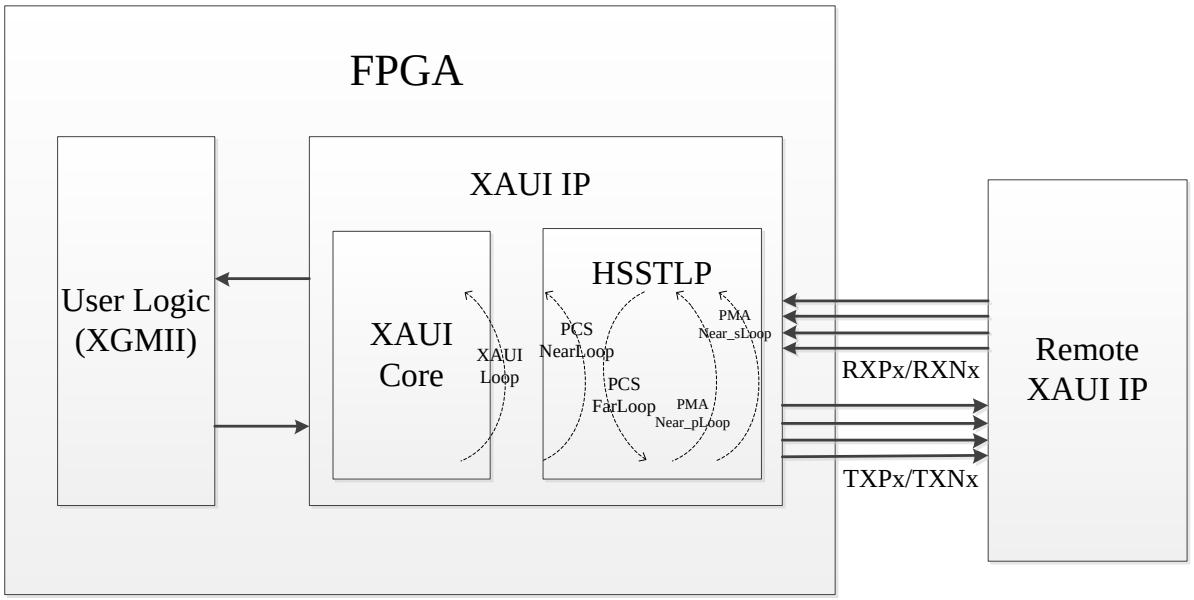

Figure 2-24 Schematic of XAUI IP Operating Mode

XAUI IP communicates with other modules through the differential input/output interface of HSSTLP, and supports two operating modes: loopback mode and test pattern.

2.8.3.1 Loopback Mode

XAUI IP supports five types of loopback modes:

- XAUI Core loopback
- PMA Near-End Serial Loopback
- PMA Near-End Parallel Loopback
- PCS Far-End Loopback
- PCS Near-End Loopback

2.8.3.1.1 XAUI Core loopback

This loopback mode supports two types of configuration: port configuration and register configuration.

Table 2-59 XAUI Core Loopback Port Configurations

Configuration Item	Configuration Descriptions
Port enable	pin_cfg_en=1, enable the port configuration.
Loopback configuration	loop_back=1; Set the XAUI Core register address 3.32768.2:0 to 110.
Non-Loopback configuration	loop_back=0; Set the XAUI Core register address 3.32768.2:0 to 001.

Table 2-60 XAUI Core Loopback Register Configuration

Configuration Item		Configuration Descriptions
Register enable		pin_cfg_en=0, enable register configuration.
10GBASE-X	Loopback configuration	Set the XAUI Core register address 1.0.0 to 1; Set the XAUI Core register address 3.32768.2:0 to 110.
	Non-Loopback configuration	Set the XAUI Core register address 1.0.0 to 0; Set the XAUI Core register address 3.32768.2:0 to 001.
PHY XS	Loopback configuration	Set the XAUI Core register address 4.0.14 to 1; Set the XAUI Core register address 4.32768.2:0 to 110.
	Non-Loopback configuration	Set the XAUI Core register address 4.0.14 to 0; Set the XAUI Core register address 4.32768.2:0 to 001.
DTE XGXS	Loopback configuration	Set the XAUI Core register address 5.0.14 to 1; Set the XAUI Core register address 5.32768.2:0 to 110.
	Non-Loopback configuration	Set the XAUI Core register address 5.0.14 to 0; Set the XAUI Core register address 5.32768.2:0 to 001.

2.8.3.1.2 PMA Near-End Serial Loopback

Attention:

PMA near-end serial loopback mode requires the corresponding register values to be set correctly before enabling the loopback function.

Table 2-61 PMA Near-end Serial Loopback Configuration

Configuration Item		Configuration Descriptions
10GBASE-X	Loopback configuration	Set the XAUI Core register address 3.32768.2:0 to 001.
	Non-Loopback configuration	Set the XAUI Core register address 3.32768.2:0 to 001.
PHY XS	Loopback configuration	Set the XAUI Core register address 4.32768.2:0 to 001.
	Non-Loopback configuration	Set the XAUI Core register address 4.32768.2:0 to 001.

Configuration Item		Configuration Descriptions
DTE XGXS	Loopback configuration	Set the XAUI Core register address 5.32768.2:0 to 001.
	Non-Loopback configuration	Set the XAUI Core register address 5.32768.2:0 to 001.
Port enable	Loopback configuration	i_p_pma_nearend_sloop_0=1 i_p_pma_nearend_sloop_1=1 i_p_pma_nearend_sloop_2=1 i_p_pma_nearend_sloop_3=1
	Non-Loopback configuration	i_p_pma_nearend_sloop_0=0 i_p_pma_nearend_sloop_1=0 i_p_pma_nearend_sloop_2=0 i_p_pma_nearend_sloop_3=0

2.8.3.1.3 PMA Near-End Parallel Loopback

Attention:

PMA near-end parallel loopback mode requires the corresponding register values to be set correctly before enabling the loopback function.

Table 2-62 PMA Near-end Parallel Loopback Configuration

Configuration Item		Configuration Descriptions
10GBASE-X	Loopback configuration	Set the XAUI Core register address 3.32768.2:0 to 010.
	Non-Loopback configuration	Set the XAUI Core register address 3.32768.2:0 to 001.
PHY XS	Loopback configuration	Set the XAUI Core register address 4.32768.2:0 to 010.
	Non-Loopback configuration	Set the XAUI Core register address 4.32768.2:0 to 001.
DTE XGXS	Loopback configuration	Set the XAUI Core register address 5.32768.2:0 to 010.
	Non-Loopback configuration	Set the XAUI Core register address 5.32768.2:0 to 001.
Port enable	Loopback configuration	i_p_pma_nearend_ploop_0=1 i_p_pma_nearend_ploop_1=1 i_p_pma_nearend_ploop_2=1 i_p_pma_nearend_ploop_3=1
Port enable	Non-Loopback configuration	i_p_pma_nearend_ploop_0=0 i_p_pma_nearend_ploop_1=0 i_p_pma_nearend_ploop_2=0 i_p_pma_nearend_ploop_3=0

2.8.3.1.4 PCS Near-End Loopback

Attention:

For the PCS near-end loopback mode, it is necessary to first ensure the corresponding register values are set correctly, then enable the loopback port. Reset HSSTLP RX Lane after completing the loopback configuration.

Table 2-63 PCS Near-end Loopback Configuration

Configuration Item		**Configuration Descriptions**
10GBASE-X	Loopback configuration	Set the XAUI Core register address 3.32768.2:0 to 010.
	Non-Loopback configuration	Set the XAUI Core register address 3.32768.2:0 to 001.
PHY XS	Loopback configuration	Set the XAUI Core register address 4.32768.2:0 to 010.
	Non-Loopback configuration	Set the XAUI Core register address 4.32768.2:0 to 001.
DTE XGXS	Loopback configuration	Set the XAUI Core register address 5.32768.2:0 to 010.
	Non-Loopback configuration	Set the XAUI Core register address 5.32768.2:0 to 001.
Port enable	Loopback configuration	i_p_pcs_nearend_loop_0=1 i_p_pcs_nearend_loop_1=1 i_p_pcs_nearend_loop_2=1 i_p_pcs_nearend_loop_3=1
	Non-Loopback configuration	i_p_pcs_nearend_loop_0=0 i_p_pcs_nearend_loop_1=0 i_p_pcs_nearend_loop_2=0 i_p_pcs_nearend_loop_3=0

2.8.3.1.5 PCS Far-End Loopback

Attention:

PCS far-end loopback mode first requires ensuring the corresponding register values are set correctly, then enabling the loopback function.

For this mode, that the data transmission and reception paths on the link must operate in the same clock domain. Configure the HSSTLP register PMA_REG_PLPBK_TXPCLK_EN==1 to ensure that the link transmission and reception paths operate in the same clock domain. For example: For HSSTLP, set the second bit at PMA TX register offset address 0x0024 for 4 lanes to 0.

For HSSTLP register configuration details, please refer to "***UG040008_Logos2 Family FPGAs High-Speed Serial Transceiver (HSSTLP) User Guide***" and "***UG041004_HSSTLP_IP***".

Table 2-64 PCS Far-end Loopback Configuration

Configuration Item		**Configuration Descriptions**
10GBASE-X	Loopback configuration	Set the XAUI Core register address 3.32768.2:0 to 001. For HSSTLP, set the [4:3] bits at PCS register offset address 0x000c for 4 lanes to 1.
	Non-Loopback configuration	Set the XAUI Core register address 3.32768.2:0 to 001.
PHY XS	Loopback configuration	Set the XAUI Core register address 4.32768.2:0 to 001. For HSSTLP, set the [4:3] bits at PCS register offset address 0x000c for 4 lanes to 1.
	Non-Loopback configuration	Set the XAUI Core register address 4.32768.2:0 to 001.
DTE XGXS	Loopback configuration	Set the XAUI Core register address 5.32768.2:0 to 001. For HSSTLP, set the [4:3] bits at PCS register offset address 0x000c for 4 lanes to 1.
	Non-Loopback configuration	Set the XAUI Core register address 5.32768.2:0 to 001.
Port enable	Loopback configuration	i_p_pcs_farend_loop_0=1 i_p_pcs_farend_loop_1=1 i_p_pcs_farend_loop_2=1 i_p_pcs_farend_loop_3=1
	Non-Loopback configuration	i_p_pcs_farend_loop_0=0 i_p_pcs_farend_loop_1=0 i_p_pcs_farend_loop_2=0 i_p_pcs_farend_loop_3=0

2.8.3.2 Test Patterns

XAUI IP can send Test Patterns for system debugging, which comply with the 48A standard in IEEE 802.3-2012 appendix.

Users can configure XAUI IP to operate in the test pattern in two ways: port configuration and register configuration.

2.8.3.2.1 Port Configuration

Table 2-65 Port Configuration for the Test Patterns Mode

Port Configuration Value	**Description**
pin_cfg_en=1	XAUI Core operates in the port configuration mode, and APB and MDIO interface configurations are ineffective at this time.
test_pattern_enb=1	XAUI IP operates in the Test Patterns mode.
test_pattern_sel	Test Pattern code type selection. 1 1 = Reserved 1 0 = Mixed-frequency Test Pattern 0 1 = Low-frequency Test Pattern 0 0 = High-frequency Test Pattern

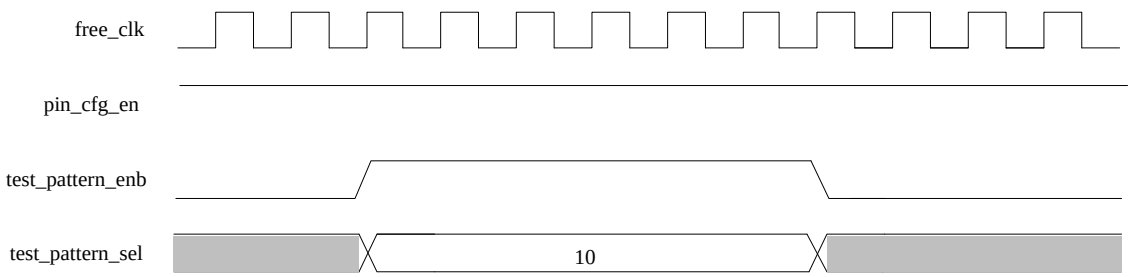

Figure 2-25 Test Pattern Configuration Timing Diagram

2.8.3.2.2 Register Configuration

Table 2-66 Register Configuration for the Test Patterns Mode

Configuration Register Address	**Configuration Register Value**	**Description**
3.25.2:0, corresponding to 10GBASE-X 4.25.2:0, corresponding to DTE XGXS 5.25.2:0, corresponding to PHY XS	0x4	Operate in the Test Patterns mode. The code type is High-frequency Test Pattern.
	0x5	Operate in the Test Patterns mode. The code type is Low-frequency Test Pattern.
	0x6	Operate in the Test Patterns mode. The code type is Mixed-frequency Test Pattern.

2.8.4 Read and Write Operation Examples of the uart_ctrl Module

2.8.4.1 Read Operation

Reading data from address 0x000001: "0x72" + "0x000001", which is 0x72000001.

2.8.4.2 Write Operation

Write 0x02 to address 0x000001: "0x77"+"0x000001"+"0x00000002", results in 0x7700000100000002.

2.9 IP Debugging Method

Debug Core and LEDs can monitor the link status of XAUI IP, please refer to Table 2-8 for the Debug Core signal list, and refer to the descriptions of Debug led indicators in Table 2-5 for the LED indicator list.

In the Example Design, the UART can read the values of the status registers in the IP to monitor the link status. For the use of the UART module, please refer to "2.4.3 Module Description".

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