HSSTLP IP

User Guide

(UG041004, V1.12)

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Revisions History

Document Revisions

Version	Date of Release	Revisions	Applicable IP and Corresponding Versions
V1.12	30.05.2024	Initial release.	V1.12

IP Revisions

IP Version	Date of Release	Revisions
V1.12	30.05.2024	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
3G-SDI	SMPTE STANDARD, Source Image Format and Ancillary Data Mapping for the 3 Gb/s Serial Interface
APB	Advanced Peripheral Bus
CDR	Clock Data Recovery
CTC	Clock Tolerance Compensation
GE	1000BASE-X
HSSTLP	High Speed Serial Transceiver Low Performance
PCIE	PCI Express
SerDes	Serializer Deserializer
SGMII	Serial-GMII Specification
XAUI	10 Gigabit Attachment Unit interface
IPC	IP Compiler
PDS	Pango Design Suite

Related Documentation

The following documentation is related to this manual:

1. ***Pango_Design_Suite_Quick_Start_Tutorial***
2. ***Pango_Design_Suite_User_Guide***
3. ***IP_Compiler_User_Guide***
4. ***Simulation_User_Guide***
5. ***User_Constraint_Editor_User_Guide***
6. ***Physical_Constraint_Editor_User_Guide***
7. ***Route_Constraint_Editor_User_Guide***
8. ***UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide***
9. ***UG042002_Logos2 Family Product 3G-SDI IP User Guide***

Table of Contents

Tables

Figures

Chapter 1 Preface

This chapter describes the scope, structure, and writing standards of this manual to help users quickly find the information they need.

1.1 Introduction of the Manual

This manual is a user guide for the HSSTLP (High Speed Serial Transceiver Low Performance) IP product launched by Pango Microsystems. The IP is based on the HSSTLP resources of the Logos2 family products. The content of this manual primarily includes the IP user guide and related information. Users can use this manual to quickly understand the related features and usage methods of the HSSTLP IP.

1.2 Writing Standards of the Manual

Table 1-1 Description of Writing Standards

Text	**Rules**
Attention	If users ignore the attention contents, they may suffer adverse consequences or fail to operate successfully due to incorrect actions.
Description	Instructions and tips provided for users.

Chapter 2 IP User Guide

This chapter provides a usage guide for the HSSTLP IP, including IP introduction, IP block diagram, IP generation process, Example Design, IP interface description, IP register description, typical applications, notes and precautions, and IP debugging methods. More details on the design process can be found in the following PDS help documentation.

- "***Pango_Design_Suite_Quick_Start_Tutorial***"
- "***Pango_Design_Suite_User_Guide***"
- "***IP_Compiler_User_Guide***"
- "***Simulation_User_Guide***"

2.1 IP Introduction

HSSTLP IP is based on the HSSTLP resources of the Logos2 family products. The IP can be configured and generated using the IPC (IP Compiler) tool in the company's PDS (Pango Design Suite).

2.1.1 Key Features

The functions supported by the HSST IP include:

- Supports independent configuration for four channels;
- Supports independent configuration of four working modes for each channel: "duplex operation", "transmit only", "receive only", and "shut down";
- Supports standard protocols (GE/SGMII, PCIEx1/PCIEx2/PCIEx4, XAUI, 3G-SDI);
- Supports customer-defined protocols;
- Supports configuration of Line Rate;
- Supports bit width configuration for the user-side interface;
- Supports configurable number of PLLs;
- Supports configuration of reference clock;
- Supports 8B10B encoding and decoding enable configuration;
- Supports configurable transparent modes 64B66B and 64B67B;

- Supports Word Alignment enable configuration and COMMA sequence value configuration;
- Supports Channel Bonding enable configuration and Bonding sequence value configuration;
- Supports CTC enable configuration and CTC operation sequence value configuration;
- Supports signal swing configuration
- Supports de-emphasis configuration
- Supports configuration of AC/DC coupling modes for the receiver;
- Termination mode configuration for the receiver;
- Provides a reference for the HSSTLP reset sequence.

2.1.2 Applicable Devices and Packages

Table 2-1 Applicable Devices and Packages for HSSTLP IP

Applicable Devices	**Supported Packages**
PG2L200H	ALL
PG2L100HX	ALL (except for MBG324)
PG2L100H	ALL (except for MBG324)
PG2L50H	ALL (except for FBG256/MBG324)
PG2L25H	ALL

2.2 IP Block Diagram

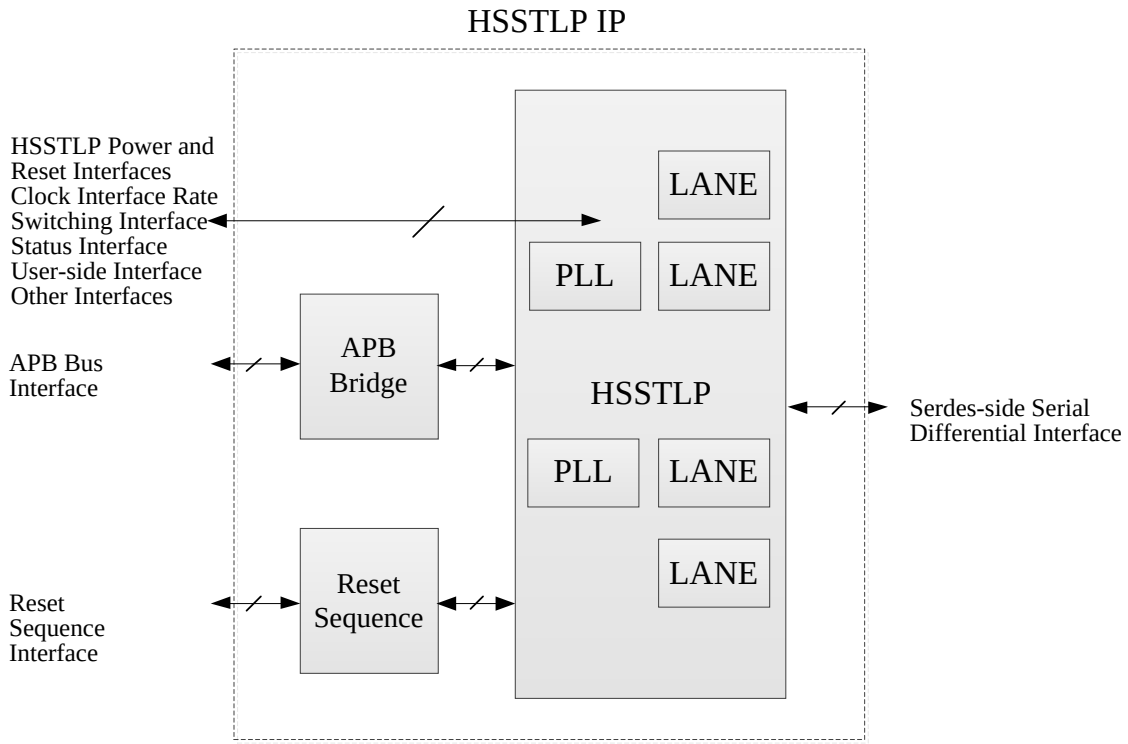

Figure 2-1 Block Diagram of HSSTLP IP Structure

HSST IP comprises the HSSTLP, APB Bridge, and the reset sequence, with the overall block diagram as shown in Figure 2-1. As the device's inherent HSSTLP IP hard core resource, HSSTLP contains 4 LANEs and 2 PLLs; APB Bridge is responsible for mapping the user-side APB bus interface to the APB interfaces of the 4 LANEs and 2 PLLs in the HSST; the reset sequence controls the timing process of HSSTLP power-up, reset, and rate switching. For specific functions, please refer to the reset sequence interface in Table 2-12.

2.2.1 HSSTLP

For specific functions of HSSTLP, please refer to "***UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide***".

2.2.2 APB Bridge

Table 2-2 APB Address Mapping[1]

Address Range	Register
0x0000~0x03FF	LANE0 PCS
0x0400~0x07FF	LANE0 PMA RX
0x0800~0x0BFF	LANE0 PMA TX
0x0C00~0x0FFF	Reserved
0x1000~0x13FF	LANE1 PCS
0x1400~0x17FF	LANE1 PMA RX
0x1800~0x1BFF	LANE1 PMA TX
0x1C00~0x1FFF	Reserved
0x2000~0x23FF	LANE2 PCS
0x2400~0x27FF	LANE2 PMA RX
0x2800~0x2BFF	LANE2 PMA TX
0x2C00~0x2FFF	Reserved
0x3000~0x33FF	LANE3 PCS
0x3400~0x37FF	LANE3 PMA RX
0x3800~0x3BFF	LANE3 PMA TX
0x3C00~0x3FFF	Reserved
0x4000~0x4FFF	PLL0
0x5000~0x5FFF	PLL1

The HSSTLP IP has 4 LANEs and 2 PLLs internally, each LANE and PLL has a separate set of configuration registers and address space. To facilitate user access, the IP has added an APB Bridge module, so users can access all LANEs and PLLs through a single APB bus interface.

The address bus width of a LANE or a PLL is 12 bits. The APB Bridge adds 4 bits as the chip select signal, making the address bus 16 bits. The mapping relationship is shown in Table 2-2.

2.2.3 Reset Sequence

To facilitate the application of HSSTLP by users, a reference reset sequence for power-up, reset,

1 For example, to access the LANE2 PMA RX 0x39 register in the RX, the corresponding hexadecimal address is 0x2439.

and rate switching is available; for the execution timing, please refer to "***UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide***".

The reset sequence has been enhanced with alignment operations and exception handling when Channel Bonding is enabled, as detailed below.

2.2.3.1 Channel Bonding

2.2.3.1.1 TX Channel Clock Synchronisation

When users utilise the Channel Bonding function, the reset sequence controls the P_LANE_SYNC port to carry out clock synchronisation for the TX Channel; the execution is after the P_TX_LANE_PD_DRIVER port is pulled low, with the specific timing shown in Figure 2-2.

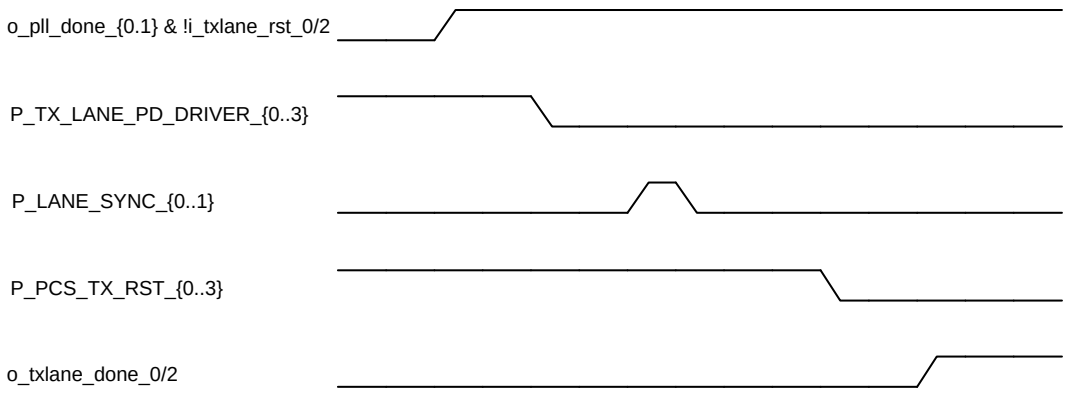

Figure 2-2 Channel Bonding Scenario TX Clock Synchronisation Timing Diagram

2.2.3.1.2 RX Channel Alignment Reset

When using the Channel Bonding function or multi-LANE mode, the reset sequence will perform alignment reset operations on the RX Channel, which is achieved by the user controlling the i_hsstlp_fifo_clr_{0..3} port or through internal signal fifo_clr_en_{0..3}, with timing as shown in Figure 2-3.

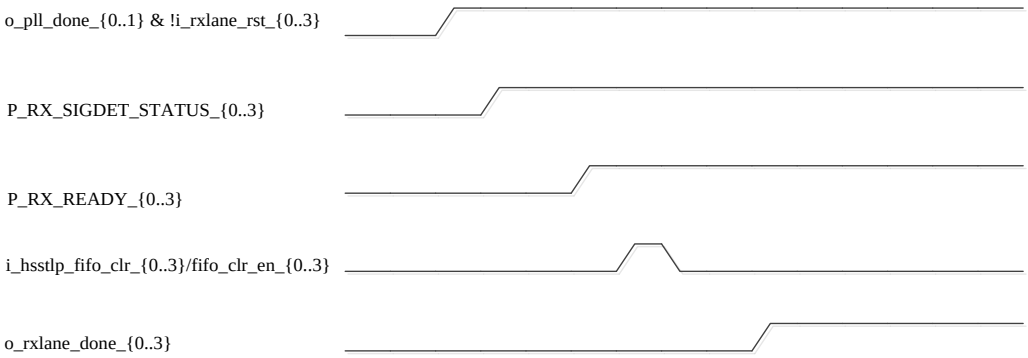

Figure 2-3 Channel Bonding Scenario RX Alignment Operation Timing Diagram

2.2.3.2 Error Handle

2.2.3.2.1 PLL LOCK Anomaly

Added a watchdog to the reset sequence, which monitors the PLL LOCK status. When the PLL fail to LOCK over an extended period and reach the watchdog threshold, the PLL will undergo a power-up reset operation, with timing as shown in Figure 2-4.

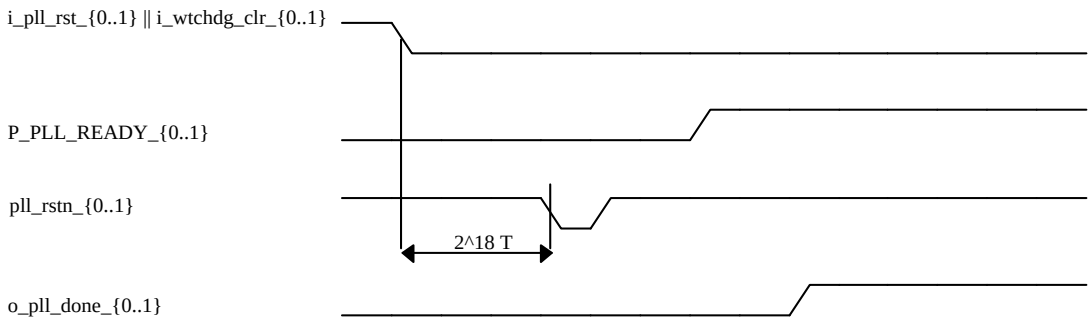

Figure 2-4 Timing Diagram of PLL Power-Up Reset after Not LOCK for Long-Time[2]

2 T denotes the clock cycle of i_free_clk, and pll_rstn_{0..1} is the internal signal of the reset sequence, pulling-down initiates the power-up reset process for the PLL until the PLL LOCK.

2.2.3.2.2 RX Channel Input Anomaly

During normal operation, when there is no data input in the RX Channel or a signal is lost, the signal detection indicator port P_RX_SIGDET_STATUS{0..1} will be pulled low. At this point, the reset sequence will re-execute the reset and un-reset operations for the RX PMA, with the timing as shown in Figure 2-5:

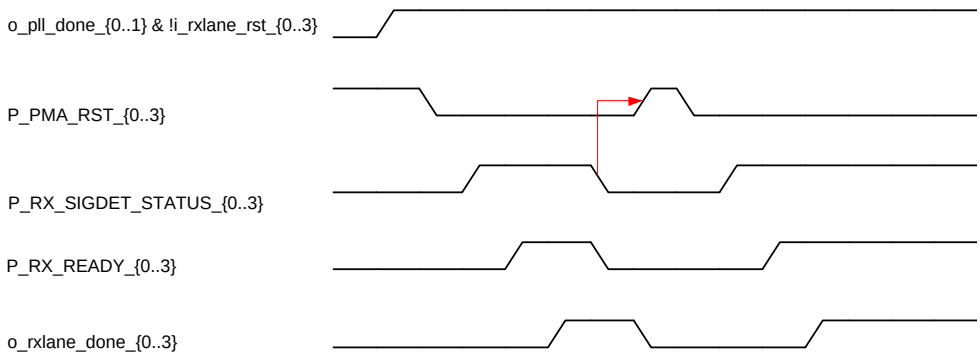

Figure 2-5 RX Channel No Signal Input Anomaly Recovery Timing Diagram

2.2.3.2.3 RX Channel CDR LOCK Anomaly

When the RX Channel CDR cannot LOCK for an extended period, the reset sequence will also re-execute the reset and un-reset operations for the RX PMA, with the timing as shown in Figure 2-6.

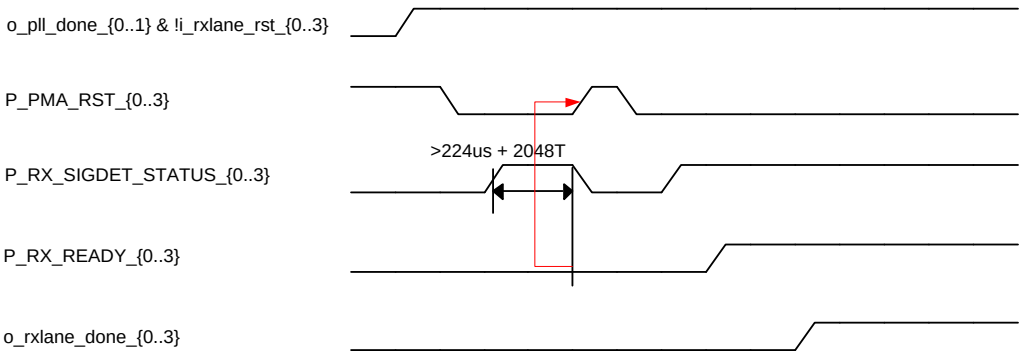

Figure 2-6 Timing Diagram of CDR Anomaly Recovery after Not LOCK for Long-Time

2.2.3.2.4 CDR LOCK Anomaly Pulling Down

During normal operation, if the CDR completion indicator signal P_RX_READY{0..3} for the RX Channel is suddenly pulled low, the reset sequence will also re-execute the reset and un-reset operations for the RX PMA, with the timing as shown in Figure 2-7:

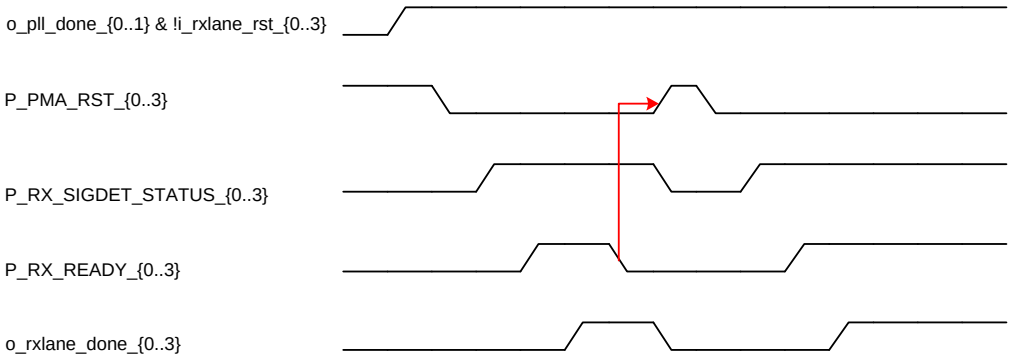

Figure 2-7 CDR LOCK Pulling Down Anomaly Recovery Timing Diagram

2.2.3.2.5 PCS Word Align Anomaly Pulling Down

When enabling Word Align function for the RX Channel PCS, if the Word Align completion indicator signal o_p_pcs_lsm_syned_{0..3} remains low and is not pulled high for an extended period, upon reaching the "Word Align Timer" threshold, the reset sequence will re-execute the reset and un-reset operations for the RX PMA, with the timing as shown in Figure 2-8.

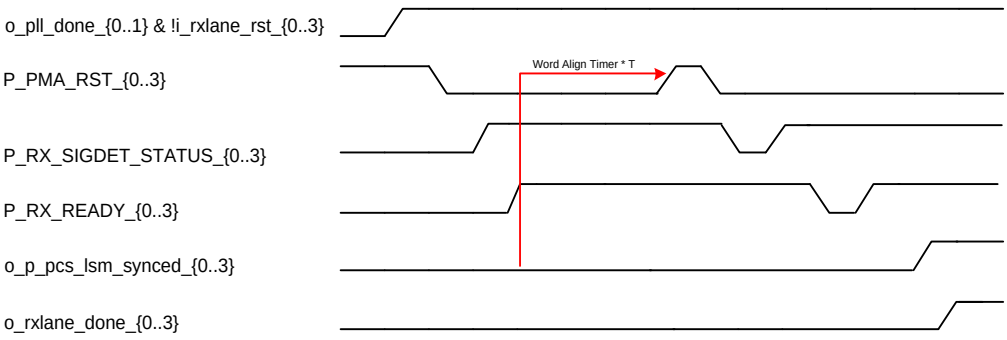

Figure 2-8 PCS Word Align Long-Period Non-Alignment Anomaly Recovery Timing Diagram

2.3 IP Generation Process

2.3.1 Module Instantiation

The configuration of HSSTLP IP can be customised by the IPC tool to instantiate the required IP modules. For detailed instructions on using the IPC tool, please refer to "***IP_Compiler_User_Guide***".

The main steps for the instantiation of the HSSTLP IP module are described as follows.

2.3.1.1 Selecting IP

Open IPC and click File > Update in the main window to open the Update IP dialog box, where you add the corresponding version of the IP model.

After selecting the FPGAs device type, the Catalog interface displays the loaded IP models. Select the corresponding IP version under the "System/HSSTLP" directory; the IP selection path interface is as shown in Figure 2-9. Then set the Pathname and Instance Name on the right side of the page. The project instantiation interface is shown in Figure 2-10.

Notes:

PG2L50H, PG2L25H: The software version must be 2022.1 or above.

PG2L100H: The software version must be 2021.1-SP7.2, 2021.4-SP1, 2022.1 or above.

PG2L200H: The software version must be 2022.2 or above.

PG2L100HX: The software version must be 2023.1 or above.

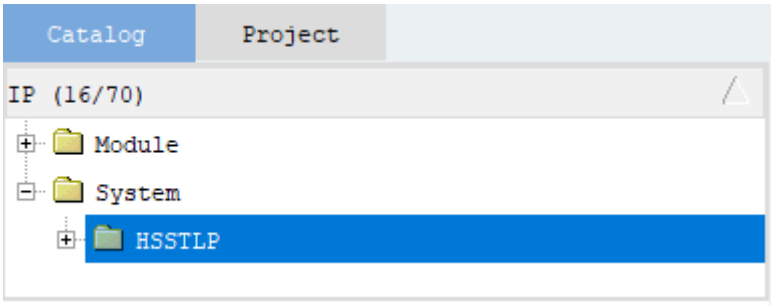

Figure 2-9 HSSTLP IP Selection Path Interface

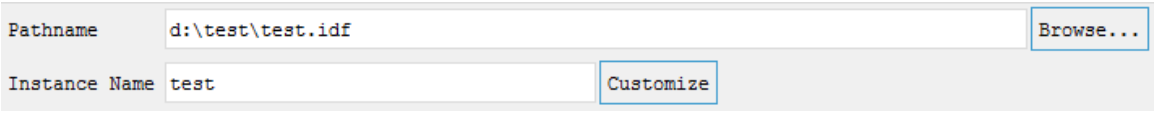

Figure 2-10 Project Instantiation Interface

2.3.1.2 Configure IP Parameters

After selecting the IP, click <Customize> to enter the HSSTLP parameter settings interface, with the Symbol on the left being the interface block diagram, as shown in Figure 2-11; the right side is the parameter configuration window, as shown in Figure 2-12.

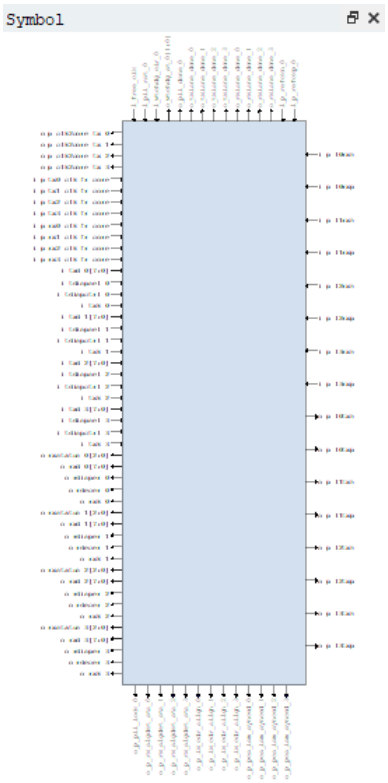

Figure 2-11 HSSTLP IP Interface Block Diagram

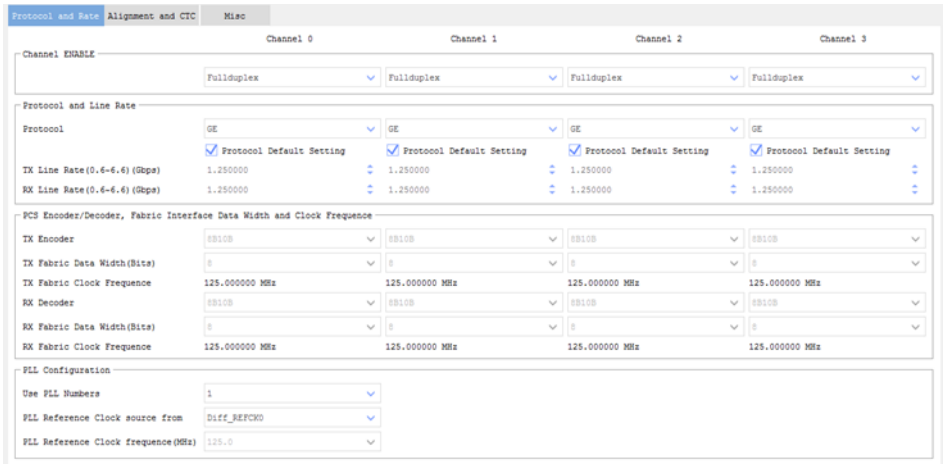

Figure 2-12 Configure HSSTLP IP Parameters Interface

Parameter configuration is divided into three pages, respectively: Protocol and Rate, Alignment and CTC, and Misc. The description of the HSST IP configuration parameters is as follows.

2.3.1.2.1 Protocol and Rate Page Configuration

Table 2-3 Explanation of Protocol and Rate Page Configuration Parameters

Parameter/Configuration Options	**Parameter Description**
Channel ENABLE	Select Channel 0~3 enable modes as Fullduplex, TX_only, RX_only, or DISABLE. When configured to TX_only mode, all the RX-related parameters for the corresponding Channel are turned off; When configured to RX_only mode, all the TX-related parameters for the corresponding Channel are turned off; When configured to DISABLE mode, all related parameters for the corresponding Channel are turned off.

Parameter/Configuration Options	Parameter Description
Protocol and Line Rate	
Protocol	Select the protocol modes for Channel 0~3 as: GE, SGMII, PCIEx1, 3G-SDI[3], CUSTOMERIZEDx1[4], PCIEx2, CUSTOMERIZEDx2[4], TX_CUSTOMERIZEDx2[4], XAUI, PCIEx4, CUSTOMERIZEDx4[4] or TX_CUSTOMERIZEDx4[4]. The aforementioned optional protocol modes, according to the number of SerDes channels used by single customer data channel, can be divided into three categories: single-lane mode[5], dual-lane mode[6,] and quad-lane mode[7]. Notes: CUSTOMERIZEDx2/x4 is used for channel bonding scenarios, where the TX end serial data is output synchronously, and the RX end can configure the data alignment mode between channels (Channel Bonding); When configuring Channel 0~1 as CUSTOMERIZEDx2, the parameters for both channels are bound together; only Channel 0 parameters can be configured, the Channel 1 parameters cannot be altered and must remain consistent with Channel 0, the same applies when configuring Channel 2~3 as CUSTOMERIZEDx2; When configuring Channel 0~3 as CUSTOMERIZEDx4, the parameters for all four channels are bound together; only Channel 0 parameters can be configured, Channel 1/2/3 parameters cannot be altered, and must remain consistent with Channel 0. TX_CUSTOMERIZEDx2/x4 is used for TX channel bonding scenarios, where the TX end serial data is output synchronously and the RX end channel can be configured individually; When configuring Channel 0~1 as TX_CUSTOMERIZEDx2, the TX configuration parameters of the two channels are bound together; only the TX parameters of Channel 0 can be configured; the parameters of Channel 1 cannot be altered and must remain consistent with Channel 0. The same applies when configuring Channel 2~3 as TX_CUSTOMERIZEDx2; When configuring Channel 0~3 as CUSTOMERIZEDx4, the TX parameters of four channels are bound together; only the TX parameters of Channel 0 can be configured; Parameters of Channel 1/2/3 cannot be altered and must remain consistent with Channel 0. (The TX_CUSTOMERIZED mode is only applicable in the TX_FIFO Bypass mode).

3 It corresponds to 3G-SDI configuration mode. For detailed information, please refer to "***UG042002_Logos2 Family Product 3G-SDI IP User Guide***";

4 CUSTOMERIZEDx1 indicates the single-lane customer-defined protocol mode; CUSTOMERIZEDx2 indicates the dual-lane customer-defined protocol mode; CUSTOMERIZEDx4 indicates the quad-lane customer-defined protocol mode; TX_CUSTOMERIZEDx2 indicates the customer-defined protocol mode for a dual-lane Tx end; TX_CUSTOMERIZEDx4 represents the customer-defined protocol mode for a four-lane Tx end.

5 Single-lane mode: 1 customer data channel uses 1 SerDes, including GE, SGMII, PCIEx1, CUSTOMERIZEDx1, and 3G-SDI.

6 Dual-lane mode: 1 customer data channel uses 2 SerDes, including CUSTOMERIZEDx2, PCIEx2, and TX_CUSTOMERIZEDx2.

7 Quad-lane mode: 1 customer data channel uses 4 SerDes, including XAUI, PCIEx4, CUSTOMERIZEDx4, and TX_CUSTOMERIZEDx4.

Parameter/Configuration Options	Parameter Description
Protocol Default Setting	Select whether Channel 0~3 is for fixed protocol configuration, to be used in conjunction with Protocol: When Protocol is configured as CUSTOMERIZEDx1/x2/x4 mode, Protocol Default Setting is fixed and cleared; When Protocol is configured as GE, SGMII, PCIEx1, 3G-SDI, PCIEx2, XAUI or PCIEx4, choose whether to check Protocol Default Setting; when selected, all parameters for the corresponding Channel on the Protocol and Rate page and Alignment and CTC page are non-selectable;
TX Line Rate(0.6~6.6Gbps)	Configure the TX line rate for Channel 0~3, ranging from 0.6 to 6.6Gbps;
RX Line Rate(0.6~6.6Gbps)	Configure the RX line rate for Channel 0~3, ranging from 0.6 to 6.6Gbps;
PCS Encoder/Decoder, Fabric Interface Data Width and Clock Frequence	
TX Encoder	Select the TX encoding mode for Channel 0~3 as 8B10B, 64B66B_transparent, 64B67B_transparent or Bypassed.
TX Fabric Data Width(Bits)	Select the TX Fabric data width for Channel 0~3, on the premise of ensuring that the Fabric clock does not exceed 206.25MHz: When configured in 8B10B encoding mode, data width options are 8/16/32 bits; When configured in 64B66B_transparent mode, data width options are 16/32 bits; When configured in 64B67B_transparent mode, data width options are 16/32 bits; When configured in Bypassed encoding mode, data width options are 8/10/16/20/32/40 bits.
TX Fabric Clock Frequence	TX Fabric clock frequency for Channel 0~3 depends on the configuration of TX Line Rate, TX Encoder and TX Fabric Data Width.
RX Decoder	Select the RX decoding mode for Channel 0~3 as 8B10B, 64B66B_transparent, 64B67B_transparent, or Bypassed.
RX Fabric Data Width(Bits)	Select the RX Fabric data width for Channel 0~3, on the premise of ensuring that the Fabric clock does not exceed 206.25MHz: When configured in 8B10B decoding mode, data width options are 8/16/32 bits; When configured in 64B66B_transparent mode, data width options are 16/32 bits; When configured in 64B67B_transparent mode, data width options are 16/32 bits; When configured in Bypassed decoding mode, data width options are 8/10/16/20/32/40 bits;
RX Fabric Clock Frequence	RX Fabric clock frequency for Channel 0~3 depends on the configuration of RX Line Rate, RX Encoder, and RX Fabric Data Width.
PLL Configuration	
Use PLL Number	Select the number of PLLs, 1 or 2. When one PLL is selected, both the TX and RX channels derive from the same PLL, which is PLL0 by default. If users need to use PLL1 separately, they can modify the physical constraints; When two PLLs are selected, the TX and RX channels can be independently configured to originate either from PLL0 or PLL1. This scenario does not support all TX/RX channels being configured to originate from PLL1; otherwise, a warning will be reported.

Parameter/Configuration Options	Parameter Description
PLL Reference Clock source from	For PLL reference clocks, user may select: Diff_REFCK0: Select the clock from the differential clock interface i_p_refckn_0/i_p_refckp_0 (REFCLK_CML_N_0/REFCLK_CML_P_0); Diff_REFCK1: Select the clock from the differential clock interface i_p_refckn_1/i_p_refckp_1 (REFCLK_CML_N_1/REFCLK_CML_P_1); Fabric_REFCK0: Select the clock from i_p_pll_ref_clk_0 (P_PLL_REF_CLK_0); Fabric_REFCK1: Select the clock from i_p_pll_ref_clk_1 (P_PLL_REF_CLK_1).
PLL Reference Clock frequence(MHz)	Select a valid value of PLL reference clock.
PLL1 Reference Clock source from	Select the PLL1 reference clock, valid when Use PLL Number is configured as 2. Diff_REFCK0: Select the clock from the differential clock interface i_p_refckn_0/i_p_refckp_0 (REFCLK_CML_N_0/REFCLK_CML_P_0); Diff_REFCK1: Select the clock from the differential clock interface i_p_refckn_1/i_p_refckp_1 (REFCLK_CML_N_1/REFCLK_CML_P_1); Fabric_REFCK0: Select the clock from i_p_pll_ref_clk_0 (P_PLL_REF_CLK_0); Fabric_REFCK1: Select the clock from i_p_pll_ref_clk_1 (P_PLL_REF_CLK_1).
PLL1 Reference Clock frequence(MHz)	Select a valid value of PLL1 reference clock, valid when Use PLL Number is configured as 2. When Use The Same Reference Clock is selected, the value must be consistent with that of PLL0; if no same value exists, default to 0 and report a warning message.
Use The Same Reference clock	Select whether PLL0 and PLL1 use the same reference clock, valid when Use PLL Number is configured as 2. Selected: PLL0 and PLL1 use the same reference clock; Cleared: PLL0 and PLL1 have independently configured reference clocks.
TX/RX Channel PLL Selection	
TX Channel PLL source from	Select the PLL used by TX Channel 0~3; valid when the Use PLL Number is configured as 2. PLL0: Select the output clock from PLL0; PLL1: Select the output clock from PLL1.
RX Channel PLL source from	Select the PLL used by RX Channel 0~3; valid when the Use PLL Number is configured as 2. PLL0: Select the output clock from PLL0; PLL1: Select the output clock from PLL1.

2.3.1.2.2 Alignment and CTC Page Configuration

Table 2-4 Explanation of Alignment and CTC Page Configuration Parameters

Parameter/Configuration Options	**Parameter Description**
Word Alignment	
Word Align Mode	Select the Word Align mode for Channel 0~3 as: GE_MODE: Corresponds to PCS_CHx_ALIGN_MODE[8]=1GB; XAUI_MODE: Corresponds to PCS_CHx_ALIGN_MODE=10GB; RAPIDIO_MODE: Corresponds to PCS_CHx_ALIGN_MODE=RAPIDIO; CUSTOMERIZED_MODE: Corresponds to PCS_CHx_ALIGN_MODE=OUTSIDE; at this point, the i_p_pcs_word_align_en_{0..3}(P_PCS_WORD_ALIGN_EN[3:0])[9] interface is valid; [Bypassed]: Corresponds to PCS_CHx_BYPASS_WORD_ALIGN=TRUE; selectable only when the RX Decoder is set to Bypassed.
COMMA code-group select	When Word Align mode is not set to Bypassed, select the byte format for Channel 0~3 Word Align as COMMA, K28.1, K28.5, or K28.7; Or select CUSTOMERIZED to customize the byte format of Word Align.
COMMA+ code-group(10bits)	When the byte format of Word Align is CUSTOMERIZED, it is used to customize the byte format for Channel 0~3 Word Align, corresponding to PCS_CHx_COMMA_REG0, and the complement of PCS_CHx_COMMA_REG1; The defined value needs to be in a 10-bit binary format.
COMMA MASK(bin)	When the byte format of Word Align is CUSTOMERIZED, it is used to customize the byte format for Channel 0~3 Word Align, corresponding to PCS_CHx_COMMA_MASK; The defined value needs to be in a 10-bit binary format.
Channel Bonding	
Channel Bonding Mode	Select the Channel Bonding mode for Channel 0~3 as: XAUI_MODE: Corresponds to PCS_CHx_CEB_MODE=10GB; RAPIDIO_MODE: Corresponds to PCS_CHx_CEB_MODE=RAPIDIO_MODE; CUSTOMERIZED_MODE: Corresponds to PCS_CHx_CEB_MODE=OUTSIDE; at this point, the i_p_pcs_mcb_ext_en_{0..3}(P_PCS_MCB_EXT_EN[3:0]) interface is valid; Bypassed: Corresponds to PCS_CHx_BYPASS_BONDING=TRUE; permanently set to Bypassed when in Single Lane mode or when RX Decoder is selected as Bypassed.
Channel Bonding Special Code(bin)	When Channel Bonding mode is not set to Bypassed, select the K code for the Channel Bonding mode of Channel 0~3, corresponding to PCS_CHx_A_REG.
Channel Bonding Range(UI)	When Channel Bonding mode is not set to [Bypassed], select the skew range for the Channel Bonding mode of Channel 0~3, corresponding to PCS_CHx_SEACH_OFFSET.

8 Uniform description constraint: PCS_CHx_* is an HSSTLP parameter; for details, please refer to the descriptions in "***UG040008_Logos2 Logos Family FPGAs High Speed Serial Transceivers (HSSTLP) User Guide***".

9 Uniform description constraint: If the IP pin name i_x or o_x is followed directly by (*), * indicates the corresponding HSSTLP pin in "***UG040008_Logos2 Family FPGAs High Speed Serial Transceivers (HSSTLP) User Guide***".

Parameter/Configuration Options	Parameter Description
Clock Tolerance Compensation	
CTC Mode	Select the CTC mode for adding or deleting SKIP bytes for Channel 0~3: GE: Perform CTC operations in accordance with the 1000GBASE-X protocol; XAUI: Perform CTC operations in accordance with the XAUI protocol; PCIE_2BYTE: Perform CTC operations with two bytes in accordance with the PCIE protocol; PCIE_4BYTE: Perform CTC operations with four bytes in accordance with the PCIE protocol; CUSTOMERIZED_1BYTE: One byte can be customized for CTC operations; CUSTOMERIZED_2BYTE: Two bytes can be customized for CTC operations; CUSTOMERIZED_4BYTE: Four bytes can be customized for CTC operations; [Bypassed]: Corresponds to PCS_CHx_BYPASS_CTC=TRUE; fixed as Bypassed when RX Decoder is set to Bypassed or when the clock frequency of TX Fabric does not match RX Fabric.
SKIP Byte#0(9bits)	Configure the first SKIP byte for Channel 0~3; The decoded value is in 9-bit binary format, where the high bit "0" indicates a data byte and "1" indicates a control byte, same below.
SKIP Byte#1(9bits)	Configure the second SKIP byte for Channel 0~3.
SKIP Byte#2(9bits)	Configure the third SKIP byte for Channel 0~3.
SKIP Byte#3(9bits)	Configure the fourth SKIP byte for Channel 0~3.

2.3.1.2.3 Misc Page Configuration

Table 2-5 Explanation of Misc Page Configuration Parameters

Parameter/Configuration Options	Parameter Description
Reset Sequence Config	
Reset Sequence	Choose whether to enable the reset sequence.
Free Clock frequence(10~100 MHz)	Configuration of the clock frequency for i_free_clk.
RXPCS Align Timer(0~65535 cycles)	Configure the RXPCS_ALIGN_TIMER threshold for the reset sequence in Channel 0~3. When Bypassed is cleared for the Word Align Mode, the time from when a valid signal is detected on the RX side (i.e., o_p_lx_cdr_ align_{0..3}=1) to when Word Align synchronisation is successful (i.e., o_p_pcs_lsm_synced_{0..3}=1) must not exceed the number of Free Clock cycles set by RXPCS_ALIGN_TIMER, otherwise the RX reset sequence will automatically restart; When Protocol Default Setting is cleared and Word Align mode is not set to Bypassed, users must configure the threshold value of RXPCS_ALIGN_TIMER, with a range of 0~65535.

Parameter/Configuration Options	Parameter Description
Channel Insertion Loss	
TX Pre-Cursor Emphasis Enable	Select whether to enable the pre-cursor De-emphasis configuration for Channel 0~3. Cleared: Disable the pre-cursor De-emphasis configuration; Selected: Enable the pre-cursor De-emphasis configuration; The corresponding parameter is PMA_REG_PD_PRE.
TX Pre-Cursor Emphasis Static Setting	Configure the recommended pre-cursor De-emphasis value for Channel 0~3. The corresponding parameter is PMA_REG_TX_CFG_PRE[10]. Note: When pre-cursor and post-cursor are used simultaneously, the total value of PMA_REG_CFG_POST and PMA_REG_TX_CFG_PRE must be less than 36, otherwise a warning will be reported.
TX Post-Cursor Emphasis Enable	Select whether to enable the post-cursor De-emphasis configuration for Channel 0~3: Cleared: Disable the post-cursor De-emphasis configuration; Selected: Enable the post-cursor De-emphasis configuration; The corresponding parameter is PMA_REG_TX_PD_POST.
TX Post-Cursor Emphasis Static Setting	Configure the recommended post-cursor De-emphasis value for Channel 0~3. The corresponding parameter is PMA_REG_TX_CFG_POST[10]. Note: When the pre-cursor and post-cursor methods are used simultaneously, the total value of PMA_REG_CFG_POST and PMA_REG_TX_CFG_PRE must be less than 36, otherwise a warning will be reported in the IP interface.
TX FFE Dynamic Control	Select whether to enable De-emphasis dynamic switching for Channel 0~3. Selected: Enable De-emphasis switching through the i_p_lx_deemp_ctl_{0..3}(P_TX_DEEMP) interface; Cleared: Disable De-emphasis switching. i_p_lx_deemp_ctl_{0..3} is: 00: The current TX De-emphasis value is the post-cursor De-emphasis recommended value; 01: The current TX De-emphasis value is the post-cursor TX Config Post1 recommended value; 10: The current TX De-emphasis value is the post-cursor TX Config Post2 recommended value; 11: Reserved. Note: This function only supports the post-cursor method. When this function is selected, it is not possible to configure the de-emphasis value using the pre-cursor method. For details, please refer to *"**UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide**"*.
TX Config Post1	Configure the Post1 post-cursor De-emphasis value for Channel 0~3; The configuration is valid when TX FFE Dynamic Control is selected; Recommended configuration values should be consistent with post-cursor De-emphasis. The corresponding parameter is PMA_REG_TX_CFG_POST1[10].
TX Config Post2	Configure the Post2 post-cursor De-emphasis value for Channel 0~3; The configuration is valid when TX FFE Dynamic Control is selected. Recommended configuration values should be consistent with post-cursor De-emphasis. The corresponding parameter is PMA_REG_TX_CFG_POST2[10].

10 For specific level correspondence, please refer to "***UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide***";

Parameter/Configuration Options	Parameter Description
PMA Receiver Front End Config	
RX Termination Mode	Configure the Channel 0~3 PMA Receiver Front End modes, which are respectively: external DC, internal DC; external DC, internal AC; external AC, internal AC; external AC, internal DC. The corresponding parameter is PMA_CH_REG_RX_TERM_MODE_CTRL. For details, please refer to ***"UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide"***.
RX Signal-detect Threshold	Configure the detection threshold voltage for the receiver signal of Channel 0–3, which are: 63MV(Reserved) and 72MV. The default value is 72MV, corresponding to the parameter PMA_CH_REG_RX_SIGDET_VTH; This configuration item must be configured according to the power noise of the test board.
APB Bus Enable	
APB Bus Enable	Select whether to enable the APB bus interface. The APB naming convention for the HSSTLP IP is i_xxx or o_xxx, which one-by-one corresponds to the HSSTLP APB interfaces, as described in the "***UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide***".
Show HSSTLP Optional Pins	
Show HSSTLP Optional Pins	Select whether to display the optional interfaces of the HSSTLP IP, for details, please refer to "2.5.2 Optional Interface Description".
Show Reset Sequence Optional Pins	
Show Reset Sequence Optional Pins	Select whether to display optional interfaces related to the reset sequence, for details, please refer to "2.5.2 Optional Interface Description".

2.3.1.3 Generating IP

Upon completion of parameter configuration, click the <Generate> button in the top left corner to generate the IP. The information report interface for IP generation is shown in Figure 2-13.

Figure 2-13 HSSTLP IP Generation Report Interface

Attention:

The .pds and .fdc files generated with the IP are for reference only; please modify the pin constraints according to the actual pin connections when in use.

Upon successful IP generation, the files shown in Table 2-6 will be output to the specified path in Figure 2-10.

Table 2-6 Output Files after IP Generation

Output File[11]	**Description**
$instname.v	The top-level .v file of the generated IP.
/rtl/ipm2l_hsstlp_wrapper_*.v	The top-level .v file of the HSSTLP module.
/rtl/ipm2l_hsstlp_apb_bridge_*.v	APB bus access-related .v files.
/rtl/ipm2l_hsstlp_rst/*.v	All .v files related to the reset sequence
/example_design/*/*.v	.v files for reference design or IP simulation
/pnr/core_only/$instname.pds	Project files for the generated IP core are used as reference for the user's project.
/pnr/core_only/$instname.fdc	Constraint reference files for the generated IP core are used as reference for the user's project.
/pnr/example_design/pango_hsstlp_top.pds	Project files from Example Design are used as reference for the user's project[12].
/pnr/example_design/pango_hsstlp_top.fdc	Constraint reference files for the Example Design are used as reference for the user's project.
/sim/modelsim/pango_hsstlp_top_sim.do	The do script files for ModelSim simulation of the generated Example Design.
/sim/modelsim/pango_hsstlp_top_wave.do	The do waveform files for ModelSim simulation of the generated Example Design.
/sim/modelsim/sim.bat	The automated script for running ModelSim simulations of the generated Example Design; simulation result file vsim_inst_tb_top.log[13] genereated after execution.
/sim/modelsim/pango_hsstlp_top_filelist.f	The list of .v files required for ModelSim simulation of the generated Example Design.
/rev_1	The default output path for synthesis reports. (This folder is generated only after specifying the synthesis tool)
readme.txt	The readme file describes the structure of the generation directory after the IP is generated.

11 "$instname" is the instantiation name entered by the user; "*" is a wildcard character representing filenames of the same type.

12 Note: The current version does not support simulation with an external PLL scenario.

13 Note: Simulation is not supported when the IP is configured as a non duplex mode or when the TX/RX rates are inconsistent.

2.3.1.4 Paramater Description

Table 2-7 Parameter Description List

Page	Parameter/Configuration Options	Parameter Description	Default Value
Protocol and Rate	Channel ENABLE	Configure the channel working mode	Fullduplex
	Protocol	Configuration the channel protocol	GE
	Protocol Default Setting	Configure whether to enable the default settings	Enabled
	TX Line Rate(0.6~6.375Gbps)	Configure the channel TX line rate	1.25Gbps
	RX Line Rate(0.6~6.375Gbps)	Configure the channel RX line rate	1.25Gbps
	TX Encoder	Configure the channel TX encoding mode	8B10B
	TX Fabric Data Width(Bits)	Configure the channel TX user-side data width	8
	TX Fabric Clock Frequence	Display the TX user-side operational clock frequency	125MHz
	RX Decoder	Configure the channel RX encoding mode	8B10B
	RX Fabric Data Width(Bits)	Configure the channel RX user-side data width	8
	RX Fabric Clock Frequence	Display the RX user-side operational clock frequency	125MHz
	Use PLL Numbers	Configure the number of PLLs used	1
	PLL Reference Clock source from	Configure the PLL reference clock source	Diff_REFCK0
	PLL Reference Clock frequence(MHz)	Select a valid PLL reference clock value	125
Alignment and CTC	Word Align Mode	Configure the synchronization state machine for COMMA alignment scenarios	GE_MODE
	COMMA code-group select	Configure the control word for Word align alignment	K28.5
	COMMA+ code-group(10bits)	Configure custom alignment control word	0101111100
	COMMA MASK(bin)	Configure whether to mask the field of the alignment word	0000000000
	Channel Bonding Mode	Configure the Channel Bonding mode of the channel	Bypassed
	Channel Bonding Special Code(bin)	Configure the A Pattern Reg value	-
	Channel Bonding Range(UI)	Configure the Channel Bonding Deskew range value	-
	CTC Mode	Configure CTC mode value:	GE
	SKIP Byte#0(9bits)	Configure the first SKP byte	110111100
	SKIP Byte#1(9bits)	Configure the second SKP byte	001010000
	SKIP Byte#2(9bits)	Configure the third SKP byte	0
	SKIP Byte#3(9bits)	Configure the fourth SKP byte	0

Page	Parameter/Configuration Options	Parameter Description	Default Value
Misc	Reset Sequence	Configure whether to enable the reset sequence	Enabled
	Free Clock frequence(10~100 MHz)	Configure the operating clock frequency of the reset sequence	100
	RXPCS Align Timer(0~65535 cycles)	Configure the exception handling threshold when word align is enabled	32767
	TX Pre-Cursor Emphasis Enable	Configure the pre-cursor de-emphasis enable	Disabled
	TX Pre-Cursor Emphasis Static Setting	Configure the pre-cursor de-emphasis value	5'b00000
	TX Post-Cursor Emphasis Enable	Configure the post-cursor de-emphasis enable	Disabled
	TX Post-Cursor Emphasis Static Setting	Configure the post-cursor de-emphasis value	5'b00000
	TX FFE Dynamic Control	Configure the TX FFE function	Disabled
	TX Config Post1	Configure the post-cursor Config1 de-emphasis value	5'b00000
	TX Config Post2	Configure the post-cursor Config2 de-emphasis value	5'b00000
	RX Termination Mode	Configure the RX coupling method	external AC, internal DC
	RX Signal-detect Threshold	Configure the PMA Receiver signal detection threshold	72MV
	APB Bus Enable	Configure the APB bus interface	Disabled
	P_REFCK2CORE_{0..1}	Configure the enable port P_REFCK2CORE_{0..1}	Disabled
	TX{0..3}_CLK2_FR_CORE	Configure the enable port TX{0..3}_CLK2_FR_CORE	Disabled
	TX{0..3} External PLL Ready	Configure the enable port i_pll_lock_tx_{0…3}	Disabled
	TX{0..3} Swing Control	Configure the enable port TX{0..3} Swing Control	Disabled
	TX{0..3} ELECIDLE Enable	Configure the enable port TX{0..3} ELECIDLE Enable	Disabled
	TX{0..3} Beacon Enable	Configure the enable port TX{0..3} Beacon Enable	Disabled
	TX{0..3} Rate Channel Select	Configure the enable port TX{0..3} Rate Channel Select	Disabled
	RX{0..3} Rate Channel Select	Configure the enable port RX{0..3} Rate Channel Select	Disabled
	RX{0..3}_CLK2_FR_CORE	Configure the enable port RX{0..3}_CLK2_FR_CORE	Disabled
	RX{0..3} External PLL Ready	Configure the enable port RX{0..3} External PLL Ready	Disabled
	RX{0..3}_Hi-z Control	Configure the enable port RX{0..3}_Hi-z Control	Disabled
	RX{0..3} OOB Status	Configure the enable port RX{0..3} OOB Status	Disabled
	RX{0..3} Detection	Configure the enable port RX{0..3} Detection	Disabled
	RX{0..3} CLK Slip	Configure the enable port RX{0..3}_CLK_SLIP	Disabled
	RX{0..3} Polarity Invert	Configure the enable port RX{0..3} Polarity Invert	Disabled

Page	Parameter/Configuration Options	Parameter Description	Default Value
	CH{0..3} Debug Bus	Configure the enable port CH{0..3} Debug Bus	Disabled
	PLL0 Reset	Configure the enable port i_pll_rst0	Enabled
	PLL1 Reset	Configure the enable port i_pll_rst1	Disabled
	PLL0 WatchDag Clear	Configure the enable port i_pll_wtchdg_clr0	Enabled
	PLL1 WatchDag Clear	Configure the enable port i_pll_wtchdg_clr1	Disabled
	PLL0 Status	Configure the enable port i_pll_done_0 and o_wtchdg_st0[1:0]	Enabled
	PLL1 Status	Configure the enable port i_pll_done_1 and o_wtchdg_st1[1:0]	Disabled
	TX{0..3} Reset	Configure the enable port i_txlane_rst_{0..3}	Disabled
	TX{0..3} Rate Change Select	Configure the enable port i_tx_rate_chng_{0..3}	Disabled
	RX{0..3} Reset	Configure the enable port i_rxlane_rst_{0..3}	Disabled
	RX{0..3} Rate Change Select	Configure the enable port i_rx_rate_chng_{0..3} and i_rxckdiv_{0..3}	Disabled
	RX{0..3} Debug Bus	Configure the enable port i_hsst_fifo_clr_{0..3} and i_loop_dbg_{0..3}[2:0]	Disabled

Note: "-" indicates that there is no default value for this parameter in the IP configuration interface.

2.3.2 Constraint Configuration

For the specific configuration method of constraint files, please refer to the relevant help documents in the PDS installation path: "***User_Constraint_Editor_User_Guide***", "***Physical_Constraint_Editor_User_Guide***", "***Route_Constraint_Editor_User_Guide***".

2.3.3 Simulation Runs

The simulation of HSST IP is based on the Test Bench of Example Design. For detailed information about Example Design, please refer to "2.4 Example Design".

For more details about the PDS simulation functions and third-party simulation tools, please consult the related help documents in the PDS installation path: "***Pango_Design_Suite_User Guide***", "***Simulation_User_Guide***".

2.3.3.1 VCS simulation

Enter the directory/sim/vcs path of the IP, execute "make" to start the simulation.

2.3.3.2 Questasim simulation

Enter the directory/sim/modelsim path of the IP, execute "sim.bat" to start the simulation.

2.3.4 Synthesis and Placement/Routing

The specific usage of PDS synthesis tools and placement/routing tools can be found in the help documents within the PDS installation path.

Attention:

Example Design project files .pds and pin constraint files .fdc generated with the IP are located in the "/pnr/example_design" directory, and physical constraints need to be modified according to the actual devices and PCB trace routing. For details, please refer to "2.8 Descriptions and Considerations".

2.3.5 Resources Utilization

Table 2-8 Typical Values of Resource Utilization for HSSTLP IP Based on Applicable Devices

Device	**Configuration Mode**	**Typical Values of Resource Utilization**			
		LUT	**FF**	**USCM**	**HSSTLP**
PG2L200H	1 HSSTLP	1053	740	9	1
PG2L100HX	1 HSSTLP	991	750	9	1
PG2L100H	1 HSSTLP	1215	765	9	1
PG2L50H	1 HSSTLP	1277	743	10	1
PG2L25H	1 HSSTLP	1279	743	10	1

2.4 Example Design

This section mainly introduces the Example Design scheme based on HSSTLP IP. The scheme involves interfacing two HSST IPs, exchanging data, and using bit-by-bit comparison to verify the correctness of the received data. The scheme can read and write registers through the APB interface.

2.4.1 Design Block Diagram

Figure 2-14 is the block diagram of the HSSTLP IP Example Design, which utilises docking tests; instance_name refers to the IP name set in the Figure 2-10 interface as Instance Name.

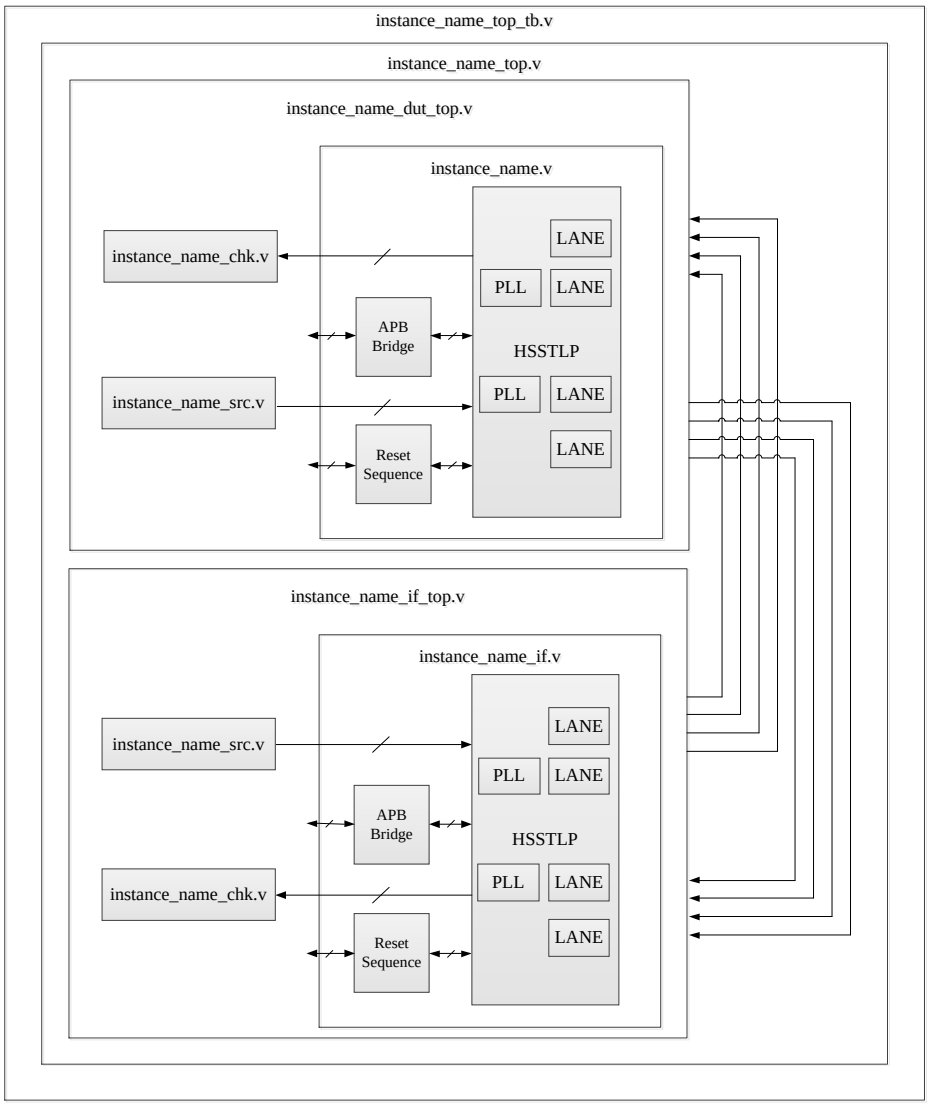

Figure 2-14 HSST IP Example Design Block Diagram

2.4.2 Module Description

2.4.2.1 Instance_name.v Module

The top-level .v file generated according to user configuration values in the IP interface includes the APB Bridge and reset sequence modules.

2.4.2.2 Instance_name_if.v Module

This module is a mirror module of instance_name.v with identical parameter configuration, with no further elaboration.

2.4.2.3 Instance_name_src.v Module

A stimulus generation module adapts to different bit widths or encoding modes.

2.4.2.3.1 Bypassed Mode

When TX Encoder and RX Decoder are set to Bypassed mode, different bit widths construct different 0/1 balanced loop Patterns.

- 8bit corresponding loop Pattern: i_txd_{0..3} is 8'b01_000_111;
- 10bit corresponding loop Pattern: i_txd_{0..3} is 10'b01_0000_1111;
- 16bit corresponding loop Pattern: i_txd_{0..3} is {2{8'b0001_0111}};
- 20bit corresponding loop Pattern: i_txd_{0..3} is {2{10'b00001_01111}};
- 32bit corresponding loop Pattern: i_txd_{0..3} is {4{8'b0101_0011}};
- 40bit corresponding loop Pattern: i_txd_{0..3} is {4{10'b00101_00111}}.

2.4.2.3.2 8B10B Mode

When TX Encoder and RX Decoder are set to 8B10B mode, the pre-encoded data i_txd_{0..3} is in a 32bytes format, which is transmitted in a loop, with specific data format as shown in Table 2-9.

Table 2-9 Data Format when 8B10B is Enabled

Byte Location	Byte Content	Content Description
byte0~3	a0_a1_a2_a3	When Channel Bonding enable is valid, a0 = CHx_RXPCS_A_REG; otherwise, a0 = i0; a_{1..3}=i_{1..3};
byte4~7 byte8~11 byte12~15 byte16~19 byte20~23	i0_i1_i2_i3	i0= CHx_RXPCS_COMMA_REG0; i1=D5.6 i2=i0 i3=i1

Byte Location	Byte Content	Content Description
byte24~27	s0_s1_s2_s3	s0= CHx_RXPCS_SKIP_REG0 s1= "GE" ? CHx_RXPCS_SKIP_REG1: "XAUI"? CHx_RXPCS_SKIP_REG0: "PCIE_2BYTE"? CHx_RXPCS_SKIP_REG1: "PCIE_4BYTE"? CHx_RXPCS_SKIP_REG1: "CUSTOMERIZED_1BYTE"? CHx_RXPCS_SKIP_REG0: "CUSTOMERIZED_2BYTE"? CHx_RXPCS_SKIP_REG1: "CUSTOMERIZED_4BYTE"?CHx_RXPCS_SKIP_REG1: D5.6 s2= "GE" ? CHx_RXPCS_SKIP_REG0: "XAUI"? CHx_RXPCS_SKIP_REG0: "PCIE_2BYTE"? CHx_RXPCS_SKIP_REG0: "PCIE_4BYTE"? CHx_RXPCS_SKIP_REG2: "CUSTOMERIZED_1BYTE"? CHx_RXPCS_SKIP_REG0: "CUSTOMERIZED_2BYTE"? CHx_RXPCS_SKIP_REG0: "CUSTOMERIZED_4BYTE"? CHx_RXPCS_SKIP_REG2: K28_5 s3= "GE" ? CHx_RXPCS_SKIP_REG1: "XAUI"? CHx_RXPCS_SKIP_REG0: "PCIE_2BYTE"? CHx_RXPCS_SKIP_REG1: "PCIE_4BYTE"? CHx_RXPCS_SKIP_REG3: "CUSTOMERIZED_1BYTE"? CHx_RXPCS_SKIP_REG0: "CUSTOMERIZED_2BYTE"? CHx_RXPCS_SKIP_REG1: "CUSTOMERIZED_4BYTE"? CHx_RXPCS_SKIP_REG3: D5.6 Note: The judgement value for the conditional statement comes from CTC Mode (refer to Table 2-4).
byte28~31	p0_p1_p2_p3	Payload bytes, with an initial value of 1, left shift operation.

2.4.2.3.3 64B66B_transparent Mode

When TX Encoder and RX Decoder are set to 64B66B_transparent mode, the looped transmission Pattern is as shown in Table 2-10.

Table 2-10 Transmission Pattern for 64B66B_transparent Mode

Bit width	i_txh_{0..3}	i_txd_{0..3}
16bit	{2'b01}	{2{8'b1010_1010}}
32bit	{2'b01}	{4{8'b1010_1010}}

2.4.2.3.4 64B67B_transparent Mode

When TX Encoder and RX Decoder are set to 64B67B_transparent mode, the looped transmission Pattern is as shown in Table 2-11.

Table 2-11 Transmission Pattern for 64B67B_transparent Mode

Bit width	**i_txh_{0..3}**	**i_txd_{0..3}**
16bit	{3'b100}	{2{8'b1010_1010}}
32bit	{3'b100}	{4{8'b1010_1010}}

2.4.2.4 Instance_name_chk.v Module

Test whether detection mechanism module adapts to different bit widths or encoding modes.

2.4.2.4.1 Bypassed Mode

When TX Encoder and RX Decoder are set to Bypassed mode, detection is performed according to the transmission Pattern format, with real-time reporting of o_pl_err[3:0].

2.4.2.4.2 8B10B mode and Channel Bonding Disabled

When TX Encoder and RX Decoder are set to 8B10B mode, and Channel Bonding is disabled; first locate the Payload byte boundary, then determine if the Payload bytes are as expected, with real-time reporting of o_pl_err[3:0].

2.4.2.4.3 8B10B mode and Channel Bonding Enabled

When the TX Encoder and RX Decoder are set to the 8B10B mode, and Channel Bonding is enabled; bit-level comparison is made between Lanes with Channel Bonding enabled while detecting Payload bytes, to ensure data alignment between the Lanes is successful, with real-time reporting of o_pl_err[3:0].

2.4.2.4.4 64B66B_transparent Mode

When the TX Encoder and RX Decoder are set to 64B66B_transparent mode, upon receiving the first rxh_start signal, rxh_{0..3} and rxd_{0..3} of the same instant are concatenated into a 66bit data, then the number of bits to be shifted is determined based on the ideal pattern {2'b 01,4{8'b1010_1010}} and shifted accordingly; after the shifting operation is completed, it checks at

every moment when rxh_vld_{0..3} is 1, whether rxh_{0..3} is 2'b01 and whether rxd_{0..3} is 2{8'b1010_1010} or 4{8'b1010_1010}, with real-time reporting of o_pl_err[3:0].

2.4.2.4.5 64B67B_transparent Mode

When the TX Encoder and RX Decoder are set to 64B67B_transparent mode, after receiving the first rxh_start signal, rxh_{0..3} and rxd_{0..3} of the same instant are concatenated into a 67bit data, and the number of bits to be shifted is determined based on the ideal pattern {3'b100,4{8'b1010_1010}} before performing the shift; upon completing the shift operation, it detects at each moment when rxh_vld_{0..3} is 1, whether rxh_{0..3} is 3'b100 and whether rxd_{0..3} is 2{8'b1010_1010} or 4{8'b1010_1010}, with real-time reporting of o_pl_err[3:0].

2.4.2.5 Instance_name_dut_top.v Module

DUT reference design module is added with stimulus generation and error detection module on the basis of the IP-generated instance_name.v.

2.4.2.6 Instance_name_if_top.v Module

This module is a mirror module of instance_name_dut_top, with identical parameter configuration, with no further elaboration.

2.4.2.7 Instance_name_top.v Module

Dock mode top-level module, which instantiates instance_name_dut_top.v and instance_name_if_top.v to connect the data differential ports; and provides the reference clocks i_p_refckp_{0..1} and i_free_clk required for simulation to implement the TX/RX power-up process.

2.4.2.8 Instance_name_top_tb.v Module

Docks mode Testbench module, including functions such as simulation acceleration, simulation duration setting, and test result determination.

2.4.3 Instance Configuration

The Example Design parameter configuration is auto-generated based on the configuration of the IP interface and does not require additional configuration.

2.4.4 Instance Simulation

On the Windows system, after the IP is generated, double-click the *.bat file under <project_path>/sim/modelsim (please refer to "2.3.1.3 Generating IP")] to run the simulation.

2.5 IP Interface Description

2.5.1 Common Interface Explanation

2.5.1.1 Clock Domain Explanation

- The clocks for o_p_pll_lock_{0..1}, o_p_rx_sigdet_sta_{0..3}, o_p_lx_cdr_align_{0..3}, o_p_pcs_lsm_synced_{0..3}, o_p_pcs_rx_mcb_status_{0..3} are generated internally and without output, thus are treated as asynchronous signals;
- Master channel explanation: when four channels are in the Channel Bonding mode, Channel0 is the master channel; when two channels are in the Channel Bonding mode, Channel0 is the master channel when Channel0 and Channel1 are bonding; Channel2 is the master channel when Channel2 and Channel3 are Bonding;
- When CTC is enabled, rxclk is the o_p_clk2core_tx of the TX end of this channel. With Channel Bonding enabled, rxclk is the o_p_clk2core_rx or o_p_clk2core_tx of the master channel (when CTC is enabled, it is o_p_clk2core_tx). Otherwise, rxclk is o_p_clk2core_rx of this channel;
- When Channel Bonding is enabled, txclk is the i_p_tx_clk_fr_core of the master channel; when Channel Bonding is disabled, txclk is the i_p_tx_clk_fr_core of this channel.

2.5.1.2 Common interface list

Table 2-12 Common Interface List[14]

Interface Name	Clock Domain	Input/Output	Description
Reset Sequence Interface[15]			
i_free_clk	clock	Input	The clock for the reset sequence logic ranges from 10 to 100MHz.
i_pll_rst_{0..1}	async	Input	Reset PLL and the driven TX/RX channels, active high.
o_pll_done_{0..1}	i_free_clk	Output	PLL reset completion indicator, active high. 0: Indicates during reset or the PLL has not achieved LOCK; 1: PLL has achieved LOCK.
o_txlane_done_{0..3}	i_free_clk	Output	TX side reset completion indicator, active high, can be used as the reset signal for the user logic, whereas in bonding scenarios only the master channel indicator is required.
o_tx_ckdiv_done_{0..3}	i_free_clk	Output	TX side rate change completion indicator, active high, whereas in bonding scenarios only the indicator of the master channel is required.
o_rxlane_done_{0..3}	i_free_clk	Output	RX side reset completion indicator, active high, can be used as the reset signal for the user logic, whereas in bonding scenarios only the master channel indicator is required.
o_rx_ckdiv_done_{0..3}	i_free_clk	Output	RX side rate change completion indicator, active high, whereas in bonding scenarios only the indicator of the master channel is required.
HSSTLP power and reset interfaces (valid when not using a reset sequence, replaced by reset sequence functionality when in use)			
i_p_lane_pd_{0..3}	async	Input	Corresponds to the P_LANE_PD interface.

14 This list only describes common interfaces. For other interfaces, please refer to "2.3.1.2 Configure IP Parameters", "2.3.1.4 Paramater Description", "2.5.2 Optional Interface Description"; HSSTLP IP interfaces are named as follows:

i_* denotes an input interface, o_* denotes an output interface;

In naming, {0..3} corresponds to four designations 0 to 3; unless specified, these correspond to Channel 0~3, and subsequent parameter naming follows the same rule.

15 Unified constraints for the reset sequence interfaces: all output signals are in the i_free_clk clock domain; unless specially stated, input signals will be internally synchronised in the i_free_clk clock domain by the reset sequence logic, and users must ensure the latching of the input. The same constraints to optional reset sequence interfaces in appendix.

Interface Name	Clock Domain	Input/Output	Description
i_p_pllpowerdown_{0..1}	async	Input	Corresponds to the P_PLLPOWERDOWN[16] interface.
i_p_tx_lane_pd_clkpath_{0..3}	async	Input	Corresponds to the P_TX_LANE_PD_CLKPATH interface.
i_p_tx_lane_pd_piso_{0..3}	async	Input	Corresponds to the P_TX_LANE_PD_PISO interface.
i_p_tx_lane_pd_driver_{0..3}	async	Input	Corresponds to the P_TX_LANE_PD_DRIVER interface.
i_p_rx_lane_pd_{0..3}	async	Input	Corresponds to the P_RX_LANE_PD interface.
i_p_lane_rst_{0..3}	async	Input	Corresponds to the P_LANE_RST interface.
i_p_pll_rst_{0..1}	async	Input	Corresponds to the P_PLL_RST interface.
i_p_tx_pma_rst_{0..3}	async	Input	Corresponds to the P_TX_PMA_RST interface.
i_p_pcs_tx_rst_{0..3}	async	Input	Corresponds to the P_PCS_TX_RST interface.
i_p_rx_pma_rst_{0..3}	async	Input	Corresponds to the P_RX_PMA_RST interface.
i_p_pcs_rx_rst_{0..3}	async	Input	Corresponds to the P_PCS_RX_RST interface.
APB interface			
i_p_cfg_clk	clock	Input	Corresponds to the P_CFG_CLK interface.
i_p_cfg_rst	i_p_cfg_clk	Input	Corresponds to the P_CFG_RST interface.
i_p_cfg_psel	i_p_cfg_clk	Input	Corresponds to the P_CFG_PSEL interface.
i_p_cfg_enable	i_p_cfg_clk	Input	Corresponds to the P_CFG_ENABLE interface.
i_p_cfg_write	i_p_cfg_clk	Input	Corresponds to the P_CFG_WRITE interface.
i_p_cfg_addr[15:0]	i_p_cfg_clk	Input	Dynamically configure the address bus of the interface, where the higher 4 bits serve as the chip select signal (for address space mapping, please refer to Table 2-2), and the lower 12 bits correspond to the P_CFG_ADDR[11:0] interface.
i_p_cfg_wdata[7:0]	i_p_cfg_clk	Input	Corresponds to the P_CFG_WDATA[7:0] interface.
o_p_cfg_rdata[7:0]	i_p_cfg_clk	Output	Corresponds to the P_CFG_RDATA[7:0] interface.
o_p_cfg_int	i_p_cfg_clk	Output	Corresponds to the P_CFG_INT interface.
o_p_cfg_ready	i_p_cfg_clk	Output	Corresponds to the P_CFG_READY interface.

16 P_* are HSSTLP interfaces, for details, please refer to the description in the "UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide", the same for below.

Interface Name	Clock Domain	Input/Output	Description
Clock Interface			
i_p_refckn_{0..1}	clock	Input	Corresponds to the REFCLK_CML_N interface.
i_p_refckp_{0..1}	clock	Input	Corresponds to the REFCLK_CML_P interface.
o_p_clk2core_tx_{0..3}	clock	Output	Corresponds to the P_TCLK2FABRIC interface.
i_p_tx{0..3}_clk_fr_core	clock	Input	Corresponds to the P_TX_CLK_FR_CORE interface.
o_p_clk2core_rx_{0..3}	clock	Output	Corresponds to the P_RCLK2FABRIC interface.
i_p_rx{0..3}_clk_fr_core	clock	Input	Corresponds to the P_RX_CLK_FR_CORE interface.
Status Interface			
o_p_pll_lock_{0..1}	async	Output	Corresponds to the P_PLL_READY interface.
o_p_rx_sigdet_sta_{0..3}	async	Output	Corresponds to the P_RX_SIGDET_STATUS interface.
o_p_lx_cdr_align_{0..3}	async	Output	Corresponds to the P_RX_READY interface.
o_p_pcs_lsm_synced_{0..3}	async	Output	Corresponds to the P_PCS_LSM_SYNCED interface.
o_p_pcs_rx_mcb_status_{0..3}	async	Output	Corresponds to the P_PCS_RX_MCB_STATUS interface.
Serdes-side Serial Differential Interface			
i_p_l{0..3}rxn[17]	async	Input	Corresponds to the P_RX_SDN interface.
i_p_l{0..3}rxp	async	Input	Corresponds to the P_RX_SDP interface.
o_p_l{0..3}txn	async	Output	Corresponds to the P_TX_SDN interface.
o_p_l{0..3}txp	async	Output	Corresponds to the P_TX_SDP interface.
User-side Interface			
i_txd_{0..3}[x-1:0]	txclk	Input	Data TXD interface, where the value of x is consistent with the parameter TX Fabric Data Width(Bits), i_p_tx{0..3}_clk_fr_core clock domain signal.

17 Denotes the HSSTLP serial differential input/output port, with different naming but consistent meaning;

Interface Name	Clock Domain	Input/Output	Description
i_tdispsel_{0..3}[x-1:0]	txclk	Input	Used for forcing the 8b10b polarity and the forced replacement from I2 to I1.
i_tdispctrl_{0..3}[x-1:0]	txclk	Input	{ i_tdispctrl_{0..3}, i_tdispsel_{0..3}} are 2'b00: Normal Data Transmission 2'b01: In accordance with the IEEE 802.3 1000BASE-X Specification protocol, the first I1/I2 options at the end of frame , with automatic replacement from I2 to I1 under certain conditions; 2'b10: Forces the 8b10b encoding polarity to be negative; 2'b11: Forces the 8b10b encoding polarity to be positive; The interface is only valid when the TX Encoder parameter is configured as 8B10B; when TX Fabric Data Width(Bits) = 8, x = 1; when TX Fabric Data Width(Bits) = 16, x = 2, where the 0bit corresponds to i_txd_{0..3}[7:0], and the 1bit corresponds to i_txd_{0..3}[15:8]; when TX Fabric Data Width(Bits) = 32, x = 4, where the 0th bit corresponds to i_txd_{0..3}[7:0], the 1bit corresponds to i_txd_{0..3}[15:8], the 2bit corresponds to i_txd_{0..3}[23:16], the 3bit corresponds to i_txd_{0..3}[31:24].
i_txk_{0..3}[x-1:0]	txclk	Input	Controls the TXK interface, only valid when the TX Encoder parameter is configured as 8B10B, whose each bit corresponds to 8 bits i_txd_{0..3}. For correspondence, please refer to in i_tdispsel_{0..3}[x-1:0]; 1 indicates that TXD is the 8b10b Special Code-groups of the IEEE 802.3 1000BASE-X Specification; 0 indicates that TXD is the 8b10b Data Code-groups of the IEEE 802.3 1000BASE-X Specification.
i_txq_{0..3}[6:0]	txclk	Input	Controls the TXQ interface, only valid when the TX Encoder parameter is configured as 64B66B_transparent or 64B67B_transparent; Indicates the user-side Sequence counter input; Wherein, [5:0] is used for 64B66B_transparent and [6:0] for 64B67B_transparent.

Interface Name	Clock Domain	Input/Output	Description
i_txh_{0..3}[2:0]	txclk	Input	Controls the TXH interface, only valid when the TX Encoder parameter is configured as 64B66B_transparent or 64B67B_transparent; Indicates synchronization word input: Wherein, [1:0] is used for 64B66B_transparent and [2:0] for 64B67B_transparent.
o_rxstatus_{0..3}[2:0]	rxclk	Output	Used for the receiving status encoding of PCI Express PHY Interface (PIPE): 3'b000: Normal termination of data; 3'b001: CTC module performed "SKIP add" operation; 3'b010: CTC module performed "SKIP delete" operation; 3'b011: PCIe 4-byte mode, continuous deletion; 3'b100: Bridge Over Flow; 3'b101: CTC FIFO Over Flow; 3'b110: CTC FIFO Under Flow; 3'b111: Bridge Under Flow.
o_rxd_{0..3}[x-1:0]	rxclk	Output	Data interface RXD interface, where the value of x is consistent with the parameter RX Fabric Data Width(Bits), i_p_rx{0..3}_clk_fr_core clock domain signal.
o_rdisper_{0..3}[x-1:0]	rxclk	Output	RDISP_ER interface, only valid when RX Encoder parameter is configured as 8B10B, whose bits correspond to 8bits i_rxd_{0..3}. For correspondence, please refer to i_tdispsel_{0..3}[x-1:0]. High injection indicates the 8b10b Decoder has detected Invalid Disparity.
o_rdecer_{0..3}[x-1:0]	rxclk	Output	RDEC_ER interface, only valid when RX Encoder parameter is configured as 8B10B, whose each bits correspond to 8bits i_rxd_{0..3}. For correspondence, please refer to i_tdispsel_{0..3}[x-1:0]. High injection indicates the 8b10b Decoder has detected Invalid Code.
o_rxk_{0..3}[x-1:0]	rxclk	Output	RXK interface, only valid when RX Encoder parameter is configured as 8B10B, whose each bit corresponds to 8bits i_rxd_{0..3}. For correspondence, please refer to i_tdispsel_{0..3}[x-1:0], 1 indicates that RXD is the 8b10b Special Code-Groups of the IEEE 802.3 1000BASE-X Specification; "0" indicates that RXD is the 8b10b Data Code-groups of the IEEE 802.3 1000BASE-X Specification.

Interface Name	Clock Domain	Input/Output	Description
o_rxd_vld_{0..3}	rxclk	Output	RXD_VLD interface, only valid when RX Decoder parameter is configured as 64B66B_transparent or 64B67B_transparent, whose each bit corresponds to 16bit or 32bit i_rxd_{0..3}, 1 indicates the RXD data is valid; "0" indicates the RXD data is invalid.
o_rxh_{0..3}[2:0]	rxclk	Output	RXH interface, only valid when RX Decoder parameter is configured 64B66B_transparent or 64B67B_transparent, whose each bit corresponds to 16bit or 32bit i_rxd_{0..3}, Indicates synchronization word output: wherein, [1:0] corresponds to 64B66B_transparent and [2:0] to 64B67B_transparent.
o_rxh_vld_{0..3}	rxclk	Output	RXH_VLD interface, only valid when RX Decoder parameter is configured as 64B66B_transparent, 64B67B_transparent, whose each bit corresponds to 3bit o_rxh_{0..3}, 1 indicates the RXH data is valid; 0 indicates the RXH data is invalid.
o_rxq_start_{0..3}	rxclk	Output	RXQ_START interface, only valid when RX Decoder parameter is configured as 64B66B_transparent or 64B67B_transparent. 1 indicates the moment when the Sequence counter corresponding to RXD data is 0; 0 indicates the moment when the Sequence counter corresponding to RXD data is not 0.

2.5.2 Optional Interface Description

On the IP Misc page, there is also a check box to select the optional interfaces for HSSTLP and reset sequences. For details, please refer to the table below.

Table 2-13 Misc Page Optional Interface Configuration Parameters Explanation

Parameter/Configuration Options	Parameter Description	Clock Domain
HSST Optional Interface (HSST Optional Pins)		
P_REFCK2CORE{0..1}	Select whether to enable o_p_refck2core_{0..1}(P_REFCK2CORE_{0..1}) interface.	clock
TX{0..3}_CLK2_FR_CORE	Select whether to enable i_tx{0..3}_clk2_fr_core(P_TCLK2_FR_CORE)_{0..3} interface.	clock

Parameter/Configuration Options	Parameter Description	Clock Domain
TX{0..3} External PLL Ready	Select whether to enable i_pll_lock_tx{0..3} interface.	async
TX{0..3} Swing Control	Select whether to enable i_p_lx_swing_ctl_0_{0..3}(P_TX_SWING_{0..3}) interface. When i_p_lx_swing_ctl_0_{0..3} is congfigured as: 1: Indicates the swing value is half of the value selected by the i_p_lx_margin_ctl_{0..3}[2:0] port; 0: Indicates the swing value is the value selected by the i_p_lx_margin_ctl_{0..3}[2:0] port. Select whether to enable i_p_lx_margin_ctl_{0..3}[2:0](P_TX_MARGIN_{0..3}[2:0]) interface. When i_p_lx_margin_ctl_{0..3}[2:0] is configured as: x00: The swing value corresponds to the parameter PMA_CH_REG_TX_AMP_DAC0; x01: The swing value corresponds to the parameter PMA_CH_REG_TX_AMP_DAC1; x01: The swing value corresponds to the parameter PMA_CH_REG_TX_AMP_DAC2; x01: The swing value corresponds to the parameter PMA_CH_REG_TX_AMP_DAC3.	async
TX{0..3} ELECIDLE Enable	Select whether to enable the ELECIDLE interface i_p_lx_elecidle_en_{0..3}[1:0] (P_TDATA_{0..3}[45:44])	async
TX{0..3}Beacon Enable	Select whether to enable the Beacon interface i_p_tx_beacon_en_{0..3} (P_TX_BEACON_EN_{0..3})	async
TX{0..3} Rate Channel Select	Select whether to enable the HSSTLP TX rate switch interface: i_p_tx_ckdiv_{0..3}[1:0](P_TX_RATE_{0..3}) The following ports correspond to PLL{0..1}, for details, please refer to ***"UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide"*** i_p_lane_sync_{0..1}(P_LANE_SYNC_{0..1}) i_p_rate_change_tclk_on_{0..1}(P_RATE_CHANGE_TCLK_ON_{0..1}) Not selectable when the reset sequence is enabled.	async
RX{0..3} Rate Channel Select	Select whether to enable the HSSTLP RX rate switch interface: i_p_lx_rx_ckdiv_{0..3}[1:0](P_RX_RATE_{0..1}) Not selectable when the reset sequence is enabled.	async
TX{0..3} ELECIDLE Enable	Select whether to enable the ELECIDLE interface: i_p_lx_elecidle_en_{0..3}[1:0] (P_TDATA_{0..3}[45:44]).	async

Parameter/Configuration Options	Parameter Description	Clock Domain
RX{0..3}_CLK2_FR_CORE	Select whether to enable the i_rx{0..3}_clk2_fr_core(P_RCLK2_FR_CORE)_{0..3} interface.	clock
RX{0..3} External PLL Ready	Select whether to enable i_pll_lock_rx_{0..3} interface.	async
RX{0..3}_Hi-z Control	Select whether to enable the i_p_rx_highz_{0..3}(P_RX_HIGHZ_{0..3}) interface.	async
RX{0..3} OOB Status	Select whether to enable the o_p_lx_oob_sta_{0..3}(P_LX_OOB_STA_{0..3}) interface.	async
RX{0..3} Detection	Select whether to enable the Receiver Detect interface: i_p_lx_rxdct_en_{0..3}(P_TX_RXDET_REQ_{0..3}) o_p_lx_rxdct_out_{0..3}(P_TX_RXDET_STATUS_{0..3}).	async
RX{0..3}_CLK_SLIP	Select whether to enable the i_p_pcs_word_align_en_{0..3}(P_PCS_WORD_ALIGN_EN[3:0]) interface.	async
RX{0..3} Polarity Invert	Select whether to enable the i_p_rx_polarity_invert_{0..3}(P_RX_POLARITY_INVERT_{0..3}) interface;	async
CH{0..3} Debug Bus	Select whether to enable control interfaces for 5 types of loopback modes, respectively: The i_p_pcs_nearend_loop_{0..3}(P_PCS_NEAREND_LOOP_{0..3}) interface; The i_p_pcs_farend_loop_{0..3}(P_PCS_FAREND_LOOP_{0..3}) interface; The i_p_pma_nearend_ploop_{0..3}(P_PMA_NEAREND_PLOOP_{0..3}) interface; The i_p_pma_nearend_sloop_{0..3}(P_PMA_NEAREND_SLOOP)_{0..3} interface; The i_p_pma_farend_ploop_{0..3}(P_PMA_FAREND_PLOOP_{0..3}) interface; For specific configuration methods, please refer to "***UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide***";	async
Reset Sequence Optional Interfaces (Reset Sequence Optional Pins)		
PLL{0..1} Reset	Indicates whether to enable the i_pll_rst_{0..1} interface, for display only, not selectable by the user; The i_pll_rst_{0..1} is the reset interface for PLL_{0..1} in the reset sequence, active high.	async

Parameter/Configuration Options	Parameter Description	Clock Domain
PLL{0..1} WatchDag Clear	Indicates whether to enable the i_wtchdg_clr_{0..1} interface, for display only, not selectable by the user; The i_wtchdg_clr_{0..1} is the internal watchdog clear signal for the reset sequence, active high, used to reset the internal watchdog alarm counter, for debugging only.	async
PLL{0..1} Status	Indicates whether to enable the o_wtchdg_st_{0..1}[1:0] and o_pll_done_{0..1} interfaces; The o_wtchdg_st_{0..1}[1:0] is the watchdog status indicator for the reset sequence, for debugging only: 2'b00: Watchdog wait state; 2'b10: Watchdog alarm state; 2'b01: Watchdog count state; The o_pll_done_{0..1} signifies the intermediate completion state for the reset sequence, active high[18], for debugging only.	i_free_clk
RX{0..3} Reset	Select whether to enable the i_rxlane_rst_{0..3} interface; The i_rxlane_rst_{0..3} is the RX-side reset signal for the reset sequence, active high; When CTC Mode (refer to parameter description) is not Bypassed, control is unified by i_txlane_rst_{0..3}; When Channels 0~3 are in single lane mode, i_rxlane_rst_{0..3} independently controls Channels 0~3; When Channels 0~3 are in quad-lane mode, i_rxlane_rst_0 controls Channel 0~3; When Channel 0~1 are in dual lane mode, i_rxlane_rst_0 controls Channel 0~1; When Channel 2~3 are in dual lane mode, i_rxlane_rst_2 controls Channel 2~3.	async
RX{0..3} Rate Change Select	Select whether to enable the i_rx_rate_chng_{0..3} and i_rxckdiv_{0..3}[1:0] interfaces of the reset sequence; i_rx_rate_chng_{0..3} enables the reset sequence rate switch, valid on the rising edge; switching can only be initiated by the next rising edge when o_tx_ckdiv_done_{0..3} is pulled high after a speed change, i_free_clk clock domain signal; When the CTC Mode (refer to parameter description) is not Bypassed, the TX/RX rate switching is uniformly controlled by i_tx_rate_chng_{0..3}; When Channels 0~3 are in single lane mode, i_rx_rate_chng_{0..3} independently controls Channels 0~3;	async

18 High pulse: A high level is maintained for one clock cycle, at all other times it is low, same below.

Parameter/Configuration Options	Parameter Description	Clock Domain
	When Channels 0~3 are in quad-lane mode, i_rx_rate_chng_0 controls Channels 0~3; When Channels 0~1 are in dual lane mode, i_rx_rate_chng_0 controls Channels 0~1; When Channels 2~3 are in dual lane mode, i_rx_rate_chng_2 controls Channels 2~3; When Channels 0~3 consist of multiple single lanes or a mix of dual and single lanes, the RX side can switch rates only after all corresponding working Channel o_rxlane_done_{0..3} is configured as 1; i_rxckdiv_{0..3}[1:0] has the same meaning as P_RX_RATE[1:0], needing to remain stable before the rising edge of i_rx_rate_chng_{0..3} arrives, i_free_clk clock domain signal.	
RX{0..3} Debug Bus	Select whether to enable the i_hsst_fifo_clr_{0..3} and i_loop_dbg_{0..3}[2:0] and i_pcs_cb_rst_{0..3} interfaces; i_hsst_fifo_clr_{0..3} is only valid in dual lane mode or quad lane mode and when the Channel Bonding mode (refer to parameter description) is Bypassed; it can input a high pulse to control and clear the internal FIFO of HSSTLP RX PCS after o_txlane_done_{0..3} is set; In the dual Lane or quad lane mode and when Channel Bonding mode (refer to parameter description) is not Bypassed, i_hsst_fifo_clr_{0..3} is taken over by reset sequence internal signal fifo_clr_en_{0..3}; When the reset sequence is enabled, i_loop_dbg_{0..3}[2:0] is used for loopback configuration and must be used in conjunction with the loopback mode guidance methods defined in the "***UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide***".Among them, A value of 1 for i_loop_dbg_{0..3}[0] enforces the IP reset sequence to treat sigdet as high, but does not affect the normal sigdet state indication; typically used in (but not limited to) near-end parallel loopback and burst-mode data reception scenarios; A value of 1 for i_loop_dbg_{0..3}[1] enforces the IP reset sequence to treat cdr align as high, but does not affect the normal cdr align state indication; typically used in (but not limited to) near-end parallel loopback and burst-mode data reception scenarios; A value of 1 for i_loop_dbg_{0..3}[2] enforces the IP reset sequence to treat word align as high, but does not affect the normal word align state indication; typically used in (but not limited to) scenarios such as enabling word align but with test data reception that does not include a synchronization header; Non-loopback mode: configured as 3'b000	async

Parameter/Configuration Options	Parameter Description	Clock Domain
	(default); PMA far-end parallel loopback: configured as 3'b000; PMA near-end parallel loopback: configured as 3'b011; PMA near-end serial loopback: configured as 3'b000; PCS far-end parallel loopback: configured as 3'b000; PCS near-end parallel loopback: configured as 3'b011; User logic loopback mode: configured as 3'b111; i_pcs_cb_rst_{0..3} can be used to reset the Channel Bonding module and the modules followed, active high.	
TX{0..3} Reset	Select whether to enable the i_txlane_rst_{0..3} interface; i_txlane_rst_{0..3} is a reset signal for the TX side of the reset sequence, active high; When Channels 0~3 are in single Lane mode, i_txlane_rst_{0..3} independently controls Channels 0~3; When Channels 0~3 are in quad-lane mode, i_txlane_rst_0 controls Channel 0~3; When Channel 0~1 are in dual lane mode, i_txlane_rst_0 controls Channel 0~1; When Channels 2~3 are in dual lane mode, i_txlane_rstn_2 controls Channels 2~3; When a channel shares a PLL with a channel in dual lane mode, a simultaneous reset operation must be carried out.	async
TX{0..3} Rate Change Select	Choose whether to enable the reset sequence i_tx_rate_chng_{0..3} and i_txckdiv_{0..3}[1:0] interfaces; When i_tx_rate_chng_{0..3} rate switching is enabled, valid on the rising edge; when the o_rx_ckdiv_done_{0..3} pulls high after rate switching initiation, it can respond to the next rising edge to start rate switching, i_free_clk clock domain signal; When Channels 0~3 are in single Lane mode, i_tx_rate_chng_{0..3} independently controls Channels 0~3; When Channels 0~3 are in quad-Lane mode, i_tx_rate_chng_0 controls Channels 0~3; When Channels 0~1 are in dual Lane mode, i_tx_rate_chng_0 controls Channels 0~1; When Channels 2~3 are in dual Lane mode, i_tx_rate_chng_2 controls Channels 2~3; i_txckdiv_{0..3}[1:0] has the same meaning as P_TX_RATE [1:0], and needs to remain stable before the rising edge of i_tx_rate_chng_{0..3} arrives, i_free_clk clock domain signal; Lanes from the same PLL must switch rates at the same moment; When more than 2 lanes come from the same PLL and only one lane undergoes rate switching,	async

Parameter/Configuration Options	Parameter Description	Clock Domain
	perform a masking operation on the lane not switching rates through the APB interface. For details, please refer to *"**UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide**"*.	

2.6 IP Register Description

This section describes the HSSTLP IP register explanations and access methods.

2.6.1 Register Description

For HSST register explanations, please refer to "***UG040008_Logos2 Family FPGAs High Speed Serial Transceiver (HSSTLP) User Guide***".

2.6.2 Register Access

Users can access the configuration registers for all LANES and PLLs via the APB bus interface, please refer to "2.2.2 APB Bridge".

2.7 Typical Applications

For typical applications of HSSTLP IP, please refer to "2.4 Example Design".

2.8 Descriptions and Considerations

2.8.1 RXPCS Align Timer Calculation Method

$$PCS\_RCLK = \frac{LINE\_RATE\ Gbps * 10^3}{INNER\_WIDTH}\ MHz$$

$$TIME0 = \left(JUMBO\_FRAME\_LEN * JUMBO\_FRAME\_NUM * 8) * \frac{1}{PCS\_RCLK}\right) \Big/ INNER\_WIDTH$$

$$TIME1 = \frac{1}{FREE\_CLK}$$

$$RXPCS\ Align\ Timer = \frac{TIME0}{TIME1} = \left(JUMBO\_FRAME\_LEN * JUMBO\_FRAME\_NUM * 8) * \frac{1}{PCS\_RCLK}\right) \Big/ INNER\_WIDTH \Big/ \frac{1}{FREE\_CLK}$$

$$= \frac{(JUMBO\_FRAME\_LEN * JUMBO\_FRAME\_NUM * 8) * \frac{1}{LINE\_RATE\ Gbps * 10^3} \Big/ INNER\_WIDTH}{INNER\_WIDTH} \Big/ \frac{1}{FREE\_CLK}$$

$$= \frac{JUMBO\_FRAME\_LEN * JUMBO\_FRAME\_NUM * 8 * FREE\_CLK}{LINE\_RATE * 10^3}$$

Where:

JUMBO_FRAME_LEN represents the length of a jumbo frame, in bytes.

JUMBO_FRAME_NUM represents the number of jumbo frames.

LINE_RATE is the line rate, measured in Gbps.

FREE_CLK is a free clock, ranging from 10~100MHz.

INNER_WIDTH represents the PCS internal data width of the HSST.

PCS_CLK represents the PCS internal working clock of the HSST.

2.8.2 Clock Constraints

In application, the PDS software automatically constrains the HSSTLP output clocks o_p_clk2core_tx_{0..3} and o_p_clk2core_rx_{0..3} to the regional clock or the global clock. It is necessary to ensure that the clock paths of o_p_clk2core_tx_{0..3} and o_p_clk2core_rx_{0..3} meet the design intentions after PDS routing. Clock attributes can be constrained through the PDS

software or by editing the clock attributes in the .fdc file. Taking the use case in this document as an example, the method of editing constraints in the .fdc file is as follows.

Constrain the clock o_p_clk2core_tx_{0..3} to the global clock:

```
define_attribute {t:U_INST.o_p_clk2core_tx_0} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}
define_attribute {t:U_INST.o_p_clk2core_tx_1} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}
define_attribute {t:U_INST.o_p_clk2core_tx_2} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}
define_attribute {t:U_INST.o_p_clk2core_tx_3} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFG}
```

Constrain the clock o_p_clk2core_tx_{0..3} to the regional clock:

```
define_attribute {t:U_INST.o_p_clk2core_tx_0} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFR}
define_attribute {t:U_INST.o_p_clk2core_tx_1} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFR}
define_attribute {t:U_INST.o_p_clk2core_tx_2} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFR}
define_attribute {t:U_INST.o_p_clk2core_tx_3} {PAP_CLOCK_ASSIGN} {GTP_CLKBUFR}
```

2.8.3 Physical Location Constraints

In applications, users need to apply physical location constraints to the differential clock input pins of the LANE, PLL, and PLL of the HSSTLP in the .fdc file through PDS based on the Single Board used. The physical location can be constrained using PDS software or by editing the physical location in the .fdc file. Taking the use case in this document as an example, the method of editing constraints in the .fdc file is as follows.

Attention:

When applying physical location constraints to the differential clock input pins of the PLL:

PG2L50H, PG2L25H: The software version must be 2022.1 or above.

PG2L100H: The software version must be 2021.1-SP7.2, 2021.4-SP1, 2022.1 or above.

PG2L200H: The software version must be 2022.2 or above.

PG2L100HX: For software versions, please contact FAE.

Constrain them to LANE0 of HSSTLP:

```
define_attribute {i:U_INST.U_GTP_HSSTLP_WRAPPER.CHANNEL0_ENABLE.U_GTP_HSSTLP_LANE0} {PAP_LOC} {HSSTLP_364_918:U0_HSSTLP_LANE}
```

Constrain them to PLL0 of HSSTLP:

```
define_attribute {i:U_INST.U_GTP_HSSTLP_WRAPPER.PLL0_ENABLE.U_GTP_HSSTLP_PLL0} {PAP_LOC} {HSSTLP_364_918:U0_HSSTLP_PLL}
```

Constrain the differential clock input pins of PLL0 and PLL1 to the CLK0 and CLK1 differential input pins:

```
define_attribute {p:i_p_refckn_0} {PAP_IO_DIRECTION} {INPUT}
define_attribute {p:i_p_refckn_0} {PAP_IO_LOC} {E13}
define_attribute {p:i_p_refckn_0} {PAP_IO_VCCIO} {3.3}
define_attribute {p:i_p_refckn_0} {PAP_IO_STANDARD} {LVCMOS33}
define_attribute {p:i_p_refckn_0} {PAP_IO_UNUSED} {TRUE}
define_attribute {p:i_p_refckp_0} {PAP_IO_DIRECTION} {INPUT}
define_attribute {p:i_p_refckp_0} {PAP_IO_LOC} {F13}
define_attribute {p:i_p_refckp_0} {PAP_IO_VCCIO} {3.3}
define_attribute {p:i_p_refckp_0} {PAP_IO_STANDARD} {LVCMOS33}
define_attribute {p:i_p_refckp_0} {PAP_IO_UNUSED} {TRUE}
define_attribute {p:i_p_refckn_1} {PAP_IO_DIRECTION} {INPUT}
define_attribute {p:i_p_refckn_1} {PAP_IO_LOC} {E11}
define_attribute {p:i_p_refckn_1} {PAP_IO_VCCIO} {3.3}
define_attribute {p:i_p_refckn_1} {PAP_IO_STANDARD} {LVCMOS33}
define_attribute {p:i_p_refckn_1} {PAP_IO_UNUSED} {TRUE}
define_attribute {p:i_p_refckp_1} {PAP_IO_DIRECTION} {INPUT}
define_attribute {p:i_p_refckp_1} {PAP_IO_LOC} {F11}
define_attribute {p:i_p_refckp_1} {PAP_IO_VCCIO} {3.3}
define_attribute {p:i_p_refckp_1} {PAP_IO_STANDARD} {LVCMOS33}
define_attribute {p:i_p_refckp_1} {PAP_IO_UNUSED} {TRUE}
```

2.8.4 Application Restrictions

In applications, when the TX and RX ends of the channel use different PLLs to provide clocks:

- The PLL used by RX and the PLL used by TX must be reset simultaneously, and should not be reset individually;
- To achieve PLL lock at the TX end, it is necessary to detect the lock status of both PLLs. This means that both o_p_pll_lock_0 and o_p_pll_lock_1 signals should be active high.

In applications supporting the OOB function such as SATA, the Electric Idle state of the link during physical layer initialization may cause the HSST RX signal detection state to pull down. The reset sequence will re-reset the RX PMA. It is recommended to design an independent reset sequence in such applications.

2.9 IP Debugging Methods

For common issues encountered by users when instantiating IP, some troubleshooting methods are listed here.

2.9.1 PLL LOCK Failure

Generally, users complete the configuration of HSSTLP reference clock source by constraining the reference clock pins in the fdc file. Refer to "2.8.2 Clock Constraints" and "2.8.3 Physical Location Constraints" for details. When a PLL LOCK failure occurs, clock pin constraints need to be checked first, regardless of whether the reference clock is shared, to ensure consistency with actual application scenarios.

2.9.2 Loopback Mode Failure

Generally, users control the HSSTLP to enter loopback mode via ports, needing to check the CH{0..3}_Debug_bus and RX{0..3}_Debug_bus options on the IP interface. If there are issues with the loopback data stream transmission and reception, users must investigate whether the i_loop_dbg_{0..3} port assignment meets requirements, please refer to Table 2-13.

2.9.3 Word Align Failure

Generally, users enable the HSSTLP Word Align function. If Word Align is unsuccessful, first check whether the RX data stream contains any COMMA codes, then check whether the included COMMA codes match the COMMA codes configured on the IP interface, and finally check the Word Align mode configuration.

Herein, CUSTOMRIZED_MODE indicates HSSTLP only completes edge alignment and requires the Fabric side to implement the synchronous state machine, GE_MODE is applicable to GE protocol, RAPIDIO_MODE is applicable to RAPIDIO protocol, and other protocols are configured as XAUI_MODE, please refer to Table 2-4.

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