Logos2 Family FPGAs High-Speed Serial Transceiver (HSSTLP) User Guide

(UG040008, V1.9)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.9	20.12.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
HSSTLP	High Speed Serial Transceiver Low Performance
PCS	Physical Code Sublayer
PMA	Physical Media Attachment
SSC	Spread Spectrum Clock
XAUI	10 Gigabit Attachment Unit interface
CPRI	Common Public Radio Interface
SRIO	Serial Rapid IO
CTC	Clock Tolerance Compensation
PRBS	Pseudo-Random Binary Sequence
APB	Advanced Peripheral Bus
UI	Unit Internal
CDR	Clock Data Recovery
LEQ	Linear Equalizer

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Chapter 1 General Introduction to HSSTLP

The Logos2 Family products have built-in high-speed serial interface modules, i.e. HSSTLP. In addition to the PMA, HSSTLP also integrates a rich set of PCS functions, which can be flexibly applied to various serial protocol standards. Within the Logos2 Family products, each HSSTLP supports 1 to 4 full-duplex transmit and receive LANEs. The key features of HSSTLP include:

- Data Rate: refer to "DS04001_Logos2 Family FPGAs Device Datasheet"
- Flexible reference clock selection
- Transmit and receive channel data rates can be independently configured
- Programmable output swing and de-emphasis
- Adaptive equalizer at receiver side
- PMA RX supports SSC
- The data channels support 8bit only, 10bit only, 8B10B 8bit, 16bit only, 20bit only, 8B10B 16bit, 32bit only, 40bit only, 8B10B 32bit, 64B66B/64B67B 16bit, and 64B66B/64B67B 32bit modes
- The PCS is flexibly configurable and supports protocols such as PCI Express GEN1, PCI Express GEN2, XAUI, Gigabit Ethernet, CPRI, SRIO, etc.
- Flexible Word Alignment functions
- RX Clock Slip function to ensure a fixed receive latency
- Protocol standard 8B10B encoding/decoding
- Protocol standard 64B66B/64B67B data adaptation function
- Flexible CTC scheme
- Supports x2 and x4 Channel Bonding
- HSSTLP configuration supports dynamic modification
- Near-end loopback and far-end loopback
- Built-in PRBS Feature

PG2L25H and PG2L50H both contain 1 HSSTLP that supports up to 4 full-duplex transmit and receive LANEs; PG2L100H contains 2 HSSTLPs that support up to 8 full-duplex transmit and receive LANEs; PG2L200H contains 4 HSSTLPs, among which HSSTLP_L3 and HSSTLP_R3 are adjacent, and HSSTLP_L7 and HSSTLP_R7 are adjacent, supporting up to 16 full-duplex transmit and receive LANEs in total.

Each HSSTLP consists of two PLLs and four transmit and receive LANEs, and each LANE contains four components: PCS Transmitter, PMA Transmitter, PCS Receiver, and PMA Receiver. The PCS Transmitter and PMA Transmitter make up the transmit path, and the PCS Receiver and PMA Receiver make up the receive path. The structures of Logos2 Family HSSTLP modules are identical. Taking PG2L100H as an example, the structure diagram of HSSTLP is shown in Figure 1-1:

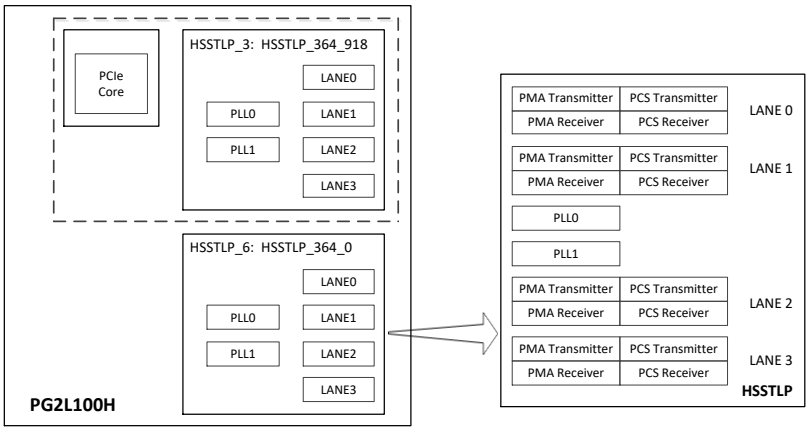

Figure 1-1 PG2L100H HSSTLP Structure Diagram

Table 1-1 lists the location constraints for each LANE and PLL in the Logos2 Family HSSTLP.

Table 1-1 HSSTLP Pin Location Constraints

Device Model/ Package	**Module Name**		**Constraint Location**	**Corresponding Pin TXP/TXN/RXP/RXN**
PG2L25H MBG325	HSSTLP_4	LANE0	HSSTLP_268_306:U0_HSSTLP_LANE	B2/B1/E4/E3
		LANE1	HSSTLP_268_306:U1_HSSTLP_LANE	D2/D1/C4/C3
		LANE2	HSSTLP_268_306:U2_HSSTLP_LANE	F2/F1/A4/A3
		LANE3	HSSTLP_268_306:U3_HSSTLP_LANE	H2/H1/G4/G3
		PLL0	HSSTLP_268_306:U0_HSSTLP_PLL	
		PLL1	HSSTLP_268_306:U1_HSSTLP_PLL	
PG2L50H FBG484	HSSTLP_3	LANE0	HSSTLP_292_612:U0_HSSTLP_LANE	D7/C7/D9/C9
		LANE1	HSSTLP_292_612:U1_HSSTLP_LANE	B6/A6/B10/A10
		LANE2	HSSTLP_292_612:U2_HSSTLP_LANE	D5/C5/D11/C11
		LANE3	HSSTLP_292_612:U3_HSSTLP_LANE	B4/A4/B8/A8
		PLL0	HSSTLP_292_612:U0_HSSTLP_PLL	
		PLL1	HSSTLP_292_612:U1_HSSTLP_PLL	
PG2L100H (X) FBG484	HSSTLP_3	LANE0	HSSTLP_364_918:U0_HSSTLP_LANE	C9/D9/C7/D7
		LANE1	HSSTLP_364_918:U1_HSSTLP_LANE	A10/B10/A6/B6/
		LANE2	HSSTLP_364_918:U2_HSSTLP_LANE	C11/D11/C5/D5
		LANE3	HSSTLP_364_918:U3_HSSTLP_LANE	A8/B8/A4/B4
		PLL0	HSSTLP_364_918:U0_HSSTLP_PLL	

Device Model/ Package	Module Name		Constraint Location	Corresponding Pin TXP/TXN/RXP/RXN
		PLL1	HSSTLP_364_918:U1_HSSTLP_PLL	
PG2L100H (X) FBG676	HSSTLP_3	LANE0	HSSTLP_364_918:U0_HSSTLP_LANE	D10/C10/D12/C12
		LANE1	HSSTLP_364_918:U1_HSSTLP_LANE	B9/A9/B13/A13
		LANE2	HSSTLP_364_918:U2_HSSTLP_LANE	D8/C8/D14/C14
		LANE3	HSSTLP_364_918:U3_HSSTLP_LANE	B7/A7/B11/A11
		PLL0	HSSTLP_364_918:U0_HSSTLP_PLL	
		PLL1	HSSTLP_364_918:U1_HSSTLP_PLL	
	HSSTLP_6	LANE0	HSSTLP_364_0:U0_HSSTLP_LANE	AE7/AF7/AE11/AF11
		LANE1	HSSTLP_364_0:U1_HSSTLP_LANE	AC8/AD8/AC14/AD14
		LANE2	HSSTLP_364_0:U2_HSSTLP_LANE	AE9/AF9/AE13/AF13
		LANE3	HSSTLP_364_0:U3_HSSTLP_LANE	AC10/AD10/AC12/AD12
		PLL0	HSSTLP_364_0:U0_HSSTLP_PLL	
		PLL1	HSSTLP_364_0:U1_HSSTLP_PLL	
PG2L200H FBB484	HSSTLP_L3	LANE0	HSSTLP_283_1224:U0_HSSTLP_LANE	A8/B8/A4/B4
		LANE1	HSSTLP_283_1224:U1_HSSTLP_LANE	C11/D11/C5/D5
		LANE2	HSSTLP_283_1224:U2_HSSTLP_LANE	A10/B10/A6/B6
		LANE3	HSSTLP_283_1224:U3_HSSTLP_LANE	C9/D9/C7D7
		PLL0	HSSTLP_283_1224:U0_HSSTLP_PLL	
		PLL1	HSSTLP_283_1224:U1_HSSTLP_PLL	
PG2L200H FBB676	HSSTLP_L3	LANE0	HSSTLP_283_1224:U0_HSSTLP_LANE	A11/B11/A7/B7
		LANE1	HSSTLP_283_1224:U1_HSSTLP_LANE	C14/D14/C8/D8
		LANE2	HSSTLP_283_1224:U2_HSSTLP_LANE	A13/B13/A9/B9
		LANE3	HSSTLP_283_1224:U3_HSSTLP_LANE	C12/D12/C10/D10
		PLL0	HSSTLP_283_1224:U0_HSSTLP_PLL	
		PLL1	HSSTLP_283_1224:U1_HSSTLP_PLL	
	HSSTLP_L7	LANE0	HSSTLP_283_0:U0_HSSTLP_LANE	AD12/AC12/AD10/AC10
		LANE1	HSSTLP_283_0:U1_HSSTLP_LANE	AF13/AE13/AF9/AE9
		LANE2	HSSTLP_283_0:U2_HSSTLP_LANE	AD14/AC14/AD8/AC8
		LANE3	HSSTLP_283_0:U3_HSSTLP_LANE	AF11/AE11/AF7/AE7
		PLL0	HSSTLP_283_0:U0_HSSTLP_PLL	
		PLL1	HSSTLP_283_0:U1_HSSTLP_PLL	

Device Model/ Package	Module Name		Constraint Location	Corresponding Pin TXP/TXN/RXP/RXN
PG2L200H FFBG1156	HSSTLP_L3	LANE0	HSSTLP_283_1224:U0_HSSTLP_LANE	B23/A23/F21/E21
		LANE1	HSSTLP_283_1224:U1_HSSTLP_LANE	D22/C22/D20/C20
		LANE2	HSSTLP_283_1224:U2_HSSTLP_LANE	B21/A21/F19/E19
		LANE3	HSSTLP_283_1224:U3_HSSTLP_LANE	B19/A19/D18/C18
		PLL0	HSSTLP_283_1224:U0_HSSTLP_PLL	
		PLL1	HSSTLP_283_1224:U1_HSSTLP_PLL	
	HSSTLP_R3	LANE0	HSSTLP_484_1224:U0_HSSTLP_LANE	B13/A13/F13/E13
		LANE1	HSSTLP_484_1224:U1_HSSTLP_LANE	D14/C14/F15/E15
		LANE2	HSSTLP_484_1224:U2_HSSTLP_LANE	B15/A15/D16/C16
		LANE3	HSSTLP_484_1224:U3_HSSTLP_LANE	B17/A17/F17/E17
		PLL0	HSSTLP_484_1224:U0_HSSTLP_PLL	
		PLL1	HSSTLP_484_1224:U1_HSSTLP_PLL	
	HSSTLP_L7	LANE0	HSSTLP_283_0:U0_HSSTLP_LANE	AN19/AP19/AL18/AM18
		LANE1	HSSTLP_283_0:U1_HSSTLP_LANE	AN21/AP21/AJ19/AK19
		LANE2	HSSTLP_283_0:U2_HSSTLP_LANE	AL22/AM22/AL20/AM20
		LANE3	HSSTLP_283_0:U3_HSSTLP_LANE	AN23/AP23/AJ21/AK21
		PLL0	HSSTLP_283_0:U0_HSSTLP_PLL	
		PLL1	HSSTLP_283_0:U1_HSSTLP_PLL	
	HSSTLP_R7	LANE0	HSSTLP_484_0:U0_HSSTLP_LANE	AN17/AP17/AJ17/AK17
		LANE1	HSSTLP_484_0:U1_HSSTLP_LANE	AN15/AP15/AL16/AM16
		LANE2	HSSTLP_484_0:U2_HSSTLP_LANE	AL14/AM14/AJ15/AK15
		LANE3	HSSTLP_484_0:U3_HSSTLP_LANE	AN13/AP13/AJ13/AK13
		PLL0	HSSTLP_484_0:U0_HSSTLP_PLL	
		PLL1	HSSTLP_484_0:U1_HSSTLP_PLL	

The four transmit and receive LANEs in the HSSTLP share PLL0 and PLL1. Each transmit or receive LANE can independently select PLL0 or PLL1. For the working frequency ranges of PLLs, refer to the “DS04001_Logos2 Family FPGAs Device Datasheet”. PLL0 and PLL1 each correspond to a pair of external differential reference clock inputs, and each PLL can also select a reference clock from another PLL or from the Fabric clock as the reference clock input (use the Fabric logic clock as a reference clock for internal testing only); PLL output frequency supports dynamic re-division to accommodate the data rate range.

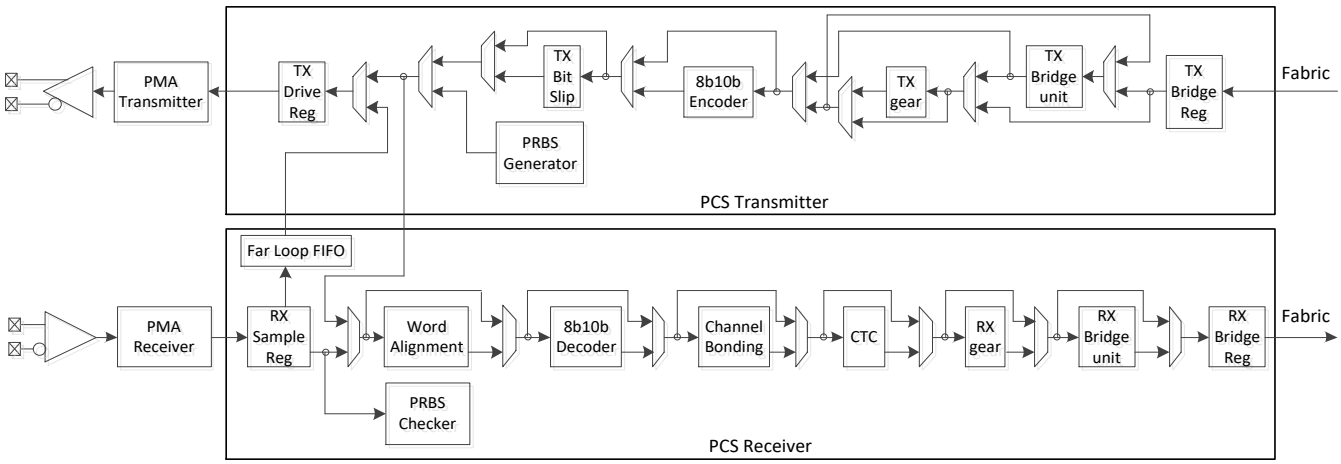

Figure 1-2 PCS Transmitter and Receiver Structure Diagram

As shown in Figure 1-2, each PCS Transmitter mainly includes the following modules:

- TX Bridge Reg module: Used for data bridging from Fabric to PCS Transmitter
- TX Bridge unit module: Used for phase compensation for the internal clock domain of the PCS Transmitter and the Fabric clock domain
- 8B10B Encoder module: Completes 8B10B encoding compliant with the IEEE 802.3 1000BASE-X specification
- TX gear module: Completes the 64B66B/64B67B data adaptation function
- TX Bit Slip module: Mainly performs bit slip on the transmitted data according to the configuration
- PRBS Generator module: Generates the PRBS test pattern
- TX Drive Reg module: Used for data bridging from PCS Transmitter to PMA Transmitter

The TX Bridge unit, TX gear, 8B10B Encoder, and TX Bit Slip modules can be bypassed to meet the application requirements of different protocols. Users can flexibly choose the interface data width between HSSTLP and Fabric according to protocol requirements, with supported bit width modes including 8bit only, 10bit only, 8B10B 8bit (using 8B10B encoding, with 10 bits of valid data after encoding), 16bit only, 20bit only, 8B10B 16bit, 32bit only, 40bit only, 8B10B 32bit, 64B66B/64B67B 16bit, and 64B66B/64B67B 32bit (where the bit width mode refers to valid data bits, the actual data interface bit count could be extended). The higher the data rate, the wider the selected interface data width, so that the timing requirements for the internal logic of the Fabric are reduced. When the data width is set to 32bit only, 40bit only, 8B10B 32bit, and 64B66B/64B67B 32bit, the PCS Transmitter converts the data to 16bits or 20bits before transferring it to the PMA Transmitter.

As shown in Figure 1-2, each PCS Receiver mainly includes the following functional modules:

- RX Sample Reg module: Used for data bridging from the PMA Receiver to the PCS Receiver
- PRBS Checker module: Checks PRBS pattern
- Word Alignment module: Flexible Word Alignment
- 8B10B Decoder module: Completes 8B10B decoding compliant with the IEEE 802.3 1000BASE-X Specification
- RX gear module: Completes the 64B66B/64B67B data adaptation function
- Channel Bonding module: Used for channel alignment
- CTC module: Compensates the slight frequency error between the transmit clock and receive clock
- RX Bridge unit module: Used for phase compensation for the internal clock domain of the PCS Receiver and the Fabric clock domain
- RX Bridge Reg module: Used for data bridging from PCS Receiver to Fabric

Users can bypass the Word Alignment, 8B10B Decoder, Channel Bonding, CTC, RX gear, and RX Bridge unit modules to meet the application requirements of different protocols. Users can also flexibly choose the interface data width between HSSTLP and Fabric according to protocol requirements, with supported bit width modes including 8bit only, 10 bit only, 8B10B 8bit (using 8B10B encoding, with 10 bits of valid data before decoding), 16bit only, 20bit only, 8B10B 16bit, 32bit only, 40bit only, 8B10B 32bit, 64B66B/64B67B 16bit, and 64B66B/64B67B 32bit. Data width modes 32bit only, 40bit only, 8B10B 32bit, and 64B66B/64B67B 32bit are suitable for applications with higher data rates, where the PCS Receiver converts the 16bits or 20bits data from the PMA Receiver to 32bits or 40bits before transferring it to Fabric.

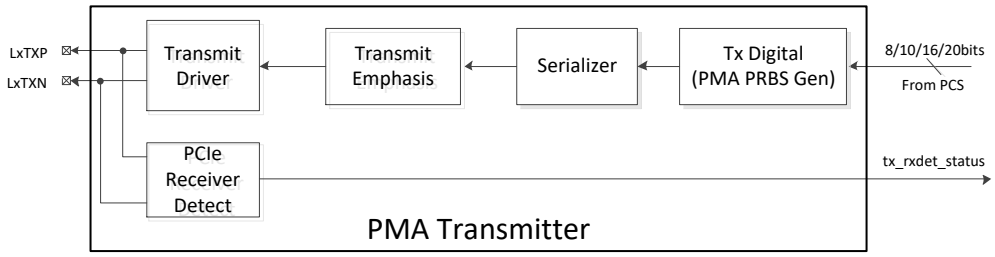

Figure 1-3 PMA Transmitter Functional Diagram

As shown in Figure 1-3, each PMA Transmitter mainly includes the following functional modules:

- TX Digital module: Completes data bridging from PCS Transmitter to PMA Transmitter, as well as PMA PRBS Generator
- Serializer module: Converts parallel data to serial data
- Transmit Emphasis module: Adjustable de-emphasis function
- Transmit Driver module: Adjustable transmit driver

- PCI Express Receiver Detect module: PCI Express-based receiver detection

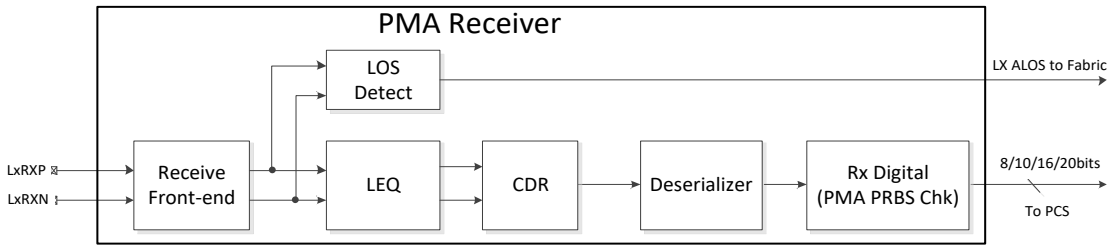

Figure 1-4 PMA Receiver Functional Diagram

As shown in Figure 1-4, each PMA Receiver mainly includes the following functional modules:

- Receive Front-end module: Multiple receive termination modes
- LEQ Module: Linear Equalizer
- CDR module: Data and clock recovery
- LOS Detect module: Detects if the receive signal is active
- Deserializer module: Converts serial data to 8-bit, 10-bit, 16-bit, and 20-bit parallel data
- RX Digital module: Completes the data bridging from the PMA Receiver to the PCS Receiver and PMA PRBS Checker

Chapter 2 HSSTLP Interface Description

Table 2-1 HSSTLP LANE Clock-Related Ports

Port	Input/ Output	Clock Domain	Description
P_RCLK2FABRIC	Output	Clock	The receive clock sent to Fabric
P_TCLK2FABRIC	Output	Clock	The transmit clock sent to Fabric
P_RX_CLK_FR_CORE	Input	Clock	The transmit clock from Fabric, serving as the RX interface data clock
P_RCLK2_FR_CORE	Input	Clock	The receive clock from Fabric, which is generated by P_REFCK2CORE through PLL frequency multiplication and 2 times the frequency of P_RX_CLK_FR_CORE
P_TX_CLK_FR_CORE	Input	Clock	The transmit clock from Fabric, serving as the TX interface data clock
P_TCLK2_FR_CORE	Input	Clock	The transmit clock from Fabric, which is generated by P_REFCK2CORE through PLL frequency multiplication and 2 times the frequency of P_TX_CLK_FR_CORE
P_CA_ALIGN_RX	Output	Asynchronous Signal	Receiving LANE CLK Aligner dynamic state output, a 0-to-1 transition indicates aligner success, an asynchronous signal
P_CA_ALIGN_TX	Output	Asynchronous Signal	Transmitting LANE CLK Aligner dynamic state output, a 0-to-1 transition indicates aligner success, an asynchronous signal
P_CIM_CLK_ALIGNER_RX[7:0]	Input	Asynchronous Signal	CLK Aligner delay step selection at the receive side, an asynchronous signal
P_CIM_CLK_ALIGNER_TX[7:0]	Input	Asynchronous Signal	CLK Aligner delay step selection at transmit side, an asynchronous signal
P_CIM_DYN_DLY_SEL_RX	Input	Asynchronous Signal	Receive LANE's CLK Aligner enable, an asynchronous signal, 1: Enabled; 0: Disabled
P_CIM_DYN_DLY_SEL_TX	Input	Asynchronous Signal	Transmit LANE's CLK Aligner enable, an asynchronous signal, 1: Enabled; 0: Disabled
P_CIM_START_ALIGN_RX	Input	Asynchronous Signal	Input source for generating receive LANE CLK Aligner pulse, the setting value is triggered once on the rising edge, an asynchronous signal
P_CIM_START_ALIGN_TX	Input	Asynchronous Signal	Input source for generating transmit LANE CLK Aligner pulse, the setting value is triggered once on the rising edge, an asynchronous signal

Table 2-2 HSSTLP LANE Reset-Related Ports

Port	Input/ Output	Clock Domain	Description
P_PCS_TX_RST	Input	Asynchronous Signal	Reset PCS Transmitter, 1: Reset; 0: Not reset
P_PCS_RX_RST	Input	Asynchronous	Reset PCS Receiver, 1: Reset; 0: Not reset

Port	Input/ Output	Clock Domain	Description
		Signal	
P_LANE_PD	Input	Asynchronous Signal	Reserved, fixed to value 0
P_LANE_RST	Input	Asynchronous Signal	LANE reset, including RX LANE and TX LANE; 1: Reset; 0: Not reset
P_RX_LANE_PD	Input	Asynchronous Signal	RX LANE power down, including RX PMA and RX PCS; 1: Power down; 0: Not power down Operate this port only for a power-up reset (HSST overall reset); Do not operate this port when resetting RX LANE only;
P_RX_PMA_RST	Input	Asynchronous Signal	Reset PMA Receiver, an asynchronous signal, 1: Reset; 0: Not reset
P_TX_PMA_RST	Input	Asynchronous Signal	Reset PMA Transmitter, an asynchronous signal, 1: Reset; 0: Not reset
P_TX_LANE_PD_CLKPATH	Input	Asynchronous Signal	TX LANE power down, 1: Power down; 0: Not power down Operate this port only for a power-up reset (HSST overall reset); Do not operate this port when resetting TX LANE only;
P_TX_LANE_PD_PISO	Input	Asynchronous Signal	TX parallel-to-serial conversion module power down, 1: Power down; 0: Not power down Operate this port only for a power-up reset (HSST overall reset); Do not operate this port when resetting TX LANE only;
P_TX_LANE_PD_DRIVER	Input	Asynchronous Signal	TX driver power down, 1: Power down; 0: Not power down Operate this port only for a power-up reset (HSST overall reset); Do not operate this port when resetting TX LANE only;
P_PCS_CB_RST	Input	Asynchronous Signal	Reset module after Channel bonding, 1: Reset; 0: Not reset; Internal test signal, fixed to value 0.
P_CTLE_ADP_RST	Input	Asynchronous Signal	Reset the linear equalizer of the PMA receiver, 1: Reset; 0: Not reset; Internal test signal, fixed to value 0.

Table 2-3 Transmitting Ports between HSSTLP LANE and Fabric

Port	Input/ Output	Clock Domain	Description
P_TDATA[45:0]	Input	P_TX_CLK _FR_CORE	Transmit data
P_TX_LS_DATA	Input	P_TX_CLK _FR_CORE	The transmitted low-frequency signal
P_TX_BEACON_EN	Input	Asynchronous Signal	TX beacon enable signal, 1: Enabled; 0: Disabled
P_TX_DEEMP[1:0]	Input	Asynchronous	Transmitter de-emphasis control

Port	Input/ Output	Clock Domain	Description
		Signal	2’00: De-emphasis source register PMA_REG_CFG_POST; 2’01: De-emphasis source register PMA_REG_CFG_POST1; 2’10: De-emphasis source register PMA_REG_CFG_POST2; 2’11: Reserved
P_TX_SWING	Input	Asynchronous Signal	Transmitter output swing value for half-swing control 1’b0: Full swing (default); 1’b1: Half swing
P_TX_MARGIN[2:0]	Input	Asynchronous Signal	Transmitter output swing DAC source selection. Default value 3’b000 3’b000: Swing source register PMA_CH_REG_TX_AMP_DAC0; 3’b001: Swing source register PMA_CH_REG_TX_AMP_DAC1; 3’b010: Swing source register PMA_CH_REG_TX_AMP_DAC2; 3’b011: Swing source register PMA_CH_REG_TX_AMP_DAC3; Other values: Reserved
P_TX_RXDET_REQ	Input	Asynchronous Signal	Receiver Detection request signal
P_TX_RXDET_STATUS	Output	Asynchronous Signal	Receiver Detection result, an asynchronous signal,1: Receiver detected
P_TX_RATE[2:0]	Input	Asynchronous Signal	TX line rate control signal 2’b00: The line rate is 1/4 of the PLL clock frequency; 2’b01: The line rate is 1/2 of the PLL clock frequency; 2’b10: The line rate is equal to the PLL clock frequency; 2’b11: The line rate is 2 times the PLL clock frequency. bit[2]: Reserved, fixed to value 0
P_TX_BUSWIDTH[2:0]	Input	Asynchronous Signal	Data width selection from TX PCS to TX PMA 3’bX00: 8bit; 3’bX01:10bit; 3’bX10:16bit; 3’bX11:20bit; bit[2]: Reserved, fixed to value 0
P_TX_SDN	Output	External port	Differential output data negative end, HSSTLP dedicated pin
P_TX_SDP	Output	External port	Differential output data positive end, HSSTLP dedicated pin

Table 2-4 Receiving Ports between HSSTLP LANE and Fabric

Port	Input/ Output	Clock Domain	Description
P_RDATA[46:0]	Output	P_RX_CLK _FR_CORE	Receive data
P_RX_SIGDET_STATUS	Output	Asynchronous Signal	Port valid signal detection, an asynchronous signal: 0: No valid signal detected from port P_RX_SDP/P_RX_SDN 1: Valid signal detected from port

Port	Input/ Output	Clock Domain	Description
			P_RX_SDP/P_RX_SDN
P_RX_SATA_COMINIT	Output	Asynchronous Signal	SATA COMINIT status, 1: Detected; 0: Not detected
P_RX_SATA_COMWAKE	Output	Asynchronous Signal	SATA COMWAKE status, 1: Detected; 0: Not detected
P_RX_LS_DATA	Output	P_RX_CLK _FR_CORE	Low-frequency signal output to Fabric
P_RX_READY	Output	Asynchronous Signal	This active-High signal indicates the CDR has locked successfully, an asynchronous signal, 1: Locked; 0: Unlocked
P_TEST_STATUS[19:0]	Output	Asynchronous Signal	RX output test status register, internal test signal
P_PCS_WORD_ALIGN_EN	Input	Asynchronous Signal	The control is valid when the RX CLK Slip port control mode is configured to be valid. It serves as the RX CLK Slip control signal and is an asynchronous signal. A rising edge from 0 to 1 causes the PMA RX's Deserializer module to slip by one bit When configured as an external state machine, it serves as the Word Alignment enable signal and is an asynchronous signal, 1: Enabled; 0: Disabled
P_PCS_LSM_SYNCED	Output	Asynchronous Signal	Word Alignment successful, state machine lock flag, an asynchronous signal, 1: Word Alignment successful; 0: Word Alignment unsuccessful;
P_PCS_MCB_EXT_EN	Input	Asynchronous Signal	Channel bonding enable under external state machine mode, an asynchronous signal, 1: Enabled; 0: Disabled
P_PCS_RX_MCB_STATUS	Output	Asynchronous Signal	Channel Bonding control state machine lock signal, an asynchronous signal, 1: Bonded; 0: Not bonded
P_RXGEAR_SLIP	Input	Asynchronous Signal	Slip indication to RX gearbox with 64B66B/67b decoder mode, edge-triggered, detection of either a rising or falling edge will cause a slip by 1 bit, asynchronous signal, internally synchronized by the PCS
P_RX_POLARITY_INVERT	Input	Asynchronous Signal	RX Sample Reg's polarity inversion enable, an asynchronous signal, 1: Polarity inverted; 0: Polarity not inverted
P_CEB_ADETECT_EN[3:0]	Input	Asynchronous Signal	Test signal, set externally to 4'b1111' in normal mode
P_RX_RATE[2:0]	Input	Asynchronous Signal	RX line rate control signal 2'b00: The line rate is 1/4 of the PLL clock frequency; 2'b01: The line rate is 1/2 of the PLL clock frequency; 2'b10: The line rate is equal to the PLL clock frequency; 2'b11: The line rate is 2 times the PLL clock frequency. bit[2]: Reserved, fixed to value 0
P_RX_BUSWIDTH[2:0]	Input	Asynchronous Signal	Data width selection from RX PMA to RX PCS 3'bX00: 8bit; 3'bX01:10bit; 3'bX10:16bit;

Port	Input/ Output	Clock Domain	Description
			3'bX11:20bit; bit[2]: Reserved, fixed to value 0
P_RX_HIGHZ	Input	Asynchronous Signal	RX input high impedance control signal, 0: Not at high impedance; 1: At high impedance
P_RX_SDN	Input	External port	Differential input data negative end, HSSTLP dedicated pin
P_RX_SDP	Input	External port	Differential input data positive end, HSSTLP dedicated pin

Table 2-5 Other Ports between HSSTLP LANE and Fabric

Port	Input/ Output	Clock Domain	Description
P_PCS_NEAREND_LOOP	Input	Asynchronous Signal	PCS Near-end loopback control signal, 1: Enabled; 0: Disabled
P_PCS_FAREND_LOOP	Input	Asynchronous Signal	PCS Far-end loopback control signal, 1: Enabled; 0: Disabled
P_PMA_NEAREND_PLOOP	Input	Asynchronous Signal	PMA Near-end parallel loopback control signal, 1: Enabled; 0: Disabled
P_PMA_NEAREND_SLOOP	Input	Asynchronous Signal	PMA Near-end serial loopback control signal, 1: Enabled; 0: Disabled
P_PMA_FAREND_PLOOP	Input	Asynchronous Signal	PMA Far-end parallel loopback control signal, 1: Enabled; 0: Disabled
P_CFG_READY	Output	P_CFG_CLK	Dynamic configuration interface read and write ready output, 1: Valid; 0: Invalid
P_CFG_RDATA[7:0]	Output	P_CFG_CLK	Read data for the dynamic configuration interface
P_CFG_INT	Output	P_CFG_CLK	Dynamic configuration interface interrupt output, 1: Valid; 0: Invalid
P_CFG_CLK	Input	Clock	Dynamically configure the clock input of the interface
P_CFG_RST	Input	P_CFG_CLK	Dynamic configuration interface reset signal, 1: Reset; 0: Not reset. All registers revert to the initial values set by the Parameter after reset
P_CFG_PSEL	Input	P_CFG_CLK	Dynamic configuration interface selection signal, 1: Selected; 0: Not selected
P_CFG_ENABLE	Input	P_CFG_CLK	Dynamic configuration interface access enable, 1: Enabled; 0: Disabled
P_CFG_WRITE	Input	P_CFG_CLK	Dynamic configuration interface read and write select signal, 1: Write; 0: Read
P_CFG_ADDR[11:0]	Input	P_CFG_CLK	Dynamic configuration interface write address
P_CFG_WDATA[7:0]	Input	P_CFG_CLK	Dynamic configuration interface write data

Table 2-6 HSSTLP PLL Ports

Port	Input/ Output	Clock Domain	Description
P_REFCK2CORE	Output	Clock	Pin input reference clock Bypass output to Fabric
P_PLL_REF_CLK	Input	Clock	PLL reference clock from Fabric
P_PLL_READY	Output	Asynchronous Signal	PLL lock status, an asynchronous signal, 1: Locked; 0: Unlocked After PLL is locked, P_PLL_READY is pulled

Port	Input/ Output	Clock Domain	Description
			high and remains unchanged. A PLL reset is required to re-indicate the PLL lock status.
P_PLLPOWERDOWN	Input	Asynchronous Signal	PLL power-down control 0: Not powered down (default); 1: Powered down
P_PLL_RST	Input	Asynchronous Signal	PLL reset control, 0: Not reset (default); 1: Reset
P_RESCAL_RST_I	Input	Asynchronous Signal	Resistor calibration reset, 1: Reset; 0: Not reset, Internal test signal, fixed to value 0.
P_RESCAL_I_CODE_I[5:0]	Input	Asynchronous Signal	PMA manually configured resistance value. It defaults to 6b'101110, internal test signal
P_RESCAL_I_CODE_O[5:0]	Output	Asynchronous Signal	The resistor control output code when invalid. It defaults to 6b'101110 internal test signal
P_LANE_SYNC	Input	Asynchronous Signal	SYNC signal for TX LANE synchronization
P_RATE_CHANGE _TCLK_ON	Input	Asynchronous Signal	Synchronization control signal enable for dynamic switching
P_PLL_LOCKDET_RST_I	Input	Asynchronous Signal	PLL lock detector reset, 1: Reset; 0: Not reset; Internal test signal, fixed to value 0.
P_CFG_READY_PLL	Output	P_CFG_CLK _PLL	Dynamic configuration interface read and write ready output, 1: Valid; 0: Invalid
P_CFG_RDATA_PLL[7:0]	Output	P_CFG_CLK _PLL	Read data for the dynamic configuration interface
P_CFG_INT_PLL	Output	P_CFG_CLK _PLL	Dynamic configuration interface interrupt output, 1: Valid; 0: Invalid
P_CFG_RST_PLL	Input	P_CFG_CLK _PLL	Dynamic configuration interface reset signal, 1: Reset; 0: Not reset. All registers revert to the initial values set by the Parameter after reset.
P_CFG_CLK_PLL	Input	Clock	Dynamic configuration interface clock input
P_CFG_PSEL_PLL	Input	P_CFG_CLK _PLL	Dynamic configuration interface selection input, 1: Selected; 0: Not selected
P_CFG_ENABLE_PLL	Input	P_CFG_CLK _PLL	Dynamic configuration interface access enable, 1: Enabled; 0: Disabled
P_CFG_WRITE_PLL	Input	P_CFG_CLK _PLL	Dynamic configuration interface read and write select signal, 1: Write; 0: Read
P_CFG_ADDR_PLL[11:0]	Input	P_CFG_CLK _PLL	Dynamic configuration interface write address
P_CFG_WDATA_PLL[7:0]	Input	P_CFG_CLK _PLL	Dynamic configuration interface write data
REFCLK_CML_N	Input	External port	Differential input reference clock negative end, HSSTLP dedicated pin
REFCLK_CML_P	Input	External port	Differential input reference clock positive end, HSSTLP dedicated pin

Chapter 3 HSSTLP Functional Description

3.1 HSSTLP Clock Structure

3.1.1 Reference Clock Selection

HSSTLP supports flexible selection of PLL0, PLL1, LANE TX and RX reference clocks: each HSSTLP has two pairs of dedicated differential reference clock input pins P_REFCK0P/P_REFCK0N and P_REFCK1P/P_REFCK1N. PLLs can also select clocks from the Fabric: P_PLL0_REF_CLK, P_PLL1_REF_CLK (Use Fabric logic clock as reference clock only for internal testing). Only the PG2L200H FFBG1156 device supports selecting the reference clock from an adjacent HSSTLP. This can be configured through PMA_PLL_REG_REFCLK_SEL and PMA_PLL_REG_CML_CLK_OUT_EN. This is not supported by PG2L25H, PG2L50H, and PG2L100H devices.

TX and RX LANEs can independently select the clock output from either PLL0 or PLL1. The dedicated clock input pins P_REFCK0P/P_REFCK0N and P_REFCK1P/P_REFCK1N can also output to Fabric through the ports P_PLL0_REFCK2CORE and P_PLL1_REFCK2CORE.

The structure diagram of the reference clock selection is shown in Figure 3-1:

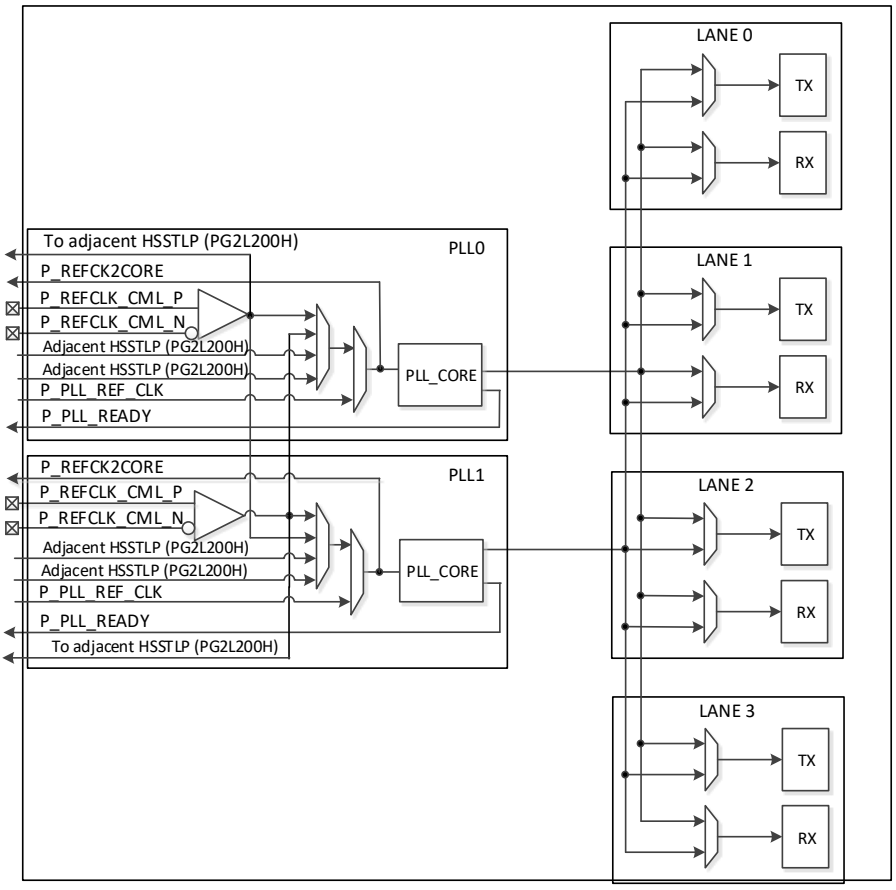

Figure 3-1 Reference Clock Source Selection Structure Diagram

The reference clock input circuit is shown in Figure 3-2, where resistors connected to the input ports P and N are used as matching resistors, with external AC coupling capacitors connected. For the resistance value HSST_R_{RCLK} and the capacitance value HSST_$C_{RCLKEXT}$, refer to the "DS04001_Logos2 Family FPGAs Device Datasheet". The matching impedance is active by default and can be disconnected through the configuration register. The reference clock is connected to the buffer after passing through the AC coupling capacitor and then output to the internal PLL loop.

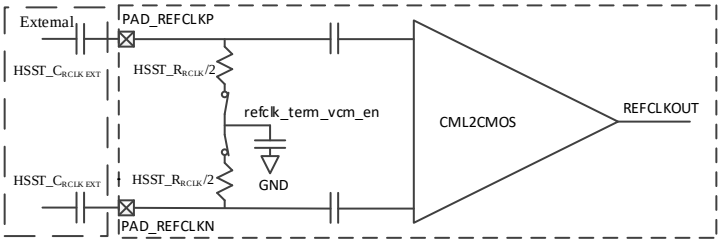

Figure 3-2 Reference Clock Input Circuit

3.1.2 Clock Structure of the Transmit Path

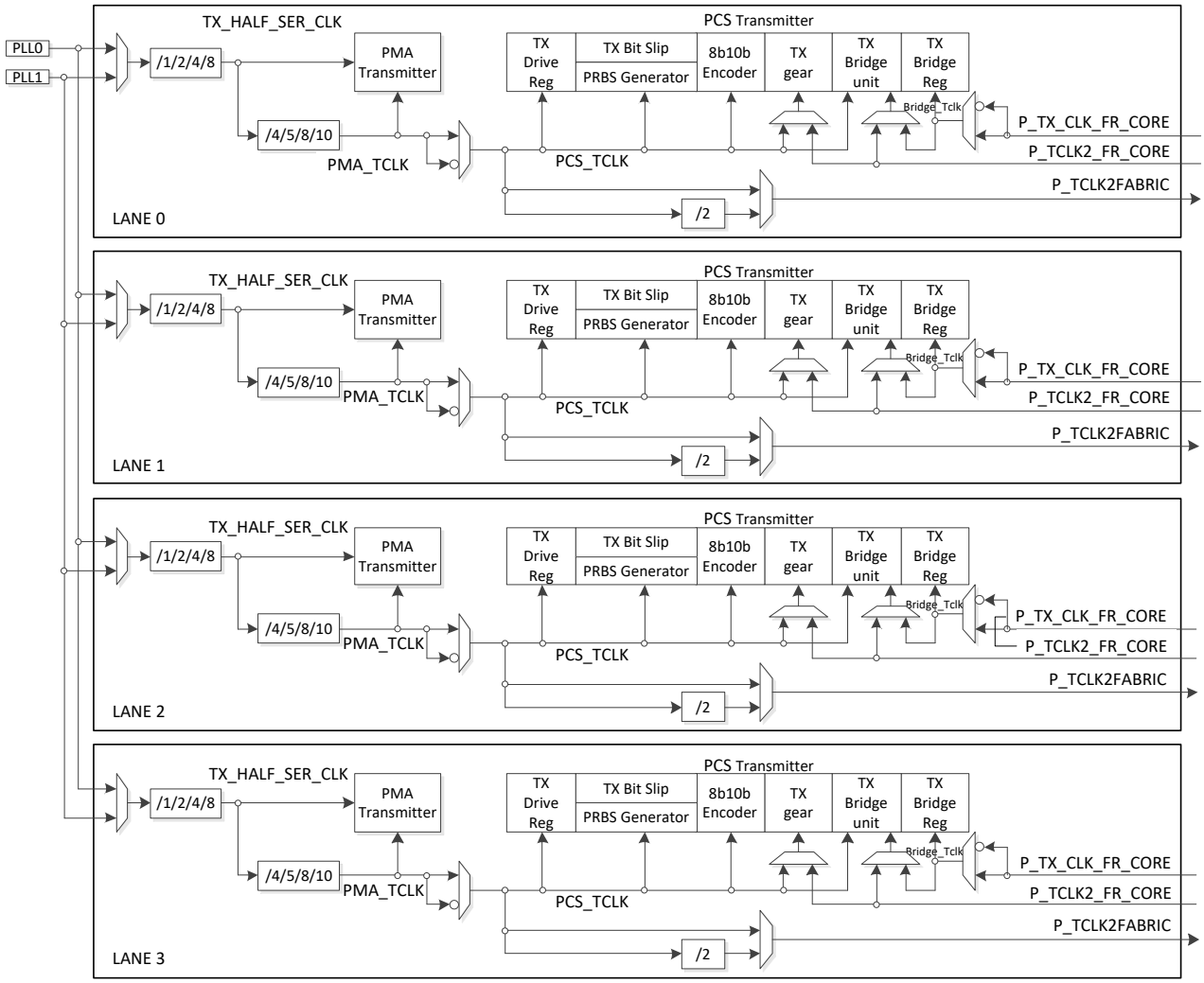

Figure 3-3 Transmit Path Clock Structure Diagram

As shown in Figure 3-3, each HSSTLP shares PLL0 and PLL1, and the high-speed clocks output by PLL0 and PLL1 are distributed to four LANEs, each of which independently selects the output clock of PLL0 or PLL1; users can, using a division factor, independently generate TX_HALF_SER_CLK for each LANE based on the PLL output, with the data rate being 2 times the frequency of TX_HALF_SER_CLK.The frequency of TX_HALF_SER_CLK can be the PLL output frequency divided by the division ratio of 1/2/4/8.

The channel rate supports dynamic configuration, suitable for dynamic rate selection in applications such as PCI Express.

PMA_TCLK is generated by further dividing the TX_SER_CLK, supporting four division ratios of 4/5/8/10, which respectively correspond to the 8/10/16/20 bits data width of the interface between PMA and PCS. PMA_TCLK, once transferred to the PCS Transmitter, is referred to as PCS_TCLK.

The clock output P_TCLK2FABRIC can be used for Fabric internal processing; at lower data rates (e.g., 3Gbps), its frequency is consistent with that of PCS_TCLK; at higher data rates, its frequency can be reduced to half of that of PCS_TCLK.

The clock input P_TX_CLK_FR_CORE is the transmit clock fed back from the Fabric, P_TX_CLK2_FR_CORE is twice the frequency of P_TX_CLK_FR_CORE and phase-aligned, P_TX_CLK_FR_CORE and P_TX_CLK2_FR_CORE can be generated by the PLL in the Fabric from the refclk output by the PCS.

3.1.3 Clock Structure of the Receive Path

Each HSSTLP receiving LANE has an RX CDR. After it is divided by 1/2/4/8, the generated clock signal RX_HALF_SER_CLK has a frequency that is half of the LANE data rate. The clock structure diagram of the receiving LANE is shown in Figure 3-4:

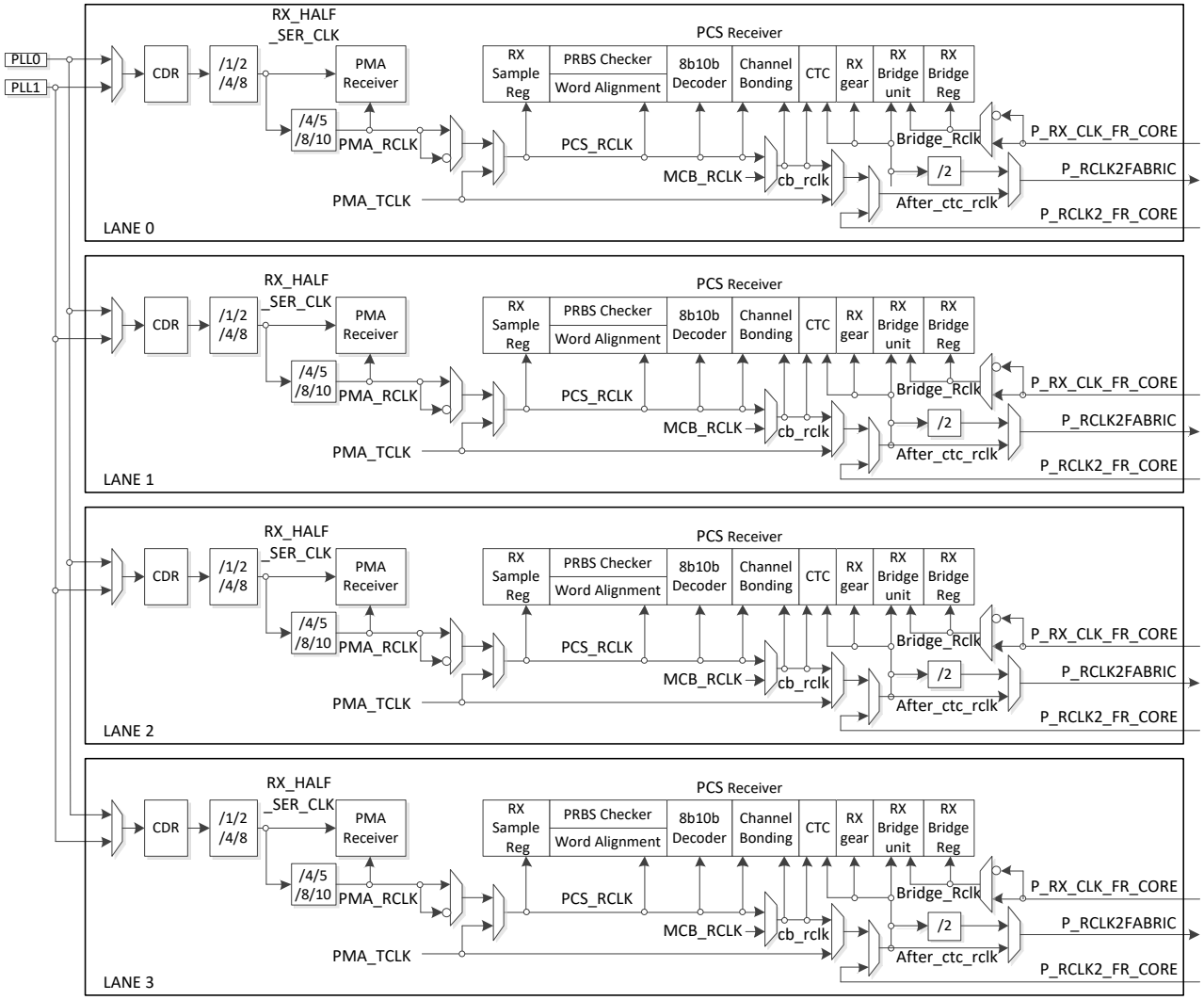

Figure 3-4 Receiving LANE Clock Structure Diagram

PMA_RCLK is generated by further dividing the RX_HALF_SER_CLK, supporting four division ratios of 4/5/8/10, which respectively correspond to the 8/10/16/20 bits data width of the interface between PMA and PCS. Once PMA_RCLK is transferred to the PCS Receiver, it is referred to as PCS_RCLK.

When Channel Bonding is enabled, the data from each LANE is synchronized to the same clock MCB_RCLK after passing through the Channel Bonding module. MCB_RCLK is derived from the Bonding Master's PMA_RCLK; in a 4-Channel Bonding, it is derived from LANE 0's PMA_RCLK; in a 2-Channel Bonding, it is derived from either LANE 0's or LANE 2's PMA_RCLK.

When the CTC function is enabled, the data processed through the CTC module will be transferred to the PMA_TCLK clock domain, where PMA_TCLK is derived from the PMA Transmitter of the respective LANE.

The clock output P_RCLK2FABRIC can be used for Fabric received data processing. At lower data rates (e.g., 3Gbps), its frequency is consistent with that of PMA_RCLK; at higher data rates, its frequency can be reduced to half of that of PMA_RCLK.

3.2 PLL Function

The TX and RX of the four LANEs in each HSSTLP share PLL0 and PLL1. The TX or RX of each channel can independently select the clock source. The functional structure diagram is shown in Figure 3-5.

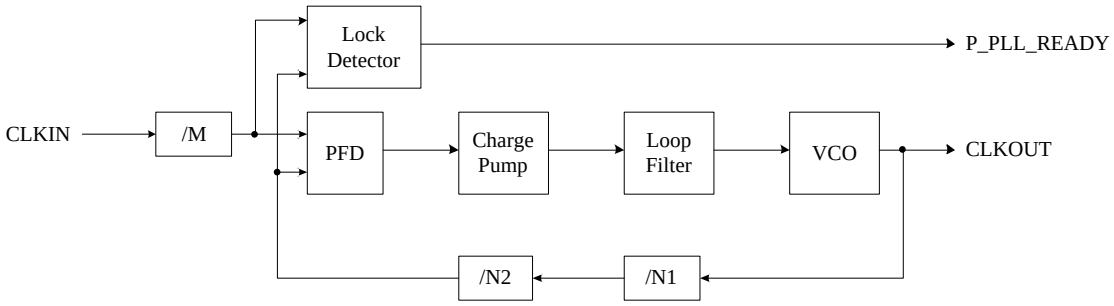

Figure 3-5 PLL Structure Diagram

The primary function of the PLL is frequency synthesis. The input clock and feedback clock pass through the Phase Frequency Detector (PFD), Charge Pump, and Loop Filter. For PLL output frequency, refer to the HSST_Fpll parameter in the "DS04001_Logos2 Family FPGAs Device Datasheet". The PLL output frequency is determined by the input clock CLKIN frequency, input division factor M, and feedback division factors N1 and N2, with the calculation method as follows:

CLKOUT frequency = CLKIN frequency* N1*N2/M (3-1)

The relationship between PMA line rate and PLL output is calculated as follows:

PMA line rate = CLKOUT frequency*2/D (3-2)

Where D represents the division ratio on the TX or RX clock path.

Table 3-1 Supported Range for PLL Division Factors

Division Factor	Supported Values	Register Definition
M	1,2	Refer to the bit[4:0] definition of pma_pll_reg2
N1	4,5	Refer to the bit[5] definition of pma_pll_reg3
N2	1,2,3,4,5,6,8,10	Refer to the bit[4:0] definition of pma_pll_reg3
D	1,2,4,8	TX: Refer to the bit[3], [1:0] definitions of pma_rx_reg12
		RX: Refer to the bit[7], [5:4] definitions of pma_rx_reg4

Attention:

1. When the PLL is operating properly, ensure the reference clock is stable;

2. If the reference clock instability causes a locking anomaly during the locking process, wait for the reference clock to stabilise, then reset the PLL and re-lock;

3. When using the PLL, if the reference clock changes or the reference clock is lost and then restored, the PLL needs to be reset;

4. When using PLL0 and PLL1 simultaneously, resetting one PLL will momentarily affect the other PLL (less than 1μs), after which it will return to its normal state. During this affected time, it may cause errors in the corresponding channel;

5. PLL1 shares certain reset control signals with PLL0. When using only one PLL, PLL0 must be used. There are no restrictions when using both PLLs simultaneously;

6. When the PLL output frequency is below 2.4GHz, the division factor D cannot be 1.

3.2.1 Dynamic Rate Switching via Register

The PMA line rate is the line rate of the TX/RX channel. Users can flexibly modify the PLL division factor, TX clock division ratio D, or RX clock division ratio D as per specific requirements to achieve Dynamic Rate Switching. Below is the description of the reset for Dynamic Rate Switching:

Table 3-2 Description of Reset for Dynamic Rate Switching

Functional Scenarios	Reset PLL	Reset TX Channel	Reset RX Channel
Modify PLL division factor (M, N1, N2)	✓	✓	✓
Modify TX clock division ratio D		✓	
Modify RX clock division ratio D			✓

Attention:

1. In scenarios involving modifying the PLL division factor, after dynamic switching, the PLL needs to be reset first, followed by resetting the TX and RX channels using the PLL;

2. In scenarios involving modifying only the TX or RX clock division ratio D, after dynamic switching, only the TX and RX channels using the PLL need to be reset;

3. Refer to Figure 4-1 for PLL reset, Figure 4-6 for TX channel reset timing, and Figure 4-7 for RX channel reset timing.

3.3 PCS Transmitter Function

3.3.1 TX Bridge Reg Module

Completes the transmission data bridging from Fabric to HSSTLP, ensuring interface timing. Each LANE has 46 bits of transmission data, with definitions varying according to different data width modes, refer to Table 3-3 for details:

Table 3-3 LANE Transmission Data Definitions

	P_TDATA_x Data Bits																		
Data Width Modes	[45:44]	[43]	[42]	[41]	[40:39]	[38:33]	[32]	[31]	[30]	[29:22]	[21]	[20]	[19]	[18:17]	[16:11]	[10]	[9]	[8]	[7:0]
8bit only	PCIe_EI	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	TXD [7:0]
10bit only	PCIe_EI	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	TXD [9:0]		
8B10B 8bit	PCIe_EI	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	TXK	TDISP CTRL	TDISP SEL	TXD [7:0]
16bit only	PCIe_EI	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	TXD [15:10]	NA	TXD [9:0]		
20bit only	PCIe_EI	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	TXD [19:10]				NA	TXD [9:0]		
8B10B 16bit	PCIe_EI	NA	NA	NA	NA	NA	NA	NA	NA	NA	TXK [1]	TDISP CTRL [1]	TDISP SEL [1]	TXD [15:8]		TXK [0]	TDISP CTRL [0]	TDISP SEL [0]	TXD [7:0]
32bit only	PCIe_EI	NA	NA	NA	NA	TXD [31:26]	NA	TXD [25:16]			NA	NA	NA	NA	TXD [15:10]	NA	TXD [9:0]		
40bit only	PCIe_EI	NA	TXD [39:30]				NA	TXD [29:20]			NA	TXD [19:10]				NA	TXD [9:0]		
8B10B 32bit	PCIe_EI	TXK [3]	TDISPCTRL [7:6]		TXD [31:24]		TXK [2]	TDISP CTRL [2]	TDISP SEL [2]	TXD [23:16]	TXK [1]	TDISP CTRL [1]	TDISP SEL [1]	TXD [15:8]		TXK [0]	TDISP CTRL [0]	TDISP SEL [0]	TXD [7:0]
64b 66b 16bit	PCIe_EI	TXH[2:0]			TXQ [6:5]	NA	NA	NA	NA	NA	TXQ[4:0]				TXD [15:10]	NA	TXD[9:0]		
64b 66b 32bit	PCIe_EI	TXH[2:0]			TXQ [6:5]	TXD [31:26]	NA	TXD[25:16]			TXQ[4:0]				TXD [15:10]	NA	TXD[9:0]		

The definitions of the data bits are shown in the following table:

Table 3-4 Definitions of Data Bits in P_TDATA

Data Bit Name	Description
TXK	1 indicates that TXD is the 8B10B Special Code-groups compliant with the IEEE 802.3 1000BASE-X Specification; 0 indicates that TXD is the 8B10B Data Code-groups compliant with the IEEE 802.3 1000BASE-X Specification;
TXD	code-groups
TDISPCTRL	Used for forcing the 8B10B polarity and the mandatory replacement from I2 to I1, {TDISPCTRL, TDISPSEL} can be: 2'b00: Normal Data Transmission 2'b01: According to the IEEE 802.3 1000BASE-X specification protocol, it implements the selection of the first I1/I2 at the frame trailer, and automatically accomplishes the replacement from I2 to I1 under the right conditions. 2'b10: Forces the 8B10B encoding polarity to be negative 2'b11: Forces the 8B10B encoding polarity to be positive
TDISPSEL	
PCIe_EI	PCI Express electrical_idle indication, including PCIe_E1_H and PCIe_E1_L
TXH	TX header in the 64B66B/64B67B mode
TXQ	Sequence number in the 64B66B/64B67B mode

3.3.2 TX Bridge Unit Module

The TX Bridge unit module completes phase compensation from BRIDGE_TCLK to PCS_TCLK, with a FIFO depth of 8.

3.3.3 TX Gear Module

The TX gear module completes the interface rate adaptation for 64B66B or 64B67B in the TX direction. It supports the following data width modes for PCS and Fabric interfaces: 64B66B_16bit/64B67B_16bit and 64B66B_32bit/64B67B_32bit.

64B66B_16bit: Corresponds to the 64B66B encoded data, with Fabric interface bit width TX_DATA being 16bit;

64B66B_32bbit: Corresponds to the 64B66B encoded data, with Fabric interface bit width TX_DATA being 32bit.

64B67B_16bit: Corresponds to the 64B67B encoded data, with Fabric interface bit width TX_DATA being 16bit;

64B67B_32bbit: Corresponds to the 64B67B encoded data, with Fabric interface width TX_DATA being 32bit.

The timing diagrams are as follows, where

CLK_cycle: c0 to c69 represent the number of P_TX_CLK_FR_CORE clocks;

TXH: h0 to h15 correspond to the values of the first frame's TX header synchronization header, and H0 corresponds to the value of the first TX header synchronization header of the second frame.

TXQ: TX sequence number;

TXD: d0 to d63 represent the data of the first frame, and D0 represents the first data of the second frame.

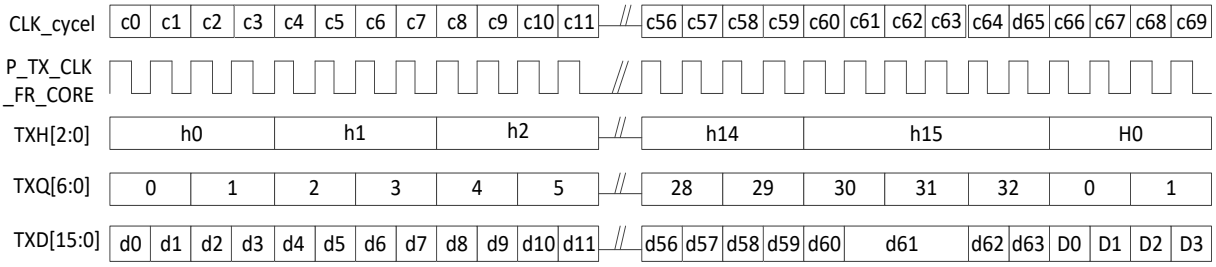

Figure 3-6 TX 64B66B_16bit Data Interface Timing Diagram

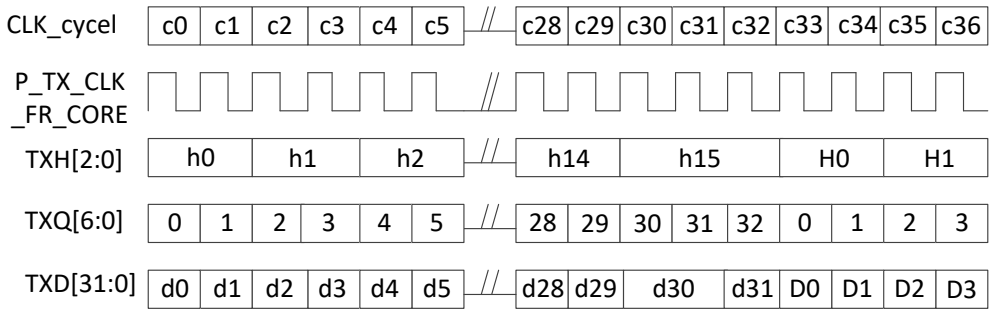

Figure 3-7 TX 64B66B_32bit Data Interface Timing Diagram

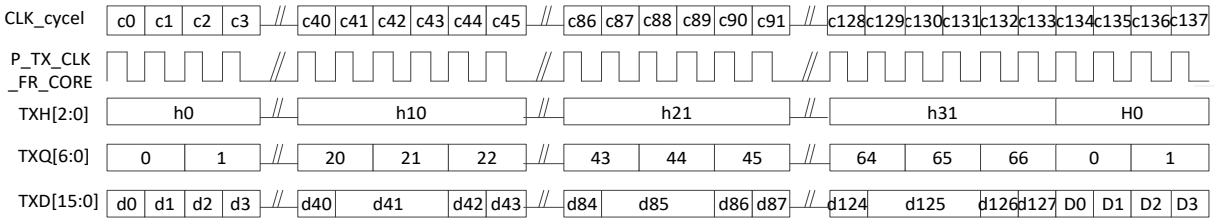

Figure 3-8 TX 64B67B_16bit Data Interface Timing Diagram

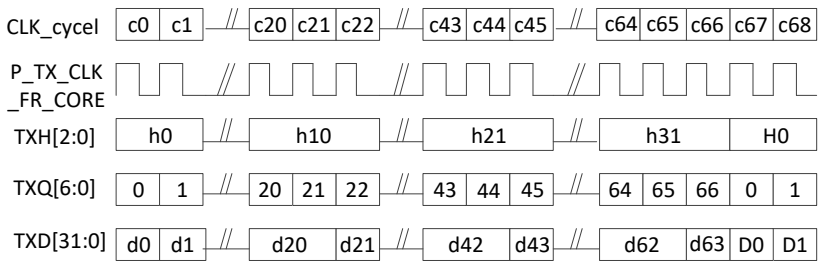

Figure 3-9 TX 64B67B_32bit Data Interface Timing Diagram

3.3.4 8B10B Encoder Module

Implements the 8B10B Encode function compliant with the IEEE 802.3 1000BASE-X Specification, refer to IEEE Std802.3 36.2 Physical Coding Sublayer (PCS) for details.

3.3.5 TX Bit Slip Module

The main function is to perform bit slip on transmission data according to configuration, to implement data transmission and reception delay consistency in applications such as CPRI. The number of Bits for Slip is set through the Parameter PCS_TX_BIT_SLIP_CYCLES.

The Slip function of the TX Bit Slip can operate under various data width modes. In 20bit only, 8B10B 16bit, 40bit only, and 8B10B 32bit modes, the TX Bit Slip can implement a 0~19bit slip, as shown in Figure 3-10:

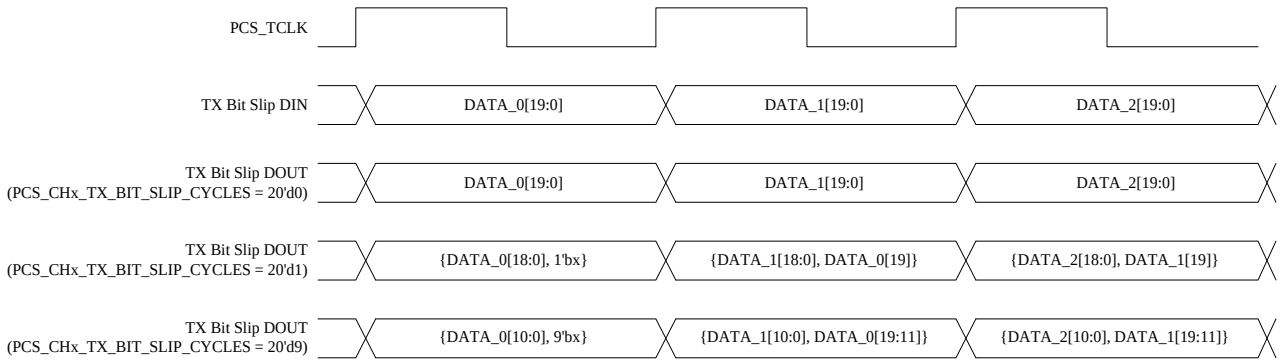

Figure 3-10 TX Bit Slip Module's 0~19bit Slip Functional Diagram

In 10bit only and 8B10B 8bit modes, the TX Bit Slip can implement a 0~9bit slip, as shown in Figure 3-11:

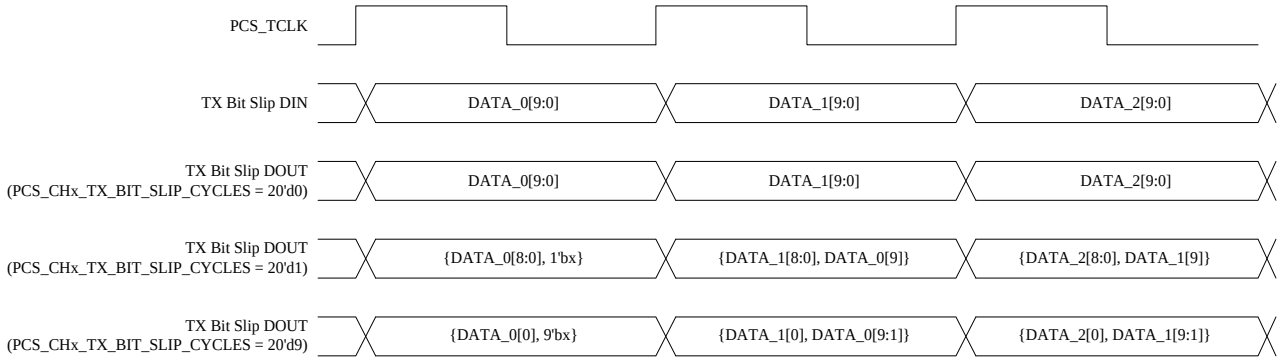

Figure 3-11 TX Bit Slip Module's 0~9bit Slip Functional Diagram

3.3.6 PRBS Generator Module

The PRBS Generator module generates various feature code streams, commonly used for PMA testing; users can select the required feature code stream through the Parameter PCS_TX_PRBS_MODE. The PRBS Generator module can operate in 8bit, 10bit, 16bit, and 20bit only modes.

Table 3-5 PRBS Generation Patterns

PCS_TX_PRBS_MODE Value	**Feature Code Stream**
“PRBS_7”	Generates random numbers based on the polynomial 1 + X6 + X7
“PRBS_15”	Generates random numbers based on the polynomial 1 + X14 + X15
“PRBS_23”	Generates random numbers based on the polynomial 1 + X18 + X23
“PRBS_31”	Generates random numbers based on the polynomial 1 + X28 + X31
“LONG_1”	Output all 1 signal
“LONG_0”	Output all 0 signal
“20UI”	Alternating transmission of 20bit 1s and 20bit 0s
“D10_2”	Outputs the sequence 20’b0101010101_0101010101; corresponding to D10.2 in 8B10B encoding
“PCIE”	Outputs PCI Express Compliance Pattern; i.e., alternating transmission of the sequence 20’b001111_1010_101010_1010 and the sequence 20’b110000_0101_010101_0101

Users can dynamically modify the PCS channel configuration parameter PCS_TX_INSERT_ER to insert error codes into the generated test code stream. With each transition of PCS_TX_INSERT_ER from 0 to 1, an error injection operation is performed, with a variable number of error bits injected.

The PRBS data of PCS and PMA have opposite polarities. Therefore, when docking the PRBS data of PMA and PCS, the PRBS data output by the PCS Generator must undergo PMA TX polarity inversion for proper docking. Additionally, polarity inversion should also be considered when docking with other devices. This is achieved by modifying the PMA_REG_TX_POLARITY register parameter.

3.3.7 TX Drive Reg Module

Completes data bridging from the PCS Transmitter to the PMA Transmitter, ensuring interface timing. The TX Drive Reg module can implement polarity inversion of the transmitted serial data and bit order inversion of parallel data based on the PCS and PMA interfaces through the PCS_TX_DRIVE_REG_MODE parameter.

When polarity inversion is enabled, the data ports P_TX_SDP and P_TX_SDN sent from the HSSTLP are exchanged with each other. When bit order inversion is enabled, the transmission data from the PCS Transmitter to the PMA Transmitter is inverted in bit order, that is:

For valid data of 8 bits, the data after bit order inversion is data_out[7:0]={data_in[0],data_in[1]…,data_in[7]}

For valid data of 10 bits, the data after bit order inversion is data_out[9:0]={data_in[0],data_in[1]…,data_in[9]}

For valid data of 16 bits, the data after bit order inversion is data_out[15:0]={data_in[0],data_in[1]…, data_in[15]}

For valid data of 20 bits, the data after bit order inversion is data_out[19:0]={data_in[0],data_in[1]…, data_in[19]}

3.4 PMA Transmitter Function

3.4.1 TX Digital Module

The TX Digital module mainly implements data bridging from PCS to PMA, including the following features:

- Processes control signals related to transmission;
- PRBS generator;
- Implements PMA Far-end parallel loopback;
- Selectable parallel data types to be transmitted to PMA;
- Data error injection;

3.4.2 Serializer Module

The main function of the Serializer is to convert the 20bits parallel data from TX Digital into serial data. Here, the 20bits refer to the parallel data width between PCS and PMA, which is part of the HSSTLP internal data width. The valid bit width of TX parallel data is controlled by the register PMA_REG_TX_BUSWIDTH, and the correspondence is as follows:

Table 3-6 Correspondence between TX Parallel Data Valid Bit Width and PMA_REG_TX_BUSWIDTH Register

PMA_REG_TX_BUSWIDTH	TX Parallel Data Valid Bit Width	Output data
2'b00	8bit	pma_txd<7:0> serialized output, higher bits discarded
2'b01	10bit	pma_txd<9:0> serialized output, higher bits discarded
2'b10	16bit	pma_txd<17:10>, pma_txd<7:0> serialized output, other bits discarded
2'b11	20bit	pma_txd<19:0> serialized output

3.4.3 Configurable TX Output Module

The output stage of TX adopts current mode to accommodate the needs of different protocols and scenarios, and it includes the following features:

- High-Speed Differential Current Mode Output;
- Configurable Output Magnitude;
- Pre- and Post-Cursor Configurable De-emphasis;
- Correctable Output Impedance;

The circuit architecture of the output stage is as follows:

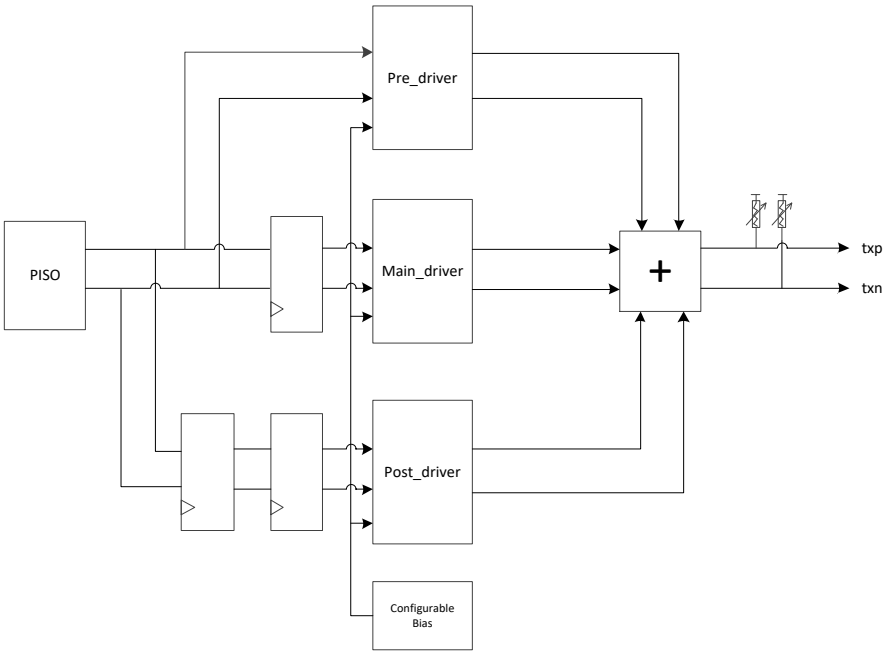

Figure 3-12 TX Output Stage Circuit Structure Diagram

3.4.4 PCI Express Receiver Detect Module

The PCIE protocol requires the PMA to be able to detect the receiver load at the transmitter to verify whether the link is established. The principle of load detection at transmitter is based on the rise time of the output signal, as shown below. During load detection, a capacitor greater than 100nF needs to be externally connected between TX output and RX input, and the RX input must be pulled down to the ground through a matching resistor. At the start of detection, TX output is first placed on the common-mode output, then the bias current of the TX drive stage is cut off. After a while, the TX output voltage is compared with the corresponding threshold voltage. If it is less than the threshold voltage, it indicates that the link is established; otherwise, the link is not established.

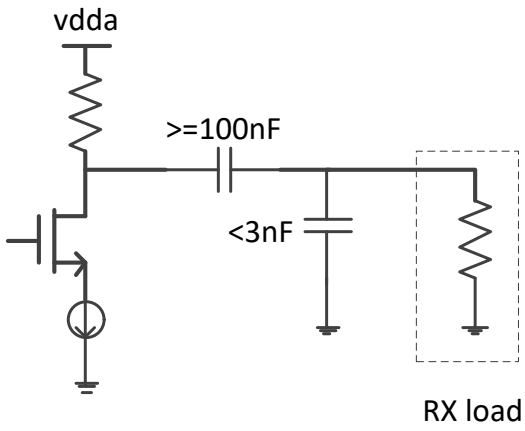

Figure 3-13 Schematic of Load Detection at Transmitter

Receiver detection is controlled by the register signal P_TX_RXDET_REQ, and the detection result is reflected by P_TX_RXDET_STATUS. The timing relationship between them is as follows.

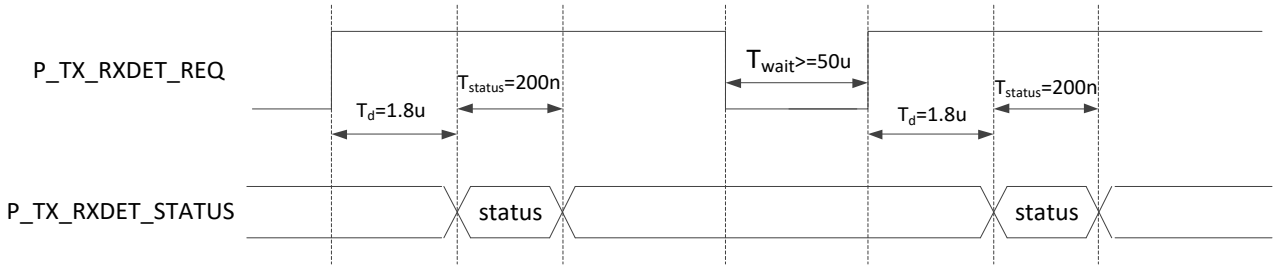

Figure 3-14 Timing Diagram of Load Detection at Transmitter

3.5 PCS Receiver Function

3.5.1 RX Sample Reg Module

Completes the data bridging from PMA Receiver to PCS Receiver, ensuring interface timing.

The RX Sample Reg module can implement polarity inversion of the received serial data by configuring the port signal parameter PCS_RX_POLARITY_INV[0]. Enabling polarity inversion compensates for the defect where HSSTLP data receiving ports P_RX_SDP and P_RX_SDN are incorrectly swapped in the PCB.

Through the parameter PCS_RX_POLARITY_INV[1], the RX Sample Reg module also supports bit order inversion of parallel data based on the PMA and PCS interfaces. When bit order inversion is enabled, the received data from the PMA Receiver to the PCS Receiver is inverted in bit order, that is:

For valid data of 8 bits, the data after bit order inversion is data_out[7:0]={data_in[0],data_in[1]…, data_in[7]}

For valid data of 10 bits, the data after bit order inversion is data_out[9:0]={data_in[0],data_in[1]…, data_in[9]}

For valid data of 16 bits, the data after bit order inversion is data_out[15:0]={data_in[0],data_in[1]…, data_in[15]}

For valid data of 20 bits, the data after bit order inversion is data_out[19:0]={data_in[0],data_in[1]…, data_in[19]}

3.5.2 Word Alignment Module

The main function of the Word Alignment module is to implement byte alignment according to a predefined pattern. For example, with a 10-bit data width, the parallel data of the transmitter is treated as one byte of 10 bits. After serial transmission, its byte boundary information is lost, so the parallel data produced after serial-to-parallel conversion in the PMA does not follow byte boundary rules. As shown in the following figure, the default bytes of parallel data before Word Alignment may be in a form where several bits have been slipped at the transmitter, with the number of slipped bits being random. The Word Alignment module utilizes certain characteristics of the transmission data stream to implement byte alignment, reverting it to the boundary consistent with the transmitter (refer to After Word Alignment in the figure).

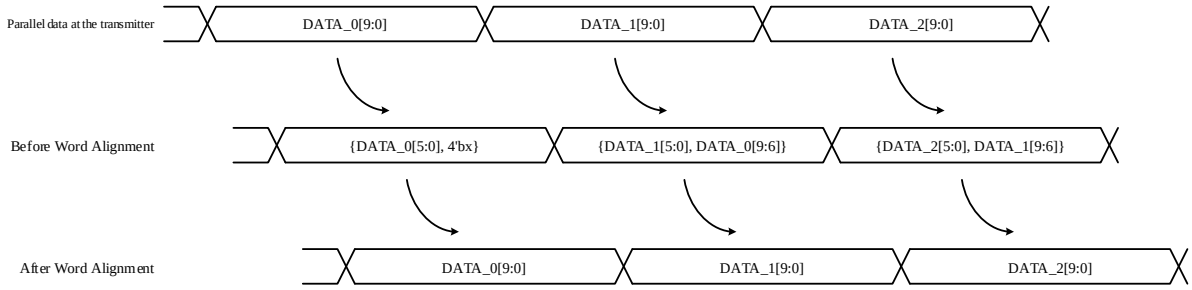

Figure 3-15 Description of Word Alignment Function

HSSTLP supports two Word Alignment modes: Comma-detection-based Word Alignment mode and RX CLK Slip-based Word Alignment mode. User logic selects the Word Alignment mode through the parameter PCS_COMMA_DET_MODE.

In the Comma-detection-based Word Alignment mode, the parameters PCS_COMMA_REG0 and PCS_COMMA_REG1 are used to specify the Comma detection patterns. For example, for K28.5 in the Special Data Group of 8B10B, PCS_COMMA_REG0/1 can be set to 10’b0101_1111_00 and 10’b1010_0000_11. The parameter PCS_COMMA_MASK masks the corresponding bits of the

parameter PCS_COMMA_REG0/1, thereby generating a Comma of less than 10 bits. In this mode, once the specified Comma is detected, the byte boundary adjustment is automatically completed.

In the RX CLK Slip-based Word Alignment mode, the byte boundary adjustment is implemented in the PMA Deserializer.

Word Alignment often requires a state machine to control the byte boundary adjustment to avoid incorrect adjustments due to line errors. HSSTLP supports internal Link State Machine or external Link State Machine. The supported internal Link State Machines include:

1. 1Gb Ethernet Link State Machine (802.3 “Figure 36–9—Synchronization state diagram”)
2. 10Gb Ethernet Link State Machine (802.3 “Figure 48–7—PCS synchronization state diagram”)
3. RapidIO Interconnect Specification Part 6 (Figure 4-15. Lane Alignment State Machine)

The Word Alignment state machine is selected by configuring the parameter PCS_ALIGN_MODE.

In the Comma-detection-based Word Alignment mode: If the internal Link State Machine is selected, HSSTLP will automatically complete the related Word Alignment, and the result of the alignment is output through the port signal P_PCS_LSM_SYNCED; if the external Link State Machine is selected, user logic can customize the Link State Machine, and enable byte realignment through the port P_PCS_WORD_ALIGN_EN.

3.5.3 8B10B Decoder Module

Implements the 8B10B Decode function compliant with the IEEE 802.3 1000BASE-X specification, refer to IEEE Std802.3 36.2 Physical Coding Sublayer (PCS) for details.

3.5.4 Channel Bonding Module

The main function of the Channel Bonding module is to implement byte alignment among multiple channels according to a predefined pattern. When multi-channel data is transmitted, the bytes between its channels are aligned. After parallel-to-serial conversion at the TX side, serial transmission on the board, and serial-to-parallel conversion at the RX side, the bytes between channels are no longer aligned after being processed by the Word Alignment module. As shown in the figure below, before Channel Bonding, there may be a skew of several bytes between the data of the channels. The Channel Bonding module leverages certain characteristics of the data stream to implement byte alignment between channels, reverting it to the boundary consistent with the transmitter (refer to After Channel Bonding in the figure).

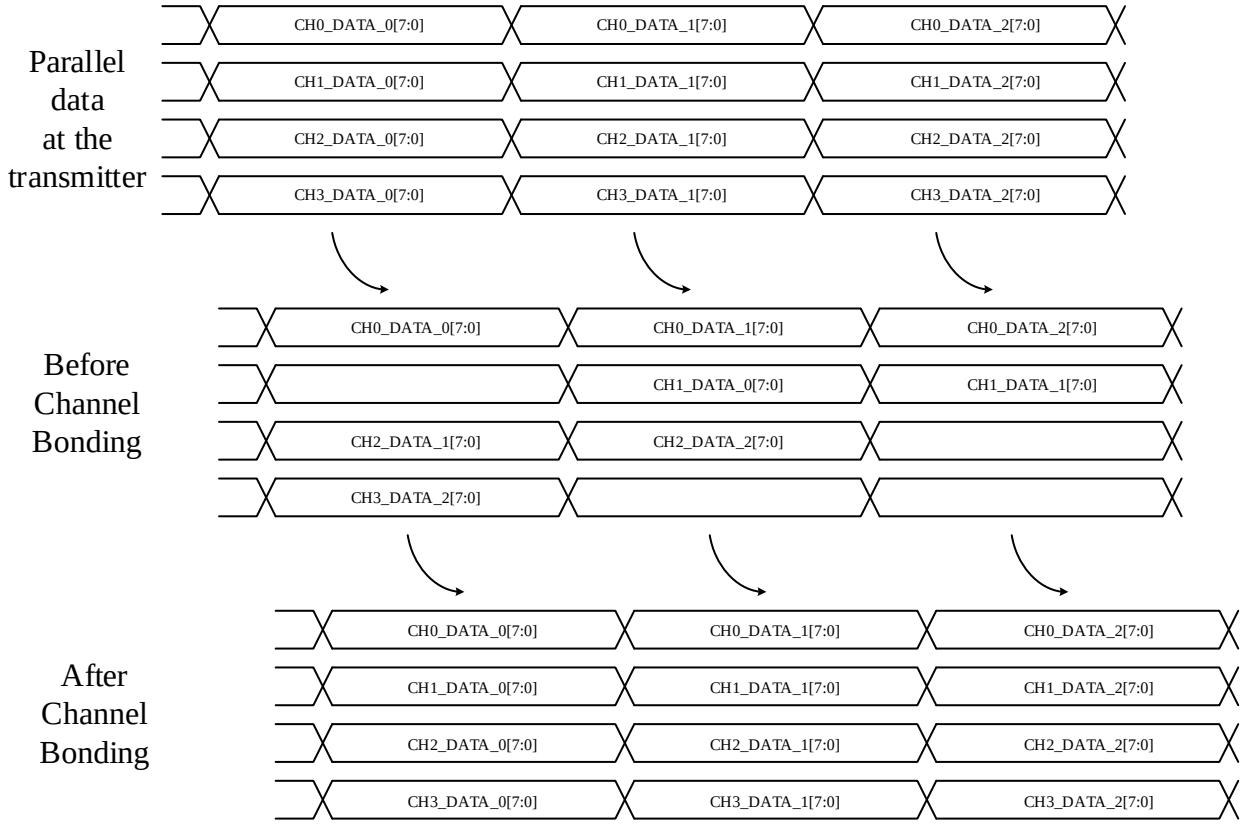

Figure 3-16 Channel Bonding Functional Diagram

Channel bonding is implemented by inserting the Special Codes into the data stream according to protocol requirements. Different protocols specify different Special Codes, which users can set using the parameter PCS_A_REG.

The Logos2 HSSTLP's Channel Bonding implements bonding between 2 Channels or 4 Channels, with a maximum Deskew capability of +/-80 bits, meeting the requirements of the supported protocols. For the bonding between two channels, only the bonding between Channel 0 and Channel 1 or between Channel 2 and Channel 3 is supported.

Channel Bonding often requires a state machine for control to avoid incorrect bonding adjustments due to line errors. The HSSTLP supports the internal Bonding State Machine or external Bonding State Machine. The supported internal Bonding State Machines include:

- Internal 10Gb XAUI Channel Bonding State Machine ("Figure 48–8—PCS Deskew State Diagram")
- Internal Rapid IO Channel Bonding State Machine ("Figure 4-15. Lane Alignment State Machine")

The Channel Bonding state machine is selected via the parameter PCS_CEB_MODE. If the internal Bonding State Machine is selected, the HSSTLP will automatically complete the related Channel Bonding, and the results will be output through the port signal P_PCS_RX_MCB_STATUS of the

Bonding Master Channel (with Channel 0/2 as the Bonding Master Channel for 2-Channel Bonding and Channel 0 as the Bonding Master Channel for 4-Channel Bonding). If the external Bonding State Machine is chosen, the user logic can customize the control of the state machine and enable the bonding process through the port P_PCS_MCB_EXT_EN.

3.5.5 CTC Module

The function of the CTC (Clock Tolerance Compensation) module is to compensate for minor frequency errors between the far-end clock and the local clock according to a predefined pattern (the frequency difference specified by the PCI Express protocol is +/-300ppm, and for other protocols, the number is typically +/-100ppm). The CTC module includes an asynchronous FIFO with a depth of 32, as shown in Figure 3-17, with the FIFO's write clock being CB_RCLK, which is derived from PMA_RCLK, and PMA_RCLK has been synchronized to the far-end transmit clock in the CDR module; the FIFO's read clock is AFTER_CTC_RCLK, which is derived from the local clock.

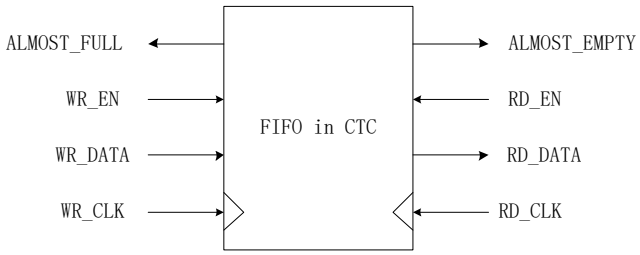

Figure 3-17 CTC Internal FIFO Diagram

When the write clock is faster than the read clock, the FIFO stauts line will gradually rise, and once it reaches a certain level, the stauts line flag signal ALMOST_FULL will be set high. At this point, the CTC will discard certain specific characters (or character sequences) before writing to the FIFO, thus preventing FIFO overflow. The specific characters (or character sequences) referred to here are called SKIP. As shown in Figure 3-18:

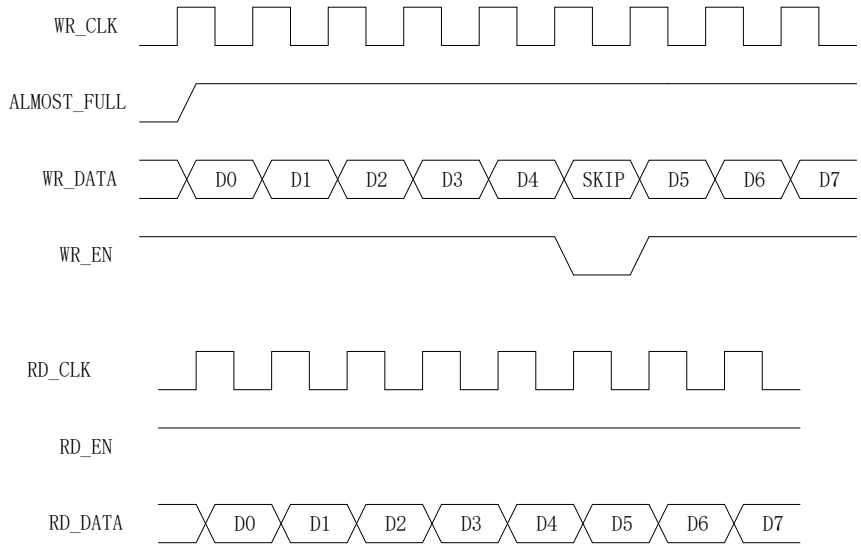

Figure 3-18 SKIP Delete Timing Diagram

When the write clock is slower than the read clock, the FIFO stauts line will gradually decrease, and once it reaches a certain level, the stauts line flag signal ALMOST_EMPTY will be set high. At this point, the CTC will pause FIFO reading upon detecting a specific character (or sequence of characters) and automatically insert a SKIP character to prevent FIFO read empty. As shown in Figure 3-19:

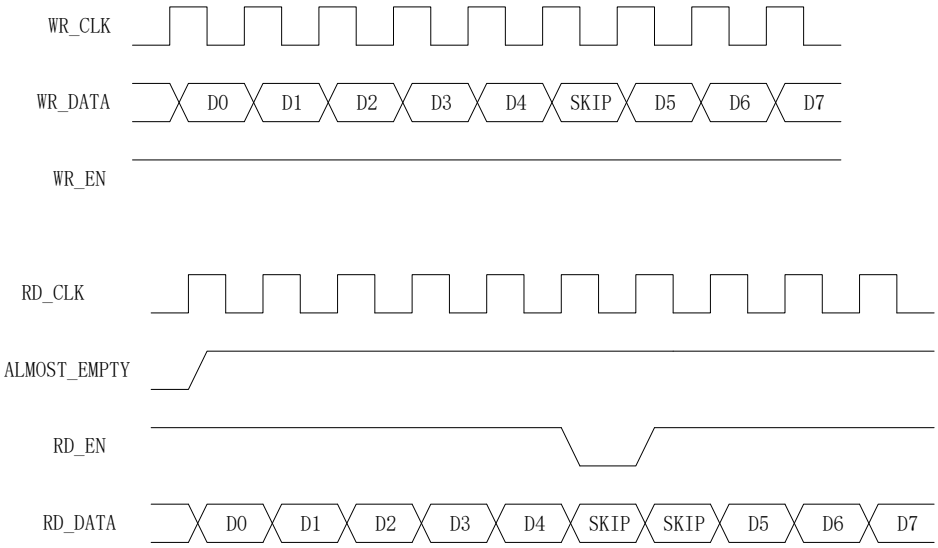

Figure 3-19 SKIP Add Timing Diagram

Different protocols define SKIP differently, and the CTC module in HSSTLP supports three types of SKIP lengths (selected by the parameter PCS_CTC_MODE):

- 1SKIP mode, set by the parameter PCS_SKIP_REG0, adds/deletes a SKIP character of 1 byte;
- 2SKIP mode, set by the parameters PCS_SKIP_REG0 and PCS_SKIP_REG1, adds/deletes a SKIP character of 2 bytes;

- PCIE_2BYTE mode, set by the parameters PCS_SKIP_REG0 and PCS_SKIP_REG1, only adds or deletes the subsequent SKIP;
- 4SKIP (PCIE_4BYTE) mode, set by Parameter PCS_SKIP_REG0, PCS_SKIP_REG1, PCS_SKIP_REG2, and PCS_SKIP_REG3. At this time, only the last byte of the SKIP sequence is added or deleted, but only the last byte of the SKIP character is added/deleted;

The Almost Full/Empty thresholds of the CTC FIFO can be modified according to application requirements, where: the Almost Full threshold is set by the parameter PCS_CTC_AFULL, with a default setting of 5'd20; the Almost Empty threshold is set by Parameter PCS_CTC_AEMPTY, with a default setting of 5'd12.

During the auto-negotiation of 1G Ethernet, both communicating parties continuously send /C/ characters, and no SKIP characters appear. Therefore, HSSTLP will automatically replace some /C/ characters with two /I2/ characters before the CTC operation to facilitate the CTC process. /I2/ will be used as the CTC's SKIP character. For detailed functions of /C/ and /I2/, refer to IEEE Std 802.3 36.2 Physical Coding Sublayer (PCS).

3.5.6 RX Gear Module

The RX gear module completes the interface rate adaptation for 64B66B or 64B67B in the RX direction, transparently transmitting the received RXD and RXH data. Users need to control the P_RXGEAR_SLIP port for bit slip to align data boundaries. The module supports the following data width modes for PCS and Fabric interfaces: 64B66B_16bit/64B67B_16bit and 64B66B_32bit/64B67B_32bit.

64B66B_16bit: Corresponds to the 64B66B encoded interface data, with the Fabric interface bit width P_RDATA being 16bit;

64B66B_32bit: Corresponds to the 64B66B encoded interface data, with the Fabric interface bit width P_RDATA being 32bit.

64B67B_16bit: Corresponds to the 64B67B encoded interface data, with the Fabric interface bit width P_RDATA being 16bit;

64B67B_32bit: Corresponds to the 64B67B encoded interface data, with the Fabric interface bit width P_RDATA being 32bit.

The timing diagrams are as follows, where

CLK_cycle: c0 to c69 indicate the number of P_RX_CLK_FR_CORE clocks;

RXH: h0 to h15 correspond to the values of the first frame's RX header synchronization header, and H0 corresponds to the value of the first RX header synchronization header of the second frame.

RXHVLD: RXH valid indication, where a high pulse indicates that the RXH value is valid;

RXQ_START: RXD data frame start indication, where a high pulse indicates the start of the data frame;

RXDVLD: RXD data valid indication, where a high pulse indicates that the RXD data is valid;

RXD: d0 to d63 represent the data of the first frame, and D0 represents the first data of the second frame.

P_RXGEAR_SLIP: This signal is not shown in the timing diagram. Users need to control the P_RXGEAR_SLIP port for bit slip to align data boundaries. The signal is edge-triggered, and either a rising or falling edge detected will cause a slip of 1 bit. It is also an asynchronous signal and is synchronized internally by the PCS.

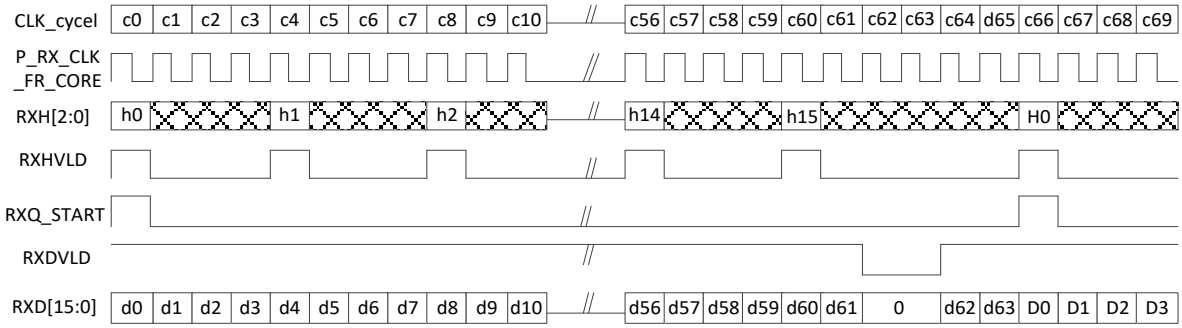

Figure 3-20 RX 64B66B_16bit Data Interface Timing Diagram

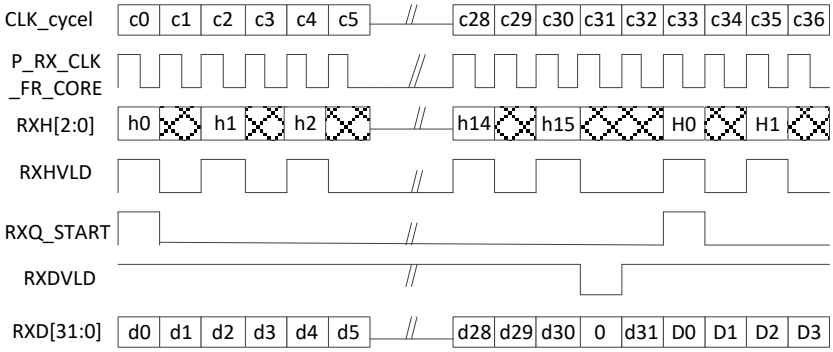

Figure 3-21 RX 64B66B_32bit Data Interface Timing Diagram

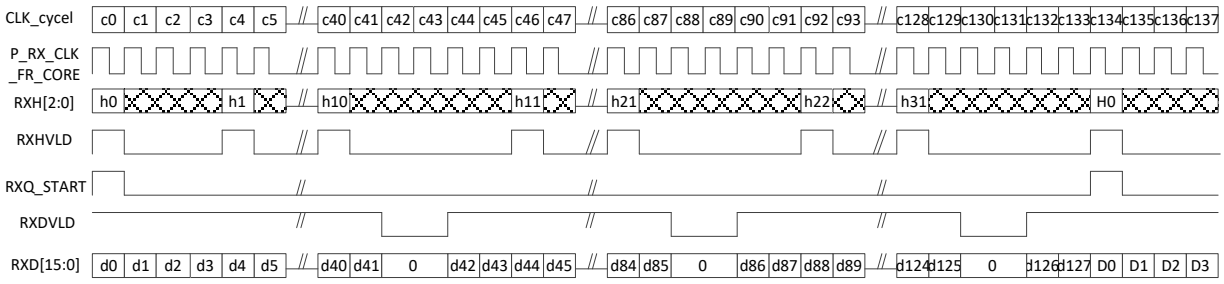

Figure 3-22 RX 64B67B_16bit Data Interface Timing Diagram

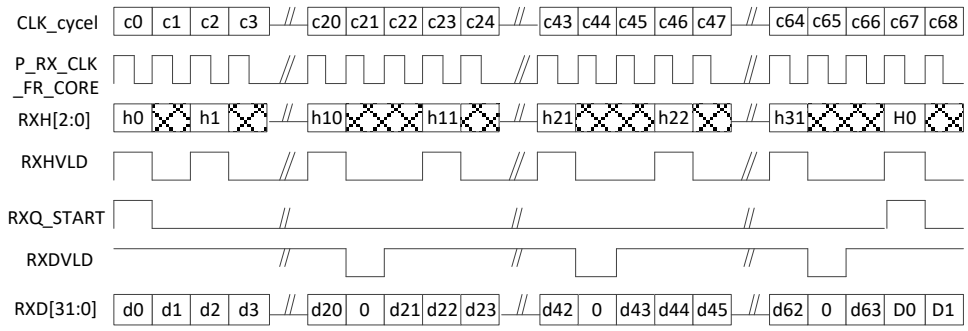

Figure 3-23 RX 64B67B_32bit Data Interface Timing Diagram

3.5.7 RX Bridge Unit Module

The RX Bridge unit module completes phase compensation from AFTER_CTC_RCLK to BRIDGE_RCLK, with a FIFO depth of 8.

3.5.8 RX Bridge Reg Module

It completes the received data bridging from HSSTLP to Fabric, ensuring interface timing. Each LANE's data receiving port P_RDATA has 47 bits, with definitions varying according to different data width modes, refer to Table 3-7:

Table 3-7 LANE Reception Data Definitions

	P_RDATA_x Data Bits																				
Data Width Modes	[46:44]	[43]	[42]	[41]	[40:39]	[38]	[37:33]	[32]	[31]	[30]	[29:22]	[21]	[20]	[19]	[18:17]	[16]	[15:11]	[10]	[9]	[8]	[7:0]
8bit only	RX STATUS	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	RXD [7:0]
10bit only	RX STATUS	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	RXD [9:0]		
8B10B 8bit	RX STATUS	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	RXK	RDEC_ER	RDISP_ER	RXD [7:0]
16bit only	RX STATUS	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	RXD [15:10]		NA	RXD [9:0]		
20bit only	RX STATUS	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	RXD [19:10]					NA	RXD [9:0]		
8B10B 16bit	RX STATUS	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	RXK [1]	RDEC_ER [1]	RDISP_ER [1]	RXD [15:8]			RXK [0]	RDEC_ER [0]	RDISP_ER [0]	RXD [7:0]
32bit only	RX STATUS	NA	NA	NA	NA	RXD [31:26]		NA	RXD [25:16]			NA	NA	NA	NA	RXD [15:10]		NA	RXD [9:0]		
40bit only	RX STATUS	NA	RXD [39:30]					NA	RXD [29:20]			NA	RXD [19:10]					NA	RXD [9:0]		
8B10B 32bit	RX STATUS	RXK [3]	RDEC_ER [3]	RDISP_ER [3]	RXD [31:24]			RXK [2]	RDEC_ER [2]	RDISP_ER [2]	RXD [23:16]	RXK [1]	RDEC_ER [1]	RDISP_ER [1]	RXD [15:8]			RXK [0]	RDEC_ER [0]	RDISP_ER [0]	RXD [7:0]
64b 66b 16bit	RX STATUS	NA										RXQ_START	RXHVLD	RXH[2:0]		RXDVLD	RXD[15:0]				
64b 66b 32bit	RX STATUS	NA				RXD[31:16]						RXQ_START	RXHVLD	RXH[2:0]		RXDVLD	RXD[15:0]				

Wherein, the definition of the data bits is shown in Table 3-8:

Table 3-8 Definitions of Data Bits in P_RDATA_x

Data Bit Name	Description
RXK	1 indicates that RXD is the 8B10B Special Code-Groups compliant with the IEEE 802.3 1000BASE-X Specification; 0 indicates that RXD is the 8B10B Data Code-Groups compliant with the IEEE 802.3 1000BASE-X Specification;
RXD	Code-Groups
RDEC_ER	A high level indicates that the 8B10B Decoder has detected an Invalid Code
RDISP_ER	A high level indicates that the 8B10B Decoder has detected an Invalid Disparity
RXSTATUS	Reception status encoding for the PCI Express PHY Interface (PIPE) 3'b000: Normal 3'b001: The CTC module executed a SKIP add operation 3'b010: The CTC module executed a SKIP delete operation 3'b011: PCIe 4byte mode. The CTC module executed continous SKIP operation 3'b100: Reserved 3'b101: CTC FIFO Over Flow 3'b110: CTC FIFO Under Flow 3'b111: Reserved
RXQ_START	RXsequence start indicator in the 64B66B mode
RXH	RX header synchronization header in the 64B66B/64B67B mode
RXHVLD	The valid indicator of RX header synchronization header in the 64B66B/64B67B mode
RXDVLD	The valid indicator of RX data reception data in the 64B66B/64B67B mode

3.5.9 PRBS Checker Module

The PRBS Checker module automatically detects various feature code streams, commonly used for HSSTLP line error code testing. Users can select the required feature code stream through the parameter PCS_RX_PRBS_MODE. The supported options include:

Table 3-9 PRBS Checker Pattern

PCS_RX_PRBS_MODE	Feature Code Stream
"PRBS_7"	Generates random numbers based on the polynomial 1 + X6 + X7
"PRBS_15"	Generates random numbers based on the polynomial 1 + X14 + X15
"PRBS_23"	Generates random numbers based on the polynomial 1 + X18 + X23
"PRBS_31"	Generates random numbers based on the polynomial 1 + X28 + X31

The error count detected by the PRBS Checker can be obtained by reading the configuration register PCS_ERR_CNT, and user logic can clear the error counter by the register PCS_RX_ERRCNT_CLR.

The PRBS data of PCS and PMA have opposite polarities. Therefore, when docking the PRBS of PMA and PCS, the PCS Checker needs to perform polarity inversion at the PMA RX end for proper

docking. Additionally, polarity inversion should also be considered when docking with other devices. This is achieved by modifying the PMA_REG_RX_DATA_POLARITY register.

3.6 PMA Receiver Function

3.6.1 Receiver Front-end Module

The RX receiver is a differential current mode input, including the following features:

- Configurable AC or DC coupling is available. Generally, it is recommended to use external AC and internal DC coupling (PCIe requires external AC and internal AC coupling);
- Configurable RX termination voltage;
- Adjustable matching resistor;

The structure is shown in Figure 3-24.

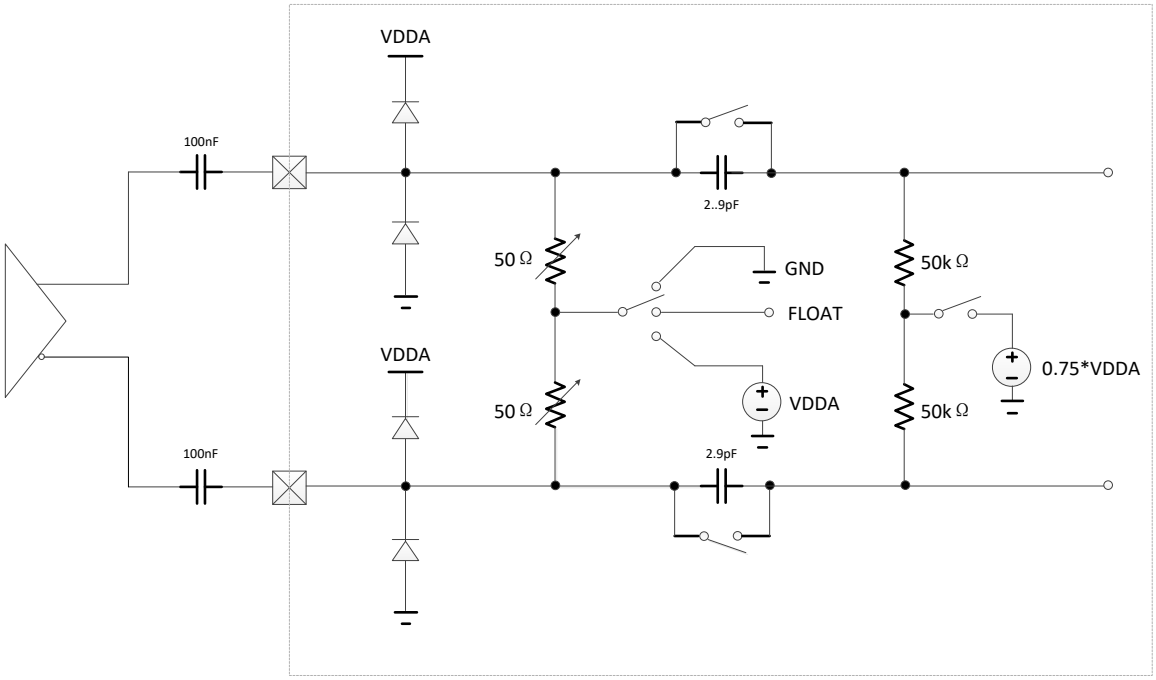

Figure 3-24 RX Receiver Structure Diagram

3.6.2 LEQ Module

The LEQ (Linear Equalizer) module is an adaptive linear equalizer at the receiver, used to compensate for high-frequency losses in the received signal. LEQ supports maximum channel attenuation compensation of approximately 15dB at 6.6Gb/s (at Nyquist frequency point).

3.6.3 CDR Module

The main function of the CDR is to recover clock information from the data, thereby recovering the correct data. The RX's CDR is based on a phase interpolation architecture, with its clock source being derived from the common clock PLL. The overall architecture is shown in Figure 3-25.

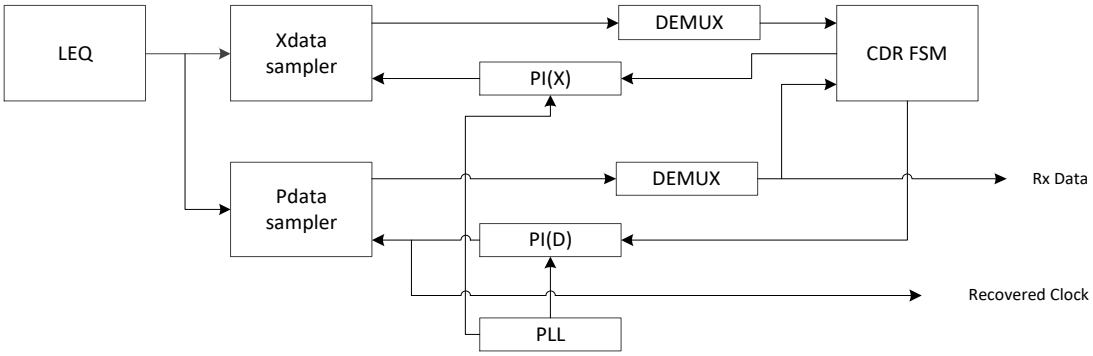

Figure 3-25 Overall CDR Architecture

After passing through the LEQ, the data goes through edge samplers and data samplers, with the sampler's clock being derived from the PI's output. The two sets of data are then processed in the CDR state machine after DEMUX processing. The CDR state machine determines the phase information by comparing the edge signal and the data signal, and then outputs control signals to control the clock, ultimately aligning the sampling clock of the data signal to the middle of the data.

3.6.4 LOS Detect Module

LOS Detect detects whether there is a valid signal at the receiving port, and the result is transmitted to Fabric through the status register PMA_REG_RX_SIGDET_STATUS. A high level indicates that the LOS Detect module has detected a valid signal via the receiving port.

3.6.5 Deserializer Module

The main function of the Deserializer is to convert PMA's high-speed serial data into 20 bits of parallel data to be sent to RX Digital. Here, the 20 bits refer to the parallel data width between the PMA Receiver and the PCS Receiver, which is part of the HSSTLP internal interface. The valid bit width of the RX parallel data is controlled by the parameter PMA_REG_RX_BUSWIDTH, and their correspondence is as follows:

Table 3-10 Correspondence between RX Parallel Data Valid Bit Width and Register PMA_REG_RX_BUSWIDTH

PMA_REG_RX_BUSWIDTH	RX Parallel Data Valid Bit Width	Output data
2'b00	8bit	pma_rxd<7:0> parallel output, higher data bits invalid
2'b01	10bit	pma_rxd<9:0> parallel output, higher data bits invalid
2'b10	16bit	pma_rxd<17:10>, pma_rxd<7:0> parallel output, other data bits invalid
2'b11	20bit	pma_rxd<19:0> parallel output

Additionally, the Deserializer module supports the RX CLK Slip function to ensure a fixed RX Latency. In the circuit, this is achieved through the PMA_REG_RXPCLK_SLIP register. Each time there is a rising edge of the PMA_REG_RXPCLK_SLIP signal, the PMA's parallel output clock PMA_RCLK will be delayed by one UI. If multiple UIs need to be delayed, there must be an equivalent number of rising edges on the PMA_REG_RXPCLK_SLIP signal. The maximum UI delay depends on the bit width of the parallel data (for example, if the bit width is N, then the parallel clock can move by up to N-1 UIs). The pulse duration of PMA_REG_RXPCLK_SLIP must be at least 20 UIs to ensure the correct response of the circuit.

3.6.6 RX Digital Module

The RX Digital module mainly completes the data bridging from the PMA Receiver to the PCS Receiver, including the following functions:

- Processing of the received control signals;
- PRBS checker;
- Implements PMA Far-end parallel loopback;
- Errors are forced in received data;
- Signal detect, OOB detect;

3.7 Loopback Function

HSSTLP supports multiple loopback modes for testing, including PCS Near-end loopback, PMANear-end parallel loopback, PMA Near-end serial loopback, PMA Far-end parallel loopback, and PCS Far-end loopback.

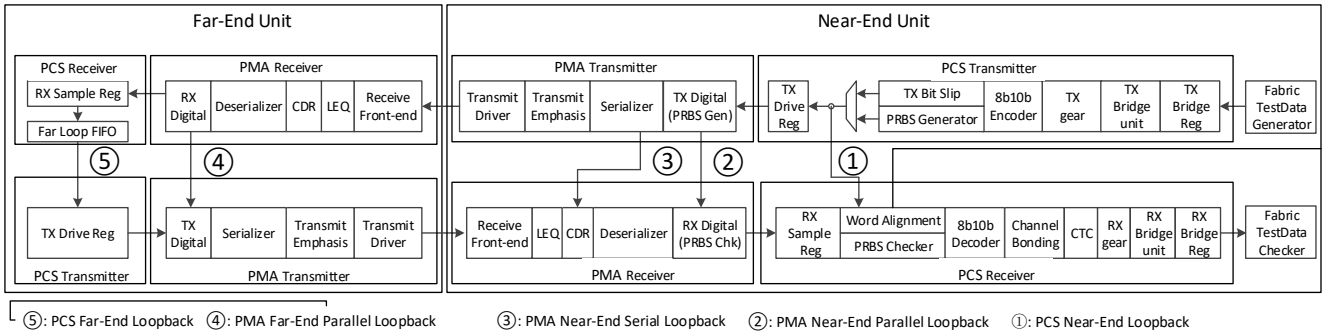

Figure 3-26 HSSTLP Loopback Mode Data Path Overview

3.7.1 PCS Near-End Loopback

PCS near-end loopback is implemented in the PCS, where the transmission data from Fabric passes through the TX Bit Slip module in the PCS Transmitter, loops back to the Word Alignment module, and then loops back out to Fabric through the PCS Receiver's RX Bridge Reg module, as shown in the figure below.

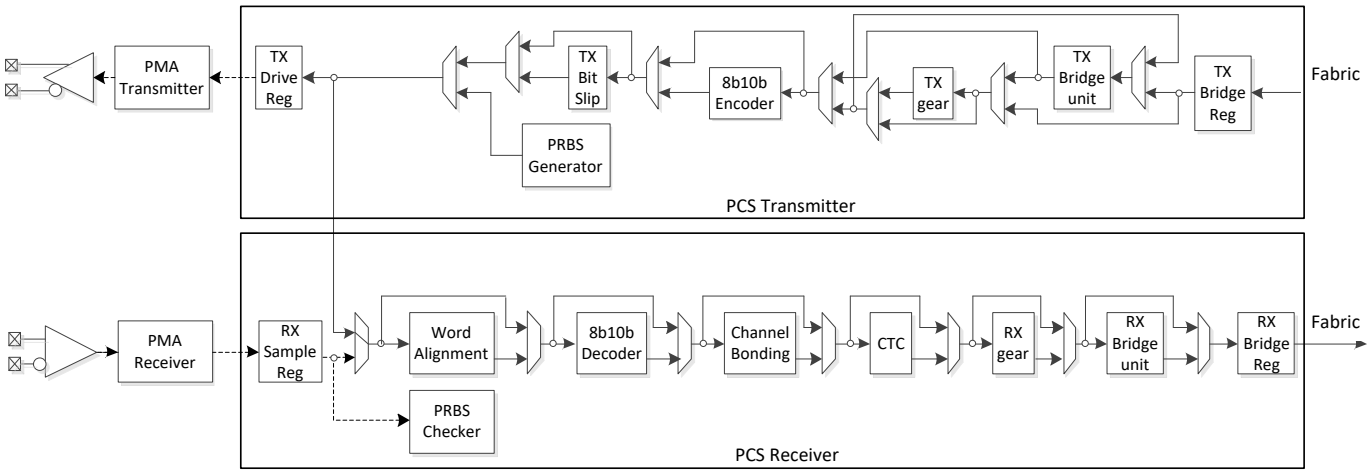

Figure 3-27 PCS Near-End Loopback Data Path Diagram

The register configuration method for PCS near-end loopback is as follows:

1. PCS_CHx_NEAR_LOOP="TRUE"

3.7.2 PMA Near-End Parallel Loopback

PMA Near-end parallel loopback is implemented in the PMA, where the parallel data from the PCS Transmitter passes through the PMA TX Digital module, loops back to the PMA RX Digital module, and finally loops back to the PCS, as shown in the figure below.

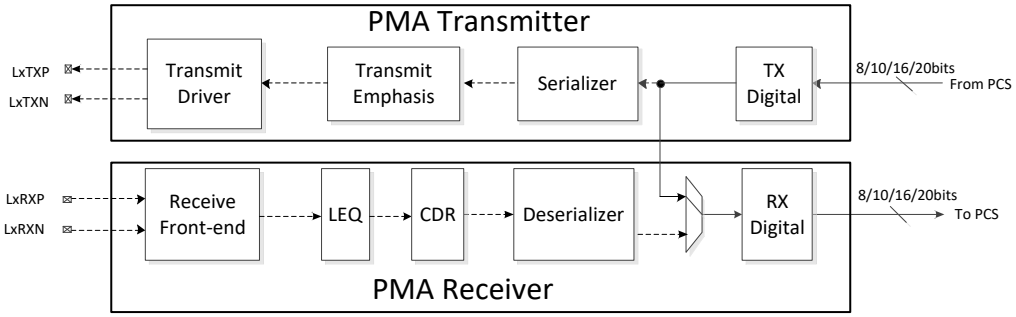

Figure 3-28 PMA Near-End Parallel Loopback Data Path Diagram

The register configuration method for PMA Near-end parallel loopback is as follows:

1. PMA_CHx_REG_RX_TX2RX_PLPBK_EN="TRUE"

3.7.3 PMA Near-End Serial Loopback

PMA near-end serial loopback is implemented in the PMA, where the parallel data from the PCS Transmitter goes through parallel-to-serial conversion, loops back to the PMA Receiver's CDR module, and finally loops back to the PCS through serial-to-parallel conversion, as shown in the figure below.

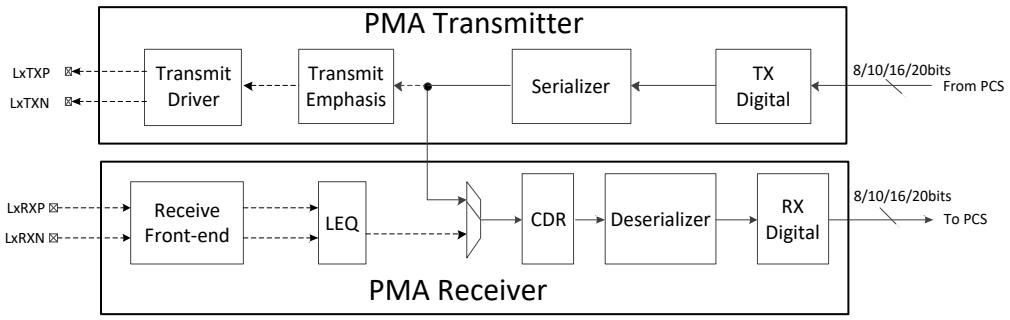

Figure 3-29 PMA Near-End Serial Loopback Data Path Diagram

The register configuration method for PMA near-end serial loopback is as follows:

1. PMA_CHx_REG_TX_TX2RX_SLPBACK_EN="TRUE"

3.7.4 PMA Far-End Parallel Loopback

PMA Far-end parallel loopback is implemented in the PMA, where the received data is sampled and converted to parallel data by PMA, then passes through the PMA RX Digital module, loops back to the PMA TX Digital module, and finally loops back out through the PMA, as shown in the figure below.

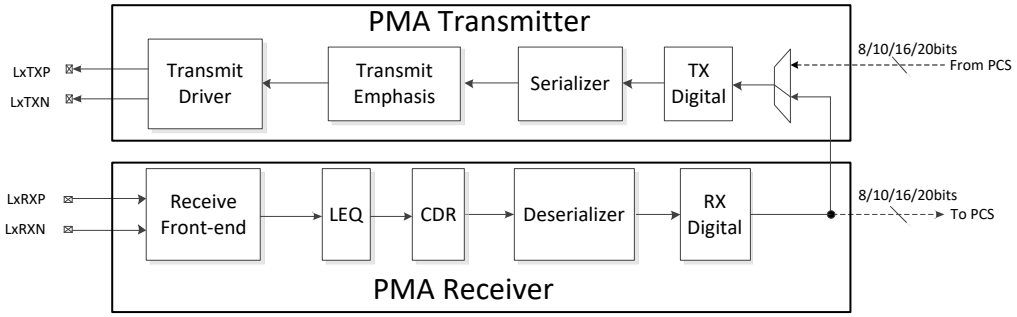

Figure 3-30 PMA Far-End Parallel Loopback Data Path Diagram

The register configuration method for PMA Far-end parallel loopback is as follows:

1. PMA_CHx_REG_TX_DATA_MUX_SEL=3
2. PMA_CHx_REG_TX_FIFO_EN="TRUE"
3. PMA_CHx_REG_PLPBK_TXPCLK_EN="TRUE"

3.7.5 PCS Far-End Loopback

PCS Far-end parallel loopback is implemented in the PCS, where the received data is sampled and converted to parallel data by PMA. After passing through the RX Sample Reg module, it loops back to the TX Drive Reg module via an asynchronous FIFO with a depth of 8 (used to compensate for phase differences between PCS_RCLK and PCS_TCLK), and then loops back out through the PMA, as shown in the figure below.

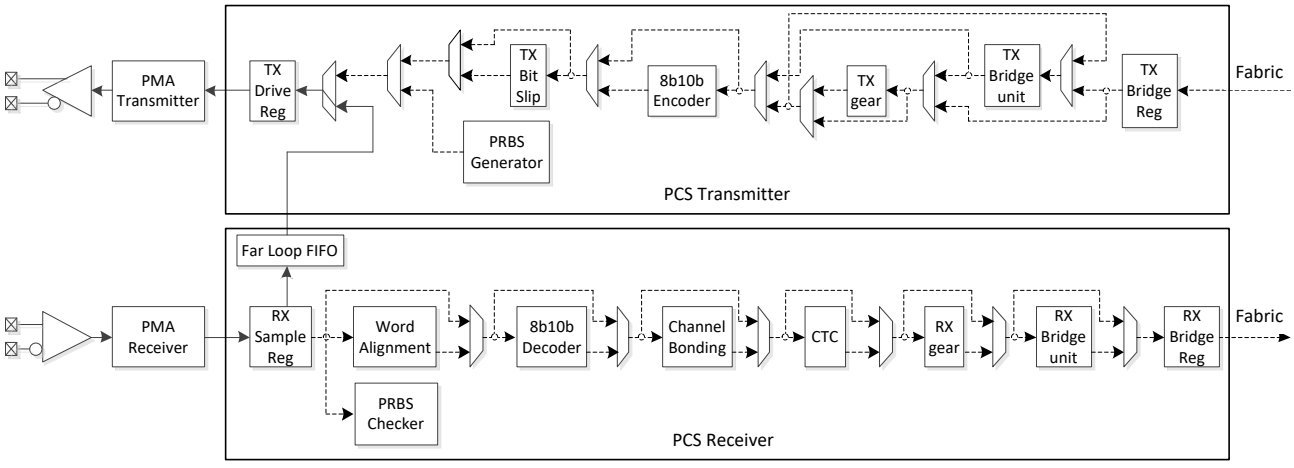

Figure 3-31 PCS Far-End Loopback Data Path Diagram

The register configuration method for PCS far-end loopback is as follows:

1. PCS_CHx_FAR_LOOP="TRUE"
2. PMA_CHx_REG_PLPBK_TXPCLK_EN="TRUE"

3. PCS_ CHx_CB_RCLK_SEL=“ PMA_TCLK”

3.8 Configuration Register Interface

HSSTLP is generally configured through the parameter GTP_HSSTLP. To meet debugging requirements, HSSTLP also supports a dynamic configuration interface similar to APB. The data width of the dynamic configuration interface is 8 bits, and its read and write timing is shown below.

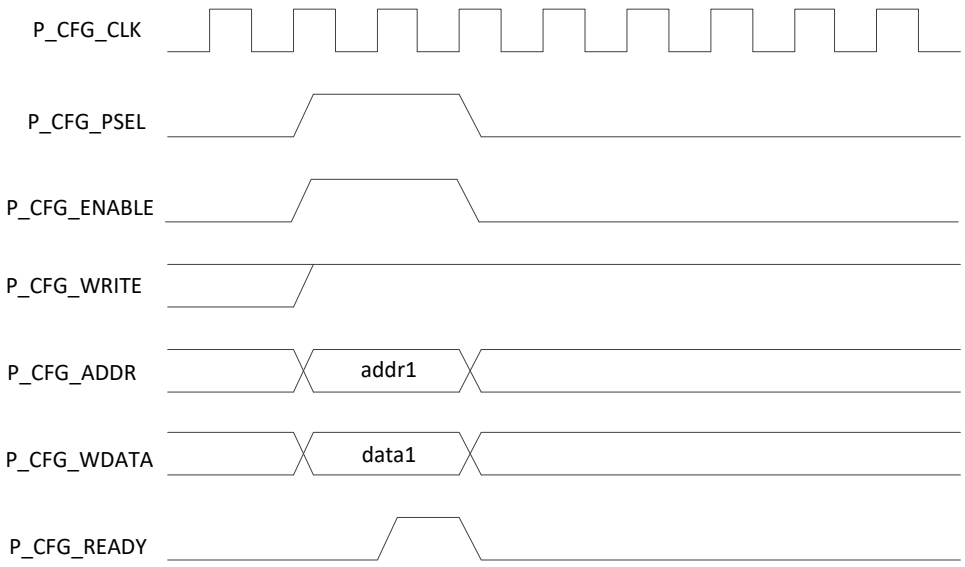

Figure 3-32 HSSTLP Dynamic Configuration Interface Write Timing Diagram

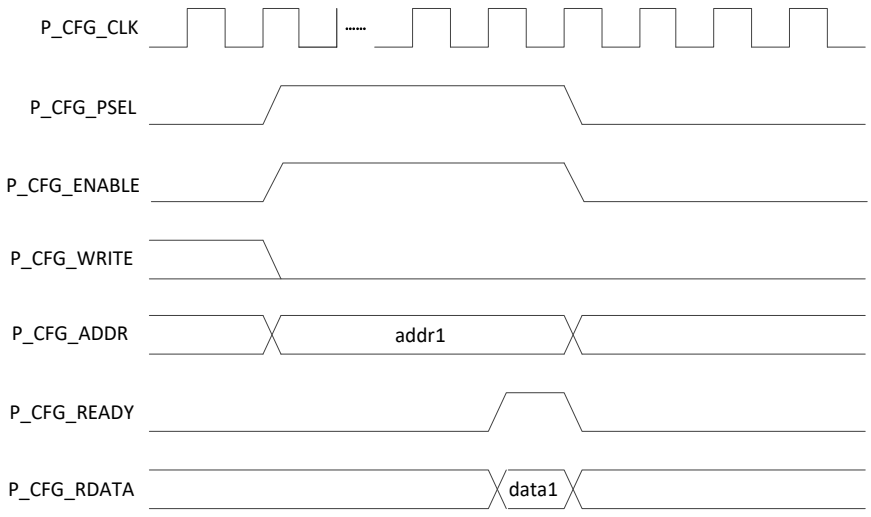

Figure 3-33 HSSTLP Dynamic Configuration Interface Read Timing Diagram

Chapter 4 Reset Sequence for HSSTLP

4.1 PLL Reset Timing

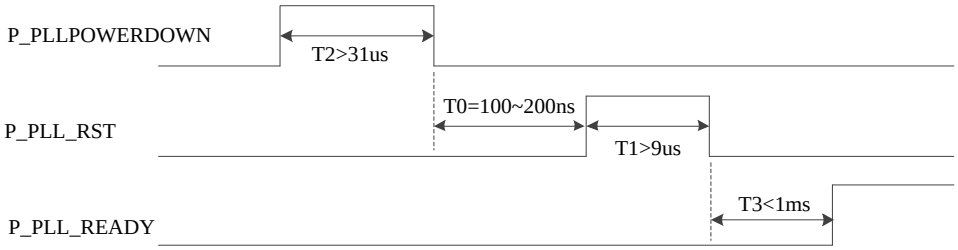

Figure 4-1 PLL Reset Timing Diagram

When the PLL is working, first the P_PLLPOWERDOWN changes from high level to low level, then waits for 100–200ns, the P_PLL_RST port is reset, the high level pulse time of the reset is longer than 9μs, and then waits for the P_PLL_READY port to transition to a high level, then the PLL is phase-locked.

When the PLL is not working, P_PLLPOWERDOWN is at a high level, and P_PLL_RST is at a low level. Before the next PLL operation, it must be ensured that the high level time of P_PLLPOWERDOWN is longer than 31μs.

P_PLLPOWERDOWN is kept low during normal operation, only P_PLL_RST needs to be operated for PLL reset.

4.2 Timing of Power-up Reset in Transmit Direction

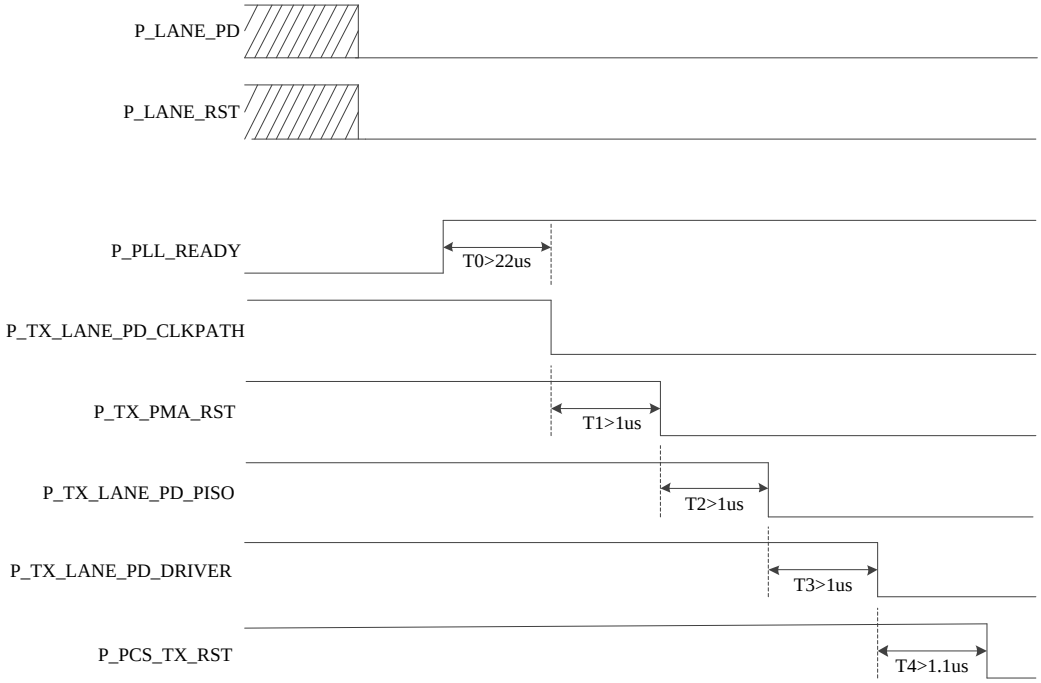

Figure 4-2 Timing Diagram of Power-up Reset in the Transmit Direction

Before P_TX_LANE_PD_CLKPATH transitions from a high level to a low level, P_LANE_PD and P_LANE_RST need to transition to a low level, and P_PLL_READY should be at a high level for more than 22μs (i.e., PLL lock).

After P_TX_LANE_PD_CLKPATH becomes low, P_TX_PMA_RST needs to wait for more than 1μs before it is released (i.e., transitioning from high to low).

After P_TX_PMA_RST becomes low, P_TX_LANE_PD_PISO needs to wait for more than 1μs before it is released (i.e., transitioning from high to low).

After P_TX_LANE_PD_PISO becomes low, P_TX_LANE_PD_DRIVER needs to wait for more than 1μs before it is released (i.e., transitioning from high to low).

After P_TX_LANE_PD_DRIVER becomes low, P_PCS_TX_RST needs to wait for more than 1.1μs before it is released (i.e., transitioning from high to low).

The synchronous timing diagram for dynamic rate switching in the transmit direction by changing P_TX_RATE is shown in the figure below. In the diagram, PCIe_EI is the indicator of PCI Express electrical_idle, which includes PCIe_E1_H and PCIe_E1_L, defined by bits P_TDATA[45:44]. During synchronous timing control, PCIe_E1_H and PCIe_E1_L both produce the same PCIe_EI control timing.

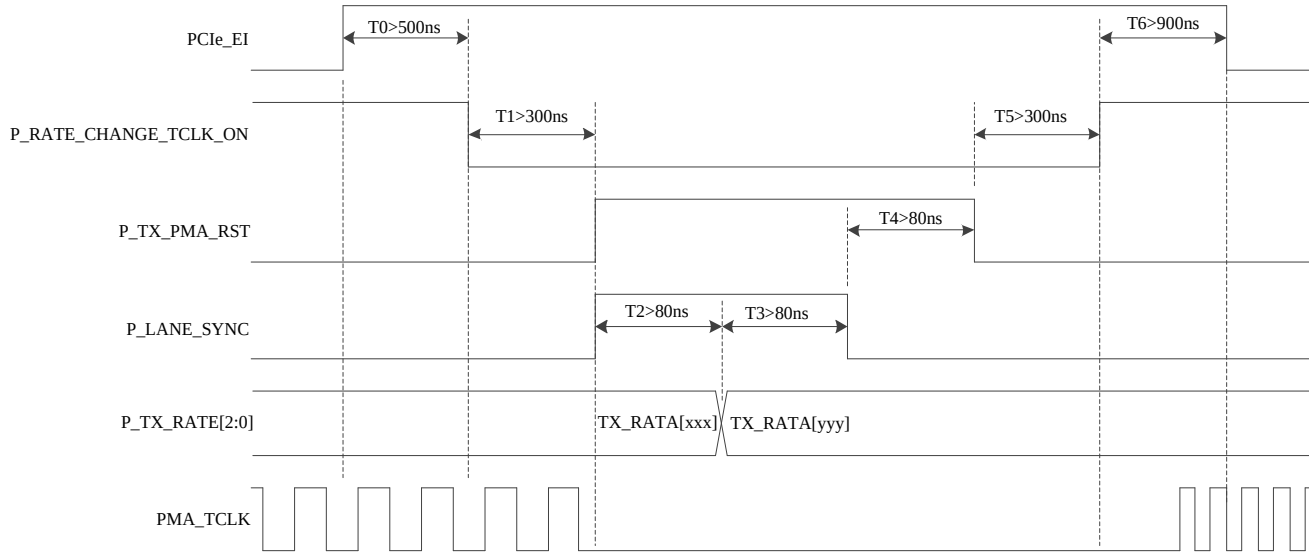

Figure 4-3 Timing Diagram of Dynamic Rate Switching in the Transmit Direction

When the dynamic rate switching in the transmit direction is performed by changing P_TX_RATE, the PLL will not be unlocked, so there is no need to reset P_PCS_TX_RST again.

If it is necessary to implement the transmit direction rate switching by modifying PLL configuration parameters, then the TX reset timing operation needs to be performed again. Refer to Figure 4-6.

4.3 Timing of Power-up Reset in the Receive Direction

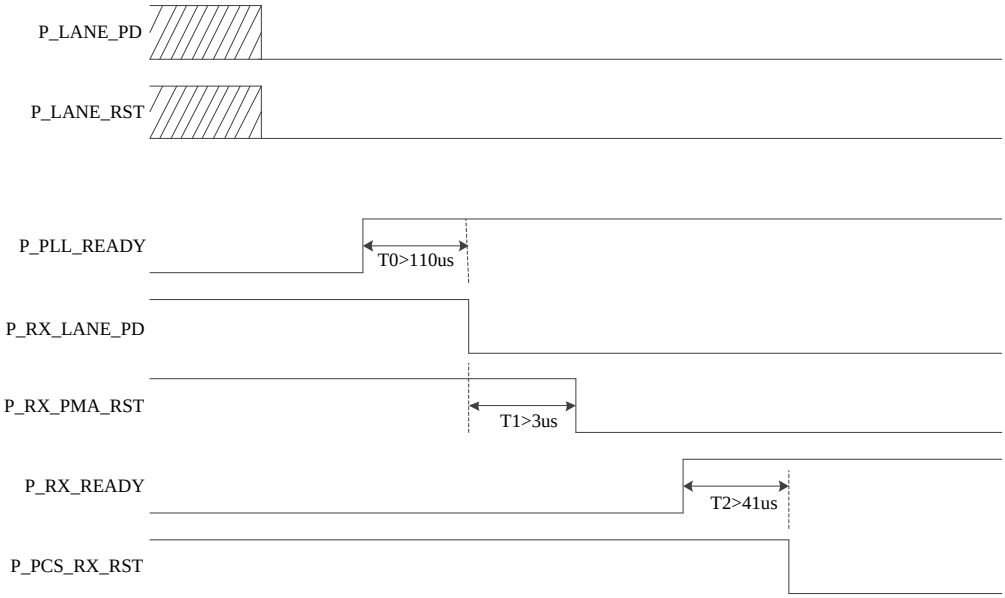

Figure 4-4 Timing Diagram of Power-up Reset in the Receive Direction

Before P_RX_LANE_PD transitions from a high level to a low level, P_LANE_PD and P_LANE_RST need to transition to a low level, and P_PLL_READY should be at a high level for more than 110μs (i.e., PLL lock).

After P_RX_LANE_PD becomes low, P_RX_PMA_RST needs to wait for more than 3μs before releasing (i.e., transitioning from high to low).

After the valid data arrives, the CDR starts the tracking lock process. When P_RX_READY is detected to become high, it indicates that the CDR has completed locking. If the data is interrupted, the CDR will be automatically reset, and P_RX_READY will become low. After the valid data arrives again, the CDR restart the tracking lock process.

After the valid data arrives, then P_RX_READY becomes high level, P_PCS_RX_RST needs to wait for more than 41μs before it is released (i.e., transitioning from high to low).

When RX is powered down during normal operation, it requires at least 110μs to ensure all modules are turned off.

The synchronous timing for dynamic rate switching in the receive direction by changing P_RX_RATE is shown in the figure below.

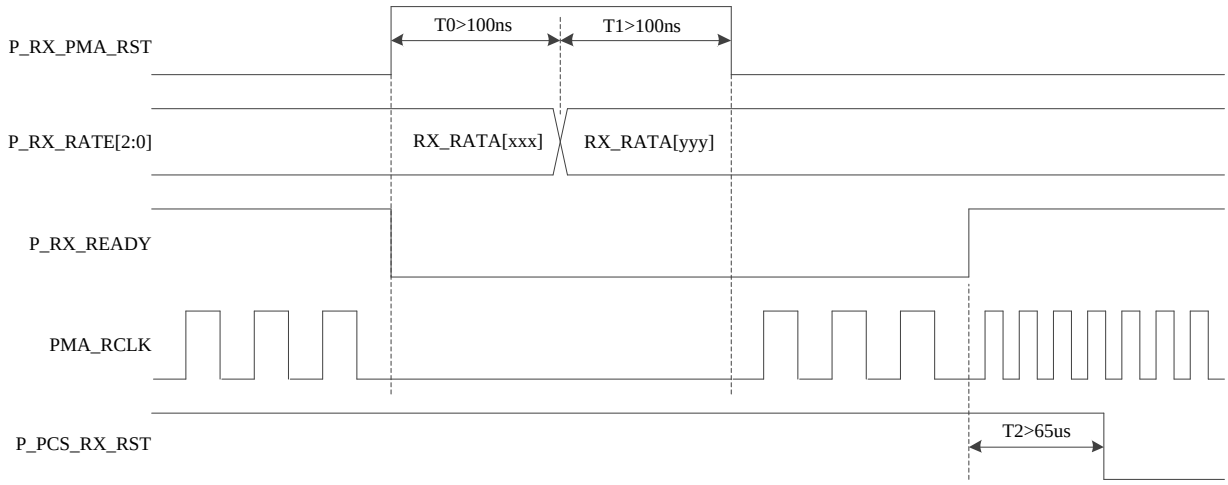

Figure 4-5 Timing Diagram of Dynamic Rate Switching in the Receive Direction

When the dynamic rate switching in the receive direction is performed by changing P_RX_RATE, it involves CDR re-locking, so P_PCS_RX_RST needs to be reset again.

If it is necessary to implement the receiving direction rate switching by modifying PLL configuration parameters, then the RX reset timing operation needs to be performed again. Refer to Figure 4-7.

4.4 TX and RX Reset Timing

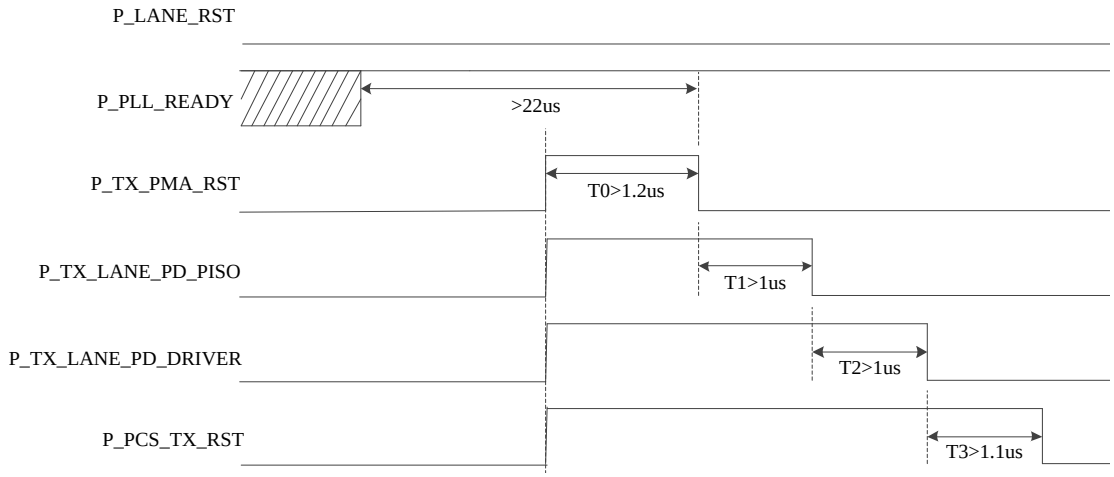

Figure 4-6 TX Reset Timing Diagram

HSSTLP supports resetting TX and RX channels only. The premise for TX reset is P_PLL_READY being high and the PLL is locked and in a stable state.

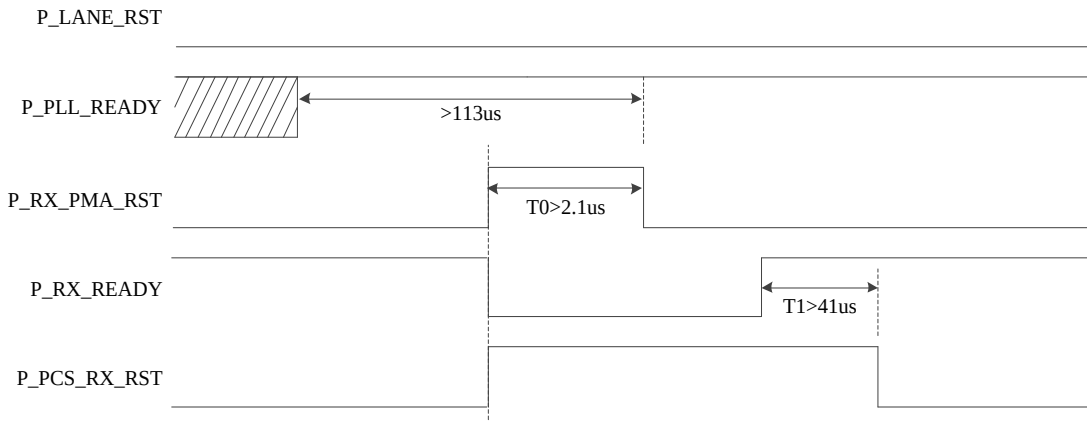

Figure 4-7 RX Reset Timing Diagram

The premise for RX reset is P_PLL_READY being high and the PLL is properly locked and in a stable state.

Chapter 5 HSSTLP Register Description

Each LANE has a separate set of PCS channel configuration registers and PMA channel configuration registers:

PCS configuration register base address: 0x000

PMA RX configuration register base address: 0x400

PMA TX configuration register base address: 0x800

Each PLL has a separate set of channel configuration registers:

PLL configuration register base address: 0x000

The HSSTLP IP has 4 LANEs and 2 PLLs internally, each LANE and PLL has a separate set of configuration registers and address space. To facilitate user access, the IP has added an APB Bridge module, so users can access all LANEs and PLLs through a single APB bus interface. Register default values are based on IP parameters, and the register descriptions are for reference only.

The address bus width for each LANE or each PLL is 12 bits. The APB Bridge adds 4 bits to the address as the Chip Select signal, making the address bus 16 bits. The APB addr[15:12]=0~3 of the IP corresponds to LANE0~LANE3, and addr[15:12]=4~5 corresponds to PLL0~PLL1.

For detailed address space allocation, refer to UG041004_Logos2_HSSTLP_IP_UserGuide.pdf.

5.1 PLL Configuration Register Descriptions

Table 5-1 PLL Configuration Register Description: pma_pll_reg0, Offset Address 0x000

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	PMA_PLL_REG_PLL_CP[1:0]	The bit[1:0] of PLL charge pump current select is 2’b11 (default).
5	R/W	PMA_PLL_REG_READY_OR_LOCK	reg_ready_or_lock 1’b0: Corresponds to the parameter value “FALSE” (default) 1’b1: Corresponds to the parameter value “TRUE”
4:3	R/W	PMA_PLL_REG_PLL_VCTRL_SET	PLL Vctrl start voltage, default: 0
2:1	R/W	PMA_PLL_REG_PFDDELAYSEL	PLL pdf delay select, default: 1
0	R/W	PMA_PLL_REG_PLL_PFDDELAY_EN	Pll pfd delay enable 1’b0: Corresponds to the parameter value “FALSE”, disable 1’b1: Corresponds to the parameter value “TRUE”, enable (default)

Table 5-2 PLL Configuration Register Description: pma_pll_reg1, Offset Address 0x001

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_PLL_REG_PLL_CP[9:2]	The bit[9:2] of PLL charge pump current select PMA_PLL_REG_PLL_CP[9:2]=8'b0000 0111(default)

Table 5-3 PLL Configuration Register Description: pma_pll_reg2, Offset Address 0x002

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_PLL_REG_PLL_READY_OW	PLL ready rewrite enable signal, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
6	R		reserved
5	R/W	PMA_PLL_REG_PLL_LOCKDET_EN	Lockdet en input to register, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
4:0	R/W	PMA_PLL_REG_PLL_REFDIV	PLL reference clock divider M, related to IP configuration 5'b10000: Division Ratio 1 (default) 5'b00000: Division Ratio 2

Table 5-4 PLL Configuration Register Description: pma_pll_reg3, Offset Address 0x003

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_PLL_REG_V2I_EN	Bias circuit enable signal: 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE" (default)
6	R/W	PMA_PLL_REG_V2I_BIAS_SEL	Bias circuit select signal; 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
5:0	R/W	PMA_PLL_REG_PLL_FBDIV	Bit[5]:Pll feedback divider N1; Bit[4:0],Pll feedback divider N2; Related to IP configuration

Setting	N1	N2	Division Ratio
6'b010000	4	1	4
6'b000000	4	2	8
6'b000001	4	3	12
6'b000010	4	4	16
6'b000011	4	5	20
6'b000101	4	6	24
6'b000110	4	8	32
6'b000111	4	10	40
6'b110000	5	1	5
6'b100000	5	2	10
6'b100001	5	3	15
6'b100010	5	4	20
6'b100011	5	5	25
6'b100101	5	6	30
6'b100110	5	8	40
6'b100111	5	10	50

Table 5-5 PLL Configuration Register Description: pma_pll_reg4, Offset Address 0x004

Bits	R/W	Corresponding Parameter Name	Description
7:5	R/W	PMA_PLL_REG_JTAG_VHYSTSEL	PLL JTAG threshold voltage selection, fixed to value 0
4	R/W	PMA_PLL_REG_JTAG_OE	PLL JTAG oe 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
3:0	R/W	PMA_PLL_REG_LPF_RES	LPF resistor control, default: 4'b0001

Table 5-6 PLL Configuration Register Description: pma_pll_reg5, Offset Address 0x005

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_PLL_REG_PLL_LOCKDET_MODE	Lockdet mode select, 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE" 1'b0: default. This mode determines whether two clocks are locked by detecting the time difference used by the two input clock domains to reach the same count limit configured by PMA_PLL_REG_PLL_LOCKDET_REFCT and PMA_PLL_REG_PLL_LOCKDET_FBCT. If the difference is less than the value set by the register (PMA_PLL_REG_PLL_LOCKDET_LOCKCT), it is considered a single lock; otherwise, it is a single unlock; repeat the operations above. When the number of consecutive locks reaches the set value (PMA_PLL_REG_PLL_LOCKDET_ITER), it is considered a PLL lock; When the number of consecutive unlocks reaches the set value (PMA_PLL_REG_PLL_UNLOCKDET_ITER), it is considered a PLL unlock; if a PLL lock is confirmed after detection, whether to continue lock detection is determined based on the PMA_PLL_REG_LOCKDET_REPEAT configuration; and if a PLL unlock is confirmed after detection, perform lock detection again. 1'b1: In this mode, the system waits for a while (the time it takes for the reference clock domain counter to reach its limit) before assuming a PLL lock; once a PLL lock is confirmed, it ceases further monitoring until a reset occurs.

Bits	R/W	Corresponding Parameter Name	Description
6:4	R/W	PMA_PLL_REG_PLL_LOCKDET_ITER	Lock loop count Number of iterations of consecutive successful one-time lock detection before set pll_lock 3'b000: 1 (default) 3'b001: 2 3'b010: 4 3'b011: 8 3'b100: 16 3'b101: 32 3'b110: 64 3'b111:127
3:1	R/W	PMA_PLL_REG_PLL_LOCKDET_FBCT	Feedback clock domain counter overflow value The upper limit number of feedback clock's cycles. If the feedback clock counter reaches this number, stop counting. 3'b000: 2^9 3'b001: 2^10 3'b010: 2^11 3'b011: 2^12(default) 3'b100: 2^13 3'b101: 2^14 3'b110: 2^15 3'b111: 2^16-1
0	R/W	PMA_PLL_REG_PLL_LOCKDET_EN_OW	Lockdet en overwrite signal, fixed to value 0. 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"

Table 5-7 PLL Configuration Register Description: pma_pll_reg6, Offset Address 0x006

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_PLL_REG_PLL_LOCKDET_RESET_N_OW	PLL lock detector reset overwrite signal, fixed to value 0. 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
6	R/W		reserved
5:3	R/W	PMA_PLL_REG_PLL_LOCKDET_REFCT	Reference clock domain counter overflow value The upper limit number of reference clock's cycles. If the reference clock counter reaches this number, stop counting. 3'b000: 2^9 3'b001: 2^10 3'b010: 2^11 3'b011: 2^12(default) 3'b100: 2^13 3'b101: 2^14 3'b110: 2^15 3'b111: 2^16-1

Bits	R/W	Corresponding Parameter Name	Description
2:0	R/W	PMA_PLL_REG_PLL_LOCKDET_LOCKCT	Difference counter overflow value The threshold of the difference counter to decide whether the pll is locked or not one time. The difference counter measures the time difference (with unit: the number of reference clock's cycle) between the reference clock counter and feedback clock counter reach their upper limit respectively. If the difference is smaller than this threshold, pll is locked one time. 3'b000: 2 3'b001: 4 3'b010: 8 3'b011: 16 3'b100: 32 (default) 3'b101: 64 3'b110: 128 3'b111: 256

Table 5-8 PLL Configuration Register Description: pma_pll_reg7, Offset Address 0x007

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_PLL_REG_PLL_UNLOCKED_STICKY_CLEAR	The clear signal for continuous PLL unlock signal, active-high 1'b0: Corresponds to the parameter value "FALSE", do not clear (default) 1'b1: Corresponds to the parameter value "TRUE", clear
6	R/W	PMA_PLL_REG_PLL_UNLOCKED_OW	Unlocked overwrite signal, fixed to value 0. 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
5:4	R/W	PMA_PLL_REG_PLL_UNLOCKDET_ITER	Non-lock loop count Set the number of iterations of lock detection attempts before setting pll_unlock. 2'b00: 64 2'b01: 128 2'b10: 256 (default) 2'b11: 1023
3	R		Reserved, fixed to value 0
2	R/W	PMA_PLL_REG_PLL_LOCKED_STICKY_CLEAR	The clear signal for continuous PLL lock signal, active-high 1'b0: Corresponds to the parameter value "FALSE", do not clear (default) 1'b1: Corresponds to the parameter value "TRUE", clear

Bits	R/W	Corresponding Parameter Name	Description
1	R/W	PMA_PLL_REG_PLL_LOCKED_OW	Locked signal output selection, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
0	R		Reserved, fixed to value 0

Table 5-9 PLL Configuration Register Description: pma_pll_reg8, Offset Address 0x008

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_PLL_REG_RESCAL_EN	Register configuration resistor calibration enable signal register for resistor calibration enable 1'b0: Corresponds to the parameter value "FALSE": disable (default) 1'b1: Corresponds to the parameter value "TRUE": normal operation
6	R/W	PMA_PLL_REG_REFCLK_TEST_EN	Enables refclk to test port, active-high 1'b0: Corresponds to the parameter value "FALSE": disable (default) 1'b1: Corresponds to the parameter value "TRUE": enable
5:0	R/W	PMA_PLL_REG_I_CTRL_MAX	The maximum value of the variable resistor control code (feedback to the variable resistor), the maximum automatic calibration value Set the maximal resistor control code allowed. If the average value of resistor control code calculated by digital system is larger than this maximal value, the result of resistor calibration is invalid. Default: 6'b111111

Table 5-10 PLL Configuration Register Description: pma_pll_reg9, Offset Address 0x009

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 0
6	R/W	PMA_PLL_REG_RESCAL_DONE_OW	Overwrite signal for resistor calibration done, fixed to value 0. 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE".
5:0	R/W	PMA_PLL_REG_I_CTRL_MIN	The minimum value of the variable resistor control code (feedback to the variable resistor), the minimum automatic calibration value Set the minimal resistor control code allowed. If the average value of resistor control code calculated by digital system is smaller than this maximal value, the result of resistor calibration is invalid. Default: 6'b000000.

Table 5-11 PLL Configuration Register Description: pma_pll_reg10, Offset Address 0x00a

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_PLL_REG_RESCAL_I_CODE_PMA	Enable input resistor control code to resistor calibration digital system.

Bits	R/W	Corresponding Parameter Name	Description
			1’b0: Corresponds to the parameter value “FALSE”, the select signal comes from the internal calibration circuit module (default); 1’b1: Corresponds to the parameter value “TRUE”, the select signal comes from the external port.
6	R/W	PMA_PLL_REG_RESCAL_I_CODE_OW	Overwrite signal of enable input resistor control code. Fixed to value 0. 1’b0: Corresponds to the parameter value “FALSE” (default) 1’b1: Corresponds to the parameter value “TRUE”
5:0	R		Reserved, fixed to value 6’b101110

Table 5-12 PLL Configuration Register Description: pma_pll_reg11, Offset Address 0x00b

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 0
6	R/W	PMA_PLL_REG_RESCAL_INT_R_SMALL_OW	Overwrite signal for comparative result between the internal resistor and external resistor. Fixed to value 0. 1’b0: Corresponds to the parameter value “FALSE” (default) 1’b1: Corresponds to the parameter value “TRUE”
5:0	R		Reserved, fixed to value 6’b101110

Table 5-13 PLL Configuration Register Description: pma_pll_reg12, Offset Address 0x00c

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 0
6	R/W	PMA_PLL_REFCLK2LANE_PD_R	pll_refclk_lane_r power down control 1’b0: Corresponds to the parameter value “FALSE” (default) 1’b1: Corresponds to the parameter value “TRUE”
5	R/W	PMA_PLL_REFCLK2LANE_PD_L	pll_refclk_lane_l power down control 1’b0: Corresponds to the parameter value “FALSE” (default) 1’b1: Corresponds to the parameter value “TRUE”

Bits	R/W	Corresponding Parameter Name	Description
4	R/W	PMA_PLL_REG_RESCAL_WAIT_SEL	Resistor calibration waiting time, which is the duration of each calibration cycle Set the time interval of tuning the resistor control code with one step when the system is working in resistor calibration. After this time interval, system will decide whether the current resistor control code is valid or there is a need to change the resistor control code and decide again. 1'b0: Corresponds to the parameter value "FALSE": 63 clock cycles 1'b1: Corresponds to the parameter value "TRUE": 31 clock cycles (default)
3	R	PMA_PLL_REG_RESCAL_RST_N_VAL	Reserved, fixed to value 0
2	R/W	PMA_PLL_REG_RESCAL_RESET_N_OW	Resistor calibration reset_n overwrite signal. Fixed to value 0. 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
1:0	R/W	PMA_PLL_REG_RESCAL_ITER_VALID_SEL	Select iteration times of valid resistor calibration. Resistor calibration is valid means that the system finds the resistor control code which resistor value closely approximate to external resistor. If iteration times of valid resistor calibration reach this number, the system will calculate the average value of resistor control code, output as the result of resistor calibration. 2'b00:64 times (default); 2'b01:32 times; 2'b10:16 times; 2'b11:8 times.

Table 5-14 PLL Configuration Register Description: pma_pll_reg13, Offset Address 0x00d

Bits	R/W	Corresponding Parameter Name	Description
7:2	R/W	PMA_PLL_REG_IBUP_A1[5:0]	Bias current control code, A1 bit[5:0]=6'b111111, PMA_PLL_REG_IBUP_A1[17:0]=18'd262143 (default)
1:0	R/W	PMA_PLL_REG_BG_TRIM	Select Vref output voltage. It defaults to 2'b10

Table 5-15 PLL Configuration Register Description: pma_pll_reg14, Offset Address 0x00e

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_PLL_REG_IBUP_A1[13:6]	Bias current control code, A1 bit[13:6]. It defaults to 0xFF

Table 5-16 PLL Configuration Register Description: pma_pll_reg15, Offset Address 0x00f

Bits	R/W	Corresponding Parameter Name	Description
7:4	R/W	PMA_PLL_REG_IBUP_A2[3:0]	Bias current control code, A2 bit[3:0]=4'b0000, PMA_PLL_REG_IBUP_A2[17:0]=18'd1023 (default)
3:0	R/W	PMA_PLL_REG_IBUP_A1[17:14]	Bias current control code, A1 bit[17:14]=4'b1111

Table 5-17 PLL Configuration Register Description: pma_pll_reg16, Offset Address 0x010

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_PLL_REG_IBUP_A2[11:4]	Bias current control code, A2 bit[11:4]. It defaults to 0

Table 5-18 PLL Configuration Register Description: pma_pll_reg17, Offset Address 0x011

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	PMA_PLL_REG_IBUP_PD[1:0]	Bias current power down signal bit[1:0]=2'b00 PMA_PLL_REG_IBUP_PD[17:0]=18'd0 (default)
5:0	R/W	PMA_PLL_REG_IBUP_A2[17:12]	Bias current control code, A2 bit[17:12]=6'b000000

Table 5-19 PLL Configuration Register Description: pma_pll_reg18, Offset Address 0x012

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_PLL_REG_IBUP_PD[9:2]	Bias current power down signal bit[9:2]. It defaults to 0

Table 5-20 PLL Configuration Register Description: pma_pll_reg19, Offset Address 0x013

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_PLL_REG_IBUP_PD[17:10]	Bias current power down signal bit[17:10]. It defaults to 0

Table 5-21 PLL Configuration Register Description: pma_pll_reg20, Offset Address 0x014

Bits	R/W	Corresponding Parameter Name	Description
7:4	R/W	PMA_PLL_REG_V2I_TB_SEL	Bias circuit test control bit. It defaults to 0
3	R/W	PMA_PLL_REG_V2I_RCALTEST_PD	Register configuration resistor bias circuit PD signal 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE": power down
2	R/W	PMA_PLL_REG_NOREFCLK_STICKY_CLEAR	Clear pll_norefclk_sticky_o_x, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE", do not clear (default) 1'b1: Corresponds to the parameter value "TRUE", clear
1	R/W	PMA_PLL_REG_NOFBCLK_STICKY_CLEAR	Clear pll_nofbclk_sticky_o_x reset, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE", do not clear (default) 1'b1: Corresponds to the parameter value "TRUE", clear

Bits	R/W	Corresponding Parameter Name	Description
0	R/W	PMA_PLL_REG_LOCKDET_REPEAT	Enable repeat lock detection after pll is locked. 1'b0: Corresponds to the parameter value "FALSE", does not repeat lock detection after PLL is locked (default). 1'b1: Corresponds to the parameter value "TRUE", repeats lock detection after PLL is locked.

Table 5-22 PLL Configuration Register Description: pma_pll_reg21, Offset Address 0x015

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5:0	R/W	PMA_PLL_REG_RES_CAL_TEST	Resistor calibration control bit (internal connection) Register of the internal resistor control code from resistor calibration. It defaults to 0

Table 5-23 PLL Configuration Register Description: pma_pll_reg22, Offset Address 0x016

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 0
6	R/W	PMA_PLL_REG_TEST_SIG_HALF_EN	Enables test signal voltage half, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
5	R/W	PMA_PLL_REG_TEST_V_EN	Enables test signal voltage, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
4:0	R/W	PMA_PLL_REG_TEST_SEL	Test signal selection. It defaults to 0

Table 5-24 PLL Configuration Register Description: pma_pll_reg23, Offset Address 0x017

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5	R/W	PMA_PLL_REG_CML_REFCLK_PD	Power down of reference clock 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE": power down
4	R/W	PMA_PLL_REG_REFCLK_PAD_SEL	Selects refclk from PAD or internal circuit, Related to IP configuration 1'b0: Corresponds to the parameter value "FALSE": from the pad reference clock 1'b1: Corresponds to the parameter value "TRUE": reference clock from fabric

Bits	R/W	Corresponding Parameter Name	Description
3	R/W	PMA_PLL_REG_CML_CLK_OUT_EN	Selects reference clock output to adjacent PLL 1'b0: Does not output to adjacent PLL (default) 1'b1: Outputs to the PLL adjacent to this HSSTLP and the adjacent HSSTLP's PLL Note: The PDS software will automatically configure this parameter according to the clock pin constraint location.
2	R/W	PMA_PLL_REG_REFCLK_TERM_IMP_CTRL	Selects the impedance for PLL differential clock input 1'b0: Corresponds to the parameter value "FALSE", high-impedance input 1'b1: Corresponds to the parameter value "TRUE", enables impedance matching (default). For matching resistor value HSST_R_{RCLK}, refer to "DS04001_Logos2 Family FPGAs Device Datasheet".
1:0	R/W	PMA_PLL_REG_REFCLK_SEL	PLL reference clock input: 2'b00: Select this HSSTLP's PLL reference clock as the input clock source (default) 2'b01: Select this HSSTLP's adjacent PLL reference clock as the input clock source 2'b10: Select the adjacent HSSTLP's PLL0 clock source 2'b11: Select the adjacent HSSTLP's PLL1 clock source Note: The PDS software will automatically configure this parameter according to the clock pin constraint location.

Table 5-25 PLL Configuration Register Description: pma_pll_reg24, Offset Address 0x018

Bits	R/W	Corresponding Parameter Name	Description
PLL0 pma_pll_reg24			
7:6	R/W	PMA_RES_CAL_DIV	Control the clock divide ratio in res calibration. After this divider, clock output to digital part for calibrate res. 2'b00: div ratio=1 (default); 2'b01: div ratio=2; 2'b10: div ratio=4; 2'b11: div ratio=8.
5	R/W	PMA_RES_CAL_CLK_SEL	Select the input clock for res calibration 1'b0: Corresponds to the parameter value "FALSE", selects the reference clock from PLL0 (default). 1'b1: Corresponds to the parameter value "TRUE": selects the reference clock from PLL1.
4:3	R/W	PLL0_TXPCLK_PLL_SEL	choose the clock to synchronize the signal pma_rate_change_on_i_x: Related to IP configuration 2'b00: Selects txpclk of LANE0; 2'b01: Selects txpclk of LANE1; 2'b10: Selects txpclk of LANE2; 2'b11: Selects txpclk of LANE3.
2:0	R/W	LANEx_REG_SYNC_OW	lane synchronize overwrite signal bit[2]~bit[0] correspond to LANE2~0, respectively, each bit fixed to value 0
PLL1 pma_pll_reg24			

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	PMA_RES_CAL_DIV	Control the clock divide ratio in res calibration. After this divider, clock output to digital part for calibrate res. 2'b00: div ratio=1 (default); 2'b01: div ratio=2; 2'b10: div ratio=4; 2'b11: div ratio=8.
5	R/W	PMA_RES_CAL_CLK_SEL	Select the input clock for res calibration 1'b0: Corresponds to the parameter value "FALSE", selects the reference clock from PLL0 (default). 1'b1: Corresponds to the parameter value "TRUE": selects the reference clock from PLL1.
4:0	R		Reserved, fixed to value 0

Table 5-26 PLL Configuration Register Description: pma_pll_reg25, Offset Address 0x019

Bits	R/W	Corresponding Parameter Name	Description
PLL0 pma_pll_reg25			
7:5	R/W	LANEx_PLL_REF_SEL	LANEx_PLL_REF_SEL[2:0]. It defaults to 0 pll refclk selection for channel x, for LANE2~0: bit[2]~bit[0] correspond to LANE2~0, respectively, with each bit value defined as: 1'b0: choose reference clock of PLL0 to channel; 1'b1: choose reference clock of PLL1 to channel.
4:1	R		Reserved, fixed to value 0
0	R/W	LANEx_REG_SYNC_OW	lane synchronize overwrite signal Correspond to LANE3, fixed to value 0
PLL1 pma_pll_reg25			
7:0	R		Reserved, fixed to value 0

Table 5-27 PLL Configuration Register Description: pma_pll_reg26, Offset Address 0x01a

Bits	R/W	Corresponding Parameter Name	Description
PLL0 pma_pll_reg26			
7:5	R		Reserved, fixed to value 0
4:1	R/W	LANEx_PLL_LOCK_OW_EN	PLL lock register overwrite signal, for LANE3~0; fixed to value 4'b0.
0	R/W	LANEx_PLL_REF_SEL	LANEx_PLL_REF_SEL[3]. It defaults to 0 pll refclk selection for channel x, for LANE3: 1'b0: choose reference clock of PLL0 to channel; 1'b1: choose reference clock of PLL1 to channel.
PLL1 pma_pll_reg26			
7:0	R		Reserved, fixed to value 0

Table 5-28 PLL Configuration Register Description: pma_pll_reg27, Offset Address 0x01b

Bits	R/W	Corresponding Parameter Name	Description
PLL0 pma_pll_reg27			
7:6	R/W	PLL_TX_SYNCK_SEL	clock selection for lane synchronization. 2'b01 (default)

Bits	R/W	Corresponding Parameter Name	Description
5	R/W	PD_CLK_GB	Power down all clocks from PLL. 1'b0: Power up all clock output from PLL (default); 1'b1: Power down all clocks output from PLL.
4:1	R/W	LANEx_PLL_LOCK_SEL	PLL lock signal selection for channel x, for LANE3~0: bit[3]~bit[0] correspond to LANE3~0, respectively, with each bit value defined as: 1'b0: choose lock signal of PLL0 to channel<x>; 1'b1: choose lock signal of PLL1 to channel<x>. It defaults to 0.
0	R		Reserved, fixed to value 0
PLL1 pma_pll_reg27			
7:0	R		Reserved, fixed to value 0

Table 5-29 PLL Configuration Register Description: pma_pll_reg28, Offset Address 0x01c

Bits	R/W	Corresponding Parameter Name	Description
PLL0 pma_pll_reg28			
7:5	R/W	LANE3_MUX_BIAS	bias current selection of cml buffer to LANE3 3'b010 (default)
4	R/W	LANE3_PD_CLK	power down clock to LANE3 1'b0: Power up clock to LANE3 (default); 1'b1: power down clock to LANE3
3:2	R/W	LANE3_CLK_RX_SEL	clock selection to rx of LANE3 2'b00: no clk to be selected; (default) 2'b01: select clk of PLL0; 2'b10: select clk of PLL1; 2'b11: no clk to be selected.
1:0	R/W	LANE3_CLK_TX_SEL	clock selection to tx of LANE3 2'b00: no clk to be selected; (default) 2'b01: select clk of PLL0; 2'b10: select clk of PLL1; 2'b11: no clk to be selected.
PLL1 pma_pll_reg28			
7:0	R		Reserved, fixed to value 0

Table 5-30 PLL Configuration Register Description: pma_pll_reg29, Offset Address 0x01d

Bits	R/W	Corresponding Parameter Name	Description
PLL0 pma_pll_reg29			
7:5	R/W	LANE2_MUX_BIAS	bias current selection of cml buffer to LANE2 3'b010 (default)
4	R/W	LANE2_PD_CLK	power down clock to LANE2 1'b0: Power up clock to LANE2 (default); 1'b1: power down clock to LANE2
3:2	R/W	LANE2_CLK_RX_SEL	clock selection to rx of LANE2 2'b00: no clk to be selected; (default) 2'b01: select clk of PLL0; 2'b10: select clk of PLL1; 2'b11: no clk to be selected.

Bits	R/W	Corresponding Parameter Name	Description
1:0	R/W	LANE2_CLK_TX_SEL	clock selection to tx of LANE2 2'b00: no clk to be selected; (default) 2'b01: select clk of PLL0; 2'b10: select clk of PLL1; 2'b11: no clk to be selected.
PLL1 pma_pll_reg29			
7:6	R/W	LANEx_PMA_RATE_CHANGE_ON_SEL	pma_rate_change_on selection for channel x, for LANE1~0: 1'b0: choose PLL0 P_RATE_CHANGE_TCLK_ON signal to channel<x>;(default) 1'b1: choose PLL1 P_RATE_CHANGE_TCLK_ON signal to channel<x>.
5:4	R/W	PLL1_TXPCLK_PLL_SEL	choose the clock to synchronize the signal pma_rate_change_on_i_1: 2'b00: Selects txpclk of LANE0 (default); 2'b01: Selects txpclk of LANE1; 2'b10: Selects txpclk of LANE2; 2'b11: Selects txpclk of LANE3.
3:0	R		Reserved, fixed to value 0

Table 5-31 PLL Configuration Register Description: pma_pll_reg30, Offset Address 0x01e

Bits	R/W	Corresponding Parameter Name	Description
PLL0 pma_pll_reg30			
7:5	R/W	LANE1_MUX_BIAS	bias current selection of cml buffer to LANE1 3'b010 (default)
4	R/W	LANE1_PD_CLK	power down clock to LANE1 1'b0: Power up clock to LANE1; (default) 1'b1: power down clock to LANE1
3:2	R/W	LANE1_CLK_RX_SEL	Clock selection to RX of LANE1, 2'b00: no clk to be selected; 2'b01: select clk of PLL0; (default) 2'b10: select clk of PLL1; 2'b11: no clk to be selected.
1:0	R/W	LANE1_CLK_TX_SEL	Clock selection to TX of LANE1, 2'b00: no clk to be selected; 2'b01: select clk of PLL0; (default) 2'b10: select clk of PLL1; 2'b11: no clk to be selected
PLL1 pma_pll_reg30			
7:4	R/W	LANEx_SYNC_SEL	Synchronize signal selection for channel x, for LANE3~0: 1'b0: choose PLL0 P_LANE_SYNC to channel<x>; 1'b1: choose PLL1 P_LANE_SYNC to channel<x>.
3:2	R/W	TX_SYNCK_PD	Power down the clock output from PLLx to synchronize P_LANE_SYNC: 1'b0: Power up (default); 1'b1: Power down.

Bits	R/W	Corresponding Parameter Name	Description
1:0	R/W	LANEx_PMA_RATE_CHANGE_ON_SEL	pma_rate_change_on selection for channel x, for LANE3~2: 1'b0: choose PLL0 P_RATE_CHANGE_TCLK_ON signal to channel<x>; 1'b1: choose PLL1 P_RATE_CHANGE_TCLK_ON signal to channel<x>.

Table 5-32 PLL Configuration Register Description: pma_pll_reg31, Offset Address 0x01f

Bits	R/W	Corresponding Parameter Name	Description
PLL0 pma_pll_reg31			
7:5	R/W	LANE0_MUX_BIAS	bias current selection of cml buffer to LANE0 3'b010 (default)
4	R/W	LANE0_PD_CLK	power down clock to LANE0 1'b0: Power up clock to LANE0 (default); 1'b1: power down clock to LANE0
3:2	R/W	LANE0_CLK_RX_SEL	clock selection to rx of LANE0 2'b00: no clk to be selected; 2'b01: select clk of PLL0; (default) 2'b10: select clk of PLL1; 2'b11: no clk to be selected.
1:0	R/W	LANE0_CLK_TX_SEL	clock selection to tx of LANE0 2'b00: no clk to be selected; 2'b01: select clk of PLL0; (default) 2'b10: select clk of PLL1; 2'b11: no clk to be selected.
PLL1 pma_pll_reg31			
7:4	R/W	LANEx_PLL_PD_SEL	pll_pd selection for channel x, for LANE3~0: 1'b0: choose pll_pd of PLL0 to channel<x>; 1'b1: choose pll_pd of PLL1 to channel<x>.
3:0	R/W	LANEx_PLL_RST_SEL	pll_rst selection for channel x, for LANE3~0: 1'b0: choose pll_rst of PLL0 to channel<x>; 1'b1: choose pll_rst of PLL1 to channel<x>.

Table 5-33 PLL Configuration Register Description: pma_pll_reg32, Offset Address 0x020

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		Reserved, fixed to value 0
2	R/W	PARM_PLL_RSTN	cfg_pll_rstn, reset when low 1'b0: Corresponds to the parameter value "FALSE", PLL reset 1'b1: Corresponds to the parameter value "TRUE", PLL normal operation (default)
1	R/W	PARM_PLL_POWERUP	Control PMA_PLL's power up 1'b0: Corresponds to the parameter value "OFF", power down 1'b1: Corresponds to the parameter value "ON", power up (default)

Bits	R/W	Corresponding Parameter Name	Description
0	R/W	PARM_CFG_HSSTLP_RSTN	cfg_hsst_rstn 1'b0: Corresponds to the parameter value "FALSE", reset 1'b1: Corresponds to the parameter value "TRUE", normal operation (default)

Table 5-34 PLL Configuration Register Description: pma_pll_reg33, Offset Address 0x021

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		reserved
2	R		pll reference clock lost,1:LOST
1	R		pll fb clock lost,1:LOST
0	R		pll locked,1:LOCK

Table 5-35 PLL Configuration Register Description: pma_pll_reg34, Offset Address 0x022

Bits	R/W	Corresponding Parameter Name	Description
7	R		PMA_PLL_STATUS[7], fixed to value 0
6:1	R		PMA_PLL_STATUS[6:1],pma_rescal_i_code_o
0	R		PMA_PLL_STATUS[0], rescal_done,1:DONE;

Table 5-36 PLL Configuration Register Description: pma_pll_reg35, Offset Address 0x023

Bits	R/W	Corresponding Parameter Name	Description
7	R		PMA_PLL_STATUS[15], pll_locked_sticky,1: LOCK When bit[2] of pma_pll_reg7 is 0, the bit value is valid. Consistent with the definition of the P_PLL_READY port signal. Under normal PLL working state, this register value should be 1.
6	R		PMA_PLL_STATUS[14], pll_unlocked,1:UN-LOCK Corresponds to the inverted PMA_PLL_STATUS[13] Under normal PLL working state, this register value should be 0.
5	R		PMA_PLL_STATUS[13], pll_locked,1:LOCK Consistent with the definition of the P_PLL_READY port signal. Under normal PLL working state, this register value should be 1.
4	R		PMA_PLL_STATUS[12], pll_norefclk_sticky_o, 0: Normal operation Under normal PLL working state, this register value should be 0.
3	R		PMA_PLL_STATUS[11], pll_nofbclk_sticky_o, 0: Normal operation Under normal PLL working state, this register value should be 0.
2	R		PMA_PLL_STATUS[10], reserved, fixed to value 0
1:0	R		PMA_PLL_STATUS[9:8], fixed to value 0

Table 5-37 PLL Configuration Register Description: pma_pll_reg36, Offset Address 0x024

Bits	R/W	Corresponding Parameter Name	Description
7:2	R		PMA_PLL_STATUS[23:18], fixed to value 0
1	R		PMA_PLL_STATUS[17], rescal_en_o,1:enable
0	R		PMA_PLL_STATUS[16], pll_unlocked_sticky,1: UN-LOCK

Table 5-38 PLL Configuration Register Description: pma_pll_reg37, Offset Address 0x025

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		PMA_PLL_STATUS[31:24],reserved

5.2 PCS Channel Configuration Register Description

Table 5-39 PCS Channel Configuration Register Description: Offset Address 0x000

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PCS_BYPASS_BRIDGE_FIFO	Bypasses RX Bridge unit/RX Bridge FIFO control module, [7:6]=2'b00: RX Bridge unit active (default); [7:6]=2'b01: Bypasses RX Bridge unit; [7:6]=2'b1x: Bypasses RX Bridge FIFO. [7] or [6]=1'b0: Corresponds to the parameter value "FALSE" [7] or [6]=1'b1: Corresponds to the parameter value "TRUE"
6	R/W	PCS_BYPASS_BRIDGE	
5	R/W	PCS_BYPASS_GEAR	Active-high, bypasses RX Gear module, related to IP configuration 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE"
4	R/W	PCS_BYPASS_CTC	Active-high, bypasses CTC module, related to IP configuration 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE"
3	R/W	PCS_BYPASS_BONDING	Active-high, bypasses the Channel Bonding module, related to IP configuration 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE"
2	R/W	PCS_BYPASS_DENC	Active-high, bypasses 8B10B Decoder module, related to IP configuration 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE"
1	R/W	PCS_BYPASS_WORD_ALIGN	Active-high, bypasses Word Alignment module, related to IP configuration 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE"
0	R		Reserved

Table 5-40 PCS Channel Configuration Register Description: Offset Address 0x001

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 0
6	R/W	PCS_FARLP_PWR_REDUCTION	Active-high, disables PCS far-end loopback FIFO, reducing

Bits	R/W	Corresponding Parameter Name	Description
			power consumption 1'b0: Corresponds to the parameter value "FALSE", enables PCS far-end loopback FIFO when conducting PCS far-end loopback test. (default) 1'b1: Corresponds to the parameter value "TRUE", disables PCS far-end loopback FIFO when not conducting PCS far-end loopback test, reducing power consumption.
5	R/W	PCS_SAMP_16B	One of the PCS Receiver module data width selections, related to IP configuration 1'b0: Corresponds to the parameter value "X20"; used for bit width modes other than 8/16/32 bits only 1'b1: Corresponds to the parameter value "X16"; used for 8/16/32 bits only bit width modes;
4:3	R/W	PCS_ALIGN_MODE	Word Alignment Link State Machine selection, related to IP configuration 2'b00: Corresponds to the parameter value "1GB"; selects Link State Machine based on Gig Ethernet 2'b01: Corresponds to the parameter value "10GB"; selects Link State Machine based on 10G Ethernet 2'b10: Corresponds to the parameter value "RAPIDIO"; selects Link State Machine based on RapidIO 2'b11: Corresponds to the parameter value "OUTSIDE"; selects External State Machine control
2:1	R/W	PCS_RX_POLARITY_INV	RX Sample Reg module polarity inversion and bit order inversion; 2'b00: Corresponds to the parameter value "DELAY"; no inversion (default) 2'b01: Corresponds to the parameter value "BIT_POLARITY_INVERION"; enables polarity inversion 2'b10: Corresponds to the parameter value "BIT_REVERSAL"; enables bit order inversion 2'b11: Corresponds to the parameter value "BOTH"; enables both polarity inversion and bit order inversion
0	R/W	PCS_DATA_MODE	One of the PCS Receiver module data width selections, related to IP configuration 1'b0: Corresponds to the parameter values "X8" and "X10"; used for 8bit only, 10bit only, or 8B10B 8bit bit width modes; 1'b1: Corresponds to the parameter values "X16" and "X20"; used for bit width modes other than 8bit only, 10bit only, and 8B10B 8bit;

Table 5-41 PCS Channel Configuration Register Description: Offset Address 0x002

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PCS_COMMA_REG0[7:0]	Word Alignment Comma byte definition 0, lower 8bits Related to IP configuration

Table 5-42 PCS Channel Configuration Register Description: Offset Address 0x003

Bits	R/W	Corresponding Parameter Name	Description
7:2	R/W	PCS_COMMA_MASK[5:0]	Word Alignment Comma Mask bit definition, lower 6bits Related to IP configuration
1:0	R/W	PCS_CHx_COMMA_REG0[9:8]	Word Alignment Comma byte definition 0, upper 2bits Related to IP configuration

Table 5-43 PCS Channel Configuration Register Description: Offset Address 0x004

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	PCS_CTC_MODE	CTC mode selection, related to IP configuration 2'b00: Corresponds to the parameter value "1SKIP"; the added/deleted SKIP character is 1 byte 2'b01: Corresponds to the parameter value "2SKIP"; the added/deleted SKIP character is 2 bytes 2'b10: Corresponds to the parameter value "PCIE_2BYTE"; PCIe's 2-byte mode, which only adds or deletes the subsequent skip 2'b11: Corresponds to the parameter value "4SKIP"; PCIe's 4-byte mode, the SKIP character is 4 bytes, but only the last byte of the SKIP character is added/deleted
5:4	R/W	PCS_CEB_MODE	Channel Bonding State Machine selection, related to IP configuration 2'b00: Corresponds to the parameter value "10GB"; selects the Channel Bonding State Machine based on XAUI 2'b01: Corresponds to the parameter value "RAPIDIO"; selects the Channel Bonding State Machine based on RapidIO 2'b10: Corresponds to the parameter value "OUTSIDE"; selects External State Machine control 2'b11: Reserved
3:0	R/W	PCS_COMMA_MASK[9:6]	Word Alignment Comma Mask bit definition, upper 4 bits Related to IP configuration

Table 5-44 PCS Channel Configuration Register Description: Offset Address 0x005

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PCS_A_REG	Definition of Align Pattern used for Channel Bonding, related to IP configuration

Table 5-45 PCS Channel Configuration Register Description: Offset Address 0x006

Bits	R/W	Corresponding Parameter Name	Description
7:2	R/W	PCS_SKIP_REG0[5:0]	SKIP character Byte 0 used by CTC, lower 6bits, related to IP configuration
1	R/W	PCS_GE_AUTO_EN	Active-high, enables automatic replacement from /C/ to /I2/ based on 1 Gig Ethernet, Related to IP configuration 1'b0: Corresponds to the parameter value "FALSE"; disable 1'b1: Corresponds to the parameter value "TRUE"; enable
0	R		Reserved, fixed to value 0

Table 5-46 PCS Channel Configuration Register Description: Offset Address 0x007

Bits	R/W	Corresponding Parameter Name	Description
7:4	R/W	PCS_SKIP_REG1[3:0]	SKIP character Byte 1 used by CTC, lower 4bits, related to IP configuration
3	R		Reserved, fixed to value 0
2:0	R/W	PCS_SKIP_REG0[8:6]	SKIP character Byte 0 used by CTC, upper 3bits, related to IP

			configuration

Table 5-47 PCS Channel Configuration Register Description: Offset Address 0x008

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	PCS_SKIP_REG2[1:0]	SKIP character Byte 2 used by CTC, lower 2bits, related to IP configuration
5	R		Reserved, fixed to value 0
4:0	R/W	PCS_SKIP_REG1[8:4]	SKIP character Byte 1 used by CTC, upper 5bits, related to IP configuration

Table 5-48 PCS Channel Configuration Register Description: Offset Address 0x009

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 0
6:0	R/W	PCS_SKIP_REG2[8:2]	SKIP character Byte 2 used by CTC, upper 7bits, related to IP configuration

Table 5-49 PCS Channel Configuration Register Description: Offset Address 0x00a

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PCS_SKIP_REG3[7:0]	SKIP character Byte 3 used by CTC, lower 8 bits, related to IP configuration

Table 5-50 PCS Channel Configuration Register Description: Offset Address 0x00b

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 0
6	R/W	PCS_ERRDETECT_SILENCE	1’b0: Corresponds to the parameter value “FALSE”, 1’b1: Corresponds to the parameter value “TRUE” (default)
5	R/W	PCS_COMMA_DET_MODE	Alignment mode selection in the Word Alignment module, related to IP configuration 1’b0: Corresponds to the parameter value “COMMA_PATTERN”, selects the Comma Alignment mode 1’b1: Corresponds to the parameter value “RX_CLK_SLIP”; selects the RX CLK Slip mode
4	R/W	PCS_FIFOFLAG_CTC	1’b0: Corresponds to the parameter value “FALSE” (default) 1’b1: Corresponds to the parameter value “TRUE”
3	R/W	PCS_SPLIT	One of the PCS Receiver module data width selections, related to IP configuration 1’b0: Corresponds to the parameter value “FALSE”; for bit width modes other than 8bit only, 10bit only, or 8B10B 8bit; 1’b1: Corresponds to the parameter value “TRUE”; for 8bit only, 10bit only, or 8B10B 8bit bit width modes;
2	R/W	PCS_DEC_DUAL	One of the PCS Receiver module data width selections, related to IP configuration 1’b1: Corresponds to the parameter value “TRUE”; 1’b0: Corresponds to the parameter value “FALSE”
1	R		Reserved, fixed to value 0
0	R/W	PCS_SKIP_REG3[8]	SKIP character Byte 3 used by CTC, upper 1bit, related to IP configuration

Table 5-51 PCS Channel Configuration Register Description: Offset Address 0x00c

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PCS_RCLK_POLINV	RCLK clock source selection 1’b0: Corresponds to the parameter value “RCLK” (default); 1’b1: Corresponds to the parameter value “REVERSE_OF_RCLK”;
6:5	R/W	PCS_AFTER_CTC_RCLK_SEL	AFTER_CTC_RCLK clock source selection, related to IP configuration 2’b00: Corresponds to the parameter value “PMA_RCLK”; 2’b01: Corresponds to the parameter value “PMA_TCLK”; 2’b10: Corresponds to the parameter value “MCB_RCLK”; 2’b11: Corresponds to the parameter value “RCLK2”
4:3	R/W	PCS_CB_RCLK_SEL	CB_RCLK clock source selection, related to IP configuration 2’b00: Corresponds to the parameter value “PMA_RCLK”; 2’b01: Corresponds to the parameter value “PMA_TCLK”; 2’b10: Corresponds to the parameter value “MCB_RCLK”; 2’b11: Reserved
2:1	R/W	PCS_PCS_RCLK_SEL	PCS_RCLK clock source selection, related to IP configuration 2’b00: Corresponds to the parameter value “PMA_RCLK”; 2’b01: Corresponds to the parameter value “PMA_TCLK”; 2’b10: Corresponds to the parameter value “RCLK”; 2’b11: Reserved;
0	R/W	PCS_PMA_RCLK_POLINV	1’b0: Corresponds to the parameter value “PMA_RCLK” (default); 1’b1: reserved

Table 5-52 PCS Channel Configuration Register Description: Offset Address 0x00d

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved
5	R/W	PCS_AFTER_CTC_RCLK_EN_GB	One of the PCS Receiver module data width selections, related to IP configuration 1’b0: Corresponds to the parameter value “FALSE”; used for bit width modes other than 32bit only, 40bit only, and 8B10B 32bit; 1’b1: Corresponds to the parameter value “TRUE”; used for 32bit only, 40bit only, or 8B10B 32bit bit width modes;
4	R/W	PCS_AFTER_CTC_RCLK_EN	One of the PCS Receiver module data width selections, related to IP configuration 1’b0: Corresponds to the parameter value “FALSE”, used for bit width modes other than 8bit only, 10bit only, or 8B10B 8bit; 1’b1: Corresponds to the parameter value “TRUE”; used for 8bit only, 10bit only, or 8B10B 8bit bit width modes;
3	R/W	PCS_CB_RCLK_EN	One of the PCS Receiver module data width selections, related to IP configuration 1’b0: Corresponds to the parameter value “FALSE”, used for bit width modes other than 8bit only, 10bit only, or 8B10B 8bit; 1’b1: Corresponds to the parameter value “TRUE”; used for 8bit only, 10bit only, or 8B10B 8bit bit width modes;

Bits	R/W	Corresponding Parameter Name	Description
2	R/W	PCS_PCS_RCLK_EN	One of the PCS Receiver module data width selections, related to IP configuration 1'b0: Corresponds to the parameter value "FALSE", used for bit width modes other than 8bit only, 10bit only, or 8B10B 8bit; 1'b1: Corresponds to the parameter value "TRUE"; used for 8bit only, 10bit only, or 8B10B 8bit bit width modes;
1:0	R/W	PCS_BRIDGE_RCLK_SEL	CB_RCLK clock source selection 2'b00: Corresponds to the parameter value "PMA_RCLK" (default); 2'b01: Corresponds to the parameter value "PMA_TCLK"; 2'b10: Corresponds to the parameter value "MCB_RCLK"; 2'b11: Corresponds to the parameter value "RCLK";

Table 5-53 PCS Channel Configuration Register Description: Offset Address 0x00e

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5	R/W	PCS_RX_BRIDGE_CLK_POLINV	1'b0: Corresponds to the parameter value "RX_BRIDGE_CLK" (default); 1'b1: Reserved
4:3	R/W	PCS_RX_64B66B_67B	64B66B_67B selection, related to IP configuration 2'b00: Corresponds to the parameter value "NORMAL"; 2'b01: Corresponds to the parameter value "64B_66B"; 2'b11: Corresponds to the parameter value "64B_67B";
2	R/W	PCS_PCIE_SLAVE	PCI Express-based channel bonding settings, related to IP configuration 1'b0: Corresponds to the parameter value "MASTER"; 1'b1: Corresponds to the parameter value "SLAVE";
1	R/W	PCS_SLAVE	Channel bonding settings other than PCI Express, related to IP configuration 1'b0: Corresponds to the parameter value 0, indicating "MASTER"; 1'b1: Corresponds to the parameter value 1, indicating "SLAVE";
0	R/W	PCS_PCS_RX_RSTN	Reset register for the PCS Receiver, i.e., cfg_pcs_rx_rstn, active low 1'b0: Corresponds to the parameter value "FALSE"; 1'b1: Corresponds to the parameter value "TRUE" (default);

Table 5-54 PCS Channel Configuration Register Description: Offset Address 0x00f

Bits	R/W	Corresponding Parameter Name	Description
7:1	R		Reserved, fixed to value 0
0	R/W	PCS_PCS_CB_RSTN	PCS CB reset register, i.e., cfg_pcs_cb_rstn, active low 1'b0: Corresponds to the parameter value "FALSE"; 1'b1: Corresponds to the parameter value "TRUE" (default);

Table 5-55 PCS Channel Configuration Register Description: Offset Address 0x010

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5	R/W	PCS_TX_BYPASS_BIT_SLIP	Enables TX BitSlip module Bypass, active-high 1'b0: Corresponds to the parameter value "FALSE"

Bits	R/W	Corresponding Parameter Name	Description
			1’b1: Corresponds to the parameter value “TRUE” (default)
4	R/W	PCS_TX_BYPASS_ENC	Enables 8B10B Encoder module Bypass, active-high, related to IP configuration 1’b0: Corresponds to the parameter value “FALSE” 1’b1: Corresponds to the parameter value “TRUE”
3	R/W	PCS_TX_BYPASS_GEAR	One of the PCS Transmitter module data width selections, related to IP configuration 1’b0: Corresponds to the parameter value “FALSE”, used for bit width modes other than 32bit only, 40bit only, and 8B10B 32bit; 1’b1: Corresponds to the parameter value “TRUE”, used for 32bit only, 40bit only, or 8B10B 32bit bit width modes;
2	R/W	PCS_TX_BYPASS_BRIDGE_FIFO	Bypass module TX Bridge unit/TX Bridge FIFO control, [2:1]=2’b00: TX Bridge unit active (default); [2:1]=2’b01: Bypasses TX Bridge unit; [2:1]=2’b10: Bypasses TX Bridge FIFO. [2] or [1]=1’b0: Corresponds to the parameter value “FALSE” [2] or [1]=1’b1: Corresponds to the parameter value “TRUE”
1	R/W	PCS_TX_BYPASS_BRIDGE_UINT	
0	R/W	PCS_TX_BRIDGE_GEAR_SEL	Configures the selection for the order of the bridge unit and gear module in the TX direction, Related to IP configuration 1’b0: Corresponds to the parameter value “FALSE”, bridge unit first; 1’b1: Corresponds to the parameter value “TRUE”, gear module first;

Table 5-56 PCS Channel Configuration Register Description: Offset Address 0x011

Bits	R/W	Corresponding Parameter Name	Description
7:3	R/W	PCS_TX_BIT_SLIP_CYCLES	Determines the number of slipped bits in the TX Bit Slip module. It defaults to 0
2:1	R/W	PCS_TX_DRIVE_REG_MODE	TX Drive Reg module polarity inversion and bit order inversion; 2’b00: Corresponds to the parameter value “NO_CHANGE”; no inversion (default) 2’b01: Corresponds to the parameter value “EN_POLARIY_REV”; enables polarity inversion 2’b10: Corresponds to the parameter value “EN_BIT_REV”; enables bit order inversion 2’b11: Corresponds to the parameter value “EN_BOTH”, enables both polarity inversion and bit order inversion
0	R/W	PCS_TX_GEAR_SPLIT	One of the PCS Transmitter module data width selections, related to IP configuration 1’b0: Corresponds to the parameter value “FALSE”; used for other modes 1’b1: Corresponds to the parameter value “TRUE”, used for 32bit only, 40bit only, or 8B10B 32bit bit width modes

Table 5-57 PCS Channel Configuration Register Description: Offset Address 0x012

Bits	R/W	Corresponding Parameter Name	Description

7:3	R		Reserved, fixed to value 0
2	R/W	PCS_INT_TX_MASK_2	Active-high Mask transmit channel interrupt status register (offset address 0x27) bit 2 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
1	R/W	PCS_INT_TX_MASK_1	Active-high Mask transmit channel interrupt status register (offset address 0x27) bit 1 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
0	R/W	PCS_INT_TX_MASK_0	Active-high Mask transmit channel interrupt status register (offset address 0x27) bit 0 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";

Table 5-58 PCS Channel Configuration Register Description: Offset Address 0x013

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		Reserved, fixed to value 0
2	R/W	PCS_INT_TX_CLR_2	Active-high clear transmit channel interrupt status register (offset address 0x27) bit 2 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
1	R/W	PCS_INT_TX_CLR_1	Active-high clear transmit channel interrupt status register (offset address 0x27) bit 1 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
0	R/W	PCS_INT_TX_CLR_0	Active-high clear transmit channel interrupt status register (offset address 0x27) bit 0 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";

Table 5-59 PCS Channel Configuration Register Description: Offset Address 0x014

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PCS_TX_GEAR_CLK_EN_SEL	One of the PCS Transmitter module data width selections, related to IP configuration 1'b0: Corresponds to the parameter value "FALSE"; used for other modes 1'b1: Corresponds to the parameter value "TRUE"; used for 32bit only, 40bit only, or 8B10B 32bit bit width modes that bypass TX Bridge FIFO;
6	R/W	PCS_TX_SLAVE	Channel bonding settings at the TX side, related to IP configuration 1'b0: Corresponds to the parameter value "MASTER"; 1'b1: Corresponds to the parameter value "SLAVE";
5	R/W	PCS_TX_PCS_TX_RSTN	Reset register for the PCS Transmitter, i.e., cfg_pcs_tx_rstn, active low 1'b0: Corresponds to the parameter value "FALSE"; 1'b1: Corresponds to the parameter value "TRUE" (default);
4	R/W	PCS_PCS_TCLK_SEL	PCS_TCLK selection, related to IP configuration 1'b0: Corresponds to the parameter value "PMA_TCLK"; 1'b1: Corresponds to the parameter value "TCLK";
3	R/W	PCS_TX_TCLK_POLINV	1'b0: Corresponds to the parameter value "TCLK" (default); 1'b1: Reserved

Bits	R/W	Corresponding Parameter Name	Description
2	R/W	PCS_TX_BRIDGE_TCLK_SEL	TCLK clock source selection, related to IP configuration 1'b0: Corresponds to the parameter value "PCS_TCLK"; 1'b1: Corresponds to the parameter value "TCLK";
1	R/W	PCS_TX_PCS_CLK_EN_SEL	One of the PCS Transmitter module data width selections, related to IP configuration 1'b0: Corresponds to the parameter value "FALSE"; used for other modes 1'b1: Corresponds to the parameter value "TRUE"; used for 32bit only, 40bit only, or 8B10B 32bit bit width modes;
0	R/W	PCS_TX_PMA_TCLK_POLINV	1'b0: Corresponds to the parameter value "PMA_TCLK" (default); 1'b1: Reserved

Table 5-60 PCS Channel Configuration Register Description: Offset Address 0x015

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved, fixed to value 0
4	R/W	PCS_GEAR_TCLK_SEL	GEAR_TCLK selection, related to IP configuration 1'b0: Corresponds to the parameter value "PMA_TCLK"; 1'b1: Corresponds to the parameter value "TCLK2";
3:2	R/W	PCS_TX_64B66B_67B	TX 64B66B_67B selection, related to IP configuration 2'b00: Corresponds to the parameter value "NORMAL"; 2'b01: Corresponds to the parameter value "64B_66B"; 2'b11: Corresponds to the parameter value "64B_67B";
1:0	R/W	PCS_DATA_WIDTH_MODE	One of the PCS Transmitter module data width selections, related to IP configuration 2'b00: Corresponds to the parameter value "X20"; used for 20bit only, 8B10B 16bit, 8B10B 32bit, and 40bit only modes 2'b01: Corresponds to the parameter value "X16"; used for 16bit only and 32bit only modes 2'b10: Corresponds to the parameter value "X10"; used for 10bit only and 8B10B 8bit modes 2'b11: Corresponds to the parameter value "X8"; used for 8bit only mode

Table 5-61 PCS Channel Configuration Register Description: Offset Address 0x016

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved, fixed to value 0
4	R/W	PCS_TX_BRIDGE_CLK_POLINV	TX_BRIDGE_CLK clock selection 1'b0: Corresponds to the parameter value "TX_BRIDGE_CLK" (default); 1'b1: Corresponds to the parameter value "REVERSE_OF_TX_BRIDGE_CLK";
3	R		Reserved, fixed to value 0
2	R/W	PCS_ENC_DUAL	One of the PCS Transmitter module data width selections, related to IP configuration 1'b0: Corresponds to the parameter value "FALSE"; used for modes other than 8B10B 16bit and 8B10B 32bit 1'b1: Corresponds to the parameter value "TRUE"; used for 8B10B 16bit and 8B10B 32bit modes
1	R/W	PCS_TX_OUTZZ	1'b0: Corresponds to the parameter value "FALSE" (default);

Bits	R/W	Corresponding Parameter Name	Description
			1’b1: Reserved
0	R/W	PCS_TX_TCLK2FABRIC_SEL	One of the PCS Transmitter module data width selections, related to IP configuration 1’b0: Corresponds to the parameter value “FALSE”; used for modes other than 32bit only, 40bit only, and 8B10B 32bit 1’b1: Corresponds to the parameter value “TRUE”; used for 32bit only, 40bit only, or 8B10B 32bit bit width modes

Table 5-62 PCS Channel Configuration Register Description: Offset Address 0x017

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PCS_COMMA_REG1	Word Alignment Comma byte definition 1, lower 8 bits, related to IP configuration

Table 5-63 PCS Channel Configuration Register Description: Offset Address 0x018

Bits	R/W	Corresponding Parameter Name	Description
7:2	R		Reserved, fixed to value 0
1:0	R/W	PCS_COMMA_REG1	Word Alignment Comma byte definition 1, upper 2 bits, related to IP configuration

Table 5-64 PCS Channel Configuration Register Description: Offset Address 0x019

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		Reserved, fixed to value 0
2:0	R/W	PCS_RAPID_IMAX	Number of bytes for lock state detection in Rapid IO Link State Machine, Related to IP configuration

Table 5-65 PCS Channel Configuration Register Description: Offset Address 0x01a

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PCS_RAPID_VMIN_1	Number of bytes for exit state detection in Rapid IO Link State Machine, lower 8bits, Related to IP configuration

Table 5-66 PCS Channel Configuration Register Description: Offset Address 0x01b

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PCS_RAPID_VMIN_2	Number of bytes for exit state detection in Rapid IO Link State Machine, upper 8bits Related to IP configuration

Table 5-67 PCS Channel Configuration Register Description: Offset Address 0x01c

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5	R/W	PCS_PRBS_ERR_LPBK	PRBS_ERR_LPBK enable 1’b0: Corresponds to the parameter value “FALSE” (default);

Bits	R/W	Corresponding Parameter Name	Description
			1’b1: Corresponds to the parameter value “TRUE”;
4	R/W	PCS_RX_ERRCNT_CLR	PCS_ERR_CNT counter clear, high level clear 1’b0: Corresponds to the parameter value “FALSE” (default); 1’b1: Corresponds to the parameter value “TRUE”, counter clear;
3:0	R/W	PCS_RX_PRBS_MODE	PRBS Checker mode selection at the receive side 4’d0: Corresponds to the parameter value “DISABLE” (default); 4’d1: Corresponds to the parameter value “PRBS_7”; 4’d2: Corresponds to the parameter value “PRBS_15”; 4’d3: Corresponds to the parameter value “PRBS_23”; 4’d4: Corresponds to the parameter value “PRBS_31”;

Table 5-68 PCS Channel Configuration Register Description: Offset Address 0x01d

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5	R/W	PCS_ENABLE_PRBS_GEN	Enables PCS PRBS Generator, active-high 1’b0: Corresponds to the parameter value “FALSE”, disables PRBS (default) 1’b1: Corresponds to the parameter value “TRUE”, enables PRBS
4	R/W	PCS_TX_INSERT_ER	PRBS error code injection, with a variable number of error bits injected Triggered by the rising edge from 0 to 1, one error code is injected into the PRBS data. During regular transmission of PRBS test data, the value remains 0. 1’b0: Corresponds to the parameter value “FALSE” (default); 1’b1: Corresponds to the parameter value “TRUE”;
3:0	R/W	PCS_TX_PRBS_MODE	PCS PRBS Generator mode selection at the TX side 4’d0: Corresponds to the parameter value “DISABLE” (default); 4’d1: Corresponds to the parameter value “PRBS_7”; 4’d2: Corresponds to the parameter value “PRBS_15”; 4’d3: Corresponds to the parameter value “PRBS_23”; 4’d4: Corresponds to the parameter value “PRBS_31”; 4’d5: Corresponds to the parameter value “LONG_1”; 4’d6: Corresponds to the parameter value “LONG_0”; 4’d7: Corresponds to the parameter value “20UI”; 4’d8: Corresponds to the parameter value “D10_2”; 4’d9: Corresponds to the parameter value “PCIE”;

Table 5-69 PCS Channel Configuration Register Description: Offset Address 0x01e

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	PCS_ERR_CNT	Checking error counter in PCS PRBS checker, which remains at 0xFF after reaching its maximum value 0xFF and will not increment with further link errors until the counter is cleared

Table 5-70 PCS Channel Configuration Register Description: Offset Address 0x01f

Bits	R/W	Corresponding Parameter Name	Description
7:4	R/W	PCS_MASTER_CHECK_OFFSET	Used for Channel Bonding, related to IP configuration
3:0	R/W	PCS_DEFAULT_RADDR	Used for Channel Bonding. It defaults to 6

Table 5-71 PCS Channel Configuration Register Description: Offset Address 0x020

Bits	R/W	Corresponding Parameter Name	Description
7	R	NA	Reserved, fixed to value 0
6:4	R/W	PCS_SEACH_OFFSET	Channel Bonding range settings, related to IP configuration 4'd0: Corresponds to the parameter value "20BIT"; 4'd1: Corresponds to the parameter value "30BIT"; 4'd2: Corresponds to the parameter value "40BIT"; 4'd3: Corresponds to the parameter value "50BIT"; 4'd4: Corresponds to the parameter value "60BIT"; 4'd5: Corresponds to the parameter value "70BIT"; 3'd6: Corresponds to the parameter value "80BIT";
3:0	R/W	PCS_DELAY_SET	Used for Channel Bonding, related to IP configuration

Table 5-72 PCS Channel Configuration Register Description: Offset Address 0x021

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		Reserved, fixed to value 0
2:0	R/W	PCS_CEB_RAPIDLS_MMAX	The MMAX value used by the Channel Bonding RapidIO state machine, Related to IP configuration

Table 5-73 PCS Channel Configuration Register Description: Offset Address 0x022

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved, fixed to value 0
4:0	R/W	PCS_CTC_AFULL	CTC FIFO Almost Full threshold. It defaults to 5'd20

Table 5-74 PCS Channel Configuration Register Description: Offset Address 0x023

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5	R/W	PCS_CTC_CONTI_SKP_SET	1'b0: Disables continuous SKP deletion (default) 1'b1: Enables continuous SKP deletion
4:0	R/W	PCS_CTC_AEMPTY	CTC FIFO Almost Empty threshold. It defaults to 5'd12

Table 5-75 PCS Channel Configuration Register Description: Offset Address 0x024

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved, fixed to value 0
4	R/W	PCS_PMA_RX2TX_PLOOP_EN	Enables PMA Far-end parallel loopback port mode, a value of 1 indicates that the P_PMA_FAREND_PLOOP port is valid. Related to IP configuration 1'b0: Corresponds to the parameter value "FALSE", disable; 1'b1: Corresponds to the parameter value "TRUE", enable
3	R/W	PCS_PMA_TX2RX_SLOOP_EN	Enables PMA Near-end serial loopback port mode, a value of 1 indicates that the P_PMA_NEAREND_SLOOP port is valid. Related to IP configuration 1'b0: Corresponds to the parameter value "FALSE", disable; 1'b1: Corresponds to the parameter value "TRUE", enable

Bits	R/W	Corresponding Parameter Name	Description
2	R/W	PCS_PMA_TX2RX_PLOOP_EN	Enables PMA Near-end parallel loopback port mode, a value of 1 indicates that the P_PMA_FAREND_PLOOP port is valid. Related to IP configuration 1'b0: Corresponds to the parameter value "FALSE", disable; 1'b1: Corresponds to the parameter value "TRUE", enable
1	R/W	PCS_NEAR_LOOP	PCS Near-end loopback enable (via register), active-high 1'b0: Corresponds to the parameter value "FALSE", disable (default); 1'b1: Corresponds to the parameter value "TRUE", enable;
0	R/W	PCS_FAR_LOOP	PCS Far-end loopback enable (via register), active-high 1'b0: Corresponds to the parameter value "FALSE", disable (default); 1'b1: Corresponds to the parameter value "TRUE", enable;

Table 5-76 PCS Channel Configuration Register Description: Offset Address 0x025

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PCS_INT_RX_MASK_7	Receive channel interrupt status register (offset address 0x28) bit 7 mask, active high 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
6	R/W	PCS_INT_RX_MASK_6	Receive channel interrupt status register (offset address 0x28) bit 6 mask, active high 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
5	R/W	PCS_INT_RX_MASK_5	Receive channel interrupt status register (offset address 0x28) bit 5 mask, active high 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
4	R/W	PCS_INT_RX_MASK_4	Receive channel interrupt status register (offset address 0x28) bit 4 mask, active high 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
3	R/W	PCS_INT_RX_MASK_3	Receive channel interrupt status register (offset address 0x28) bit 3 mask, active high 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
2	R/W	PCS_INT_RX_MASK_2	Receive channel interrupt status register (offset address 0x28) bit 2 mask, active high 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
1	R/W	PCS_INT_RX_MASK_1	Receive channel interrupt status register (offset address 0x28) bit 1 mask, active high 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
0	R/W	PCS_INT_RX_MASK_0	Receive channel interrupt status register (offset address 0x28) bit 0 mask, active high 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";

Table 5-77 PCS Channel Configuration Register Description: Offset Address 0x026

Bits	R/W	Corresponding Parameter Name	Description

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PCS_INT_RX_CLR_7	Clear receive channel interrupt status register (offset address 0x28) bit 7, active high 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
6	R/W	PCS_INT_RX_CLR_6	Clear receive channel interrupt status register (offset address 0x28) bit 6, active-high 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
5	R/W	PCS_INT_RX_CLR_5	Clear receive channel interrupt status register (offset address 0x28) bit 5, active-high 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
4	R/W	PCS_INT_RX_CLR_4	Clear receive channel interrupt status register (offset address 0x28) bit 4, active high 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
3	R/W	PCS_INT_RX_CLR_3	Clear receive channel interrupt status register (offset address 0x28) bit 3, active high 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
2	R/W	PCS_INT_RX_CLR_2	Clear receive channel interrupt status register (offset address 0x28) bit 2, active high 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
1	R/W	PCS_INT_RX_CLR_1	Clear receive channel interrupt status register (offset address 0x28) bit 1, active high 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";
0	R/W	PCS_INT_RX_CLR_0	Clear receive channel interrupt status register (offset address 0x28) bit 0, active high 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE";

Table 5-78 PCS Channel Configuration Register Description: Offset Address 0x027

Bits	R/W	Corresponding Parameter Name	Description
7:3	R	NA	Reserved
2	R	NA	1'b1: Invalid character detected in 8B10B encoding, and the abnormal state remains; This state can be cleared via bit[2] of register 0x013.
1	R	NA	Reserved
0	R	NA	Reserved

Table 5-79 PCS Channel Configuration Register Description: Offset Address 0x028

Bits	R/W	Corresponding Parameter Name	Description
7	R	NA	Reserved
6	R	NA	Reserved
5	R	NA	1'b1: CTC FIFO read empty, and the abnormal state remains; This state can be cleared via bit[5] of register 0x026.
4	R	NA	1'b1: CTC FIFO overflow, and the abnormal state remains;

Bits	R/W	Corresponding Parameter Name	Description
			This state can be cleared via bit[4] of register 0x026.
3	R	NA	Reserved
2	R	NA	Reserved
1	R	NA	1'b0: Channel Bonding state machine unlocks, and the abnormal state remains; This state can be cleared via bit[1] of register 0x026.
0	R	NA	1'b0: Word Alignment state machine unlocks, and the abnormal state remains; This state can be cleared via bit[0] of register 0x026.

Table 5-80 PCS Channel Configuration Register Description: Offset Address 0x029

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		Reserved, fixed to value 0
2	R/W	PCS_CA_DYN_DLY_SEL_RX	Active-high, enables the CLK Aligner function of the corresponding receive channel. 1'b0: Corresponds to the parameter value "FALSE", bypasses CLK Aligner (default); 1'b1: Corresponds to the parameter value "TRUE", enables CLK Aligner;
1	R/W	PCS_CA_DYN_DLY_EN_RX	Active-high, enable the CLK Aligner delay step of the receive channel 1'b0: Corresponds to the parameter value "FALSE", and the CLK Aligner delay step is 0 (default); 1'b1: Corresponds to the parameter value "TRUE", the CLK Aligner delay step is determined by CLK_ALIGNER_RXx or P_CIM_CLK_ALIGNER_RXx [7:0];
0	R/W	PCS_CA_RSTN_RX	RX CLK Aligner reset, i.e., cfg_ca_rstn_rx, active low. 1'b0: Corresponds to the parameter value "FALSE" (default); 1'b1: Corresponds to the parameter value "TRUE".

Table 5-81 PCS Channel Configuration Register Description: Offset Address 0x02a

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PCS_CA_RX	Static setting of the CLK Aligner delay step for the corresponding receive channel, Used when P_CIM_CLK_DYN_DLY_SEL_RX[x] is invalid. It defaults to 0

Table 5-82 PCS Channel Configuration Register Description: Offset Address 0x02b

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		Reserved, fixed to value 0
2	R/W	PCS_CA_DYN_DLY_SEL_TX	Active-high, enables the CLK Aligner function of the corresponding transmit channel 1'b0: Corresponds to the parameter value "FALSE", bypasses CLK Aligner (default); 1'b1: Corresponds to the parameter value "TRUE", enables CLK Aligner
1	R/W	PCS_CA_DYN_DLY_EN_TX	Active-high, enable the CLK Aligner delay step of the transmit

			channel 1’b0: Corresponds to the parameter value “FALSE”, and the CLK Aligner delay step is 0 (default); 1’b1: Corresponds to the parameter value “TRUE”, the CLK Aligner delay step is determined by CLK_ALIGNER_TXx or P_CIM_CLK_ALIGNER_TXx [7:0];
0	R/W	PCS_CA_RSTN_TX	TX CLK Aligner reset, i.e., cfg_ca_rstn_tx, active low. 1’b0: Corresponds to the parameter value “FALSE” (default); 1’b1: Corresponds to the parameter value “TRUE”.

Table 5-83 PCS Channel Configuration Register Description: Offset Address 0x02c

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PCS_CA_TX	Static setting for the CLK Aligner delay step of the corresponding transmission channel, Used when P_CIM_CLK_DYN_DLY_SEL_TX[x] is invalid. It defaults to 0

Table 5-84 PCS Channel Configuration Register Description: Offset Address 0x02d

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PCS_RXTEST_PWR_REDUCTION	Active-high, disables RX test_status, reducing the power 1’b0: Corresponds to the parameter value “NORMAL” (default), 1’b1: Corresponds to the parameter value “POWER_REDUCTION”
6	R/W	PCS_RXBRG_PWR_REDUCTION	Active-high, disables RX bridge, reducing the power 1’b0: Corresponds to the parameter value “NORMAL” (default), 1’b1: Corresponds to the parameter value “POWER_REDUCTION”
5	R/W	PCS_RXGEAR_PWR_REDUCTION	Active-high, disables RX GEAR, reducing the power 1’b0: Corresponds to the parameter value “NORMAL” (default), 1’b1: Corresponds to the parameter value “POWER_REDUCTION”
4	R/W	PCS_RXCTC_PWR_REDUCTION	Active-high, disables RX CTC, reducing the power 1’b0: Corresponds to the parameter value “NORMAL” (default), 1’b1: Corresponds to the parameter value “POWER_REDUCTION”
3	R/W	PCS_RXCB_PWR_REDUCTION	Active-high, disables RX channel bonding, reducing the power 1’b0: Corresponds to the parameter value “NORMAL” (default), 1’b1: Corresponds to the parameter value “POWER_REDUCTION”
2	R/W	PCS_RXDEC_PWR_REDUCTION	Active-high, disables RX decoder, reducing the power 1’b0: Corresponds to the parameter value “NORMAL” (default), 1’b1: Corresponds to the parameter value “POWER_REDUCTION”
1	R/W	PCS_WDALIGN_PWR_REDUCTION	Active-high, disables RX wordalign, reducing the power

Bits	R/W	Corresponding Parameter Name	Description
			1’b0: Corresponds to the parameter value “NORMAL” (default), 1’b1: Corresponds to the parameter value “POWER_REDUCTION”
0	R/W	PCS_RXPRBS_PWR_REDUCTION	Active-high, disables RX PRBS, reducing the power 1’b0: Corresponds to the parameter value “NORMAL” (default), 1’b1: Corresponds to the parameter value “POWER_REDUCTION”

Table 5-85 PCS Channel Configuration Register Description: Offset Address 0x02e

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved, fixed to value 0
4	R/W	PCS_TXPRBS_PWR_REDUCTION	Active-high, disables TX PRBS, reducing the power 1’b0: Corresponds to the parameter value “NORMAL” (default), 1’b1: Corresponds to the parameter value “POWER_REDUCTION”
3	R/W	PCS_TXBSLP_PWR_REDUCTION	Active-high, disables TX bitslip, reducing the power 1’b0: Corresponds to the parameter value “NORMAL” (default), 1’b1: Corresponds to the parameter value “POWER_REDUCTION”
2	R/W	PCS_TXENC_PWR_REDUCTION	Active-high, disables TX encoder, reducing the power 1’b0: Corresponds to the parameter value “NORMAL” (default), 1’b1: Corresponds to the parameter value “POWER_REDUCTION”
1	R/W	PCS_TXGEAR_PWR_REDUCTION	Active-high, disables TX GEAR, reducing the power 1’b0: Corresponds to the parameter value “NORMAL” (default), 1’b1: Corresponds to the parameter value “POWER_REDUCTION”
0	R/W	PCS_TXBRG_PWR_REDUCTION	Active-high, disables TX bridge, reducing the power 1’b0: Corresponds to the parameter value “NORMAL” (default), 1’b1: Corresponds to the parameter value “POWER_REDUCTION”

5.3 PMA Channel Configuration Register Description

5.3.1 PMA TX Section

Table 5-86 PMA Channel Configuration Register Description: pma_tx_reg0, Offset Address 0x800

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 0
6	R/W	PMA_REG_TX_RXDET_REQ_OW	rxdet request enable register overwrite signal, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
5:4	R/W	PMA_REG_TX_BEACON_TIMER_SEL	tx beacon timer selection register 2'b00: 2 clock cycles(default) 2'b01: 4 clock cycles 2'b10: 8 clock cycles 2'b11: 16 clock cycles
3	R/W	PMA_REG_TX_MAIN_PRE_Z_OW	reg_tx_main_pre_z overwrite signal, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
2	R		reserved
1	R/W	PMA_REG_TX_PD_OW	TX power down register overwrite signal, fixed to value 0. 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
0	R		reserved

Table 5-87 PMA Channel Configuration Register Description: pma_tx_reg1, Offset Address 0x801

Bits	R/W	Corresponding Parameter Name	Description
7:4	R		Reserved, fixed to value 0
3	R		Reserved, fixed to value 0
2	R/W	PMA_REG_TX_EI_EN_OW	EI enable register overwrite signal, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
1	R		Reserved, fixed to value 0
0	R/W	PMA_REG_TX_BEACON_EN_OW	Beacon enable register overwrite signal, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"

Table 5-88 PMA Channel Configuration Register Description: pma_tx_reg2, Offset Address 0x802

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 0
6:1	R/W	PMA_REG_TX_RES_CAL	Register TX res ctrl code. It defaults to 48
0	R/W	PMA_REG_TX_BIT_CONV	Sets whether the bit order of tx data_o[19:0] is inverted 1'b0: Corresponds to the parameter value "FALSE": bit order not inverted (default) 1'b1: Corresponds to the parameter value "TRUE": bit order inverted

Table 5-89 PMA Channel Configuration Register Description: pma_tx_reg3, Offset Address 0x803

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5:0	R		Reserved, fixed to value 6'b100000

Table 5-90 PMA Channel Configuration Register Description: pma_tx_reg4, Offset Address 0x804

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved, fixed to value 0

Table 5-91 PMA Channel Configuration Register Description: pma_tx_reg5, Offset Address 0x805

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	PMA_REG_TX_RESERVED_41_34	Reserved, fixed to value 0

Table 5-92 PMA Channel Configuration Register Description: pma_tx_reg6, Offset Address 0x806

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved, fixed to value 0

Table 5-93 PMA Channel Configuration Register Description: pma_tx_reg7, Offset Address 0x807

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved, fixed to value 0

Table 5-94 PMA Channel Configuration Register Description: pma_tx_reg8, Offset Address 0x808

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 1
6	R		Reserved, fixed to value 0
5	R		Reserved, fixed to value 1
4	R/W	PMA_REG_TX_RESET_N_OW	TX reset n register overwrite signal, fixed to value 0. 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
3	R/W	PMA_REG_TX_PD_POST_OW	tx_pd_post register overwrite signal.

Bits	R/W	Corresponding Parameter Name	Description
			1'b0: Corresponds to the parameter value "FALSE", overwrite disabled 1'b1: Corresponds to the parameter value "TRUE" (default) overwrite with pma_tx_reg8[2]
2	R/W	PMA_REG_TX_PD_POST	Enables post-cursor de-emphasis, the value is determined by the IP configuration 1'b0: Corresponds to the parameter value "ON", enabled 1'b1: Corresponds to the parameter value "OFF", disabled
1	R		Reserved, fixed to value 0
0	R/W	PMA_REG_TX_SYNC_OW	TX sync register overwrite signal, fixed to value 0. 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"

Table 5-95 PMA Channel Configuration Register Description: pma_tx_reg9, Offset Address 0x809

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5	R		Reserved, fixed to value 1
4	R/W	PMA_REG_PLL_READY_OW	TX PLL ready register overwrite signal, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
3:1	R/W	PMA_REG_TX_BUSWIDTH	TX buswidth control, the value is determined by the IP configuration bit[1:0]=2'b00: 8bit bit[1:0]=2'b01:10bit bit[1:0]=2'b10:16bit bit[1:0]=2'b11:20bit (default) bit[2] is reserved.
0	R/W	PMA_REG_TX_BUSWIDTH_OW	tx buswidth register overwrite signal. 1'b0: Corresponds to the parameter value "FALSE" Selects the port P_TX_BUSWIDTH 1'b1: Corresponds to the parameter value "TRUE" (default) Selects the register PMA_REG_TX_BUSWIDTH

Table 5-96 PMA Channel Configuration Register Description: pma_tx_reg10, Offset Address 0x80a

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5	R		Reserved, fixed to value 0

Bits	R/W	Corresponding Parameter Name	Description
4:3	R/W	PMA_REG_EI_PCLK_DELAY_SEL	Control tx_main_pre_z delay relative with normal parallel data. 2'b00: 0 txpclk cycle, the four signals are synchronized with parallel data. (default) 2'b01: -1 txpclk cycle, the four signals are 1 cycle earlier than parallel data. 2'b10: +1 txpclk cycle, the four signals are 1 cycle later than parallel data. 2'b11: reserved
2	R		Reserved, fixed to value 0
1	R		Reserved, fixed to value 0
0	R		Reserved, fixed to value 0

Table 5-97 PMA Channel Configuration Register Description: pma_tx_reg11, Offset Address 0x80b

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5:0	R		Reserved, fixed to value 0

Table 5-98 PMA Channel Configuration Register Description: pma_tx_reg12, Offset Address 0x80c

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5:0	R		Reserved, fixed to value 0

Table 5-99 PMA Channel Configuration Register Description: pma_tx_reg13, Offset Address 0x80d

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5:0	R		Reserved, fixed to value 0

Table 5-100 PMA Channel Configuration Register Description: pma_tx_reg14, Offset Address 0x80e

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5:0	R		Reserved, fixed to value 0

Table 5-101 PMA Channel Configuration Register Description: pma_tx_reg15, Offset Address 0x80f

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5:0	R		Reserved, fixed to value 0

Table 5-102 PMA Channel Configuration Register Description: pma_tx_reg16, Offset Address 0x810

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5:0	R		Reserved, fixed to value 0

Table 5-103 PMA Channel Configuration Register Description: pma_tx_reg17, Offset Address 0x811

<table>
<tr><th>Bits</th><th>R/W</th><th>Corresponding Parameter Name</th><th>Description</th></tr>
<tr><td>7:6</td><td>R</td><td></td><td>Reserved, fixed to value 0</td></tr>
<tr><td>5:0</td><td>R/W</td><td>PMA_REG_TX_AMP_DAC0</td><td>TX output swing control DAC0 (default selection), bit[5] reserved, fixed to value 0, bit[4:0] defined as follows
<table>
<tr><th>Setting</th><th>tx output swing(V)</th></tr>
<tr><td>5’b00000</td><td>0.193</td></tr>
<tr><td>5’b00001</td><td>0.229</td></tr>
<tr><td>5’b00010</td><td>0.269</td></tr>
<tr><td>5’b00011</td><td>0.305</td></tr>
<tr><td>5’b00100</td><td>0.344</td></tr>
<tr><td>5’b00101</td><td>0.383</td></tr>
<tr><td>5’b00110</td><td>0.416</td></tr>
<tr><td>5’b00111</td><td>0.453</td></tr>
<tr><td>5’b01000</td><td>0.486</td></tr>
<tr><td>5’b01001</td><td>0.519</td></tr>
<tr><td>5’b01010</td><td>0.552</td></tr>
<tr><td>5’b01011</td><td>0.582</td></tr>
<tr><td>5’b01100</td><td>0.615</td></tr>
<tr><td>5’b01101</td><td>0.646</td></tr>
<tr><td>5’b01110</td><td>0.679</td></tr>
<tr><td>5’b01111</td><td>0.706</td></tr>
<tr><td>5’b10000</td><td>0.736</td></tr>
<tr><td>5’b10001</td><td>0.760</td></tr>
<tr><td>5’b10010</td><td>0.787</td></tr>
<tr><td>5’b10011</td><td>0.815</td></tr>
<tr><td>5’b10100</td><td>0.839</td></tr>
<tr><td>5’b10101</td><td>0.860</td></tr>
<tr><td>5’b10110</td><td>0.884</td></tr>
<tr><td>5’b10111</td><td>0.905</td></tr>
<tr><td>5’b11000</td><td>0.923</td></tr>
<tr><td>5’b11001</td><td>0.941(default)</td></tr>
<tr><td>5’b11010</td><td>0.959</td></tr>
<tr><td>5’b11011</td><td>0.974</td></tr>
<tr><td>5’b11100</td><td>0.987</td></tr>
<tr><td>5’b11101</td><td>0.996</td></tr>
<tr><td>5’b11110</td><td>1.008</td></tr>
<tr><td>5’b11111</td><td>1.011</td></tr>
</table></td></tr>
</table>

Table 5-104 PMA Channel Configuration Register Description: pma_tx_reg18, Offset Address 0x812

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5:0	R/W	PMA_REG_TX_AMP_DAC1	TX output swing control DAC1; for register definition, refer to the register definition of PMA_CH_REG_TX_AMP_DAC0. It defaults to 19.

Table 5-105 PMA Channel Configuration Register Description: pma_tx_reg19, Offset Address 0x813

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5:0	R/W	PMA_REG_TX_AMP_DAC2	TX output swing control DAC2; for register definition, refer to the register definition of PMA_CH_REG_TX_AMP_DAC0. It defaults to 14.

Table 5-106 PMA Channel Configuration Register Description: pma_tx_reg20, Offset Address 0x814

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5:0	R/W	PMA_REG_TX_AMP_DAC3	TX output swing control DAC3, for register definition, refer to the register definition of PMA_CH_REG_TX_AMP_DAC0. It defaults to 9.

Table 5-107 PMA Channel Configuration Register Description: pma_tx_reg21, Offset Address 0x815

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved, fixed to value 5

Table 5-108 PMA Channel Configuration Register Description: pma_tx_reg22, Offset Address 0x816

Bits	R/W	Corresponding Parameter Name	Description
7:4	R		Reserved, fixed to value 0
3	R/W	PMA_REG_TX_MARGIN_OW	TX_margin register overwrite signal, fixed to value 0. 1’b0: Corresponds to the parameter value “FALSE” (default) 1’b1: Corresponds to the parameter value “TRUE”
2:0	R/W		Reserved, fixed to value 0

Table 5-109 PMA Channel Configuration Register Description: pma_tx_reg23, Offset Address 0x817

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_TX_BEACON_OSC_CTRL	beacon osc frequence control 1'b0: Corresponds to the parameter value "FALSE": 36M (default) 1'b1: Corresponds to the parameter value "TRUE": 18M
6:5	R		Reserved, fixed to value 0
4:3	R/W	PMA_REG_TX_RXDET_THRESHOLD	TX rxdet threshold select; 2'b00: Corresponds to the parameter value "28MV" 2'b01: Corresponds to the parameter value "56MV" 2'b10: Corresponds to the parameter value "84MV" (default) 2'b11: Corresponds to the parameter value "112MV"
2	R		Reserved, fixed to value 0
1	R/W	PMA_REG_TX_SWING_OW	TX_swing register overwrite signal, fixed to value 0. 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
0	R		Reserved, fixed to value 0

Table 5-110 PMA Channel Configuration Register Description: pma_tx_reg24, Offset Address 0x818

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 1
6	R/W	PMA_REG_TX_RXDET_STATUS_OW	rxdetect status register overwrite signal, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
5	R/W	PMA_REG_TX_PCLK_EDGE_SEL	Controls whether the rising edge or falling edge of txpclk is sent to the digital interface. 1'b0: Corresponds to the parameter value "FALSE": rise edge is selected (default) 1'b1: Corresponds to the parameter value "TRUE": fall edge is selected
4	R/W	PMA_REG_TX_TX2RX_SLPBACK_EN	PMA near-end serial loopback enable (via register) 1'b0: Corresponds to the parameter value "FALSE", disabled (default) 1'b1: Corresponds to the parameter value "TRUE", enabled
3:0	R		Reserved, fixed to value 0

Table 5-111 PMA Channel Configuration Register Description: pma_tx_reg25, Offset Address 0x819

Bits	R/W	Corresponding Parameter Name	Description

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved, fixed to value 0
4:3	R/W	PMA_REG_TX_PRBS_SEL	PMA TX PRBS mode selection 2'b00: PRBS7 (default) 2'b01: PRBS15 2'b10: PRBS23 2'b11: PRBS31
2:1	R/W	PMA_REG_TX_PRBS_GEN_WIDTH_SEL	PRBS width select 2'b00: 8 bit 2'b01: 10 bit 2'b10: 16 bit 2'b11: 20 bit (default)
0	R/W	PMA_REG_TX_PRBS_GEN_EN	Enables PMA TX PRBS generator 1'b0: Corresponds to the parameter value "FALSE": disable (default) 1'b1: Corresponds to the parameter value "TRUE": enable

Table 5-112 PMA Channel Configuration Register Description: pma_tx_reg26, Offset Address 0x81a

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_TX_UDP_DATA_7_TO_0	constant 20-bit pattern, TX_UDP_DATA[7:0], TX_UDP_DATA. It defaults to 5

Table 5-113 PMA Channel Configuration Register Description: pma_tx_reg27, Offset Address 0x81b

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_TX_UDP_DATA_15_TO_8	constant 20-bit pattern, TX_UDP_DATA[15:8], It defaults to 235

Table 5-114 PMA Channel Configuration Register Description: pma_tx_reg28, Offset Address 0x81c

Bits	R/W	Corresponding Parameter Name	Description
7:5	R/W	PMA_REG_TX_FIFO_WP_CTRL	TX_FIFO write protection control signal (set read initial address, range 0~5). It defaults to 4
4	R		Reserved, fixed to value 0
3:0	R/W	PMA_REG_TX_UDP_DATA_19_TO_16	Constant 20-bit pattern, TX_UDP_DATA[19:16]. It defaults to 3

Table 5-115 PMA Channel Configuration Register Description: pma_tx_reg29, Offset Address 0x81d

Bits	R/W	Corresponding Parameter Name	Description
7:4	R		Reserved, fixed to value 0
3	R/W	PMA_REG_TX_ERR_INSERT	PRBS error code injection; Triggered by the rising edge from 0 to 1, one error code is injected into the PRBS data. During regular transmission of PRBS test data, the value remains 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
2:1	R/W	PMA_REG_TX_DATA_MUX_SEL	Data selection control signal 2'b00: data from pcs (default) 2'b01: PRBS data

Bits	R/W	Corresponding Parameter Name	Description
			2’b10: udp data 2’b11: rx loopback data
0	R/W	PMA_REG_TX_FIFO_EN	Register configuration TX_fifo_en enable, 1’b0: Corresponds to the parameter value “FALSE”, disable (default) 1’b1: Corresponds to the parameter value “TRUE”, enable When TX PMA PRBS function or PMA Far-end parallel loopback is used, set this value to 1. The default value under normal conditions is 0.

Table 5-116 PMA Channel Configuration Register Description: pma_tx_reg30, Offset Address 0x81e

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5	R		Reserved, fixed to value 1
4	R/W	PMA_REG_RATE_CHANGE_TXPCLK_ON_OW	Rate change txpclk on register overwrite signal, fixed to value 0. 1’b0: Corresponds to the parameter value “FALSE” (default) 1’b1: Corresponds to the parameter value “TRUE”
3:2	R		Reserved, fixed to value 0
1	R/W	PMA_CH_REG_TX_SATA_EN	SATA mode enable register 1’b0: Corresponds to the parameter value “FALSE”: SATA mode is disabled (default) 1’b1: Corresponds to the parameter value “TRUE”: SATA mode is enabled
0	R		Reserved, fixed to value 0

Table 5-117 PMA Channel Configuration Register Description: pma_tx_reg31, Offset Address 0x81f

Bits	R/W	Corresponding Parameter Name	Description
7:5	R/W	PMA_REG_TX_CFG_POST2[2:0]	TX post-cursor de-emphasis PMA_REG_CFG_POST2[2:0], related to IP configuration, for register definition, refer to the register definition of PMA_REG_CFG_POST.
4:0	R/W	PMA_REG_TX_CFG_POST1	TX post-cursor de-emphasis PMA_REG_CFG_POST1, related to IP configuration, for register definition, refer to the register definition of PMA_REG_CFG_POST

Table 5-118 PMA Channel Configuration Register Description: pma_tx_reg32, Offset Address 0x820

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved, fixed to value 0
4	R/W	PMA_REG_TX_DEEMP_OW	TX_DEEMP register overwrite signal, fixed to value 0. 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
3:2	R		Reserved, fixed to value 0
1:0	R/W	PMA_REG_TX_CFG_POST2[4:3]	TX post-cursor de-emphasis PMA_REG_CFG_POST2[4:3], related to IP configuration, for register definition, refer to the register definition of PMA_REG_CFG_POST

Table 5-119 PMA Channel Configuration Register Description: pma_tx_reg33, Offset Address 0x821

Bits	R/W	Corresponding Parameter Name	Description
7:4	R/W	PMA_REG_TX_OOB_DELAY_SEL	controls the oob ei enable signal delay steps to compensate data latency. bit[1:0]=2'b00: 0 txpclk cycle, tx_oob_ei_en is synchronized with parallel data. (default) bit[1:0]=2'b01: -1 txpclk cycle, tx_oob_ei_en is 1 cycle earlier than parallel data. bit[1:0]=2'b10: +1 txpclk cycle, tx_oob_ei_en is 1 cycle later than parallel data. bit[1:0]=2'b11: reserved bit[3:2]: reserved, fixed to value 0
3:0	R		Reserved, fixed to value 0

Table 5-120 PMA Channel Configuration Register Description: pma_tx_reg34, Offset Address 0x822

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 0
6	R/W	PMA_REG_RX_JTAG_MODE_EN_OW	RX JTAG mode enable register overwrite signal, fixed to value 0. 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
5	R		Reserved, fixed to value 0
4	R/W	PMA_REG_TX_JTAG_MODE_EN_OW	TX JTAG mode enable register overwrite signal, fixed to value 0. 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
3	R/W	PMA_REG_TX_LS_MODE_EN	low-speed 270M mode enable signal 1'b0: Corresponds to the parameter value "FALSE": low-speed mode is disabled (default) 1'b1: Corresponds to the parameter value "TRUE": low-speed mode is enabled

Bits	R/W	Corresponding Parameter Name	Description
2	R		Reserved, fixed to value 0
1	R/W	PMA_REG_ANA_TX_JTAG_DATA_O_SEL	JTAG data overwrite signal, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
0	R/W	PMA_REG_TX_POLARITY	PMA TX polarity inversion 1'b0: Corresponds to the parameter value "NORMAL" txpdata_out[19:0] = txpdata_in[19:0] (default) 1'b1: Corresponds to the parameter value "REVERSE" txpdata_out[19:0] = ~txpdata_in[19:0]

Table 5-121 PMA Channel Configuration Register Description: pma_tx_reg35, Offset Address 0x823

Bits	R/W	Corresponding Parameter Name	Description
7:5	R/W	PMA_REG_RX_TERM_MODE_CTRL	RX termination working mode control register Related to IP configuration 3'b010: external DC, internal DC 3'b100: external DC, internal AC 3'b101: external AC, internal AC(PCIe) 3'b110: external AC, internal DC(default) Note: Configure the external AC and internal AC mode for the PCIe application scenario. Select modes for other application scenarios as needed.
4	R/W	PMA_REG_TX_RES_CAL_EN	Enable PLL resistor calibration output resistor control code to TX 1'b0: Corresponds to the parameter value "FALSE", TX resistor control code comes from register (default) 1'b1: Corresponds to the parameter value "TRUE", TX resistor control code comes from PLL resistor calibration
3:1	R/W	PMA_REG_RX_ACJTAG_VHYSTSEL	rx acjtag hysteresis voltage control register It defaults to 0.
0	R/W	PMA_REG_RX_JTAG_OE	rx jtag module enable register 1'b0: Corresponds to the parameter value "FALSE": disabled; 1'b1: Corresponds to the parameter value "TRUE": enable (default)

Table 5-122 PMA Channel Configuration Register Description: pma_tx_reg36, Offset Address 0x824

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		Reserved, fixed to value 0
2	R/W	PMA_REG_PLPBK_TXPCLK_EN	txpclk enable register in parallel loopback mode 1'b0: Corresponds to the parameter value "FALSE": txpclk is used, normal working mode (default) 1'b1: Corresponds to the parameter value "TRUE": rxpclk is used in parallel loopback mode to guarantee no FIFO overflow, When in PMA and PCS remote loopback mode, it is necessary to set it to 1, and the default value under normal conditions is 0.
1:0	R		Reserved, fixed to value 0

Table 5-123 PMA Channel Configuration Register Description: pma_tx_reg37, Offset Address 0x825

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5:0	R/W	PMA_REG_TX_PH_SEL	TX PISO sample clock phase selection, fixed to value 1

Table 5-124 PMA Channel Configuration Register Description: pma_tx_reg38, Offset Address 0x826

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved, fixed to value 0
4:0	R/W	PMA_REG_TX_CFG_PRE	TX pre-cursor de-emphasis setting value, which is defined as follows:

Setting	Gain (dB)
5'b00000	0
5'b00001	0.219
5'b00010	0.472
5'b00011	0.791
5'b00100	1.001
5'b00101	1.246
5'b00110	1.542
5'b00111	1.871
5'b01000	2.109
5'b01001	2.460
5'b01010	2.714
5'b01011	3.053
5'b01100	3.446
5'b01101	3.871
5'b01110	4.215
5'b01111	4.619
5'b10000	5.043
5'b10001	5.438
5'b10010	5.958
Others	reserved

Table 5-125 PMA Channel Configuration Register Description: pma_tx_reg39, Offset Address 0x827

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved, fixed to value 0

Table 5-126 PMA Channel Configuration Register Description: pma_tx_reg40, Offset Address 0x828

<table>
<tr><th>Bits</th><th>R/W</th><th>Corresponding Parameter Name</th><th>Description</th></tr>
<tr><td>7:5</td><td>R</td><td></td><td>Reserved, fixed to value 0</td></tr>
<tr><td>4:0</td><td>R/W</td><td>PMA_REG_CFG_POST</td><td>TX post-cursor de-emphasis setting value, which is defined as follows:
<table>
<tr><th>Setting</th><th>Gain (dB)</th></tr>
<tr><td>5’b00000</td><td>0</td></tr>
<tr><td>5’b00001</td><td>0.219</td></tr>
<tr><td>5’b00010</td><td>0.500</td></tr>
<tr><td>5’b00011</td><td>0.732</td></tr>
<tr><td>5’b00100</td><td>0.970</td></tr>
<tr><td>5’b00101</td><td>1.215</td></tr>
<tr><td>5’b00110</td><td>1.499</td></tr>
<tr><td>5’b00111</td><td>1.771</td></tr>
<tr><td>5’b01000</td><td>2.109</td></tr>
<tr><td>5’b01001</td><td>2.388</td></tr>
<tr><td>5’b01010</td><td>2.789</td></tr>
<tr><td>5’b01011</td><td>3.092</td></tr>
<tr><td>5’b01100</td><td>3.446</td></tr>
<tr><td>5’b01101</td><td>3.829</td></tr>
<tr><td>5’b01110</td><td>4.171</td></tr>
<tr><td>5’b01111</td><td>4.619</td></tr>
<tr><td>5’b10000</td><td>5.091</td></tr>
<tr><td>5’b10001</td><td>5.539</td></tr>
<tr><td>5’b10010</td><td>5.904</td></tr>
<tr><td>5’b10011</td><td>6.511</td></tr>
<tr><td>5’b10100</td><td>7.001</td></tr>
<tr><td>5’b10101</td><td>7.563</td></tr>
<tr><td>5’b10110</td><td>8.095</td></tr>
<tr><td>5’b10111</td><td>8.809</td></tr>
<tr><td>5’b11000</td><td>9.588</td></tr>
<tr><td>5’b11001</td><td>10.353</td></tr>
<tr><td>5’b11010</td><td>11.325</td></tr>
<tr><td>5’b11011</td><td>12.159</td></tr>
<tr><td>5’b11100</td><td>13.205</td></tr>
<tr><td>Others</td><td>reserved</td></tr>
</table>
</td></tr>
</table>

Table 5-127 PMA Channel Configuration Register Description: pma_tx_reg41, Offset Address 0x829

Bits	R/W	Corresponding Parameter Name	Description

Bits	R/W	Corresponding Parameter Name	Description
7:2	R		Reserved, fixed to value 0
1	R/W	PMA_REG_PD_PRE	Enables pre-cursor de-emphasis, related to IP configuration 1'b0: Corresponds to the parameter value "FALSE ", enabled 1'b1: Corresponds to the parameter value "TRUE", disable
0	R/W	PMA_REG_PD_MAIN	Fixed to value 1 1'b0: Corresponds to the parameter value "TRUE" 1'b1: Corresponds to the parameter value "FALSE" (default)

Table 5-128 PMA Channel Configuration Register Description: pma_tx_reg42, Offset Address 0x82a

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved, fixed to value 0

Table 5-129 PMA Channel Configuration Register Description: pma_tx_reg43, Offset Address 0x82b

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved, fixed to value 0

Table 5-130 PMA Channel Configuration Register Description: pma_tx_reg44, Offset Address 0x82c

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved, fixed to value 0

Table 5-131 PMA Channel Configuration Register Description: pma_tx_reg45, Offset Address 0x82d

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved, fixed to value 0

Table 5-132 PMA Channel Configuration Register Description: pma_tx_reg46, Offset Address 0x82e

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_TX_CFG_15_TO_8	Reserved. It defaults to 0.

Table 5-133 PMA Channel Configuration Register Description: pma_tx_reg47, Offset Address 0x82f

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_TX_CFG_23_TO_16	Reserved. It defaults to 0.

Table 5-134 PMA Channel Configuration Register Description: pma_tx_reg48, Offset Address 0x830

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_TX_CFG_31_TO_24	It defaults to 8'b10000000 When reg_tx_cfg_31_to_24[7] is 1, (default) ana_tx_pd_driver_o comes from pma_tx_pd_driver_o; When reg_tx_cfg_31_to_24[7] is 0, ana_tx_pd_driver_o comes from reg_tx_cfg_31_to_24[6]

Table 5-135 PMA Channel Configuration Register Description: pma_tx_reg49, Offset Address 0x831

Bits	R/W	Corresponding Parameter Name	Description
7:4	R		Reserved, fixed to value 0
3	R/W	PMA_REG_TX_BEACON_EN_DELAYED_OW	tx_beacon_en_delayed register overwrite signal, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
2	R		Reserved, fixed to value 0
1	R/W	PMA_REG_TX_OOB_EI_EN_OW	tx_oob_ei_en register overwrite signal, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
0	R		Reserved, fixed to value 0

Table 5-136 PMA Channel Configuration Register Description: pma_tx_reg50, Offset Address 0x832

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_TX_RXDET_TIMER_SEL	Register control the sample waiting time of rx detect; Waiting time equals to the value of PMA_CH_REG_TX_RXDET_TIMER_SEL + 4 periods of PLL reference clock. It defaults to 87

Table 5-137 PMA Channel Configuration Register Description: pma_tx_reg51, Offset Address 0x833

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved, fixed to value 0

Table 5-138 PMA Channel Configuration Register Description: pma_tx_reg52, Offset Address 0x834

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved, fixed to value 0

Table 5-139 PMA Channel Configuration Register Description: pma_tx_reg53, Offset Address 0x835

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved, fixed to value 0

Table 5-140 PMA Channel Configuration Register Description: pma_tx_reg54, Offset Address 0x836

Bits	R/W	Corresponding Parameter Name	Description
7:0	R		Reserved, fixed to value 0

Table 5-141 PMA Channel Configuration Register Description: pma_tx_reg55, Offset Address 0x837

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5	R/W	PMA_REG_CFG_TX_PMA_RSTN	Configures TX lane resetn 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE" (default)
4	R/W	PMA_REG_CFG_TX_LANE_POWERUP_DRIVER	Configures TX lane power-up driver 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE" (default)
3	R/W	PMA_REG_CFG_TX_LANE_POWERUP_PISO	Configures TX lane piso powerup 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE" (default)
2	R/W	PMA_REG_CFG_TX_LANE_POWERUP_CLKPATH	Configures TX lane clkpath powerup 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE" (default)
1	R/W	PMA_REG_CFG_PMA_POR_N	Configures PMA lane resetn 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE" (default)
0	R/W	PMA_REG_CFG_LANE_POWERUP	Configures PMA lane powerup 1'b0: Corresponds to the parameter value "OFF" 1'b1: Corresponds to the parameter value "ON" (default)

5.3.2 PMA RX Section

Table 5-142 PMA Channel Configuration Register Description: pma_rx_reg0, Offset Address 0x400

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_RX_SIGDET_PD_EN	Enables RX signal to detect power down control from register 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
6	R/W	PMA_REG_RX_SIGDET_PD	rx signal detect power down control 1'b0: Corresponds to the parameter value "ON" (default) 1'b1: Corresponds to the parameter value "OFF"
5	R/W	PMA_REG_RX_DATAPATH_PD_EN	Enables the data path power down control from register, fixed to value 0 1'b0: rsv 1'b1: Corresponds to the parameter value "TRUE" (default)
4	R/W	PMA_REG_RX_DATAPATH_PD	receiver datapath power down control 1'b0: Corresponds to the parameter value "ON" (default) 1'b1: Corresponds to the parameter value "OFF"
3:2	R		Reserved, fixed to value 0
1	R/W	PMA_REG_RX_PD_EN	Enables RX power down control from register, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
0	R/W	PMA_REG_RX_PD	receiver power down 1'b0: Corresponds to the parameter value "ON" (default) 1'b1: Corresponds to the parameter value "OFF"

Table 5-143 PMA Channel Configuration Register Description: pma_rx_reg1, Offset Address 0x401

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_RXPCLK_SLIP_OW	Enables rxpclk slip control from register, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
6	R/W	PMA_REG_RXPCLK_SLIP	1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
5	R/W	PMA_REG_RX_SIGDET_RST_N_EN	Enables the sigdet reset control from register, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
4	R/W	PMA_REG_RX_SIGDET_RST_N	RX signal detect reset register, active low 1'b0: Corresponds to the parameter value "FALSE": reset 1'b1: Corresponds to the parameter value "TRUE": normal (default)

3	R/W	PMA_REG_RX_CDR_RST_N_EN	Enables the CDR reset control from register, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
2	R/W	PMA_REG_RX_CDR_RST_N	CDR reset register, active low 1'b0: Corresponds to the parameter value "FALSE": reset 1'b1: Corresponds to the parameter value "TRUE": normal (default)
1	R/W	PMA_REG_RX_DCC_RST_N_EN	Enables the DCC reset control from register, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
0	R/W	PMA_REG_RX_DCC_RST_N	RX DCC reset register, active low 1'b0: Corresponds to the parameter value "FALSE": reset 1'b1: Corresponds to the parameter value "TRUE": normal (default)

Table 5-144 PMA Channel Configuration Register Description: pma_rx_reg2, Offset Address 0x402

Bits	**R/W**	**Corresponding Parameter Name**	**Description**
7:6	R		Reserved, fixed to value 0
5	R/W	PMA_REG_RX_HIGHZ_EN	Enables the RX highZ control from register, fixed to value 0. 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
4	R/W	PMA_REG_RX_HIGHZ	receiver termination res high z control register 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
3	R/W	PMA_REG_RX_PCLKSWITCH_EN	Enables the TX pclk switch control from register, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
2	R/W	PMA_REG_RX_PCLKSWITCH	rx pclk switch control register: 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
1	R/W	PMA_RX_PCLKSWITCH_RST_N_EN	Enables the RX pclk switch reset control from register, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
0	R/W	PMA_REG_RX_PCLKSWITCH_RST_N	RX sync reset register, active low 1'b0: Corresponds to the parameter value "FALSE": resets RX pclk switch block 1'b1: Corresponds to the parameter value "TRUE": normal operation (default)

Table 5-145 PMA Channel Configuration Register Description: pma_rx_reg3, Offset Address 0x403

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5	R/W	PMA_REG_RX_RESET_N_OW	1’b0: Corresponds to the parameter value “FALSE”, selects the internal state machine (default) 1’b1: Corresponds to the parameter value “TRUE”, selects reg_rx_reset_n
4	R/W	PMA_REG_RX_RESET_N	1’b0: Corresponds to the parameter value “FALSE”, RX reset (default) 1’b1: Corresponds to the parameter value “TRUE”, normal operation
3	R/W	PMA_REG_RX_PD_BIAS_RX_OW	1’b0: Corresponds to the parameter value “FALSE”, selects the internal signal (default) 1’b1: Corresponds to the parameter value “TRUE”, selects reg_rx_pd_bias_rx
2	R/W	PMA_REG_RX_PD_BIAS_RX	1’b0: Corresponds to the parameter value “FALSE”, normal operation (default) 1’b1: Corresponds to the parameter value “TRUE”, RX internal bias circuit power-down
1	R/W	PMA_REG_RX_SIGDET_CLK_WINDOW_OW	1’b0: Corresponds to the parameter value “FALSE”, from the internal circuit (default) 1’b1: Corresponds to the parameter value “TRUE”, selects reg_rx_sigdet_clk_window
0	R/W	PMA_REG_RX_SIGDET_CLK_WINDOW	Register configuration reg_rx_sigdet_clk_window, signal detection clock signal 1’b0: Corresponds to the parameter value “FALSE” (default) 1’b1: Corresponds to the parameter value “TRUE”

Table 5-146 PMA Channel Configuration Register Description: pma_rx_reg4, Offset Address 0x404

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_RX_RATE_EN	RX line rate division ratio control selection, 1’b0: Corresponds to the parameter value “FALSE” (default) Controlled by the port P_RX_RATE 1’b1: Corresponds to the parameter value “TRUE” Controlled by the register PMA_REG_RX_RATE
6	R		Reserved, fixed to value 0

Bits	R/W	Corresponding Parameter Name	Description
5:4	R/W	PMA_REG_RX_RATE	RX line rate division ratio D control register 2'b00: The line rate is 1/4 of the PLL clock frequency; Corresponds to the parameter value "DIV4"; Corresponds to the division ratio of 8 2'b01: The line rate is 1/2 of the PLL clock frequency; Corresponds to the parameter value "DIV2"; Corresponds to the division ratio of 4 2'b10: Line rate and PLL clock frequency are equal (default); Corresponds to the parameter value "DIV1"; Corresponds to the division ratio of 2 2'b11: The line rate is 2 times the PLL clock frequency; Corresponds to the parameter value "MUL2"; Corresponds to the division ratio of 1
3	R/W	PMA_REG_RX_BUSWIDTH_EN	Enables the RX data width control from register, Related to IP configuration 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE" (default)
2:0	R/W	PMA_REG_RX_BUSWIDTH	RX databus width, which is determined by the IP configuration bit[1:0]=2'b00: 8-bit, the parameter value "8BIT" bit[1:0]=2'b01:10-bit, the parameter value "10BIT" bit[1:0]=2'b10:16-bit, the parameter value "16BIT" bit[1:0]=2'b11:20-bit, the parameter value "20BIT" bit[2] is reserved

Table 5-147 PMA Channel Configuration Register Description: pma_rx_reg5, Offset Address 0x405

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5:0	R/W	PMA_REG_RX_RES_TRIM	RX termination resistor calibration register. It defaults to 6'b101110: 100 ohm

Table 5-148 PMA Channel Configuration Register Description: pma_rx_reg6, Offset Address 0x406

Bits	R/W	Corresponding Parameter Name	Description
7:4	R/W	PMA_REG_RX_ICTRL_SIGDET	sigdet bias current control register, [1:0] to control sigdet module, [3:2] to control sigdet preamp module. It defaults to 5
3:2	R		Reserved, fixed to value 0
1	R/W	PMA_REG_RX_SIGDET_STATUS_EN	1'b0: Corresponds to the parameter value "FALSE", selects the internal circuit generation (default) 1'b1: Corresponds to the parameter value "TRUE", selects register reg_rx_sigdet_status control
0	R		Reserved, fixed to value 0

Table 5-149 PMA Channel Configuration Register Description: pma_rx_reg7, Offset Address 0x407

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_CDR_READY_THD[7:0]	bit[7:0] of the register configuration reg_cdr_ready_thd, the default value of reg_cdr_ready_thd is 2734, bit[7:0]=0xAE

Table 5-150 PMA Channel Configuration Register Description: pma_rx_reg8, Offset Address 0x408

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5	R/W	PMA_REG_RX_PCLK_EDGE_SEL	rx pclk edge select, 1'b0: Corresponds to the parameter value "POS_EDGE": rx_pdata is clocked out to TX on the rising edge of rxpclk (default) 1: rx_pdata is clocked out to TX on the falling edge of rxpclk
4	R		Reserved, fixed to value 0
3:0	R/W	PMA_REG_CDR_READY_THD[11:8]	bit[11:8] of the register configuration reg_cdr_ready_thd, the default value of reg_cdr_ready_thd is 2734, bit[11:8]=0xA

Table 5-151 PMA Channel Configuration Register Description: pma_rx_reg9, Offset Address 0x409

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 0
6:5	R/W	PMA_REG_CDR_READY_CHECK_CTRL	CDR ready source selection, fixed to value 0 2'b00: From the cdr_ready_o port (default); 2'b01: From ready_reg_once; 2'b10: From ready_reg; 2'b11:reserved
4:3	R/W	PMA_REG_RX_DCC_IC_RX	RX dcc cml2cmos current dac control, with a default value of 1
2	R		Reserved, fixed to value 0
1:0	R/W	PMA_REG_RX_PIBUF_IC	RX pi buf bandwidth control logic. It defaults to 1

Table 5-152 PMA Channel Configuration Register Description: pma_rx_reg10, Offset Address 0x40a

Bits	R/W	Corresponding Parameter Name	Description
7:4	R		Reserved, fixed to value 5
3:2	R		Reserved, fixed to value 0
1:0	R/W	PMA_REG_RX_ICTRL_TRX	trx global bias current control 2'b00: 87.5%, the parameter value "87_5PCT" 2'b01: 100%, the parameter value "100PCT" (default) 2'b10: 112.5%, the parameter value "112_5PCT" 2'b11: 125%, the parameter value "125PCT"

Table 5-153 PMA Channel Configuration Register Description: pma_rx_reg11, Offset Address 0x40b

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 1
5:4	R/W	PMA_REG_RX_ICTRL_DCC	receiver DCC bias current control 2'b00: 87.5%, the parameter value "87_5PCT" 2'b01: 100%, the parameter value "100PCT" (default) 2'b10: 112.5%, the parameter value "112_5PCT" 2'b11: 125%, the parameter value "125PCT"
3:2	R/W	PMA_REG_RX_ICTRL_PI	phase interpolator path bias current control 2'b00: 87.5%, the parameter value "87_5PCT" 2'b01: 100%, the parameter value "100PCT" (default) 2'b10: 112.5%, the parameter value "112_5PCT" 2'b11: 125%, the parameter value "125PCT"
1:0	R/W	PMA_REG_RX_ICTRL_PIBUF	phase interpolator pre-buffer bias current control 2'b00: 87.5%, the parameter value "87_5PCT" 2'b01: 100%, the parameter value "100PCT" (default) 2'b10: 112.5%, the parameter value "112_5PCT" 2'b11: 125%, the parameter value "125PCT"

Table 5-154 PMA Channel Configuration Register Description: pma_rx_reg12, Offset Address 0x40c

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_TXCLK_SEL	txclk source selection: 1'b0: Corresponds to the parameter value "PLL": selects PLL clock as txclk (default) 1'b1: select rxclk as txclk
6	R/W	PMA_REG_RX_TX2RX_PLPBK_EN	Enables PMA Near-end parallel loopback (via register) 1'b0: Corresponds to the parameter value "FALSE": disable (default) 1'b1: corresponds to the parameter value "TRUE": enable
5	R/W	PMA_REG_RX_TX2RX_PLPBK_RST_N_EN	enable the tx2rx parallel loop back reset control from register 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
4	R/W	PMA_REG_RX_TX2RX_PLPBK_RST_N	RX TX2RX parallel loop back block reset register, active low 1'b0: Corresponds to the parameter value "FALSE": reset tx2rx parallel loop back block 1'b1: Corresponds to the parameter value "TRUE": normal operation (default)

Bits	R/W	Corresponding Parameter Name	Description
3	R/W	PMA_REG_TX_RATE_EN	TX line rate division ratio control selection 1'b0: Corresponds to the parameter value "FALSE" (default) Controlled by the port P_TX_RATE 1'b1: Corresponds to the parameter value "TRUE", Controlled by the register PMA_REG_TX_RATE
2	R		Reserved, fixed to value 0
1:0	R	PMA_REG_TX_RATE	TX line rate division ratio D control register 2'b00: The line rate is 1/4 of the PLL clock frequency; Corresponds to the parameter value "DIV4"; Corresponds to the division ratio of 8 2'b01: The line rate is 1/2 of the PLL clock frequency; Corresponds to the parameter value "DIV2"; Corresponds to the division ratio of 4 2'b10: The line rate is equal to the PLL clock frequency; Corresponds to the parameter value "DIV1" (default); Corresponds to the division ratio of 2 2'b11: The line rate is 2 times the PLL clock frequency; Corresponds to the parameter value "MUL2"; Corresponds to the division ratio of 1

Table 5-155 PMA Channel Configuration Register Description: pma_rx_reg13, Offset Address 0x40d

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	PMA_REG_PRBS_CHK_WIDTH_SEL	Selection of width for PRBS check 2'b00: 8b, corresponds to the parameter value "8BIT" 2'b01: 10b, corresponds to the parameter value "10BIT" 2'b10: 16b, corresponds to the parameter value "16BIT" 2'b11: 20b, corresponds to the parameter value "20BIT" (default)
5	R/W	PMA_REG_PRBS_CHK_EN	PMA RX PRBS check enable 1'b0: Corresponds to the parameter value "FALSE", disabled (default) 1'b1: Corresponds to the parameter value "TRUE", enabled

Bits	R/W	Corresponding Parameter Name	Description
4:3	R/W	PMA_REG_PRBS_SEL	PMA RX PRBS mode selection. It defaults to 2'b00 2'b00: PRBS7, corresponds to the parameter value "PRBS7" 2'b01: PRBS15, corresponds to the parameter value "PRBS15" 2'b10: PRBS23, corresponds to the parameter value "PRBS23" 2'b11: PRBS31, corresponds to the parameter value "PRBS31"
2	R/W	PMA_REG_UDP_CHK_EN	BIST UDP check enable 1'b0: Corresponds to the parameter value "FALSE": disabled (default) 1'b1: Corresponds to the parameter value "TRUE": enabled
1	R/W	PMA_REG_RX_ERR_INSERT	rising edge is used to generate on clock cycle pulse 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
0	R/W	PMA_REG_RX_DATA_POLARITY	RX data polarity inversion control register 1'b0: Corresponds to the parameter value "NORMAL": normal (default) 1'b1: Data bitwise inversion output

Table 5-156 PMA Channel Configuration Register Description: pma_rx_reg14, Offset Address 0x40e

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5:3	R/W	PMA_REG_CDR_PROP_GAIN	proportional gain control: 3'b000: 1/2^12 3'b001: 1/2^11 3'b010: 1/2^10 3'b011: 1/2^9 3'b100: 1/2^8 3'b101: 1/2^7 3'b110: 1/2^6 3'b111: 1/2^5 (default)
2	R/W	PMA_REG_CHK_COUNTER_EN	Checking error detection count enable/clear control 1'b0: Corresponds to the parameter value "FALSE", disable, counter value reset (default) 1'b1: Corresponds to the parameter value "TRUE", enable, counter statistics error
1	R/W	PMA_REG_LOAD_ERR_CNT	Checking error detection counter hold control 1'b0: Corresponds to the parameter value "FALSE", the counter value constantly updates the detected accumulated error value of the current link (default) 1'b1: Corresponds to the parameter value "TRUE", the counter value holds and does not update even if the link has an error
0	R/W	PMA_REG_BIST_CHK_PAT_SEL	BIST constant pattern or PRBS pattern selection 1'b0: Corresponds to the parameter value "PRBS",

Bits	R/W	Corresponding Parameter Name	Description
			PRBS pattern (default) 1'b1: Corresponds to the parameter value "CONSTANT", constant pattern

Table 5-157 PMA Channel Configuration Register Description: pma_rx_reg15, Offset Address 0x40f

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5:3	R/W	PMA_REG_CDR_INT_GAIN	integral gain control 3'b000: 1/2^17 3'b001: 1/2^16 3'b010: 1/2^15 3'b011: 1/2^14 3'b100: 1/2^13(default) 3'b101: 1/2^12 3'b110: 1/2^11 3'b111: 1/2^10
2:0	R/W	PMA_REG_CDR_PROP_TURBO_GAIN	turbo proportional gain control: (refer to the PI control value) 3'b000: 1/2^12 3'b001: 1/2^11 3'b010: 1/2^10 3'b011: 1/2^9 3'b100: 1/2^8 3'b101: 1/2^7(default) 3'b110: 1/2^6 3'b111: 1/2^5

Table 5-158 PMA Channel Configuration Register Description: pma_rx_reg16, Offset Address 0x410

Bits	R/W	Corresponding Parameter Name	Description
7:3	R/W	PMA_REG_CDR_INT_SAT_MAX[4:0]	Maximum positive deviation of integration path, CDR_INT_SAT_MAX[4:0]=5'b00000(default)
2:0	R/W	PMA_REG_CDR_INT_TURBO_GAIN	turbo integral gain control: (refer to the PI control value) 3'b000: 1/2^17 3'b001: 1/2^16 3'b010: 1/2^15 3'b011: 1/2^14 3'b100: 1/2^13 3'b101: 1/2^12(default) 3'b110: 1/2^11 3'b111: 1/2^10

Table 5-159 PMA Channel Configuration Register Description: pma_rx_reg17, Offset Address 0x411

Bits	R/W	Corresponding Parameter Name	Description
7:5	R/W	PMA_REG_CDR_INT_SAT_MIN[2:0]	Maximum negative deviation of integration path, CDR_INT_SAT_MIN[2:0]=3'b111(default)
4:0	R/W	PMA_REG_CDR_INT_SAT_MAX[9:5]	Maximum positive deviation of integration path, CDR_INT_SAT_MAX[9:5]=5'b11000(default)

Table 5-160 PMA Channel Configuration Register Description: pma_rx_reg18, Offset Address 0x412

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 0
6:0	R/W	PMA_REG_CDR_INT_SAT_MIN[9:3]	Maximum negative deviation of integration path, CDR_INT_SAT_MIN [9:3] =7'b0011111(default)

Table 5-161 PMA Channel Configuration Register Description: pma_rx_reg19, Offset Address 0x413

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 0
6	R/W	PMA_REG_CDR_RX_PI_FORCE_SEL	CDR RX PI control force value selection. 1'b0: rx pi ctrl using the accumulator output (default) 1'b1: rx pi ctrl using the force data(Bypass CDR) Notes: 1. In Bypass CDR scenarios, the auto-adjust function for equalization needs to be disabled as well. To do so, configures the register's 0x429 Bit[0] and 0x42a Bit[4] to 1; 2. After dynamically configuring Bypass CDR related configurations, a global reset of HSSTLP or reset of RX LANE is required.
5	R/W	PMA_REG_CDR_LOCK_RST_OW	CDR lock counter reset overwrite 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
4	R/W	PMA_REG_CDR_LOCK_RST	CDR lock counter reset, active-high 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE": reset
3	R/W	PMA_REG_CDR_PROP_RST_OW	CDR proportional path reset overwrite 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
2	R/W	PMA_REG_CDR_PROP_RST	CDR proportional path reset, active-high 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE": reset
1	R/W	PMA_REG_CDR_INT_RST_OW	CDR integral path reset overwrite 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
0	R/W	PMA_REG_CDR_INT_RST	CDR integral path reset, active-high 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE": reset

Table 5-162 PMA Channel Configuration Register Description: pma_rx_reg20, Offset Address 0x414

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_CDR_RX_PI_FORCE_D	CDR RX PI control force data, value range

			0~255. It defaults to 0

Table 5-163 PMA Channel Configuration Register Description: pma_rx_reg21, Offset Address 0x415

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_CDR_INT_SAT_DET_EN	Integral path saturation detection enable: 1'b0: Corresponds to the parameter value "FALSE": disable 1'b1: corresponds to the parameter value "TRUE": enable (default)
6	R/W	PMA_REG_CDR_LOCK_OW	CDR lock detection (cdr_ready) overwrite enable 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
5	R/W	PMA_REG_CDR_LOCK_VAL	CDR lock detection overwrite value 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE": reset
4:3	R/W	PMA_REG_CDR_TURBO_MODE_TIMER	2'b00:turbo_mode time equal to the lock time 2'b01:turbo_mode time 3/4 of the lock time(default) 2'b10:turbo_mode time 1/2 of the lock time 2'b11:turbo_mode time 1/4 of the lock time
2:0	R/W	PMA_REG_CDR_LOCK_TIMER	CDR lock detection pseudo timer control (for 312.5MHz clock) 3'b000: Corresponds to the parameter "0_8U", 256 cycles 3'b001: Corresponds to the parameter "1_2U", 384 cycles (PCIE default) 3'b010: Corresponds to the parameter "1_6U", 512 cycles 3'b011: Corresponds to the parameter "2_4U", 768 cycles 3'b100: Corresponds to the parameter "3_2U", 1024 cycles 3'b101: Corresponds to the parameter "4_8U", 1536 cycles 3'b110: Corresponds to the parameter "12_8U", 4096 cycles 3'b111: Corresponds to the parameter "25_6U", 8191 cycles (others default)

Table 5-164 PMA Channel Configuration Register Description: pma_rx_reg22, Offset Address 0x416

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		Reserved, fixed to value 0
2	R/W	PMA_REG_CDR_TURBO_GAIN_AUTO	Turbo Gain select signal 1'b0: Corresponds to the parameter value "FALSE", cdr_turbo_prop_gain_sel directly

Bits	R/W	Corresponding Parameter Name	Description
			comes from reg_cdr_turbo_prop_gain_sel, and cdr_turbo_int_gain_sel directly comes from reg_cdr_turbo_int_gain_sel (default) 1'b1: Corresponds to the parameter value "TRUE", internal circuit generation
1	R/W	PMA_REG_CDR_GAIN_AUTO	Gain select signal 1'b0: Corresponds to the parameter value "FALSE", cdr_prop_gain_sel directly comes from reg_cdr_prop_gain_sel, and cdr_int_gain_sel directly comes from reg_cdr_int_gain_sel (default) 1'b1: Corresponds to the parameter value "TRUE", internal circuit generation
0	R/W	PMA_REG_CDR_SAT_AUTO_DIS	CDR_SAT_MAX selection control signal 1'b0: Corresponds to the parameter value "FALSE", selects internal circuit generation signal 1'b1: Corresponds to the parameter value "TRUE", cdr_sat_max directly comes from reg_cdr_sat_max, and cdr_sat_min directly comes from reg_cdr_sat_min (default)

Table 5-165 PMA Channel Configuration Register Description: pma_rx_reg23, Offset Address 0x417

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_CDR_PI_CTRL_RST_OW	CDR pi control reset overwrite, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE"
6	R/W	PMA_REG_CDR_PI_CTRL_RST	CDR pictrl reset register, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE"
5	R/W	PMA_REG_CDR_SAT_DET_STATUS_RESET_EN	When the CDR saturation is detected, reset the CDR: 1'b0: Corresponds to the parameter value "FALSE", disable (default) 1'b1: Corresponds to the parameter value "TRUE", enable
4	R/W	PMA_REG_CDR_SAT_DET_STATUS_EN	Enable CDR saturation status detection: 1'b0: Corresponds to the parameter value "FALSE", disable (default) 1'b1: Corresponds to the parameter value "TRUE", enable
3:0	R		Reserved, fixed to value 0

Table 5-166 PMA Channel Configuration Register Description: pma_rx_reg24, Offset Address 0x418

Bits	R/W	Corresponding Parameter Name	Description

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 0
6:5	R/W	PMA_REG_CDR_SAT_DET_TIMER	2'b00: 64 out ot 1024 cycles saturation detected is reckoned as saturation 2'b01: 128 out ot 1024 cycles saturation detected is reckoned as saturation 2'b10: 256 out ot 1024 cycles saturation detected is reckoned as saturation(default) 2'b11: 512 out ot 1024 cycles saturation detected is reckoned as saturation
4	R/W	PMA_REG_CDR_SIGDET_STATUS_DIS	Disable the sigdet_status. 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE".
3	R/W	PMA_REG_CDR_SAT_DET_STICKY_RST_OW	CDR saturation detection status sticky reset overwrite, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE"
2	R/W	PMA_REG_CDR_SAT_DET_STICKY_RST	CDR saturation detection status sticky reset, active-high. 1'b0: Corresponds to the parameter value "FALSE", disable (default) 1'b1: Corresponds to the parameter value "TRUE": reset.
1	R/W	PMA_REG_CDR_SAT_DET_RST_OW	CDR saturation detection reset overwrite, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE"
0	R/W	PMA_REG_CDR_SAT_DET_RST	CDR saturation detection reset, active-high. 1'b0: Corresponds to the parameter value "FALSE", disable (default) 1'b1: Corresponds to the parameter value "TRUE", reset

Table 5-167 PMA Channel Configuration Register Description: pma_rx_reg25, Offset Address 0x419

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_CDR_STATUS_FIFO_EN	Enable signal of CDR status FIFO 1'b0: Corresponds to the parameter value "FALSE": disabled 1'b1: Corresponds to the parameter value "TRUE": enabled (default)
6:3	R		Reserved, fixed to value 0
2	R/W	PMA_REG_CDR_TURBO_MODE_EN	CDR turbo mode enable: 1'b0: Corresponds to the parameter value "FALSE": disabled 1'b1: Corresponds to the parameter value "TRUE": enabled (default)

Bits	R/W	Corresponding Parameter Name	Description
1	R/W	PMA_REG_CDR_SAT_DET_STATUS_OW	CDR saturation detection status overwrite enable, fixed to value 0 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE"
0	R/W	PMA_REG_CDR_SAT_DET_STATUS_VAL	register for CDR saturation detection status overwrite 1'b0: Corresponds to the parameter value "FALSE", disable (default) 1'b1: Corresponds to the parameter value "TRUE", reset

Table 5-168 PMA Channel Configuration Register Description: pma_rx_reg26, Offset Address 0x41a

Bits	R/W	Corresponding Parameter Name	Description
7:3	R/W	PMA_REG_OOB_COMWAKE_GAP_MIN[4:0]	Minimum length threshold for a COMWAKE signal gap. (4/75M~53ns), with a default value of 3
2:0	R/W	PMA_REG_PMA_TEST_SEL	Select which signal connected to fifo for test 3'b000: CDR pictrl value(default) 3'b001: cdr int data others reserved

Table 5-169 PMA Channel Configuration Register Description: pma_rx_reg27, Offset Address 0x41b

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 0
6:1	R/W	PMA_REG_OOB_COMWAKE_GAP_MAX	Maximum length threshold for a COMWAKE signal gap. (12/75M~160ns), with a default value of 11
0	R/W	PMA_REG_OOB_COMWAKE_GAP_MIN[5]	Minimum length threshold for a COMWAKE signal gap. (4/75M~53ns), It defaults to 0.

Table 5-170 PMA Channel Configuration Register Description: pma_rx_reg28, Offset Address 0x41c

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_OOB_COMINIT_GAP_MIN	Minimum length threshold for a COMINIT signal gap. (16/75M~213ns), with a default value of 15

Table 5-171 PMA Channel Configuration Register Description: pma_rx_reg29, Offset Address 0x41d

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_OOB_COMINIT_GAP_MAX	Maximum length threshold for a COMINIT signal gap. (36/75M~480ns), with a default value of 35

Table 5-172 PMA Channel Configuration Register Description: pma_rx_reg30, Offset Address 0x41e

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5	R/W	PMA_REG_RX_SYNC_RST_N	rx sync module reset register 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE" (default)
4	R/W	PMA_REG_RX_SYNC_RST_N_EN	rx sync module reset overwrite 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
3	R/W	PMA_REG_COMINIT_STATUS_CLEAR	Clears the COMINIT detected by the circuit when high It defaults to 0.
2	R/W	PMA_REG_COMWAKE_STATUS_CLEAR	Clears the COMWAKE detected by the circuit when high It defaults to 0.
1:0	R		Reserved, fixed to value 1

Table 5-173 PMA Channel Configuration Register Description: pma_rx_reg31, Offset Address 0x41f

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5	R/W	PMA_REG_RX_SATA_COMWAKE	1'b0: Corresponds to the parameter value "FALSE", COMWAKE signal is not detected(default) 1'b1: Corresponds to the parameter value "TRUE", COMWAKE signal is detected
4	R/W	PMA_REG_RX_SATA_COMWAKE_OW	rx COMWAKE signal in sata mode overwrite: 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
3	R/W	PMA_REG_RX_SATA_COMINIT	1'b0: Corresponds to the parameter value "FALSE", COMINIT signal is not detected (default) 1'b1: Corresponds to the parameter value "TRUE", COMINIT signal is detected
2	R/W	PMA_REG_RX_SATA_COMINIT_OW	rx COMINIT signal in sata mode overwrite: 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
1:0	R		Reserved, fixed to value 0

Table 5-174 PMA Channel Configuration Register Description: pma_rx_reg32, Offset Address 0x420

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_RX_SLIP_EN	1'b0: Corresponds to the parameter value "FALSE", CDR demux works normally(default) 1'b1: Corresponds to the parameter value "TRUE", bypass CDR demux

Bits	R/W	Corresponding Parameter Name	Description
6:3	R/W	PMA_REG_RX_SLIP_SEL	Slip output selection signal based on counter value of slip control. It defaults to 0
2	R/W	PMA_REG_RX_SLIP_SEL_EN	overwrite enable of rx slip 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
1	R		Reserved, fixed to value 0
0	R/W	PMA_REG_RX_DCC_DISABLE	rx dcc disable control: 1'b0: Corresponds to the parameter value "FALSE", rx dcc is enable (default) 1'b1: Corresponds to the parameter value "TRUE", rx dcc is disable.

Table 5-175 PMA Channel Configuration Register Description: pma_rx_reg33, Offset Address 0x421

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5	R/W	PMA_REG_RX_SIGDET_STATUS	rx signal detection status: 1'b0: Corresponds to the parameter value "FALSE", no signal detected (default) 1'b1: Corresponds to the parameter value "TRUE", input signal is detected
4	R		Reserved, fixed to value 0
3	R/W	PMA_REG_RX_SIGDET_FSM_RST_N	rx signal status post process fsm resetn: 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE" (default)
2:0	R/W	PMA_REG_RX_SIGDET_STATUS_SEL	rx signal detection status signals selection: 3'b000: channel 1 (comparator based signal detector) 3'b001: channel 2 (comparator based signal detector+ check window filter) 3'b010: channel 3 (slicer based signal detector) 3'b011: channel1 || channel2 3'b100: channel1 || channel3 3'b101: channel1 || channel2 || channel3 || channel4 (default) 3'b110: channel2 || channel3 3'b111: channel 4

Table 5-176 PMA Channel Configuration Register Description: pma_rx_reg34, Offset Address 0x422

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_RX_SIGDET_CH2_SEL	rx signal detect channel 2 input signal selection. 1'b0: the RC filtered comparison signal is sent to detect channel 2 (default) 1'b1: the comparison signal is directly sent to signal detect channel 2
6	R/W	PMA_REG_RX_SIGDET_PULSE_EXT	signal pulse extention enable for rx signal detection. 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
5:4	R/W	PMA_REG_RX_SIGDET_GRM	glitch remove setting for rx signal detection. It defaults to 2'b00
3:0	R/W	PMA_REG_RX_SIGDET_VTH	RX single-ended peak-to-peak threshold control, HSSTLP IP can be configured as: bit[3:0]=4'b0110: the parameter value "63MV" (reserved) bit[3:0]=4'b0111: the parameter value "72MV" others:Reserved

Note: Principles for setting the PMA_REG_RX_SIGDET_VTH threshold:
1. The 72MV in the description is the RX threshold control level setting and does not represent the input noise tolerance of the RX signal detection function;
2. The noise differential peak-to-peak value at the RX input and the threshold control level should meet the following relationship:

Noise at the RX input (differential peak-to-peak value)	Threshold control level selection
≤54mV	"72MV"
>54mV	Requires noise reduction at RX input

3. The threshold control function outputs signal detection status via the port P_RX_SIGDET_STATUS;
4. Evaluation method for noise differential at RX input: For applications with electrical idle mode (electrical_idle, such as the PCIE protocol), evaluate in the electrical idle mode at the TX end; for other serdes applications without electrical idle mode, evaluate in the TX shutdown mode (set to power down mode: TX is powered up normally, but there is no AC signal at the TX end);
5. The 63MV is a reserved level; please contact the manufacturer for estimation if needed.

Table 5-177 PMA Channel Configuration Register Description: pma_rx_reg35, Offset Address 0x423

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5	R/W	PMA_REG_RX_SIGDET_CHK_WINDOW_EN	if high, sigdet fsm use check window to filter sigdet otherwise send out directly. 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE" (default)
4:0	R/W	PMA_REG_RX_SIGDET_CH2_CHK_WINDOW	Channel 2 sigdet filter check window is configurable from 1 cycle to 32 cycles. It defaults to 3.

Table 5-178 PMA Channel Configuration Register Description: pma_rx_reg36, Offset Address 0x424

Bits	R/W	Corresponding Parameter Name	Description
7:5	R/W	PMA_REG_RX_SIGDET_OOB_DET_COUNT_VAL[2:0]	Counter value of sigdet in OOB detection mode. It defaults to 0.
4	R/W	PMA_REG_SLIP_FIFO_INV	Slip fifo clock domain edge select signal. 1'b0: Corresponds to the parameter value "POS_EDGE" (default) 1'b1: Corresponds to the parameter value "NEG_EDGE"
3	R/W	PMA_REG_SLIP_FIFO_INV_EN	owerwrite enable of Slip fifo clock domain edge select 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
2:0	R/W	PMA_REG_RX_SIGDET_NOSIG_COUNT_SETTING	counter of consecutive clock cycls during which no signal is detected. 3'b000: nosig_count_timeout=8'd0 3'b001: nosig_count_timeout=8'd3 3'b010: nosig_count_timeout=8'd7 3'b011: nosig_count_timeout=8'd15 3'b100: nosig_count_timeout=8'd31 (default) 3'b101: nosig_count_timeout=8'd63 3'b110: nosig_count_timeout=8'd127 3'b111: nosig_count_timeout=8'd255

Table 5-179 PMA Channel Configuration Register Description: pma_rx_reg37, Offset Address 0x425

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved, fixed to value 0
4:2	R/W	PMA_REG_RX_SIGDET_4OOB_DET_SEL	It's for oob application. rx signal detection status signals selection: 3'b000: channel 1 (comparator based signal detector) 3'b001: channel 2 (comparator based signal detector+ check window filter) 3'b010: channel 3 (slicer based signal detector) 3'b011: channel1 || channel2 3'b100: channel1 || channel3 3'b101: channel1 || channel2 || channel3 || channel4 3'b110: channel2 || channel3 3'b111: channel 4(default)
1:0	R/W	PMA_REG_RX_SIGDET_OOB_DET_COUNT_VAL[4:3]	Counter value of sigdet in OOB detection mode. It defaults to 0.

Table 5-180 PMA Channel Configuration Register Description: pma_rx_reg38, Offset Address 0x426

Bits	R/W	Corresponding Parameter Name	Description
7	R/W	PMA_REG_RX_OOB_DETECTOR_PD_OW	rx oob detector powerdown overwrite 1'b0: Corresponds to the parameter value "FALSE", uses FSM output signal (default) 1'b1: Corresponds to the parameter value "TRUE", uses reg_rx_oob_detector_pd
6	R/W	PMA_REG_RX_OOB_DETECTOR_RESET_N	RX OOB detector reset register, active low 1'b0: Corresponds to the parameter value "FALSE", resets RX OOB detector (default) 1'b1: Corresponds to the parameter value "TRUE", normal operation
5	R/W	PMA_REG_RX_OOB_DETECTOR_RESET_N_OW	Enable the oob detector reset control from register 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
4:1	R/W	PMA_REG_RX_SIGDET_IC_I	RX signal detector mux and comparator current control. It defaults to 10
0	R		Reserved, fixed to value 0

Table 5-181 PMA Channel Configuration Register Description: pma_rx_reg39, Offset Address 0x427

Bits	R/W	Corresponding Parameter Name	Description
7:6	R		Reserved, fixed to value 0
5:4	R/W	PMA_REG_RX_EQ1_R_SET_TOP	2'b00: 150 ohm (default) 2'b01: 110 ohm Other values: reserved
3	R/W	PMA_REG_ANA_RX_EQ2_R_SET_FB_O_SEL	1'b0: Corresponds to the parameter value "FALSE", manually adjusts the EQ2 value using PMA_REG_RX_EQ2_R_SET_FB 1'b1: Corresponds to the parameter value "TRUE", auto-adjusts the EQ2 value (default)
2	R/W	PMA_REG_ANA_RX_EQ1_R_SET_FB_O_SEL	1'b0: Corresponds to the parameter value "FALSE", manually adjusts the EQ1 value using PMA_REG_RX_EQ1_R_SET_FB 1'b1: Corresponds to the parameter value "TRUE", auto-adjust the EQ1 value (default)

Bits	R/W	Corresponding Parameter Name	Description
1	R/W	PMA_REG_RX_LS_MODE_EN	Register configuration low-speed mode enable signal 1’b0: Corresponds to the parameter value “FALSE” Disables low-speed mode (default) 1’b1: Corresponds to the parameter value “TRUE” Enables low-speed mode
0	R/W	PMA_REG_RX_OOB_DETECTOR_PD	rx oob detector powerdown: 1’b0: Corresponds to the parameter value “ON” poweron rx oob detector(default) 1: powerdown rx oob detector

Table 5-182 PMA Channel Configuration Register Description: pma_rx_reg40, Offset Address 0x428

Bits	R/W	Corresponding Parameter Name	Description
7:4	R/W	PMA_REG_RX_EQ1_C_SET_FB	EQ1 AC cap setting. It defaults to 0
3:0	R/W	PMA_REG_RX_EQ1_R_SET_FB	EQ1 setting value. It defaults to 15, valid when manually adjusted, 0.5dB/step During the adjustment, EQ1 and EQ2 setting values must be equal, equivalent to an EQ value of 1dB/step

Table 5-183 PMA Channel Configuration Register Description: pma_rx_reg41, Offset Address 0x429

Bits	R/W	Corresponding Parameter Name	Description
7	R		Reserved, fixed to value 0
6:3	R/W	PMA_REG_RX_EQ2_R_SET_FB	EQ2 setting valueIt defaults to 0, valid when manually adjusted, 0.5dB/step During the adjustment, EQ1 and EQ2 setting values must be equal, equivalent to an EQ value of 1dB/step
2:1	R/W	PMA_REG_RX_EQ2_R_SET_TOP	2’b00: 150 ohm (default) 2’b01: 110 ohm Other values: reserved
0	R/W	PMA_REG_RX_EQ1_OFF	Shut off equalisation for 1st stage of EQ1 1’b0: Corresponds to the parameter value “FALSE” (default) 1’b1: Corresponds to the parameter value “TRUE”

Table 5-184 PMA Channel Configuration Register Description: pma_rx_reg42, Offset Address 0x42a

Bits	R/W	Corresponding Parameter Name	Description
7:5	R		Reserved, fixed to value 0
4	R/W	PMA_REG_RX_EQ2_OFF	Shut off equalization for 2nd stage of EQ2 1’b0: Corresponds to the parameter value “FALSE” (default) 1’b1: Corresponds to the parameter value “TRUE”
3:0	R/W	PMA_REG_RX_EQ2_C_SET_FB	EQ2 AC cap setting. It defaults to 0

Table 5-185 PMA Channel Configuration Register Description: pma_rx_reg43, Offset Address 0x42b

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	PMA_REG_RX_ICTRL_EQ	Eq base current setting. 2'b00: 87.5% 2'b01: 100% 2'b10: 112.5%(default) 2'b11: 125%
5:0	R/W	PMA_REG_EQ_DAC	EQ DC offset current DAC setting. It defaults to 0

Table 5-186 PMA Channel Configuration Register Description: pma_rx_reg44, Offset Address 0x42c

Bits	R/W	Corresponding Parameter Name	Description
7:2	R		Reserved, fixed to value 0
1	R/W	PMA_REG_EQ_DC_CALIB_SEL	Dc offset calib sel 1'b0: Corresponds to the parameter value "FALSE", EQ negative output is selected for calib(default) 1'b1: Corresponds to the parameter value "TRUE", EQ positive output is selected for calib
0	R/W	PMA_REG_EQ_DC_CALIB_EN	DC calibration enable signal 1'b0: Corresponds to the parameter value "FALSE", disable 1'b1: Corresponds to the parameter value "TRUE", enable (default)

Table 5-187 PMA Channel Configuration Register Description: pma_rx_reg45, Offset Address 0x42d

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_RX_RESERVED_337_330	reg_rx_config_reserved. It defaults to 0

Table 5-188 PMA Channel Configuration Register Description: pma_rx_reg46, Offset Address 0x42e

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_RX_RESERVED_345_338	reg_rx_config_reserved. It defaults to 0

Table 5-189 PMA Channel Configuration Register Description: pma_rx_reg47, Offset Address 0x42f

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_RX_RESERVED_353_346	reg_rx_config_reserved, related to IP configuration

Table 5-190 PMA Channel Configuration Register Description: pma_rx_reg48, Offset Address 0x430

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_REG_RX_RESERVED_361_354	reg_rx_config_reserved. It defaults to 0

Table 5-191 PMA Channel Configuration Register Description: pma_rx_reg49, Offset Address 0x431

Bits	R/W	Corresponding Parameter Name	Description

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	PMA_CTLE_REG_INIT_DAC_I[1:0]	CTLE adaptive DAC initial value, which defaults to 0
5	R/W	PMA_CTLE_REG_HOLD_I	Accumulator hold enable signal 1'b0: Corresponds to the parameter value "FALSE", Postadder normal operation (default) 1'b1: Corresponds to the parameter value "TRUE" Maintains the current status
4	R/W	PMA_CTLE_REG_FORCE_SEL_I	Selection configuration signal 1'b0: Corresponds to the parameter value "FALSE", Output auto-adjust result (default) 1'b1: Corresponds to the parameter value "TRUE" Output external register pma_rx_reg49[3:0]
3:0	R/W	PMA_CTLE_CTRL_REG_I	Gain adjustment configuration value of the register configuration. It defaults to 0

Table 5-192 PMA Channel Configuration Register Description: pma_rx_reg50, Offset Address 0x432

Bits	R/W	Corresponding Parameter Name	Description
7:6	R/W	PMA_CTLE_REG_THRESHOLD_I[1:0]	Threshold value required by the self-use lock_detect module. It defaults to 3072, bit[1:0]=0 (default)
5:3	R/W	PMA_CTLE_REG_SHIFTER_GAIN_I	Initial gain setting. It defaults to 1
2	R/W	PMA_CTLE_REG_POLARITY_I	CTLE module input polarity indicator signal 1'b0: Corresponds to the parameter value "FALSE", no polarity inversion (default) 1'b1: Corresponds to the parameter value "TRUE", performs input signal polarity inversion
1:0	R/W	PMA_CTLE_REG_INIT_DAC_I[3:2]	CTLE adaptive DAC initial value, which defaults to 0

Table 5-193 PMA Channel Configuration Register Description: pma_rx_reg51, Offset Address 0x433

Bits	R/W	Corresponding Parameter Name	Description
7:0	R/W	PMA_CH_CTLE_REG_THRESHOLD_I[9:2]	Threshold value required by the self-use lock_detect module. It defaults to 3072, bit[9:2]=0 (default)

Table 5-194 PMA Channel Configuration Register Description: pma_rx_reg52, Offset Address 0x434

Bits	R/W	Corresponding Parameter Name	Description
7:3	R		Reserved, fixed to value 0
2	R/W	PMA_REG_RX_RES_TRIM_EN	Enable rx termination resistor calibration control from register 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE" (default)
1:0	R/W	PMA_CTLE_REG_THRESHOLD_I[11:10]	Threshold value required by the self-use lock_detect module. It defaults to 3072,

			bit[11:10]=2'b11 (default)

Table 5-195 PMA Channel Configuration Register Description: pma_rx_reg53, Offset Address 0x435

Bits	**R/W**	**Corresponding Parameter Name**	**Description**
7:6	R		Reserved, fixed to value 0
5	R		PMA interrupt, 1: valid interrupt, pma_prbs_err
4	R/W	PMA_CFG_CTLE_ADP_RSTN	Register configuration pma_lane_reg53[4] 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE" (default)
3	R/W	PMA_INT_PMA_RX_CLR_0	PMA interrupt clear 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
2	R/W	PMA_INT_PMA_RX_MASK_0	PMA interrupt mask 1'b0: Corresponds to the parameter value "FALSE" (default) 1'b1: Corresponds to the parameter value "TRUE"
1	R/W	PMA_CFG_RX_PMA_RSTN	Register configuration pma_lane_reg53[1] 1'b0: Corresponds to the parameter value "FALSE" 1'b1: Corresponds to the parameter value "TRUE" (default)
0	R/W	PMA_CFG_RX_LANE_POWERUP	Register configuration pma_lane_reg53[0] 1'b0: Corresponds to the parameter value "OFF" 1'b1: Corresponds to the parameter value "ON" (default)

Table 5-196 PMA Channel Configuration Register Description: pma_rx_reg54, Offset Address 0x436

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	REG_RX_ERR_COUNTER[7:0]	Checking error counter in PMA PRBS checker REG_RX_ERR_COUNTER[7:0]

Table 5-197 PMA Channel Configuration Register Description: pma_rx_reg55, Offset Address 0x437

Bits	**R/W**	**Corresponding Parameter Name**	**Description**
7:0	R	REG_RX_ERR_COUNTER[15:8]	Checking error counter in PMA PRBS checker REG_RX_ERR_COUNTER[15:8]

Table 5-198 PMA Channel Configuration Register Description: pma_rx_reg56, Offset Address 0x438

Bits	**R/W**	**Corresponding Parameter Name**	**Description**
7:0	R	REG_RX_ERR_COUNTER[23:16]	Checking error counter in PMA PRBS checker REG_RX_ERR_COUNTER[23:16]

Table 5-199 PMA Channel Configuration Register Description: pma_rx_reg57, Offset Address 0x439

Bits	R/W	Corresponding Parameter Name	Description
7:0	R	REG_RX_ERR_COUNTER[31:24]	Checking error counter in PMA PRBS checker After the counter REG_RX_ERR_COUNTER[31:24] accumulates to the maximum value, it will reset to 0 and start accumulating again.

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