Compa Family CPLDs Dedicated RAM Module (DRM) User Guide

(UG030002, V1.2)

(03.03.2020)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.2	03.03.2020	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
DRM	Dedicated RAM Module
DP	Dual Port
SDP	Simple Dual Port
SP	Single Port
NW	Normal Write
RBW	Read before Write
TW	Transparent Write
BW	Byte Write
OR	Output Register
IPC	IP Compiler

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Chapter 1 Overview

The DRM of the Compa Family CPLDs has storage units of up to 9K bits, and two adjacent DRMs can be combined into one 16Kx1 memory without the need for additional external logic. Each DRM supports DP (True Dual Port) RAM mode, and can also be configured as SP (Single Port) RAM mode, SDP (Simple Dual Port) RAM mode, ROM mode, as well as synchronous/asynchronous FIFO mode. DRM resources also support Input Register (IR) and Output Register (OR), allowing superior performance when DRMs are cascaded. The total number of DRMs depends on the type of Compa Family device.

The port data width of DP RAM mode goes up to 9 bits, with its two ports being completely independent apart from sharing RAM content, and supporting different clock domains; the port data width of SDPRAM goes up to 18 bits, with its two ports also supporting different clock domains, but one port is limited to write operations and the other is limited to read operations. In ROM mode, the port data width of the ROM can be up to 18 bits. The content of the DRM is typically initialized during the process of downloading FPGA's configuration data. Of course, the content of the DRM can also be initialized using FPGA's programmed configurations in other modes. In synchronous or asynchronous FIFO mode, one port is dedicated to FIFO data writing, and the other port is dedicated to FIFO data reading; read and write ports can support different clocks, but do not support mixed bit widths or byte enable write operations. Two adjacent DRMs can be combined into one 16Kx1 memory without the need for additional external logic. The DRM function overview list is shown in Table 1-1.

DPRAM, SPRAM, SDPRAM, ROM, and synchronous/asynchronous FIFO modules can be conveniently generated through the IP Compiler tool embedded in the Pango Design Suite software by Shenzhen Pango Microsystems Co., Ltd.

1.1 Features

The DRM function overview list for the Compa Family CPLDs is shown in Table 1-1.

Table 1-1 Function Overview List

Function Overview List	
Memory Capacity	9Kbits
Configurable Mode	Dual-port, simple dual-port, single-port, ROM, FIFO modes
DRM Configuration	Dual-port: 8Kx1/4Kx2/2Kx4/1Kx8/1Kx9
	Simple dual-port: 8Kx1/4Kx2/2Kx4/1Kx8/512x16/1Kx9/512x18

Function Overview List	
	Single-port: 8Kx1/4Kx2/2Kx4/1Kx8/512x16/1Kx9/512x18
	FIFO: 8Kx1/4Kx2/2Kx4/1Kx8/512x16/1Kx9/512x18
Write Mode	Normal Write mode supported
	Transparent Write mode supported
	Read-Before Write mode supported
Reset Mode	Synchronous reset supported
	Asynchronous reset supported
	Independent reset of A/B ports supported
Output clock inversion supported	
Configurable output registers during reset/set supported	
Configurable address hold supported	
Configurable output register supported	
Independent configuration of bit widths for ports A and B of dual-port supported	
Byte write enable supported	
Input register supported	
Read and write operations require only one clock cycle (two clock cycles are required when the output register is enabled)	
Combining two adjacent DRMs into one 16Kx1 memory without additional external logic is supported	
Read/write pointer output in FIFO mode supported	

1.2 Supported Configurations

1.2.1 DPRAM Mode

In DPRAM mode, DRM has a maximum data width of 9 bits, the bit widths of the two ports can be independently configured according to DRM resources. In the DRM module, both A and B ports can independently perform read and write operations, each supporting an independent clock. The allowed bit width combinations for DPRAM mode are shown in Table 1-2.

Table 1-2 Allowed Bit Width Combinations for DPRAM Mode

		Port B				
		8Kx1	**4Kx2**	**2Kx4**	**1Kx8**	**1Kx9**
Port A	**8Kx1**	√	√	√	√	
	4Kx2	√	√	√	√	
	2Kx4	√	√	√	√	
	1Kx8	√	√	√	√	
	1Kx9					√

1.2.2 SDPRAM Mode

In SDPRAM mode, the DRM data width increases to 18 bits, with one port dedicated to data writing and the other for data reading, both read and write ports also support different clocks. The allowed bit width combinations for SDPRAM mode are shown in Table 1-3.

Table 1-3 Allowed Bit Width Combinations for SDPRAM Mode

		Write Port						
		8Kx1	**4Kx2**	**2Kx4**	**1Kx8**	**512x16**	**1Kx9**	**512x18**
Read Port	8Kx1	√	√	√	√	√		
	4Kx2	√	√	√	√	√		
	2Kx4	√	√	√	√	√		
	1Kx8	√	√	√	√	√		
	512x16	√	√	√	√	√		
	1Kx9						√	√
	512x18						√	√

1.2.3 SPRAM Mode and ROM Mode

The allowed bit width combinations for SPRAM mode and ROM mode are shown in Table 1-4.

Table 1-4 Allowed Bit Width Combinations for SPRAM Mode and ROM Mode

		8Kx1	**4Kx2**	**2Kx4**	**1Kx8**	**512x16**	**1Kx9**	**512x18**
Mode	**SP RAM**	√	√	√	√	√	√	√
	ROM	√	√	√	√	√	√	√

1.2.4 Data Width

In DRM memory mode, the corresponding address and data port mapping can be seen in Table 1-5, and the data address mapping for different bit widths can be seen in Table 1-6 and Table 1-7.

Table 1-5 Table Address and Data Port Mapping Corresponding to DRM Memory Mode

DRM Port Mode	**Address and Data Port Mapping**					
	Port A Address	**Port B Address**	**Port A data input**	**Port B data input**	**Port A data output**	**Port B data output**
8K*1	ADDRA [12:0]	ADDRB [12:0]	DIA [0]	DIB [0]	DOA [0]	DOB [0]
4K*2	ADDRA [12:1]	ADDRB [12:1]	DIA [1:0]	DIB [1:0]	DOA [1:0]	DOB [1:0]
2K*4	ADDRA [12:2]	ADDRB [12:2]	DIA [3:0]	DIB [3:0]	DOA [3:0]	DOB [3:0]
1K*8	ADDRA [12:3]	ADDRB [12:3]	DIA [7:0]	DIB [7:0]	DOA [7:0]	DOB [7:0]
1K*9	ADDRA [12:3]	ADDRB [12:3]	DIA [8:0]	DIB [8:0]	DOA [8:0]	DOB [8:0]

DRM Port Mode	Address and Data Port Mapping					
	Port A Address	Port B Address	Port A data input	Port B data input	Port A data output	Port B data output
512*16	ADDRA [12:4]	ADDRB [12:4]	{DIB[7:0],DIA[7:0]}	N/A	N/A	{DOB[7:0],DOA [7:0]}
512*18	ADDRA [12:4]	ADDRB [12:4]	{DIB[8:0],DIA 8:0]}	N/A	N/A	{DOB[8:0],DOA [8:0]}

Table 1-6 Data Address Mapping for Different Data Widths (x1, x2, x4, x8, x16 data widths)

Data Width	Lowest-bit port address (compared with the least-bit port address in the maximum data width mode)															
16	0															
8	1								0							
4	3				2				1				0			
2	7		6		5		4		3		2		1		0	
1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 1-7 Data Address Mapping for Different Data Widths (x9 and x18 data widths)

Data Width	Lowest-bit port address (compared with the least-bit port address in the maximum data width mode)	
18	0	
9	1	0

1.2.5 Usage Rules for Compa Family CPLDs DRM

In DPRAM and SDP RAM modes, there are two relatively independent ports, and performing a read and a write operation on the same address through both ports simultaneously will cause a collision. He conflicts between two ports simultaneously writing data to the same address and performing a read or a write on the same address are illegal operations in DRM, and the current operation cannot be completed normally, so users need to avoid them logically in actual applications.

1.2.6 DRM Simulation Model

The simulation model for the Compa Family CPLDs DRM is GTP_DRM9K_E1, and the simulation model for FIFO is GTP_FIFO9K, and their supported types are shown in Table 1-8:

Table 1-8 Compa Family CPLDs DRM Primitives

Simulation Model	Supported Mode
GTP_DRM9K_E1	Supports bit widths of x1, x2, x4, x8, x16 (and x9, x18)
GTP_FIFO9K	Supports bit widths of x1, x2, x4, x8, x16 (and x9, x18)

Note: All simulation models can be found in the software installation path, e.g., C:\Pango\PDS\arch\vendor\pango\verilog\simulation.

Chapter 2 DRM

2.1 Ports and Description

DRM data ports are shown in Figure 2-1, DRM configuration parameters are shown in Table 2-1, and DRM port names and descriptions are shown in Table 2-2.

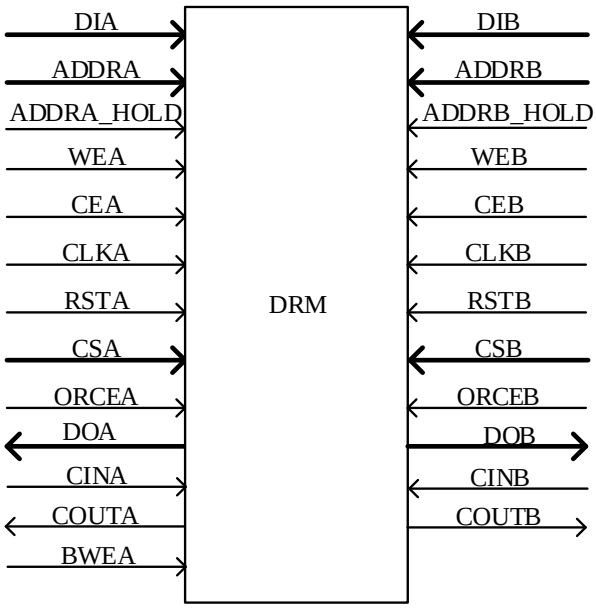


Figure 2-1 DRM Data Ports

Table 2-1 DRM Configuration Parameters

Parameter	Description	Setting Value
CSA_MASK[2:0]	Port A address extension control signal	0 ~ 7
CSB_MASK[2:0]	Port B address extension control signal	0 ~ 7
DATA_WIDTH_A	Data width of Port A	1, 2, 4, 8, 16, 9, 18
DATA_WIDTH_B	Data width of Port B	1, 2, 4, 8, 16, 9, 18
WRITE_MODE_A	Port A write mode	NORMAL_WRITE TRANSPARENT_WRITE READ_BEFORE_WRITE
WRITE_MODE_B	Port B write mode	NORMAL_WRITE TRANSPARENT_WRITE READ_BEFORE_WRITE
DOA_REG	Port A output register	0 = Do not enable output register 1 = Enable output register
DOB_REG	Port B output register	0 = Do not enable output register 1 = Enable output register
RST_TYPE	Reset mode selection	SYNC: Synchronous reset ASYNC: Asynchronous reset
RAM_MODE	RAM mode selection	TRUE_DUAL_PORT: Dual-port RAM SIMPLE_DUAL_PORT: Simple dual-port RAM

Parameter	Description	Setting Value
		SINGLE_PORT: Single-port RAM ROM: ROM
RAM_CASCADE	16Kx1 hard cascade mode	NONE: No hard cascade UPPER: Serves as a hard cascade data output module LOWER: Serves as a hard cascade additional module
GRS_EN	Global reset enable signal (Internal Chip)	FALSE: Global Reset not enabled TRUE: Global Reset enabled.
DOA_REG_CLKINV	Port A output register clock inversion	0 = Clock not inverted 1 = Clock inverted
DOB_REG_CLKINV	Port B output register clock inversion	0 = Clock not inverted 1 = Clock inverted
RSTA_VAL	Port A output reset/set	0 = Reset 1 = Set
RSTB_VAL	Port B output reset/set	0 = Reset 1 = Set
INIT_00 INIT_01 INIT_02 … INIT_1F	RAM Initialization Configuration Parameters	0 ~2^288-1
INIT_FILE	Initialization files	"NONE": No initialization file is specified, the default initialization data will be the value set by the parameter INIT_00~INIT_1F; "XXX": XXX represents the specific initialization file path
BLOCK_X	Data cascade coordinates when RAM is cascaded	Depends on the number of cascaded DRMs
BLOCK_Y	Address cascade coordinates when RAM is cascaded	Depends on the number of cascaded DRMs
RAM_DATA_WIDTH	Maximum data width after RAM is cascaded	Depends on the number of cascaded DRMs
RAM_ADDR_WIDTH	Maximum address width after RAM is cascaded	Depends on the number of cascaded DRMs
INIT_FORMAT	Initialization file format	"BIN": Binary "HEX": Hexadecimal

Table 2-2 DRM Port Naming and Description

Port Naming	Valid Bit Width	Active Level	Direction	Description
DIA	[8:0]		Input	Port A data input bus
ADDRA	[13:0]		Input	Port A address input bus
WEA	1	1 for write, 0 for read	Input	Port A write enable
CEA	1	Active-high	Input	Port A clock enable
CLKA	1		Input	Port A clock
RSTA	1	Active-high	Input	Port A output register reset
CSA	[2:0]		Input	Port A address extension
ORCEA	1	Active-high	Input	Port A output register enable
DOA	[8:0]		Output	Port A data output bus
CINA	1		Input	Port A cascade input

Port Naming	Valid Bit Width	Active Level	Direction	Description
COUTA	1		Output	Port A cascade output
BWEA	[1:0]		I	Port A bytes write enable
DIB	[8:0]		I	Port B data input bus
ADDRB	[13:0]		I	Port B address input bus
WEB	1	1 for write, 0 for read	I	Port B write enable
CEB	1	Active-high	I	Port B clock enable
CLKB	1		I	Port B clock
RSTB	1	Active-high	I	Port B output register reset
CSB	[2:0]		I	Port B address extension
ORCEB	1	Active-high	I	Port B output register enable
DOB	[8:0]		Output	Port B data output bus
CINB	1		I	Port B cascade input
COUTB	1		Output	Port B cascade output

In x9 and x18 data width modes, there is one additional information storage bit per byte, as shown in Table 2-3:

Table 2-3 List of Additional Information Bit for Bytes

Port Mode	Port A data input bus		Port B data input bus		Port A data output bus		Port B data output bus	
	Byte	Additional Information Bit	Byte	Additional Information Bit	Byte	Additional Information Bit	Byte	Additional Information Bit
1K*9	DIA[7:0]	DIA[8]	DIB[7:0]	DIB[8]	DOA[7:0]	DOA[8]	DOB[7:0]	DOB[8]
512*18	DIA[16:9]	DIA[17]	DIB[16:9]	DIB[17]	DOA[16:9]	DOA[17]	DOB[16:9]	DOB[17]
	DIA[7:0]	DIA[8]	DIB[7:0]	DIB[8]	DOA[7:0]	DOA[8]	DOB[7:0]	DOB[8]

2.2 Memory Model

2.2.1 DPRAM Mode

The DPRAM mode has two independent ports, A and B, besides the ports that share DRM content. Their structures are completely symmetrical, as shown in Figure 2-2. The port names and descriptions are shown in Table 2-4.

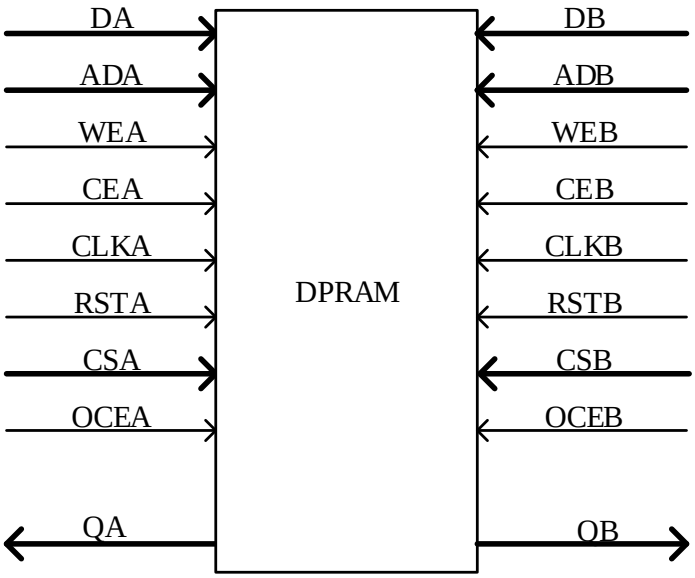


Figure 2-2 DP RAM Data Ports

Table 2-4 DP RAM Port Naming and Description

Port Naming	GTP Mapping Relationships	Valid Bit Width	Active Level	Direction	Description
DA	DIA	[8:0]		Input	Port A data input bus
ADA	ADDRA	[13:0]		Input	Port A address input bus
WEA	WEA	1	1 for write, 0 for read	Input	Port A write enable
CEA	CEA	1	Active-high	Input	Port A clock enable
CLKA	CLKA	1		Input	Port A clock
RSTA	RSTA	1	Active-high	Input	Port A output register reset
CSA	CSA	[2:0]		Input	Port A address extension
OCEA	ORCEA	1	Active-high	Input	Port A output register enable
QA	DOA	[8:0]		Output	Port A data output bus
DB	DIB	[8:0]		Input	Port B data input bus
ADB	ADDRB	[13:0]		Input	Port B address input bus
WEB	WEB	1	1 for write, 0 for read	Input	Port B write enable
CEB	CEB	1	Active-high	Input	Port B clock enable
CLKB	CLKB	1		Input	Port B clock
RSTB	RSTB	1	Active-high	Input	Port B output register reset
CSB	CSB	[2:0]		Input	Port B address extension
OCEB	ORCEB	1	Active-high	Input	Port B output register enable
QB	DOB	[8:0]		Output	Port B data output bus

2.2.2 SDPRAM Mode

Each DRM can also be configured as SDPRAM. In this mode, the DRM port data width is

increased to 18 bits, with port A dedicated to data writing and port B to data reading, and both reading and writing ports support different clocks. The supported combination modes for SDPRAM are shown in Table 1-6 and Table 1-7, the SDPRAM data port descriptions are shown in Figure 2-3, and port names and descriptions are shown in Table 2-5.

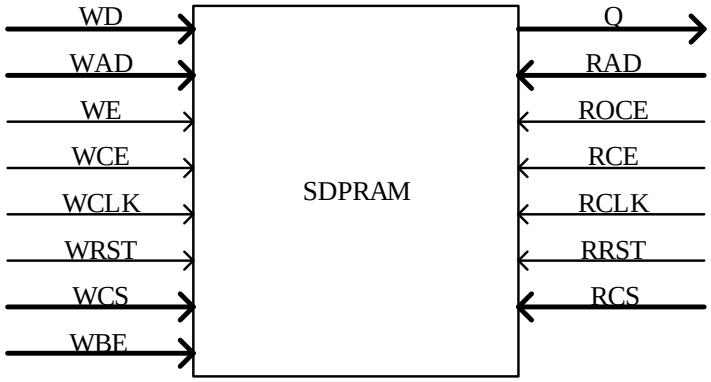


Figure 2-3 SDPRAM Data Ports

Table 2-5 SDPRAM Port Naming and Description

Port Naming	GTP Mapping Relationships	Valid Bit Width	Active Level	Direction	Description
WD	DIA	[8:0]		Input	Data input bus
WAD	ADDRA	[13:0]		Input	Write address input bus
WE	WEA	1	Active-high	Input	Write enable
WCE	CEA	1	Active-high	Input	Write clock enable
WCLK	CLKA	1		Input	Write clock
WRST	RSTA	1	Active-high	Input	Write register reset
WCS	CSA	[2:0]		Input	Write address extension
WBE	BWEA	[1:0]		Input	Write byte enable control
Q	DOB	[8:0]		Output	Data output bus
RAD	ADDRB	[13:0]		Input	Read address input bus
ROCE	ORCEB	1	Active-high	Input	Output register enable
RCE	CEB	1	Active-high	Input	Read clock enable
RCLK	CLKB	1		Input	Read clock
RRST	RSTB	1	Active-high	Input	Read register reset
RCS	CSB	[2:0]		Input	Read address extension

2.2.3 SPRAM Mode and ROM Mode

2.2.3.1 SPRAM Mode Data Ports

In SPRAM mode, DRM contains two ports, and SPRAM mode allows independent read and write operations on these two ports.

The data flow of SPRAM is explained in Figure 2-4, Table 2-6 and port names and port descriptions are listed in.

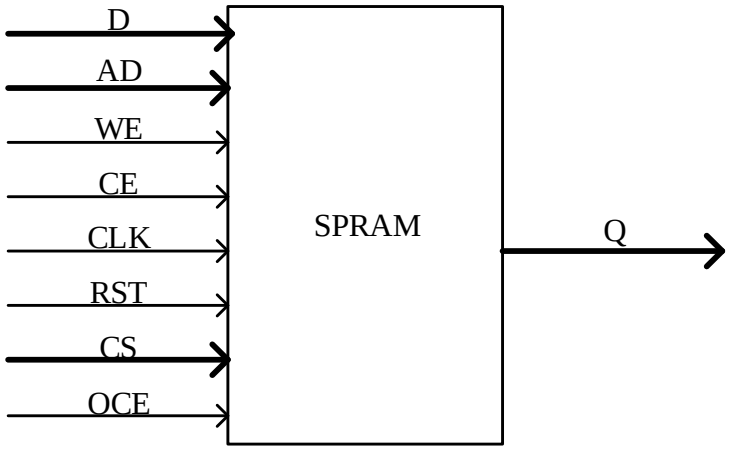


Figure 2-4 SPRAM Mode

Table 2-6 SPRAM Mode Port Naming and Description

Port Naming	GTP Mapping Relationships	Valid Bit Width	Active Level	Direction	Description
D	DIA	[8:0]		Input	Data input bus
AD	ADDRA	[13:0]		Input	Address input bus
WE	WEA	1	Active-high	Input	Write enable
CE	CEA	1	Active-high	Input	Write clock enable
CLK	CLKA	1		Input	Write clock
RST	RSTA	1	Active-high	Input	Write register reset
CS	CSA	[2:0]		Input	Address extension
OCE	ORCEA	1	Active-high	Input	Output register enable
Q	DOA	[8:0]		Output	Data output bus

2.2.3.2 ROM Mode Data Ports

The DRM can be configured as ROM, with ROM contents initialized through the configuration interface. ROM mode only has read ports.

The data flow of ROM is explained in Figure 2-5, and port names and port descriptions are listed in Table 2-7.

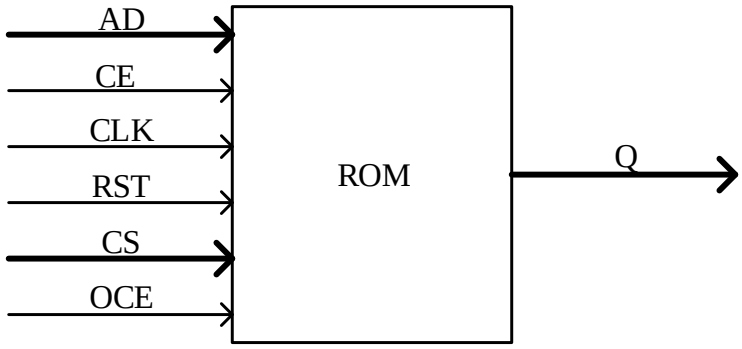


Figure 2-5 ROM Mode

Table 2-7 ROM Mode Port Naming and Description

Port Naming	GTP Mapping Relationships	Valid Bit Width	Active Level	Direction	Description
AD	ADDRA	[13:0]		Input	Read address input
CE	CEA	1	Active-high	Input	Read clock enable
CLK	CLKA	1		Input	Read clock
RST	RSTA	1	Active-high	Input	Read register reset
CS	CSA	[2:0]		Input	Address extension
OCE	ORCEA	1	Active-high	Input	Output register enable
Q	DOA	[8:0]		Output	Data output bus

2.2.3.3 Implementation Descriptions for TW and RBW in SPRAM (x16/x18) Mode

DRM cannot enable TW and RBW modes in 16/18 bits SPRAM mode through direct configuration; additional configurations are required, as detailed below:

1. Port A and Port B are both configured as 8/9 bits DPRAM mode (for 16/18 bits SPRAM, respectively);
2. Port A and Port B are configured to the same write mode; other configuration bits also need to be the same.
3. The CE, CS, WE, ADDR, ORCE, RST, CLK, and other control signals for Port A are paralleled with the corresponding signals for Port B, meaning they are connected to the same signals for both ports;
4. Splicing DIA and DIB as data inputs; splicing DOA and DOB as data outputs;

5. Both Port A and Port B address input ports must be connected to the address input simultaneously; ADDRA[3] and ADDRB[3] must be connected to 0 or 1 respectively (in opposite), as shown in Figure 2-6:

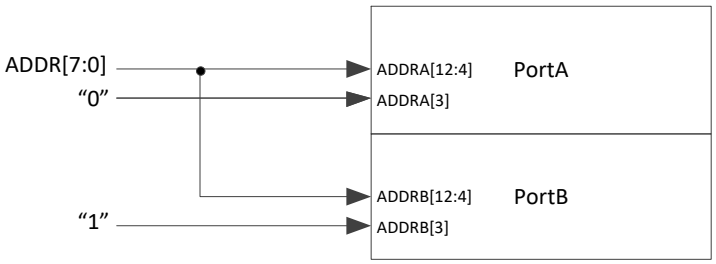


Figure 2-6 Address Line Configuration for TW and RBW Modes in SPRAM Mode

2.3 Write Operation Mode

Depending on the data output from the same port during data writing, the port write operations of DRM support three modes: NW, TW, and RBW. The timing diagram for the three write operation modes is shown in Figure 2-7.

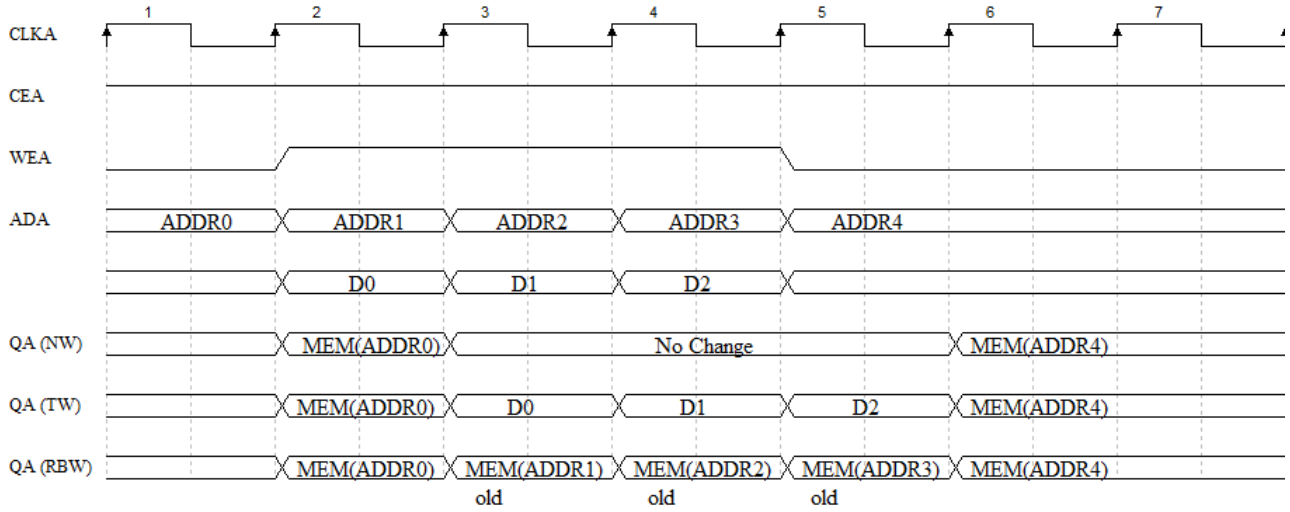


Figure 2-7 Output Timing Diagram for the Three Writing Operation Modes

Notes: The port write operating mode of DRM is only applicable to ports with read/write functions, i.e., the A/B ports of DP RAM and the ports of SP RAM.

2.3.1 NW Mode

The read-write timing diagram for the NW mode is shown in Figure 2-8; when a user writes data to a port of the DRM, the output data of that port is not updated at this time. The NW mode is the default mode.

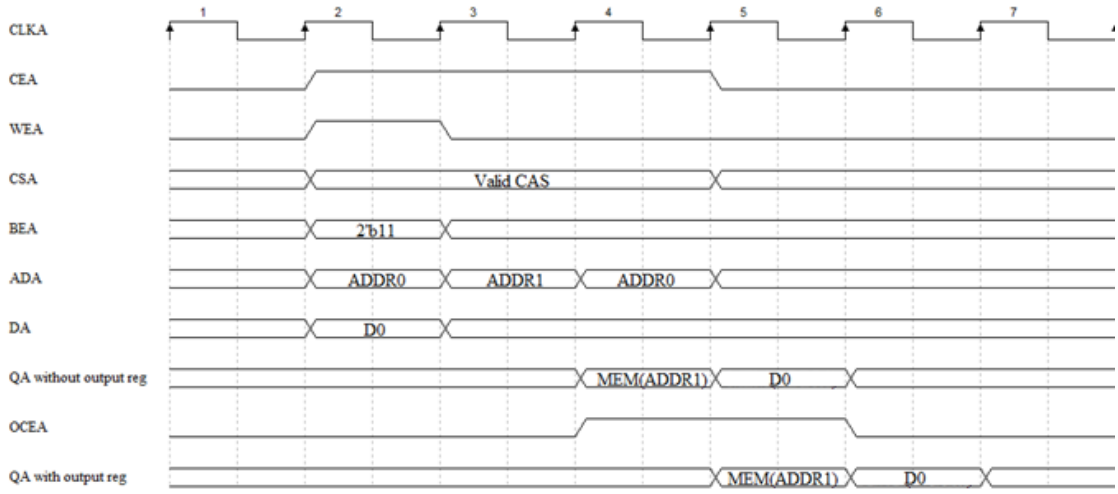


Figure 2-8 Read-Write Timing Diagram for NW Mode

2.3.2 TW Mode

The TW mode read-write timing diagram is shown in Figure 2-9, when a user writes data to a port of the DRM, the written data is directly output to the output port at the same time as it is written to the RAM (i.e., the next clock cycle of the write operation).

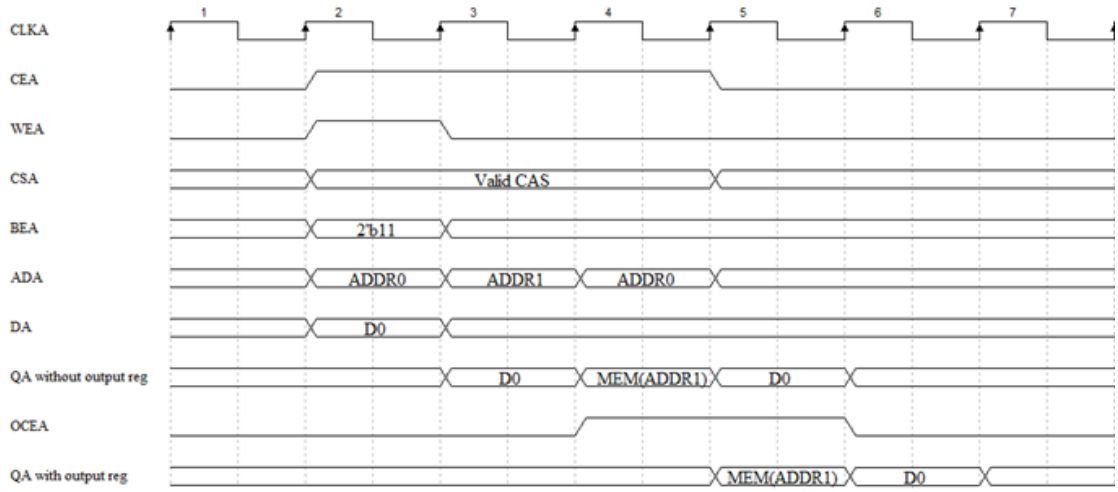


Figure 2-9 Read-Write Timing Diagram for TW Mode

2.3.3 RBW Mode

As the output timing diagram for the three write operation modes shown in Figure 2-7 or the

read-write timing diagram for the RBW mode shown in Figure 2-10, when a user writes data to a port of the DRM, the original data at that address is first read and then output to the output port in the next clock cycle of the write operation.

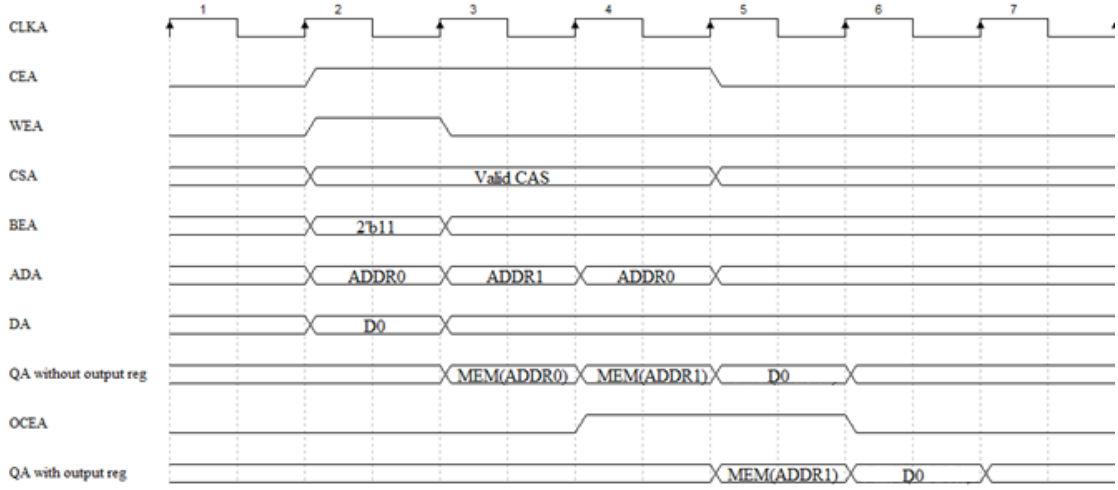


Figure 2-10 Read-Write Timing Diagram for RBW Mode

2.3.4 Byte Write Mode

DRM supports byte enable for write operations, which writes to selected data bytes through the BWEA signals (active-high) while masking the writing to other bytes at the same address index. When the port width is 2^N bits, only byte enable for 16-bit write operations is supported, with each byte containing 8 bits.When the port width is 9×2^N bits, only byte enable for 18-bit write operations is supported, with each byte containing 9 bits.

Table 2-8 lists the control of the written data bits by the byte enable signal.

Table 2-8 Byte Enable Signal Control

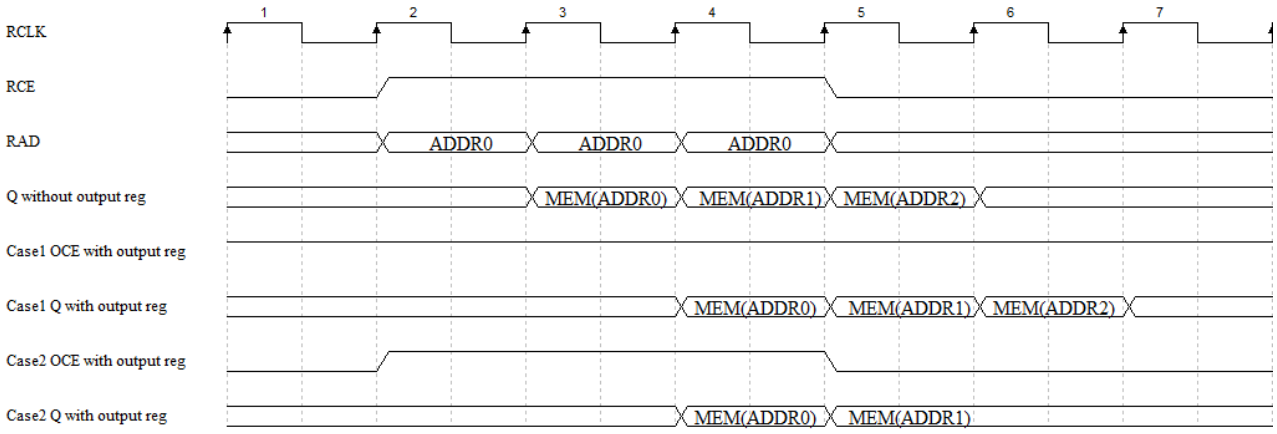
DRM Data Bus Width	Byte Width	Byte Enable Signal	Actual Data Bit Written
18 bits	18 bits	BWEA [1:0]=2'b11	DIA [17:0]
	9 bits	BWEA [1:0]=2'b01	DIA [8:0]
		BWEA [1:0]=2'b10	DIA [17:9]

Note: The BW write operation mode supports x18 (x16) data port width.

2.4 Output Register Mode

For data output ports, DRM provides an optional Output Register for improved timing performance. As shown in Figure 2-11, the output register can be controlled by an independent enable signal ORCE. When ORCE is a constant 1, the use of the output register will increase the delay of the read operation from one clock cycle to two clock cycles (Case 1); in pipeline designs with flow control,

the user can also flexibly control OCE with logic (Case 2).



Note: The timing diagram of the output register in SDPRAM mode provided in this figure is applicable to other modes

Figure 2-11 Read Timing Diagram with Output Register

2.5 Synchronous and Asynchronous Reset

The DOA/DOB output list when resetting/setting is shown in Table 2-9.

Table 2-9 DOA/B Output List when Resetting/Setting

DATA WIDTH	OR Bypass		OR Enable	
	DOA	DOB	DOA	DOB
x1	{8'b0,SC_SRVAL_A[0]}	{8'b0,SC_SRVAL_B[0]}	SC_SRVAL_A	SC_SRVAL_B
x2	{7'b0,SC_SRVAL_A[1:0]}	{7'b0,SC_SRVAL_B[1:0]}	SC_SRVAL_A	SC_SRVAL_B
x4	{5'b0,SC_SRVAL_A[3:0]}	{5'b0,SC_SRVAL_B[3:0]}	SC_SRVAL_A	SC_SRVAL_B
x8	SC_SRVAL_A	SC_SRVAL_B	SC_SRVAL_A	SC_SRVAL_B
x9	SC_SRVAL_A	SC_SRVAL_B	SC_SRVAL_A	SC_SRVAL_B
x16	N/A	{SC_SRVAL_B,SC_SRVAL_A}	N/A	{SC_SRVAL_B,SC_SRVAL_A}
x18	N/A	{SC_SRVAL_B,SC_SRVAL_A}	N/A	{SC_SRVAL_B,SC_SRVAL_A}

2.6 Mixed Bit Width Function

The port of DRM supports two types of data widths: one is 2^N (including 1/2/4/8/16 bit).The other is 9×2^N (including 9/18 bit).

DPRAM and SDPRAM modes support mixed width, meaning the two ports can be configured with different widths. For example, an SDPRAM can be configured to 8Kx1 at the write port and 512x16 at the read port, thereby saving the serial-to-parallel conversion logic from 1 bit to 16 bits. Please refer to Table 1-5, Table 1-6, and Table 1-7.

2.7 DRM Cascade Expansion Function

Multiple DRMs can be combined into larger DPRAMs, SDPRAMs, SPRAMs, or ROMs through cascade expansion. For this, DRM provides an additional 3-bit address extension (CS[2:0]), commonly used for deeply-extended applications.

In x1 width mode, two adjacent DRMs can be combined into a 16Kx1 via hard cascading, and support 16Kx1 single-port RAM, 16Kx1 dual-port RAM, 16Kx1 simple dual-port RAM, and 16Kx1 ROM.

Chapter 3 DRM FIFO Mode

3.1 DRM FIFO Mode Ports and Descriptions

The ports and descriptions for DRM FIFO mode are shown in Figure 3-1 and Table 3-3, the supported bit widths are shown in Table 3-1, and the parameter list is shown in Table 3-2.

Table 3-1 Asynchronous/Synchronous FIFO Mode Data Width List

		Write Port				
		16K*1	**8K*2**	**4K*4**	**2K*9(8)**	**1K*18(16)**
Read Port	16K*1	√				
	8K*2		√			
	4K*4			√		
	2K*9(8)				√	
	1K*18(16)					√

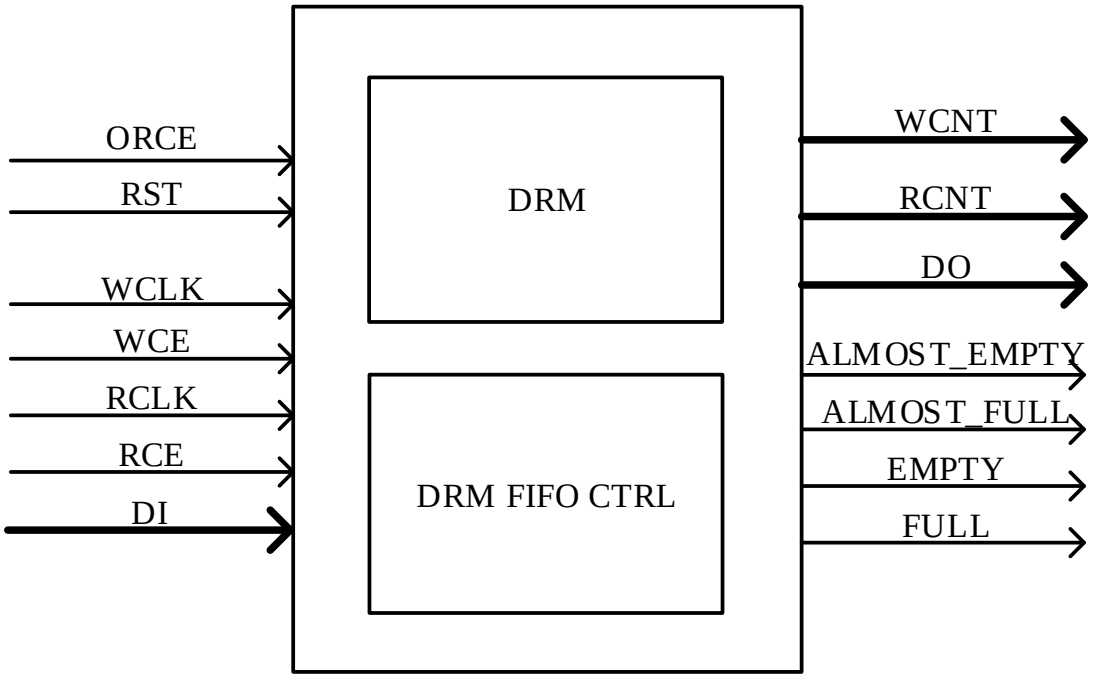


Figure 3-1 DRM FIFO Mode Ports

Table 3-2 DRM_FIFO Parameter List

Parameter	**Description**	**Setting Value**
GRS_EN	Global reset enable signal (Internal Chip)	TRUE: Enable global reset; FALSE: Do not enable global reset.
DATA_WIDTH	FIFO data width	1, 2, 4, 8, 9, 16, 18
ALMOST_FULL_OFFSET	When the FIFO is almost full and the difference between the write and read	DATA_WIDTH = 1: 1~8190 2: 1~4094

Parameter	Description	Setting Value
	pointers is greater than or equal to ALMOST_FULL_OFFSET, the ALMOST_FULL flag is set to 1.	4: 1~2046 8/9: 1~1022 16/18: 1~510
ALMOST_EMPTY_OFFSET	When the FIFO is almost empty and the difference between the read and write pointers is less than or equal to ALMOST_EMPTY_OFFSET, the ALMOST_EMPTY flag is set to 1.	DATA_WIDTH = 1: 1~8190 2: 1~4094 4: 1~2046 8/9: 1~1022 16/18: 1~510
SYNC_FIFO	Asynchronous/Synchronous FIFO Selection	TRUE: Use synchronous FIFO; FALSE: Use asynchronous FIFO.
USE_EMPTY	Enable read empty flag	1: Read empty flag enabled; 0: Read empty flag not enabled.
USE_FULL	Enable write full flag	1: Write full flag enabled; 0: Write full flag not enabled.
DO_REG	Output register enable	1: Enabled; 0: Not enabled.

Table 3-3 DRM FIFO Mode Port Description

Port Naming	Direction	Description
ORCE	Input	Output register enable
RST	Input	Reset
WCLK	Input	Write clock
WCE	Input	Write enable
RCLK	Input	Read clock
RCE	Input	Read enable
DI	Input	Data input bus
WCNT	Output	Write pointer
RCNT	Output	Read pointer
DO	Output	Data output bus
ALMOST_EMPTY	Output	Almost empty signal
ALMOST_FULL	Output	Almost full signal
EMPTY	Output	Empty signal
FULL	Output	Full signal

3.2 DRM_FIFO Read/Write Timing

3.2.1 Write Timing to Empty FIFO

The EMPTY signal indicates the FIFO is empty. When WCE is active and data is successfully written, in synchronous FIFO, the EMPTY signal is cleared after one RCLK clock cycle; in asynchronous FIFO, the EMPTY signal is cleared after one to two RCLK clock cycles. When WCE remains active, the ALMOST_EMPTY signal is cleared with a delay based on the configuration of ALMOST_EMPTY_OFFSET. The write timing to empty asynchronous FIFO is shown in Figure 3-2:

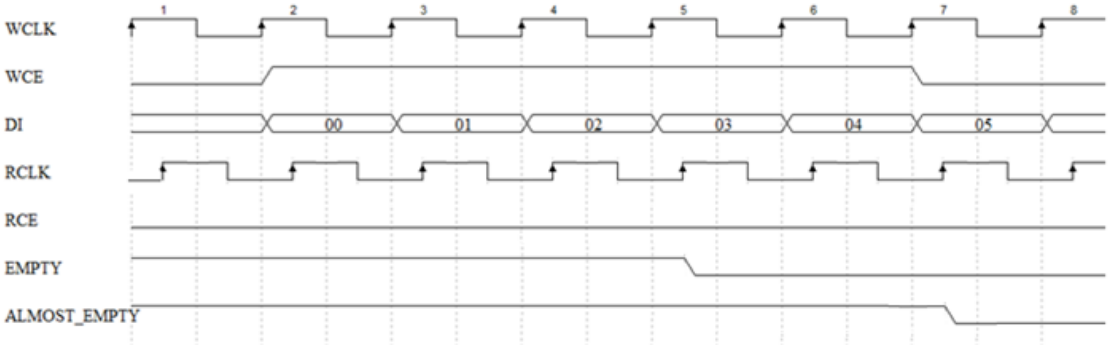


Figure 3-2 Writing Timing to Empty Asynchronous FIFO

3.2.2 Write Timing to Almost Full FIFO

When the FIFO is almost full, ALMOST_FULL is set in advance, according to the configuration of ALMOST_FULL_OFFSET. When the FULL signal of FIFO is set to 1, the write pointer will no longer be incremented. Write timing to almost full FIFO is shown in Figure 3-3:

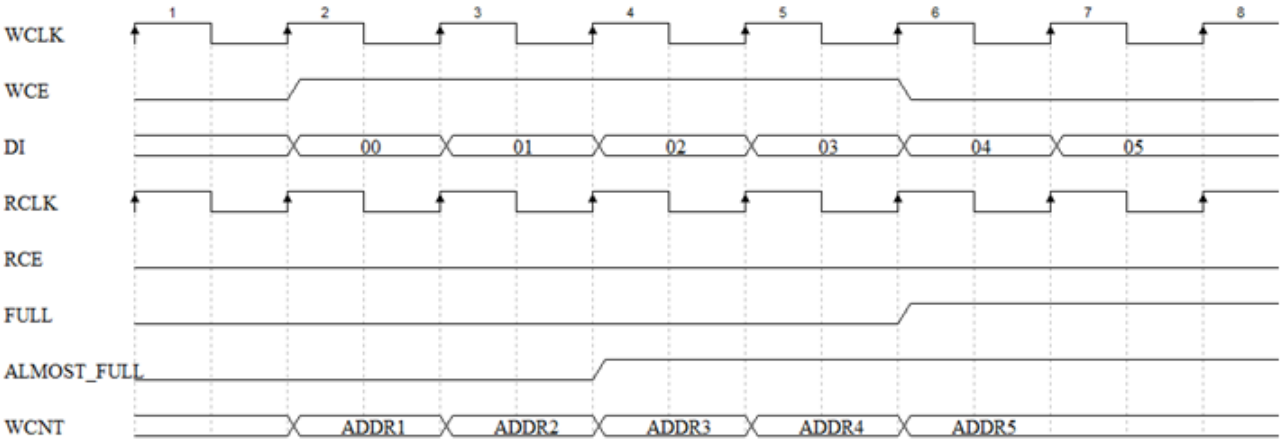


Figure 3-3 Write Timing to Almost Full FIFO

3.2.3 Read Timing from Full FIFO

The FULL signal indicates the FIFO is full. After data is read out when RCE is active, the FULL

signal is cleared within one to two WCLK clock cycles. When RCE remains active, the ALMOST_FULL signal is cleared with a delay based on the configuration of ALMOST_FULL_OFFSET. Read timing from full asynchronous FIFO is shown in Figure 3-4:

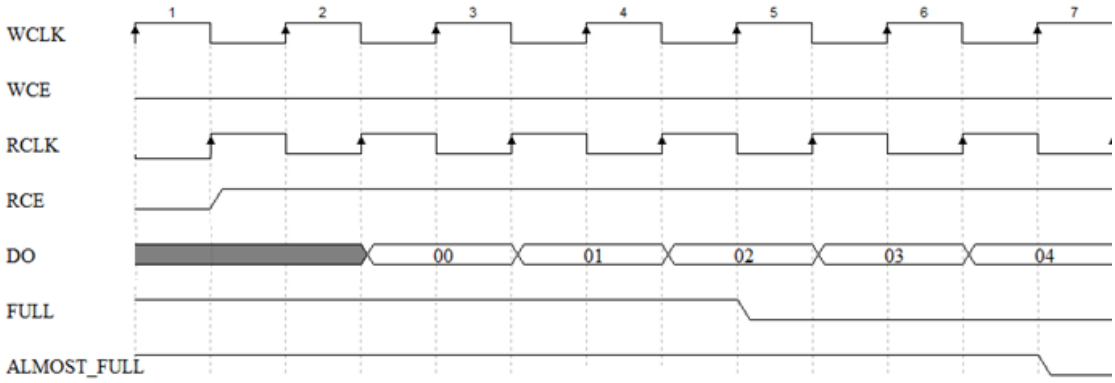


Figure 3-4 Read Timing from Full Asynchronous FIFO

3.2.4 Read Timing from Almost Empty FIFO

When the FIFO is almost empty, ALMOST_EMPTY is set in advance, based on the configuration of ALMOST_EMPTY_OFFSET. When the EMPTY signal of FIFO is set to 1, the read pointer will no longer be incremented. Read timing from almost empty FIFO is shown in Figure 3-5:

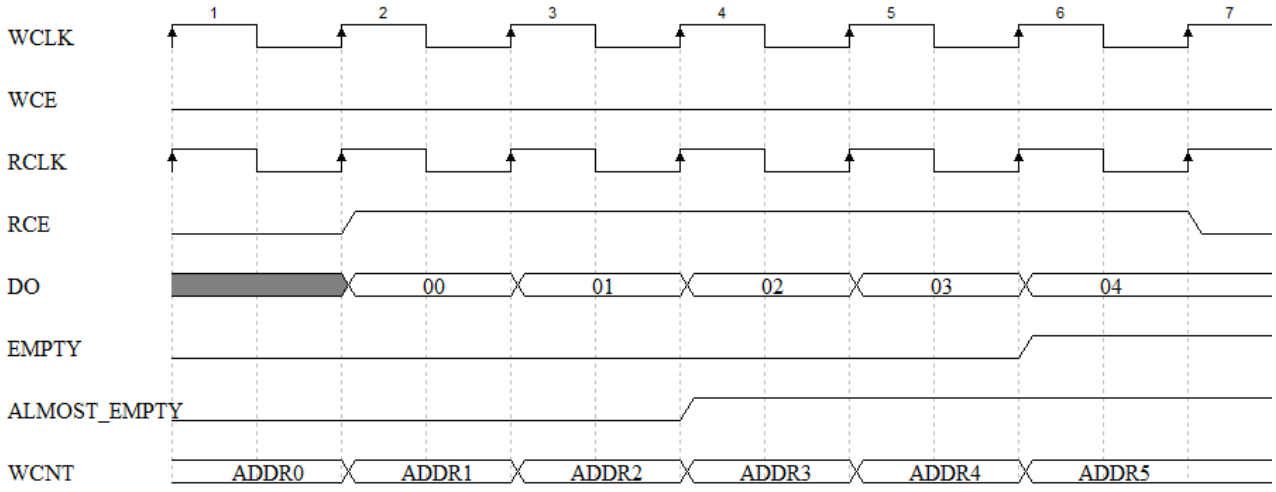


Figure 3-5 Read Timing from Almost Empty FIFO

3.3 DRM FIFO Cascade Expansion

3.3.1 Recommended Method for Depth Expansion

Depth expansion can be achieved by cascading N FIFOs: if the frequency of WCLK is higher than that of the RCLK, then INTCLK = WCLK; if the frequency of WCLK is less than or equal to that

of the RCLK, then INTCLK = RCLK. The ALMOST_EMPTY signal is generated by the last FIFO, and the ALMOST_FULL signal is generated by the first FIFO. See Figure 3-6 for the recommended method for depth expansions.

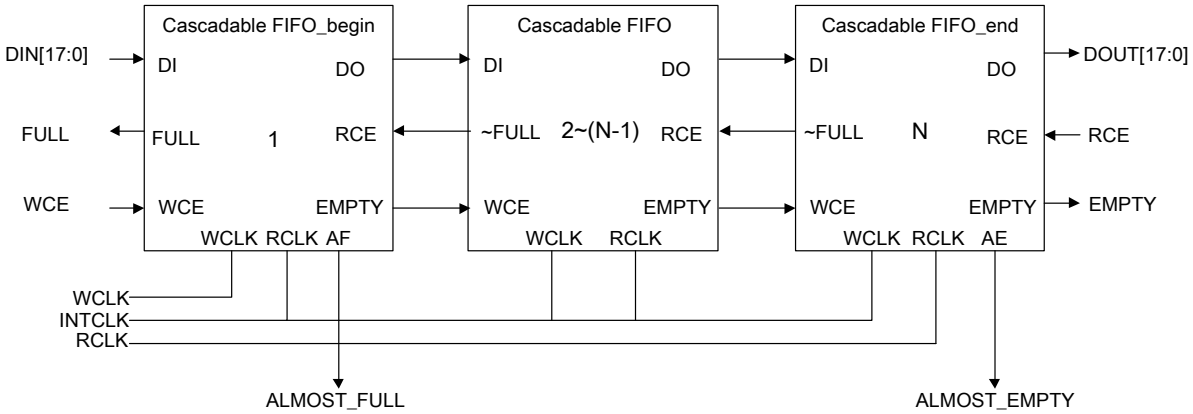


Figure 3-6 Recommended Method for Depth Expansion

Note: The "~FULL" in the diagram indicates the inverse of the FIFO FULL signal.

3.3.2 Recommended Method for Width Expansion

Width expansion can be achieved through parallel FIFOs, see Figure 3-7 for the recommended method for width expansion.

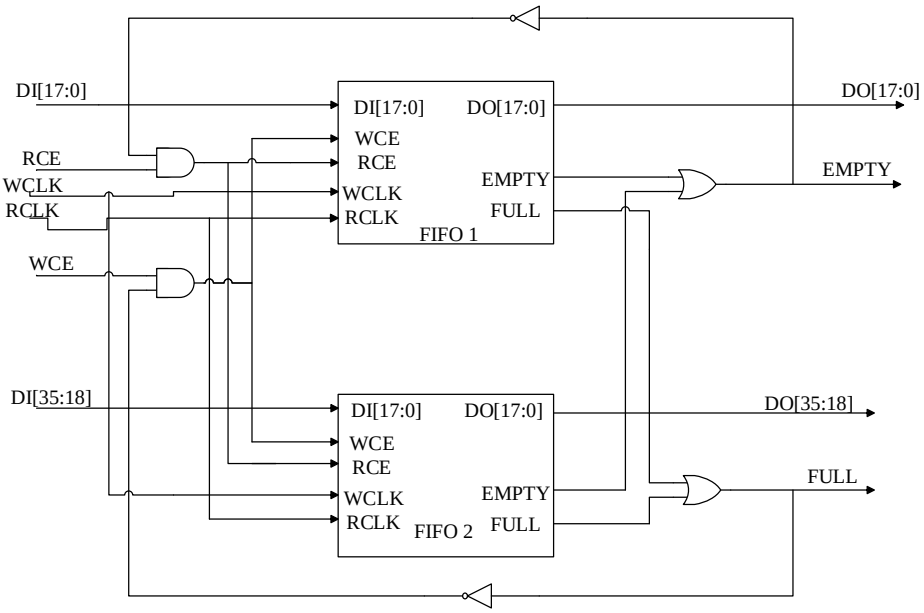


Figure 3-7 Recommended Method for Width Expansion

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