pgr_pg2l_iol_serdes Application Guide

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Shenzhen Pango Microsystems Co., Ltd.

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.1	25.02.2021	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
DDR	Double Data Rate

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Chapter 1 Overview

1.1 Introduction

This document is an application document for FPGA products IOL SERDES (Serialisation and Deserialisation) from Shenzhen Pango Microsystems Co., Ltd. This document mainly introduces the function list, design architecture, interface definition, interface timing, supported devices, and reference designs of IOL SERDES.

IOL SERDES implements IOL serialisation and deserialisation function and can serve as a basic module for applications including LVDS, MIPI, and TMDS.

1.2 Main Functions

The main functions supported include:

- SDR (Single data rate) transmission and reception support serialisation ratios of 3:1, 4:1, 5:1, 6:1, 7:1, and 8:1
- DDR (Double data rate) transmission and reception support serialisation ratios of 4:1, 6:1, 8: 1, 10:1, and 14:1.
- Each clock group supports up to 16 pairs of data.
- The input clocks and data channels support independent delay adjustment from 0 to 247 steps with a step value of 10ps.
- The output clocks and data channels support independent delay adjustment from 0 to 127 steps with a step value of 5ps.

1.3 Design Information

Table 1-1 IOL SERDES Design Information

IOL SERDES	
Supported Devices	Logos2 family FPGA products
Supported User Interface	Customize
Provided Design Files	
Design File	Verilog files
Reference Designs	Verilog files
Simulation File	Verilog files
Constraint File	fdc file
Development Tools	
Design Tools	PDS Development Suite Pango Design Suite 2022.2-sp6.8

1.4 Resource Usage

Table 1-2 Resource Usage Rate

Project Type	**Device**	**DRM**	**FF**	**LUT**	**PLL**
5 channels, DDR mode, serialisation ratio 8:1	PG2L100H	0	182	144	1
5 channels, SDR mode, serialisation ratio 7:1	PG2L100H	0	172	139	2

Chapter 2 Function Description

IOL SERDES includes 2 main modules for deserialisation and serialisation: the pgr_oser_phy_io_tx module implements the parallel-to-serial conversion of data, while the pgr_ides_phy_io_rx module implements the serial-to-parallel conversion of data. The typical applications are shown in Figure 1. LVDS data is sent to an LVDS display using the transmit module, and the signal from the LVDS camera is deserialized and received by the receive module for further processing by other modules.

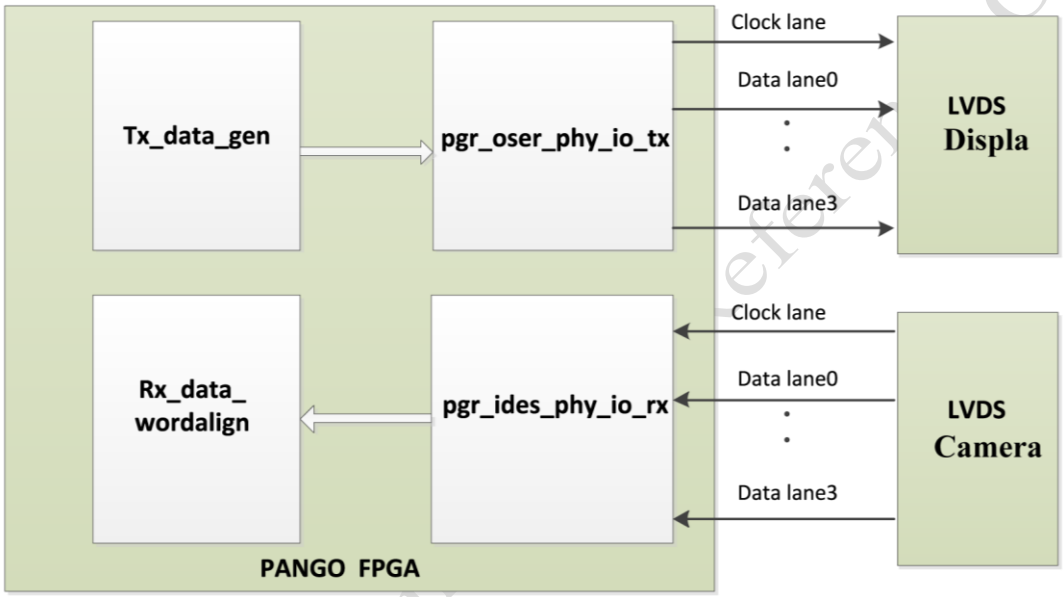

Figure 2-1 Typical Applications

2.1 lock Module Design

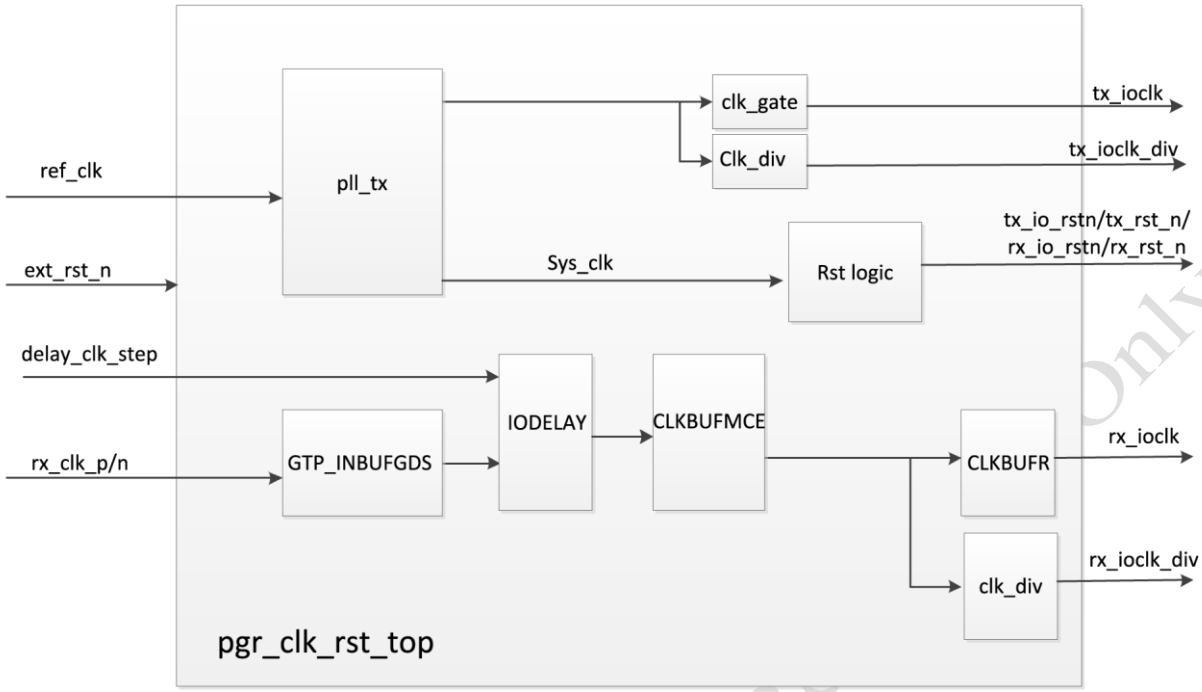

Figure 2-2 Dual-Edge Application Clock Architecture Block Diagram

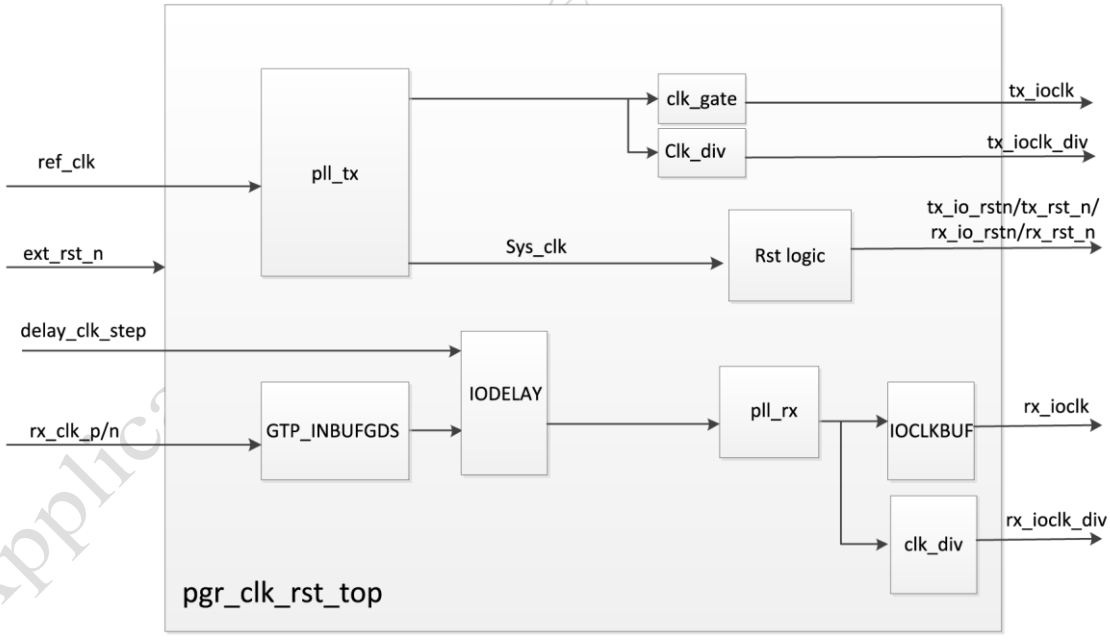

Figure 2-3 Single Data Rate Application Clock Architecture Block Diagram

The pgr_clk_rst_top module mainly provides system clocks and reset signals. For DDR MODE applications, source synchronous clock is used for sampling. For single data rate applications,

pll_rx generates the corresponding high-speed clock for sampling. The multiplier ratio equals the serialisation ratio.

Note: For double data rate applications, the differential clock should be connected to the clock pin of GMCLK. For both single data rate and double data rate applications, the transmitter needs to utilize the gate function of PLL output.

2.2 Transmit Module Design

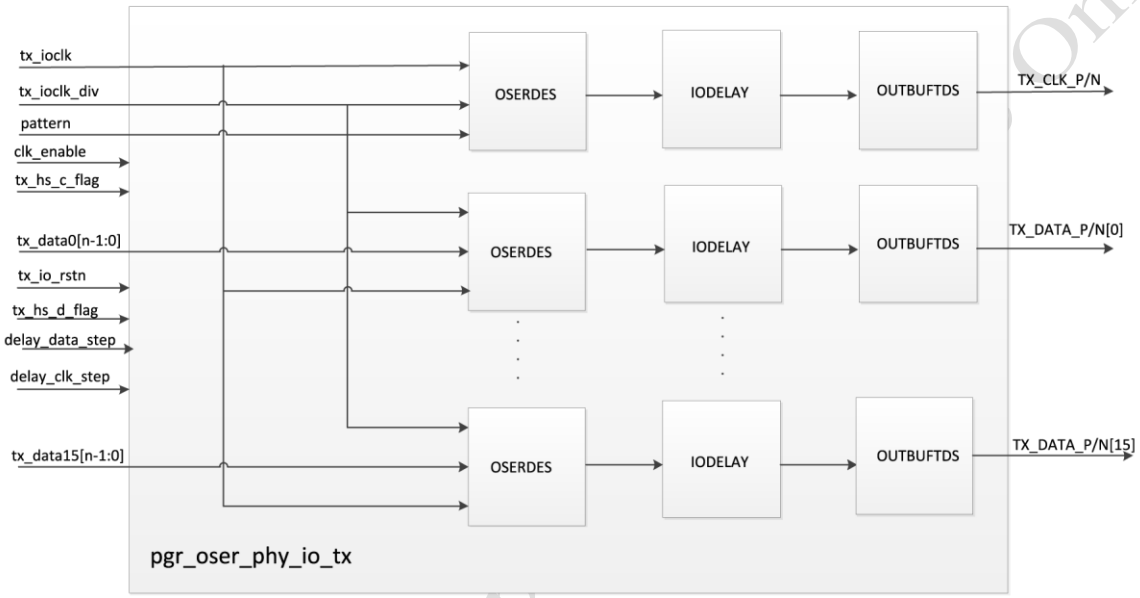

Figure 2-4 Transmission Function Block Diagram

The pgr_oser_phy_io_tx module implements parallel-to-serial conversion of data and supports independent delay adjustment for clock and data channels. Transmitted parallel data undergoes parallel-to-serial conversion through OSERDES and delay adjustment through IODELAY. OUTBUFTDS outputs the serial data in the differential form.

2.3 Receive Module Design

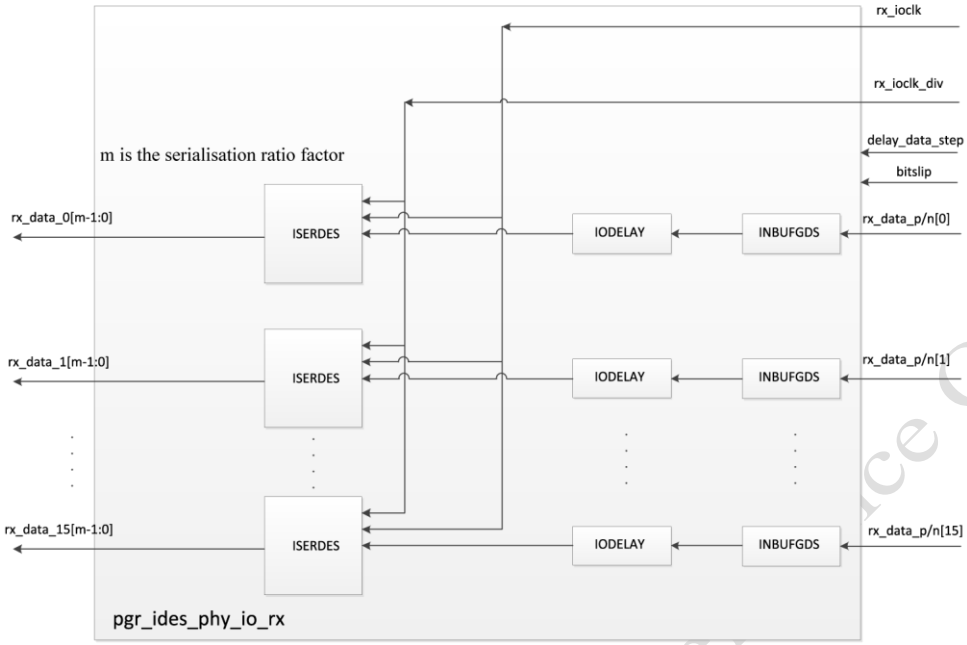

Figure 2-5 Reception Function Block Diagram

The pgr_ides_phy_io_rx module implements serial-to-parallel conversion of data. Differential data signals are converted to single-ended signals by the INBUFDS unit and passed through the IODELAY unit before entering the ISERDES for serial-to-parallel conversion. The IODELAY of each data channel can be adjusted independently.

2.4 List of Interfaces

Table 2-1 List of Clock Module Interfaces

Signal Name	Input / Output	Bit width	Description
Global signals			
ref_clk	Input	1	System clock signal, 50MHz
ext_rst_n	Input	1	System reset signal, active-low
rx_clk_p	Input	1	Differential clock input, p side
rx_clk_n	Input	1	Differential clock input, n side
delay_clk_step	Input	8	Input clock channel delay, 0~247 steps with a step value of 10 ps
tx_ioclk	Output	1	High-speed clock of output channel, used for driving OSERDES
tx_ioclk_div	Output	1	Division clock for the high-speed clock of output channel

Signal Name	Input / Output	Bit width	Description
tx_io_rstn	Output	1	IOL reset signal of output channel, active-low
tx_rstn	Output	1	Transmit module logic reset signal, active-low
rx_ioclk	Output	1	High-speed clock for input channel, used for driving ISERDES
rx_ioclk_div	Output	1	Division clock for the high-speed clock of input channel
rx_io_rstn	Output	1	IOL reset signal of input channel, active-low
rx_rstn	Output	1	Receive module logic reset signal, active-low

Table 2-2 List of Transmit Module Interfaces

Signal Name	Input / Output	Bit width	Description
Global signals			
tx_ioclk	Input	1	High-speed clock of output channel, used for driving OSERDES
tx_ioclk_div	Input	1	Division clock for the high-speed clock of output channel
clk_enable	Input	1	Clock channel data enable signal, active-high
tx_io_rstn	Input	1	IOL reset signal of output channel, active-low
tx_hs c flag	Input	1	Output clock channel high-speed mode enable, 1: high speed enable, 0: high impedance
tx_hs d flag	Input	1	Output data channel high-speed mode enable, 1: high speed enable, 0: high impedance
delay_data_step	Input	8*CHANNEL	Output channel data delay, independently adjustable for each channel, each channel uses 8 bits. Each channel has a value of 0~127, each step delay is 5ps, and the IODELAY device intrinsic delay is about 0.6ns
delay_clk_step	Input	8	Output clock channel delay value, the value is 0~127, and each step delay is 5ps, and the IODELAY device intrinsic delay is about 0.6ns
tx_data	Input	CHANNEL*DATA_WIDTH	Transmit parallel high-speed data
tx_data_p	Output	CHANNEL	High-speed data port of output channel, p side
tx_data_n	Output	CHANNEL	High-speed data port of output channel,n side
tx_clk_p	Output	1	High-speed clock port of output channel,p side
tx_clk_n	Output	1	High-speed clock port of output channel,n side

Table 2-3 Receive Module Interface List

Signal Name	Input / Output	Bit width	Description
Global signals			
rx_io_rstn	Input	1	IOL reset signal of input channel, active-low
rx_ioclk	Input	1	High-speed clock of input channel
rx_ioclk_div	Input	1	Division clock for the high-speed clock of input channel
delay_data_step	Input	8* CHANNEL	Input channel data delay, independently adjustable for each channel, each channel uses 8 bits.Each channel has a value of 0–247, each step delay is 10ps, and the IODELAY module device intrinsic delay is about 0.6ns
bitslip	Input	CHANNEL	Used for shifting bits of iserdes to achieve byte alignment. Each bitslip rising edge generates one shift. A high level greater than one rx_ioclk_div clock cycle must be maintained. There should be more than two rx_ioclk_div clock cycles between two valid bitslip operations.
rx_data_p	Input	CHANNEL	Input channel high-speed data port, p side
rx_data_n	Input	CHANNEL	Input channel high-speed data port, n side
rx_data	Output	CHANNEL*DATA_WIDTH	Deserialized parallel data

2.5 Parameter Definitions

Table 2-4 Definitions of Top-level Parameters

Parameter	Description
SIM_ON	Simulation enable: "TRUE" enables simulation, "FALSE" disables simulation; Default value = "FALSE"
CHANNEL	Number of channels, with an optional range of 1–16 Default value = 5;
DATA_WIDTH	Data width, which needs to match the actual serialization ratio Default value = 8;
DIV_FACTOR	Clock division factor, which supports "1", "2", "3", "4", "5", "6", "7", "8", and "BYPASS" Needs to match the serialization ratio Default value= "4"
OSERDES_MODE	OSERDES mode selection for the transmit module, optional "SDR3TO1", "SDR4TO1", "SDR5TO1", "SDR6TO1", "SDR7TO1", "SDR8TO1", "DDR4TO1","DDR8TO1","DDR10TO1","DDR14TO1" Default value = "DDR8TO1"
ISERDES_MODE	ISERDES Mode signal, optional "SDR1TO3","SDR1TO4","SDR1TO5","SDR1TO6","SDR1TO7","SDR1TO8","DDR1TO4","DDR1 TO6","DDR1TO8","DDR1TO10","DDR1TO14" Default value = "DDR1TO8"

2.6 Interface Timing

The reset timing of the receive module: First release rx_io_rstn (ISERDES reset), then release rx_gate_rstn (high-speed clock and division clock reset) to ensure all ISERDES work simultaneously. Finally, release rx_rstn (logic reset). The reset timing for the transmit module is similar.

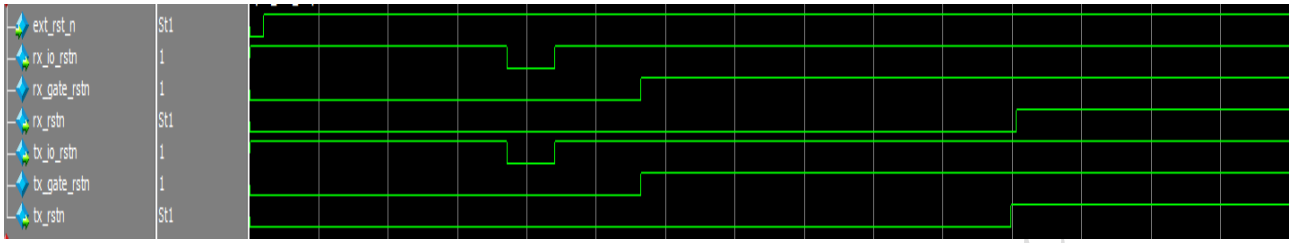

Figure 2-6 Typical Reset Timing

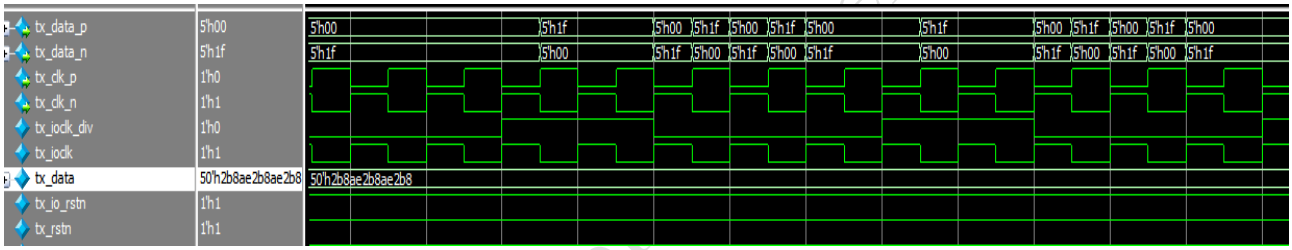

Figure 2-7 Typical Transmission Timing

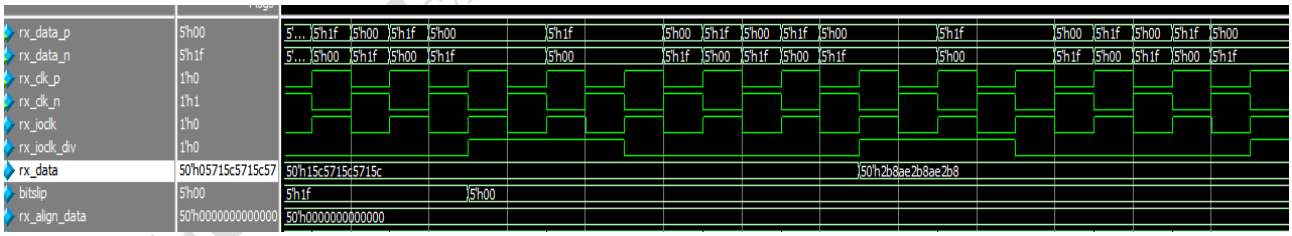

Figure 2-8 Typical Receive Timing

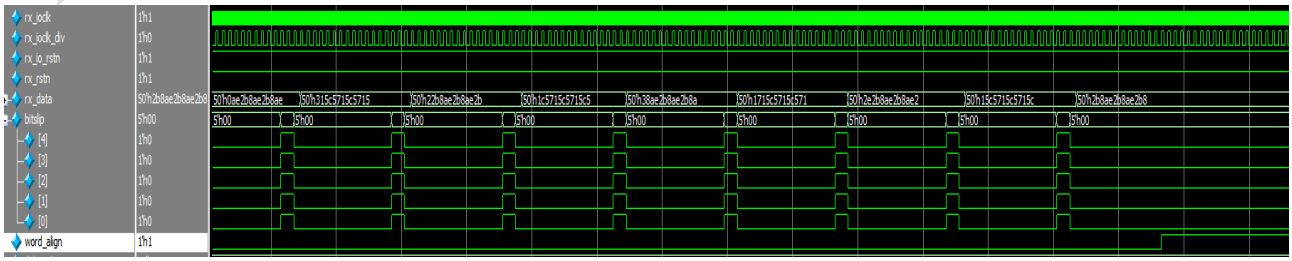

Figure 2-9 Typical Bitslip Timing

Chapter 3 Reference Design

3.1 Reference Function Design

To simplify the verification environment for the reference design, PG2L100H is used simultaneously as both the transmitter and receiver, which are connected with an SMA cable. The design function block diagram is shown in Figure 3-1.

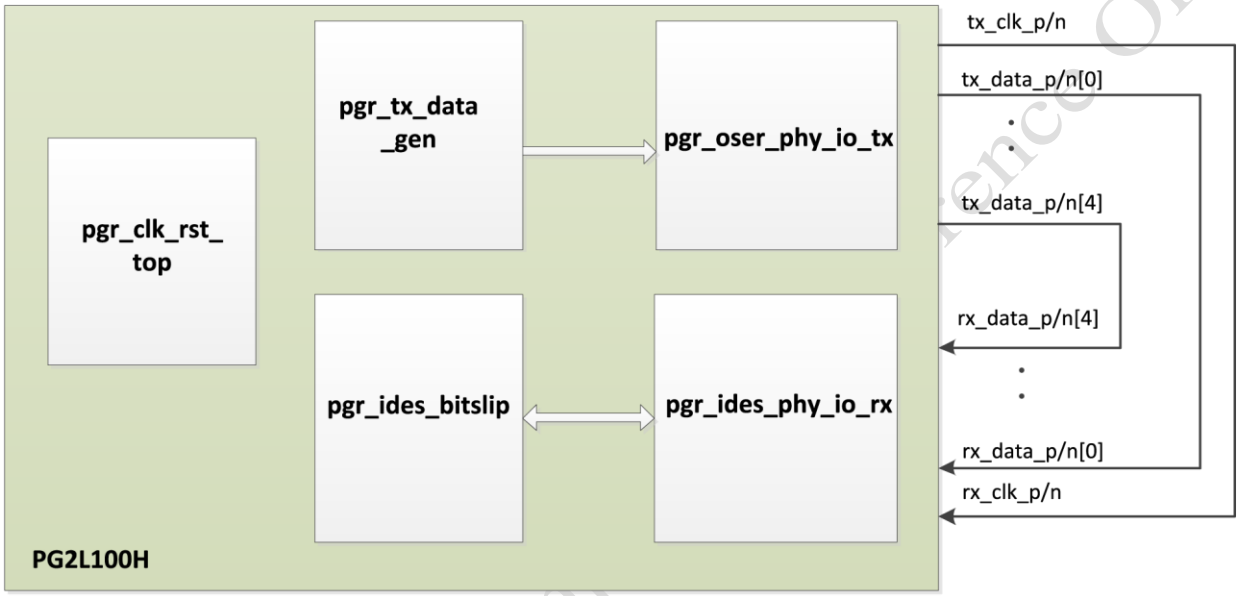

Figure 3-1 Reference Design Function Block Diagram

pgr_clk_rst_top module: generates the clock and reset signals required by the system.

pgr_tx_data_gen module, generates parallel high-speed transmission data

pgr_oser_phy_io_tx module, implements parallel-to-serial data conversion

pgr_ides_phy_io_rx module, implements serial-to-parallel data conversion

pgr_ides_bitslip module, implements byte alignment of received data

3.2 Reference Design Interface List

Table 3-1 Reference Design Interface List

Signal Name	Input / Output	Bit width	Description
Global signals			
ref_clk	I	1	System clock signal, 50MHz
ext_rst_n	I	1	System reset signal, active-low
dly_key_n	I	1	Debug button, reserved
test	O	1	Reserved
train_done_led	O	1	Test signal: A low level indicates alignment of received bytes, D6 light on
High-speed serial interfaces			
tx_data_p	O	5	Transmitter high-speed data port, p side;
tx_data_n	O	5	Transmitter high-speed data port, n side;
tx_clk_p	O	1	Transmitter high-speed clock port, p side;
tx_clk_n	O	1	Transmitter high-speed clock port, n side;
rx_data_p	I	5	Receiver high-speed data port, p side;
rx_data_n	I	5	Receiver high-speed data port, n side;
rx_clk_p	I	1	Receiver high-speed clock port, p side;
rx_clk_n	I	1	Receiver high-speed clock port, n side;

3.3 Reference Design File Directory

```
pgr_iol_serdes_top
|
├─bench                  // Example simulation test bench
├─docs                   //Design document
├─ip                     // Relevant IP called by the design
├─pnr                    // Example project directory
|  ├─ipcore              // IP CORE files generated by PDS
|  |  └─pll_tx           // PLL IP CORE used in the example
|  |  └─pll_rx           // PLL IP CORE used in the example
|  ├─PG2L100KF01_A1.fdc  // Example project constraint reference files
|  ├─top_inserter.fic    // Debug Core debugging files
|  └─project.pds         //PDS project file
├─simulation             // Simulation project directory
|  ├─file_list.f         // Design file list
|  ├─sim.bat             // Simulation scripts
|  ├─sim.tcl             // Simulation TCL scripts
|  └─wave.do             // Simulation waveform scripts
├─src                    // RTL files included in the design example
```

Figure 3-2 File Directory

3.4 Reference Design Simulation

Run the sim.bat script in the reference design file directory, or run the sim.tcl script in the simulation software to start the simulation. The simulation waveform is shown in Figure 3-3.

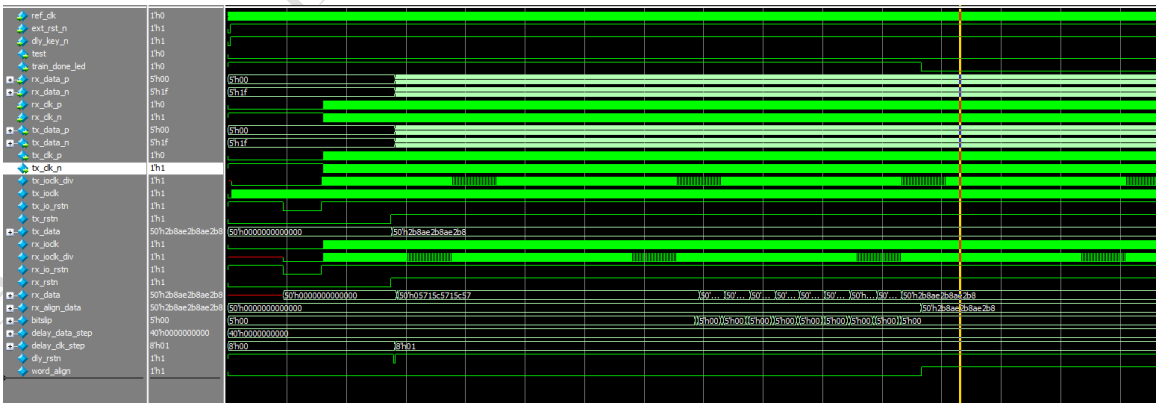

Figure 3-3 Simulation Waveform

3.5 Reference Design On-board Verification

The on-board verification environment is shown in Figure 3-4. The PG4I100KF01_A2 and FMC_LVDS_TEST_A0 boards are used, with 12 pairs of SMA cables connected, and the J35 jumper cap selects 2.5V.

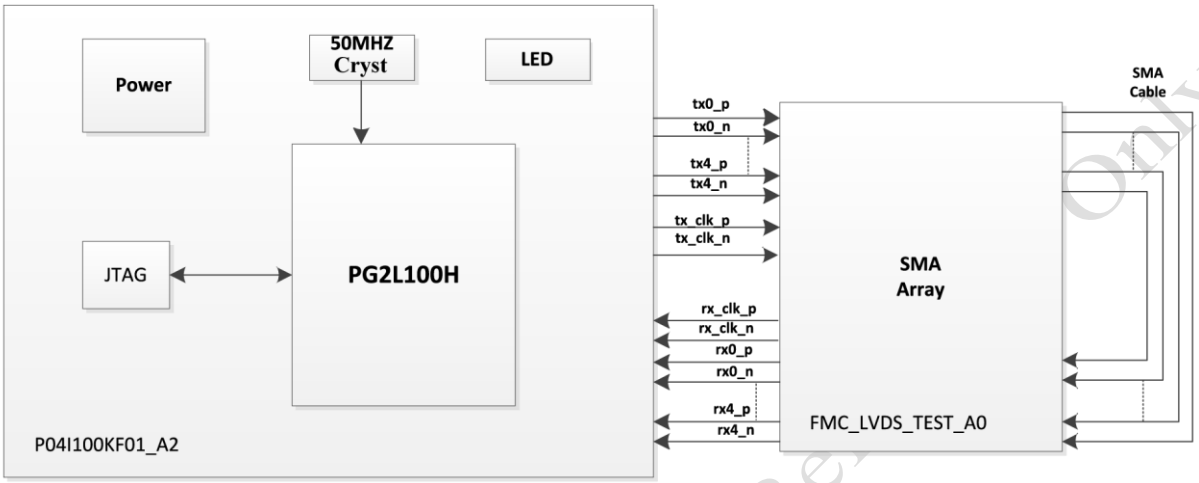

Figure 3-4 Reference Design On-board Environment

Connect the 12V DC power supply, program the bitstream, and use the debugcore tool to capture waveforms. As shown in Figure 3-5, this is an 8:1 serialization and deserialization, with word_align being high indicating successful verification.

Other serialization ratio verifications can be tested by modifying the top-level parameters. For example, 7:1 applications require modifying DATA_WIDTH to "7", DIV_FACTOR to"7", OSERDES_MODE to "SDR7TO1", ISERDES_MODE to "SDR1TO7", change pll_rx output frequency to 7 times the input frequency.

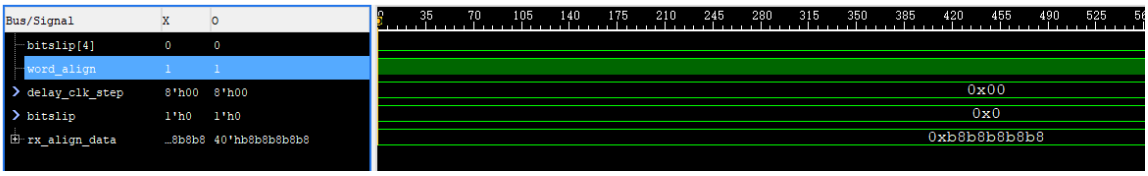

Figure 3-5 On-board Verification Waveform

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