PK03003_PGC2KL_UWG49

(V1.8)

(25.12.2020)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.8	25.12.2020	Initial release

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
POD	Package Outline Drawing
WLCSP	Wafer Level Chip Scale Packaging

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Chapter 1 Introduction to Packaging

The PGC2KL-UWG49 device is packaged with WLCSP wafer-level chip. Its package size is 3.189x3.052mm, with 49 solder balls, a pitch of 0.4mm between the balls and a maximum package thickness of 0.595mm.

Chapter 2 Package Dimension and Pins

2.1 Package Outline Dimension

Table 2-1 Dimensional Data

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
D	3.032	3.052	3.072	A	0.485	0.540	0.595
D1	-	2.4	-	A1	0.157	0.175	0.193
E	3.169	3.189	3.209	A2	0.340	0.365	0.390
E1	-	2.4	-	e	-	0.4	-
b	0.207	0.230	0.253				

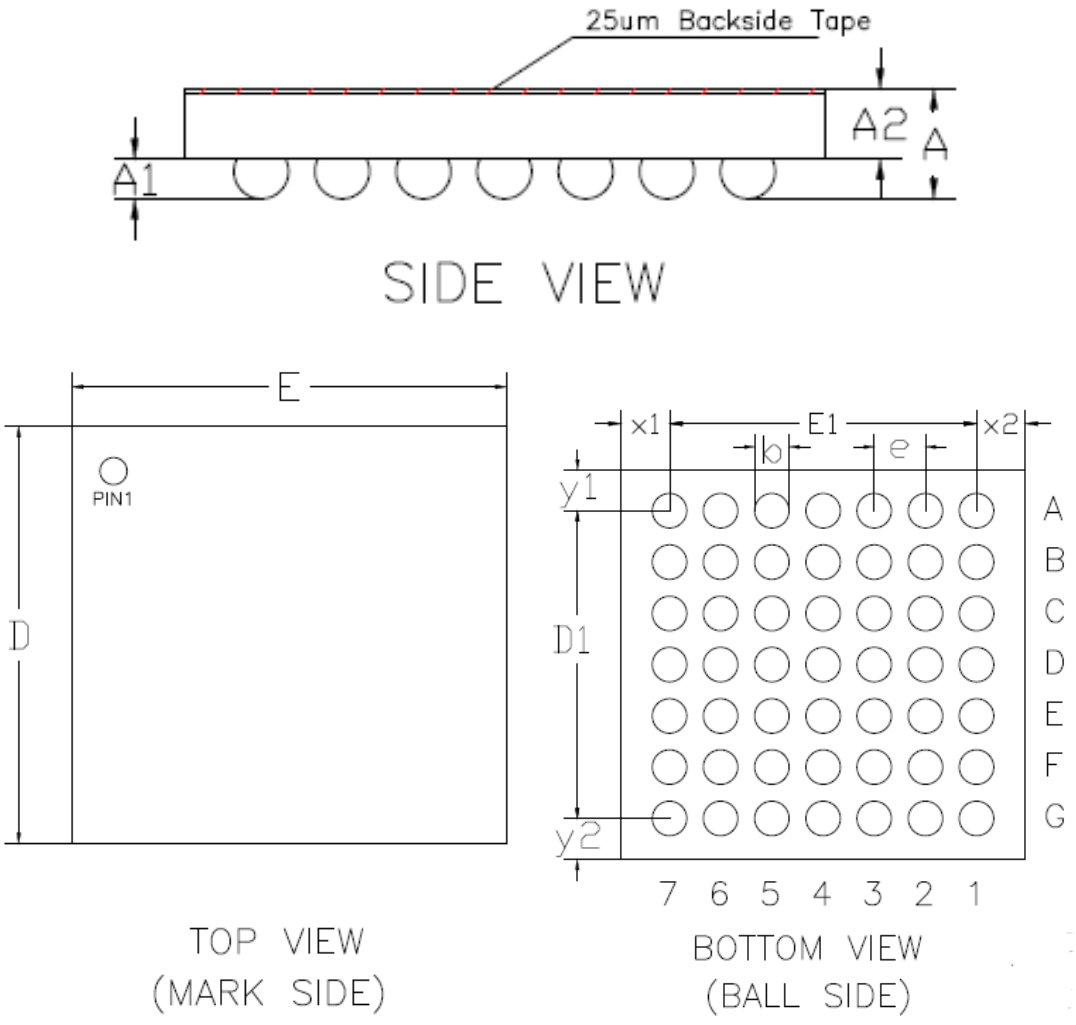

Figure 2-1 Package Outline Dimension (POD)

2.2 Pin Description

The PGC2KL-UWG49 device has 39 user I/Os.

Table 2-2 Product Pin Definitions

Pin Name	Pin Type	Direction	Pin Description
User I/O Pin			
DIFF[I,IO]_XX_NN[P,N]	User pin	Input/Output	User I/O. (1) DIFFI indicates support for differential signal input and pseudo-differential output; DIFFIO indicates support for differential signal input and true differential output, which can be used for transmitting and receiving LVDS signals; (2) "XX" denotes the Bank number, with possible values being B0, B1, B2, B3, B4, and B5; (3) "NN" denotes the sequence number of the programmable I/O group within the Bank, starting from 0 and increasing incrementally; (4) [P,N]: "P" denotes the positive side of the differential pair, and "N" denotes the negative side; During power-up, the user I/O is at a low voltage; After power-up is complete but before configuration, the general user I/O is at pull-down status; During configuration, the user I/O is at pull-down status;
Configuration[1]			
INIT_FLAG_N	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, with an internal weak pull-up resistor. When used as a configuration pin: During power-up, it is at a low voltage; After power-up is complete before configuration, it is open-drain at weak pull-up status; During configuration, it is open-drain at weak pull-up status; During initialization, the pin can be driven to a low voltage by an external input to indicate an error or to delay configuration. During configuration, the pin serves as an indicator output for configuration errors, where a low voltage indicates an error has occurred;
CFG_DONE	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, with an internal weak pull-up resistor. When it is used as configuration pin, it serves as an indicator output for configuration completion, where a high voltage indicates configuration is complete; Before or during configuration, the pin is driven to a low voltage; after configuration is complete, the pin can continue to be driven to a low voltage by an external source. If the internal start-up timing detects CFG_DONE at a low voltage, the internal start-up circuitry maintains its state until CFG_DONE goes high to continue the start-up process;
RSTN	Multi-function pin	Input	Configurable multiplexed reset pin, with an internal weak pull-up resistor. When it is used as a reset pin, it serves to restart the configuration process, active low. At this situation, it must be pulled up with an external resistor (internal weak pull-up resistor typically has a value of over 20kOhms, with a relatively weak pull-up strength); when the pin is at a low voltage, the CPLD enters reset state, with all I/Os in a weak pull-down status;

Pin Name	Pin Type	Direction	Pin Description
CFG_CLK	Multi-function pin	Input/Output	Configurable multiplexed clock pin, with an internal weak pull-up resistor. When it is used as a configuration pin: In slave SPI configuration mode, the pin serves as a clock input to acquire configuration data from an external source; In master SPI configuration mode, the pin serves as a clock output to acquire configuration data from an external source; in this mode, a 1kOhms pull-up resistor is needed; Master SPI mode and slave SPI mode are allowed to be enabled simultaneously, but using them at the same time is not permitted;
TCK	Multi-function pin	Input	Multiplexed JTAG test clock input pin; requires an external 4.7kOhms pull-down resistor;
TMS	Multi-function pin	Input	Multiplexed JTAG test mode select input pin; with an internal weak pull-up resistor, pulled up to VCCIO0;
TDI	Multi-function pin	Input	Multiplexed JTAG test data input pin; with an internal weak pull-up resistor, pulled up to VCCIO0;
TDO	Multi-function pin	Output	Multiplexed JTAG test data output pin; with an internal weak pull-up resistor, pulled up to VCCIO0.
JTAGEN	Multi-function pin	Input	Optional JTAG port behaviour control pin, usually used in user mode, when JTAG pins are configured as configuration I/Os, this pin is user I/O, with the state controlled by the user; when JTAG pins serve as user I/Os, JTAGEN serves as a dedicated input used to control the availability of JTAG pins; the default state is weak pull-down; when JTAGEN is configured as a dedicated I/O: (1) When at a low voltage, the JTAG pins function as user I/Os; (2) When at a high voltage, the JTAG pins function as JTAG configuration port.
FCS_N	Multi-function pin	Output	Configurable multiplexed pin, used for master SPI configuration mode, (1) In master SPI mode, outputs an active-low chip select signal to an external Flash; (2) After configuration is completed, it can be used as a user I/O.
MISO_SO	Multi-function pin	Input/Output	Configurable multiplexed pin; (1) MISO, serial data input in master SPI mode; (2) SO, serial data output in slave SPI mode; Master and slave SPI modes are allowed to be enabled simultaneously, but using them at the same time is not permitted.
MOSI_SI	Multi-function pin	Input/Output	Configurable multiplexed pin; (1) MOSI, serial data output in master SPI mode; (2) SI, serial data input in slave SPI mode; Master and slave SPI modes are allowed to be enabled simultaneously, but using them at the same time is not permitted.
FCSI_N	Multi-function pin	Input	Configurable multiplexed pin, with an internal weak

Pin Name	Pin Type	Direction	Pin Description
			pull-up resistor; In slave SPI mode, active-low chip select input.
SCL	Multi-function pin	Input (Open-drain)	Configurable multiplexed pin, clock input in slave I2C mode; requires an external weak pull-up resistor.
SDA	Multi-function pin	Bi-Directional (Open-drain)	Configurable multiplexed pin, data input/output in I2C mode; requires an external weak pull-up resistor.
SPAL_CLK	Multi-function pin	Input	Clock input in slave parallel X16 configuration mode.
SPAL_CS_N	Multi-function pin	Input	Chip select input in slave parallel X16 configuration mode. Active-low
SPAL_RDWR_N	Multi-function pin	Input	Read/write control input in slave parallel X16 configuration mode; 1: read; 0: write.
SPAL_BUSY	Multi-function pin	Output	Busy indicator in slave parallel X16 configuration mode; During readback, if the data is not ready, SPAL_BUSY changes to high voltage.
SPAL_D15~SPAL_D0	Multi-function pin	Input/Output	Data bus in slave parallel X16 configuration mode.
Clock, PLL			
CLK[0,1,2][P,N]_[B0,B1,…,B5]	Multi-function pin	Input	Global clock input pin; can also be used as user I/O; (1) [0,1,2]: clock pin numbers; (2) [P,N]: positive and negative sides of the differential clock pins; (3) [B0,B1,…,B5]: bank numbers.
PLL[0,1]_CLKIN_[P,N]	Multi-function pin	Input	PLL input. PLL can choose to directly input a clock from these pins; they can also be used as user I/Os; (1) [0,1]: corresponds to PLL0 and PLL1; (2) [P,N]: positive and negative sides of the differential clock pins.
PLL[0,1]_CLKFB_[P,N]	Multi-function pin	Input	Optional PLL feedback clock input. PLL can select to feedback clock externally from these pins; they can also be used as user I/Os; (1) [0,1]: corresponds to PLL0 and PLL1; (2) [P,N]: positive and negative sides of the differential clock pins.
Power			
VCC		Power	External power supply of 1.2V, providing power to the core logic.
VCCIO[0,2,5]		Power	I/O Bank power.
VSS		Ground	Ground associated with VCC;
MIPI_CTRL	Dedicated		MIPI high-performance application control pin; when connected to 2.5V or 3.3V, the device supports high-performance MIPI transmission functions; when connected to VSS or left floating, the device does not support the high-performance MIPI transmission capabilities.

Note:

1. When the configured multiplexed pin is used as a user I/O, its status is the same as the user I/O pin.

2.2.1 Pinout Diagram

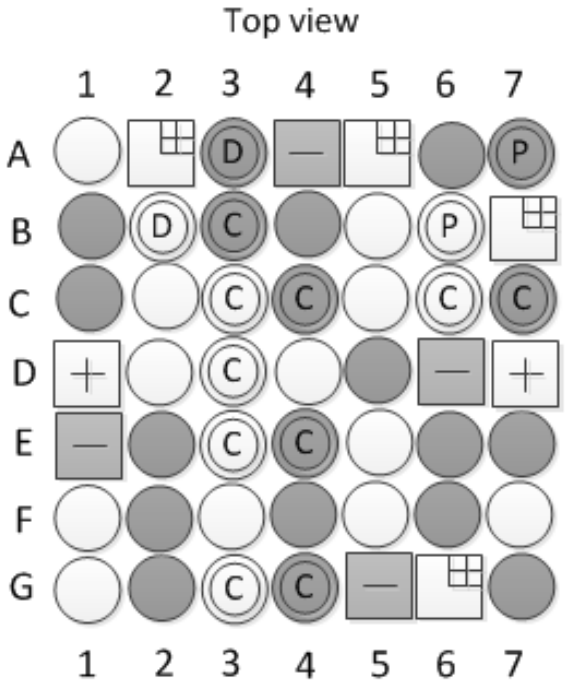

Figure 2-2 Pinout Diagram

Note: the Pinout symbols have the following meanings:

General IO	DIFFIO*	COMP(N) TRUE(P)
Multiplex IO	DIFFIO*/D0~D31 DIFFIO*/CLK* DIFFIO*/PLL*	D D C C P P
Power , Ground	VSS VCC VCCIO	

2.2.2 IO Banks

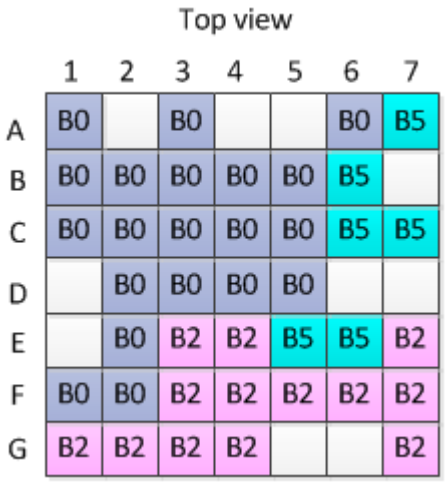

Figure 2-3 IO Banks

2.2.3 Power and GND Placement

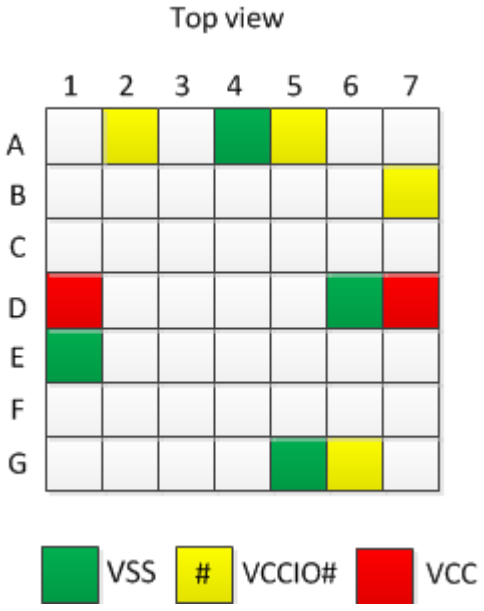

Figure 2-4 Power and GND Placement

2.2.4 Pin Name List

Table 2-3 Pin Name List

Bank Name	Pin Name	Pin Number	Differential Pair
B0	DIFFI_B0_0N/CFG_DONE	A1	IO_1_N
B0	DIFFI_B0_0P/INIT_FLAG_N	B1	IO_1_P

Bank Name	Pin Name	Pin Number	Differential Pair
B0	DIFFIO_B0_1N/SPAL_CLK	D2	IO_2_N
B0	DIFFIO_B0_1P/SPAL_CS_N	C1	IO_2_P
B0	DIFFIO_B0_3N/SPAL_RDWR_N	C2	IO_4_N
B0	DIFFIO_B0_3P/SPAL_BUSY	E2	IO_4_P
B0	DIFFI_B0_8N/RSTN	F1	IO_9_N
B0	DIFFI_B0_8P/JTAGEN	F2	IO_9_P
B0	DIFFIO_B0_9N/SPAL_D7	B2	IO_10_N
B0	DIFFIO_B0_9P/SPAL_D6	A3	IO_10_P
B0	DIFFI_B0_12N/SDA/CLK0N_B0	C3	IO_13_N
B0	DIFFI_B0_12P/SCL/CLK0P_B0	B3	IO_13_P
B0	DIFFIO_B0_15N/CLK1N_B0	D3	IO_16_N
B0	DIFFIO_B0_15P/CLK1P_B0	C4	IO_16_P
B0	DIFFI_B0_16N/TMS	B5	IO_17_N
B0	DIFFI_B0_16P/TCK	B4	IO_17_P
B0	DIFFI_B0_20N/TDI	C5	IO_21_N
B0	DIFFI_B0_20P/TDO	A6	IO_21_P
B0	DIFFIO_B0_25N	D4	IO_26_N
B0	DIFFIO_B0_25P	D5	IO_26_P
B2	DIFFI_B2_1N/MOSI_SI	G1	IO_56_N
B2	DIFFI_B2_1P/FCSI_N	G2	IO_56_P
B2	DIFFI_B2_13N/CLK1N_B2	G3	IO_68_N
B2	DIFFI_B2_13P/CLK1P_B2	G4	IO_68_P
B2	DIFFI_B2_15N	F3	IO_70_N
B2	DIFFI_B2_15P	F4	IO_70_P
B2	DIFFI_B2_17N/CLK0N_B2	E3	IO_72_N
B2	DIFFI_B2_17P/CLK0P_B2	E4	IO_72_P
B2	DIFFI_B2_21N/MISO_SO	F5	IO_76_N
B2	DIFFI_B2_21P/CFG_CLK	F6	IO_76_P
B2	DIFFI_B2_25P/FCS_N	G7	IO_80_P
B2	DIFFI_B2_27N	F7	IO_82_N
B2	DIFFI_B2_27P	E7	IO_82_P
B5	DIFFI_B5_2P/PLL0_CLKIN_P	A7	IO_101_P
B5	DIFFI_B5_2N/PLL0_CLKIN_N	B6	IO_101_N
B5	DIFFI_B5_4P/CLK0P_B5	C7	IO_103_P
B5	DIFFI_B5_4N/CLK0N_B5	C6	IO_103_N
B5	DIFFI_B5_8P	E6	IO_107_P
B5	DIFFI_B5_8N	E5	IO_107_N
	VCC	D1	
	VCC	D7	

Bank Name	Pin Name	Pin Number	Differential Pair
	MIPI_CTRL	A4	
	VCCIO0	A2	
	VCCIO0	A5	
	VCCIO2	G6	
	VCCIO5	B7	
	VSS	D6	
	VSS	E1	
	VSS	G5	

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