PCI Express IP

User Guide

(UG042004, V1.6)

(10.01.2023)

Revisions History

Document Revisions

Version	Date of Release	Revisions	Applicable IP and Corresponding Versions
V1.6	10.01.2023	Initial release.	V1.6

IP Revisions

IP Version	Date of Release	Revisions
V1.6	10.01.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
EP	Endpoint
RC	Root Complex
IPC	IP Compiler
PDS	Pango Design Suite

Related Documentation

The following documentation is related to this manual:

1. ***Pango_Design_Suite_Quick_Start_Tutorial***
2. ***Pango_Design_Suite_User_Guide***
3. ***IP_Compiler_User_Guide***
4. ***Simulation_User_Guide***
5. ***User_Constraint_Editor_User_Guide***
6. ***Physical_Constraint_Editor_User_Guide***
7. ***Route_Constraint_Editor_User_Guide***
8. ***PCI Express®Base Specification Revision 2.1***
9. ***PCI Local Bus Specification Revision 3.0***
10. ***AMBA® 4 AXI4-Stream Protocol Version: 1.0***
11. ***AMBA® APB Protocol Version: 2.0***
12. ***PHY Interface for the PCI ExpressTM Architecture Version 2.00***

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Chapter 1 Preface

This chapter describes the scope, structure, and writing standards of this manual to help users quickly find the information they need.

1.1 Introduction of the Manual

This manual serves as a user guide for the PCI Express IP, which is launched by Pango Microsystems. It is applicable to Logos2 Family FPGA products, mainly including the IP usage guidelines and relevant information. Through this manual, users can quickly understand the features and usage methods related to PCI Express IP.

1.2 Writing Standards of the Manual

Table 1-1 Description of Writing Standards

Text	**Rules**
Attention	If users ignore the attention contents, they may suffer adverse consequences or fail to operate successfully due to incorrect actions.
Description	Instructions and tips provided for users.

Chapter 2 IP User Guide

This chapter provides a guide on the use of PCI Express IP, including an introduction to IP, IP block diagram, IP generation process, Example Design, IP interface description, IP register description, and instructions and considerations. More details on the design process can be found in the following PDS help documentation.

- "***Pango_Design_Suite_Quick_Start_Tutorial***"
- "***Pango_Design_Suite_User_Guide***"
- "***IP_Compiler_User_Guide***"
- "***Simulation_User_Guide***"

2.1 IP Introduction

PCI Express IP is designed to implement the PCIe protocol in the Logos2 family FPGA product. Users can configure and generate the IP module using the IPC (IP Compiler) tool within the PDS (Pango Design Suite).

2.1.1 Key Features

The PCI Express IP of the Logos2 family is implemented in accordance with the "***PCI Express® Base Specification Revision 2.1***" and the "***PHY Interface for the PCI ExpressTM Architecture Version 2.00***" (with the data path expanded to 32 bits) protocols. The main features are provided in Table 2-1.

Table 2-1 Main Features of PCIe IP

Features	**Feature Description**
Supports configuration of Device Type	PCI Express Endpoint
	Legacy PCI Express Endpoint
	Root Port of PCI Express Root Complex
Supports configuration of Max Link Width	x1
	x2
	x4
Supports configuration of Max Link Speed	2.5GT/s
	5GT/s

Features	Feature Description
Supports 100MHz Reference Clk	-
Supports upconfigure Capability	-
Supports selection of the number of AXI-Stream Slaves	1
	2
	3
Supports Debug interface	-
Supports dynamic configuration of PCIe Configuration Space via Apb	-
Supports Receive Queue Management	
Supports Lane Reversal	-
Supports Force No Scrambling	-
Supports configuration of ID.	Supports configuration of Vendor ID
	Supports configuration of Device ID
	Supports configuration of Revision ID
	PCI Express Endpoint and Legacy PCI Express Endpoint support configuration of Subsystem Vendor ID
	PCI Express Endpoint and Legacy PCI Express Endpoint support configuration of Subsystem ID
	Configuration of Classcode
Configuration of BAR	PCI Express Endpoint and Legacy PCI Express Endpoint support configuration of 6 BARs
	Root Port of PCI Express Root Complex only supports configuration of BAR0 and BAR1
	PCI Express Endpoint supports configuration as Memory BAR
	Legacy PCI Express Endpoint and Root Port of PCI Express Root Complex support configuration as Memory and IO BAR
	Supports 32bit BAR
	32bit BAR supports configuration sizes from 256Bytes to 2GB
	BAR0, BAR2, and BAR4 support 64bit BAR
	64bit BAR supports being Prefetchable
	64bit BAR supports configuration sizes from 256Bytes to 8EB
	Supports Expansion ROM BAR
	Expansion ROM BAR supports configuration sizes from 2KB to 16MB
Supports configuration of Max Payload Size	128 Byte
	256 Byte
	512 Byte
	1024 Byte
Supports configuration of the Extended Tag Field and Extended Tag Default	-
Supports Atomic transactions	-
RC supports setting the Read Completion Boundary	-
Supports configuration of Target Link Speed	-

Features	Feature Description
RC supports setting CRS Software Visibility	-
Supports setting of ECRC Generation Capable	-
ECRC Check Capable is enabled by default	-
Supports INIT interrupt	PCI Express Endpoint and Legacy PCI Express Endpoint only support INTA
	Root Port of PCI Express Root Complex supports INTA, INTB, INTC, and INTD
Supports MSI interrupt	Supports 64-bit Address MSI interrupt
	Supports Multiple Message Capable: 1, 2, 4, 8, 16, or 32 Vectors
	Supports Per Vector Masking Capable
Supports MSIx interrupt	Supports configuration of Table Size, Offset, and BIR
	Supports configuration of PBA Offset and BIR

Note: "-" indicates that there is no description for the item.

2.1.2 Applicable Devices

Table 2-2 Applicable Devices for PCI Express IP

Applicable Devices	Supported Packages
PG2L200H	ALL
PG2L100H	ALL (except for MBG324)
PG2L100HX	ALL (except for MBG324)
PG2L50H	ALL (Except for FBG256/MBG324)
PG2L25H	ALL

2.2 IP Block Diagram

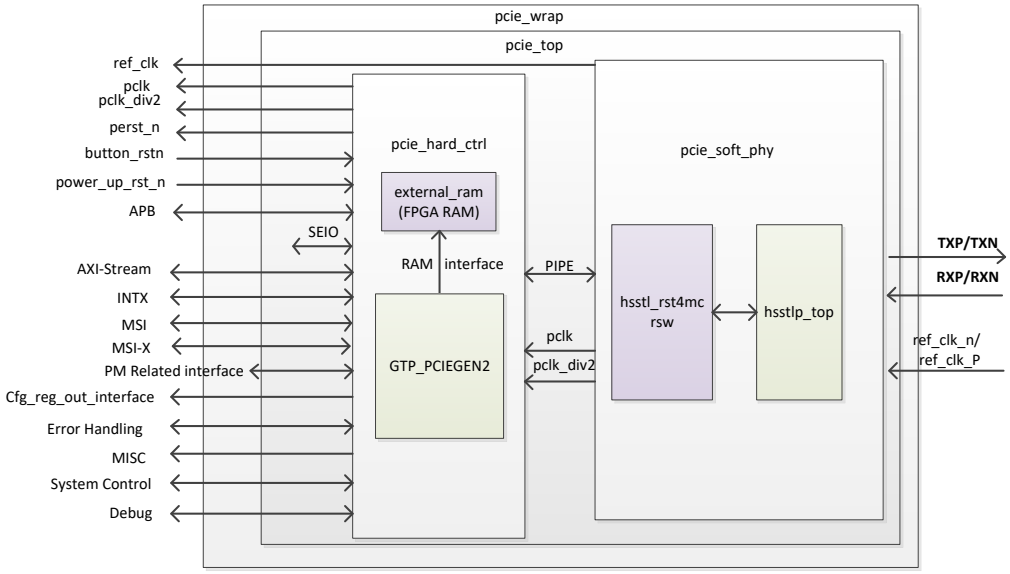

Figure 2-1 Functional Diagram of PCI Express IP

PCI Express IP primarily consists of two parts: pcie_hard_ctrl and pcie_soft_phy.

2.2.1 pcie_hard_ctrl

The pcie_hard_ctrl implements the main functions of the Transaction Layer, Data Link Layer, and Physical Layer (MAC) related to the protocol.

- external_ram: Implements RCV_HEAD_RAM, RCV_DATA_RAM, RETRY_DATA_RAM functions of PCIe;
- GTP_PCIEGEN2: Implements the primary functions of PCIe.

2.2.2 pcie_soft_phy

pcie_soft_phy includes HSST and its corresponding reset sequence.

- hsst_rst4mcrsw: HSST reset sequence;
- hsst_top: HSST top level.

2.3 IP Generation Flow Steps

2.3.1 Module Instantiation

Users can customise the PCI Express IP and instantiate the required IP modules via the IPC tool. For detailed instructions on using the IPC tool, please refer to *"**IP_Compiler_User_Guide**"*.

The main steps for instantiating the PCI Express IP module are described as follows.

2.3.1.1 Selecting IP

Open IPC and click File > Update in the main window to open the Update IP dialog box, where you add the corresponding version of the IP model.

After selecting the FPGAs device type, the Catalog interface displays the loaded IP models. Select the corresponding version of PCI Express under the "System/PCIe" directory. The IP selection path is shown in Figure 2-2. Then set the Pathname and Instance Name on the right side of the page. The project instantiation interface is shown in Figure 2-3.

Attention:

PG2L50H, PG2L25H: The software version must be 2022.1 or above.

PG2L100H: The software version must be 2021.1-SP7.2, 2021.4-SP1, 2022.1 or above.

PG2L200H: The software version must be 2022.2 or above.

PG2L100HX: The software version must be 2023.1 or above.

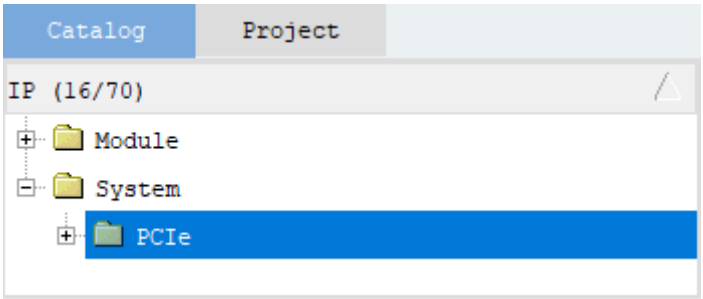

Figure 2-2 PCI Express IP Selection Path Interface

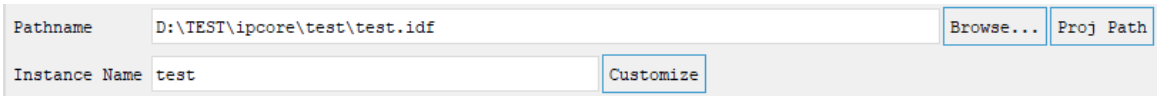

Figure 2-3 Project Instantiation Interface

2.3.1.2 IP parameter configuration

After selecting IP, click <Customize> to enter the PCI Express parameter settings interface, where the configuration window is as shown below. For IP configuration parameters, please refer to Table 2-3.

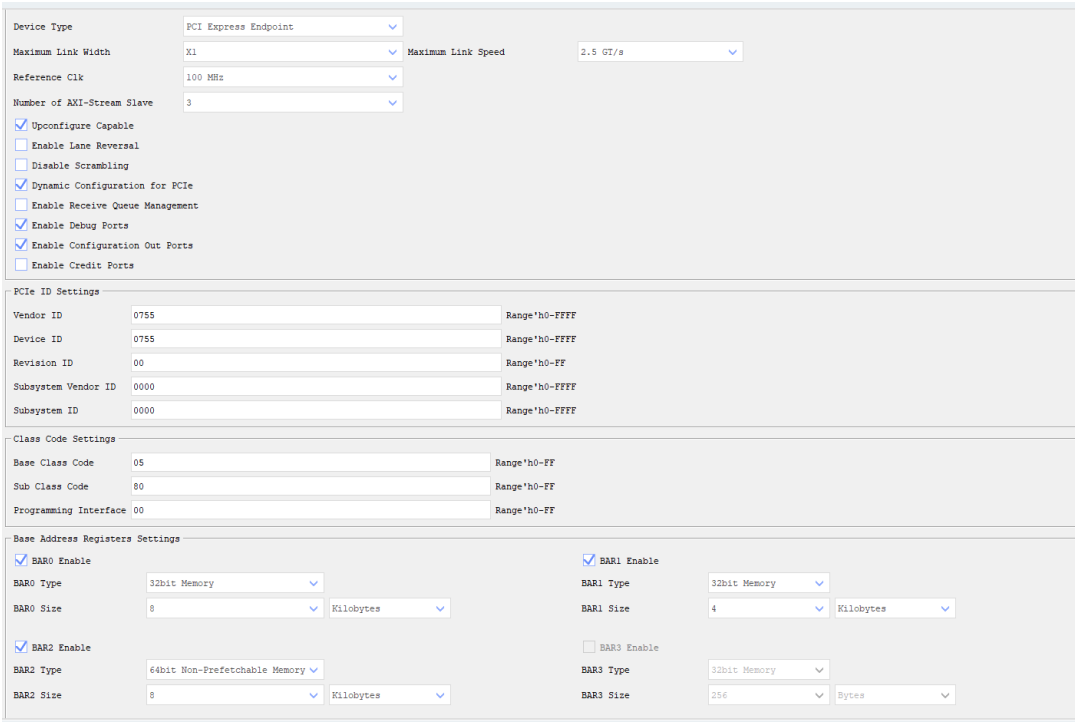

Figure 2-4 PCI Express Parameter Configuration Interface

Table 2-3 PCIe IP Configuration Parameter Description

Option Domain	**Parameter/Configuration Options**	**Parameter Description**	**Default Value**
PCIe Basic Settings	Device Type	Select PCIe device type	PCI Express Endpoint
	Maximum Link Width	Set the maximum link width supported by PCIe device	X1
	Maximum Link Speed	Configure the maximum link speed supported by PCIe device	2.5 GT/s
	Reference Clk	Select reference clock	100 MHz
	Number of AXI-Stream Slave	Select the number of AXI-Stream Slaves	3

Option Domain	Parameter/Configuration Options	Parameter Description	Default Value
	Upconfigure Capable	Upconfigure Capable enable option Selected: Enable Upconfigure Capable function Cleared: Disable Upconfigure Capable function	Selected
	Enable Lane Reversal	Lane Reversal enable option Selected: Enable automatic Lane Reversal function Cleared: Disable automatic Lane Reversal function	Cleared
	Disable Scrambling	Scrambling and descrambling enable option Selected: Disable scrambling and descrambling Cleared: Enable scrambling and descrambling	Cleared
	Dynamic Configuration for PCIe	PCIe configuration space register dynamic read/write interface (APB interface) enable option Selected: Enable dynamic read/write of PCIe configuration space registers Cleared: Disable dynamic read/write of PCIe configuration space registers	Selected
	Enable Receive Queue Management	User interface receive Buffer management interface enable option Selected: Enable Receive Queue Management Cleared: Disable Receive Queue Management	Cleared
	Enable Debug Ports	Debug interface enable option Selected: Enable Debug interface Cleared: Disable Debug interface	Selected
	Enable Configuration Out Ports	Configuration space information output interface enable option Only valid when Debug interface is enabled Selected: Enable Configuration Out interface Cleared: Disable Configuration Out interface	Selected
	Enable Credit Ports	Peer Credit information enable option Only valid when Debug interface is enabled Selected: Enable Credit information interface Cleared: Disable Credit information interface	Cleared
PCIe ID Settings	Vendor ID	Set Vendor ID	0755
	Device ID	Set Device ID	0755
	Revision ID	Set Revision ID	00
	Subsystem Vendor ID	Set Subsystem Vendor ID Invalid in RC mode	0000
	Subsystem ID	Set Subsystem ID Invalid in RC mode	0000

Option Domain	Parameter/Configuration Options	Parameter Description	Default Value
Class Code Settings	Base Class Code	Set Base Class Code Fixed as 06 in RC mode	05
	Sub Class Code	Set Sub Class Code Fixed as 00 in RC mode	80
	Programming Interface	Set Programming Interface Fixed as 00 in RC mode	00
Base Address Registers Settings	BAR0 Enable	BAR0 enable option Selected: Enable BAR0 Cleared: Disable BAR0	Selected
	BAR0 Type	BAR0 type setting Options: 32bit Memory 32bit IO 64bit Prefetchable Memory 64bit Non-Prefetchable Memory 32bit IO cannot be selected in EP mode	32bit Memory
	BAR0 Size	BAR0 size setting For 32bit Memory and 32bit IO: The range is 256 Byte-2G Byte For 64bit Prefetchable Memory and 64bit Non-Prefetchable Memory: The range is 256 Byte-8E Byte	8 Kilobytes
	BAR1 Enable	BAR1 enable option Selected: Enable BAR1 Cleared: Disable BAR1	Selected
	BAR1 Type	BAR1 type setting Options: 32bit Memory 32bit IO 32bit IO cannot be selected in EP mode	32bit Memory
	BAR1 Size	BAR1 size setting The range is 256Byte-2G Byte	4 Kilobytes
	BAR2 Enable	BAR2 enable option Selected: Enable BAR2 Cleared: Disable BAR2	Selected
	BAR2 Type	BAR2 type setting Options: 32bit Memory 32bit IO 64bit Prefetchable Memory 64bit Non-Prefetchable Memory 32bit IO cannot be selected in EP mode	64bit Non-Prefetchable Memory
	BAR2 Size	BAR2 size setting: For 32bit Memory and 32bit IO: The range is 256Byte-2G Byte For 64bit Prefetchable Memory and 64bit Non-Prefetchable Memory: The range is 256Byte-8E Byte	8 Kilobytes
	BAR3 Enable	BAR3 enable option Selected: Enable BAR3 Cleared: Disable BAR3	Cleared
	BAR3 Type	BAR3 type setting Options: 32bit Memory 32bit IO 32bit IO cannot be selected in EP mode	32bit Memory

Option Domain	Parameter/Configuration Options	Parameter Description	Default Value
	BAR3 Size	BAR3 size setting The range is 256 Byte-2G Byte	256 Bytes
	BAR4 Enable	BAR4 enable option Selected: Enable BAR4 Cleared: Disable BAR4	Cleared
	BAR4 Type	BAR4 type setting Options: 32bit Memory 32bit IO 64bit Prefetchable Memory 64bit Non-Prefetchable Memory 32bit IO cannot be selected in EP mode	32bit Memory
	BAR4 Size	BAR4 size setting For 32bit Memory and 32bit IO: The range is 256 Byte-2G Byte For 64bit Prefetchable Memory and 64bit Non-Prefetchable Memory: The range is 256 Byte-8E Byte	256 Bytes
	BAR5 Enable	BAR5 enable option Selected: Enable BAR5 Cleared: Disable BAR5	Cleared
	BAR5 Type	BAR5 type setting Options: 32bit Memory 32bit IO 32bit IO cannot be selected in EP mode	32bit Memory
	BAR5 Size	BAR5 size setting The range is 256 Byte-2G Byte	256 Bytes
	Expansion ROM Enable	Expansion ROM enable option Selected: Enable Expansion ROM Cleared: Disable Expansion ROM	Cleared
	Expansion ROM Size	Expansion ROM size setting The range is 2KB-16MB	2 Kilobytes
Device Capabilities Settings	Max Payload Size	Select Max Payload Size supported by PCIe	128 Bytes
	Extended Tag Field	Extended Tag Field enable option Selected: Enable Extended Tag Field (IP supports up to 64 Tags) Cleared: Disable Extended Tag Field (IP supports up to 32 Tags)	Selected
	Extended Tag Default	Extended Tag Default enable option Selected: Enable Extended Tag Field Cleared: Disable Extended Tag Field	Selected
Device Capabilities 2 Settings	Atomic Enable	Atomic enable option Selected: Enable Atomic (AtomicOp supported) Cleared: Disable Atomic (AtomicOp not supported)	Cleared
Link Control Settings	Read Completion Boundary	Configure Link Control Register[3] (only configurable in RC) The rest is fixed at 128Byte	128 byte
Link Control2 Settings	Target Link Speed	Configure Link Control 2 Register[3:0] Only configurable at 5GT/s	2.5 GT/s
Root Capabilities Settings	CRS Software Visibility	Configure Root Capabilities Register [0] Only configurable in RC	Cleared

Option Domain	Parameter/Configuration Options	Parameter Description	Default Value
Advanced Error Capabilities Settings	ECRC Generation Capable	Configure Advanced Error Capabilities and Control Register[5]	Cleared
	ECRC Check Capable	Configure Advanced Error Capabilities and Control Register[7]	Selected
Legacy Interrupt Settings	INTX Enable	INTX enable option: Selected: Enable INTX Cleared: Disable INTX	Cleared
	Interrupt Pin	Select INTX Interrupt PIN (only valid when INTX Enable is enabled) EP and Legacy EP: Only INTA and INTB are supported RC: INTA, INTB, INTC, and INTD are supported	INTA
MSI Interrupt Settings	MSI Enable	MSI Capability enable option Selected: Enable MSI Capability Cleared: Disable MSI Capability	Cleared
	64bit Address Capable	MSI 64bit Address Capable enable option Selected: 64bit Address MSI supported Cleared: 64bit Address MSI not supported	Cleared
	Multiple Message Capable	Select the number of supported MSI vectors	1 Vector
	Per-Vector Masking Capable	MSI Per-Vector Masking Capable enable option Selected: Per-Vector Masking Capable supported Cleared: Per-Vector Masking Capable not supported	Cleared
MSIx Interrupt Settings	MSIx Enable	MSI-X Capability enable option Selected: Enable MSI-X Capability Cleared: Disable MSI-X Capability	Cleared
	Table Size	Configure MSI-X Table size	0x1
	Table Offset	Configure MSI-X Table Offset	0x0
	Table BIR	Configure MSI-X Table mapping BAR location	BAR0
	PBA Offset	Configure MSI-X PBA Offset	0x0
	PBA BIR	Configure MSI-X PBA mapping BAR location	BAR0

2.3.1.3 Generating IP

Upon completion of parameter configuration, click the <Generate> button in the top left corner to generate the PCIe IP set by the user. The information report interface for IP generation is shown in Figure 2-5.

Figure 2-5 PCIe IP Generation Report Interface

Attention:

The .pds and .fdc files generated with the IP are for reference only; please modify the pin constraints according to the actual pin connections when in use.

Upon successful IP generation, the files indicated in Table 2-4 will be output under the Instance path specified in step 1.

Table 2-4 Output Files after PCIe IP Generation

Output File[1]	**Description**
$instname.v	The top-level .v file of the generated IP.
$instname.idf	The Configuration file of the generated IP.
/rtl/*.v	The RTL code file of the generated IP.
/rtl/ external_ram/*.v	The plaintext RTL file of the generated IP, which contains the RAM modules for implementing the PCIe functions RCV_HEAD_RAM, RCV_DATA_RAM, RETRY_DATA_RAM.
/rtl/ hsstlp/*.v	Plaintext RTL files of the generated IP. This folder stores the HSSTLP module.
/rtl/ hsst_pipe/*.v	Plaintext RTL file of the generated IP, which stores the HSSTLP reset sequence.
<project_path>/sim/modelsim/*.f	The list of .v files required for ModelSim simulation of the generated Example Design.
/sim/modelsim/*.do	The do script files and do waveform files for ModelSim simulation of the generated Example Design.
/sim/modelsim/*.bat	The script for ModelSim simulation of the generated Example Design.
/example_design/bench/ pango_ pcie _top_tb.v	The tb file of the Example Design's top-level file.
/example_design/bench/ pango_pcie_top.v	The top-level file of the Example Design.
/example_design/bench/ pango_pcie_top_sim.v	The top-level file of the Example Design for simulation connection.
/example_design/bench/ ips2l_pcie_wrap_v1_3_sim.v	The IP top-level file for simulation connection.
/example_design/rtl/*.v	Some module files and top-level files used in Example Design. For detailed information, please refer to "2.4 Example Design".
/pnr/core_only/<instance_name>.pds	The project file of the generated IP core.
/pnr/core_only/<instance_name>.fdc	The constraint file of the generated IP core.
/pnr/example_design /pango_pcie_top.pds	The project file of the Example Design.
/pnr/example_design /pango_pcie_top.fdc	The constraint file of the generated Example_Design.
/rev_1	The default output path for synthesis reports. (This folder is generated only after specifying the synthesis tool)

1 "$instname" is the instantiation name entered by the user; "*" is a wildcard character representing filenames of the same type.

Output File[1]	Description
readme.txt	The readme file describes the structure of the generation directory after the IP is generated.

2.3.2 Constraint Configuration

For the specific configuration method of constraint files, please refer to the relevant help documents in the PDS installation path: "***User_Constraint_Editor_User_Guide***", "***Physical_Constraint_Editor_User_Guide***", "***Route_Constraint_Editor_User_Guide***".

2.3.3 Simulation Runs

The simulation of the PCI Express IP is based on the Test Bench of the Example Design. For detailed information about Example Design, please refer to "2.4 Example Design".

For more details about the PDS simulation functions and third-party simulation tools, please consult the related help documents in the PDS installation path: "***Pango_Design_Suite_User Guide***", "***Simulation_User_Guide***".

2.3.4 Synthesis and Placement/Routing

The specific usage of PDS synthesis tools and placement/routing tools can be found in the help documents within the PDS installation path.

Attention:

Example Design project files .pds and pin constraint files .fdc generated with the IP are located in the "/pnr/example_design" directory, and physical constraints need to be modified according to the actual devices and PCB trace routing. For details, please refer to "2.8 Descriptions and Considerations".

2.3.5 Resources Utilization

Table 2-5 Typical Resource Utilization Values for PCIe IP Based on Applicable Devices

Device	Configuration Mode		Typical Resource Utilization Values						
			LUT	FF	DRAM	HSSTLP	GPLL	PCIE	USCM
PG2L200H	PCI Express Endpoint	Gen1, x1	506	694	8.5	0.5	1	1	3
		Gen2, x1	500	683	8.5	0.5	1	1	3
		Gen1, x2	651	810	8.5	0.5	0	1	1
		Gen2, x2	635	810	8.5	0.5	0	1	1
		Gen1, x4	862	1024	8.5	1	0	1	1
		Gen2, x4	864	1024	8.5	1	0	1	1
	Legacy PCI Express Endpoint	Gen1, x1	506	694	8.5	0.5	1	1	3
		Gen2, x1	500	683	8.5	0.5	1	1	3
		Gen1, x2	651	810	8.5	0.5	0	1	1
		Gen2, x2	635	810	8.5	0.5	0	1	1
		Gen1, x4	862	1024	8.5	1	0	1	1
		Gen2, x4	864	1024	8.5	1	0	1	1
	PCI Express Root Complex	Gen1, x1	498	683	8.5	0.5	1	1	3
		Gen2, x1	500	683	8.5	0.5	1	1	3
		Gen1, x2	644	810	8.5	0.5	0	1	1
		Gen2, x2	637	810	8.5	0.5	0	1	1
		Gen1, x4	855	1024	8.5	1	0	1	1
		Gen2, x4	857	1024	8.5	1	0	1	1
PG2L100H	PCI Express Endpoint	Gen1, x1	567	707	8	0.5	1	1	3
		Gen2, x1	565	705	8	0.5	1	1	3
		Gen1, x2	720	845	8	0.5	0	1	1
		Gen2, x2	727	847	8	0.5	0	1	1
		Gen1, x4	996	1101	8	1	0	1	1
		Gen2, x4	996	1102	8	1	0	1	1
	Legacy PCI Express Endpoint	Gen1, x1	569	705	8	0.5	1	1	3
		Gen2, x1	570	704	8	0.5	1	1	3
		Gen1, x2	741	842	8	0.5	0	1	1
		Gen2, x2	712	842	8	0.5	0	1	1
		Gen1, x4	995	1102	8	1	0	1	1
		Gen2, x4	995	1104	8	1	0	1	1
	PCI Express Root Complex	Gen1, x1	588	705	8	0.5	1	1	3
		Gen2, x1	561	704	8	0.5	1	1	3
		Gen1, x2	725	842	8	0.5	0	1	1
		Gen2, x2	723	840	8	0.5	0	1	1
		Gen1, x4	1001	1101	8	1	0	1	1
		Gen2, x4	1001	1101	8	1	0	1	1

Device	Configuration Mode		Typical Resource Utilization Values						
			LUT	FF	DRAM	HSSTLP	GPLL	PCIE	USCM
PG2L100HX	PCI Express Endpoint	Gen1, x1	502	694	8.5	0.5	1	1	3
		Gen2, x1	494	683	8.5	0.5	1	1	3
		Gen1, x2	622	810	8.5	0.5	0	1	1
		Gen2, x2	617	810	8.5	0.5	0	1	1
		Gen1, x4	830	1024	8.5	1	0	1	1
		Gen2, x4	830	1024	8.5	1	0	1	1
	Legacy PCI Express Endpoint	Gen1, x1	502	694	8.5	0.5	1	1	3
		Gen2, x1	494	683	8.5	0.5	1	1	3
		Gen1, x2	622	810	8.5	0.5	0	1	1
		Gen2, x2	617	810	8.5	0.5	0	1	1
		Gen1, x4	830	1024	8.5	1	0	1	1
		Gen2, x4	830	1024	8.5	1	0	1	1
	PCI Express Root Complex	Gen1, x1	492	683	8.5	0.5	1	1	3
		Gen2, x1	491	683	8.5	0.5	1	1	3
		Gen1, x2	619	810	8.5	0.5	0	1	1
		Gen2, x2	619	810	8.5	0.5	0	1	1
		Gen1, x4	838	1024	8.5	1	0	1	1
		Gen2, x4	842	1024	8.5	1	0	1	1
PG2L50H	PCI Express Endpoint	Gen1, x1	567	707	8	0.5	1	1	3
		Gen2, x1	565	705	8	0.5	1	1	3
		Gen1, x2	720	845	8	0.5	0	1	1
		Gen2, x2	727	847	8	0.5	0	1	1
		Gen1, x4	996	1101	8	1	0	1	1
		Gen2, x4	996	1102	8	1	0	1	1
	Legacy PCI Express Endpoint	Gen1, x1	569	705	8	0.5	1	1	3
		Gen2, x1	570	704	8	0.5	1	1	3
		Gen1, x2	741	842	8	0.5	0	1	1
		Gen2, x2	712	842	8	0.5	0	1	1
		Gen1, x4	995	1102	8	1	0	1	1
		Gen2, x4	995	1104	8	1	0	1	1
	PCI Express Root Complex	Gen1, x1	588	705	8	0.5	1	1	3
		Gen2, x1	561	704	8	0.5	1	1	3
		Gen1, x2	725	842	8	0.5	0	1	1
		Gen2, x2	723	840	8	0.5	0	1	1
		Gen1, x4	1001	1101	8	1	0	1	1
		Gen2, x4	1001	1101	8	1	0	1	1

Device	Configuration Mode		Typical Resource Utilization Values						
			LUT	FF	DRAM	HSSTLP	GPLL	PCIE	USCM
PG2L25H	PCI Express Endpoint	Gen1, x1	567	707	8	0.5	1	1	3
		Gen2, x1	565	705	8	0.5	1	1	3
		Gen1, x2	720	845	8	0.5	0	1	1
		Gen2, x2	727	847	8	0.5	0	1	1
		Gen1, x4	996	1101	8	1	0	1	1
		Gen2, x4	996	1102	8	1	0	1	1
	Legacy PCI Express Endpoint	Gen1, x1	569	705	8	0.5	1	1	3
		Gen2, x1	570	704	8	0.5	1	1	3
		Gen1, x2	741	842	8	0.5	0	1	1
		Gen2, x2	712	842	8	0.5	0	1	1
		Gen1, x4	995	1102	8	1	0	1	1
		Gen2, x4	995	1104	8	1	0	1	1
	PCI Express Root Complex	Gen1, x1	588	705	8	0.5	1	1	3
		Gen2, x1	561	704	8	0.5	1	1	3
		Gen1, x2	725	842	8	0.5	0	1	1
		Gen2, x2	723	840	8	0.5	0	1	1
		Gen1, x4	1001	1101	8	1	0	1	1
		Gen2, x4	1001	1101	8	1	0	1	1

2.4 Example Design

This section introduces the Example Design scheme for PCIe IP based on Root Complex and Endpoint connection. The scheme instantiates a Root Complex type PCIe IP and an Endpoint type PCIe IP, which auto-negotiation upon connection. After successful negotiation, the RC performs DMA or PIO operations by sending TLP packets.

2.4.1 Design Block Diagram

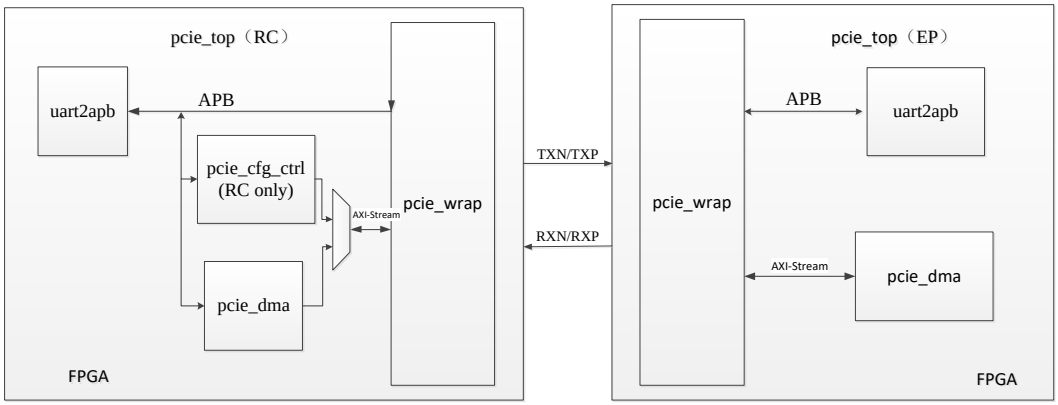

Figure 2-6 PCIe IP Example Design Block Diagram

2.4.2 Module Description

2.4.2.1 pcie_top module

The top level of the Example Design.

2.4.2.2 uart2apb module

Interface conversion module, converting serial port to standard APB interface.

2.4.2.3 pcie_cfg_ctrl module

Only effective in RC. It generates Cfg TLP packets that comply with the AXI-Stream interface timing based on the user's configuration through the APB interface, completing the configuration of the EP. For details on the specific register configuration, please refer to "2.4.3.3 CFG_CTRL (Offset = 0x9000)".

2.4.2.4 pcie_dma module

DMA control module, which generates TLP packets that comply with AXI-Stream interface timing based on the configuration, completing the DMA control function. For details on the specific register configuration, please refer to "2.4.3.2 DMA_CTRL (Offset=0x8000)".

2.4.2.5 pcie_wrap module

The top level of the PCIe IP.

2.4.3 Module register description

For module registers related to the Example Design, please refer to Table 2-6.

Table 2-6 Example Design Register Configuration Table

Base Addr	**Register Name**
0x7000	DBI_CORE_REG
0x8000	DMA_CTRL_REG
0x9000	CFG_CORE_REG

2.4.3.1 APB2DBI (Offset = 0x7000)

Convert APB interface to DBI interface, configuring the PCIe hard core function via the DBI interface.

2.4.3.2 DMA_CTRL (Offset=0x8000)

2.4.3.2.1 RC

Table 2-7 apb_cmd_reg (offset+0x140)

bit	**Name**	**Access**	**Description**
7:0	Reserved	Reserved	Must be 0
8	User_Data_Flag	W/R	Configure the source of Data in the MWr TLP packets 1: Use user-defined data packaging (only 1DW supported) 0: Use data packaging from the BAR Default: 0
15:9	Reserved	Reserved	None
16	ADDR_64	W/R	Configure the address length type 0: 32bit 1: 64bit Default: 0
23:17	Reserved	Reserved	None
24	FMT	W/R	Configure the type of TLP packets 0: MRd 1: MWr Default: 0
31:25	Reserved	Reserved	None

Table 2-8 apb_cmd_length (offset+0x150)

bit	Name	Access	Description
9: 0	Length	W/R	Configure the length of TLP packets [2] Default: 0
31:10	Reserved	Reserved	None

Table 2-9 apb_cmd_l_addr (offset+0x160)

bit	Name	Access	Description
1:0	Reserved	Reserved	None
31:2	ADDR_L	W/R	The lower 30 bits of the MEM access address Default: 0

Table 2-10 apb_cmd_h_addr (offset+0x170)

bit	Name	Access	Description
31:0	ADDR_H	W/R	The upper 32 bits of the MEM access address Default: 0

Table 2-11 apb_cmd_data (offset+0x180)

bit	Name	Access	Description
31:0	USER_DATA	W/R	Configure user data, used for configuring the DMA_REG of the EP

2.4.3.2.2 EP

Table 2-12 dma_cmd_reg (bar1+0x100)

bit	Name	Access	Description
9:0	Length	Reserved	P2P WR/RD Length[3]
16	ADDR_64	W/R	Configures address length type 0: 32bit 1: 64bit Default: 0
23:15	Reserved	Reserved	None

2 The actual effective length is {apb_cmd_length[9:0]+1} DW.

3 The actual effective length is { dma_cmd_reg [9:0]+1} DW.

bit	Name	Access	Description
24	FMT	W/R	Configure the type of TLP packets 0: MRd 1: MWr Default: 0
31:25	Reserved	Reserved	None

Table 2-13 dma_cmd_l_addr (bar1+0x110)

bit	Name	Access	Description
1:0	Reserved	Reserved	None
31:2	ADDR_L	W/R	The lower 30 bits of the MEM access address Default: 0

Table 2-14 dma_cmd_h_addr (bar1+0x120)

bit	Name	Access	Description
31:0	ADDR_H	W/R	The upper 32 bits of the MEM access address Default: 0

2.4.3.3 CFG_CTRL (Offset = 0x9000)

Table 2-15 CFG_CORE_REG0 (Offset+0x0)

bit	Name	Access	Description
0	FMT	W/R	Configure the type of TLP packets 0: RD FMT=3'b000 1: WR FMT=3'b010 Default: 0
1	TYPE	W/R	Configure Type 0: TYPE0 type=5'b00100 1: TYPE1 type=5'b00101 Default: 0
5:2	FBE	W/R	Configure First BE Default: 4'b0000
7:6	Reserved	Reserved	None
15:8	TAG	W/R	Configure TAG Default: 8'h0
16	CPL_RCV	W1C	Cpl receive Flag, indicates receipt of Cpl TLP
19:17	CPL_STATUS	W1C	Type of received Cpl 000: Successful Completion (SC) 001: Unsupported Request (UR) 010: Configuration Request Retry Status (CRS) 100: Completer Abort (CA) Others: Reserved
23:20	Reserved	Reserved	None

bit	Name	Access	Description
24	TX_EN	W/R	Cfg Request transmit enable Default: 0
31:25	Reserved	Reserved	None

Table 2-16 CFG_CORE_REG1 (Offset+0x4)

bit	Name	Access	Description
15:0	REQ_ID	W/R	Configure Requester ID Default: 15'h00
31:16	DES_ID	W/R	Configure destination ID field

Table 2-17 CFG_CORE_REG2 (Offset+0x8)

bit	Name	Access	Description
9:0	REG_NUM	W/R	Configure Cfg REG_NUM Default: 0x0
23:10	Reserved	Reserved	None
24	CFG_CTRL_EN	W/R	When this Bit is 1: CFG_CTRL can use axis_master interface
31:25	Reserved	Reserved	None

Table 2-18 CFG_CORE_REG3 (Offset+0xc)

bit	Name	Access	Description
31:0	DATA	W/R	Transmit the DATA field in the CFG write request default: 0x0

Table 2-19 CFG_CORE_REG4 (Offset+0x10)

bit	Name	Access	Description
31:0	RDATA	R	Receive the DATA field by sending CFG read request default: 0x0

2.4.3.4 Configuration Process

For the detailed configuration process of the Example Design, please refer to <instance_name>/example_design/bench/ pango_ pcie _top_tb.v[4].

2.4.4 Instance Configuration

This scheme requires using APB to configure the configuration space registers, and there are requirements for the setting of BARs, which can be supported by using the default configuration of IPC.

2.4.5 Instance Simulation

In the Windows system, after IP generation, double-click the *.bat file[4] under the "<project_path>/sim/modelsim" path to run simulation.

2.5 IP Interface Description

Descirption:

All ports and parameters listed in this document are those applied to the Example Design and IP; for requirements on other functions, ports, or parameters, please contact FAE/AE.

4 For the output files after IP generation, please refer to Table 2-4.

2.5.1 Descriptions of Ports

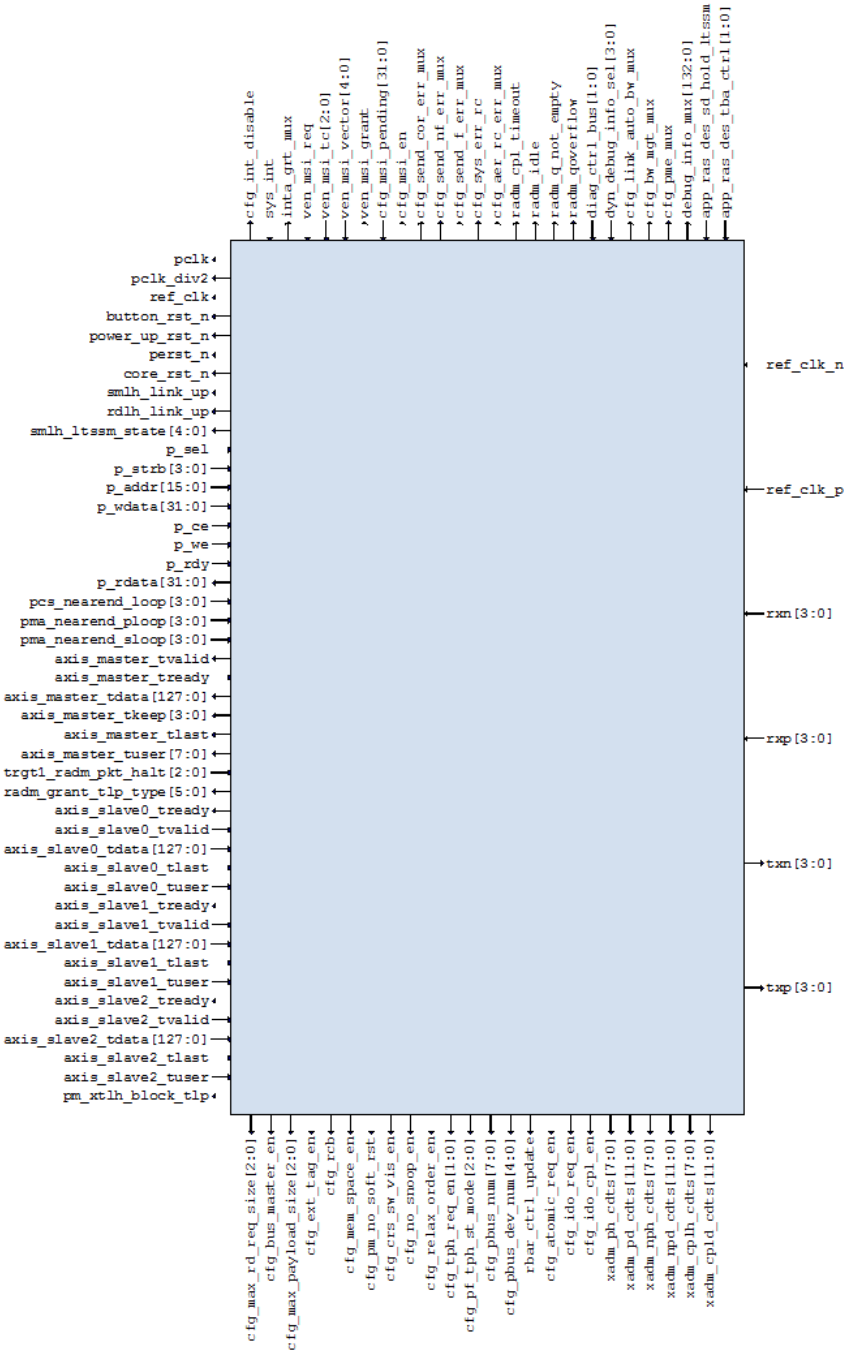

Figure 2-7 PCIe IP Interface Description

2.5.2 1I/O Pin List Description

Table 2-20 PCIe IP Pin List

Port	I/O	Bit width	Description
pclk	O	1	PCIe core working clock (provided by HSST) 2.5GT/S: 125MHz 5GT/S: 250MHz
pclk_div2	O	1	User interface clock (provided by HSST) 2.5GT/S: 62.5MHz 5GT/S: 125MHz
button_rst_n	I	1	Reset signal, active low, asynchronous reset, button reset, for debugging only.
power_up_rst_n	I	1	Reset signal, active low, asynchronous reset, from slot PERST#.
perst_n	I	1	Reset signal, active low, asynchronous reset, from slot PERST#.
ref_clk	O	1	Bypass output of HSSTLP reference clock (for apb_clk)
core_rst_n	O	1	Hard core reset signal output, for user logic. pclk_div2 clock domain, active low.
System Control			
smlh_link_up	O	1	1: PHY Link up (pclk_div2 clock domain)
rdlh_link_up	O	1	1: DLL Link up (pclk_div2 clock domain)
smlh_ltssm_state	O	5	5'h00: DETECT_QUIET 5'h01: DETECT_ACT 5'h02: POLL_ACTIVE 5'h03: POLL_COMPLIANCE 5'h04: POLL_CONFIG 5'h05: PRE_DETECT_QUIET 5'h06: DETECT_WAIT 5'h07: CFG_LINKWD_START 5'h08: CFG_LINKWD_ACEPT 5'h09: CFG_LANENUM_WAI 5'h0A: FG_LANENUM_ACEPT 5'h0B: CFG_COMPLETE 5'h0C: CFG_IDLE 5'h0D: RCVRY_LOCK 5'h0E: RCVRY_SPEED 5'h0F: RCVRY_RCVRCFG 5'h10: RCVRY_IDLE 5'h11: L0 5'h12: L0S 5'h13: L123_SEND_EIDLE 5'h14: L1_IDLE 5'h15: L2_IDLE 5'h16: L2_WAKE 5'h17: DISABLED_ENTRY 5'h18: DISABLED_IDLE 5'h19: DISABLED 5'h1A: LPBK_ENTRY 5'h1B: LPBK_ACTIVE 5'h1C: LPBK_EXIT 5'h1D: LPBK_EXIT_TIMEOUT 5'h1E: HOT_RESET_ENTRY 5'h1F: HOT_RESET

Port	I/O	Bit width	Description
pcs_nearend_loop	I	4	Control HSST to conduct near-end loopback in PCS (bit 0~3 corresponds to lane 0~3 separately) 1: Enable 0: Disable
pma_nearend_ploop	I	4	Control HSST to conduct near-end parallel loopback in PMA (bit 0~3 corresponds to lane 0~3 separately) 1: Enable 0: Disable
pma_nearend_sloop	I	4	Control HSST to conduct near-end serial loopback in PMA (bit 0~3 corresponds to lane 0~3 separately) 1: Enable 0: Disable
Configuration Signals			
cfg_pbus_num	O	8	Bus Num currently acquired by the device
cfg_pbus_dev_num	O	5	Device Num currently acquired by the device
cfg_max_rd_req_size	O	3	The value of the Max_Read_Request_Size field in the Device Control register[14:12]
cfg_bus_master_en	O	1	The state of the bus master enable bit in the PCI-compatible Command register
cfg_max_payload_size	O	3	The value of the Max_Payload_Size field in the Device Control register[7:5]
cfg_ext_tag_en	O	1	0: Devices must use the tag in the range of 0~31 1: Devices must use the tag in the range of 0~63
cfg_rcb	O	1	The value of the RCB bit in the Link Control register[3]
cfg_mem_space_en	O	1	The state of the Memory Space Enable bit in the PCI-compatible Command register[1]
cfg_pm_no_soft_rst	O	1	This is the value of the No Soft Reset bit in the Power Management Control and Status Register
cfg_crs_sw_vis_en	O	1	Indicates the value of the CRS Software Visibility enable bit in the Root Control register
cfg_no_snoop_en	O	1	Contents of the "Enable No Snoop" field in the Device_ Control register[11]
cfg_relax_order_en	O	1	Contents of the "Enable Relaxed Ordering" field in the Device_ Control register[4]
cfg_tph_req_en	O	2	The 2-bit TPH Requester Enabled field of each TPH Requester Control register.
cfg_pf_tph_st_mode	O	3	Steering Tag Mode of Operation for Physical Function
cfg_atomic_req_en	O	1	The AtomicOp Requester Enable field of the Device Control 2 register[6]
cfg_atomic_egress_block	O	1	The AtomicOp Egress Blocking field of the Device Control 2 register
rbar_ctrl_update	O	1	Indicates that a resizable BAR control register has been updated
PHY Diff Signals			
ref_clk_n	I	1	HSSTHP differential reference clock signal (100MHz)
ref_clk_p	I	1	
rxn	I	4	HSSTHP differential receive signal
rxp	I	4	
txn	O	4	HSSTHP differential transmit signal
txp	O	4	

Port	I/O	Bit width	Description
APB Interface			
p_sel	I	1	Corresponding to standard APB protocol PSELx
p_strb	I	4	Corresponding to standard APB protocol PSTRB
p_addr	I	16	Corresponding to standard APB protocol PADDR
p_wdata	I	32	Corresponding to standard APB protocol PWDATA
p_ce	I	1	Corresponding to standard APB protocol PENABLE
p_we	I	1	Corresponding to standard APB protocol PWRITE
p_rdy	O	1	Corresponding to standard APB protocol PREADY
p_rdata	O	32	Corresponding to standard APB protocol PRDATA
AXI Master Interface			
axis_master_tvalid	O	1	Corresponding to standard AXI4-Stream protocol TVALID
axis_master_tready	I	1	Corresponding to standard AXI4-Stream protocol TREADY
axis_master_tdata	O	128	Corresponding to standard AXI4-Stream protocol TDATA
axis_master_tkeep	O	4	DW enable signal[5] ("1" indicates the corresponding DW data is valid) axis_master_tkeep[3] control axis_master_tdata[127:96] axis_master_tkeep[2] control axis_master_tdata[95:64] axis_master_tkeep[1] control axis_master_tdata[63:32] axis_master_tkeep[0] control axis_master_tdata[31:0]
axis_master_tlast	O	1	Corresponding to standard AXI4-Stream protocol TLAST
axis_master_tuser	O	8	Sideband information transmitted alongside axis_master_tdata: 0: radm_trgt1_tlp_abort (Indicates to your application to drop the TLP because of malformed TLP on TRGT1, ECRC error, or completion lookup failures) 1: radm_trgt1_dllp_abort (Indicates to your application to drop the TLP on TRGT1 because of a Data Link Layer error such as LCRC or otherwise) 2: radm_trgt1_ecrc_err (Indicates to your application to drop the TLP because of an ECRC error in the received TLP on TRGT1) 3: radm_trgt1_cpl_last: Indicates the last completion TLP of a split completion transaction. [6:4] : radm_trgt1_in_membar_range[2:0] (Indicates which of the configured BARs contains the target address in the received TLP) 3'b0: bar0… 3'b1: bar1 3'b2: bar2 3'b3: bar3 3'b4: bar4 3'b5: bar5 7: radm_trgt1_rom_in_range (Indicates that the target address in the received TLP in range of the expansion ROM)

5 The difference from the AXIS standard is that here one Bit corresponds to the Enable of 4 Bytes.

Port	I/O	Bit width	Description
trgt1_radm_pkt_halt	I	3	Halts the transfer of packets from individual queues. There is one bit of trgt1_radm_pkt_halt for each TLP type for each configured VC: Bit 0: Halt posted TLPs for VC0 mwr Bit 1: Halt non-posted TLPs for VC0 mrd Bit 2: Halt CPL TLPs for VC0
radm_grant_tlp_type	O	6	Indicates that a particular VC and type transaction has been granted to output from the receive queue. There are two bits for each TLP type for each configured VC: Bit [1:0] : Grant posted TLPs for VC0 Bit [3:2] : Grant non-posted TLPs for VC0 Bit [5:4] : Grant CPL TLPs for VC0 Each 2-bit signal represents granted times in one cycle as follows: 2'b00: 0 granted 2'b01: 1 granted 2'b10: 1 granted 2'b11: 2 granted It is used together with trgt1_radm_pkt_halt to control the amount of dequeued transactions.
pm_xtlh_block_tlp	O	1	Indicates that your application must stop generating new outgoing request TLPs due to the current power management state
AXI Slave Interface			
axis_slave0/1/2_tready	O	1	Corresponding to standard AXI4-Stream protocol TVALID
axis_slave0/1/2_tvalid	I	1	Corresponding to standard AXI4-Stream protocol TREADY
axis_slave0/1/2_tdata	I	128	Corresponding to standard AXI4-Stream protocol TDATA
axis_slave0/1/2_tlast	I	1	Corresponding to standard AXI4-Stream protocol TLAST
axis_slave0/1/2_tuser	I	1	Sideband information transmitted alongside axis_slave_tdata: Bit 0: client0/1/2_tlp_bad_eot (Indicates that the current TLP must be nullified.)
Interrupt			
cfg_int_disable	O	1	When high a functions ability to generate INTx messages is Disabled
sys_int	I	1	When sys_int goes from low to high, the controller generates an Assert_INTx Message
inta_grt_mux	O	1	EP: 0->1: The signal indicates that the controller sent an Assert_INTA Message to the upstream device. 1->0: The signal indicates that the controller sent an Deassert_INTA Message to the upstream device. RC: 0->1: The signal indicates that the controller received an Assert_INTA Message from the downstream device 1->0: The signal indicates that the controller received an Deassert_INTA Message from the downstream device
intb_grt_mux	O	1	EP: Not used RC: 0->1: The signal indicates that the controller received an Assert_INTB Message from the downstream device 1->0: The signal indicates that the controller received an Deassert_INTB Message from the downstream device

Port	I/O	Bit width	Description
intc_grt_mux	O	1	EP: Not used RC: 0->1: The signal indicates that the controller received an Assert_INTC Message from the downstream device 1->0: The signal indicates that the controller received an Deassert_INTC Message from the downstream device
intd_grt_mux	O	1	EP: Not used RC: 0->1: The signal indicates that the controller received an Assert_INTD Message from the downstream device 1->0: The signal indicates that the controller received an Deassert_INTD Message from the downstream device
ven_msi_req	I	1	Request from your application to send an MSI/MSI-X when MSI/MSI-X is enabled 1: MSI/MSI-X Request active 0: MSI/MSI-X Request inactive
ven_msi_tc	I	3	Traffic Class of the MSI request, valid when ven_msi_req is asserted.
ven_msi_vector	I	5	Used to modulate the lower five bits of the MSI Data register when multiple message mode is enabled
ven_msi_grant	O	1	One-cycle pulse that indicates that the controller has accepted the request to send an MSI
cfg_msi_pending	I	32	Indication from application about which functions have a pending associated message
cfg_msi_en	O	1	Indicates that MSI is enabled (INTx message is not sent) 1: MSI Capability enable 0: MSI Capability disable
msix_addr	I	64	The address value for the MSI-X
msix_data	I	32	The data value for the MSI-X
cfg_msix_en	O	1	The MSI-X Enable bit of the MSI-X Control register in the MSI-X Capability structure 1: MSI-X Capability enable 0: MSI-X Capability disable
cfg_msix_func_mask	O	1	The function Mask bit of the MSI-X Control register in the MSI-X Capability structure
cfg_link_auto_bw_mux	O	1	cfg_link_auto_bw_int when legacy int is used, cfg_link_auto_bw_msi when MSI is enabled. Only for RC
cfg_bw_mgt_mux	O	1	cfg_bw_mgt_int when legacy int is used, cfg_bw_mgt_msi when MSI is enabled. Only for RC
cfg_pme_mux	O	1	cfg_pme_int when legacy int is used, cfg_pme_msi when MSI is enabled.
cfg_aer_rc_err_mux	O	1	cfg_aer_rc_err_int: when MSI is NOT enabled. Otherwise used as cfg_aer_rc_err_msi
Error Handling			
radm_cpl_timeout	O	1	Indicates that the completion TLP for a request has not been received within the expected time window
cfg_send_cor_err_mux	O	1	EP: cfg_send_cor_err Sent Correctable Error. RC: radm_correctable_err, One-clock-cycle pulse that indicates that the controller received an ERR_COR message.
cfg_send_nf_err_mux	O	1	EP: radm_nonfatal_err, Sent Non-Fatal Error RC: One-clock-cycle pulse that indicates that the controller received an ERR_NONFATAL message

Port	I/O	Bit width	Description
cfg_send_f_err_mux	O	1	EP: radm_fatal_err, Sent Fatal Error RC: One-clock-cycle pulse that indicates that the controller received an ERR_FATAL message.
cfg_sys_err_rc	O	1	System error detected
Debug Interface			
dyn_debug_info_sel	I	4	Dynamic debug_info_mux selection
app_ras_des_sd_hold_ltssm	I	1	Hold and release LTSSM. For as long as this signal is '1', thecontroller stays in the current LTSSM.
app_ras_des_tba_ctrl	I	2	Controls the start/end of time based analysis. You must only set the pins to the required value for the duration of one clock cycle. 2'b00: No action 2'b01: Start 2'b10: End. This setting is only used when the TIME_BASED_DU-RATION_SELECT field of TIME_BASED_ANALYSIS_CON-TROL_REG is set to "manual control". 2'b11: Reserved
radm_idle	O	1	RADM activity status signal
radm_q_not_empty	O	1	Level indicating that the receive queues contain TLP header/data.
radm_qoverflow	O	1	Pulse indicating that one or more of the P/NP/CPL receive queues have overflowed
diag_ctrl_bus	I	2	Diagnostic Control Bus, 01: Insert LCRC error by inverting the LSB of LCRC 10: Insert ECRC error by inverting the LSB of ECRC
debug_info_mux	O	133	dyn_debug_info_sel = 0: MSI [31:0] cfg_msi_mask[31:0] [95:32] cfg_msi_addr[63:0] [127:96] cfg_msi_data[31:0] 128 cfg_msi_64 [131:129] cfg_multi_msi_en[2:0] 132 cfg_msi_ext_data_en dyn_debug_info_sel =1: MSI-X [10:0] cfg_msix_table_size[10:0] [13:11] cfg_msix_table_bir[2:0] [42:14] cfg_msix_table_offset[28:0] [45:43] cfg_msix_pba_bir[2:0] [74:46] cfg_msix_pba_offset[28:0] dyn_debug_info_sel =2: TX debug &DL debug 0 xadm_no_fc_credit[NVC-1:0] 1 xadm_tlp_pending 2 xadm_had_enough_credit[NVC-1:0] 3 xdlh_not_expecting_ack 4 xdlh_xmt_pme_ack 5 xdlh_nodllp_pending [14:6] rtfcgen_incr_amt[8:0] 15 rtfcgen_incr_enable [17:16] rtfcgen_fctype[1:0] 18 xdlh_xtlh_halt 19 xtlh_xdlh_badeot 20 xtlh_xdlh_eot 21 xtlh_xdlh_sot [26:22] active_grant[NCL+2-1:0]

Port	I/O	Bit width	Description
			[31:27] grant_ack[NCL+2-1:0] [36:32] fc_cds_pass[(NCL+2)*NVC-1:0] [41:37] arb_reqs[NCL+2-1:0] 42 xmlh_xdlh_halt [44:43] xdlh_xmlh_sdp[1:0] [46:45] xdlh_xmlh_stp[1:0] [48:47] xdlh_xmlh_eot[1:0] [60:49] rdlh_xdlh_req_acknack_seqnum[11:0] 61 rdlh_xdlh_req2send_nack 62 rdlh_xdlh_req2send_ack_due2dup 63 rdlh_xdlh_req2send_ack [75:64] rdlh_xdlh_rcvd_acknack_seqnum[11:0] 76 rdlh_xdlh_rcvd_ack 77 rdlh_xdlh_rcvd_nack 78 cfg_link_retrain 79 rtlh_req_link_retrain 80 xdlh_smlh_start_link_retrain 81 rdlh_rtlh_tlp_dv [83:82] rdlh_rtlh_tlp_eot[1:0] [85:84] rdlh_rtlh_tlp_sot[1:0] 86 ecrc_err_asserted 87 lcrc_err_asserted dyn_debug_info_sel =3: 0 unexpected_cpl_err 1 cpl_ca_err 2 cpl_ur_err 3 flt_q_cpl_last 4 flt_q_cpl_abort 5 cpl_mlf_err [8:6] flt_q_header_cpl_status[2:0] [10:9] flt_q_header_destination[1:0] 11 form_filt_ecrc_err 12 form_filt_malform_tlp_err 13 form_filt_dllp_err 14 form_filt_eot [16:15] form_filt_dwen[NW-1:0] 17 form_filt_dv 18 form_filt_hv [20:19] rmlh_rdlh_pkt_err[NW-1:0] 21 rmlh_rdlh_pkt_dv [23:22] rmlh_rdlh_pkt_edb[NW-1:0] [25:24] rmlh_rdlh_pkt_end[NW-1:0] [27:26] rmlh_rdlh_tlp_start[NW-1:0] [29:28] rmlh_rdlh_dllp_start[NW-1:0] [31:30] rmlh_rdlh_nak[NW-1:0] [35:32] smlh_lanes_rcving[NL-1:0] 36 rmlh_rcvd_eidle_set 37 rmlh_rcvd_idle0 38 rmlh_rcvd_idle1 39 smlh_rcvd_lane_rev 40 smlh_ts_link_num_is_k237 41 rmlh_deskew_alignment_err 42 smlh_ts_lane_num_is_k237 43 smlh_ts2_rcvd 44 smlh_ts1_rcvd 45 smlh_ts_rcv_err

Port	I/O	Bit width	Description
			46 smlh_inskip_rcv dyn_debug_info_sel =4: [48:0] cxpl_debug_info[63:0] [64:49] cxpl_debug_info_ei[15:0] [67:65] pm_curnt_state[2:0] 68 pm_sel_aux_clk 69 en_muxd_aux_clk_g 70 en_radm_clk_g 71 link_req_rst_not 72 pm_req_core_rst 73 pm_req_phy_rst 74 pm_req_sticky_rst 75 pm_req_non_sticky_rst dyn_debug_info_sel =5: [7:0] cfg_int_pin[7:0] [43:8] cfg_rbar_size[35:0] 44 cfg_br_ctrl_serren 45 xdlh_replay_timeout_err 46 xdlh_replay_num_rlover_err 47 rdlh_bad_dllp_err 48 rdlh_bad_tlp_err 49 rdlh_prot_err 50 rtlh_fc_prot_err 51 rmlh_rcvd_err 52 int_xadm_fc_prot_err 53 radm_unexp_cpl_err 54 radm_rcvd_cpl_ur 55 radm_rcvd_cpl_ca 56 radm_rcvd_req_ca 57 radm_rcvd_req_ur 58 radm_ecrc_err 59 radm_mlf_tlp_err 60 radm_rcvd_cpl_poisoned 61 radm_rcvd_wreq_poisoned 62 cfg_sys_err_rc_cor 63 cfg_sys_err_rc_nf 64 cfg_sys_err_rc_f dyn_debug_info_sel =6: 0 cdm_lbc_ack [4:1] lbc_cdm_wr[3:0] 5 lbc_cdm_cs [37:6] lbc_cdm_data[31:0] [69:38] lbc_cdm_addr[31:0] dyn_debug_info_sel =7: 0 smlh_eidle_inferred_in_l0: Level: Detect EI Infer 1 rmlh_rcvd_err: Pulse: Receiver Error 2 smlh_rx_rcvry_req: Level: Rx Recovery Request 3 smlh_timeout_nfts: Level: FTS Timeout 4 rmlh_framing_err: Pulse: Framing Error 5 rmlh_deskew_alignment_err: Level: Deskew Error 6 rdlh_bad_tlp_err_pertlp : Pulse: BAD TLP 7 rdlh_lcrc_tlp_err_pertlp : Pulse: LCRC Error 8 rdlh_bad_dllp_err_perdllp: Pulse: BAD DLLP

Port	I/O	Bit width	Description
			9 xdlh_replay_num_rlover_err: Pulse: Replay_Num Rollover 10 xdlh_replay_timeout_err: Pulse: Replay Timeout 11 rdlh_rcvd_nack_perdllp: Pulse: Rx Nak DLLP 12 xdlh_nak_sent: Pulse: Tx Nak DLLP 13 xdlh_retry_req: Pulse: Retry TLP 14 rtlh_req_link_retrain: Level: FC Timeout [16:15] cfg_poisned_tlp: Pulse: Poisoned TLP [18:17] cfg_ecrc_tlp_err: Pulse: ECRC Error [20:19] cfg_ur_tlp: Pulse: Unsupported Request [22:21] cfg_ca_tlp: Pulse: Completer Abort [24:23] cfg_cpl_timeout[1:0]: Pulse: Completion Timeout 25 smlh_l0_to_recovery: Pulse: L0 to Recovery Entry 26 smlh_l1_to_recovery: Pulse: L1 to Recovery Entry 27 smlh_in_l0s: Level: Tx L0s Entry 28 smlh_in_rl0s: Level: Rx L0s Entry 29 pm_asnak: Level: ASPM L1 reject 30 smlh_in_l1: Level: L1 Entry 31 pm_in_l11: Level: L1.1 Entry 32 pm_in_l12: Level: L1.2 Entry 33 pm_in_l1_short: Level: L1 short duration 34 pm_in_l1_cpm: Level: L1 Clock PM (L1 with REFCLK removal/PLL Off) 35 pm_in_l1_abort: Level: L1.2 abort 36 smlh_in_l23: Level: L2 Entry 37 smlh_spd_change: Pulse: Speed Change 38 smlh_lwd_change: Pulse: Link width Change 39 xdlh_ack_sent: Pulse: Tx Ack DLLP 40 xdlh_update_fc_sent: Pulse: Tx Update FC DLLP 41 rdlh_rcvd_ack_perdllp: Pulse: Rx Ack DLLP 42 rtlh_rcvd_ufc_perdllp: Pulse: Rx Update FC DLLP 43 rdlh_nulified_tlp_err_pertlp : Pulse: Rx Nullified TLP 44 xtlh_xadm_restore_enable: Pulse: Tx Nullified TLP 45 rdlh_duplicate_tlp_err_pertlp: Pulse: Rx Duplicate TLP 46 xtlh_tx_memwr_evt: Pulse: Tx Memory Write 47 xtlh_tx_memrd_evt: Pulse: Tx Memory Read 48 xtlh_tx_cfgwr_evt: Pulse: Tx Config Write 49 xtlh_tx_cfgrd_evt: Pulse: Tx Config Read 50 xtlh_tx_iowr_evt: Pulse: Tx IO Write 51 xtlh_tx_iord_evt: Pulse: Tx IO Read 52 xtlh_tx_cplwod_evt: Pulse: Tx Completion wo data 53 xtlh_tx_cplwd_evt: Pulse: Tx Completion w data 54 xtlh_tx_msg_evt: Pulse: Tx Message 55 xtlh_tx_atmcop_evt: Pulse: Tx AtomicOp 56 xtlh_tx_tlpwprefix_evt: Pulse: Tx TLP with Prefix 57 rtlh_rx_memwr_evt: Pulse: Rx Memory Write 58 rtlh_rx_memrd_evt: Pulse: Rx Memory Read 59 rtlh_rx_cfgwr_evt: Pulse: Rx Config Write 60 rtlh_rx_cfgrd_evt: Pulse: Rx Config Read 61 rtlh_rx_iowr_evt: Pulse: Rx IO Write 62 rtlh_rx_iord_evt: Pulse: Rx IO Read 63 rtlh_rx_cplwod_evt: Pulse: Rx Completion wo data 64 rtlh_rx_cplwd_evt: Pulse: Rx Completion w data 65 rtlh_rx_msg_evt: Pulse: Rx Message TLP 66 rtlh_rx_atmcop_evt: Pulse: Rx Atomic 67 rtlh_rx_tlpwprefix_evt: Pulse: Rx TLP with Prefix 68 xtlh_tx_ccix_tlp_evt: Pulse: Tx CCIX TLP 69 rtlh_rx_ccix_tlp_evt: Pulse: Rx CCIX TLP

Port	I/O	Bit width	Description
			82:70 cdm_ras_des_ec_info_l0[12:0] 95:83 cdm_ras_des_ec_info_l1[12:0] 108:96 cdm_ras_des_ec_info_l2[12:0] 121:109 cdm_ras_des_ec_info_l3[12:0] 128:122 cdm_ras_des_tba_info_common[6:0] dyn_debug_info_sel =8: [4:0] pm_master_state[4:0]: Level: PM Internal State (Master) [8:5] pm_slave_state[3:0]: Level: PM Internal State (Slave) [15:9] rmlh_framing_err_ptr[6:0]: Pulse: 1st Framing Error Pointer [16] smlh_lane_reversed: Level: Lane Reversal Operation [17] pm_pme_resend_flag: Pulse: PME Re-Send flag [33:18] smlh_ltssm_variable [15:0]: Level: LTSSM Variable [36:34] ltssm_powerdown[1:0]: Level: PIPE: Power Down [44:37] latched_ts_nfts[7:0]: Level: Latched NFTS [46:45] rdlh_dlcntrl_state [1:0]: Level: DLCM [47] rdlh_vc0_initfc1_status: Level: Init-FC Flag1 VC0 [48] rdlh_vc0_initfc2_status: Level: Init-FC Flag2 VC0 [60:49] rdlh_curnt_rx_ack_seqnum[11:0]: Level: Rx ACK SEQ# [72:61] xdlh_curnt_seqnum [11:0]: Level: Tx TLP SEQ# 85:73 cdm_ras_des_sd_info_l0[12:0] 98:86 cdm_ras_des_sd_info_l1[12:0] 111:99 cdm_ras_des_sd_info_l2[12:0] 124:112 cdm_ras_des_sd_info_l3[12:0] dyn_debug_info_sel =9: 119:0 cdm_ras_des_sd_info_v0[239:120] dyn_debug_info_sel =10: 119:0 cdm_ras_des_sd_info_v0[119:0]
MISC			
cfg_ido_req_en	O	1	ID-Based Ordering Requests Enabled
cfg_ido_cpl_en	O	1	ID-Based Ordering Completions Enabled
xadm_ph_cdts	O	8	The amount of posted header buffer space currently available at the receiver at the other end of the link
xadm_pd_cdts	O	12	The amount of posted data buffer space currently available at the receiver at the other end of the link
xadm_nph_cdts	O	8	The amount of non-posted header buffer space currently available at the receiver at the other end of the link
xadm_npd_cdts	O	12	The amount of non-posted data buffer space currently available at the receiver at the other end of the link
xadm_cplh_cdts	O	8	The amount of completion header buffer space currently available at the receiver at the other end of the link
xadm_cpld_cdts	O	12	The amount of completion data buffer space currently available at the receiver at the other end of the link

2.5.3 APB Interface Timing

2.5.3.1 APB Read Timing

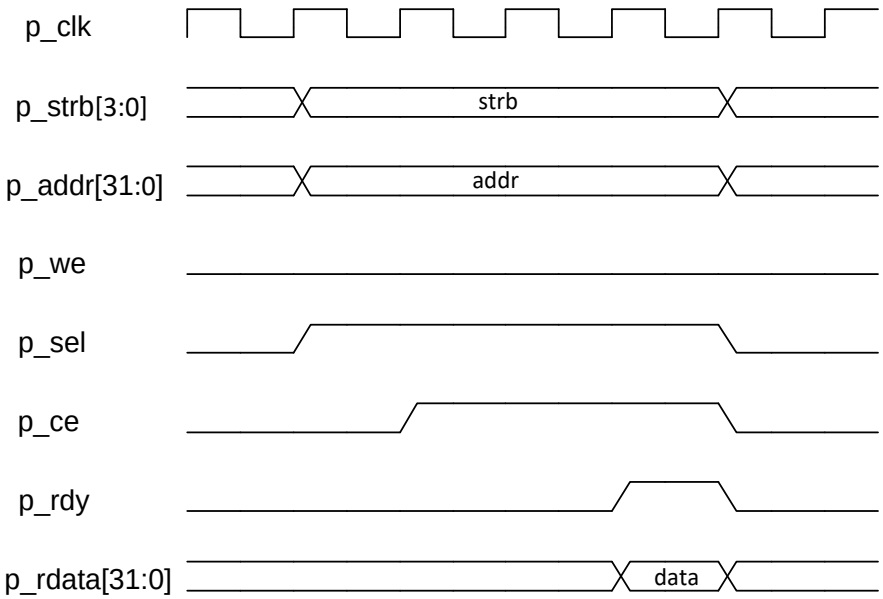

Figure 2-8 Basic APB Read Timing

2.5.3.2 APB Write Timing

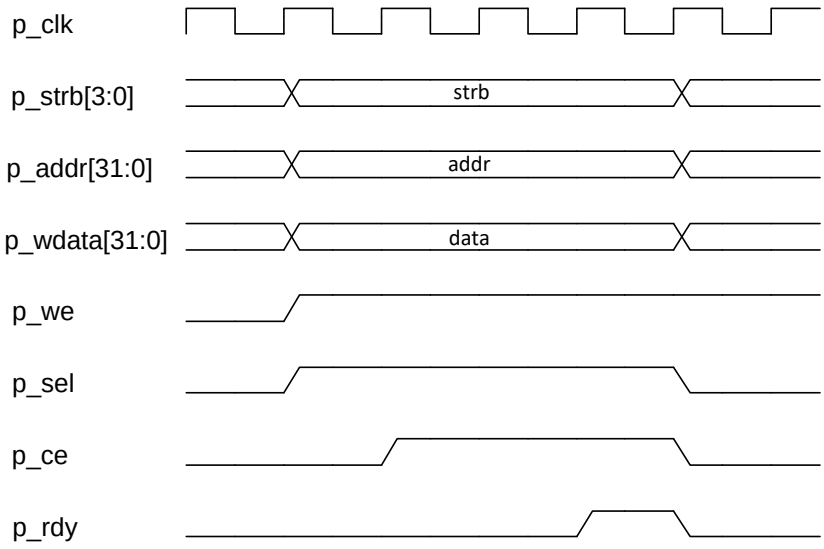

Figure 2-9 Basic APB Write Timing

2.5.4 User Interface Timing

2.5.4.1 AXI4-Stream Master operation timing

In the first cycle, axis_master_tdata is the TLP Header, and axis_master_tkeep is all 1s in the TLP Header field; for TLP format, please refer to "2.8.6 AXI-Stream Master Interface 3DW Usage Instructions".

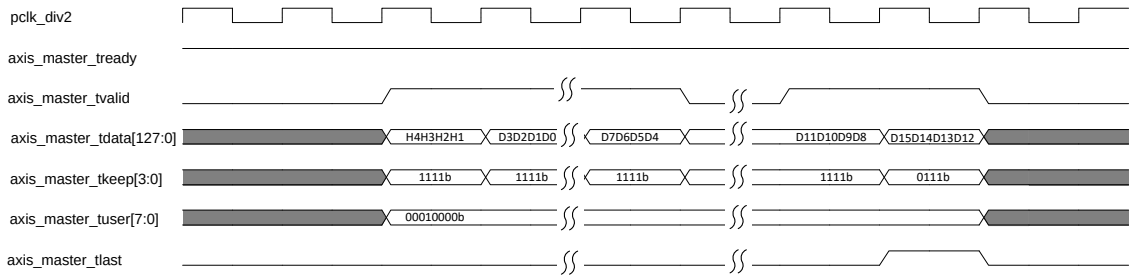

Figure 2-10 4DW Posted Operation Timing

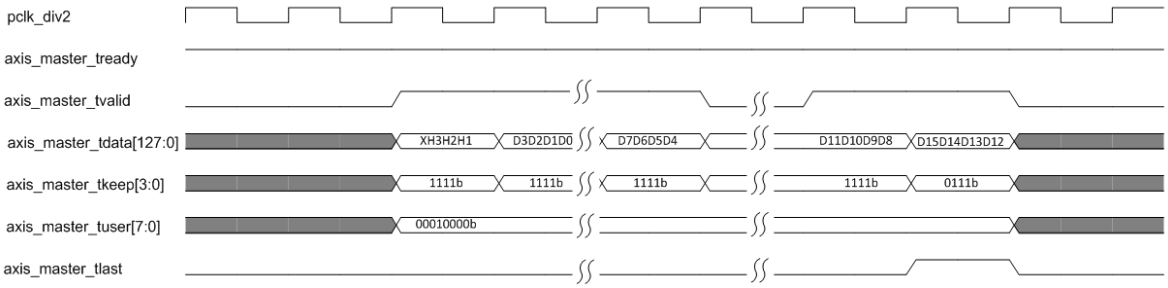

Figure 2-11 3DW Posted Operation Timing

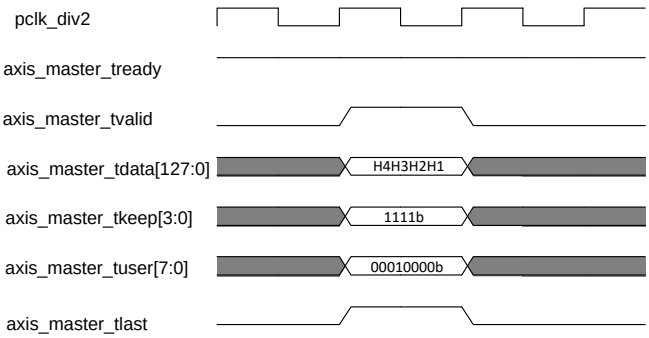

Figure 2-12 4DW Non-Posted Operation Timing

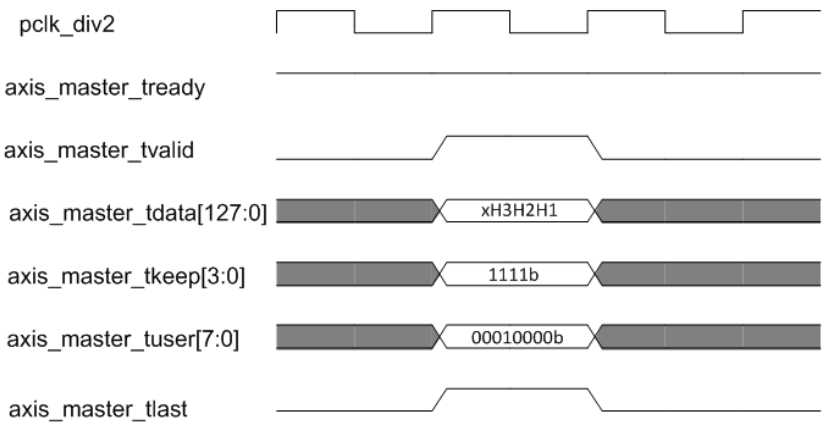

Figure 2-13 3DW Non-Posted Operation Timing

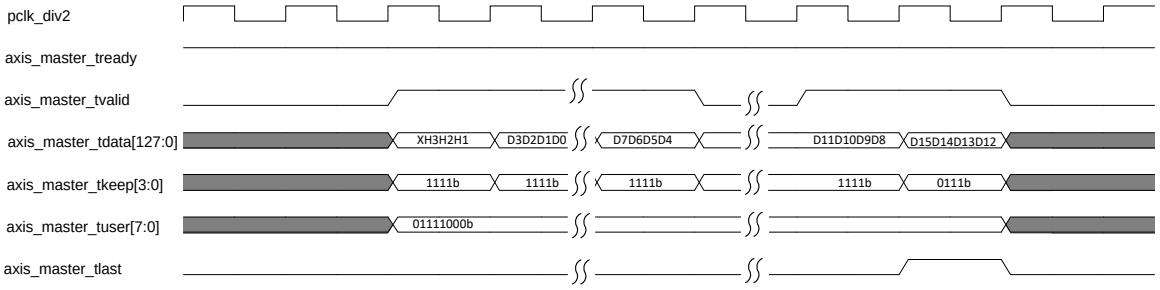

Figure 2-14 Completion Operation Timing

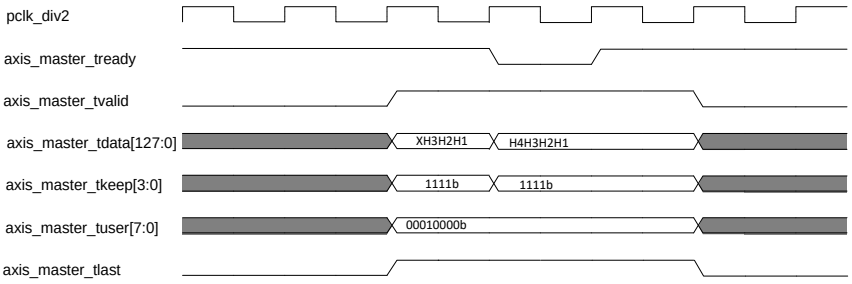

Figure 2-15 Back to Back Non-Posted Operation Timing

2.5.4.2 AXI4-Stream Slave operation timing

Once data transfer starts, axis_slave0/1/2_tvalid must remain high until the final data transfer is complete (axis_slave0/1/2_tlast goes high).

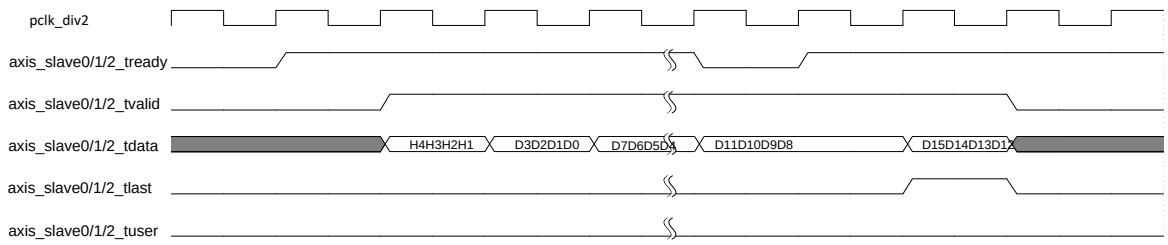

Figure 2-16 4DW Posted Operation Timing

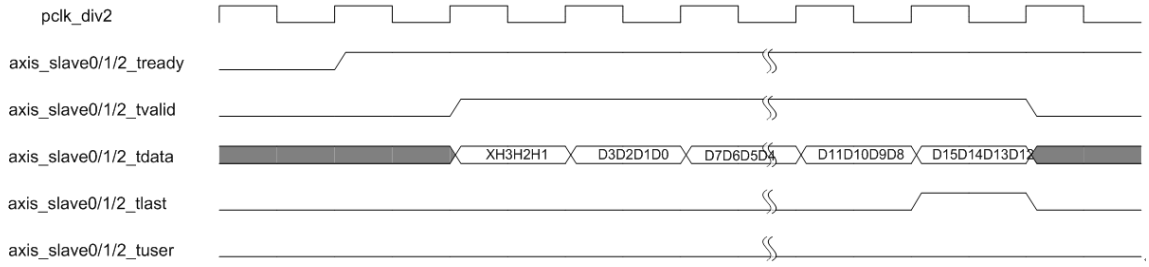

Figure 2-17 3DW Posted Operation Timing

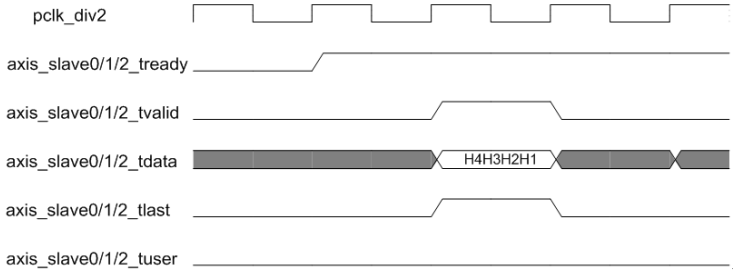

Figure 2-18 4DW Non-Posted Operation Timing

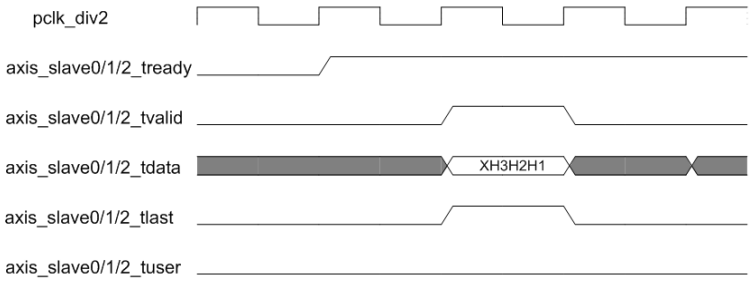

Figure 2-19 3DW Non-Posted Operation Timing

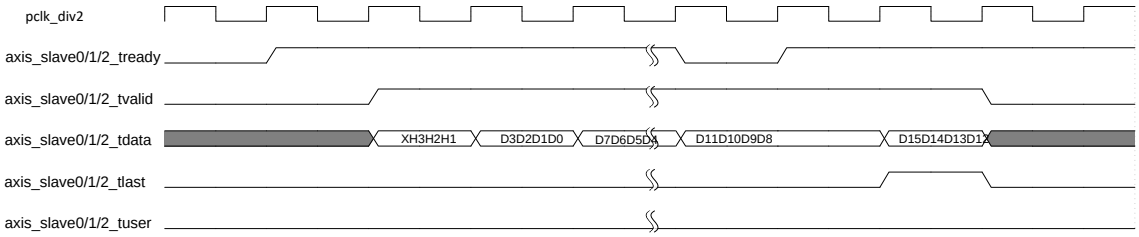

Figure 2-20 Completion Operation Timing

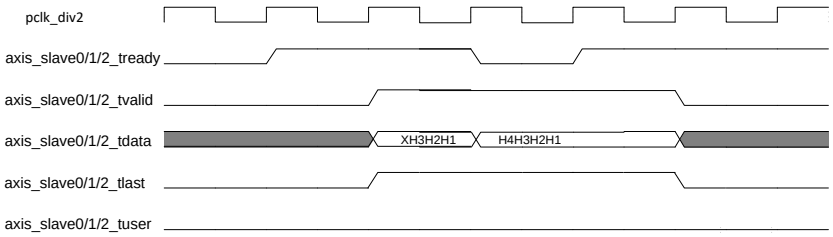

Figure 2-21 Back to Back Non-Posted Operation Timing

2.5.4.3 MSI operation timing

Prior to initiating an MSI request, ensure the MSI Capability is enabled and cfg_msi_en is high.

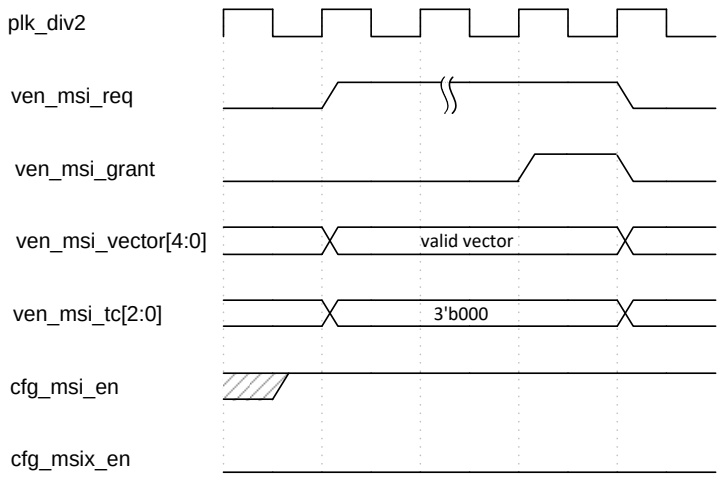

Figure 2-22 MSI Operation Timing

2.5.4.4 MSI-X operation timing

Prior to initiating an MSI-X request, ensure the MSI-X Capability is enabled and cfg_msix_en is high.

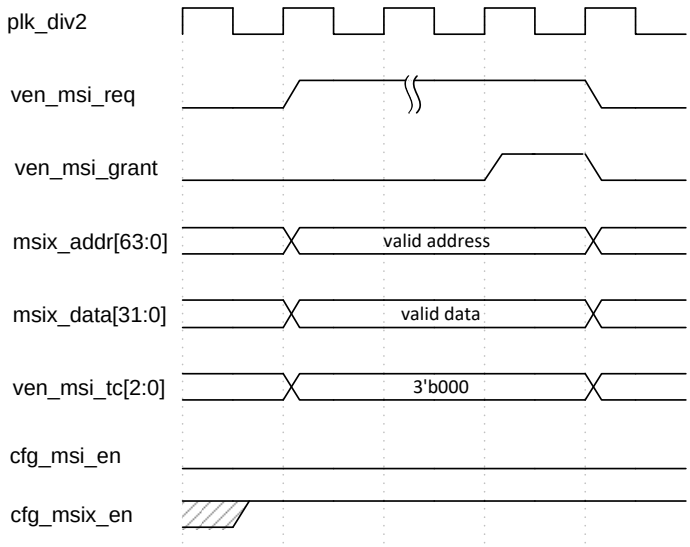

Figure 2-23 MSI-X Operation Timing

2.6 Description of the IP Register

2.6.1 Endpoint

PCI Express Endpoint and Legacy PCI Express Endpoint related registers are described as follows.

2.6.1.1 Configuration space registers

Table 2-21 PCI Express IP Upstream Configuration Space Registers

PCI Express Configuration Space				
31	16	15	0	Address
Device ID		Vendor ID		000h
Status		Command		004h
Class Code			RevID	008h
BIST	Header	Lat Timer	Cache Ln	00Ch
Base Address Register 0				010h
Base Address Register 1				014h
Base Address Register 2				018h
Base Address Register 3				01Ch
Base Address Register 4				020h

PCI Express Configuration Space				
Base Address Register 5				024h
Cardbus CIS Pointer				028h
Subsystem ID		Subsystem Vendor ID		02Ch
Expansion ROM Base Address				030h
Reserved			CapPtr	034h
Reserved				038h
Max Lat	Min Gnt	Intr Pin	Intr Line	03Ch
Reserved				040h
				044h
				048h
				04Ch
MSI Control		Next Cap Pointer	Cap ID	050h
Message Address [31:0]				054h
Message Address [63:32]				058h
Reserved		Message Data		05Ch
Mask Bits				060h
Pending Bits				064h
Reserved				068h
Reserved				06Ch
PE Cap		Next Cap Pointer	Cap ID	070h
Device Capabilities				074h
Device Status		Device Control		078h
Link Capabilities				07Ch
Link Status		Link Control		080h
Reserved				084h
				088h
				08Ch
				090h
Device Capabilities 2				094h
Device Status 2		Device Control 2		098h
Link Capabilities 2				09Ch
Link Status 2		Link Control 2		0A0h
Reserved				0A4h
				0A8h
				0ACh
Message Control		Next Pointer	Capability ID	0B0h
Table Offset			Table BIR	0B4h
PBA Offset			PBA BIR	0B8h
Reserved				…

PCI Express Configuration Space	
Advanced Error Capabilities and Control Register	118h

2.6.1.1.1 Device/Vendor ID REG

Table 2-22 Device/Vendor ID REG (Offset = 000h)

Bits	Item	Reset Values	Access Type	Description
15:0	Vendor ID	0x 16C3	R/W	Vendor ID
31:16	Device ID	0x ABCD	R/W	Device ID

2.6.1.1.2 Command REG

Table 2-23 Command REG (Offset = 004h)

Bits	Item	Reset Values	Access Type	Description
0	IO Space Enable	0	R/W	1: Receive IO-type requests 0: Does not receive IO-type requests
1	MEM Space Enable	0	R/W	1: Receive MEM-type requests 0: Does not Receive MEM-type requests
2	Bus Master Enable	0	R/W	1: Can transmit MEM/IO-type requests 0: Cannot transmit MEM/IO-type requests
9:3	Reserved	0x0	RO	Reserved
10	Interrupt Disable	0	R/W	1: Disable INTx interrupts 0: Enable INTx interrupts
15:11	Reserved	0x0	RO	Reserved

2.6.1.1.3 Status REG

Table 2-24 Status REG (Offset = 006h)

Bits	Item	Reset Values	Access Type	Description
2:0	Reserved	0	RO	Reserved
3	Interupt Status	0	RO	High indicates INTx interrupt triggered
4	Capabilities List	1	RO	Set to 1
15:5	Reserved	0x0	RO	Reserved

2.6.1.1.4 Class Code Revision ID REG

Table 2-25 Class Code Revision ID REG (Offset = 008h)

Bits	Item	Reset Values	Access Type	Description
7:0	Revision ID	0x01	R/W	Revision ID
31:8	Class Code	0x000000	R/W	Class Code

2.6.1.1.5 Header Type REG

Table 2-26 Header Type REG (Offset = 00eh)

Bits	Item	Reset Values	Access Type	Description
6:0	Header Type	0x00	RO	None
7	Multi-Function Device	0	RO	0: Only support single Function

2.6.1.1.6 BAR0 REG

Table 2-27 BAR0 REG (Offset = 010h)

Bits	Item	Reset Values	Access Type	Description
0	Memory Space Indicator	0	R/W	1: IO 0: MEM
2:1	Type	2'b10	R/W	00: Allocates 32-bit address 10: Allocate 64-bit address 11,01: Reserved
3	Prefetchable	1	R/W	Set high to access memory space through BAR
31:4	Base Address	28'h000000	RO	Base address

2.6.1.1.7 BAR1 REG

Table 2-28 BAR1 REG (Offset = 014h)

Bits	Item	Reset Values	Access Type	Description
0	Memory Space Indicator	0	R/W	1: IO 0: MEM
2:1	Type	2'b0	R/W	00: Allocates 32-bit address 10: Allocate 64-bit address 11,01: Reserved
3	Prefetchable	0	R/W	Set high to access memory space through BAR
31:4	Base Address	28'h000000	RO	Base address

2.6.1.1.8 BAR2 REG

Table 2-29 BAR2 REG (Offset = 018h)

Bits	Item	Reset Values	Access Type	Description
0	Memory Space Indicator	0	R/W	1: IO 0: MEM
2:1	Type	2'b10	R/W	00: Allocates 32-bit address 10: Allocate 64-bit address 11,01: Reserved
3	Prefetchable	1	R/W	Set high to access memory space through BAR
31:4	Base Address	28'h000000	RO	Base address

2.6.1.1.9 BAR3 REG

Table 2-30 BAR3 REG (Offset = 01ch)

Bits	Item	Reset Values	Access Type	Description
0	Memory Space Indicator	0	R/W	1: IO 0: MEM
2:1	Type	2'b00	R/W	00: Allocates 32-bit address 10: Allocate 64-bit address 11,01: Reserved
3	Prefetchable	0	R/W	Set high to access memory space through BAR
31:4	Base Address	28'h000000	RO	Base address

2.6.1.1.10 BAR4 REG

Table 2-31 BAR4 REG (Offset = 020h)

Bits	Item	Reset Values	Access Type	Description
0	Memory Space Indicator	0	R/W	1: IO 0: MEM
2:1	Type	2'b00	R/W	00: Allocates 32-bit address 10: Allocate 64-bit address 11,01: Reserved
3	Prefetchable	0	R/W	Set high to access memory space through BAR
31:4	Base Address	28'h000000	RO	Base address

2.6.1.1.11 BAR5 REG

Table 2-32 BAR5 REG (Offset = 024h)

Bits	Item	Reset Values	Access Type	Description
0	Memory Space Indicator	1	R/W	1: IO 0: MEM
2:1	Type	2'b00	R/W	00: Allocates 32-bit address 10: Allocate 64-bit address 11,01: Reserved
3	Prefetchable	0	R/W	Set high to access memory space through BAR
31:4	Base Address	28'h000000	RO	Base address

2.6.1.1.12 SUB_ID REG

Table 2-33 SUB_ID REG (Offset = 02ch)

Bits	Item	Reset Values	Access Type	Description
15:0	Subsystem Vendor ID	0x0000	R/W	Subsystem Vendor ID
31:16	Subsystem ID	0x0000	R/W	Subsystem ID

2.6.1.1.13 EXP_ROM_INIT REG

Table 2-34 EXP_ROM_INIT REG (Offset = 030h)

Bits	Item	Reset Values	Access Type	Description
0	E_ROM_enable	0	R/W	1: Expansion ROM available 0: Expansion ROM not available
10:1	Reserved	0	RO	Reserved
31:11	Base Address	0	RO	Base address

2.6.1.1.14 CAP_PTR REG

Table 2-35 CAP_PTR REG (Offset = 034h)

Bits	Item	Reset Values	Access Type	Description
7:0	CAP_POINT	0x40	RO	Capabilities Pointer

2.6.1.1.15 INTR REG

Table 2-36 INTR REG (Offset = 03ch)

Bits	Item	Reset Values	Access Type	Description
7:0	INTR_LINE	0xFF	RO	Store interrupt information
15:8	INTR_PIN	1	RO	0: Interrupt Pin not supported 1: INTA 2: INTB 3: INTC 4: INTD 5-FF: Reserved
23:16	Min Gnt	0	RO	PCIE protocol not used (set to 0)
31:24	Max Lat	0	RO	PCIE protocol not used (set to 0)

2.6.1.1.16 MSI_ CAP_List REG

Table 2-37 MSI_CAP_List REG (Offset = 050h)

Bits	Item	Reset Values	Access Type	Description
7:0	Capability ID	0x05	RO	Capability ID
15:8	Next Capability Pointer	0x70	RO	Next Capability Pointer

2.6.1.1.17 MSI_Control REG

Table 2-38 MSI_Control REG (Offset = 052h)

Bits	Item	Reset Values	Access Type	Description
0	MSI Enable	0	R/W	0: Disable MSI 1: Enable MSI
3:1	Multiple Message Capable	3'b101	R/W	Indicates how many Messages the EP supports 000b 1 001b 2 010b 4 011b 8 100b 16 101b 32 110b Reserved 111b Reserved

Bits	Item	Reset Values	Access Type	Description
6:4	Multiple Message Enable	3'b0	R/W	Software allocate a specific number of Messages to the EP based on the value of Multiple Message Cap, with the number being less than or equal to Multiple Message Capable. 000b 1 001b 2 010b 4 011b 8 100b 16 101b 32 110b Reserved 111b Reserved
7	64-bit Address Capable	1	R/W	0: Only 32-bit Address supported 1: 64-bit Address supported
8	Per-Vector Masking Capable	1	RO	0: Masking and Pending not used 1: Masking and Pending used
15:9	Reserved	0	RO	Reserved

2.6.1.1.18 MSI_CAP_REG1

Table 2-39 MSI_CAP_REG1 (Offset = 054h)

Bits	Item	Reset Values	Access Type	Description
31:0	MSI_CAP_REG1	0x0	RO	Message Address[31:0]

2.6.1.1.19 MSI_CAP_REG2

Table 2-40 MSI_CAP_REG2 (Offset = 058h)

Bits	Item	Reset Values	Access Type	Description
31:0	MSI_CAP_REG2	0x0	RO	When MSI_Control REG[7] is 0: Only 32-bit Address supported [15:0]: Message Data [31:16]: Reserved When MSI_Control REG[7] is 1: 64-bit Address supported [31:0] : Message Address[63:32]

2.6.1.1.20 MSI_CAP_REG3

Table 2-41 MSI_CAP_REG3 (Offset = 05ch)

Bits	Item	Reset Values	Access Type	Description
31:0	MSI_CAP_REG3	0x0	RO	When MSI_Control REG[7] is 0: Only 32-bit Address supported [31:0] : Mask Bits When MSI_Control REG[7] is 1: 64-bit Address supported [15:0] : Message Data [31:16]: Reserved

2.6.1.1.21 MSI_CAP_REG4

Table 2-42 MSI_CAP_REG4 (Offset = 060h)

Bits	Item	Reset Values	Access Type	Description
31:0	MSI_CAP_REG4	0x0	RO	When MSI_Control REG[7] is 0: Only 32-bit Address supported [31:0] : Pending Bits When MSI_Control REG[7] is 1: 64-bit Address supported [31:0] : Mask Bits

2.6.1.1.22 MSI_CAP_REG5

Table 2-43 MSI_CAP_REG5 (Offset = 064h)

Bits	Item	Reset Values	Access Type	Description
31:0	MSI_CAP_REG5	0x0	RO	When MSI_Control REG[7] is 0: Only 32-bit Address supported [31:0]: Reserved When MSI_Control REG[7] is 1: 64-bit Address supported [31:0] : Pending Bits

2.6.1.1.23 PCIE_CAP_List REG

Table 2-44 PCIE_CAP_List REG (Offset = 070h)

Bits	Item	Reset Values	Access Type	Description
7:0	Capability ID	0x10	RO	Capability ID
15:8	Next Capability Pointer	0xB0	RO	Next Capability Pointer

2.6.1.1.24 PCIE _CAP REG

Table 2-45 PCIE_CAP REG (Offset = 072h)

Bits	Item	Reset Values	Access Type	Description
3:0	Capability Version	02h	RO	Fixed value is 02h
7:4	Device/Port Type	0	RO	0000b : PCI Express Endpoint 0001b : Legacy PCI Express Endpoint 0100b : Root Port of PCI Express Root Complex 0101b : Upstream Port of PCI Express Switch 0110b : Downstream Port of PCI Express Switch Others: Reserved
8	Slot Implemented	0	RO	1: Connected to a Slot 0: Not Connected to a Slot
13:9	Interrupt Message Number	0	RO	Interrupt Message Number
15:14	Reserved	0	RO	Reserved

2.6.1.1.25 Device_CAP REG

Table 2-46 Device_CAP REG (Offset = 074h)

Bits	Item	Reset Values	Access Type	Description
2:0	Max_Payload_Size Supported	3'b011	RO	000b: 128 Byte 001b: 256 Byte 010b: 512 Byte 011b: 1024 Byte Others: Reserved
4:3	Phantom Functions Supported	2'b10	RO	00b: No Phantom Functions used 01b: The lowest bit of the Function Number is used for Phantom Functions 10b: The lowest two bits of the Function Number are used for Phantom Functions 11b: Function Number completely used for Phantom Functions
5	Extended Tag Field Supported	1	RO	0b: 5-bit Tag field supported 1b: 8-bit Tag field supported Others: Reserved
8:6	Endpoint L0s Acceptable Latency	3'b011	RO	000b: Maximum of 64 ns 001b: Maximum of 128 ns 010b: Maximum of 256 ns 011b: Maximum of 512 ns 100b: Maximum of 1 μs 101b: Maximum of 2 μs 110b: Maximum of 4 μs 111b: No Limit

Bits	Item	Reset Values	Access Type	Description
11:9	Endpoint L1 Acceptable Latency	3'b111	RO	000b: Maximum of 1 μs 001b: Maximum of 2 μs 010b: Maximum of 4 μs 011b: Maximum of 8 μs 100b: Maximum of 16 μs 101b: Maximum of 32 μs 110b: Maximum of 64 μs 111b: No Limit
31:12	Reserved	0x1	RO	Reserved

2.6.1.1.26 Device_ Control REG

Table 2-47 Device_Control REG (Offset = 078h)

Bits	Item	Reset Values	Access Type	Description
0	Correctable Error Reporting Enable	0	RO	Control transmitting ERR_COR Messages
1	Non-Fatal Error Reporting Enable	0	RO	Control transmitting ERR_NONFATAL Messages
2	Fatal Error Reporting Enable	0	RO	Control transmitting ERR_FATAL Messages
3	Unsupported Request Reporting Enable	0	RO	Signaling of Unsupported Requests
4	Enable Relaxed Ordering	1	RO	1: Relaxed Ordering supported 0: Relaxed Ordering not supported
7:5	Max_Payload_Size	3'b0	RO	000b: 128 Byte 001b: 256 Byte 010b: 512 Byte 011b: 1024Byte 100b: 2048 Byte 101b: 4096 Byte 110b: Reserved 111b: Reserved
8	Extended Tag Field Enable	1	RO	1: 8bit Tag can be used 0: 8bit Tag cannot be used
9	Phantom Functions Enable	0	RO	1: Phantom Functions can be used 0: Phantom Functions cannot be used
10	AUX Power PM Enable	0	RO	1: AUX Power allowed 0: AUX Power not allowed
11	Enable No Snoop	0	RO	1: No Snoop allowed 0: No Snoop not allowed
14:12	Max_Read_Request_ Size	3'b10	RO	000b: 128 Byte 001b: 256 Byte 010b: 512 Byte 011b: 1024 Byte 100b: 2048 Byte 101b: 4096 Byte 110b: Reserved 111b: Reserved

Bits	Item	Reset Values	Access Type	Description
15	Bridge Enable	0	RO	1: Response to CRS allowed 0: Response to CRS not allowed

2.6.1.1.27 Device_ Status

Table 2-48 Device_Status REG (Offset = 07ah)

Bits	Item	Reset Values	Access Type	Description
0	Correctable Error Detected	0	RO	1 indicates Correctable Errors detected
1	Non-Fatal Error Detected	0	RO	1 indicates Non-Fatal Error detected
2	Fatal Error Detected	0	RO	1 indicates Fatal Error detected
3	UR Detected	0	RO	1 indicates Unsupported Request detected
4	AUX Power Detected	1	RO	1 indicates AUX Power required
5	Transactions Pending	0	RO	1 indicates no CPL received corresponding to the transmitted NP
15:6	Reserved	0x0	RO	Reserved

2.6.1.1.28 Link_CAP REG

Table 2-49 Link_CAP REG (Offset = 07ch)

Bits	Item	Reset Values	Access Type	Description
3:0	Supported Link Speeds	4'b10	R/W	0001b: 2.5 GT/s 0010b: 5.0 GT/s and 2.5 GT/s Others: Reserved
9:4	Maximum Link Width	6'b100	R/W	000000b: Reserved 000001b: x1 000010b: x2 000100b: x4 Others: Reserved
11:10	ASPM Support	2'b10	RO	00b: Reserved 01b: L0s 10b: Reserved 11b: L0s and L1
14:12	L0s Exit Latency	3'b111	RO	000b: Less than 64 ns 001b: 64 ns to less than 128 ns 010b: 128 ns to less than 256 ns 011b: 256 ns to less than 512 ns 100b: 512 ns to less than 1 μs 101b: 1 μs to less than 2 μs 110b: 2 μs-4 μs 111b: More than 4 μs

Bits	Item	Reset Values	Access Type	Description
17:15	L1 Exit Latency	3'b111	RO	000b: Less than 1μs 001b: 1 μs to less than 2 μs 010b: 2 μs to less than 4 μs 011b: 4 μs to less than 8 μs 100b: 8 μs to less than 16 μs 101b: 16 μs to less than 32 μs 110b: 32 μs-64 μs 111b: More than 64 μs
31:24	Port Number	0	RO	Port Number

2.6.1.1.29 Link_Control REG

Table 2-50 Link_Control REG (Offset = 080h)

Bits	Item	Reset Values	Access Type	Description
1:0	ASPM Control	0	RO	00b: Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled
2	Reserved	0	RO	Reserved
3	RCB	0	RO	0b: 64 Byte 1b: 128 Byte
4	Link Disable	0	RO	Reserved on Endpoints
5	Retrain Link	0	RO	Reserved for Endpoints
6	Common Clock Configuration	0	RO	1: Common Reference Clock 0: Asynchronous Reference Clock
7	Extended Synch	0	RO	When Set, this bit forces the transmission of additional Ordered Sets when exiting the L0s state and when in the Recovery state
8	Enable Clock Power Management	0	RO	0b: Clock power management is disabled and the device must hold CLKREQ# signal low 1b: When this bit is Set, the device is permitted to use CLKREQ# signal to power manage Link clock according to the protocol defined in the appropriate form factor specification
9	Hardware Autonomous Width Disable	0	RO	When Set, this bit disables hardware from changing the Link width
10	Link Bandwidth Management Interrupt Enable	0	RO	When Set, this bit disables hardware from changing the Link width
11	Link Autonomous Bandwidth Interrupt Enable	0	RO	When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set
15:12	Reserved	0	RO	Reserved

2.6.1.1.30 Link_Status REG

Table 2-51 Link_Status REG (Offset = 082h)

Bits	Item	Reset Values	Access Type	Description
3:0	Current Link Speed	4'b1	RO	0001b: 2.5GT/s 0010b: 5.0GT/s Others: Reserved
9:4	Link Width	6'b1	RO	000000b: Reserved 000001b: x1 000010b: x2 000100b: x4 001000b: x8 001100b: x12 010000b: x16 100000b: x32
10	Undefined	0	RO	Undefined
11	Link Traning	0	RO	1: LTSSM in Cfg/Recovery status 0: LTSSM exits Cfg/Recovery status
12	Slot Clock Cfg	1	RO	1: Use the platform-provided reference clock 0: Use an independent clock.
13	DLL Link Active	0	RO	1: DLCMSM in DL_Active status. 0: DLCMSM not in DL_Active status
14	Link Bandwidth Management Status	0	RO	This bit is reserved for Endpoint
15	Link Autonomous Bandwidth Status	0	RO	1 indicates automatic adjustment of rate or link width.

2.6.1.1.31 Device_CAP2 REG

Table 2-52 Device_CAP2 REG (Offset = 094h)

Bits	Item	Reset Values	Access Type	Description
3:0	Completion Timeout Ranges Supported	4'hf	R/W	0000b: Completion Timeout programming not supported – the Function must implement a timeout value in the range 50 μs to 50 ms 0001b: Range A 0010b: Range B 0011b: Ranges A and B 0110b: Ranges B and C 0111b: Ranges A, B, and C 1110b: Ranges B, C and D 1111b: Ranges A, B, C, and D
4	Completion Timeout Disable Supported	1	R/W	When set to 1, the CPL timeout mechanism is not used
5	Reserved	0x0	RO	Reserved
6	AtomicOp Routing Supported	0x0	RO	1: AtomicOp Routing supported 0: AtomicOp Routing not supported
7	32-bit AtomicOp Completer Supported	0x1	RO	1: 32-bit AtomicOp Completer supported 0: 32-bit AtomicOp Completer not supported

Bits	Item	Reset Values	Access Type	Description
8	64-bit AtomicOp Completer Supported	0x1	RO	1: 64-bit AtomicOp Completer supported 0: 64-bit AtomicOp Completer not supported
9	128-bit CAS Completer Supported	0x1	RO	1: 128-bit CAS Completer supported 0: 128-bit CAS Completer not supported
31:10	Reserved	0x4	RO	Reserved

2.6.1.1.32 Device_Control2 REG

Table 2-53 Device_Control2 REG (Offset = 098h)

Bits	Item	Reset Values	Access Type	Description
3:0	CPL Timeout Value	4'h0	RO	0000b: 50 μs to 50 ms 0001b: 50 μs to 100 μs 0010b: 1 ms to 10 ms 0101b: 16 ms to 55 ms 0110b: 65 ms to 210 ms 1001b: 260 ms to 900 ms 1010b: 1 s to 3.5 s 1101b: 4 s to 13 s 1110b: 17 s to 64
4	CPL Timeout Disable	0	RO	When set to 1, the CPL Timeout mechanism is not used
5	ARI Forwarding Enable	0	RO	When set to 1, Enable ARI Forwarding
6	AtomicOp Requester Enable	0	RO	When set to 1, allows transmitting AtomicOp requests.
8	IDO Request Enable	0	RO	When set to 1, allows IDO Request
9	IDO Completion Enable	0	RO	When set to 1, allows IDO Completion
10	LTR Mechanism Enable	0	RO	When set to 1, allows the LTR mechanism
14: 11	Reserved	0x0	RO	Reserved
15	End-End TLP Prefix Blocking	0	RO	0: Forwarding Enabled 1: Forwarding Blocked

2.6.1.1.33 Device_Status2 REG

Table 2-54 Device_Status2 REG (Offset = 09ah)

Bits	Item	Reset Values	Access Type	Description
15:0	Reserved	0	RO	Reserved

2.6.1.1.34 Link_CAP2 REG

Table 2-55 Link_CAP2 REG (Offset = 09ch)

Bits	Item	Reset Values	Access Type	Description
31:0	Reserved	0x6	RO	Reserved

2.6.1.1.35 Link_Control2 REG

Table 2-56 Link_Control2 REG (Offset = 0a0h)

Bits	Item	Reset Values	Access Type	Description
3:0	Target Link Speed	0x2	R/W	0001b: 2.5GT/s 0010b: 5GT/s Others: Reserved
4	Enter Compliance	0	RO	When the value is 1, it indicates the device is forced into Compliance mode
5	Hw_Auto Speed Disable	0	RO	When the value is 1, it means the PCIe device cannot change the existing negotiated PCIe link width unless to correct errors in the PCIe lanes
6	Selectable De-emphasis	0	RO	1b: -3.5 dB 0b: -6 dB
10	Enter Modified Compliance	0	RO	When the value is 1, transmit Modified Compliance Pattern while LTSSM state machine is in Polling
11	Compaliance SOS	0	RO	When the value is 1, LTSSM transmits SKP Ordered Sets
12	Compliance De-emphasis	0	RO	1b: -3.5 dB 0b: -6 dB

2.6.1.1.36 Link_Status2 REG

Table 2-57 Link_Status2 REG (Offset = 0a2h)

Bits	Item	Reset Values	Access Type	Description
0	De-emphasis Level	1	RO	In the case of 5GT/s 1: -3.5dB 0: -6dB Remains 0 at 2.5GT/s
15:1	Reserved	0x0	RO	Reserved

2.6.1.1.37 MSI-X _CAP_List REG

Table 2-58 MSI-X_CAP_List REG (Offset = 0b0h)

Bits	Item	Reset Values	Access Type	Description
7:0	Capability ID	0x11	RO	Capability ID
15:8	Next Pointer	0x0	RO	Next Capability Pointer

2.6.1.1.38 Message_Control REG

Table 2-59 Message_Control REG (Offset = 0b0h)

Bits	Item	Reset Values	Access Type	Description
10:0	Table Size	0x80	RO	System software reads this field to determine the MSI-X Table Size N, which is encoded as N-1. For example, a returned value of "00000000011" indicates a table size of 4
13:11	Reserved	0x0	RO	Reserved
14	Function Mask	0x0	RO	1: All of the vectors associated with the function are masked, regardless of their per-vector Mask bit states 0: Each vector's Mask bit determines whether the vector is masked or not
15	MSI-X Enable	0x0	RO	0: Disable MSI-X 1: Enable MSI-X

2.6.1.1.39 MSI-X _Table_Offset REG

Table 2-60 MSI-X_Table_Offset REG (Offset = 0b4h)

Bits	Item	Reset Values	Access Type	Description
2:0	Table BIR	0x2	RO	Indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X Table into Memory Space BIR Value Base Address register 0 10h 1 14h 2 18h 3 1Ch 4 20h 5 24h 6 Reserved 7 Reserved
31:3	Table Offset	0x0	RO	Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X Table. The lower 3 Table BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset

2.6.1.1.40 MSI-X _PBA_Offset REG

Table 2-61 MSI-X_PBA_Offset REG (Offset = 0b8h)

Bits	Item	Reset Values	Access Type	Description
2:0	PBA BIR	0x2	RO	Indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X PBA into Memory Space The PBA BIR value definitions are identical to those for the MSI-X Table BIR
31:3	PBA Offset	0x800	RO	Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X PBA. The lower 3 PBA BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset.

2.6.1.1.41 MSI-X _PBA_Offset REG

Table 2-62 MSI-X_PBA_Offset REG (Offset = 0b8h)

Bits	Item	Reset Values	Access Type	Description
4: 0	Reserved	0x0	RO	Reserved
5	ECRC Generation Capable	0x0	RO	1: Device is capable of generating ECRC 0: Device is not capable of generating ECRC
6	ECRC Generation Enable	0x0	RO	1: Enable ECRC Generation 0: Disable ECRC Generation
7	ECRC Check Capable	0x0	RO	1: Device is capable of checking ECRC 0: Device is not capable of checking ECRC
8	ECRC Check Enable	0x0	RO	1: Enable ECRC Check 0: Disable ECRC Check
31:9	Reserved	0x0	RO	Reserved

2.6.1.2 Shadow register

Table 2-63 Shadow Register

PCI Express Shadow Register				
31	16	15	0	Address
BAR0_MASK_REG				011h
BAR1_MASK_REG				015h
BAR2_MASK_REG				019h
BAR3_MASK_REG				01Dh
BAR4_MASK_REG				021h
BAR5_MASK_REG				025h
EXP_ROM_BAR_MASK_REG				031h

2.6.1.2.1 BAR0_MASK_REG

Table 2-64 BAR0_MASK_REG (Offset = 011h)

Bits	Item	Reset Values	Access Type	Description
0	BAR0_ENABLED	0x1	WO	BAR0 Enable
31:1	BAR0_MASK	0x7fff_ffff	WO	BAR0 MASK

2.6.1.2.2 BAR1_MASK_REG

Table 2-65 BAR1_MASK_REG (Offset = 015h)

Bits	Item	Reset Values	Access Type	Description
0	BAR1_ENABLED	0x1	WO	BAR1 Enable
31:1	BAR1_MASK	0x3f	WO	BAR1 MASK

2.6.1.2.3 BAR2_MASK_REG

Table 2-66 BAR2_MASK_REG (Offset = 019h)

Bits	Item	Reset Values	Access Type	Description
0	BAR2_ENABLED	0x1	WO	BAR2 Enable
31:1	BAR2_MASK	0x7fff_ffff	WO	BAR2 MASK

2.6.1.2.4 BAR3_MASK_REG

Table 2-67 BAR3_MASK_REG (Offset = 01dh)

Bits	Item	Reset Values	Access Type	Description
0	BAR3_ENABLED	0x1	WO	BAR3 Enable
31:1	BAR3_MASK	0x3f	WO	BAR3 MASK

2.6.1.2.5 BAR4_MASK_REG

Table 2-68 BAR4_MASK_REG (Offset = 021h)

Bits	Item	Reset Values	Access Type	Description
0	BAR4_ENABLED	0x1	WO	BAR4 Enable
31:1	BAR4_MASK	0x3fff_ffff	WO	BAR4 MASK

2.6.1.2.6 BAR5_MASK_REG

Table 2-69 BAR0_MASK_REG (Offset = 025h)

Bits	Item	Reset Values	Access Type	Description
0	BAR5_ENABLED	0x1	WO	BAR5 Enable
31:1	BAR5_MASK	0x7f	WO	BAR5 MASK

2.6.1.2.7 EXP_ROM_BAR_MASK

Table 2-70 EXP_ROM_BAR (Offset = 031h)

Bits	Item	Reset Values	Access Type	Description
0	ROM_BAR_ENABLED	0x1	WO	Expansion ROM Bar Mask Register Enabled
31:1	ROM_MASK	0x7fff_ffff	WO	Expansion ROM Mask

2.6.1.3 Port Logic register

Table 2-71 Port Logic Register

PCI Express Port Logic Registers				
31	16	15	0	Address
PORT_LINK_CTRL_OFF				710h
GEN2_CTRL_OFF				80ch

2.6.1.3.1 PORT_LINK_CTRL_OFF

Table 2-72 PORT_LINK_CTRL_OFF (Offset = 710h)

Bits	Item	Reset Values	Access Type	Description
0	Reserved	0x0	RO	Reserved
1	SCRAMBLE_DISABLE	0x0	R/W	Scramble Disable
15:2	Reserved	0x0	RO	Reserved
21:16	LINK_CAPABLE	0x7	R/W	0x1 (X1): x1 0x3 (X2) : x2 0x7 (X4) : x4
31:22	Reserved	0x0	RO	Reserved

2.6.1.3.2 GEN2_CTRL_OFF

Table 2-73 GEN2_CTRL_OFF (Offset = 80ch)

Bits	Item	Reset Values	Access Type	Description
7:0	Reserved	0x0	RO	Reserved
12:8	NUM_OF_LANES	0x4	R/W	0x1: 1 lane 0x2: 2 lanes 0x3: 3 lanes 0x4: 4 lanes
15:13	Reserved	0x0	RO	Reserved
16	AUTO_LANE_FLIP_CTRL_EN	0x1	R/W	Enable Auto Flipping of the Lanes
31:17	Reserved	0x0	RO	Reserved

2.6.2 Root Complex

PCI Express Root Complex related configuration space registers are described as follows.

Table 2-74 PCI Express IP Downstream Configuration Space Registers

PCI Express Configuration Space				
31	16	15	0	Address
Device ID		Vendor ID		000h
Status		Command		004h
Class Code			RevID	008h
BIST	Header	Lat Timer	Cache Ln	00Ch
Base Address Register 0				010h
Base Address Register 1				014h
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	018h
Secondary Status		I/O Limit	I/O Base	01Ch
Memory Limit		Memory Base		020h
Prefetchable Memory Limit		Prefetchable Memory Base		024h
Prefetchable Base Upper 32 Bits				028h
Prefetchable Limit Upper 32 Bits				02Ch
I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits		030h
Reserved			CapPtr	034h
Expansion ROM Base Address				038h
Bridge Control		Intr Pin	Intr Line	03Ch
Reserved				040h
				044h
				048h
				04Ch

PCI Express Configuration Space			
MSI Control	Next Cap Pointer	Cap ID	050h
Message Address [31:0]			054h
Message Address [63:32]			058h
Reserved	Message Data		05Ch
Mask Bits			060h
Pending Bits			064h
Reserved			068h
Reserved			06Ch
PE Cap	Next Cap Pointer	Cap ID	070h
Device Capabilities			074h
Device Status	Device Control		078h
Link Capabilities			07Ch
Link Status	Link Control		080h
Slot Capabilities			084h
Slot Status	Slot Control		088h
Root Capabilities	Root Control		08Ch
Root Status			090h
Device Capabilities 2			094h
Device Status 2	Device Control 2		098h
Link Capabilities 2			09Ch
Link Status 2	Link Control 2		0A0h
Reserved			0A4h
			0A8h
			0ACh
Message Control	Next Pointer	Capability ID	0B0h
Table Offset		Table BIR	0B4h
PBA Offset		PBA BIR	0B8h
Reserved			…
Advanced Error Capabilities and Control Register			118h

2.6.2.1 Root Control REG

Table 2-75 Root Control REG (Offset = 08ch)

Bits	Item	Reset Values	Access Type	Description
3:0	Reserved	02h	RO	Reserved
4	CRS Software Visibility Enable	0	RO	1: enables the Root Port to return Configuration Request Retry Status (CRS) Completion Status to software

Bits	Item	Reset Values	Access Type	Description
15:5	Reserved	0	RO	Reserved

2.6.2.2 Root Capabilities REG

Table 2-76 Root Capabilities REG (Offset = 08eh)

Bits	Item	Reset Values	Access Type	Description
0	CRS Software Visibility	0	RO	1: indicates that the Root Port is capable of returning Configuration Request Retry Status (CRS) Completion Status to software
15:1	Reserved	0	RO	Reserved

2.7 Typical Applications

For typical applications of the PCIe IP, please refer to "2.4 Example Design".

2.8 Descriptions and Considerations

2.8.1 Operating Modes

2.8.1.1 PCI Express Endpoint and Legacy PCI Express Endpoint mode

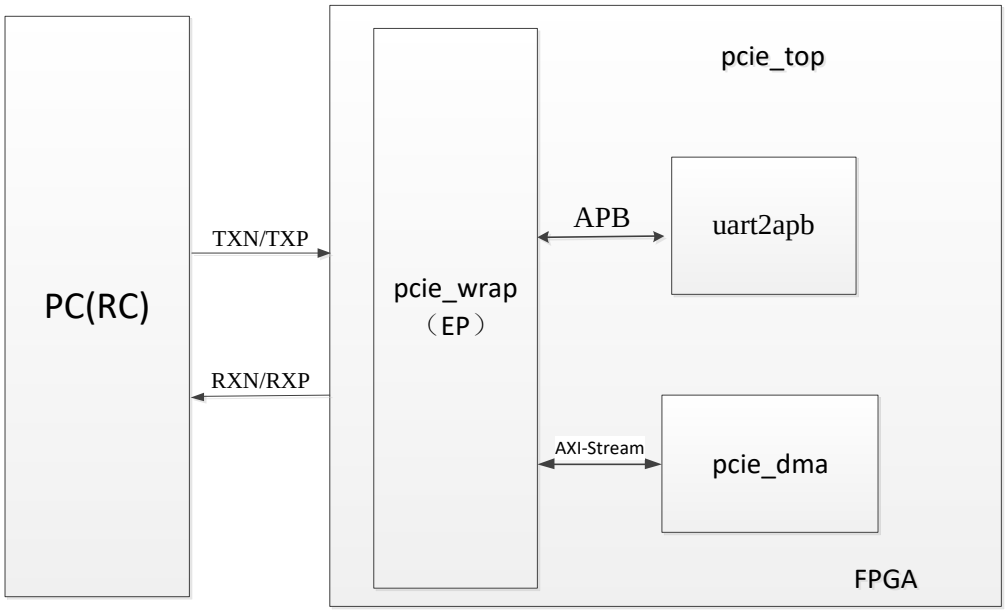

Figure 2-24 PCI Express Endpoint Mode Diagram

2.8.1.2 Root Port of PCI Express Root Complex mode

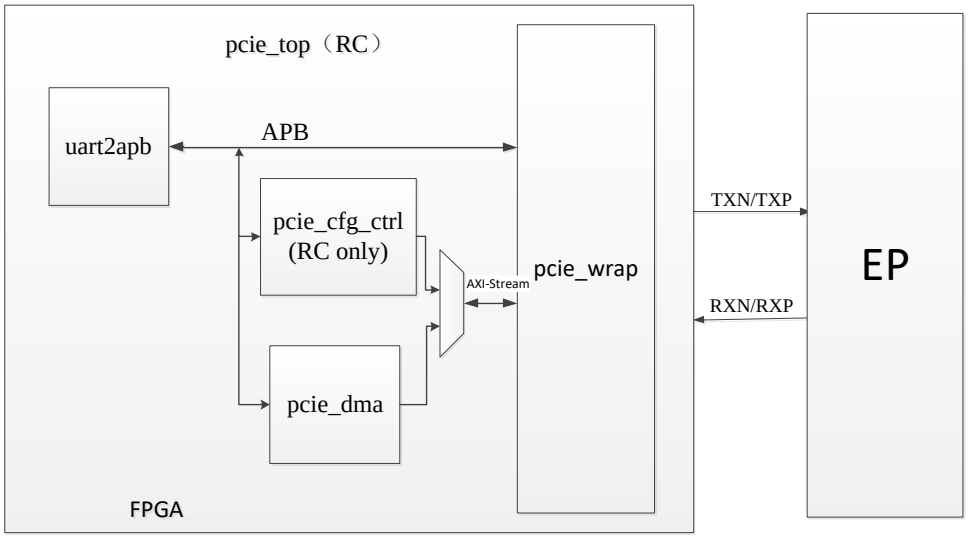

Figure 2-25 Root Port of PCI Express Root Complex Mode Diagram

2.8.2 BAR Size Limitations

Due to address width limitations, the BAR Size is limited as follows:

- The total size of 32-bit Bars cannot exceed 4GB;
- The total size of 64-bit Bars cannot exceed 16EB;
- The combined total of 32-bit and 64-bit Bars cannot exceed 16EB.

2.8.3 MSI-X Limitations

When configuring MSI-X, since both Table Offset and PBA Offset are 29 bits, the configuration value cannot exceed 0x1FFF_FFFF.

2.8.4 Lane Reversal Usage Instructions

It is not recommended to use Lane Reversal with X1 and X2; if necessary, consult FAE/AE.

2.8.5 PCIe Recommended and Supported Connection Methods

PCIe IP defaults to the recommended connection method.

Table 2-77 Recommended Connection Methods

PCIe Lane	**X1**	**X2**	**X4**
Lane0	Q3 LANE0	Q3 LANE0	Q3 LANE0
Lane1	-	Q3 LANE1	Q3 LANE1
Lane2	-	-	Q3 LANE2
Lane3	-	-	Q3 LANE3

Note: "-" indicates that there is no description for the item.

Table 2-78 Supported Connection Methods

PCIE Lane	**X1**	**X2**	**X2**	**X2**	**X2**	**X4**	**X4**
Lane0	Q3 Anylane	Q3 LANE0	Q3 LANE1	Q3 LANE2	Q3 LANE3	Q3 LANE0	Q3 LANE3
Lane1	-	Q3 LANE1	Q3 LANE0	Q3 LANE3	Q3 LANE2	Q3 LANE1	Q3 LANE2
Lane2	-	-	-	-	-	Q3 LANE2	Q3 LANE1
Lane3	-	-	-	-	-	Q3 LANE3	Q3 LANE0

Note: "-" indicates that there is no description for the item.

2.8.6 AXI-Stream Master Interface 3DW Usage Instructions

The AXI-Stream Master interface needs to determine the TLP format based on the FMT field in the TLP header.

Table 2-79 Meaning of FMT[1:0] Field

FMT[1:0]	**Corresponding TLP format**
000b	3 DW header, no data
001b	4 DW header, no data
010b	3 DW header, with data
011b	4 DW header, with data

2.8.7 Resizable BAR Usage Instructions

The IP supports manually modifying parameters to implement the Resizable BAR function. For parameter description, please refer to Table 2-80, with the following points to note:

- BAR_RESIZABLE and BAR_MASK_WRITABLE are exclusive. Both parameters need to be XORed to all 1;

- The IP supports up to 3 Resizable BARs;
- Apart from BAR_RESIZABLE and BAR_MASK_WRITABLE parameters, other parameters are consistent with the protocol. Detailed explanations are based on the protocol. If you have any questions, please contact FAE/AE.

Table 2-80 Resizable BAR Parameter Descriptions

Parameter	**Description**
BAR_RESIZABLE	6 bits correspond to 6 BARs, each bit meaning: 0: Resizable BAR function not enabled 1: Resizable BAR function enabled
BAR_MASK_WRITABLE	6 bits correspond to 6 BARs, each bit meaning: 0: Resizable BAR function enabled 1: Resizable BAR function not enabled
NUM_OF_RBARS	Number of Resizable BARs (up to 3 supported)
BAR_INDEX_0	Resizable BAR0 Index
BAR_INDEX_1	Resizable BAR1 Index
BAR_INDEX_2	Resizable BAR2 Index
RESBAR_BAR0_MAX_SUPP_SIZE	Maximum supported size for Resizable BAR0
RESBAR_BAR0_INIT_SIZE	Resizable BAR0 initial size
RESBAR_BAR1_MAX_SUPP_SIZE	Maximum supported size for Resizable BAR1
RESBAR_BAR1_INIT_SIZE	Resizable BAR1 initial size
RESBAR_BAR2_MAX_SUPP_SIZE	Maximum supported size for Resizable BAR2
RESBAR_BAR2_INIT_SIZE	Resizable BAR2 initial size
AER_CAP_NEXT_OFFSET	AER Capability next function offset 12'h0: Resizable BAR function not enabled 12'h2E4: Resizable BAR function enabled

2.8.8 Max_Read_Request_Size Limitations

The maximum value for Max_Read_Request_Size is 011b, which is 1024Bytes.

2.8.9 Correspondence between AXI-Stream Interface and PCIe TLP

2.8.9.1 Description of Byte Positions in TLP

Table 2-81 TLP Byte Position Description

Packet	**TLP**			
Header0	pcie_hdr_byte0	pcie_hdr_byte1	pcie_hdr_byte2	pcie_hdr_byte3
Header1	pcie_hdr_byte4	pcie_hdr_byte5	pcie_hdr_byte6	pcie_hdr_byte7
Header2	pcie_hdr_byte8	pcie_hdr_byte9	pcie_hdr_byte10	pcie_hdr_byte11
Header3	pcie_hdr_byte12	pcie_hdr_byte13	pcie_hdr_byte14	pcie_hdr_byte15
Data0	pcie_data_byte0	pcie_data_byte1	pcie_data_byte2	pcie_data_byte3

Packet	TLP			
Data1	pcie_data_byte4	pcie_data_byte5	pcie_data_byte6	pcie_data_byte7
Data2	pcie_data_byte8	pcie_data_byte9	pcie_data_byte10	pcie_data_byte11
…	…	…	…	…
Datan	pcie_data_byte <4n>	pcie_data_byte <4n+1>	pcie_data_byte <4n+2>	pcie_data_byte <4n+3>

2.8.9.2 Correspondence between AXI-Stream and 4DW Header TLP

Table 2-82 Correspondence Between AXI-Stream and 4DW Header TLP

AXI-Stream width	[127:96]	[95:64]	[63:32]	[31:0]
TLP	H3	H2	H1	H0
	D3	D2	D1	D0
	…	…	…	…
	Dn	D<n-1>	D<n-2>	D<n-3>

2.8.9.3 Correspondence between AXI-Stream and 3DW Header TLP

Table 2-83 Correspondence Between AXI-Stream and 3DW Header TLP

AXI-Stream width	[127:96]	[95:64]	[63:32]	[31:0]
TLP	X	H2	H1	H0
	D3	D2	D1	D0
	…	…	…	…
	Dn	D<n-1>	D<n-2>	D<n-3>

2.9 IP Debugging Methods

By utilising DebugCore to capture signals related to smlh_ltssm_state, the working status of the PCIe IP link can be monitored. Different control commands are initiated through the serial port, and execute DebugCore to capture the Example Design's APB Interface and AXI-Stream Interface to verify the normal operation of the PCIe IP. For the list of signals, please refer to Table 2-20.

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