Compa Family CPLDs Datasheet

(DS03001, V1.6)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.6	09.10.2023	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
CPLD	Complex Programmable Logic Device
CLM	Configurable Logic Module
DRM	Dedicated RAM Module
IDDR	Input Double Data Rate
ODDR	Output Double Data Rate
APB	Advanced Peripheral Bus
POR	Power-On Reset
ESD	Electro-Static Discharge
CRAM	Configurable RAM
NW	Normal Write
TW	Transparent Write
RBW	Read Before Write

Related Documentation

The following documentation is related to this manual:

1. ***UG030001_Compa Family CPLDs Configurable Logic Module (CLM) User Guide***
2. ***UG030002_Compa Family CPLDs Dedicated RAM Module (DRM) User Guide***
3. ***UG030003_Compa Family CPLDs Clock Resources (Clock&PLL) User Guide***
4. ***UG030004_Compa Family CPLDs Configuration User Guide***
5. ***UG030005_Compa Family CPLDs Input/Output Interface (IO) User Guide***
6. ***UG030006_Compa Family CPLDs Embedded Flash (EFlash) User Guide***
7. ***UG030007_Compa Family CPLDs Embedded Hard Core User Guide***
8. ***UG030008_Compa Family GTP User Guide"***
9. ***UG030009_Compa Family PCB Design User Guide***

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Chapter 1 Introduction

Compa device family is a low-cost and high-density IO family which is designed on a 55nm non-volatile process. The Compa devices utilize advanced package technology and offer instant-on after power-up capabilities. The Compa devices have the equivalent LUT4 densities ranging from 1300 to 9900, dedicated storage modules (DRM), a variety of on-chip clock resources, multi-functional I/O resources, extensive routing resources, and integrated hard cores such as SPI, I^2C, and timers/counters. The Compa devices also supports various configuration modes, remote upgrade and dual boot, while offering functions such as UID (Unique Identification) to secure user's designs.

The Compa devices are available in three types G (general purpose), L (low power), and D (Master Self Configuration Dual Boot) with two speed grades: -5 and -6, with -6 being the fastest grade. G and D type devices support an external supply voltage V_{CC} of 2.5V or 3.3V, through an internal LDO circuit to generate the core voltage VCC_{CORE} of 1.2 V; L type devices only support a V_{CC} of 1.2V, with VCC_{CORE} being the same as V_{CC}. Each I/O Bank of the CPLD device is powered by its corresponding V_{CCIO} independently, supporting 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.

1.1 Features

➢ **Flexible Architecture**

- 1300-9900 equivalent LUT4s
- Up to 384 user I/Os

➢ **Multi-functional I/O**

- Various types of I/O interfaces supported
  - LVCMOS33/LVCMOS25 /LVCMOS18/LVCMOS15 / LVCMOS12
  - LVTTL33
  - PCI33
  - LVDS/MLVDS/LVPECL33 /BLVDS25
  - MIPI
- Optional on-chip differential termination 100 Ω
- Programmable slew rate
- Programmable pull-up or pull-down
- Includes input, output, and tri-state registers
- IDDR (1:2) and ODDR (2:1) supported
- Includes I/O input and output delay units

➢ **Dedicated RAM Module**

- A single DRM provides 9Kbits of storage
- Various working modes supported, including Dual-Port (DP) RAM, Simple Dual-Port (SDP) RAM, Single-Port (SP) RAM or ROM mode, as well as FIFO mode
- Dual-port RAM and simple dual-port RAM support different bit widths for both ports
- Byte Enable supported

➢ **High-Speed Data Transfer Supported**

- OSERDES supports 4:1, 7:1, 8:1
- ISERDES supports 1:4, 1:7, 1:8

➢ **Clock Resources**

- Eight global clocks and eight global signals, supporting up to 400MHz
- Four I/O clocks, supporting up to 600MHz
- Up to 2 PLLs supported

➢ **Various Configuration Modes and Applications**

- JTAG configuration supported
- Master self configuration supported
- Master SPI configuration supported
- Slave SPI configuration supported
- Slave I^2C configuration supported
- Dual boot supported
- Online upgrade supported
- Compressed bitstream supported

➢ **Embedded Hard Core**

- Two I^2C hard cores
- One SPI hard core
- One timer/counter
- One on-chip oscillator

➢ **Application Areas**

- Consumer electronics
- Computing and storage
- Wireless communication
- Industrial control system

1.2 Device Resources and Package Information

The Compa family has five devices. The resource list for different devices is shown in Table 1-1:

Table 1-1 Compa Device Resources

Resource Name		PGC1K	PGC2K	PGC4K	PGC7K	PGC10K
CLM	LUT5	1064	2024	3968	5920	8256
	Equivalent LUT4	1276	2428	4761	7104	9907
	FF	1596	3036	5952	8880	12384
	Distributed RAM (Kbits)	11	16	39	56	78
DRM	9K[1]	7	8	11	26	45
	Maximum Capacity (Kbits)	63	72	99	234	405
PLL		1	1	2	2	2
Maximum User-available Capacity of Embedded Flash (Kbits)[2]		80[3]	80	1520	2070	3016
Maximum Capacity of Embedded Flash (Kbits)[4]		664	664	2560	3616	5120
Hard Cores	I^2C	2	2	2	2	2
	SPI	1	1	1	1	1
	Timer/Counters	1	1	1	1	1
on-chip Oscillator		1	1	1	1	1
Support for MIPI D-PHY		Yes	Yes	Yes	Yes	Yes

Note:

1. Each DRM has a capacity of 9 Kbits
2. The maximum user-available capacity of embedded Flash refers to the size of the ordinary memory space remaining after removing a set of ordinary bitstreams that do not include initialization data
3. The maximum user-available capacity of embedded Flash for PGC1KL is 310Kbits, while for PGC1KG it is 80Kbits
4. The maximum capacity of embedded Flash refers to the size of the ordinary memory space, which can be used to store bitstreams or other user data, etc.

The package information for Compa devices is shown in Table 1-2.

Table 1-2 Compa Devices Package and I/O Count

Device / Package Information	PGC1KL	PGC1KG	PGC2KL	PGC2KG	PGC4KL	PGC4KD	PGC7KD	PGC10KD
UWG36 (2.5mm*2.5mm,0.4mm)	29/3[1]							
UWG49 (3.2mm*3.2mm,0.4mm)			39/5[1]					
UWG81 (3.8mm*3.8mm,0.4mm)					64/10[1]			
LPG100 (14mm*14mm,0.5mm)		80/4[1]		80/4[1]				
LPG144		112/9[1]		112/9[1]		115/9[1]	115/9[1]	

Device / Package Information	PGC1KL	PGC1KG	PGC2KL	PGC2KG	PGC4KL	PGC4KD	PGC7KD	PGC10KD
(20mm*20mm,0.5mm)								
SSBG256 (9mm*9mm,0.5mm)			207/14[1]		207/18[1]			
MBG256 (14mm*14mm,0.8mm)		207/14[1]		207/14[1]		207/18[1]	207/20[1]	
MBG324 (15mm*15mm,0.8mm)						280/18[1]		
MBG332 (17mm*17mm,0.8mm)						275/18[1]	279/21[1]	
MBG400 (17mm*17mm,0.8mm)							336/21[1]	
MBG484 (19mm*19mm,0.8mm)								384/24[1]
FBG256 (17mm*17mm,1.0mm)		207/14[1]		207/14[1]		207/18[1]		
FBG484 (23mm*23mm,1.0mm)							335/21[1]	

Note:

1. X/Y indicates X user I/Os, Y pairs of true differential output pins

1.3 Ordering Information

The Compa family CPLDs devices ordering information are shown in Figure 1-1.

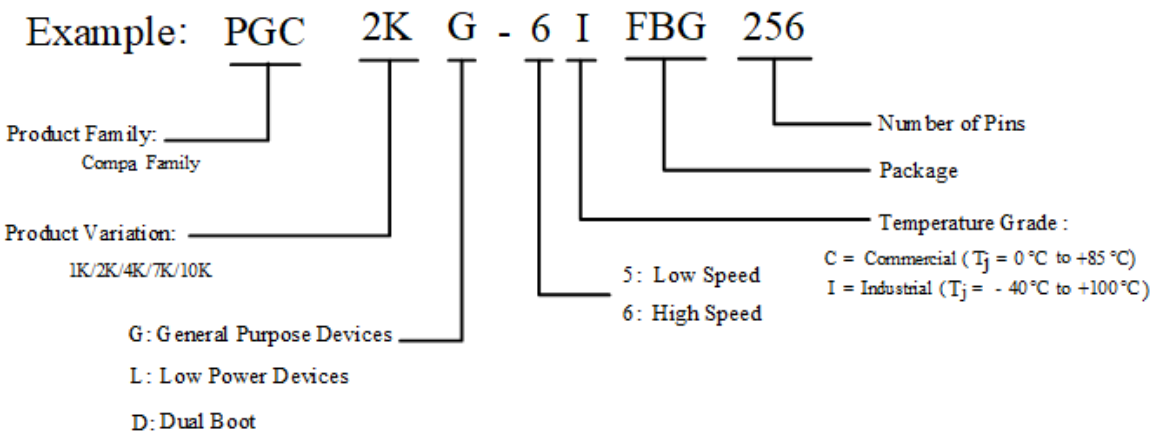

Figure 1-1 Compa Family CPLDs Device Ordering Information

1.4 Reference

Table 1-3 List of Compa Devices Documentation

Document Number	Document Name
UG030001	"Compa Family CPLDs Configurable Logic Module (CLM) User Guide"
UG030002	"Compa Family CPLDs Dedicated RAM Module (DRM) User Guide"
UG030003	"Compa Family CPLDs Clock Resources (Clock&PLL) User Guide"

Document Number	Document Name
UG030004	"Compa Family CPLDs Configuration User Guide"
UG030005	"Compa Family CPLDs Input/Output Interface (IO) User Guide"
UG030006	"Compa Family CPLDs Embedded Flash (EFlash) User Guide"
UG030007	"Compa Family CPLDs Embedded Hard Core User Guide"
UG030008	"Compa Family GTP User Guide"
UG030009	"Compa Family PCB Design User Guide"

Chapter 2 Functional Description

2.1 Configurable Logic Module (CLM)

CLM (Configurable Logic Module) is the basic logic unit of the Compa devices, each CLM contains 4 LUT5s, 6 registers, bit expansion function selectors, fast carry logic, and four independent cascade chains, which include the fast carry chain (Carry Chain), reset/set control cascade chain (RS Chain), clock enable control cascade chain (CE Chain), and shift register data cascade chain (SR Chain).

In each CLM, two LUT5s can implement one LUT6, and two LUT6s can implement one LUT7. Two adjacent CLMs can implement one LUT8.

There are two types of CLMs:

- CLMA, capable of implementing logic, arithmetic, shift registers, and ROM function
- CLMS, capable of implementing logic, arithmetic, shift registers, ROM function and distributed RAM function

CLMs can be configured in different functional modes:

- Logic Functional Mode
- Arithmetic Functional Mode
- ROM Memory Mode
- Distributed RAM Memory Mode
- Multiplexer Mode
- Output Register

For detailed information, please refer to the "***UG030001_Compa Family CPLDs Configurable Logic Module (CLM) User Guide***".

2.2 Dedicated Storage Module (DRM)

Compa devices contain up to 45 DRMs, each DRM has 9Kbits of storage, as well as input and output registers.

- Various Working Modes

DRM supports various working modes, including Dual-Port RAM, Simple Dual-Port RAM, Single-Port RAM or ROM mode, and FIFO mode. Table 2-1 shows the configuration modes supported by DRM.

Table 2-1 DRM Configuration List

DRM Mode	Single-Port RAM	Dual-Port RAM	Simple Dual-Port RAM	FIFO
Configurations	8K*1	8K*1	8K*1	8K*1
	4K*2	4K*2	4K*2	4K*2
	2K*4	2K*4	2K*4	2K*4
	1K*9(8)	1K*9(8)	1K*9(8)	1K*9(8)
	512*18(16)	N/A	512*18(16)	512*18(16)

- Mixed Data Width

DRM supports dual-port mixed data width in dual-port RAM and simple dual-port RAM modes.

Table 2-2 List of Dual-Port RAM Mode Mixed Data Width

Port A	Port B				
	8K x 1	4K x 2	2Kx4	1Kx8	1Kx9
8Kx1	√	√	√	√	
4Kx2	√	√	√	√	
2Kx4	√	√	√	√	
1Kx8	√	√	√	√	
1Kx9					√

Table 2-3 List of Simple Dual-Port RAM Mode Mixed Data Width

Read Port	Write Port						
	8Kx1	4Kx2	2Kx4	1Kx8	512x16	1Kx9	512x18
8Kx1	√	√	√	√	√		
4Kx2	√	√	√	√	√		
2Kx4	√	√	√	√	√		
1Kx8	√	√	√	√	√		
512x16	√	√	√	√	√		
1Kx9						√	√
512x18						√	√

- Byte Enable

DRM supports Byte Enable function for write operations, which allows writing to selected data bytes through enable signals while masking the write operations to other bytes at the same address index.

- Optional Output Registers

For data output ports, DRM provides an optional Output Register for improved timing performance.

- DRM Cascading and Extension

Multiple DRMs can be combined into larger Dual-Port RAM, Simple Dual-Port RAM, Single-Port RAM or ROM, and FIFO through cascading and extension. For this, DRM provides an additional 3-bit address extension for deeply-extended applications.

For detailed information, please refer to the "***UG030002_Compa Family CPLDs Dedicated RAM Module (DRM) User Guide***".

2.3 Clock

Compa devices have up to 8 pairs of dedicated clock differential input pins, which can receive differential input signals as well as single-ended input signals. When a single-ended clock signal is input, the P side of the differential signal is used. As clock inputs, these pins are used to drive clock network, and when not needed to drive clock network, they can also be used as general I/O.

- Global Clock Network

  The global clock network supports 8 global clocks as well as 8 global signals, which can also be used as global clocks.

  The global clock can provide clock signals for various resources within the device, such as CLM, DRM, and IO Logic. The global clock supports a clock frequency of up to 400MHz. The global clock supports dynamic clock enable and dynamic switching.

  Global signals are used as global control signals, such as clock enable signals, synchronous/asynchronous clear, reset, or output enable signals.

- I/O Clock Network

  There are 4 I/O clock networks, with 2 in BANK0 and 2 in BANK2. The clock signal can reach the IO Logic through the I/O clock, serving as the signal's high-speed sampling clock.

  The I/O clock has the characteristics of a high frequency (600 MHz) and low skew. The I/O clock supports dynamic enable.

- PLL

  Compa devices have up to 2 PLLs. The PLL of CPLD is the core subsystem that provides clock resources, its main functions include clock frequency synthesis, clock skew reduction, clock phase adjustment, and low power management.

  The PLL's input clock supports input from external I/O and internal routing. The PLL's feedback clock supports input from external I/O and internal routing.

  The PLL supports multiple clock outputs, each with an independent divider supporting division by 1-128; each clock output can be cascaded, and each PLL can be cascaded with one another; each clock output has an optional dynamic clock enable control; the PLL also supports fractional division clock output with 16-bit precision, allowing users to generate non-integer

output clocks. For the fractional division calculation method and usage restrictions, please refer to the "***UG030003_Compa Family CPLDs Clock Resources (Clock & PLL) User Guide***".

The PLL supports both static configuration and dynamic control of clock phase. Among these, the dynamic adjustment of the PLL's phase can be overridden via the APB interface or controlled through the corresponding port. The PLL can dynamically and continuously implement a gradual increase or decrease in phase, and there are no glitches in the clock output during phase adjustment.

PLL supports Standby mode, which allows the PLL to be powered down when not needed in the design to save power.

PLL allows users to change the PLL's operating parameters dynamically via the APB interface, providing users with another way to dynamically configure the PLL. For detailed information, please refer to the "***UG030003_Compa Family CPLDs Clock Resources (Clock & PLL) User Guide***".

2.4 I/O Cell

2.4.1 IO Buffer (IOB)

IO Buffers have varying numbers of I/O Banks depending on the device scale (see Table 2-4), with the bank distribution for each device as shown in Figure 2-1 and Figure 2-2.

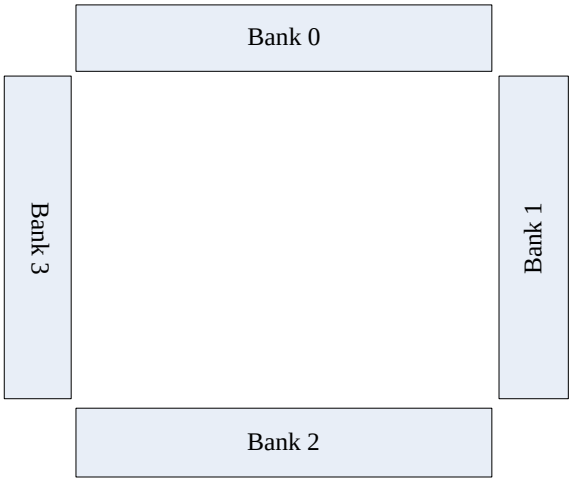

Figure 2-1 Top View of PGC1KL Bank Distribution

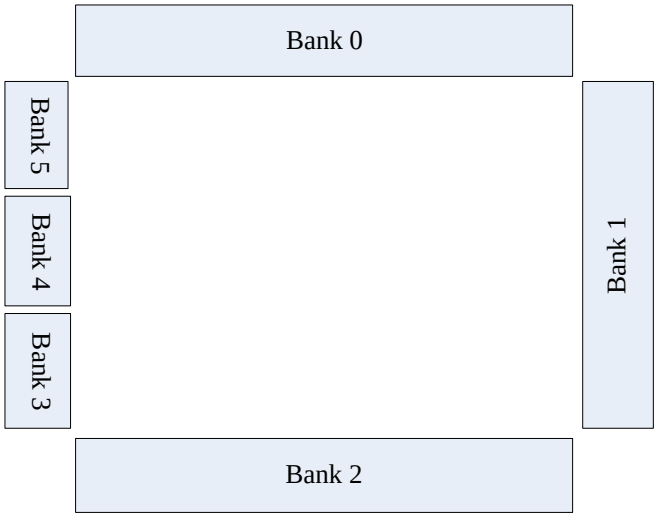

Figure 2-2 Top View of PGC1KG/2K/4K/7K/10K Bank Distribution

Table 2-4 Compa Device Bank Resource Distribution

I/O Bank Resources	PGC1KL1	PGC1KG	PGC2K1	PGC4K1	PGC7K	PGC10K
I/O Banks on the left	1	3	3	3	3	3
I/O Banks on the right	1	1	1	1	1	1
I/O Banks on the top	1	1	1	1	1	1
I/O Banks on the bottom	1	1	1	1	1	1
Total Number of I/O Banks	4	6	6	6	6	6

Note: 1. Devices in UWG package only support 3 banks, for detailed information, please refer to the package manual.

Each bank independently supports 1.2V-3.3V bank voltage. When the I/O in the entire bank is not in use, the bank power can be left floating or connected to the normal operating voltage. It is recommended to connect the bank power to V_{CC}. Each bank supports various single-ended and differential interface standards to accommodate different application scenarios. The IO Buffer is powerful, supports flexible configuration of I/O standards, output drive strength, slew rate, input hysteresis, and bus hold states. Furthermore, the IO Buffer supports an internal differential termination resistor of 100Ω, as well as LVDS and MIPI level standards.

All I/Os of the Compa devices support differential inputs, but only the I/Os on the bottom side (Bank2) support internal differential termination resistor. Some I/Os on the top side (Bank0) support true differential output (pins defined as DIFFIO support true differential output, for specific pin definitions, please refer to the PK family package manual). The I/O standards supported by the CPLD are shown in Table 2-5.

Table 2-5 I/O Standards Supported by Compa Family CPLDs

I/O Std	Typical Operating Voltage of I/O	Position	Comment
Input Single-Ended Standard			
LVTTL33	3.3 V	Top, Bottom, Left, Right	
LVCMOS	3.3/2.5/1.8/1.5/1.2 V	Top, Bottom, Left, Right	
PCI33	3.3 V	Bottom	
Input Differential Standard			
LVDS	3.3/2.5 V	Top, Bottom, Left, Right	Only the differential pairs on the bottom side (BANK2) support internal termination resistors
BLVDS	3.3/2.5 V	Top, Bottom, Left, Right	
MLVDS	3.3/2.5 V	Top, Bottom, Left, Right	
LVPECL33	3.3/2.5 V	Top, Bottom, Left, Right	
MIPI(D-PHY)	1.2 V	Top, Bottom, Left, Right	Only the differential pairs on the bottom side (BANK2) support internal termination resistors
Output Single-Ended Standard			
LVTTL33	3.3 V	Top, Bottom, Left, Right	
LVCMOS	3.3/2.5/1.8/1.5/1.2 V	Top, Bottom, Left, Right	
PCI33	3.3 V	Bottom	
Output Differential Standard			
LVDS	3.3/2.5 V	Top	True differential output, only pins with the function name DIFFIO are supported, see the package manual for details
BLVDS	2.5 V	Top, Bottom, Left, Right	LVCMOS analogue
MLVDS	2.5 V	Top, Bottom, Left, Right	LVCMOS analogue
LVPECL33	3.3 V	Top, Bottom, Left, Right	LVCMOS analogue
MIPI(D-PHY)	2.5 V	Top	
Bidirectional Level Standard			
LVTTL33	3.3 V	Top, Bottom, Left, Right	
LVCMOS	3.3/2.5/1.8/1.5/1.2 V	Top, Bottom, Left, Right	

2.4.2 IO Logic (IOL)

IO Logic mainly includes the following functions:

- Input, output, and tri-state combinatorial logic
- Input registers (flip-flops/latches), output registers (flip-flops), and tri-state registers (flip-flops)
- IDDR (1:2) and ODDR (2:1), where ODDR includes both output and tri-state ODDR

2.4.3 I/O Input/Output Delay Unit

The I/O input delay function and output delay function of the CPLD are respectively implemented by the same delay unit. All I/Os support static configuration for input and output delays, but only the I/Os on the bottom side support dynamically adjustable input and output delay.

Table 2-6 Step Delay of I/O Delay Unit

Symbol	Description	Min.	Typ.	Max.
$T_{IODELAY}$	The delay for each input/output delay step	55 ps	79 ps	125 ps

2.4.4 High-Speed Data Transfer

I/O units, in conjunction with ISERDES and OSERDES modules, can implement high-speed data transmission and reception.

- ISERDES: For high-speed interfaces, supports 1:4, 1:7, 1:8
- OSERDES: For high-speed interfaces, supports 4:1, 7:1, 8:1

All Banks support IDDR/ODDR and input/output/tri-state registers. For high-speed interface applications, the bottom Bank supports ISERDES, while the top Bank supports OSERDES.

2.5 On-chip Oscillator

Each Compa device has an on-chip Oscillator (OSC). The output of the OSC can be programmed to connect to the global clock network or to the PLL as a reference clock for the PLL. The output of the OSC can also provide a programmable clock for the configuration system, used as the main configuration clock. The output of the OSC can also provide a fixed frequency clock for embedded Flash.

Users can perform clock division for the OSC by instantiating GTP_OSC_E2. The intrinsic frequency of the OSC is 266MHz, with an integer division factor range of 2-128, and the output frequency range of the OSC is 2.08MHz-133MHz; these frequency points are discontinuous, with a default value of 2.08MHz. When the OSC output clock serves as the user clock, the frequency that can be output is shown in Table 2-7.

Table 2-7 OSC Output Frequency

OSC Output Frequency (Division Factor), in MHz							
2.08(128)	2.09(127)	2.11(126)	2.13(125)	2.15(124)	2.16(123)	2.18(122)	2.20(121)
2.22(120)	2.24(119)	2.25(118)	2.27(117)	2.29(116)	2.31(115)	2.33(114)	2.35(113)
2.38(112)	2.40(111)	2.42(110)	2.44(109)	2.46(108)	2.49(107)	2.51(106)	2.53(105)
2.56(104)	2.58(103)	2.61(102)	2.63(101)	2.66(100)	2.69(99)	2.71(98)	2.74(97)
2.77(96)	2.80(95)	2.83(94)	2.86(93)	2.89(92)	2.92(91)	2.96(90)	2.99(89)

OSC Output Frequency (Division Factor), in MHz							
3.02(88)	3.06(87)	3.09(86)	3.13(85)	3.17(84)	3.20(83)	3.24(82)	3.28(81)
3.33(80)	3.37(79)	3.41(78)	3.45(77)	3.50(76)	3.55(75)	3.59(74)	3.64(73)
3.69(72)	3.75(71)	3.80(70)	3.86(69)	3.91(68)	3.97(67)	4.03(66)	4.09(65)
4.16(64)	4.22(63)	4.29(62)	4.36(61)	4.43(60)	4.51(59)	4.59(58)	4.67(57)
4.75(56)	4.84(55)	4.93(54)	5.02(53)	5.12(52)	5.22(51)	5.32(50)	5.43(49)
5.54(48)	5.66(47)	5.78(46)	5.91(45)	6.05(44)	6.19(43)	6.33(42)	6.49(41)
6.65(40)	6.82(39)	7.00(38)	7.19(37)	7.39(36)	7.60(35)	7.82(34)	8.06(33)
8.31(32)	8.58(31)	8.87(30)	9.17(29)	9.50(28)	9.85(27)	10.23(26)	10.64(25)
11.08(24)	11.57(23)	12.09(22)	12.67(21)	13.30(20)	14.00(19)	14.78(18)	15.65(17)
16.63(16)	17.73(15)	19.00(14)	20.46(13)	22.17(12)	24.18(11)	26.60(10)	29.56(9)
33.25(8)	38.00(7)	44.33(6)	53.20(5)	66.50(4)	88.67(3)	133.00(2)	

The accuracy of the OSC in Compa devices is shown in Table 2-8.

Table 2-8 List of OSC Accuracy for CPLD Devices

Device / Temperature Grade	PGC1KL	PGC1KG	PGC2KL	PGC2KG	PGC4KL	PGC4KD	PGC7KD	PGC10KD
Commercial (C)	**±5.5%**	±10%	**±5.5%**	±10%	**±5.5%**	±10%	±10%	±10%
Industrial (I)	±10%	±10%	±10%	±10%	±10%	±10%	±10%	±10%

For detailed information, please refer to the "***UG030003_Compa Family CPLDs Clock Resources (Clock & PLL) User Guide***".

2.6 Embedded Hard Core

Compa devices have multiple embedded hard cores, such as I^2C, SPI, and timers/counters. Users can access these hard cores via the APB interface.

2.6.1 I^2C Hard Core

Each CPLD device includes 2 I^2C Hard Cores, each of which can be configured as a master or slave device. When the I^2C Hard Core is configured as a master device, it can control other devices via the I^2C bus interface.

The I^2C Hard Core mainly supports the following functions:

- Configurable as master or slave, supports master-slave operation
- 7-bit and 10-bit addressing
- Arbitration among multiple masters

- Fast mode/standard mode I^2C bus protocols, with data transfer speeds up to 400KHz
- 8-bit APB bus user interface
- Soft reset
- Interrupt
- All-Call addressing

2.6.2 SPI Hard Core

Each CPLD device includes 1 SPI Hard Core, which can be configured as a master or slave device. When acting as a master device, it can control other chips with SPI interfaces via the SPI bus. The SPI Hard Core supports the following functions:

- Configurable as master or slave, supports master-slave operation
- Interrupt
- Serial clock with programmable polarity and phase
- Data transfer supports least significant bit first or most significant bit first
- 8-bit APB bus user interface
- Controls up to 8 slave devices

2.6.3 Timer/Counters

Each CPLD device provides a general, bidirectional 16-bit timer/counter Hard Core. It has an independent output compare unit and supports pulse width modulation. This Hard Core supports the following functions:

- Supports the following working modes
  - Watchdog
  - Auto clear timer
  - Fast pulse width modulation
  - Phase and frequency correction pulse width modulation
- Programmable clock input
- Interrupt request
- Auto reload
- Time stamps
- 8-bit APB bus user interface

For more information, please refer to the "***UG030007_Compa Family CPLDs Embedded Hard Core User Guide***".

2.7 Embedded Flash

Compa devices include an embedded Flash that can be used to store configuration information or provide general Flash storage space for the user. Embedded Flash has the following functions:

- 1.2V Supply voltage, provided by VCC_{CORE}
- Storage space up to 5120 Kbits
- At least 100,000 erase/write cycles
- Auto-incrementing addressing
- Supports JTAG, I^2C, SPI, and APB interfaces

For detailed information, please refer to the "***UG030006_Compa Family CPLDs Embedded Flash (***EFlash***) User Guide***".

2.8 Power-On Reset (POR) Circuit

Each Compa device has a Power-On Reset circuit (POR), which monitors VCC_{CORE} and V_{CCIO0} voltage levels during power-up and operation. At power-up, once the POR circuit detects that VCC_{CORE} and V_{CCIO0} reach V_{PUP} (as shown in Table 3-6), the device will start initialization.

Shared I/O can be set as configuration I/O or user I/O by setting the feature control bits. All I/Os are at a low level during power-up; before and during configuration, user I/Os are held in tri-state with a weak pull-down, and configuration I/Os have a weak pull-up or their inherent state; after configuration is complete and the device enters user mode, user I/Os are then released for user use.

After entering user mode, the POR circuit continues to monitor VCC_{CORE}. If VCC_{CORE} drops to the specified voltage V_{PDN}, the device is not guaranteed to work properly; should this occur, the POR circuit resets the entire chip and monitors VCC_{CORE} and V_{CCIO0} again.

2.9 Configuration and Test

- Configuration

Compa devices include various configuration interfaces, such as JTAG, SPI, and I^2C. JTAG supports the IEEE 1149.1 boundary scan specification and the IEEE 1532 in-system configuration specification. With the support of these configuration interfaces, there are multiple modes available to configure Compa Family devices.

- Master Self Download
- JTAG mode

- Master SPI mode
- Slave SPI mode
- Slave I^2C mode

After the device is powered up, it starts initialization, then selects a configuration mode after reading feature control bits; once the configuration mode is determined, the corresponding pins are set as configuration pins, users can use them to download the bitstream to the configuration memory; when the bitstream is loaded successfully, the device enters user mode.

All configuration pins can be shared, and when some configuration pins are not used for configuration functions, they can be used as general I/Os after entering user mode.

CPLD devices support compressed bitstreams.

CPLD devices support readback functionality to read configuration data from CRAM. The readback process does not affect the system's normal operation. They also support disabling readback of CRAM to secure user information.

CPLD devices support dual boot.

CPLD devices support remote upgrade.

- Boundary Scan Test

Compa devices integrate a boundary scan unit that supports IEEE 1149.1, which users can access via JTAG. JTAG includes four signals: TDI, TDO, TCK, and TMS.

Each I/O inside the device comes with a boundary scan unit, and these units are interconnected internally through the input and output pins. Test data flows through the TDI port, accesses each I/O via serial shifting, and then flows out from the TDO port. By analyzing the test response, fault diagnosis of the circuit under test can be performed.

The JTAG port is powered by V_{CCIO0} and supports LVCMOS33/LVCMOS25/LVCMOS18/LVCMOS15/LVCMOS12. For detailed information, please refer to the "***UG030004_Compa Family CPLDs Configuration User Guide***".

2.10 UID (Unique Identification)

Each Compa device has a unique UID, which can be used to track information or guarantee IP security. The UID has 64 bits and is read-only. The UID can be read via the on-chip UID interface or the on-chip APB interface, as well as through SPI, I^2C, or JTAG interfaces.

For detailed information, please refer to the "***UG030004_Compa Family CPLDs Configuration User Guide***".

Chapter 3 DC Characteristics

3.1 Device Absolute Maximum Ratings

The absolute maximum ratings for Compa devices are shown in Table 3-1:

Table 3-1 Absolute Maximum Ratings

Parameter Description1,2	**L type (1.2V)**	**G type/D type (2.5V or 3.3V)**	**Unit**
External supply voltage V_{CC}	-0.5 ~ 1.32	-0.5 ~ 3.75	V
I/O Bank voltage V_{CCIO}	-0.5 ~ 3.75	-0.5 ~ 3.75	V
I/O tri-state voltage	-0.5 ~ 3.75	-0.5 ~ 3.75	V
Input I/O voltage V_{IN}	-0.5 ~ 3.75	-0.5 ~ 3.75	V
Storage ambient temperature (T_A)	-55 ~ 125	-55 ~ 125	℃
Junction temperature T_J	-40 ~ 125	-40 ~ 125	℃
Maximum soldering temperature T_{SOL}	260	260	℃

Note:

1. Exceeding the limits specified in the table above may cause permanent damage to the device; operating within the absolute maximum ratings will not damage the device, but does not guarantee normal operation at these limits; prolonged operation at these limits will drastically impact the device's reliability.
2. All voltage values are with respect to GND

3.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions for Device

Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{CC}[1]	External supply voltage for L-type devices	1.14	1.2	1.26	V
	External supply voltage for G-type/D-type devices	2.375	2.5/3.3	3.465	V
V_{CCIO}[1]	I/O Bank voltage	1.14	--	3.465	V
T_J	Commercial operating junction temperature	0	--	85	℃
	Industrial operating junction temperature	-40	--	100	℃

Note:

1. In PCB design, unused I/O Bank V_{CCIO} pins can be left floating or powered; it is recommended to connect them to V_{CC}; to ensure the chip functions properly, V_{CCIO0} must be powered correctly.

3.3 Allowed AC Maximum Overshoot and Undershoot Voltage for V_{IN}

Table 3-3 Allowed AC Maximum Overshoot and Undershoot Voltage for V_{IN}

Overshoot Voltage (V)	%UI (-40 ℃~100 ℃)	Undershoot Voltage (V)	%UI (-40 ℃~100 ℃)
3.75	100	-0.45	100
3.8	86	-0.5	86
3.85	58	-0.55	58
3.9	39.5	-0.6	39.5
3.95	27	-0.65	27
4	18.5	-0.7	18.5
4.05	12.75	-0.75	12.75
4.1	8.81	-0.8	8.81
4.15	6.13	-0.85	6.13
4.2	4.28	-0.9	4.28

3.4 ESD and Latch Up Specifications

Table 3-4 ESD and Latch Up Specifications

ESD (HBM)	ESD (CDM)	Latch-up
±2000 V	±500 V	±100 mA

3.5 Power Ramp-up Time

Table 3-5 Ramp-up Time

Symbol	Description	Min.	Typ.	Max.	Unit
T_{VCCR}	Ramp-up time for V_{CC}	0.20	--	100.0	ms
T_{CCIOR}	Ramp-up time for I/O Bank voltage	0.20	--	100.0	ms
There is no power-up sequence requirement for V_{CC} and each bank's V_{CCIO}					

3.6 Power-up Reset Voltage Standard

Table 3-6 Power-up Reset Voltage Standard[1,2]

Symbol	Description	Min.	Typ.	Max.	Unit
V_{PUP}	Power-up reset trigger level (monitoring VCC_{CORE} and V_{CCIO0})	0.9	--	1.06	V
V_{PUPEXT}	Power-up reset trigger level (monitoring V_{CC})	1.5	--	2.1	V
V_{PDN}	Power-down reset trigger level (monitoring VCC_{CORE})	0.75	--	0.93	V
V_{PDNEXT}	Power-down reset trigger level (monitoring V_{CC})	1.6	--	1.85	V

Note:

1. L-type devices do not have an internal LDO, thus VCC_{CORE} are same with V_{CC}; for G-type/D-type devices, VCC_{CORE} is generated from V_{CC} by the LDO

2. V_{PUPEXT} and V_{PDNEXT} are only applicable to G-type/D-type devices

3.7 Hot Socketing Specifications

Table 3-7 Hot Socketing Specifications

Symbol	Description	Condition	Min.	Max.	Unit
I_{DK}	I/O Leakage current	$0<V_{IN}<V_{IH}$(Max)	-1000	+1000	μA

3.8 Single-Ended DC Characteristics

Table 3-8 Single-Ended I/O DC Characteristics

Standard	V_{IL}(V)		V_{IH} (V)		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min.	Max.	Min.	Max.				
PCI33	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.465	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5
LVCMOS33 LVCMOS33D LVTTL33	-0.3	0.8	2.0	3.465	0.4	V_{CCIO}-0.4	4	-4
							8	-8
							12	-12
							16	-16
LVCMOS25 LVCMOS25D	-0.3	0.7	1.7	3.465	0.4	V_{CCIO}-0.4	4	-4
							8	-8
							12	-12
							16	-16
LVCMOS18	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.465	0.4	V_{CCIO}-0.4	4	-4
							8	-8
							12	-12
LVCMOS15	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.465	0.4	V_{CCIO}-0.4	4	-4
							8	-8
LVCMOS12	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.465	0.4	V_{CCIO}-0.4	2	-2
							6	-6

3.9 Differential DC Electrical Characteristics

The main electrical parameters of LVDS, BLVDS, and LVPECL33 are defined as shown in Figure 3-1.

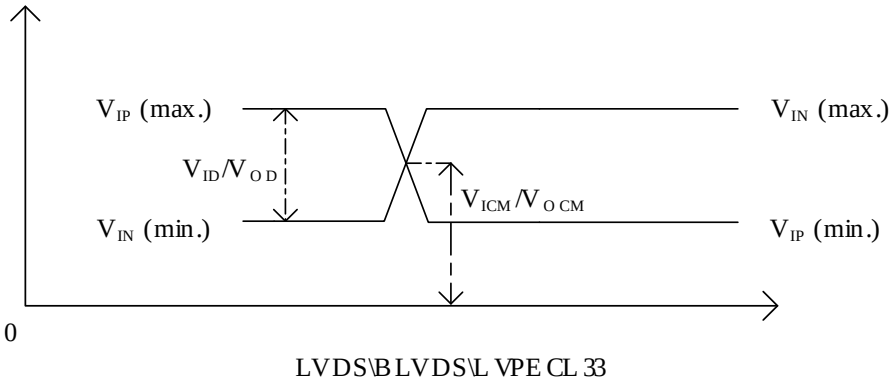

Figure 3-1 LVDS\BLVDS\LVPECL33 Voltage Waveforms

3.9.1 LVDS DC Characteristics

Table 3-9 LVDS DC Characteristics

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{IP}, V_{IN}	Input Voltage	V_{CCIO}=3.3V	0	--	2.605	V
		V_{CCIO}=2.5V	0	--	2.05	V
V_{ID}	Input Differential Mode Voltage		0.1	--	--	V
V_{ICM}	Input Common Mode Voltage	V_{CCIO}=3.3V	0.4	--	2.4	V
		V_{CCIO}=2.5V	0.4	--	1.9	V
V_{OD}	Output Differential Mode Voltage	(Vop-Von), Rt=100 Ω	0.245	0.350	0.455	V
$\triangle V_{OD}$	V_{OD} Variation Range		--	--	0.050	V
V_{OCM}	Output Common Mode Voltage	(Vop+Von)/2, Rt=100 Ω	1.0	1.2	1.4	V
$\triangle V_{OCM}$	V_{OCM} Variation Range		--	--	0.050	V

3.9.2 BLVDS DC Characteristics

Table 3-10 BLVDS DC Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
VIP,VIN	Input Voltage	0	--	2.05	V
VID	Input Differential Mode Voltage	0.1	--	--	V
VICM	Input Common Mode Voltage	0.4	--	1.9	V
VOD	Output Differential Mode Voltage	0.230	--	0.460	V

Symbol	Description	Min.	Typ.	Max.	Unit
VIP,VIN	Input Voltage	0	--	2.05	V
VID	Input Differential Mode Voltage	0.1	--	--	V
VOCM	Output Common Mode Voltage	1.1	--	1.4	V
R_{left}	Left Terminal Resistance	40	--	100	Ω
R_{right}	Right Terminal Resistance	40	--	100	Ω
R_S	Driver Serial Resistance	--	80	--	Ω

3.9.3 LVPECL33 DC Characteristics

Table 3-11 LVPECL33 DC Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
V_{ICM}	Input Common Mode Voltage	0.4	--	2.4	V
V_{OD}	Output Differential Mode Voltage	0.78	--	1.0	V
V_{OCM}	Output Common Mode Voltage	1.3	--	2.1	V
R_S	Driver Serial Resistance	--	100	--	Ω
R_P	Driver Parallel Resistance	--	200	--	Ω
R_T	Receiver Terminal Resistance	--	100	--	Ω

3.9.4 MIPI DC Characteristics

Compa devices support unidirectional HS (High Speed) and bidirectional LP (Low Power) input and output for MIPI D-PHY. The electrical parameters for the MIPI receiver are defined as shown in Figure 3-2.

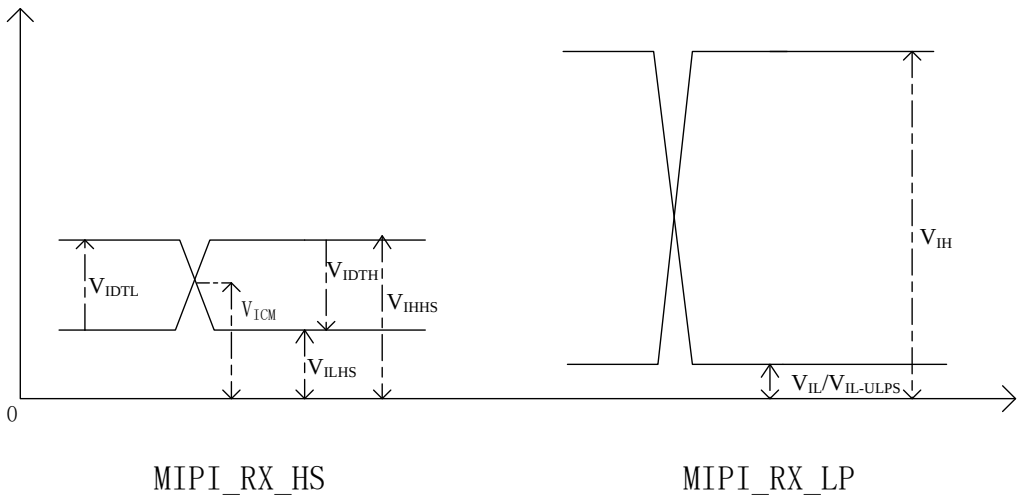

Figure 3-2 MIPI Receiver Voltage Waveforms

Table 3-12 lists the DC characteristics of the MIPI receiver.

Table 3-12 MIPI Receiver DC Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
High Speed RX					
V_{ICM}	HS Input Common Mode Voltage	70	--	330	mV
V_{CCIO}	I/O Bank voltage	--	1.2	--	V
V_{IDTH}	Differential Input High Level Threshold	--	--	70	mV
V_{IDTL}	Differential Input Low Level Threshold	-70	--	--	mV
V_{IHHS}	Single-Ended Input High Level Voltage	--	--	460	mV
V_{ILHS}	Single-Ended Input Low Level Voltage	-40	--	--	mV
$V_{TERM-EN}$	Termination Enabled Voltage Threshold	--	--	450	mV
Z_{ID}	Differential Input Impedance	80	100	125	Ω
Low Power RX					
V_{IH}	Input High Level Voltage	880	--	--	mV
V_{CCIO}	I/O Bank voltage	--	1.2	--	V
V_{IL}	Input Low Level Voltage	--	--	550	mV
$V_{IL-ULPS}$	Input Low Level Voltage (Ultra-Low Power Mode)	--	--	300	mV
V_{HYST}	Input Hysteresis	25	--	--	mV

Table 3-13 lists the DC characteristics of the MIPI transmitter. The electrical parameters for the MIPI transmitter are defined as shown in Figure 3-3.

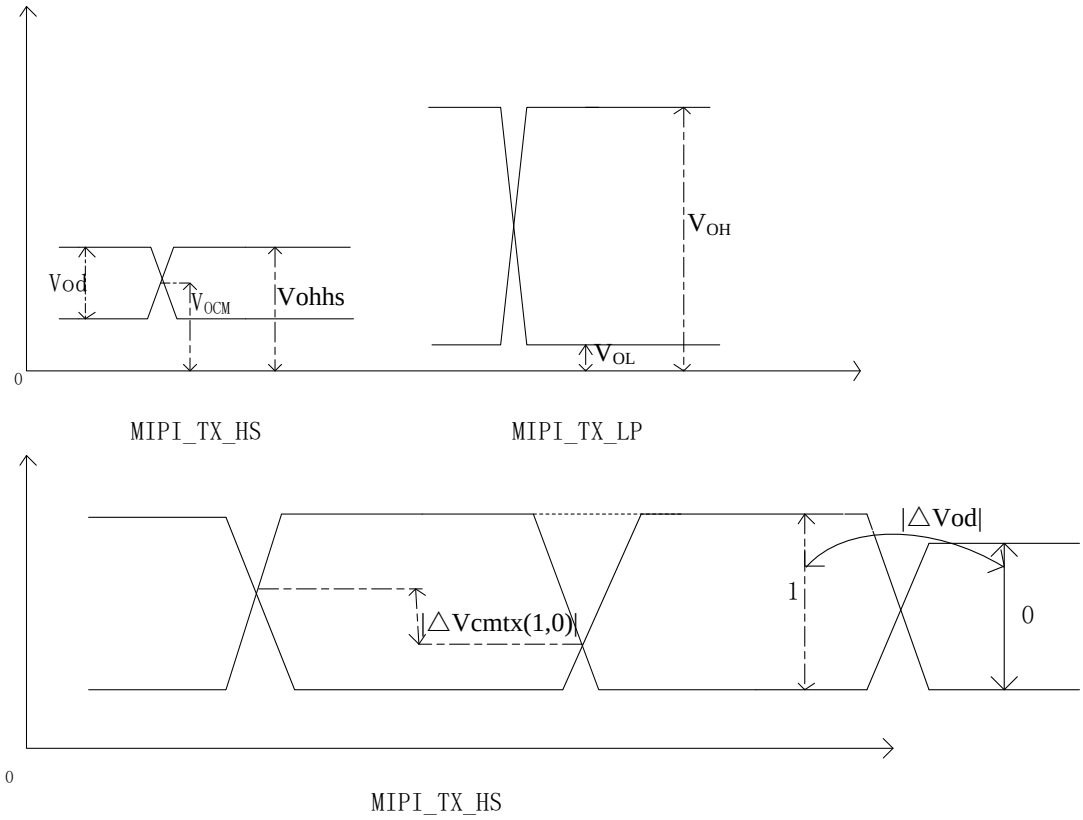

Figure 3-3 MIPI Transmitter Voltage Waveforms

Table 3-13 MIPI Transmitter DC Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
High Speed TX					
V_{OCM}	HS Output Common Mode Voltage	150	200	250	mV
V_{CCIO}	I/O Bank voltage	--	2.5	--	V
|△Vcmtx(1,0)|	Difference in Output Common Mode Voltage between Differential 1 and Differential 0	--	--	5	mV
|Vod|	Output Differential Mode Voltage	140	200	270	mV
|△Vod|	Difference in Output Differential Mode Voltage between Differential 1 and Differential 0	--	--	10	mV
Vohhs	HS Output High Level Voltage	--	--	360	mV
Z_{OS}	Single-Ended Output Impedance	40	50	62.5	Ω
$\triangle Z_{OS}$	Difference in Single-End Output Impedance	--	--	10%	--
Low Power TX					
V_{OH}	Output High Level	1.1	1.2	1.3	V
V_{CCIO}	I/O Bank voltage	--	1.2	--	V
V_{OL}	Output Low Level	-50	--	50	mV
Z_{OLP}	LP Mode Output Impedance	110	--	--	Ω

3.10 Input DC Characteristics

Table 3-14 Input DC Characteristics under Recommended Operating Conditions

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
I_{IL}	Leakage Current during Input Low Level	$0 \le V_{IN} \le (V_{CCIO} - 0.2V)$	-10	--	10	μA
I_{IH}	Leakage Current during Input High Level	$(V_{CCIO} - 0.2V) < V_{IN} \le 3.6V$	--	--	175	μA
C_{IN}	I/O Input Capacitor	25 ℃, 1MHz Signal Frequency	--	--	10	pF
I_{PU}	I/O Pull-Up Current	$0 \le V_{IN} \le 0.7\ V_{CCIO}$	-30	--	-310	μA
I_{PD}	I/O Pull-Down Current	$V_{IL}(Max) \le V_{IN} \le V_{CCIO}$	30	--	310	μA
I_{BKL}	Sustaining Current during Bus Keep Low	$V_{IN} = V_{IL}$ (Max)	30	--	--	μA
I_{BKH}	Sustaining Current during Bus Keep High	$V_{IN} = 0.7\ V_{CCIO}$	-30	--	--	μA
I_{BKLOD}	Overdrive Current during Bus Keep Low	$0 \le V_{IN} \le V_{CCIO}$	--	--	310	μA
I_{BKHOD}	Overdrive Current during Bus Keep High	$0 \le V_{IN} \le V_{CCIO}$	--	--	-310	μA
V_{BKV}	Bus Keep Threshold		V_{IL} (Max)	--	V_{IH} (Min)	--

3.11 Quiescent Current

At an ambient temperature of 25 ℃ and with the device unconfigured, the quiescent current is shown in Table 3-15.

Table 3-15 Quiescent Current

Symbol	Description	Device	Typ.	Unit
I_{VCC}	External Power Supply Current	PGC1KL	3	mA
		PGC1KG	4.6	mA
		PGC2KL	4	mA
		PGC2KG	4.6	mA
		PGC4KL	4.6	mA
		PGC4KD	7.2	mA
		PGC7KD	9	mA
		PGC10KD	12	mA
I_{CCIO}	I/O Bank Current, I/O Bank Voltage at 2.5V	All devices	0	mA

3.12 Embedded Flash Program and Erase Current

Table 3-16 Embedded Flash Program and Erase Current[1,2]

Symbol	Description	Device	Typ.
I_{VCC}	External Power Supply	PGC1KL	--

Symbol	Description	Device	Typ.
	Current	PGC1KG	8.4 mA
		PGC2KL	--
		PGC2KG	--
		PGC4KL	--
		PGC4KD	--
		PGC7KD	--
I_{CCIO}	I/O Bank Current, I/O Bank Voltage at 2.5V	All devices	0 mA

Note:

1. Bitstream function is implemented in a marquee form.

2. Test conditions: room temperature at 25 ℃, V_{CCIO} =2.5V, JTAG interface frequency at 15MHz

Chapter 4 AC Switching Characteristics

4.1 DRM Switching Characteristics

Table 4-1 DRM AC Characteristics

Symbol	Description	Speed Grade		Unit
		-5	-6	
F_{MAX_DRM}	Single DRM, NW Mode	235	280	MHz
	Single DRM, TW Mode	235	280	MHz
	Single DRM, RBW Mode	168	200	MHz
	Single DRM, FIFO Mode	235	280	MHz

4.2 Clock AC Characteristics

Table 4-2 Clock AC Characteristics

Parameter Description	-5			-6			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Global Clock Frequency	--	--	340	--	--	400	MHz
Global Clock Pulse Width	0.575	--	--	0.5	--	--	ns
Global Clock Skew	--	--	920	--	--	800	ps
Global Clock Duty Cycle	45%	50%	55%	45%	50%	55%	--
Global Clock Dynamic Switching Hold Time	$2(T_{CLKIN0}+T_{CLKIN1})$	--	--	$2(T_{CLKIN0}+T_{CLKIN1})$	--	--	--
I/O Clock Frequency	--	--	510	--	--	600	MHz
I/O Clock Skew	--	--	40.25	--	--	35	ps
I/O Clock Duty Cycle	43%	50%	57%	43%	50%	57%	--

4.3 PLL AC Characteristics

Table 4-3 PLL AC Characteristics

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
f_{IN}	Input Clock Frequency		10	--	500	MHz
f_{OUT}	Output Clock Frequency		3.125	--	600	MHz
$f_{OUT-CAS}$[1]	Cascaded Output Clock Frequency (Stage 1)		0.0244	--	600	MHz
f_{VCO}	VCO Frequency (G/D)		400	--	1200	MHz
	VCO Frequency (L)		400	--	800	MHz
f_{PFD}	PFD Frequency (Integer Division)		10	--	500	MHz
	PFD Frequency (Fractional		20	--	40	MHz

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
	Division)					
t_{DUTY}	Output Clock Duty Cycle		45%	50%	55%	--
$t_{IJITTER}$	Input Clock Cycle-to-Cycle Jitter	f_{PFD} ≥20 MHz	--	--	0.01	UIPP
		f_{PFD} < 20 MHz	--	--	500	ps p-p
$t_{OJITTER}$	Output Clock Period Jitter (Integer Division)	f_{OUT} ≥ 100 MHz	--	--	155	ps p-p
		f_{OUT} < 100 MHz	--	--	0.008	UIPP
	Output Clock Cycle-to-Cycle Jitter (Integer Division)	f_{OUT} ≥ 100 MHz	--	--	185	ps p-p
		f_{OUT} < 100 MHz	--	--	0.010	UIPP
	Output Clock Period Jitter (Fractional Division)	f_{OUT} ≥ 100 MHz	--	--	235	ps p-p
		f_{OUT} < 100 MHz	--	--	0.13	UIPP
	Output Clock Cycle-to-Cycle Jitter (Fractional Division)	f_{OUT} ≥ 100 MHz	--	--	235	ps p-p
		f_{OUT} < 100 MHz	--	--	0.13	UIPP
	Output Clock Phase Jitter (Integer Division)	f_{PFD} ≥ 100 MHz	--	--	165	ps p-p
		f_{PFD} < 100 MHz	--	--	0.012	UIPP
t_{PH}	Phase Shift Accuracy		-6% Tvco	--	+6% Tvco	--
t_{LOCK}	PLL Lock Time		--	--	5	ms
t_{RST}	RST Pulse Width		10	--	--	ns

Note:

1. For each additional stage of cascade, divide by 128 based on the output clock of the previous stage.

4.4 Configuration AC Characteristics

Table 4-4 Configuration AC Characteristics

Configuration Mode	Description	Min.	Typ.	Max.	Unit
JTAG	TCK Frequency	--	--	50	MHz
	TCK Low Pulse Width	10	--	--	ns
	TCK High Pulse Width	10	--	--	ns
	TMS/TDI Setup Time (TCK Rising Edge)	3	--	--	ns
	TMS/TDI Hold Time (TCK Rising Edge)	2	--	--	ns
	TCK Falling Edge to Valid TDO Output	--	--	8	ns
Master SPI	SCK Initial Frequency	--	--	2.08	MHz
	SCK Frequency (High Speed Mode)	--	--	53.2	MHz
	SCK Frequency (Low Speed Mode, Max 5ns from SPI Flash Clock Falling Edge to Valid Data Output)	--	--	29.55	MHz

Configuration Mode	Description	Min.	Typ.	Max.	Unit
	SCK Frequency (Low Speed Mode, Max 6ns from SPI Flash Clock Falling Edge to Valid Data Output)	--	--	26.6	MHz
	SCK Frequency (Low Speed Mode, Max 7ns from SPI Flash Clock Falling Edge to Valid Data Output)	--	--	26.6	MHz
	SCK Frequency (Low Speed Mode, Max 8ns from SPI Flash Clock Falling Edge to Valid Data Output)	--	--	24.18	MHz
	SCK Duty Cycle	45%	50%	55%	--
	SCK Frequency Deviation	--	--	5%	--
	MISO Setup Time (SCK Rising Edge)	10	--	--	ns
	MISO Hold Time (SCK Rising Edge)	0	--	--	ns
	MISO Setup Time (SCK Falling Edge)	9	--	--	ns
	MISO Hold Time (SCK Falling Edge)	0	--	--	ns
	SCK Falling Edge to Valid MOSI Output	--	--	4	ns
	SCK Falling Edge to Valid CS_N Output	--	--	4	ns
Slave SPI	SCK Frequency	--	--	100	MHz
	SCK Low Pulse Width	5	--	--	ns
	SCK High Pulse Width	5	--	--	ns
	MOSI Setup Time (SCK Rising Edge)	3	--	--	ns
	MOSI Hold Time (SCK Rising Edge)	2	--	--	ns
	SCK Falling Edge to Valid MISO Output	--	--	10	ns
Reset Pulse Width		384	--	--	ns
Delay from Completion of Device Initialization to SCK Output		400	--	--	ns
INIT_FLAG_N Low Time	PGC1K	--	--	964	µs
	PGC2K	--	--	964	µs
	PGC4K	--	--	600	µs
	PGC7K	--	--	870	µs
	PGC10K	--	--	1500	µs

4.5 I²C Interface AC Characteristics

Table 4-5 I²C Interface AC Characteristics

Description(1)	Standard Mode		Fast Mode		Unit
	Min.	Max.	Min.	Max.	
SCL Frequency	--	100	--	400	KHz
SCL Low Pulse Width	4.7	--	1.3	--	µs
SCL High Pulse Width	4	--	0.6	--	µs

Note:

1. Other parameters are as specified in the I²C protocol

4.6 SPI Hard Core AC Characteristics

Table 4-6 SPI Hard Core AC Characteristics

Description	Fast Mode		Unit
	Min.	Max.	
SCK Frequency[1]	--	45	MHz

Note:

1. For performance specifications of configuration mode, see Table 4-4 Configuration AC Characteristics

4.7 IO Buffer Performance

Table 4-7 IO Buffer Performance

Standard	Maximum Speed		Unit
	-5	-6	
LVDS[1]	1080 (540 MHz)	1200 (600 MHz)	Mbps
MIPI[2]	810 (405 MHz)	900 (450 MHz)	Mbps
BLVDS25	270 (135 MHz)	300 (150 MHz)	Mbps
MLVDS25	270 (135 MHz)	300 (150 MHz)	Mbps
LVPECL33	270 (135 MHz)	300 (150 MHz)	Mbps
LVTTL33	270 (135 MHz)	300 (150 MHz)	Mbps
LVCMOS33	270 (135 MHz)	300 (150 MHz)	Mbps
LVCMOS25	270 (135 MHz)	300 (150 MHz)	Mbps
LVCMOS18	270 (135 MHz)	300 (150 MHz)	Mbps
LVCMOS15	270 (135 MHz)	300 (150 MHz)	Mbps
LVCMOS12	180 (90 MHz)	200 (100 MHz)	Mbps
PCI33	59	66	MHz

Note:

1. G-type/D-type devices support such performance
2. L-type devices support such performance

4.8 High-Speed Data Transfer Performance

Table 4-8 List of High-Speed Data Transfer Performance

High-Speed Data Transfer Application	Transfer Rate		Unit
	-5	-6	
LVDS 2: 1	360	400	Mbps
LVDS 4: 1	630	700	Mbps
LVDS 7: 1	693	770	Mbps
LVDS 8: 1	720	800	Mbps
MIPI D-PHY	810	900	Mbps

4.9 Master Self Configuration Time

Table 4-9 Master Self Configuration Time[1]

Device	Configuration Time1	Unit
PGC1K	1.3	ms
PGC2K	1.3	ms
PGC4K	2.4	ms
PGC7K	3.8	ms
PGC10K	5.8	ms

Note:

1. Master Self Configuration Time refers to the time from the completion of CPLD initialization to entering user mode

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