PK02007_PGL25G_MBG324

(V1.4)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.4	28.01.2021	Initial release

About this Manual

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Terms and Abbreviations	Meaning
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Chapter 1 Introduction to Packaging

PGL25G_MBG324 uses a Wire-Bond BGA type of packaging. Its package size is 15mmx15mm, with 324 solder balls, a pitch of 0.8mm and a maximum package thickness of 1.41mm.

Chapter 2 Package Dimension and Pins

2.1 Package Outline Dimension

Table 2-1 Dimensional Values

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	1.21	1.31	1.41	c	0.22	0.26	0.30
A1	0.30	0.35	0.40	e	-	0.8	-
A2	0.91	0.96	1.01	b	0.40	0.45	0.50
D	14.9	15.0	15.1	aaa	-	-	0.15
E	14.9	15.0	15.1	bbb	-	-	0.25
D1	-	13.6	-	ddd	-	-	0.20
E1	-	13.6	-	eee	-	-	0.15

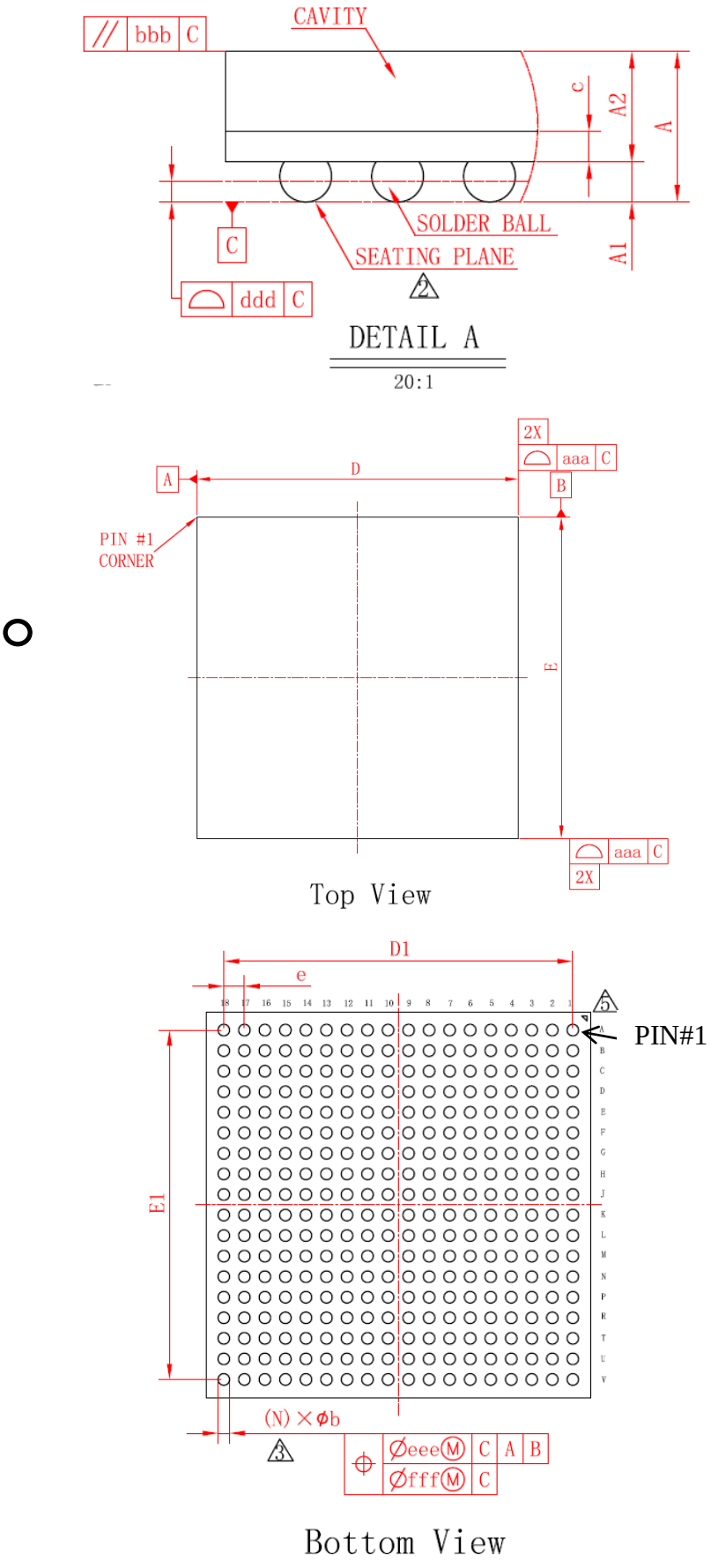

Figure 2-1 Package Outline Dimension (POD)

Note: Pin #1 is the pin 1 position of the chip

2.2 Pin Description

PGL25G_MBG324 has 226 user IOs.

Table 2-2 Product Pin Definitions

PIN name	PIN type	PIN description
General IO PIN		
IO	I/O	General IO Before or during configuration, when IO_STATUS_C=0, enable internal pull-up; when IO_STATUS_C=1,disable internal pull-up In user mode, unused IOs default to pull-down, but can also be configured by the user as pull-up, pull-down, or float via bitstream
-- Multi-function Configuration Pin		
MODE_1	input	Multi-function configuration input pin, used for selecting between master and slave configuration modes; MODE_1=0 master mode; MODE_1=1 slave mode
MODE_0	input	Multi-function configuration input pin, used for selecting between parallel and serial configuration modes MODE_0=0 parallel configuration; MODE_0=1 serial configuration
INIT_FLAG_N	Bidirectional (open-drain)	When it is low, it indicates that the FPGA's internal CRAM is being cleared, and this pin will be released by internal control upon completion. If this pin is pulled low externally, it will delay the configuration process If this pin is low during configuration, it indicates an internal configuration error occurred
CFG_CLK	inpu, output	Configuration clock pin. In the slave mode, this pin serves as a clock input to obtain configuration data from external sources; In the master mode, this pin serves as a clock output to obtain configuration data from external sources; When the clock is not needed (such as in the JTAG mode), this pin is high-z.
ECCLK	input	Optional external configuration clock input pin in the master mode
CS_N	inpu, output	Multi-function configuration pin. (1) In the Slave Parallel configuration mode, this pin enables the parallel configuration mode data interface at a low level; (2) In the SPI x1 mode, when this pin is connected to the Slave Data input interface of the SPI Flash, FPGA will send instructions and initial address to the SPI Flash; (3) In the SPI x2 and x4 modes, it is connected to the SPI flash's IO0 as the [0]th bit of the data bus.
CSO_N	output	Multi-function configuration pin (1) In the slave parallel configuration mode, it serves as the cascaded chip select signal output; (2) In the master SPI mode, it serves as the chip select signal output.
D0	input	Multi-function configuration data pin (1) In the SPI x1 mode, this pin connects to the Slave Data output interface of the SPI Flash, and FPGA receives serial data from the SPI Flash, i.e., Master Input/Slave Output; (2) In the SPI x2 and x4 modes, this pin also serves as the

PIN name	PIN type	PIN description
		[1]st bit of the SPI data bus; (3) In the Parallel or BPI mode, this pin serves as the lowest bit of the data bus; (4) In the Slave Serial mode, this pin serves as data input.
D[1,2]	inpu, output	Multi-function configuration data pin (1) In the SPI x2 and x4 modes, pin D[1] serves as the [2]nd bit connected to SPI flash's IO2, pin D[2] as the [3]rd bit connected to SPI flash's IO3 (2) In the slave parallel or BPI mode, this pin serves as the [2:1] bits of the data bus.
D[3、5…15]	inpu, output	Multi-function configuration data pin In the Slave Parallel or BPI mode with x8 width, D[7:4] serves as the [7:3]th bit of the data bus; In the Slave Parallel or BPI mode with x16 width, D[15:4] serves as the [15:3]th bit of the data bus.
RWSEL	input	Multi-function configuration pin. For selecting the read/write input in the Slave Parallel configuration mode (high for read and low for write). (1) When it is high, the Slave Parallel configuration mode reads data from the data bus; (2) When it is low, the Slave Parallel configuration mode writes data to the data bus; (3) Read and write can be switched only when CS_N is high.
DOUT_BUSY	output	Multi-function configuration pin. (1) During readback in the Slave Parallel mode, this pin indicates the device status. It indicates the data read from the bus is invalid when high; (2) In the Serial configuration mode, this pin serves as cascaded data output, and the data is valid on the falling edge of CFG_CLK; (3) In the SPI configuration mode, this pin serves as cascaded data output, and the data is valid on the falling edge of CFG_CLK.
IO_STATUS_C	input	Multi-function input pin; used for controlling whether the pull-up resistors for all user IOs are enabled during the configuration process. (1) When the signal is 0, the internal IO pull-up resistors,for user IOs are enabled before or during configuration; (2) When the signal is 1, the internal IO pull-up resistors,for user IOs are disable before or during configuration.
ADR[0, 1, …, 25]	output	Multi-function configuration pin, address output in BPI configuration mode. (1) After configuration is completed, it can be used as a user IO
BFWE_N	output	Multi-function configuration pin, used for providing a low-level write enable signal for parallel NOR FLASH in the BPI configuration mode.
BFOE_N	output	Multi-function configuration pin, used for providing a low-level output enable signal for parallel NOR FLASH in the BPI configuration mode.
BFCE_N	output	Multi-function configuration pin, used for providing a low-level chip select control signal for parallel NOR FLASH in the BPI configuration mode.
BHDC	output	In BPI mode, there is high output during the configuration
BLDC	output	In BPI mode, there is low output during the configuration
-- Clock, PLL, Crystal Oscillator Multi-function Pin		

PIN name	PIN type	PIN description
GCLK[0,1,2,3…,30,31]	input	Dedicated Global Clock Input pin. Can also serve as a general user I/O, 8 pins for each bank When serves as differential clock input, GCLK[1,3,5,…,27,29,31] are the internal valid input
PLL[0,1,2,3]_CLK[0,1,2,…,13,14,15]	input	Optional PLL reference clock input, PLL can directly input a clock from these pins; Optional PLL feedback clock input, PLL can externally feedback the clock from these pins.; Can also be used as general user I/Os.
--Differential Pin		
DIFFIO_[0,1,2,3]_[0…n][N,P]	I/O, true differential input/output	Transmitting and receiving differential signals. Used for transmitting and receiving LVDS signals. The suffix "P" indicates the "positive" signal and the suffix "N" indicates the "negative" signal. If not used as differential signal pins, these pins can serve as general user I/Os. Each IOBD tile is provided with a pair of differential signals.
DIFFI_[0,1,2,3]_[0…n]_[N,P]	I/O, true differential input	Differential signal receive pin. Can be used for receiving differential input signals. The suffix "P" indicates the "positive" signal and the suffix "N" indicates the "negative" signal. If not used as differential input pins, these pins can be used as general user I/Os; each IOBS tile is provided with a pair of differential inputs.
-- External Memory Interface Pin		
DQS[0,1,2,3,4,5][#]_[1,3]	DQS	Multi-function pin. Used to connect to the DQS/DQS# signal pins of external memory. Also used as general user I/Os.
DQ[0,1,2,3,4,5][#]_[1,3]	DQ	Multi-function pin, can connect to the DQ signal pins of external memory. Also used as general user I/Os.
Dedicated Pin		
--Configuration Pin, JTAG Pin		
CFG_DONE	Bidirectional (open-drain)	Dedicated pin for configuration state. Serves as a status output, driven low before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released.
RST_N	input	Dedicated configuration input pin, internally weak pull-up, for restarting the configuration process, active-low. It is recommended that users externally pull up the RST_N with a resistor when using this pin. When this pin is low, the FPGA enters a reset state, and all IOs are in the High-Z state.
CMPCS_B		No need to be connected, left floating
STAND_BY		No need to be connected, left floating
TCK	input	Dedicated JTAG test clock input pin
TMS	input	Dedicated JTAG test mode selection input pin
TDI	input	Dedicated JTAG test data input pin.
TDO	output	Dedicated JTAG test data output pin.
--Reference Pin		
VREF_[B0,B1,B2,B3]	input	External reference voltage pin, one for each bank. Provide reference voltage input for each BANK When a VREF is used, all VREFs in that bank must be connected
Power Pin, Ground Pin		

PIN name	PIN type	PIN description
VCC	POWER	Core power supply, 1.2V. Power supply for core logic
VCCAUX	POWER	3.3V auxiliary power supply for IOB, LDO, EFUSE, dedicated configuration IOB, and other modules
VCCIO[0,1,2,3]	POWER	IO BANK power
VSS	GROUND	GND relative to VDD11 & VDD33 & VDDIO

2.2.1 Pin Name list

Table 2-3 Pin Name List

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B0	DIFFIO_B0_0P/IO_STATUS_C	D4	IO_1_P	52.4701	
B0	DIFFIO_B0_0N/VREF_B0	C4	IO_1_N	52.9778	
B0	DIFFIO_B0_1P	B2	IO_2_P	61.5623	
B0	DIFFIO_B0_1N	A2	IO_2_N	63.1409	
B0	DIFFIO_B0_2P	D6	IO_3_P	52.3575	
B0	DIFFIO_B0_2N	C6	IO_3_N	49.6892	
B0	DIFFIO_B0_3P	B3	IO_4_P	47.6484	
B0	DIFFIO_B0_3N	A3	IO_4_N	51.5523	
B0	DIFFIO_B0_4P	B4	IO_5_P	56.6733	
B0	DIFFIO_B0_4N	A4	IO_5_N	57.2247	
B0	DIFFIO_B0_5P	C5	IO_6_P	51.0343	
B0	DIFFIO_B0_5N	A5	IO_6_N	53.3312	
B0	DIFFIO_B0_6P	C7	IO_7_P	54.2334	
B0	DIFFIO_B0_6N	A7	IO_7_N	59.2472	
B0	DIFFIO_B0_7P	B6	IO_8_P	40.6995	
B0	DIFFIO_B0_7N/VREF_B0	A6	IO_8_N	41.1881	
B0	DIFFIO_B0_13P	D8	IO_14_P	28.295	
B0	DIFFIO_B0_13N	C8	IO_14_N	27.66	
B0	DIFFIO_B0_14P	B8	IO_15_P	60.8503	
B0	DIFFIO_B0_14N	A8	IO_15_N	62.8958	
B0	DIFFIO_B0_15P/GCLK19/PLL0_CLK0/PLL1_CLK0	D9	IO_16_P	57.5811	
B0	DIFFIO_B0_15N/GCLK18/PLL0_CLK1/PLL1_CLK1	C9	IO_16_N	57.8194	
B0	DIFFIO_B0_16P/GCLK17/PLL0_CLK2/PLL1_CLK2	B9	IO_17_P	62.2248	
B0	DIFFIO_B0_16N/GCLK16/PLL0_CLK3/PLL1_CLK3	A9	IO_17_N	61.6134	
B0	DIFFIO_B0_17P/GCLK15/PLL0_CLK4/PLL1_CLK4	D11	IO_18_P	49.423	
B0	DIFFIO_B0_17N/GCLK14/PLL0_CLK5/PLL1_CLK5	C11	IO_18_N	50.5312	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B0	DIFFIO_B0_18P/GCLK13/PLL0_CLK6/PLL1_CLK6	C10	IO_19_P	58.1264	
B0	DIFFIO_B0_18N/GCLK12/PLL0_CLK7/PLL1_CLK7	A10	IO_19_N	59.7338	
B0	DIFFIO_B0_19P	G9	IO_20_P	56.1173	
B0	DIFFIO_B0_19N/VREF_B0	F9	IO_20_N	52.5955	
B0	DIFFIO_B0_20P	B11	IO_21_P	64.2857	
B0	DIFFIO_B0_20N	A11	IO_21_N	64.5473	
B0	DIFFIO_B0_21P	G11	IO_22_P	56.6986	
B0	DIFFIO_B0_21N	F10	IO_22_N	55.7093	
B0	DIFFIO_B0_22P	B12	IO_23_P	69.5739	
B0	DIFFIO_B0_22N	A12	IO_23_N	68.3292	
B0	DIFFIO_B0_23P	F11	IO_24_P	38.1971	
B0	DIFFIO_B0_23N	E11	IO_24_N	37.6869	
B0	DIFFIO_B0_24P	D12	IO_25_P	72.4704	
B0	DIFFIO_B0_24N	C12	IO_25_N	68.571	
B0	DIFFIO_B0_27P	C13	IO_28_P	46.6633	
B0	DIFFIO_B0_27N	A13	IO_28_N	39.289	
B0	DIFFIO_B0_28P	F12	IO_29_P	64.2877	
B0	DIFFIO_B0_28N	E12	IO_29_N	64.9687	
B0	DIFFIO_B0_29P	B14	IO_30_P	52.7972	
B0	DIFFIO_B0_29N/VREF_B0	A14	IO_30_N	42.6886	
B0	DIFFIO_B0_30P	F13	IO_31_P	57.399	
B0	DIFFIO_B0_30N	E13	IO_31_N	55.6879	
B0	DIFFIO_B0_31P	C15	IO_32_P	50.685	
B0	DIFFIO_B0_31N	A15	IO_32_N	53.5273	
B0	DIFFIO_B0_32P	D14	IO_33_P	58.5692	
B0	DIFFIO_B0_32N	C14	IO_33_N	60.7782	
B0	DIFFIO_B0_33P	B16	IO_34_P	56.1126	
B0	DIFFIO_B0_33N	A16	IO_34_N	43.7311	
B1	DIFFI_B1_0P/ADR25	F15	IO_35_P	32.0428	DQ0_B1
B1	DIFFI_B1_0N/ADR24/VREF_B1	F16	IO_35_N	31.7661	DQ0_B1
B1	DIFFI_B1_7P/ADR23	C17	IO_42_P	55.7455	DQ1_B1
B1	DIFFI_B1_7N/ADR22	C18	IO_42_N	50.6111	DQ1_B1
B1	DIFFI_B1_8P/ADR21	F14	IO_43_P	41.7712	DQ1_B1
B1	DIFFI_B1_8N/ADR20	G14	IO_43_N	41.0063	DQ1_B1
B1	DIFFI_B1_9P/ADR19	D17	IO_44_P	49.4419	DQ1_B1
B1	DIFFI_B1_9N/ADR18	D18	IO_44_N	59.8922	DQ1_B1
B1	DIFFI_B1_10P/ADR17	H12	IO_45_P	55.7093	DQS1_B1
B1	DIFFI_B1_10N/ADR16	G13	IO_45_N	54.7555	DQS1#_B1

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B1	DIFFI_B1_11P/ADR15	E16	IO_46_P	53.2503	DQ1_B1
B1	DIFFI_B1_11N/ADR14	E18	IO_46_N	56.3536	DQ1_B1
B1	DIFFI_B1_12P/ADR13	K12	IO_47_P	64.0453	DQ1_B1
B1	DIFFI_B1_12N/ADR12	K13	IO_47_N	63.3124	DQ1_B1
B1	DIFFI_B1_13P/ADR11	F17	IO_48_P	45.9356	DQ2_B1
B1	DIFFI_B1_13N/ADR10	F18	IO_48_N	59.0836	DQ2_B1
B1	DIFFI_B1_14P/ADR9	H13	IO_49_P	50.1472	DQ2_B1
B1	DIFFI_B1_14N/ADR8	H14	IO_49_N	50.0842	DQ2_B1
B1	DIFFI_B1_15P/ADR7	H15	IO_50_P	45.8197	DQS2_B1
B1	DIFFI_B1_15N/ADR6	H16	IO_50_N	51.2488	DQS2#_B1
B1	DIFFI_B1_16P/ADR5	G16	IO_51_P	42.0387	DQ2_B1
B1	DIFFI_B1_16N/ADR4	G18	IO_51_N	44.0844	DQ2_B1
B1	DIFFI_B1_17P	J13	IO_52_P	69.5639	DQ2_B1
B1	DIFFI_B1_17N	K14	IO_52_N	67.8847	DQ2_B1
B1	DIFFI_B1_18P/GCLK11/PLL0_CLK8/PLL1_CLK8	L12	IO_53_P	79.4102	DQ2_B1
B1	DIFFI_B1_18N/GCLK10/PLL0_CLK9/PLL1_CLK9	L13	IO_53_N	81.4688	DQ2_B1
B1	DIFFI_B1_19P/GCLK9/PLL0_CLK10/PLL1_CLK10	K15	IO_54_P	57.0056	DQ2_B1
B1	DIFFI_B1_19N/GCLK8/PLL0_CLK11/PLL1_CLK11	K16	IO_54_N	56.3695	DQ2_B1
B1	DIFFI_B1_21P/GCLK7/PLL2_CLK8/PLL3_CLK8	L15	IO_56_P	69.1431	DQ3_B1
B1	DIFFI_B1_21N/GCLK6/PLL2_CLK9/PLL3_CLK9	L16	IO_56_N	69.7664	DQ3_B1
B1	DIFFI_B1_22P/GCLK5/PLL2_CLK10/PLL3_CLK10	H17	IO_57_P	45.7723	DQ3_B1
B1	DIFFI_B1_22N/GCLK4/PLL2_CLK11/PLL3_CLK11	H18	IO_57_N	53.2464	DQ3_B1
B1	DIFFI_B1_23P/ADR3	J16	IO_58_P	72.8158	DQ3_B1
B1	DIFFI_B1_23N/ADR2	J18	IO_58_N	61.5452	DQ3_B1
B1	DIFFI_B1_24P/ADR1	K17	IO_59_P	30.4575	DQS3_B1
B1	DIFFI_B1_24N/ADR0	K18	IO_59_N	31.2903	DQS3#_B1
B1	DIFFI_B1_25P/BFCE_N	L17	IO_60_P	57.5752	DQ3_B1
B1	DIFFI_B1_25N/BFOE_N	L18	IO_60_N	57.2848	DQ3_B1
B1	DIFFI_B1_26P/BFWE_N	M16	IO_61_P	36.8294	DQ3_B1
B1	DIFFI_B1_26N/BLDC	M18	IO_61_N	38.2094	DQ3_B1
B1	DIFFI_B1_28P/BHDC	N17	IO_63_P	55.1656	DQ4_B1
B1	DIFFI_B1_28N	N18	IO_63_N	56.5817	DQ4_B1
B1	DIFFI_B1_29P	P17	IO_64_P	66.5251	DQ4_B1
B1	DIFFI_B1_29N	P18	IO_64_N	66.3262	DQ4_B1
B1	DIFFI_B1_30P	N15	IO_65_P	36.281	DQS4_B1
B1	DIFFI_B1_30N	N16	IO_65_N	28.5249	DQS4#_B1

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B1	DIFFI_B1_31P	T17	IO_66_P	68.936	DQ4_B1
B1	DIFFI_B1_31N	T18	IO_66_N	70.73	DQ4_B1
B1	DIFFI_B1_32P	U17	IO_67_P	73.859	DQ4_B1
B1	DIFFI_B1_32N	U18	IO_67_N	72.2951	DQ4_B1
B1	DIFFI_B1_33P	M14	IO_68_P	64.1183	DQ5_B1
B1	DIFFI_B1_33N/VREF_B1	N14	IO_68_N	61.5786	DQ5_B1
B1	DIFFI_B1_36P	L14	IO_71_P	49.0412	DQ5_B1
B1	DIFFI_B1_36N	M13	IO_71_N	47.8475	DQ5_B1
B1	DIFFI_B1_39P	P15	IO_74_P	41.9963	DQ5_B1
B1	DIFFI_B1_39N/DOUT_BUSY	P16	IO_74_N	49.0036	DQ5_B1
B2	DIFFIO_B2_0N/CSO_N	V3	IO_75_N	64.092	
B2	DIFFIO_B2_0P/INIT_FLAG_N	U3	IO_75_P	63.0629	
B2	DIFFIO_B2_1N/D9	P6	IO_76_N	52.1922	
B2	DIFFIO_B2_1P/D8	N5	IO_76_P	53.3843	
B2	DIFFIO_B2_2N	V4	IO_77_N	44.5318	
B2	DIFFIO_B2_2P	T4	IO_77_P	47.523	
B2	DIFFIO_B2_3N/D6	T3	IO_78_N	58.3775	
B2	DIFFIO_B2_3P/D5	R3	IO_78_P	57.0415	
B2	DIFFIO_B2_11N/D4	V5	IO_86_N	61.0346	
B2	DIFFIO_B2_11P/D3	U5	IO_86_P	64.0549	
B2	DIFFIO_B2_12N/RDWR_B/VREF_B2	T5	IO_87_N	45.486	
B2	DIFFIO_B2_12P/D7	R5	IO_87_P	46.395	
B2	DIFFIO_B2_13N	P7	IO_88_N	53.6989	
B2	DIFFIO_B2_13P	N6	IO_88_P	54.3416	
B2	DIFFIO_B2_14N	T7	IO_89_N	32.1829	
B2	DIFFIO_B2_14P	R7	IO_89_P	44.1873	
B2	DIFFIO_B2_15N	V6	IO_90_N	61.2548	
B2	DIFFIO_B2_15P	T6	IO_90_P	59.9949	
B2	DIFFIO_B2_16N	P8	IO_91_N	48.7594	
B2	DIFFIO_B2_16P	N7	IO_91_P	47.6618	
B2	DIFFIO_B2_17N	V7	IO_92_N	50.7572	
B2	DIFFIO_B2_17P	U7	IO_92_P	47.7764	
B2	DIFFIO_B2_19N/VREF_B2	V8	IO_94_N	42.6899	
B2	DIFFIO_B2_19P	U8	IO_94_P	41.481	
B2	DIFFIO_B2_20N	N8	IO_95_N	50.0965	
B2	DIFFIO_B2_20P	M8	IO_95_P	52.2277	
B2	DIFFIO_B2_21N/GCLK28/PLL2_CLK0/PLL3_CLK0	V9	IO_96_N	44.8453	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B2	DIFFIO_B2_21P/GCLK29/PLL2_CLK1/PLL3_CLK1	T9	IO_96_P	41.807	
B2	DIFFIO_B2_22N/GCLK30/D15/PLL2_CLK2/PLL3_CLK2	T8	IO_97_N	41.2947	
B2	DIFFIO_B2_22P/GCLK31/D14/PLL2_CLK3/PLL3_CLK3	R8	IO_97_P	41.2294	
B2	DIFFIO_B2_23N/GCLK0/ECCLK/PLL2_CLK4/PLL3_CLK4	V10	IO_98_N	56.5967	
B2	DIFFIO_B2_23P/GCLK1/D13/PLL2_CLK5/PLL3_CLK5	U10	IO_98_P	57.3558	
B2	DIFFIO_B2_24N/GCLK2/PLL2_CLK6/PLL3_CLK6	T10	IO_99_N	41.6786	
B2	DIFFIO_B2_24P/GCLK3/PLL2_CLK7/PLL3_CLK7	R10	IO_99_P	41.9433	
B2	DIFFIO_B2_25N	V11	IO_100_N	58.679	
B2	DIFFIO_B2_25P	U11	IO_100_P	53.5255	
B2	DIFFIO_B2_26N	N9	IO_101_N	50.5346	
B2	DIFFIO_B2_26P	M10	IO_101_P	52.6474	
B2	DIFFIO_B2_28N	P11	IO_103_N	47.6593	
B2	DIFFIO_B2_28P	N10	IO_103_P	46.6593	
B2	DIFFIO_B2_29N	V12	IO_104_N	55.8485	
B2	DIFFIO_B2_29P	T12	IO_104_P	59.705	
B2	DIFFIO_B2_30N/VREF_B2	T11	IO_105_N	31.0775	
B2	DIFFIO_B2_30P	R11	IO_105_P	30.6394	
B2	DIFFIO_B2_31N	N11	IO_106_N	69.5847	
B2	DIFFIO_B2_31P	M11	IO_106_P	69.4281	
B2	DIFFIO_B2_32N/D12	V13	IO_107_N	43.0463	
B2	DIFFIO_B2_32P/D11	U13	IO_107_P	52.0097	
B2	DIFFIO_B2_33N/D10	P12	IO_108_N	56.7464	
B2	DIFFIO_B2_33P/MODE_1	N12	IO_108_P	55.8569	
B2	DIFFIO_B2_34N/D2	V14	IO_109_N	49.987	
B2	DIFFIO_B2_34P/D1	T14	IO_109_P	58.1267	
B2	DIFFIO_B2_36N	V15	IO_111_N	62.7616	
B2	DIFFIO_B2_36P	U15	IO_111_P	58.1102	
B2	DIFFIO_B2_37N/CS_N	T13	IO_112_N	39.3534	
B2	DIFFIO_B2_37P/D0	R13	IO_112_P	49.7451	
B2	DIFFIO_B2_38N	V16	IO_113_N	47.6463	
B2	DIFFIO_B2_38P	U16	IO_113_P	56.2324	
B2	DIFFIO_B2_39N/MODE_0	T15	IO_114_N	41.9307	
B2	DIFFIO_B2_39P/CFG_CLK	R15	IO_114_P	41.8383	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B3	DIFFI_B3_0N/VREF_B3	C1	IO_115_N	42.5944	DQ0_B3
B3	DIFFI_B3_0P	C2	IO_115_P	40.1184	DQ0_B3
B3	DIFFI_B3_7N	F5	IO_122_N	63.0423	DQ1_B3
B3	DIFFI_B3_7P	F6	IO_122_P	62.7236	DQ1_B3
B3	DIFFI_B3_8N	D3	IO_123_N	47.0692	DQ1_B3
B3	DIFFI_B3_8P	E4	IO_123_P	47.6352	DQ1_B3
B3	DIFFI_B3_9N	G6	IO_124_N	59.999	DQ1_B3
B3	DIFFI_B3_9P	H7	IO_124_P	60.5527	DQ1_B3
B3	DIFFI_B3_10N	D1	IO_125_N	73.5303	DQS1#_B3
B3	DIFFI_B3_10P	D2	IO_125_P	74.1913	DQS1_B3
B3	DIFFI_B3_11N	F3	IO_126_N	60.028	DQ1_B3
B3	DIFFI_B3_11P	F4	IO_126_P	61.5238	DQ1_B3
B3	DIFFI_B3_12N	E1	IO_127_N	65.1889	DQ1_B3
B3	DIFFI_B3_12P	E3	IO_127_P	63.9827	DQ1_B3
B3	DIFFI_B3_13N	H5	IO_128_N	59.0221	DQ2_B3
B3	DIFFI_B3_13P	H6	IO_128_P	60.6452	DQ2_B3
B3	DIFFI_B3_14N	F1	IO_129_N	55.6909	DQ2_B3
B3	DIFFI_B3_14P	F2	IO_129_P	55.4387	DQ2_B3
B3	DIFFI_B3_15N	J6	IO_130_N	61.2716	DQS2#_B3
B3	DIFFI_B3_15P	J7	IO_130_P	62.358	DQS2_B3
B3	DIFFI_B3_16N	G1	IO_131_N	54.2552	DQ2_B3
B3	DIFFI_B3_16P	G3	IO_131_P	54.3246	DQ2_B3
B3	DIFFI_B3_17N	K6	IO_132_N	61.795	DQ2_B3
B3	DIFFI_B3_17P	L7	IO_132_P	59.1006	DQ2_B3
B3	DIFFI_B3_18N/GCLK20/PLL0_CLK12/PLL1_CLK12	H3	IO_133_N	35.7023	DQ2_B3
B3	DIFFI_B3_18P/GCLK21/PLL0_CLK13/PLL1_CLK13	H4	IO_133_P	45.0415	DQ2_B3
B3	DIFFI_B3_19N/GCLK22/PLL0_CLK14/PLL1_CLK14	K5	IO_134_N	47.4484	DQ2_B3
B3	DIFFI_B3_19P/GCLK23/PLL0_CLK15/PLL1_CLK15	L5	IO_134_P	46.1427	DQ2_B3
B3	DIFFI_B3_21N/GCLK24/PLL2_CLK12/PLL3_CLK12	K3	IO_136_N	45.5366	DQ3_B3
B3	DIFFI_B3_21P/GCLK25/PLL2_CLK13/PLL3_CLK13	K4	IO_136_P	41.3689	DQ3_B3
B3	DIFFI_B3_22N/GCLK26/PLL2_CLK14/PLL3_CLK14	H1	IO_137_N	47.0919	DQ3_B3
B3	DIFFI_B3_22P/GCLK27/PLL2_CLK15/PLL3_CLK15	H2	IO_137_P	50.2362	DQ3_B3
B3	DIFFI_B3_23N	J1	IO_138_N	65.1677	DQ3_B3
B3	DIFFI_B3_23P	J3	IO_138_P	65.6229	DQ3_B3
B3	DIFFI_B3_24N	L3	IO_139_N	47.6211	DQS3#_B3
B3	DIFFI_B3_24P	L4	IO_139_P	46.661	DQS3_B3

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B3	DIFFI_B3_25N	K1	IO_140_N	60.0043	DQ3_B3
B3	DIFFI_B3_25P	K2	IO_140_P	56.1222	DQ3_B3
B3	DIFFI_B3_26N	L1	IO_141_N	51.6355	DQ3_B3
B3	DIFFI_B3_26P	L2	IO_141_P	50.6313	DQ3_B3
B3	DIFFI_B3_28N	M1	IO_143_N	45.2781	DQ4_B3
B3	DIFFI_B3_28P	M3	IO_143_P	42.0166	DQ4_B3
B3	DIFFI_B3_29N	N1	IO_144_N	43.9435	DQ4_B3
B3	DIFFI_B3_29P	N2	IO_144_P	51.4008	DQ4_B3
B3	DIFFI_B3_30N	P1	IO_145_N	58.2251	DQS4#_B3
B3	DIFFI_B3_30P	P2	IO_145_P	53.8929	DQS4_B3
B3	DIFFI_B3_31N	T1	IO_146_N	64.9111	DQ4_B3
B3	DIFFI_B3_31P	T2	IO_146_P	69.0601	DQ4_B3
B3	DIFFI_B3_32N	U1	IO_147_N	72.6813	DQ4_B3
B3	DIFFI_B3_32P	U2	IO_147_P	71.7652	DQ4_B3
B3	DIFFI_B3_33N/VREF_B3	M5	IO_148_N	53.2324	DQ5_B3
B3	DIFFI_B3_33P	L6	IO_148_P	51.3589	DQ5_B3
B3	DIFFI_B3_38N	P3	IO_153_N	33.9769	DQ5_B3
B3	DIFFI_B3_38P	P4	IO_153_P	35.714	DQ5_B3
B3	DIFFI_B3_39N/VREF_B3	N3	IO_154_N	34.6537	DQ5_B3
B3	DIFFI_B3_39P	N4	IO_154_P	42.0452	DQ5_B3
B2	CFG_DONE	V17			
B2	CMPCS_B	P13			
B2	RST_N	V2			
	STAND_BY	R16			
	TCK	A17			
	TDI	D15			
	TDO	D16			
	TMS	B18			
	NC	E6			
	NC	E7			
	NC	E8			
	NC	F7			
	NC	F8			
	NC	G8			
	VCC	G7			
	VCC	H9			
	VCC	H11			
	VCC	J8			
	VCC	J10			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
	VCC	K9			
	VCC	K11			
	VCC	L8			
	VCC	L10			
	VCC	M7			
	VCC	M12			
	VCCAUX	B1			
	VCCAUX	B17			
	VCCAUX	E5			
	VCCAUX	E9			
	VCCAUX	E14			
	VCCAUX	G10			
	VCCAUX	J12			
	VCCAUX	K7			
	VCCAUX	M9			
	VCCAUX	P5			
	VCCAUX	P10			
	VCCAUX	P14			
	VCCIO0	B5			
	VCCIO0	B10			
	VCCIO0	B15			
	VCCIO0	D7			
	VCCIO0	D13			
	VCCIO0	E10			
	VCCIO1	E17			
	VCCIO1	G15			
	VCCIO1	J14			
	VCCIO1	J17			
	VCCIO1	M15			
	VCCIO1	R17			
	VCCIO2	P9			
	VCCIO2	R6			
	VCCIO2	R12			
	VCCIO2	U4			
	VCCIO2	U9			
	VCCIO2	U14			
	VCCIO3	E2			
	VCCIO3	G4			
	VCCIO3	J2			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
	VCCIO3	J5			
	VCCIO3	M4			
	VCCIO3	R2			
	VSS	A1			
	VSS	A18			
	VSS	B7			
	VSS	B13			
	VSS	C3			
	VSS	C16			
	VSS	D5			
	VSS	D10			
	VSS	E15			
	VSS	G2			
	VSS	G5			
	VSS	G12			
	VSS	G17			
	VSS	H8			
	VSS	H10			
	VSS	J4			
	VSS	J9			
	VSS	J11			
	VSS	J15			
	VSS	K8			
	VSS	K10			
	VSS	L9			
	VSS	L11			
	VSS	M2			
	VSS	M6			
	VSS	M17			
	VSS	N13			
	VSS	R1			
	VSS	R4			
	VSS	R9			
	VSS	R14			
	VSS	R18			
	VSS	T16			
	VSS	U6			
	VSS	U12			
	VSS	V1			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
	VSS	V18			

2.2.2 Thermal Resistance

Table 2-4 Thermal Resistance

θJA(℃/W) (Flow: 0m/s)	θJB (℃/W)	θJC (℃/W)	θJA(℃/W) (Flow: 1m/s)	θJA(℃/W) (Flow: 2m/s)
18.1	9.5	8.0	15.3	14.3

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