PK02009_PGL50H_FBG484

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.1	12.07.2021	Initial release

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
POD	Package Outline Drawing

Table of Contents

Tables

Figures

Chapter 1 Introduction to Packaging

PGL50H_FBG484 uses a Wire-Bond BGA type of packaging. Package size: 23x23mm; Number of balls: 484; Ball pitch: 1.0mm; Maximum package thickness: 2.4mm

Chapter 2 Package Dimension

Table 2-1 Dimensional Values

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	2.00	2.20	2.40	c	0.51	0.56	0.61
A1	0.37	0.47	0.57	e	-	1.0	-
A2	1.12	1.17	1.22	b	0.50	0.60	0.70
D	22.8	23.0	23.2	aaa	-	-	0.20
E	22.8	23.0	23.2	ccc	-	-	0.20
D1	-	21.0	-	ddd	-	-	0.15
E1	-	21.0	-	eee	-	-	0.25
D2	19.30	19.5	19.70	D3	-	14.7	-
E2	19.30	19.5	19.70	E3	-	14.7	-

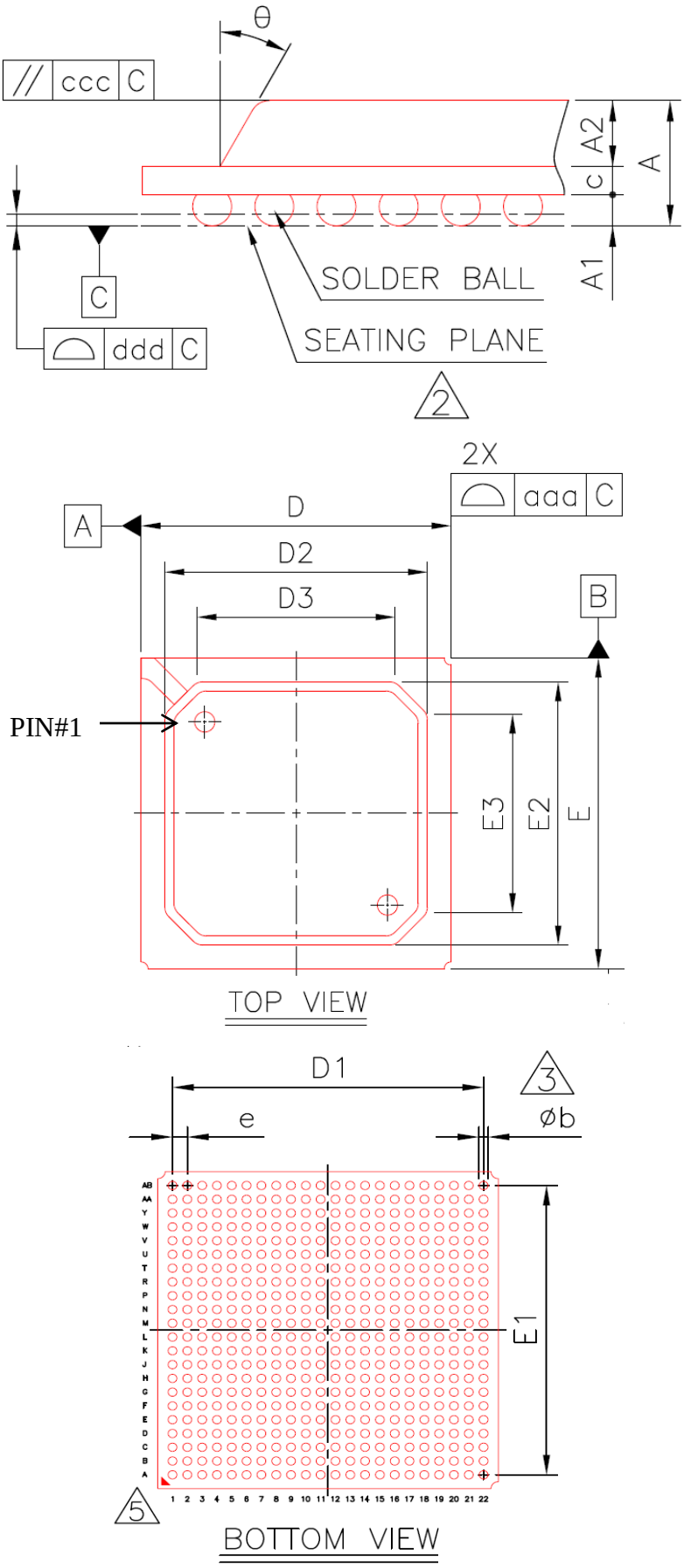

Figure 2-1 Package Outline Dimension (POD)

Note: Pin #1 is the pin 1 position of the chip.

Chapter 3 Pin Definitions

PGL50H_FBG484 has 296 user IOs.

Table 3-1 Product Pin Definitions

PIN name	PIN type	PIN description
General PIN		
DIFFIO_[0,1,2,3]_[0…n][N,P]	I/O	General IO: (1) "DIFFIO" indicates the pin supports differential input/output and can be used for transmitting and receiving LVDS signals; (2) "B[0,1,2,3]" indicates bank numbers; (3) "[0…n]" indicates the number of programmable I/O pairs in a bank; (4) In "[N,P]", "P" indicates the positive end of the differential pair and "N" indicates the negative end; (5) Before or during configuration, when IO_STATUS_C=0, enable internal pull-up resistors, when IO_STATUS_C=1, disable internal pull-up resistors; (6) In user mode, Unused I/Os default to PLLDOWN, but can be set to PLLUP, PLLDOWN, or UNUSED via bitstream;
DIFFI_[0,1,2,3]_[0…n]_[N,P]	I/O	**General** IO: (1) "DIFFI" indicates the pin only supports differential input and can receive differential input signals; (2) "B[0,1,2,3]" indicates bank numbers; (3) "[0…n]" indicates the number of programmable I/O pairs in a bank; (4) In "[N,P]", "P" indicates the positive end of the differential pair and "N" indicates the negative end; (5) Before or during configuration, when IO_STATUS_C=0, enable internal pull-up resistors, when IO_STATUS_C=1, disable internal pull-up resistors; (6) In user mode, Unused I/Os default to PLLDOWN, but can be set to PLLUP, PLLDOWN, or UNUSED via bitstream;
Multiplexed Pin		
Configurable Multiplexed PIN		
MODE_1	input	Multi-function configuration input pin, used for selecting between master and slave configuration modes: (1) MODE_1=0, master mode; (2) MODE_1=1, slave mode.
MODE_0	input	Multi-function configuration input pin, used for selecting between parallel and serial configuration modes: (1) MODE_0=0, parallel configuration; (2) MODE_0=1, serial configuration.
INIT_FLAG_N	Bidirectional (open-drain)	Initialization and configuration status pin: (1) When it is low, it indicates that the FPGA's internal

PIN name	PIN type	PIN description
		CRAM is being cleared, and this pin will be released by internal control upon completion. (2) If this pin is pulled low externally, it will delay the configuration process; (3) If this pin is low during configuration, it indicates an internal configuration error occurred; (4) This pin is an open-drain output and should be connected to VCCIO2 via an external pull-up resistor.
CFG_CLK	input, output	Multi-function configuration clock pin: (1) In the slave mode, this pin serves as a clock input to obtain configuration data from external sources; (2) In the master mode, this pin serves as a clock output to obtain configuration data from external sources; (3) When the clock is not needed (such as in the JTAG mode), this pin is in the High-Z state.
ECCLK	input	Multi-function configuration clock pin: Optional external configuration clock input pin in the master mode
CS_N	inpu, output	Multi-function configuration pin: (1) In the Slave Parallel configuration mode, this pin enables the configuration data interface when it is low; (2) In the SPI x1 mode, when this pin is connected to the Slave Data input interface of the SPI Flash, FPGA will send instructions and initial address to the SPI Flash; (3) In the SPI x2 and x4 modes, it is connected to the SPI flash's IO0 as the [0]th bit of the data bus.
CSO_N	output	Multi-function configuration pin: (1) In the Slave parallel configuration mode, this pin serves as cascaded chip select signal output; (2) In the master SPI mode, this pin serves as the chip select signal output.
D0	input	Multi-function configuration pin: (1) In the SPI x1 mode, this pin connects to the Slave Data output interface of the SPI Flash, and FPGA receives serial data from the SPI Flash, i.e., Master Input/Slave Output; (2) In the SPI x2 and x4 modes, this pin also serves as the [1]st bit of the SPI data bus; (3) In the parallel or BPI mode, this pin serves as the lowest bit of the data bus (4) In the Slave Serial mode, this pin serves as data input.
D[1,2]	inpu, output	Multi-function configuration pin: (1) In the SPI x2 and x4 modes, pin D[1] serves as the [2]nd bit connected to SPI flash's IO2, pin D[2] as the [3]rd bit connected to SPI flash's IO3; (2) In the parallel mode, this pin serves as the [1:2] bits of the data bus.
D[3, 4, 5…15]	inpu, output	Multi-function configuration pin: (1) In the Slave Parallel mode with x8 width, D[7:3] serves as the [7:3]th bit of the data bus; (2) In the Slave Parallel mode with x16 width, D[15:3] serves as the [15:3]th bit of the data bus.
RWSEL	input	Multi-function configuration pin, for selecting the read/write input in the Slave Parallel configuration mode:

PIN name	PIN type	PIN description
		(1) When it is high, the Slave Parallel configuration mode reads data from the data bus; (2) When it is low, the Slave Parallel configuration mode writes data to the data bus; (3) Read and write can be switched only when CS_N is high.
DOUT_BUSY	output	Multi-function configuration pin: (1) During readback in the Slave Parallel mode, this pin indicates the device status; It indicates the data read from the bus is invalid when high; (2) In the Slave Serial configuration mode, this pin serves as cascaded data output, and the data is valid on the falling edge of CFG_CLK; (3) In the SPI configuration mode, this pin serves as cascaded data output, and the data is valid on the falling edge of CFG_CLK.
IO_STATUS_C	input	Multi-function configuration pin, used for controlling whether the pull-up resistors for all user IOs are enabled during the configuration process: (1) When it is set to "0", the internal pull-up resistors for user IOs are enabled before or during configuration; (2) When it is set to "1", the internal pull-up resistors for user IOs are disabled before or during configuration; (3) This pin must not be left floating before or during configuration.
ADR[0, 1, …, 25], BFWE_N, BFOE_N, BFCE_N, BHDC, BLDC	output	Multi-function configuration pin, signals related to BPI configuration mode, This device does not support BPI configuration mode.
Clock Pin		
GCLK[0,1,2,3…,30,31]	input	Dedicated global clock pin. Can also serve as a general user I/O, 8 PADs for each bank When it serves as a differential clock input, GCLK[1,3,5,…,27,29,31] are the internal valid input.
PLL[1,2,3,4]_CLK[0,1,2,…,13,14,15]	input	Optional PLL reference clock input, PLL can directly input the clock from these pins. Optional PLL feedback clock input, PLL can externally feedback the clock from these pins. Also used as general user I/Os.
Reference Pin		
VREF_[B0,B1,B2,B3]	input	External reference voltage pin, for providing reference voltage input for each BANK.
Dedicated Pin		
CFG_DONE	Bidirectional (open-drain)	Dedicated configuration status pin. Serves as a status output,driven low before or during configuration..Once all configuration data are correctly received and the start-up timing is commenced, this pin is released.
RST_N	input	Dedicated configuration pin, internally weak pull-up, for restarting the configuration process, active-low. It is recommended that users externally pull up the RST_N with a resistor when using this pin. When this pin is low, the FPGA enters a reset state, and all IOs are in the High-Z state.
TCK	input	Dedicated JTAG test clock input pin
TMS	input	Dedicated JTAG test mode selection input pin

PIN name	PIN type	PIN description
TDI	input	Dedicated JTAG test data input pin
TDO	output	Dedicated JTAG test data output pin
HSST Pin		
PAD_TX_SD[P,N] [0,1,2,3]	output	Differential outputs of HSST. Each HSST has 4 pairs
PAD_RX_SD[P,N] [0,1,2,3]	input	Differential inputs of HSST. Each HSST has 4 pairs
PAD_REFCLK[P,N] _[0,1]	input	HSST PLL reference clock differential input.
PAD_PLL_TEST_0	input, output	HSST precise reference resistors and HSST PLL test outputs. Requires an external 2k ohm pull-down resistor with a precision of ±1% and a switch; the switch is turned on during the test and turned off when not in the test.
Power Pin, Ground Pin		
VCC	POWER	Core power supply, 1.2V. Power supply for core logic
VCCAUX	POWER	Auxiliary power, 3.3V.
VCCEFUSE	POWER	eFuse power pin; should be used in the following two situations: When the configuration of eFuse function is needed, this pin is connected to 3.3V power and should be powered up according to the recommended power-on sequence. After configuration, the voltage can be maintained at 3.3V or grounded after powering down according to the power-down sequence requirements; it should not be left floating. If the configuration of eFuse function is not needed, this pin should be grounded.
VCCIO[0,1,2,3]	POWER	IO BANK power
VCCA_LANE	POWER	1.2V HSST Lane Power Supply
VCCA_PLL_0	POWER	1.2V HSST PLL0 Power Supply. For unused HSST, connect to VSS at the board level
VCCA_PLL_1	POWER	1.2V HSST PLL1 Power Supply. For unused HSST, connect to VSS at the board level
VSSA	GROUND	HSST analog ground; can be connected to VSS
VSS	GROUND	GND
Reserved Pin		
NC		No need to be connected, left floating
CMPCS_B		No need to be connected, left floating
STAND_BY		No need to be connected, left floating

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