PK02008_PGL25G_FBG484

(V1.3)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.3	28.01.2021	Initial release

About this Manual

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Terms and Abbreviations	Meaning
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Chapter 1 Introduction to Packaging

PGL25G_FBG484 uses a Wire-Bond BGA type of packaging. Its package size is 23mmx23mm, with 484 solder balls, a pitch of 1.0mm and a maximum package thickness of 2.36mm.

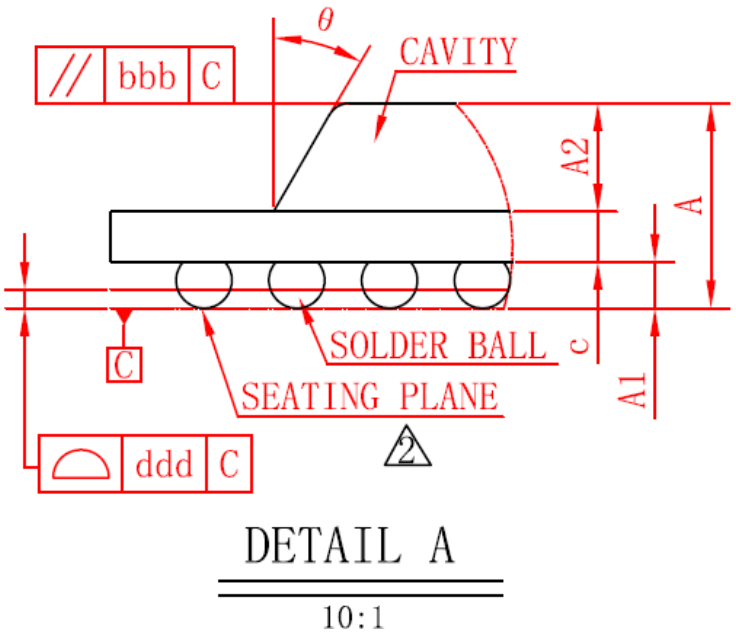
Chapter 2 Package Dimension and Pins

2.1 Package Outline Dimension

Table 2-1 Dimensional Values

Unit: mm

Dimension Symbols	Values			Dimension Symbols	Values		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	2.06	2.21	2.36	c	0.50	0.54	0.58
A1	0.45	0.50	0.55	e	-	1.0	-
A2	1.12	1.17	1.22	b	0.55	0.60	0.65
D	22.8	23.0	23.2	aaa	-	-	0.20
E	22.8	23.0	23.2	bbb	-	-	0.25
D1	-	21.0	-	ddd	-	-	0.20
E1	-	21.0	-	eee	-	-	0.25



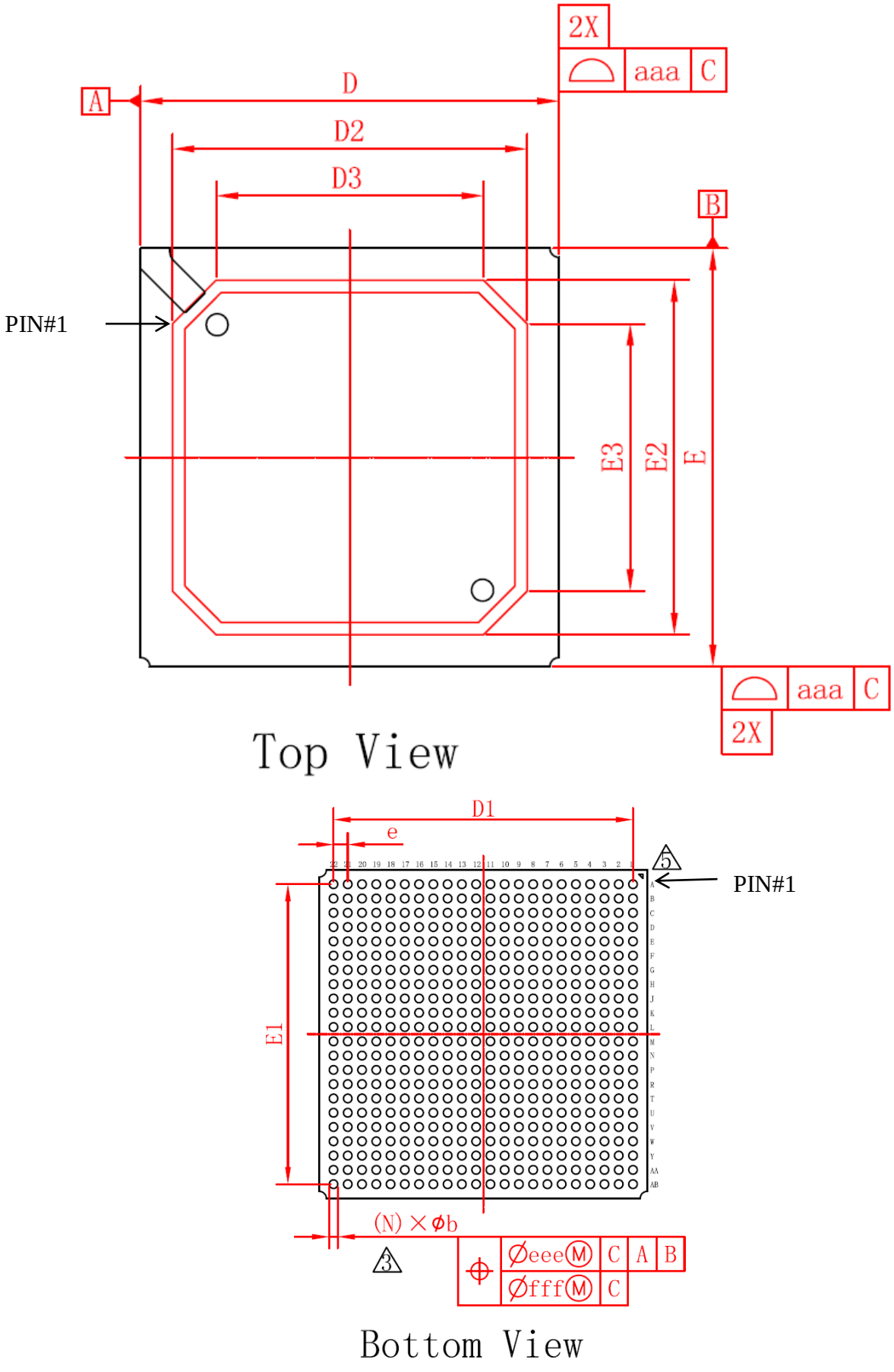


Figure 2-1 Package Outline Dimension (POD)

Note: Pin #1 is the pin 1 position of the chip

2.2 Pin Description

PGL25G_FBG484 has 308 user IOs.

Table 2-2 Product Pin Definitions

PIN name	PIN type	PIN description
General IO PIN		
IO	I/O	**General** IO Before or during configuration, when IO_STATUS_C=0, enable internal pull-up; when IO_STATUS_C=1, disable internal pull-up In user mode, unused IOs default to pull-down, but can also be configured by the user as pull-up, pull-down, or float via bitstream
-- Multi-function Configuration Pin		
MODE_1	input	Multi-function configuration input pin, used for selecting between master and slave configuration modes; MODE_1=0 master mode; MODE_1=1 slave mode
MODE_0	input	Multi-function configuration input PAD, used for selecting between parallel and serial configuration modes MODE_0=0 parallel configuration; MODE_0=1 serial configuration
INIT_FLAG_N	Bidirectional (open-drain)	When it is low, it indicates that the FPGA's internal CRAM is being cleared, and this pin will be released by internal control upon completion. If this pin is pulled low externally, it will delay the configuration process If this pin is low during configuration, it indicates an internal configuration error occurred
CFG_CLK	inpu, output	Configuration Clock pin. In the slave mode, this pin serves as a clock input to obtain configuration data from external sources; In the master mode, this pin serves as a clock output to obtain configuration data from external sources; When the clock is not needed (such as in the JTAG mode), this pin is high-z.
ECCLK	input	Optional external configuration clock input pin in the master mode
CS_N	inpu, output	Multi-function Configuration pin. (1) In the Slave Parallel configuration mode, this pin enables the parallel configuration mode data interface at a low level; (2) In the SPI x1 mode, when this pin is connected to the Slave Data input interface of the SPI Flash, FPGA will send instructions and initial address to the SPI Flash; (3) In the SPI x2 and x4 modes, it is connected to the SPI flash's IO0 as the [0]th bit of the data bus.
CSO_N	output	Multi-function Configuration pin (1) In the slave parallel configuration mode, it serves as the cascaded chip select signal output; (2) In the master SPI mode, it serves as the chip select signal output.
D0	input	Multi-function configuration data pin (1) In the SPI x1 mode, this pin connects to the Slave Data output interface of the SPI Flash, and FPGA receives serial data from the SPI Flash, i.e., Master Input/Slave Output; (2) In the SPI x2 and x4 modes, this pin also serves as the

PIN name	PIN type	PIN description
		[1]st bit of the SPI data bus; (3) In the Parallel or BPI mode, this pin serves as the lowest bit of the data bus; (4) In the Slave Serial mode, this pin serves as data input.
D[1,2]	inpu, output	Multi-function configuration data pin (1) In the SPI x2 and x4 modes, pin D[1] serves as the [2]nd bit connected to SPI flash's IO2, pin D[2] as the [3]rd bit connected to SPI flash's IO3; (2) In the slave parallel or BPI mode, this pin serves as the [2:1] bits of the data bus.
D[3、5…15]	inpu, output	Multi-function configuration data pin In the Slave Parallel or BPI mode with x8 width, D[7:3] serves as the [7:3]th bit of the data bus; In the Slave Parallel or BPI mode with x16 width, D[15:3] serves as the [15:3]th bit of the data bus.
RWSEL	input	Multi-function Configuration pin. For selecting the read/write input in the Slave Parallel configuration mode (high for read and low for write). (1) When it is high, the Slave Parallel configuration mode reads data from the data bus; (2) When it is low, the Slave Parallel configuration mode writes data to the data bus; (3) Read and write can be switched only when CS_N is high.
DOUT_BUSY	output	Multi-function Configuration pin. (1) During readback in the slave Parallel mode, this pin indicates the device status. It indicates the data read from the bus is invalid when high; (2) In the Serial configuration mode, this pin serves as cascaded data output, and the data is valid on the falling edge of CFG_CLK; (3) In the SPI configuration mode, this pin serves as cascaded data output, and the data is valid on the falling edge of CFG_CLK.
IO_STATUS_C	input	Multi-function input pin; used for controlling whether the pull-up resistors for all user IOs are enabled during the configuration process. (1) When the signal is 0, the internal IO pull-up resistors for user IOs are enabled before or during configuration; (2) When the signal is 1, the internal IO pull-up resistors,for user IOs are disable before or during configuration.
ADR[0, 1, …, 25]	output	Multi-function configuration pin, address output in BPI configuration mode. (1) After configuration is completed, it can be used as a user IO
BFWE_N	output	Multi-function configuration pin, used for providing a low-level write enable signal for parallel NOR FLASH in the BPI configuration mode.
BFOE_N	output	Multi-function configuration pin, used for providing a low-level output enable signal for parallel NOR FLASH in the BPI configuration mode.
BFCE_N	output	Multi-function configuration pin, used for providing a low-level chip select control signal for parallel NOR FLASH in the BPI configuration mode.
BHDC	output	In BPI mode, there is high output during the configuration
BLDC	output	In BPI mode, there is low output during the configuration
-- Clock, PLL, Oscillator Multi-function Pin		

PIN name	PIN type	PIN description
GCLK[0,1,2,3…,30,31]	input	Dedicated Global Clock Input pin. Can also serve as a general user I/O, 8 pins for each bank When serves as differential clock input, GCLK[1,3,5,…,27,29,31] are the internal valid input
PLL[0,1,2,3]_CLK[0,1,2,…,13,14,15]	input	Optional PLL reference clock input, PLL can directly input a clock from these pins; Optional PLL feedback clock input, PLL can externally feedback the clock from these pads.; Can also be used as general user I/Os.
--Differential Pin		
DIFFIO_[0,1,2,3]_[0…n][N,P]	I/O, true differential input/output	Transmitting and receiving differential signals. Used for transmitting and receiving LVDS signals. The suffix "P" indicates the "positive" signal and the suffix "N" indicates the "negative" signal. If not used as differential signal pins, these pins can serve as general user I/Os. Each IOBD tile is provided with a pair of differential signals.
DIFFI_[0,1,2,3]_[0…n]_[N,P]	I/O, true differential input	Differential signal receive pin. Can be used for receiving differential input signals. The suffix "P" indicates the "positive" signal and the suffix "N" indicates the "negative" signal. If not used as differential input pins, these pins can be used as general user I/Os; each IOBS tile is provided with a pair of differential inputs.
-- External Memory Interface Pin		
DQS[0,1,2,3,4,5][#]_[1,3]	DQS	Multi-function pin. Used to connect to the DQS/DQS# signal pins of external memory. Also used as general user I/Os.
DQ[0,1,2,3,4,5][#]_[1,3]	DQ	Multi-function pin, can connect to the DQ signal pins of external memory. Also used as general user I/Os.
Dedicated Pin		
--Configuration Pin, JTAG Pin		
CFG_DONE	Bidirectional (open-drain)	Dedicated pin for configuration state. Serves as a status output, driven low before or during configuration. Once all configuration data are correctly received and the start-up timing is commenced, this pin is released.
RST_N	input	Dedicated configuration input pin, internally weak pull-up, for restarting the configuration process, active-low. It is recommended that users externally pull up the RST_N with a resistor when using this pin. When this pin is low, the FPGA enters a reset state, and all IOs are in the High-z state.
CMPCS_B		No need to be connected, left floating
STAND_BY		No need to be connected, left floating
TCK	input	Dedicated JTAG test clock input pin
TMS	input	Dedicated JTAG test mode selection input pin
TDI	input	Dedicated JTAG test data input pin.
TDO	output	Dedicated JTAG test data output pin.
--Reference Pin		
VREF_[B0,B1,B2,B3]	input	External reference voltage pin, one for each bank. Provide reference voltage input for each BANK When a VREF is used, all VREFs in that bank must be connected

PIN name	PIN type	PIN description
Power Pin, Ground Pin		
VCC	POWER	Core power supply, 1.2V. Power supply for core logic
VCCAUX	POWER	3.3V auxiliary power supply for IOB, LDO, EFUSE, dedicated configuration IOB, and other modules
VCCIO[0,1,2,3]	POWER	IO BANK power
VSS	GROUND	GND relative to VDD11 & VDD33 & VDDIO

2.2.1 Pin Name list

Table 2-3 Pin Name List

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B0	DIFFIO_B0_0P/IO_STATUS_C	A3	IO_1_P	90.4127	
B0	DIFFIO_B0_0N/VREF_B0	A4	IO_1_N	94.0098	
B0	DIFFIO_B0_1P	C5	IO_2_P	84.0695	
B0	DIFFIO_B0_1N	A5	IO_2_N	87.537	
B0	DIFFIO_B0_2P	D6	IO_3_P	68.8465	
B0	DIFFIO_B0_2N	C6	IO_3_N	66.4523	
B0	DIFFIO_B0_3P	B6	IO_4_P	78.9713	
B0	DIFFIO_B0_3N	A6	IO_4_N	81.5087	
B0	DIFFIO_B0_4P	C7	IO_5_P	80.8438	
B0	DIFFIO_B0_4N	A7	IO_5_N	80.6154	
B0	DIFFIO_B0_5P	B8	IO_6_P	73.5075	
B0	DIFFIO_B0_5N	A8	IO_6_N	76.2749	
B0	DIFFIO_B0_6P	D9	IO_7_P	64.5277	
B0	DIFFIO_B0_6N	C8	IO_7_N	64.5934	
B0	DIFFIO_B0_7P	C9	IO_8_P	76.5757	
B0	DIFFIO_B0_7N/VREF_B0	A9	IO_8_N	79.2284	
B0	DIFFIO_B0_8P	E8	IO_9_P	59.9222	
B0	DIFFIO_B0_8N	F8	IO_9_N	63.0216	
B0	DIFFIO_B0_9P	G8	IO_10_P	60.7617	
B0	DIFFIO_B0_9N	F9	IO_10_N	57.9881	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B0	DIFFIO_B0_10P	G9	IO_11_P	72.3405	
B0	DIFFIO_B0_10N	H10	IO_11_N	72.5869	
B0	DIFFIO_B0_11P	E10	IO_12_P	45.9132	
B0	DIFFIO_B0_11N	F10	IO_12_N	45.8221	
B0	DIFFIO_B0_12P	G11	IO_13_P	74.615	
B0	DIFFIO_B0_12N	H11	IO_13_N	75.8231	
B0	DIFFIO_B0_13P	D7	IO_14_P	76.4221	
B0	DIFFIO_B0_13N	D8	IO_14_N	75.8829	
B0	DIFFIO_B0_14P	D10	IO_15_P	66.5564	
B0	DIFFIO_B0_14N	C10	IO_15_N	64.0874	
B0	DIFFIO_B0_15P/GCLK19/PLL0_CLK0/PLL1_CLK0	B10	IO_16_P	76.4929	
B0	DIFFIO_B0_15N/GCLK18/PLL0_CLK1/PLL1_CLK1	A10	IO_16_N	79.4999	
B0	DIFFIO_B0_16P/GCLK17/PLL0_CLK2/PLL1_CLK2	C11	IO_17_P	80.6387	
B0	DIFFIO_B0_16N/GCLK16/PLL0_CLK3/PLL1_CLK3	A11	IO_17_N	79.07	
B0	DIFFIO_B0_17P/GCLK15/PLL0_CLK4/PLL1_CLK4	D11	IO_18_P	56.9773	
B0	DIFFIO_B0_17N/GCLK14/PLL0_CLK5/PLL1_CLK5	C12	IO_18_N	59.678	
B0	DIFFIO_B0_18P/GCLK13/PLL0_CLK6/PLL1_CLK6	B12	IO_19_P	72.3489	
B0	DIFFIO_B0_18N/GCLK12/PLL0_CLK7/PLL1_CLK7	A12	IO_19_N	75.3283	
B0	DIFFIO_B0_19P	C13	IO_20_P	77.9851	
B0	DIFFIO_B0_19N/VREF_B0	A13	IO_20_N	79.9775	
B0	DIFFIO_B0_20P	E12	IO_21_P	54.8928	
B0	DIFFIO_B0_20N	D12	IO_21_N	55.8436	
B0	DIFFIO_B0_21P	H12	IO_22_P	65.8887	
B0	DIFFIO_B0_21N	F12	IO_22_N	64.6324	
B0	DIFFIO_B0_22P	F13	IO_23_P	51.4399	
B0	DIFFIO_B0_22N	D13	IO_23_N	55.0696	
B0	DIFFIO_B0_23P	H13	IO_24_P	63.7608	
B0	DIFFIO_B0_23N	G13	IO_24_N	61.553	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
				6	
B0	DIFFIO_B0_24P	E14	IO_25_P	74.655 5	
B0	DIFFIO_B0_24N	F15	IO_25_N	75.435 9	
B0	DIFFIO_B0_25P	F14	IO_26_P	60.975	
B0	DIFFIO_B0_25N	H14	IO_26_N	63.525 9	
B0	DIFFIO_B0_26P	D14	IO_27_P	61.369 8	
B0	DIFFIO_B0_26N	C14	IO_27_N	61.608 5	
B0	DIFFIO_B0_27P	B14	IO_28_P	75.786 3	
B0	DIFFIO_B0_27N	A14	IO_28_N	77.307 3	
B0	DIFFIO_B0_28P	C15	IO_29_P	81.049 2	
B0	DIFFIO_B0_28N	A15	IO_29_N	83.734 6	
B0	DIFFIO_B0_29P	D15	IO_30_P	63.067 1	
B0	DIFFIO_B0_29N/VREF_B0	C16	IO_30_N	65.828 4	
B0	DIFFIO_B0_30P	B16	IO_31_P	86.261 9	
B0	DIFFIO_B0_30N	A16	IO_31_N	86.892 2	
B0	DIFFIO_B0_31P	C17	IO_32_P	86.872 3	
B0	DIFFIO_B0_31N	A17	IO_32_N	88.492	
B0	DIFFIO_B0_32P	B18	IO_33_P	86.361 7	
B0	DIFFIO_B0_32N	A18	IO_33_N	90.876 6	
B0	DIFFIO_B0_33P	E16	IO_34_P	62.904 7	
B0	DIFFIO_B0_33N	D17	IO_34_N	64.451 3	
B1	DIFFI_B1_0P/ADR25	C19	IO_35_P	83.180 1	DQ0_B1
B1	DIFFI_B1_0N/ADR24/VREF_B1	B20	IO_35_N	87.257 3	DQ0_B1
B1	DIFFI_B1_1P	G16	IO_36_P	62.374 9	DQ0_B1
B1	DIFFI_B1_1N	G17	IO_36_N	63.556 8	DQ0_B1
B1	DIFFI_B1_2P	F16	IO_37_P	64.872 7	DQ0_B1
B1	DIFFI_B1_2N	F17	IO_37_N	67.905 5	DQ0_B1
B1	DIFFI_B1_3P	B21	IO_38_P	103.43 7	DQ0_B1

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B1	DIFFI_B1_3N	B22	IO_38_N	104.126	DQ0_B1
B1	DIFFI_B1_4P	A20	IO_39_P	125.8	DQS0_B1
B1	DIFFI_B1_4N	A21	IO_39_N	121.042	DQS0#_B1
B1	DIFFI_B1_5P	K16	IO_40_P	65.5831	DQ0_B1
B1	DIFFI_B1_5N	J16	IO_40_N	66.2539	DQ0_B1
B1	DIFFI_B1_6P	H16	IO_41_P	47.4766	DQ0_B1
B1	DIFFI_B1_6N	H17	IO_41_N	44.0017	DQ0_B1
B1	DIFFI_B1_7P/ADR23	D19	IO_42_P	85.8421	DQ1_B1
B1	DIFFI_B1_7N/ADR22	D20	IO_42_N	89.9259	DQ1_B1
B1	DIFFI_B1_8P/ADR21	F18	IO_43_P	67.687	DQ1_B1
B1	DIFFI_B1_8N/ADR20	F19	IO_43_N	69.3975	DQ1_B1
B1	DIFFI_B1_9P/ADR19	D21	IO_44_P	99.4534	DQ1_B1
B1	DIFFI_B1_9N/ADR18	D22	IO_44_N	100.713	DQ1_B1
B1	DIFFI_B1_10P/ADR17	C20	IO_45_P	114.096	DQS1_B1
B1	DIFFI_B1_10N/ADR16	C22	IO_45_N	118.625	DQS1#_B1
B1	DIFFI_B1_11P/ADR15	G19	IO_46_P	78.564	DQ1_B1
B1	DIFFI_B1_11N/ADR14	F20	IO_46_N	77.169	DQ1_B1
B1	DIFFI_B1_12P/ADR13	H19	IO_47_P	58.8266	DQ1_B1
B1	DIFFI_B1_12N/ADR12	H18	IO_47_N	61.4938	DQ1_B1
B1	DIFFI_B1_13P/ADR11	E20	IO_48_P	96.6377	DQ2_B1
B1	DIFFI_B1_13N/ADR10	E22	IO_48_N	94.9631	DQ2_B1
B1	DIFFI_B1_14P/ADR9	J17	IO_49_P	48.6591	DQ2_B1
B1	DIFFI_B1_14N/ADR8	K17	IO_49_N	45.9391	DQ2_B1
B1	DIFFI_B1_15P/ADR7	F21	IO_50_P	90.3719	DQS2_B1
B1	DIFFI_B1_15N/ADR6	F22	IO_50_N	90.4121	DQS2#_B1
B1	DIFFI_B1_16P/ADR5	H20	IO_51_P	68.9031	DQ2_B1
B1	DIFFI_B1_16N/ADR4	J19	IO_51_N	68.4009	DQ2_B1
B1	DIFFI_B1_17P	G20	IO_52_P	84.6248	DQ2_B1

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B1	DIFFI_B1_17N	G22	IO_52_N	90.185	DQ2_B1
B1	DIFFI_B1_18P/GCLK11/PLL0_CLK8/PLL1_CLK8	K20	IO_53_P	61.1861	DQ2_B1
B1	DIFFI_B1_18N/GCLK10/PLL0_CLK9/PLL1_CLK9	K19	IO_53_N	59.4577	DQ2_B1
B1	DIFFI_B1_19P/GCLK9/PLL0_CLK10/PLL1_CLK10	H21	IO_54_P	91.0527	DQ2_B1
B1	DIFFI_B1_19N/GCLK8/PLL0_CLK11/PLL1_CLK11	H22	IO_54_N	93.4451	DQ2_B1
B1	DIFFI_B1_20P	M18	IO_55_P	52.5583	DQ3_B1
B1	DIFFI_B1_20N	M17	IO_55_N	53.0237	DQ3_B1
B1	DIFFI_B1_21P/GCLK7/PLL2_CLK8/PLL3_CLK8	M20	IO_56_P	63.8137	DQ3_B1
B1	DIFFI_B1_21N/GCLK6/PLL2_CLK9/PLL3_CLK9	L19	IO_56_N	62.2692	DQ3_B1
B1	DIFFI_B1_22P/GCLK5/PLL2_CLK10/PLL3_CLK10	J20	IO_57_P	84.0454	DQ3_B1
B1	DIFFI_B1_22N/GCLK4/PLL2_CLK11/PLL3_CLK11	J22	IO_57_N	87.599	DQ3_B1
B1	DIFFI_B1_23P/ADR3	K21	IO_58_P	81.2234	DQ3_B1
B1	DIFFI_B1_23N/ADR2	K22	IO_58_N	83.3433	DQ3_B1
B1	DIFFI_B1_24P/ADR1	L20	IO_59_P	77.7412	DQS3_B1
B1	DIFFI_B1_24N/ADR0	L22	IO_59_N	81.1318	DQS3#_B1
B1	DIFFI_B1_25P/BFCE_N	M21	IO_60_P	75.2848	DQ3_B1
B1	DIFFI_B1_25N/BFOE_N	M22	IO_60_N	76.8659	DQ3_B1
B1	DIFFI_B1_26P/BFWE_N	N20	IO_61_P	76.6917	DQ3_B1
B1	DIFFI_B1_26N/BLDC	N22	IO_61_N	77.7277	DQ3_B1
B1	DIFFI_B1_27P	P18	IO_62_P	64.3613	DQ4_B1
B1	DIFFI_B1_27N	P17	IO_62_N	67.0167	DQ4_B1
B1	DIFFI_B1_28P/BHDC	P21	IO_63_P	75.1576	DQ4_B1
B1	DIFFI_B1_28N	P22	IO_63_N	76.4582	DQ4_B1
B1	DIFFI_B1_29P	R20	IO_64_P	82.0614	DQ4_B1
B1	DIFFI_B1_29N	R22	IO_64_N	95.69	DQ4_B1
B1	DIFFI_B1_30P	T21	IO_65_P	89.1925	DQS4_B1
B1	DIFFI_B1_30N	T22	IO_65_N	90.3413	DQS4#_B1
B1	DIFFI_B1_31P	U20	IO_66_P	101.187	DQ4_B1

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B1	DIFFI_B1_31N	U22	IO_66_N	100.288	DQ4_B1
B1	DIFFI_B1_32P	V21	IO_67_P	95.693	DQ4_B1
B1	DIFFI_B1_32N	V22	IO_67_N	100.101	DQ4_B1
B1	DIFFI_B1_33P	M19	IO_68_P	69.1401	DQ5_B1
B1	DIFFI_B1_33N/VREF_B1	N19	IO_68_N	69.9024	DQ5_B1
B1	DIFFI_B1_34P	P19	IO_69_P	61.586	DQ5_B1
B1	DIFFI_B1_34N	P20	IO_69_N	62.9481	DQ5_B1
B1	DIFFI_B1_35P	W20	IO_70_P	108.213	DQS5_B1
B1	DIFFI_B1_35N	W22	IO_70_N	106.359	DQS5#_B1
B1	DIFFI_B1_36P	L17	IO_71_P	91.2477	DQ5_B1
B1	DIFFI_B1_36N	K18	IO_71_N	91.3569	DQ5_B1
B1	DIFFI_B1_37P	U19	IO_72_P	88.0645	DQ5_B1
B1	DIFFI_B1_37N	V20	IO_72_N	86.6711	DQ5_B1
B1	DIFFI_B1_38P	V19	IO_73_P	88.4046	DQ5_B1
B1	DIFFI_B1_38N	V18	IO_73_N	87.9666	DQ5_B1
B1	DIFFI_B1_39P	T19	IO_74_P	62.381	DQ5_B1
B1	DIFFI_B1_39N/DOUT_BUSY	T20	IO_74_N	63.3191	DQ5_B1
B2	DIFFIO_B2_0N/CSO_N	T5	IO_75_N	59.7402	
B2	DIFFIO_B2_0P/INIT_FLAG_N	T6	IO_75_P	62.3633	
B2	DIFFIO_B2_1N/D9	AB2	IO_76_N	107.11	
B2	DIFFIO_B2_1P/D8	AA2	IO_76_P	105.052	
B2	DIFFIO_B2_2N	V5	IO_77_N	64.6978	
B2	DIFFIO_B2_2P	U6	IO_77_P	63.6201	
B2	DIFFIO_B2_3N/D6	Y4	IO_78_N	83.9698	
B2	DIFFIO_B2_3P/D5	W4	IO_78_P	82.1372	
B2	DIFFIO_B2_4N	R7	IO_79_N	53.8559	
B2	DIFFIO_B2_4P	T7	IO_79_P	55.538	
B2	DIFFIO_B2_5N	R8	IO_80_N	61.9991	
B2	DIFFIO_B2_5P	R9	IO_80_P	59.167	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
				8	
B2	DIFFIO_B2_6N	AB3	IO_81_N	106.716	
B2	DIFFIO_B2_6P	Y3	IO_81_P	105.83	
B2	DIFFIO_B2_7N	AB4	IO_82_N	104.774	
B2	DIFFIO_B2_7P	AA4	IO_82_P	99.5946	
B2	DIFFIO_B2_8N	AB5	IO_83_N	98.9006	
B2	DIFFIO_B2_8P	Y5	IO_83_P	96.4785	
B2	DIFFIO_B2_9N	Y6	IO_84_N	78.6251	
B2	DIFFIO_B2_9P	W6	IO_84_P	78.1449	
B2	DIFFIO_B2_10N	V9	IO_85_N	57.6667	
B2	DIFFIO_B2_10P	U9	IO_85_P	57.2469	
B2	DIFFIO_B2_11N/D4	AB6	IO_86_N	94.8369	
B2	DIFFIO_B2_11P/D3	AA6	IO_86_P	92.1234	
B2	DIFFIO_B2_12N/RDWR_B/VREF_B2	AB7	IO_87_N	90.7843	
B2	DIFFIO_B2_12P/D7	Y7	IO_87_P	93.5278	
B2	DIFFIO_B2_13N	Y8	IO_88_N	74.7705	
B2	DIFFIO_B2_13P	W9	IO_88_P	76.1941	
B2	DIFFIO_B2_14N	V7	IO_89_N	70.6826	
B2	DIFFIO_B2_14P	W8	IO_89_P	69.8479	
B2	DIFFIO_B2_15N	AB8	IO_90_N	84.658	
B2	DIFFIO_B2_15P	AA8	IO_90_P	86.1471	
B2	DIFFIO_B2_16N	Y10	IO_91_N	65.8789	
B2	DIFFIO_B2_16P	W10	IO_91_P	63.5888	
B2	DIFFIO_B2_17N	AB9	IO_92_N	88.2775	
B2	DIFFIO_B2_17P	Y9	IO_92_P	83.5827	
B2	DIFFIO_B2_18N	W11	IO_93_N	50.2297	
B2	DIFFIO_B2_18P	V11	IO_93_P	51.575	
B2	DIFFIO_B2_19N/VREF_B2	AB10	IO_94_N	82.3023	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B2	DIFFIO_B2_19P	AA10	IO_94_P	81.0903	
B2	DIFFIO_B2_20N	T11	IO_95_N	53.9066	
B2	DIFFIO_B2_20P	R11	IO_95_P	53.2355	
B2	DIFFIO_B2_21N/GCLK28/PLL2_CLK0/PLL3_CLK0	AB11	IO_96_N	82.1222	
B2	DIFFIO_B2_21P/GCLK29/PLL2_CLK1/PLL3_CLK1	Y11	IO_96_P	82.5613	
B2	DIFFIO_B2_22N/GCLK30/D15/PLL2_CLK2/PLL3_CLK2	AB12	IO_97_N	77.0574	
B2	DIFFIO_B2_22P/GCLK31/D14/PLL2_CLK3/PLL3_CLK3	AA12	IO_97_P	70.9506	
B2	DIFFIO_B2_23N/GCLK0/ECCLK/PLL2_CLK4/PLL3_CLK4	AB13	IO_98_N	80.0401	
B2	DIFFIO_B2_23P/GCLK1/D13/PLL2_CLK5/PLL3_CLK5	Y13	IO_98_P	76.1654	
B2	DIFFIO_B2_24N/GCLK2/PLL2_CLK6/PLL3_CLK6	Y12	IO_99_N	63.5206	
B2	DIFFIO_B2_24P/GCLK3/PLL2_CLK7/PLL3_CLK7	W12	IO_99_P	63.2527	
B2	DIFFIO_B2_25N	AB15	IO_100_N	85.3913	
B2	DIFFIO_B2_25P	Y15	IO_100_P	83.5511	
B2	DIFFIO_B2_26N	Y14	IO_101_N	62.1896	
B2	DIFFIO_B2_26P	W14	IO_101_P	61.8767	
B2	DIFFIO_B2_27N	AB16	IO_102_N	91.0414	
B2	DIFFIO_B2_27P	AA16	IO_102_P	87.6852	
B2	DIFFIO_B2_28N	W13	IO_103_N	59.0104	
B2	DIFFIO_B2_28P	V13	IO_103_P	58.6676	
B2	DIFFIO_B2_29N	W15	IO_104_N	69.2739	
B2	DIFFIO_B2_29P	Y16	IO_104_P	68.876	
B2	DIFFIO_B2_30N/VREF_B2	AB14	IO_105_N	110.393	
B2	DIFFIO_B2_30P	AA14	IO_105_P	111.345	
B2	DIFFIO_B2_31N	AB17	IO_106_N	91.1982	
B2	DIFFIO_B2_31P	Y17	IO_106_P	92.4729	
B2	DIFFIO_B2_32N/D12	AB18	IO_107_N	93.3935	
B2	DIFFIO_B2_32P/D11	AA18	IO_107_P	89.4799	
B2	DIFFIO_B2_33N/D10	V15	IO_108_N	47.076	

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B2	DIFFIO_B2_33P/MODE_1	U15	IO_108_P	48.619	
B2	DIFFIO_B2_34N/D2	U13	IO_109_N	59.3108	
B2	DIFFIO_B2_34P/D1	U14	IO_109_P	61.3257	
B2	DIFFIO_B2_25N	Y18	IO_110_N	74.8229	
B2	DIFFIO_B2_25P	W18	IO_110_P	75.8061	
B2	DIFFIO_B2_36N	AB19	IO_111_N	89.513	
B2	DIFFIO_B2_36P	Y19	IO_111_P	85.411	
B2	DIFFIO_B2_37N/CS_N	AB20	IO_112_N	93.7612	
B2	DIFFIO_B2_37P/D0	AA20	IO_112_P	94.6426	
B2	DIFFIO_B2_38N	AB21	IO_113_N	101.515	
B2	DIFFIO_B2_38P	AA21	IO_113_P	95.2153	
B2	DIFFIO_B2_39N/MODE_0	AA22	IO_114_N	105.278	
B2	DIFFIO_B2_39P/CFG_CLK	Y21	IO_114_P	99.5848	
B3	DIFFI_B3_0N/VREF_B3	B3	IO_115_N	108.953	DQ0_B3
B3	DIFFI_B3_0P	A2	IO_115_P	111.246	DQ0_B3
B3	DIFFI_B3_1N	E6	IO_116_N	66.841	DQ0_B3
B3	DIFFI_B3_1P	E5	IO_116_P	66.2835	DQ0_B3
B3	DIFFI_B3_2N	C4	IO_117_N	88.658	DQ0_B3
B3	DIFFI_B3_2P	D3	IO_117_P	89.5061	DQ0_B3
B3	DIFFI_B3_3N	B1	IO_118_N	116.555	DQ0_B3
B3	DIFFI_B3_3P	B2	IO_118_P	115.12	DQ0_B3
B3	DIFFI_B3_4N	H8	IO_119_N	52.5094	DQS0#_B3
B3	DIFFI_B3_4P	J7	IO_119_P	50.8291	DQS0_B3
B3	DIFFI_B3_5N	E4	IO_120_N	83.6229	DQ0_B3
B3	DIFFI_B3_5P	D5	IO_120_P	83.666	DQ0_B3
B3	DIFFI_B3_6N	K8	IO_121_N	54.7422	DQ0_B3
B3	DIFFI_B3_6P	K7	IO_121_P	57.1282	DQ0_B3
B3	DIFFI_B3_7N	F5	IO_122_N	70.4365	DQ1_B3
B3	DIFFI_B3_7P	G6	IO_122_P	66.8908	DQ1_B3

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B3	DIFFI_B3_8N	C1	IO_123_N	108.212	DQ1_B3
B3	DIFFI_B3_8P	C3	IO_123_P	109.333	DQ1_B3
B3	DIFFI_B3_9N	D1	IO_124_N	99.3136	DQ1_B3
B3	DIFFI_B3_9P	D2	IO_124_P	95.5757	DQ1_B3
B3	DIFFI_B3_10N	E1	IO_125_N	97.345	DQS1#_B3
B3	DIFFI_B3_10P	E3	IO_125_P	93.7631	DQS1_B3
B3	DIFFI_B3_11N	F3	IO_126_N	80.6116	DQ1_B3
B3	DIFFI_B3_11P	G4	IO_126_P	76.6739	DQ1_B3
B3	DIFFI_B3_12N	F1	IO_127_N	90.6475	DQ1_B3
B3	DIFFI_B3_12P	F2	IO_127_P	88.7177	DQ1_B3
B3	DIFFI_B3_13N	H5	IO_128_N	66.5324	DQ2_B3
B3	DIFFI_B3_13P	H6	IO_128_P	70.1393	DQ2_B3
B3	DIFFI_B3_14N	G1	IO_129_N	87.6819	DQ2_B3
B3	DIFFI_B3_14P	G3	IO_129_P	84.594	DQ2_B3
B3	DIFFI_B3_15N	H1	IO_130_N	83.9738	DQS2#_B3
B3	DIFFI_B3_15P	H2	IO_130_P	81.2541	DQS2_B3
B3	DIFFI_B3_16N	H3	IO_131_N	75.466	DQ2_B3
B3	DIFFI_B3_16P	H4	IO_131_P	80.9113	DQ2_B3
B3	DIFFI_B3_17N	J6	IO_132_N	66.9916	DQ2_B3
B3	DIFFI_B3_17P	K6	IO_132_P	63.8945	DQ2_B3
B3	DIFFI_B3_18N/GCLK20/PLL0_CLK12/PLL1_CLK12	J4	IO_133_N	62.8805	DQ2_B3
B3	DIFFI_B3_18P/GCLK21/PLL0_CLK13/PLL1_CLK13	K3	IO_133_P	63.8115	DQ2_B3
B3	DIFFI_B3_19N/GCLK22/PLL0_CLK14/PLL1_CLK14	K4	IO_134_N	57.1965	DQ2_B3
B3	DIFFI_B3_19P/GCLK23/PLL0_CLK15/PLL1_CLK15	K5	IO_134_P	54.2022	DQ2_B3
B3	DIFFI_B3_20N	L6	IO_135_N	42.9535	DQ3_B3
B3	DIFFI_B3_20P	M6	IO_135_P	46.4062	DQ3_B3
B3	DIFFI_B3_21N/GCLK24/PLL2_CLK12/PLL3_CLK12	L4	IO_136_N	62.2763	DQ3_B3
B3	DIFFI_B3_21P/GCLK25/PLL2_CLK13/PLL3_CLK13	M3	IO_136_P	63.4977	DQ3_B3

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
B3	DIFFI_B3_22N/GCLK26/PLL2_CLK14/PLL3_CLK14	J1	IO_137_N	93.4455	DQ3_B3
B3	DIFFI_B3_22P/GCLK27/PLL2_CLK15/PLL3_CLK15	J3	IO_137_P	93.879	DQ3_B3
B3	DIFFI_B3_23N	K1	IO_138_N	86.1055	DQ3_B3
B3	DIFFI_B3_23P	K2	IO_138_P	83.0353	DQ3_B3
B3	DIFFI_B3_24N	L1	IO_139_N	79.6711	DQS3#_B3
B3	DIFFI_B3_24P	L3	IO_139_P	77.6304	DQS3_B3
B3	DIFFI_B3_25N	M1	IO_140_N	77.444	DQ3_B3
B3	DIFFI_B3_25P	M2	IO_140_P	74.8113	DQ3_B3
B3	DIFFI_B3_26N	N1	IO_141_N	79.9665	DQ3_B3
B3	DIFFI_B3_26P	N3	IO_141_P	76.6385	DQ3_B3
B3	DIFFI_B3_27N	P4	IO_142_N	86.6281	DQ4_B3
B3	DIFFI_B3_27P	R4	IO_142_P	88.942	DQ4_B3
B3	DIFFI_B3_28N	P1	IO_143_N	77.7562	DQ4_B3
B3	DIFFI_B3_28P	P2	IO_143_P	72.784	DQ4_B3
B3	DIFFI_B3_29N	R1	IO_144_N	80.2069	DQ4_B3
B3	DIFFI_B3_29P	R3	IO_144_P	81.2049	DQ4_B3
B3	DIFFI_B3_30N	T1	IO_145_N	92.6603	DQS4#_B3
B3	DIFFI_B3_30P	T2	IO_145_P	86.9673	DQS4_B3
B3	DIFFI_B3_31N	U1	IO_146_N	90.5749	DQ4_B3
B3	DIFFI_B3_31P	U3	IO_146_P	90.5267	DQ4_B3
B3	DIFFI_B3_32N	V1	IO_147_N	99.1182	DQ4_B3
B3	DIFFI_B3_32P	V2	IO_147_P	92.191	DQ4_B3
B3	DIFFI_B3_33N/VREF_B3	M4	IO_148_N	71.0611	DQ5_B3
B3	DIFFI_B3_33P	M5	IO_148_P	70.1002	DQ5_B3
B3	DIFFI_B3_34N	N4	IO_149_N	65.5537	DQ5_B3
B3	DIFFI_B3_34P	P3	IO_149_P	66.6815	DQ5_B3
B3	DIFFI_B3_25N	V3	IO_150_N	89.9905	DQS5#_B3
B3	DIFFI_B3_25P	U4	IO_150_P	84.914	DQS5_B3
B3	DIFFI_B3_36N	T3	IO_151_N	72.287	DQ5_B3

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
				9	
B3	DIFFI_B3_36P	T4	IO_151_P	74.9655	DQ5_B3
B3	DIFFI_B3_37N	P5	IO_152_N	61.6247	DQ5_B3
B3	DIFFI_B3_37P	P6	IO_152_P	62.579	DQ5_B3
B3	DIFFI_B3_38N	W1	IO_153_N	99.7456	DQ5_B3
B3	DIFFI_B3_38P	W3	IO_153_P	94.0458	DQ5_B3
B3	DIFFI_B3_39N/VREF_B3	Y1	IO_154_N	101.988	DQ5_B3
B3	DIFFI_B3_39P	Y2	IO_154_P	99.0443	DQ5_B3
B2	CFG_DONE	Y22			
B2	CMPCS_B	Y20			
B2	RST_N	AA1			
	STAND_BY	N15			
	TCK	G15			
	TDI	E18			
	TDO	A19			
	TMS	C18			
	VCC	J8			
	VCC	J10			
	VCC	J12			
	VCC	J14			
	VCC	K9			
	VCC	K11			
	VCC	K13			
	VCC	L10			
	VCC	L12			
	VCC	L14			
	VCC	M9			
	VCC	M11			
	VCC	M13			
	VCC	N10			
	VCC	N12			
	VCC	N14			
	VCC	P9			
	VCC	P11			
	VCC	P13			
	VCC	R14			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
	VCCAUX	D16			
	VCCAUX	F11			
	VCCAUX	G12			
	VCCAUX	H9			
	VCCAUX	H15			
	VCCAUX	K15			
	VCCAUX	L8			
	VCCAUX	M15			
	VCCAUX	N8			
	VCCAUX	R6			
	VCCAUX	R10			
	VCCAUX	R12			
	VCCAUX	U11			
	VCCAUX	V6			
	VCCIO0	B4			
	VCCIO0	B7			
	VCCIO0	B11			
	VCCIO0	B15			
	VCCIO0	B19			
	VCCIO0	E9			
	VCCIO0	E13			
	VCCIO0	E17			
	VCCIO0	G10			
	VCCIO0	G14			
	VCCIO1	C21			
	VCCIO1	E19			
	VCCIO1	G21			
	VCCIO1	J18			
	VCCIO1	L16			
	VCCIO1	L21			
	VCCIO1	N18			
	VCCIO1	R21			
	VCCIO1	U18			
	VCCIO1	W21			
	VCCIO2	T9			
	VCCIO2	T13			
	VCCIO2	V8			
	VCCIO2	V12			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
	VCCIO2	V16			
	VCCIO2	W5			
	VCCIO2	AA3			
	VCCIO2	AA7			
	VCCIO2	AA11			
	VCCIO2	AA15			
	VCCIO2	AA19			
	VCCIO3	C2			
	VCCIO3	F4			
	VCCIO3	F6			
	VCCIO3	G2			
	VCCIO3	J5			
	VCCIO3	L2			
	VCCIO3	L7			
	VCCIO3	N5			
	VCCIO3	R2			
	VCCIO3	U5			
	VCCIO3	W2			
	VSS	A1			
	VSS	A22			
	VSS	B5			
	VSS	B9			
	VSS	B13			
	VSS	B17			
	VSS	D4			
	VSS	D18			
	VSS	E2			
	VSS	E7			
	VSS	E11			
	VSS	E15			
	VSS	E21			
	VSS	G5			
	VSS	G18			
	VSS	H7			
	VSS	J2			
	VSS	J9			
	VSS	J11			
	VSS	J13			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
	VSS	J15			
	VSS	J21			
	VSS	K10			
	VSS	K12			
	VSS	K14			
	VSS	L5			
	VSS	L9			
	VSS	L11			
	VSS	L13			
	VSS	L18			
	VSS	M10			
	VSS	M12			
	VSS	M14			
	VSS	N2			
	VSS	N9			
	VSS	N11			
	VSS	N13			
	VSS	N17			
	VSS	N21			
	VSS	P10			
	VSS	P12			
	VSS	P14			
	VSS	R5			
	VSS	R18			
	VSS	U2			
	VSS	U7			
	VSS	U21			
	VSS	V4			
	VSS	V10			
	VSS	V14			
	VSS	W7			
	VSS	W16			
	VSS	W19			
	VSS	AA5			
	VSS	AA9			
	VSS	AA13			
	VSS	AA17			
	VSS	AB1			

Bank Name	Pin Name(Function name)	Pin Number	Differential Pair	Time Delay (ps)	DQS Grouping
	VSS	AB22			
	NC	F7			
	NC	G7			
	NC	L15			
	NC	M7			
	NC	M8			
	NC	M16			
	NC	N6			
	NC	N7			
	NC	N16			
	NC	P7			
	NC	P8			
	NC	P15			
	NC	P16			
	NC	R13			
	NC	R15			
	NC	R16			
	NC	R17			
	NC	R19			
	NC	T8			
	NC	T10			
	NC	T12			
	NC	T14			
	NC	T15			
	NC	T16			
	NC	T17			
	NC	T18			
	NC	U8			
	NC	U10			
	NC	U12			
	NC	U16			
	NC	U17			
	NC	V17			
	NC	W17			

2.2.2 Thermal Resistance

Table 2-4 Thermal Resistance

θJA(°C/W) (Flow: 0m/s)	**θJB (°C/W)**	**θJC (°C/W)**	**θJA(°C/W) (Flow: 1m/s)**	**θJA(°C/W) (Flow: 2m/s)**
17.8	11.1	10.1	14.8	13.8

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