# Logos Family Products HMEMC Use Case User Guide

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# Revisions History

## Document Revisions

| Version | Date of Release | Revisions |
|---|---|---|
| V1.2 | 04.11.2019 | Initial release. |
| | | |

# About this Manual

## Terms and Abbreviations

| Terms and Abbreviations | Meaning |
|---|---|
| HMEMC | Hard Memory Controller |
| DDR | Double Data Rate |
| IOL | IO Logic |
| IOB | IO Buffer |
| QoS | quality of service |
| | |

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# Chapter 1 Overview

This document primarily describes the main functions of HMEMC and the use cases of implementing DDR3 memory read and write operations using HMEMC.

HMEMC is a high-performance embedded hard core memory controller in the Logos Family FPGA chips, simplifying the interface interconnection operations with current popular memory standards. Compared to similar scale IPs, HMEMC offers better performance and reduces power consumption and development time. HMEMC preserves valuable FPGA resources, allowing developers to focus more on the FPGA design tasks.

Key features:

- LPDDR, DDR2, DDR3 supported
- x8, x16 DDR memory supported
- Standard AXI4 bus protocol supported
- Three AXI4 user channels in total, one 128-bit, and two 64-bit, supporting read and write operations
- AXI4 read reordering supported
- BANK Management supported
- Various low power modes supported, including self-refresh, power down, deep power down
- Bypass DDRC supported
- DDR3 write leveling and DQS gate training supported
- DDR3 maximum transfer rate reaches up to 1066Mb/s

Performance parameters:

Table 1-1 Data Rate and Peak Bandwidth of the Memory Interface

| **Memory type** | **Data rate: Mb/s DDR (MHz Clock)** | | **Peak bandwidth per HMEMC (Gb/s)** | |
|---|---|---|---|---|
| | **Min.** | **Max.** | **8-bit** | **16-bit** |
| DDR2 | 250 Mb/s (125 MHz) | 800 Mb/s (400 MHz) | 6.4 Gb/s | 12.8 Gb/s |
| DDR3 | 606 Mb/s (303 MHz) | 1066 Mb/s (533 MHz) | 8.528 Gb/s | 17.056Gb/s |
| LPDDR | 200 Mb/s (100 MHz) | 400 Mb/s (200 MHz) | 3.2 Gb/s | 6.4 Gb/s |

# Chapter 2 HMEMC Functional Description

HMEMC has realized the FPGA fabric connection with DDR memory. Its main function is to receive access requests from the upper user logic on the FPGA fabric through the AXI4 bus interface, schedule them according to the priority of the requests, convert them into various commands recognizable by the memory in accordance with memory timing requirements, send them to the memory, and ultimately complete read and write operations on memory data. The figure below describes the connection among HMEMC, FPGA fabric, and DDR memory.

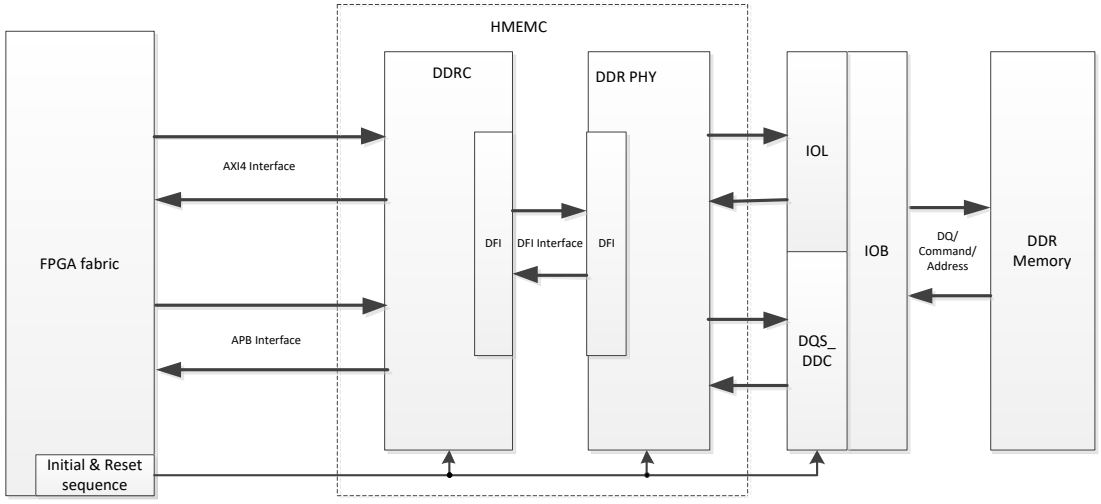


Figure 2-1 Interconnection of HMEMC with Other Hardware Resources

## 2.1 HMEMC Structural Description

The HMEMC is primarily composed of the DDR Controller and DDR PHY.

The DDRC module mainly arbitrates user read and write requests, completes the conversion of AXI4 commands to DFI read and write commands and operational timing, and schedules read and write operations to DDR memory.

The DDR PHY performs initialization of different types of DDR memory, write leveling for DDR3, DQS gate training, and read data eye leveling of different types of DDR memory. Receives DFI commands sent by the DDRC and performs protocol conversion then transmit them to DDR memory.

In addition, to enable the HMEMC to function properly, initialization and reset modules are needed to handle power-up initialization of the entire system and reset control of all modules. To minimize risk, this functionality is placed within the FPGA fabric and implemented through soft logic.

## 2.2 HMEMC Interface Description

### 2.2.1 AXI4 Bus Interface

#### 2.2.1.1 Signal Description

The table below describes the AXI4 bus signals of HMEMC. The suffix "_X" of each signal represents different AXI4 user channels ranging from 0 to 2.

Table 2-1 Description of AXI4 Bus Signals

| Signal Name | Direction | Signal Description |
|---|---|---|
| CSYSREQ_X | Input | Request to exit AXI low-power mode, active-high |
| CSYSACK_X | Output | Response to exit AXI low-power mode, active-high |
| CACTIVE_X | Output | Peripheral device clock request, active-high |
| ACLK_X | Input | Input clock signal |
| AWID_X [7:0] | Input | Write address ID |
| AWADDR_X [31:0] | Input | Write Address |
| AWLEN_X [7:0] | Input | Write burst length |
| AWSIZE_X [2:0] | Input | Write burst size |
| AWBURST_X [1:0] | Input | Write burst type, does not support fixed burst type |
| AWVALID_X | Input | Write address valid, active-high |
| AWREADY_X | Output | Write address ready, active-high |
| AWURGENT_X | Input | Once enabled, this port has the highest priority. If the PCFGW_n.wr_port_urgent_en register is enabled, the arbitrator PA immediately enters write command arbitration. When the corresponding port and address queue requests are empty, PA will ignore this signal |
| WDATA_X [127:0] | Input | Write data signal |
| WSTRB_X[15:0] | Input | Write data strobe signal, active-high |
| WLAST_X | Input | Write the signal indicating the last data, active-high |
| WVALID_X | Input | Write valid signal, active-high |
| WREADY_X | Output | Write ready signal, active-high |
| BID_X [7:0] | Output | Write response ID |
| BRESP_X [1:0] | Output | Write response, indicating the status of the write transaction. Possible responses: OKAY, EXOKAY, SLVERR, and DECERR |
| BVALID_X | Output | Write response valid, active-high |
| BREADY_X | Input | Write response ready, active-high |
| ARID_X [7:0] | Input | Read address ID |
| ARADDR_X [31:0] | Input | Read Address |
| ARLEN_X [7:0] | Input | Read burst length |
| ARSIZE_X [2:0] | Input | Read burst size |
| ARBURST_X[1:0] | Input | Read burst type |
| ARLOCK_X | Input | Lock type. In AXI4: 0 represents normal access, 1 represents exclusive access. For exclusive access, please refer to the relevant description in the AXI4 protocol |
| ARVALID_X | Input | Read address valid, active-high |

| Signal Name | Direction | Signal Description |
|---|---|---|
| ARREADY_X | Output | Read address ready, active-high |
| ARURGENT_X | Input | Once enabled, this port has the highest priority. If the PCFGR_n.rd_port_urgent_en register is enabled, the arbitrator PA immediately enters read command arbitration. PA will ignore this signal when the corresponding port and address queue requests are empty |
| RID_X [7:0] | Output | Read ID |
| RDATA_X [127:0] | Output | Read data |
| RRESP_X [1:0] | Output | Read response |
| RLAST_X | Output | The last data in a read transaction, active-high |
| RVALID_X | Input | Read data valid, active-high |
| RREADY_X | Output | Read data ready, active-high |

### 2.2.1.2 Timing Description

The following is a step-by-step introduction to the interface timing of the AXI4 bus.

- Write channel timing

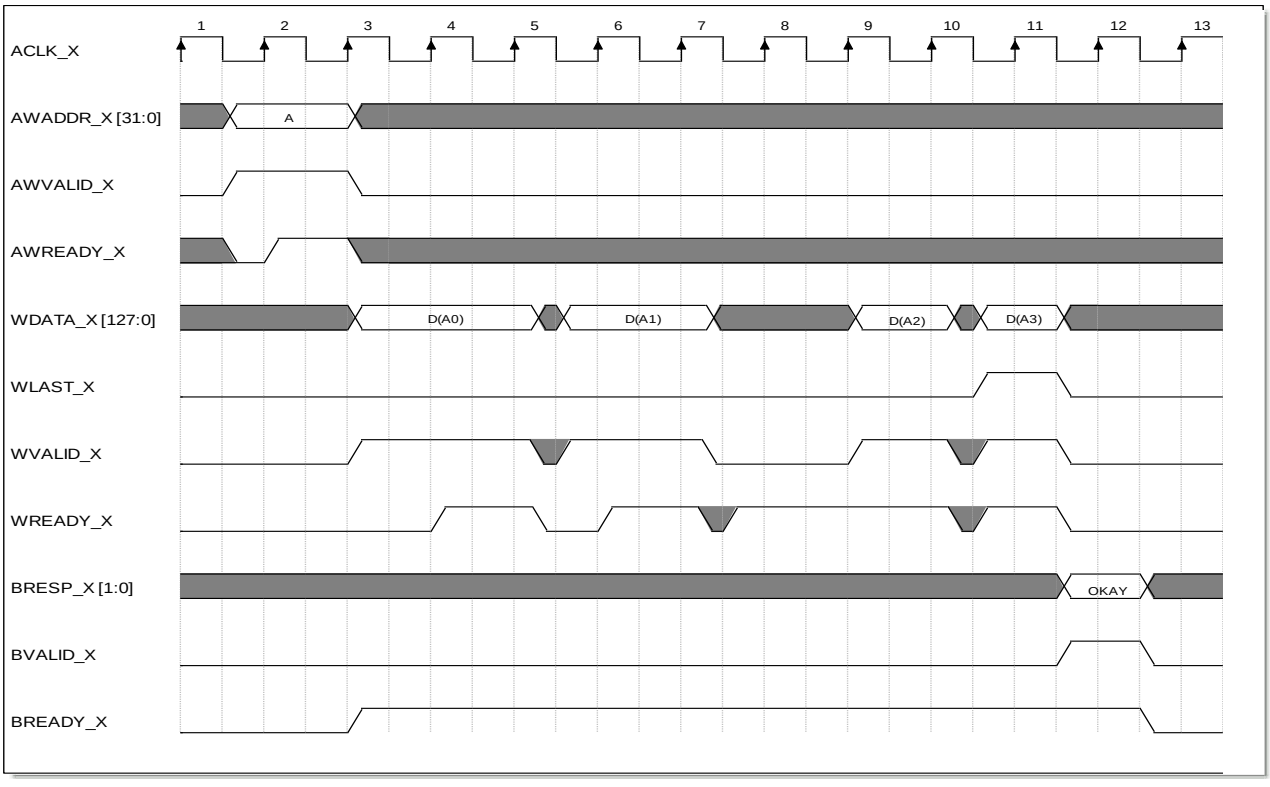


Figure 2-2 Write Burst Timing Diagram

- Read channel timing

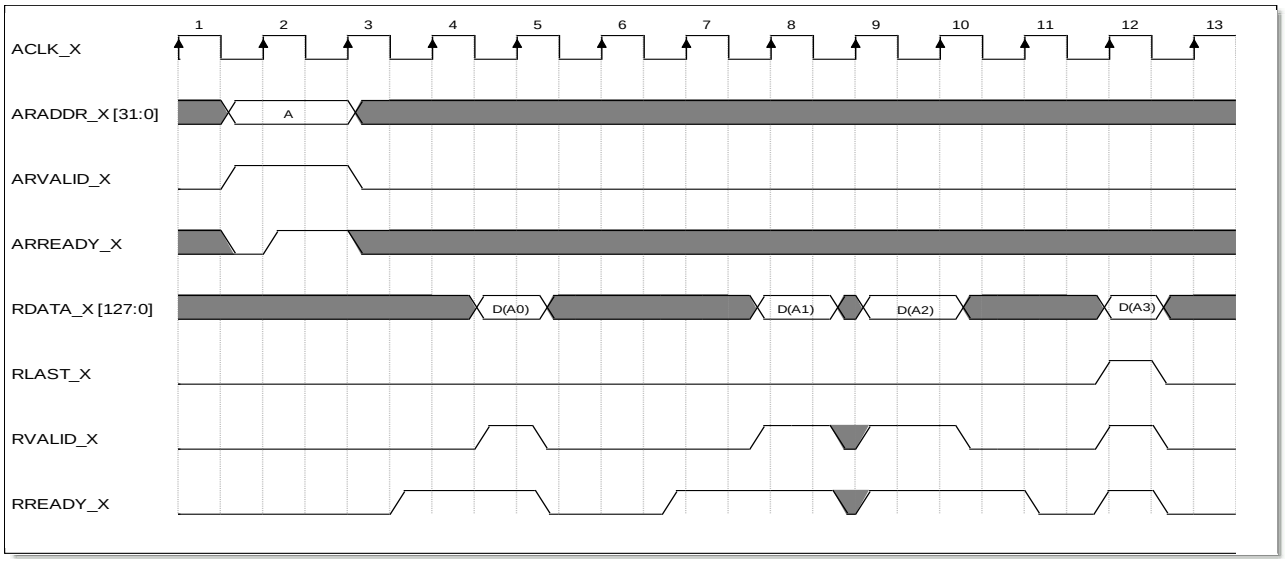


Figure 2-3 Read Burst Timing Diagram

## 2.2.2 APB Bus Interface

### 2.2.2.1 Signal Description

The table below describes the APB bus signals of HMEMC.

Table 2-2 Description of APB Bus Signals

| **Signal Name** | **Direction** | **Signal Description** |
|---|---|---|
| PCLK | Input | APB clock signal |
| PRESET | Input | APB reset signal, active-high |
| PADDR[11:0] | Input | APB address signal |
| PWDATA[31:0] | Input | APB write data signal |
| PWRITE | Input | APB read/write direction, high level for write operation |
| PSEL | Input | APB selection signal, active-high |
| PENABLE | Input | APB enable signal, active-high |
| PREADY | Output | APB ready signal, active-high |
| PRDATA [31:0] | Output | APB read data signal |
| PSLVERR | Output | APB error signal, active-high |

### 2.2.2.2 Timing Description

- APB interface write timing

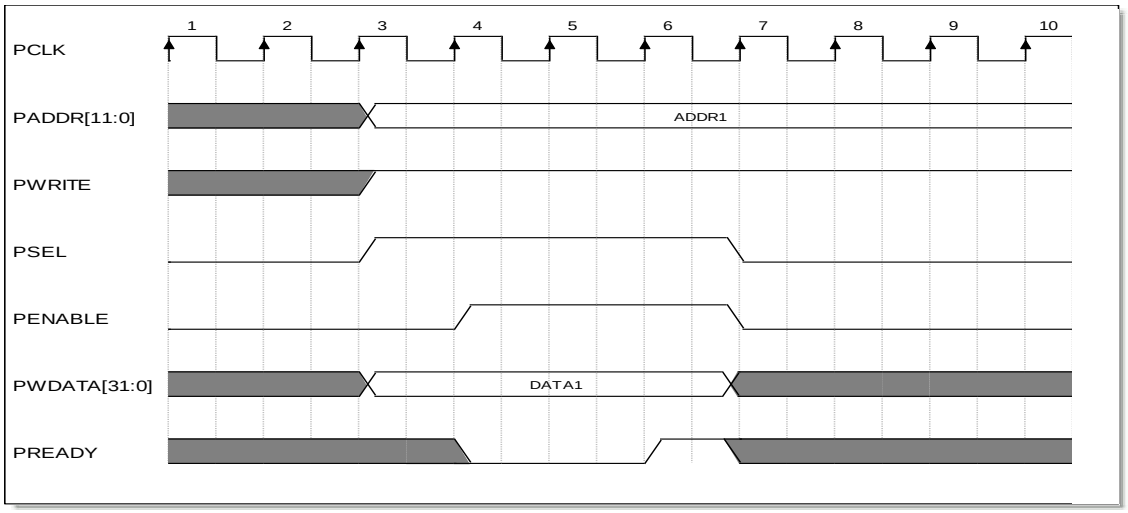


Figure 2-4 APB Interface Write Timing Diagram

- APB interface read timing

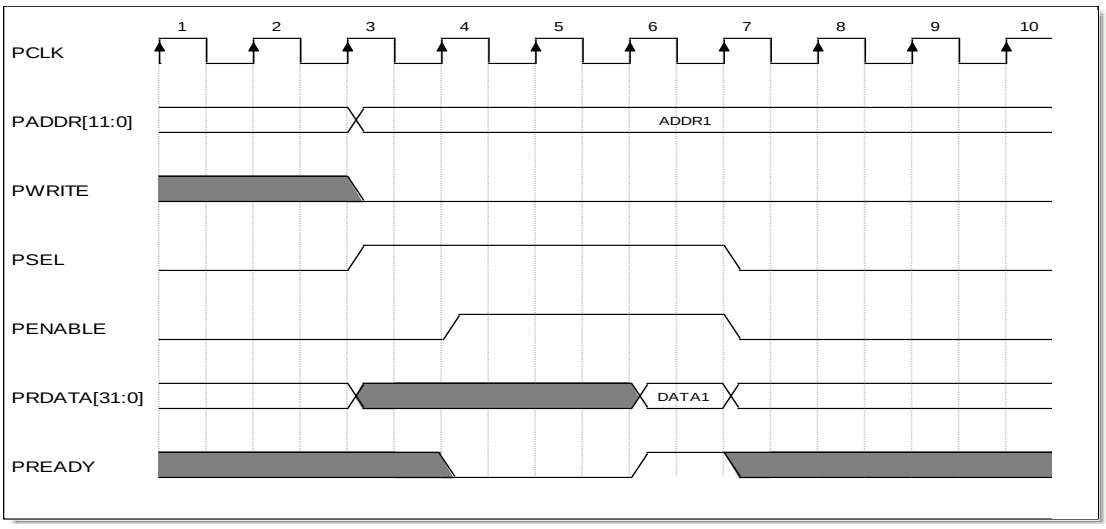


Figure 2-5 APB Interface Read Timing Diagram

### 2.2.3 Clock and Reset Signal

Figure 2-6 describes the logic block diagram of the main clock and reset signals of HMEMC.

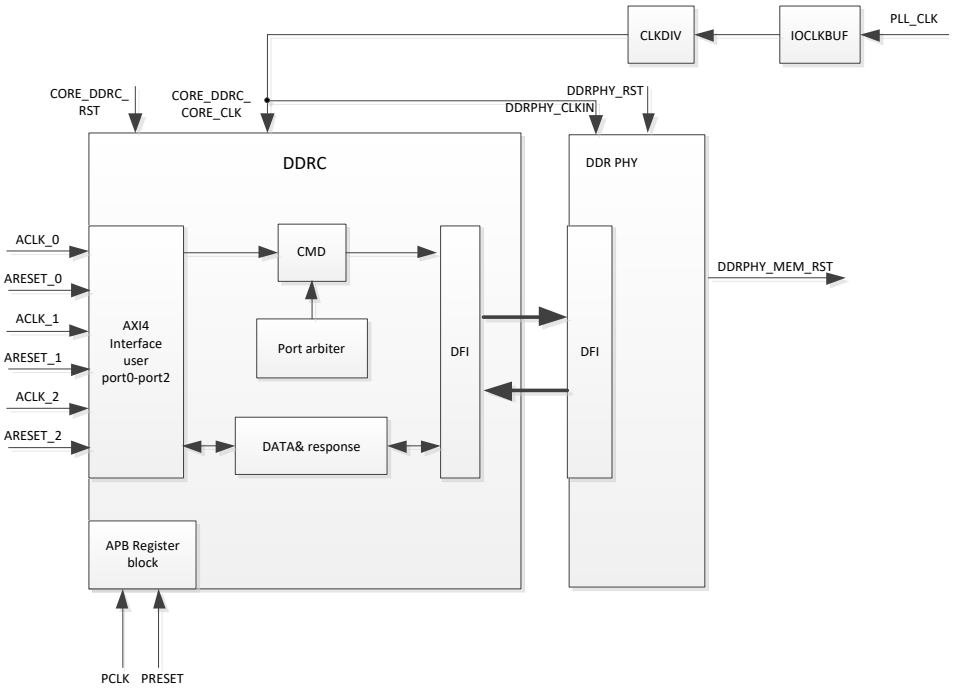


Figure 2-6 HMEMC Clock and Reset Signals

The clock signals of HMEMC are shown in Table 2-3. These clocks are all asynchronous.

Table 2-3 HMEMC Clock Signals

| **Signal Name** | **Direction** | **Signal Description** |
|---|---|---|
| CORE_DDRC_CORE_CLK | Input | DDRC system clock, comes from the PLL, i.e., PLL_CLK. The maximum clock frequency is 266.5MHz. |
| ACLK_X | Input | AXI4 bus interface clock, generated by the PLL. The maximum clock frequency is 133MHz. The value of X ranges from 0 to 2, representing different user ports. |
| PCLK | Input | APB bus interface clock, generated by the PLL. The frequency of PCLK must be less than or equal to the frequency of CORE_DDRC_CORE_CLK. The maximum clock frequency is 100MHz. |

The reset signals of HMEMC are shown in Table 2-4.

Table 2-4 HMEMC Reset Signals

| **Signal Name** | **Direction** | **Signal Description** |
|---|---|---|
| DDRPHY_RST | Input | The reset signal of DDR PHY, coming from FPGA fabric, active-high |
| PRESET | Input | The reset signal of the APB bus interface, coming from FPGA fabric, active-high |
| CORE_DDRC_RST | Input | The reset signal of DDRC, coming from FPGA fabric, active-high |
| ARESET_X | Input | The reset signal of the AXI4 bus interface, coming from FPGA fabric, active-high |
| DDRPHY_MEM_RST | Output | The reset signal from DDR PHY to external DDR memory, active-high |

### 2.2.4 User Port Mask Signal

Table 2-5 User Port Mask Signal

| Signal Name | Direction | Signal Description |
|---|---|---|
| pa_rmask[2:0] | Input | Mask the read address request to PA from the corresponding port. 0 to 2 corresponds to port0 to port2 |
| pa_wmask[2:0] | Input | Mask the write address request to PA from the corresponding port. 0 to 2 corresponds to port0 to port2 |

### 2.2.5 Low-Power Mode Signal

Table 2-6 HMEMC Low-Power Mode Signal

| Signal Name | Direction | Signal Description |
|---|---|---|
| csysreq_ddrc | Input | DDRC low-power request signal |
| csysack_ddrc | Output | DDRC low-power response signal |
| cactive_ddrc | Output | DDRC low-power clock valid signal, a low level indicates clock removal |
| CSYSREQ_X | Input | Request to exit AXI low-power mode, active-high |
| CSYSACK_X | Output | Response to exit AXI low-power mode, active-high |
| CACTIVE_X | Output | Peripheral device clock request, active-high |

## 2.3 User Port Selection

HMEMC supports 3 AXI4 channels, one 128-bit, and two 64-bit. Users can choose the appropriate port according to their actual needs. For unused ports, it is best to configure the reset signal to be high level, other signals can be left floating. If more ports are needed on the user side, a soft core must be developed independently.

When multiple AXI4 channels are in use, the mask function can filter out a unique port for read and write operations. The description of related signals is shown in Table 2-5.

## 2.4 Low-Power Mode

### 2.4.1 AXI Low-Power Mode

HMEMC has a total of 3 sets of AXI channels, therefore there are 3 sets of AXI low-power port signals, which are CSYSREQ_X, CACTIVE_X, and CSYSACK_X, as shown in Table 2-6. External devices can initiate a request to enter or exit the AXI low-power mode through CSYSREQ_X, while HMMEC indicates acceptance or rejection of the request through CACTIVE_X, and HMEMC responds to external device requests through CSYSACK_X.

When an external device makes a request, if the AXI channel has no pending read/write requests

and there is no data in the write queue that has been accepted, it can enter a low-power state; otherwise, the request will be rejected. The timing relationship for entering and exiting the AXI low-power mode is shown in the figure below:

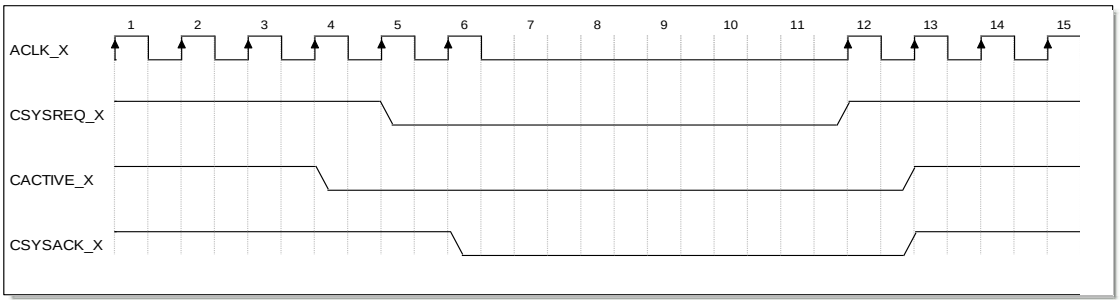


Figure 2-7 Timing Diagram for Entering and Exiting Axi Low-Power Mode

As Figure 2-7 shows, when an AXI channel requests to enter the AXI low-power mode CSYSREQ_X is pulled low, and after one clock cycle CSYSACK_X is also pulled low, if at this time CACTIVE_X is also low, then the clock of this port is canceled, and it enters AXI low-power mode; when requesting to exit the AXI low-power mode, CSYSREQ_X is pulled high, the clock signal is restored, and after one clock cycle CSYSACK_X is pulled high, the port returns to normal operation.

Figure 2-8 provides the scenarios where entering the AXI low-power mode is denied.

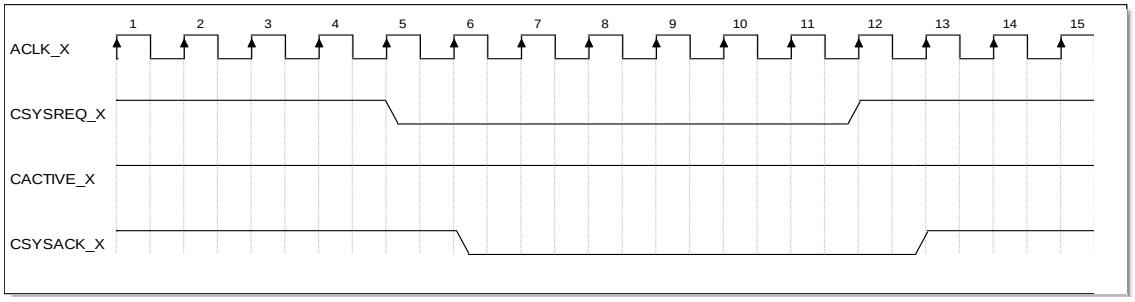


Figure 2-8 Timing for Denying Access to AXI Low-Power Mode

When the AXI channel has a data read or write request, it can also exit the AXI low-power mode through CACTIVE_X. Its timing diagram is shown below:

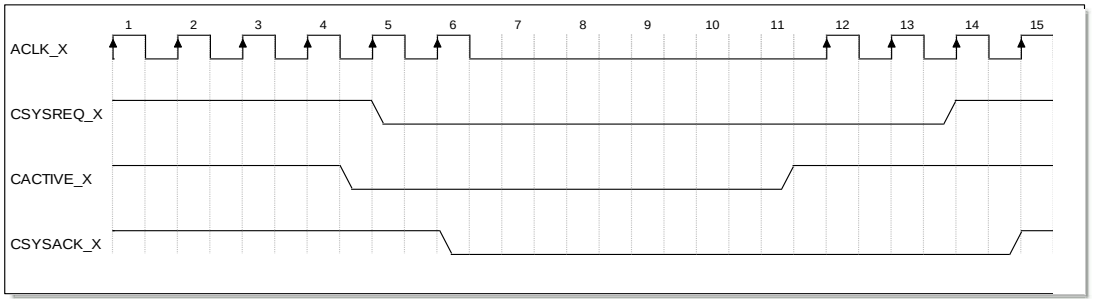


Figure 2-9 Request to Exit AXI Low-Power Mode Initiated by CACTIVE_X

As Figure 2-9 shows, external devices can also initiate a request to exit the AXI low-power mode through the CACTIVE_X status. A low CACTIVE_X indicates that the AXI channel has no pending read or write requests and the write data queue has no data to be received, meaning the port is idle and can initiate a request to enter a low-power mode at this time; when there is a read or write request, CACTIVE_X is high, the system reactivates the clock signal, and when CSYSACK_X is high, the port starts to operate normally.

### 2.4.2 DDRC Low-Power Mode

When the DDRC is idle, it can request to enter low-power mode. The DDRC low-power interface signals include CSYSREQ_DDRC, CSYSACK_DDRC, and CACTIVE_DDRC; as Table 2-6 shows, these signals can put the DDRC into low-power mode. Trigger the DDRC to enter self-refresh mode via CSYSREQ_DDRC. The existing commands in the DDRC will be executed before entering self-refresh mode. The timing diagram for entering the DDRC low-power mode is shown below:

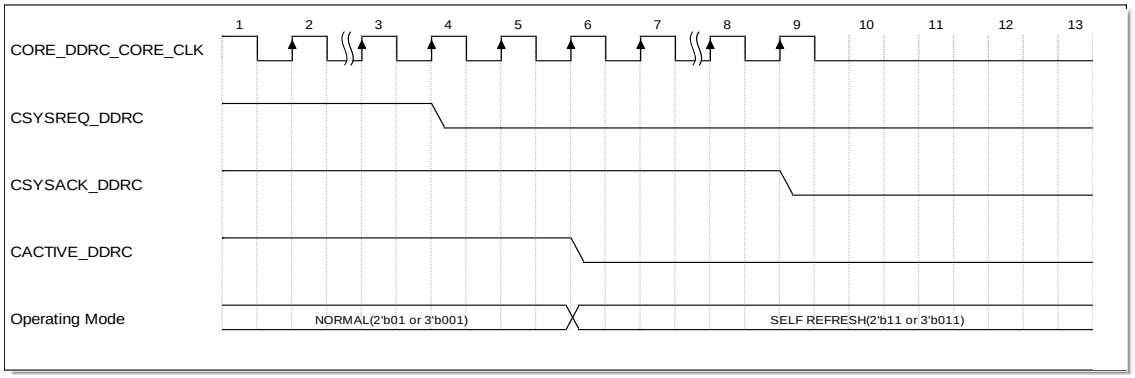


Figure 2-10 Entering DDRC Low-Power Mode

The timing for exiting the DDRC low-power mode is shown in the figure below. The FPGA fabric requests to exit the DDRC low-power mode by pulling CSYSREQ_DDRC high. When CACTIVE_DDRC is high and CSYSACK_DDRC is also pulled high, the DDRC exits low-power mode and the HMEMC transitions from self-refresh mode to normal working mode.

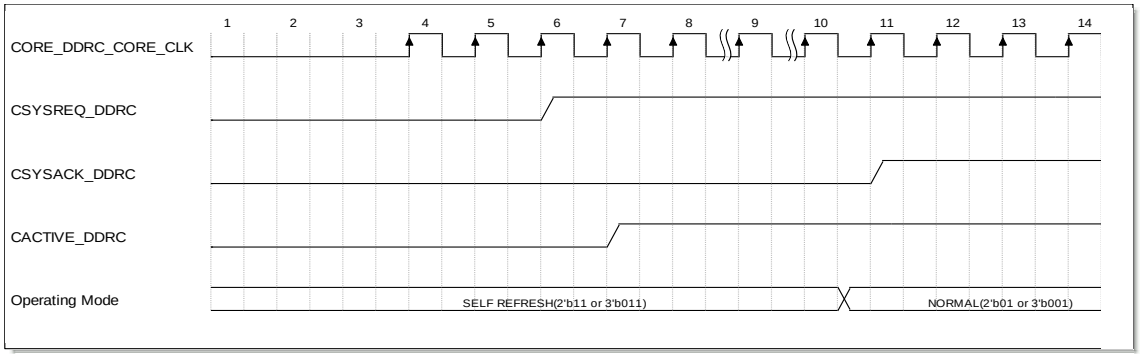


Figure 2-11 Exiting DDRC Low-Power Mode

# Chapter 3 Introduction to the HMEMC DDR3 Case

This case is a random read/write use case for HMEMC-based DDR3 memory, with the main modules DDRC and DDR_PHY implemented by calling the corresponding GTPs. Read and write control as well as initialization and reset modules are implemented through RTL code. This case uses an AXI channel. Externally, it employs one x16 DDR3 memory, Micron, MT41K512M16HA.

## 3.1 Design Description

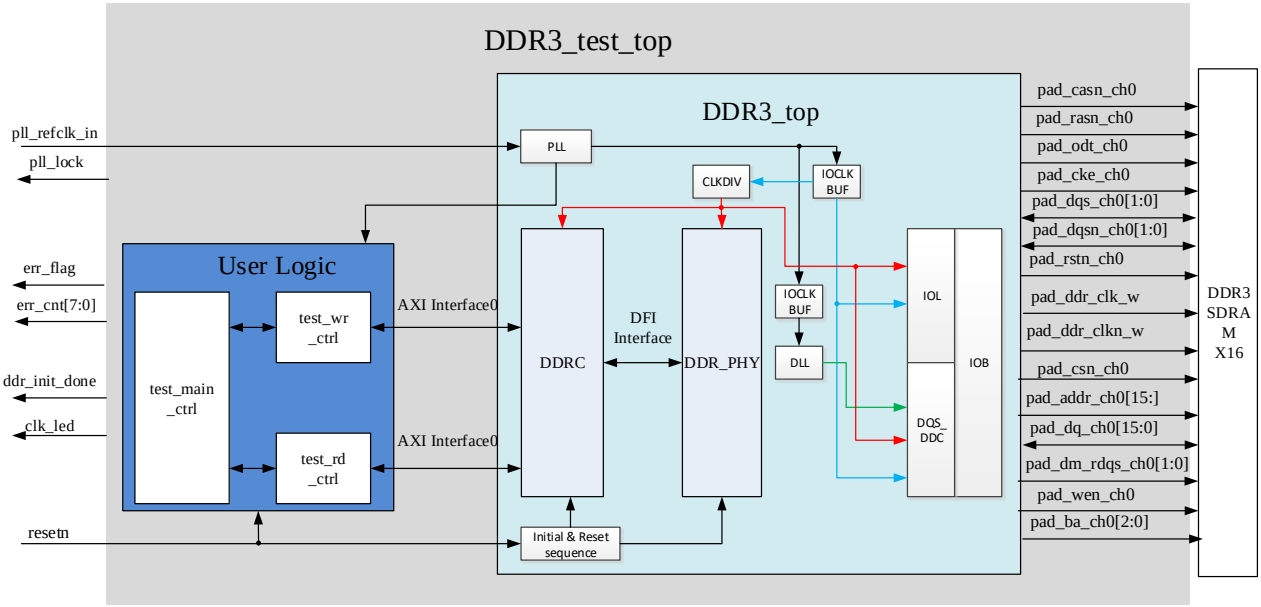


Figure 3-1 Logic Block Diagram of DDR3 Design Case Logic

The logic block diagram of this case is as shown in Figure 3-1, primarily comprising the User Logic module and the DDR3 master module DDR3_top. Within this, the User Logic module can be developed by the user as needed, with HMEMC encapsulated within the DDR3 master module, requiring no modifications.

The User Logic module includes test_main_ctrl, test_wr_ctrl, and test_rd_ctrl.

- test_main_ctrl: DDR3 read/write master control module, controls the initialization of DDR3 SDRAM, and manages read/write switching;
- test_wr_ctrl: Write control module, performs write burst operations;
- test_rd_ctrl: Read control module, performs read burst operations;
- The DDR3 master module includes HMEMC (DDRC and DDR PHY), initialization and reset modules, PLL, IOL, DQS_DDC, and IOB.

- DDRC: Completes the conversion of AXI4 commands to DFI read and write commands and operational timing, schedules read and write operations to DDR3 memory;
- DDR PHY: Completes the initialization of DDR3 memory, accomplishes write leveling, DQS gate training, read leveling, and other tasks, while also receiving DFI commands from DDRC, performing protocol conversion, and sending them to the external DDR3 memory;
- Initialization and reset modules: Complete the power-up initialization of the entire system and the reset control of all modules;
- PLL: The external reference clock enters the PLL, generates the AXI4 interface clock, which then through IOCLKBUF, CLKDIV, and DLL, produces the DDRC system clock, DDR PHY system clock, and the clocks required for IOL and DQS_DDC;
- DLL: Provides the delay adjustment code ctrl_code needed for DQS_DDC delay tuning;
- IOL: Completes the serialization and deserialization of high-speed data;
- IOB: Completes the level conversion for various DDR memory devices, provides an interface between the FPGA and DDR3 memory;
- DQS_DDC: Completes the gating operation on the input DQS to remove noise influence, shifts the gated DQS phase by 1/4 clock cycle, and controls the read/write pointers of IOL IFIFO.

HMEMC first initializes the DDR3 memory; upon completion, the ddr_init_done signal is pulled high. Thereafter, users can control the DDR3 master module through the user-side AXI4 port.

In this case, all addresses of the DDR3 memory are first written sequentially, followed by the first random write operation. This write operation is of random length, writing random data to random addresses. After completing the first write operation, random read and write operations begin. Subsequent operations are either read or write, depending on the output of the pseudo-random number generator module. During read operations, the read-back data is verified; if incorrect, an error is outputted.

In this case, data is written through the write channel of the AXI4 interface and received through the read channel of the AXI4 interface.

## 3.2 Parameter Description

Table 3-1 Parameter Description of DDR3 Design Case

| Parameter Name | Parameter Description |
|---|---|
| DDR_TYPE | DDR type, supports "DDR3", "DDR2", and "LPDDR" |
| DQ_WIDTH | DDR data width, supports "8" and "16" |
| SPEED | DDR speed, supports "600Mbps", "800Mbps", and "1066Mbps" |
| DDR_SIZE | DDR memory capacity, supports "512Mb", "1Gb", "2Gb", "4Gb", and "8Gb" |

## 3.3 Signal Description

The table below describes the top-level signals for the HMEMC DDR3 design case, primarily including the interface signals between the FPGA and DDR memory.

Table 3-2 Description of HMEMC DDR3 Design Case Top-Level Signal

| Signal Name | Direction | Signal Description |
|---|---|---|
| pll_refclk_in | Input | FPGA external input reference clock, 50MHz |
| resetn | Input | System reset signal, active-low |
| clk_led | Output | System normal operation indicator signal, high and low-level changes |
| pll_lock | Output | PLL LOCK signal, active-high |
| ddr_init_done | Output | HMEMC initialization complete signal, active-high |
| pad_loop_in | Input | DQS_GATE temperature drift compensation input signal, corresponding to lower 8 bits of DQS |
| pad_loop_in_h | Input | DQS_GATE temperature drift compensation input signal, corresponding to upper 8 bits of DQS |
| pad_rstn_ch0 | Output | Reset signal of DDR memory |
| pad_ddr_clk_w | Output | P side of DDR memory |
| pad_ddr_clkn_w | Output | N side of DDR memory |
| pad_csn_ch0 | Output | DDR memory chip selection signal, active-low |
| pad_addr_ch0[15:0] | Output | DDR memory address |
| pad_dq_ch0[15:0] | Input/Output | DDR memory data |
| pad_dqs_ch0[1:0] | Input/Output | P side of DDR memory data strobe signal |
| pad_dqsn_ch0[1:0] | Input/Output | N side of DDR memory data strobe signal |
| pad_dm_rdqs_ch0[1:0] | Output | Data mask signal, active-high |
| pad_cke_ch0 | Output | DDR memory clock enable signal, active-high |
| pad_odt_ch0 | Output | DDR memory on-die termination enable signal, high to enable on-die termination |
| pad_rasn_ch0 | Output | Row address valid signal, active-low |
| pad_casn_ch0 | Output | Column address valid signal, active-low |
| pad_wen_ch0 | Output | DDR memory write enable signal, active-low |
| pad_ba_ch0[2:0] | Output | DDR memory bank address |
| pad_loop_out | Output | DQS_GATE temperature drift compensation output signal, corresponding to lower 8 bits of DQS |
| pad_loop_out_h | Output | DQS_GATE temperature drift compensation output signal, corresponding to upper 8 bits of DQS |
| err_flag | Output | Data verification error indicator |
| err_cnt[7:0] | Output | Data verification error statistics |

The user-side signal description of DDR3 master module is as follows (only AXI4 port0 is listed):

Table 3-3 User-Side Signal Description of DDR3 Master Module

| Signal Name | Direction | Signal Description |
|---|---|---|
| pll_refclk_in | Input | FPGA external input reference clock, 50MHz |
| rstn | Input | System reset signal, active-low |

| Signal Name | Direction | Signal Description |
|---|---|---|
| pll_lock | Output | PLL LOCK signal, active-high |
| axi_clk_fast | Output | High-speed clock output to AXI4 bus, supporting up to 133MHz |
| axi_clk_slow | Output | Low-speed clock output to AXI4 bus |
| pclk | Output | Clock signal output to APB bus, 50MHz |
| ddr_init_done | Output | HMEMC initialization complete signal, active-high |
| ddrc_rst | Input | DDRC reset signal, active-high |
| pa_rmask[2:0] | Input | Mask the read address request to the PA from the corresponding port. 0 to 2 corresponds to port0 to port2 |
| pa_wmask[2:0] | Input | Mask the write address request to the PA from the corresponding port. 0 to 2 corresponds to port0 to port2 |
| csysreq_ddrc | Input | DDRC low-power signal |
| csysack_ddrc | Output | DDRC low-power request response signal |
| cactive_ddrc | Output | DDRC low-power clock valid signal, a low level indicates clock removal |
| RAQ_PUSH _0 | Output | Write transaction to read address FIFO, pulse signal |
| RAQ_SPLIT_0 | Output | Read command execution in read address FIFO, pulse signal |
| WAQ_PUSH _0 | Output | Write transaction to write address FIFO, pulse signal |
| WAQ_SPLIT_0 | Output | Write command execution in write address FIFO, pulse signal |
| AWQOS_0[3:0] | Input | Write channel priority indication, higher value indicates higher priority; the default value is 4'b0000, QoS not implemented |
| ARQOS_0[3:0] | Input | Read channel priority indication, higher value indicates higher priority; the default value is 4'b0000, QoS not implemented |
| CSYSREQ_0 | Input | Request to exit AXI low-power mode, active-high |
| CSYSACK_0 | Output | Response to exit AXI low-power mode, active-high |
| CACTIVE_0 | Output | Peripheral device clock request, active-high |
| ARPOISON_0 | Input | AXI read poison, active-high, indicating the read priority is the highest |
| ARLOCK_0 | Input | Not supported |
| AWPOISON_0 | Input | AXI write poison, active-high, indicating the write priority is the highest |
| AWLOCK_0 | Input | Not supported |
| ACLK_0 | Input | Input clock signal |
| ARESET_0 | Input | Reset signal for AXI4 bus interface, active-high |
| AWID_0 [7:0] | Input | Write address ID |
| AWADDR_0 [31:0] | Input | Write address |
| AWLEN_0[7:0] | Input | Write burst length |
| AWSIZE_0 [2:0] | Input | Write burst size |
| AWBURST_0 [1:0] | Input | Write burst type, does not support fixed burst type |
| AWVALID_0 | Input | Write address valid, active-high |
| AWREADY_0 | Output | Write address ready signal, active-high |
| AWURGENT_0 | Input | Once enabled, this port has the highest priority. If the PCFGW_n.wr_port_urgent_en register is enabled, the arbitrator PA immediately enters write command arbitration. When the corresponding port and address queue requests are empty, PA will ignore this signal |
| WDATA_0[127:0] | Input | Write data signal |
| WSTRB_0[15:0] | Input | Write data strobe signaling, active-high |

| Signal Name | Direction | Signal Description |
|---|---|---|
| WLAST_0 | Input | Write the signal indicating the last data, active-high |
| WVALID_0 | Input | Write valid signal, active-high |
| WREADY_0 | Output | Write ready signal, active-high |
| BID_0[7:0] | Output | Write response ID |
| BRESP_0[1:0] | Output | Write response, indicating the status of the write transaction. Possible responses: OKAY, EXOKAY, SLVERR, and DECERR |
| BVALID_0 | Output | Write response valid, active-high |
| BREADY_0 | Input | Write response ready, active-high |
| ARID_0[7:0] | Input | Read address ID |
| ARADDR_0[31:0] | Input | Read address |
| ARLEN_0[7:0] | Input | Read burst length |
| ARSIZE_0[2:0] | Input | Read burst size |
| ARBURST_0[1:0] | Input | Read burst type |
| ARLOCK_0 | Input | Lock type In AXI4: 0 represents normal access, 1 represents exclusive access. For exclusive access, please refer to the relevant description in the AXI4 protocol |
| ARVALID_0 | Input | Read address valid, active-high |
| ARREADY_0 | Output | Read address ready, active-high |
| ARURGENT_0 | Input | Once enabled, this port has the highest priority. If the PCFGR_n.rd_port_urgent_en register is enabled, the arbitrator PA immediately enters read command arbitration. PA will ignore this signal when the corresponding port and address queue requests are empty |
| RID_0[7:0] | Output | Read ID |
| RDATA_0[127:0] | Output | Read data |
| RRESP_0[1:0] | Output | Read response |
| RLAST_0 | Output | The last data in a read transaction, active-high |
| RVALID_0 | Input | Read valid, active-high |
| RREADY_0 | Output | Read ready, active-high |
| PRESET | Input | APB reset signal, active-high |
| PADDR[11:0] | Input | APB address signal |
| PWDATA[31:0] | Input | APB write data signal |
| PWRITE | Input | APB read/write direction, high level for write operation |
| PSEL | Input | APB selection signal, active-high |
| PENABLE | Input | APB enable signal, active-high |
| PREADY | Output | APB ready signal, active-high |
| PRDATA [31:0] | Output | APB read data signal |
| PSLVERR | Output | APB error signal, active-high |

### 3.4 Simulation Description

The HMEMC simulation model is encrypted, and the related simulation files are located in the directories modelsim10.2c and vcs2014.03 under the path \arch\vendor\pango\verilog\simulation;

users should add the simulation library according to this path during simulation.

PDS supports the following simulation tools:

Modelsim version 10 and above

Debussy version 5.4 and above

To emulate this case, first, navigate to the "\scripts" directory, right-click in an empty area of the folder while holding down the shift key, enter "source_prj" in the command box that appears, press "Enter", then type "sim.bat demo_test FSDB_DUMP_ON", press "Enter" again to start the functional simulation. Users can also observe the waveforms in Debussy.

## 3.5 Description of the Resources Used

Table 3-4 DDR3 Case Resource List

| **Resource Type** | **Resource usage in x16 mode** |
|---|---|
| HMEMC | 1, 50% |
| IO | 70, 38% |
| LUT | 1044, 6% |
| PLL | 1, 17% |

# Chapter 4 PCB Design Description

There are two HMEMCs inside the Logos Family FPGA chips (one on the left and one on the right). If using the hard core on the right, in the connections between the DDR memory and the FPGA, only the connections of the DQ pins can be swapped within their respective groups, while the other pins must correspond strictly according to Table 4-1. (Required)

After routing DQSU_GATE_OUT outside the chip, it connects to DQSU_GATE_IN, and the routing length should be approximately equal to the sum of the CK trace length and the DQS trace length. DQSL_GATE_OUT and DQSL_GATE_IN should be treated similarly. (Not required, can be used without connection)

The trace length of CK should be slightly greater than that of DQS to ensure that the time difference between the arrival of the CK and DQS signals at the DDR memory is within one clock cycle. For example, if the DDR rate is 800Mbps, then the time difference should not exceed 2.5ns. If the PCB trace delay is 152mm/ns, then the CK trace length must not exceed 380mm, longer than the length of DQS. (Required)

Add pull-down resistors to the FPGA pins DQSU_P and DQSL_P, and pull-up resistors to the FPGA pins DQSU_N and DQSL_N, with resistance values between 500-1000ohms. The voltage applied to the pull-up resistors should match the voltage of the DDR memory, for example, 1.5V for DDR3. (Not required, used to improve signal quality).

The table below provides the mapping between FPGA pins and DDR memory signals.

Table 4-1 Mapping of FPGA Pins to DDR Memory Signals

| **FPGA Pin Number** | **Pin Description** | **DDR Memory Signal** |
|---|---|---|
| E2 | DIFFIO_L1_10_N/CLK3_L1/DIFFCLK1_L1_N/PLL3_CLKIN1 | L_A14 |
| E1 | DIFFIO_L1_10_P/CLK2_L1/DIFFCLK1_L1_P/PLL3_CLKIN0 | L_A15 |
| G3 | DIFFIO_L1_11_N/PLL3_CLKIN3 | L_A12 |
| G4 | DIFFIO_L1_11_P/PLL3_CLKIN2 | L_A13 |
| F1 | DIFFIO_L1_12_P/ | L_A11 |
| H6 | DIFFIO_L1_13_N/ | L_A10 |
| G2 | DIFFIO_L1_14_N/ | L_RESET_N |
| G1 | DIFFIO_L1_14_P/ | L_A9 |
| H3 | DIFFIO_L1_15_N/ | L_CKE |
| H4 | DIFFIO_L1_15_P/ | L_A8 |
| H2 | DIFFIO_L1_16_N/ | L_A6 |
| H1 | DIFFIO_L1_16_P/ | L_A7 |

| FPGA Pin Number | Pin Description | DDR Memory Signal |
|---|---|---|
| J4 | DIFFIO_L1_17_N/ | L_A4 |
| J3 | DIFFIO_L1_17_P/ | L_A5 |
| J2 | DIFFIO_L1_18_N/ | L_A2 |
| J1 | DIFFIO_L1_18_P/ | L_A3 |
| K7 | DIFFIO_L1_19_N/ | L_A0 |
| J7 | DIFFIO_L1_19_P/ | L_A1 |
| L3 | DIFFIO_L2_0_N/ | L_DQSU_GATE_IN |
| K3 | DIFFIO_L2_0_P/ | L_DQSU_GATE_OUT |
| K2 | DIFFIO_L2_1_N/ | L_DQ15 |
| K1 | DIFFIO_L2_1_P/ | L_DMU |
| R2 | DIFFIO_L2_10_N/CLK3_L2/DIFFCLK1_L2_N/PLL5_CLKIN1 | L_ODT |
| R1 | DIFFIO_L2_10_P/CLK2_L2/DIFFCLK1_L2_P/PLL5_CLKIN0 | L_WE_N |
| N4 | DIFFIO_L2_11_N/PLL5_CLKIN3 | L_CK_N |
| N3 | DIFFIO_L2_11_P/PLL5_CLKIN2 | L_CK |
| T7 | DIFFIO_L2_13_N/ | L_DQ7 |
| T4 | DIFFIO_L2_14_N/ | L_DQ5 |
| R4 | DIFFIO_L2_14_P/ | L_DQ6 |
| P6 | DIFFIO_L2_15_N/ | L_DQSL_N |
| P5 | DIFFIO_L2_15_P/ | L_DQSL |
| T5 | DIFFIO_L2_16_N/ | L_DQ3 |
| R5 | DIFFIO_L2_16_P/ | L_DQ4 |
| T8 | DIFFIO_L2_17_N/ | L_DQ1 |
| R8 | DIFFIO_L2_17_P/ | L_DQ2 |
| T6 | DIFFIO_L2_18_N/ | L_DML |
| R6 | DIFFIO_L2_18_P/ | L_DQ0 |
| M5 | DIFFIO_L2_19_N/ | L_DQSL_GATE_IN |
| N5 | DIFFIO_L2_19_P/ | L_DQSL_GATE_OUT |
| K6 | DIFFIO_L2_2_N/ | L_DQ13 |
| J6 | DIFFIO_L2_2_P/ | L_DQ14 |
| L2 | DIFFIO_L2_3_N/ | L_DQ11 |
| L1 | DIFFIO_L2_3_P/ | L_DQ12 |
| M2 | DIFFIO_L2_4_N/ | L_DQSU_N |
| M1 | DIFFIO_L2_4_P/ | L_DQSU |
| L4 | DIFFIO_L2_5_N/ | L_DQ9 |
| K4 | DIFFIO_L2_5_P/ | L_DQ10 |
| K5 | DIFFIO_L2_6_P/ | L_DQ8 |
| N2 | DIFFIO_L2_7_N/ | L_RAS_N |
| N1 | DIFFIO_L2_7_P/ | L_CS_N |
| T3 | DIFFIO_L2_8_N/PLL4_CLKOUT_N | L_BA2 |

| FPGA Pin Number | Pin Description | DDR Memory Signal |
|---|---|---|
| R3 | DIFFIO_L2_8_P/PLL4_CLKOUT_P | L_CAS_N |
| P2 | DIFFIO_L2_9_N/CLK1_L2/DIFFCLK0_L2_N/PLL4_CLKFB_N/ XTALB_L2 | L_BA0 |
| P1 | DIFFIO_L2_9_P/CLK0_L2/DIFFCLK0_L2_P/ PLL4_CLKFB_P/XTALA_L2 | L_BA1 |
| D15 | DIFFIO_R1_10_N/CLK3_R1/DIFFCLK1_R1_N/ PLL3_CLKFB_N | R_A14 |
| D16 | DIFFIO_R1_10_P/CLK2_R1/DIFFCLK1_R1_P/ PLL3_CLKFB_P | R_A15 |
| G13 | DIFFIO_R1_11_N/PLL3_CLKOUT_N | R_A12 |
| F13 | DIFFIO_R1_11_P/PLL3_CLKOUT_P | R_A13 |
| E16 | DIFFIO_R1_12_P/ | R_A11 |
| H14 | DIFFIO_R1_13_N/ | R_A10 |
| F15 | DIFFIO_R1_14_N/ | R_RESET_N |
| F16 | DIFFIO_R1_14_P/ | R_A9 |
| J13 | DIFFIO_R1_15_N/ | R_CKE |
| J14 | DIFFIO_R1_15_P/ | R_A8 |
| G15 | DIFFIO_R1_16_N/ | R_A6 |
| G16 | DIFFIO_R1_16_P/ | R_A7 |
| J10 | DIFFIO_R1_17_N/ | R_A4 |
| H10 | DIFFIO_R1_17_P/ | R_A5 |
| H15 | DIFFIO_R1_18_N/ | R_A2 |
| H16 | DIFFIO_R1_18_P/ | R_A3 |
| J11 | DIFFIO_R1_19_N/ | R_A0 |
| J12 | DIFFIO_R1_19_P/ | R_A1 |
| K13 | DIFFIO_R2_0_N/ | R_DQSU_GATE_IN |
| K14 | DIFFIO_R2_0_P/ | R_DQSU_GATE_OUT |
| J15 | DIFFIO_R2_1_N/ | R_DQ15 |
| J16 | DIFFIO_R2_1_P/ | R_DMU |
| P15 | DIFFIO_R2_10_N/CLK3_R2/DIFFCLK1_R2_N/PLL5_CLKFB_N | R_ODT |
| P16 | DIFFIO_R2_10_P/CLK2_R2/DIFFCLK1_R2_P/PLL5_CLKFB_P | R_WE_N |
| R16 | DIFFIO_R2_11_N/PLL5_CLKOUT_N | R_CK_N |
| R15 | DIFFIO_R2_11_P/PLL5_CLKOUT_P | R_CK |
| T11 | DIFFIO_R2_13_N/ | R_DQ7 |
| T14 | DIFFIO_R2_14_N/ | R_DQ5 |
| R14 | DIFFIO_R2_14_P/ | R_DQ6 |
| T10 | DIFFIO_R2_15_N/ | R_DQSL_N |
| R10 | DIFFIO_R2_15_P/ | R_DQSL |
| T13 | DIFFIO_R2_16_N/ | R_DQ3 |
| R13 | DIFFIO_R2_16_P/ | R_DQ4 |
| T9 | DIFFIO_R2_17_N/ | R_DQ1 |

| FPGA Pin Number | Pin Description | DDR Memory Signal |
|---|---|---|
| R9 | DIFFIO_R2_17_P/ | R_DQ2 |
| T12 | DIFFIO_R2_18_N/ | R_DML |
| R12 | DIFFIO_R2_18_P/ | R_DQ0 |
| N11 | DIFFIO_R2_19_N/ | R_DQSL_GATE_IN |
| N12 | DIFFIO_R2_19_P/ | R_DQSL_GATE_OUT |
| K12 | DIFFIO_R2_2_N/ | R_DQ13 |
| K11 | DIFFIO_R2_2_P/ | R_DQ14 |
| K15 | DIFFIO_R2_3_N/ | R_DQ11 |
| K16 | DIFFIO_R2_3_P/ | R_DQ12 |
| L16 | DIFFIO_R2_4_N/ | R_DQSU_N |
| L15 | DIFFIO_R2_4_P/ | R_DQSU |
| L12 | DIFFIO_R2_5_N/ | R_DQ9 |
| L11 | DIFFIO_R2_5_P/ | R_DQ10 |
| L14 | DIFFIO_R2_6_P/ | R_DQ8 |
| M15 | DIFFIO_R2_7_N/ | R_RAS_N |
| M16 | DIFFIO_R2_7_P/ | R_CS_N |
| P13 | DIFFIO_R2_8_N/PLL4_CLKIN1 | R_BA2 |
| N13 | DIFFIO_R2_8_P/PLL4_CLKIN0 | R_CAS_N |
| N15 | DIFFIO_R2_9_N/CLK1_R2/DIFFCLK0_R2_N/PLL4_CLKIN3/ XTALB_R2 | R_BA0 |
| N16 | DIFFIO_R2_9_P/CLK0_R2/DIFFCLK0_R2_P/PLL4_CLKIN2/ XTALA_R2 | R_BA1 |

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