U1A

DIFFIO_B0_0P/IO_STATUS_C	D4	IO_STATUS_C
DIFFIO_B0_0N/VREF_B0	C4 B0_L0_N	RESET
DIFFIO_B0_1P	B2 B0_L1_P	MIPI_DSI_D2_P
DIFFIO_B0_1N	A2 B0_L1_N	MIPI_DSI_D2_N
DIFFIO_B0_2P	D6 B0_L2_P	MIPI_DSI_D0_P
DIFFIO_B0_2N	C6 B0_L2_N	MIPI_DSI_D0_N
DIFFIO_B0_3P	B3 B0_L3_P	MIPI_DSI_D1_P
DIFFIO_B0_3N	A3 B0_L3_N	MIPI_DSI_D1_N
DIFFIO_B0_4P	B4 B0_L4_P	MIPI_DSI_CLK_P
DIFFIO_B0_4N	A4 B0_L4_N	MIPI_DSI_CLK_N
DIFFIO_B0_5P	C5 B0_L5_P	MIPI_DSI_D3_P
DIFFIO_B0_5N	A5 B0_L5_N	MIPI_DSI_D3_N
DIFFIO_B0_6P	C7 B0_L6_P	MIPI_DSI_ID
DIFFIO_B0_6N	A7 B0_L6_N	MIPI_DSI_BL
DIFFIO_B0_7P	B6 B0_L7_P	ETH_RST_N
DIFFIO_B0_7N/VREF_B0	A6 B0_L7_N	MIPI_DSI_RST
DIFFIO_B0_13P	D8 B0_L13_P	I2C5_SCL_1V8
DIFFIO_B0_13N	C8 B0_L13_N	I2C5_SDA_1V8
DIFFIO_B0_14P	B8 B0_L14_P	MIPI_RX1_RST
DIFFIO_B0_14N	A8 B0_L14_N	MIPI_RX1_PDN
DIFFIO_B0_15P/GCLK19/PLL0_CLK0/PLL1_CLK0	D9 B0_L15_P	TPAD
DIFFIO_B0_15N/GCLK18/PLL0_CLK1/PLL1_CLK1	C9 B0_L15_N	MIPI_CSI_CLK1
DIFFIO_B0_16P/GCLK17/PLL0_CLK2/PLL1_CLK2	B9 B0_L16_P	ETH_MDIO
DIFFIO_B0_16N/GCLK16/PLL0_CLK3/PLL1_CLK3	A9 B0_L16_N	ETH_MDC
DIFFIO_B0_17P/GCLK15/PLL0_CLK4/PLL1_CLK4	D11 B0_L17_P	ETH_RX_DV
DIFFIO_B0_17N/GCLK14/PLL0_CLK5/PLL1_CLK5	C11 B0_L17_N	ETH_RXC
DIFFIO_B0_18P/GCLK13/PLL0_CLK6/PLL1_CLK6	C10 B0_L18_P	MIPI_CSI_CLK_P
DIFFIO_B0_18N/GCLK12/PLL0_CLK7/PLL1_CLK7	A10 B0_L18_N	MIPI_CSI_CLK_N
DIFFIO_B0_19P	G9 B0_L19_P	ETH_TXC
DIFFIO_B0_19N/VREF_B0	F9 B0_L19_N	ETH_TX_EN
DIFFIO_B0_20P	B11 B0_L20_P	MIPI_CSI_D2_P
DIFFIO_B0_20N	A11 B0_L20_N	MIPI_CSI_D2_N
DIFFIO_B0_21P	G11 B0_L21_P	
DIFFIO_B0_21N	F10 B0_L21_N	
DIFFIO_B0_22P	B12 B0_L22_P	MIPI_CSI_D0_P
DIFFIO_B0_22N	A12 B0_L22_N	MIPI_CSI_D0_N
DIFFIO_B0_23P	F11 B0_L23_P	
DIFFIO_B0_23N	E11 B0_L23_N	
DIFFIO_B0_24P	D12 B0_L24_P	
DIFFIO_B0_24N	C12 B0_L24_N	
DIFFIO_B0_27P	C13 B0_L27_P	MIPI_CSI_D3_P
DIFFIO_B0_27N	A13 B0_L27_N	MIPI_CSI_D3_N
DIFFIO_B0_28P	F12 B0_L28_P	
DIFFIO_B0_28N	E12 B0_L28_N	
DIFFIO_B0_29P	B14 B0_L29_P	ETH_TXD2
DIFFIO_B0_29N/VREF_B0	A14 B0_L29_N	ETH_TXD3
DIFFIO_B0_30P/STB_CTRL7	F13 B0_L30_P	ETH_TXD0
DIFFIO_B0_30N/STB_CTRL6	E13 B0_L30_N	ETH_TXD1
DIFFIO_B0_31P/STB_CTRL5	C15 B0_L31_P	MIPI_CSI_D1_P
DIFFIO_B0_31N/STB_CTRL4	A15 B0_L31_N	MIPI_CSI_D1_N
DIFFIO_B0_32P/STB_CTRL3	D14 B0_L32_P	ETH_RXD2
DIFFIO_B0_32N/STB_CTRL2	C14 B0_L32_N	ETH_RXD3
DIFFIO_B0_33P/STB_CTRL1	B16 B0_L33_P	ETH_RXD0
DIFFIO_B0_33N/STB_CTRL0	A16 B0_L33_N	ETH_RXD1

U-PGL25G-MBG324

G11,F10 F11,E11 D12,C12 F12,E12
蓝色字体8个引脚仅25G可用，50G不可用

棕色字体标识为底板拓展接口差分对IO

红色字体标识为专用IO

U1B

DIFFI_B1_0P/ADR25	F15	DDR3_CS_N
DIFFI_B1_0N/ADR24/VREF_B1	F16	DDR3_VREF
DIFFI_B1_7P/ADR23	C17	DDR3_A13
DIFFI_B1_7N/ADR22	C18	DDR3_A14
DIFFI_B1_8P/ADR21	F14	DDR3_RESET_N
DIFFI_B1_8N/ADR20	G14	DDR3_A11
DIFFI_B1_9P/ADR19	D17	DDR3_CKE
DIFFI_B1_9N/ADR18	D18	DDR3_A12
DIFFI_B1_10P/ADR17	H12	DDR3_A8
DIFFI_B1_10N/ADR16	G13	DDR3_A9
DIFFI_B1_11P/ADR15	E16	DDR3_A10
DIFFI_B1_11N/ADR14	E18	DDR3_A4
DIFFI_B1_12P/ADR13	K12	DDR3_WE_N
DIFFI_B1_12N/ADR12	K13	DDR3_BA2
DIFFI_B1_13P/ADR11	F17	DDR3_A7
DIFFI_B1_13N/ADR10	F18	DDR3_A2
DIFFI_B1_14P/ADR9	H13	DDR3_BA0
DIFFI_B1_14N/ADR8	H14	DDR3_BA1
DIFFI_B1_15P/ADR7	H15	DDR3_A0
DIFFI_B1_15N/ADR6	H16	DDR3_A1
DIFFI_B1_16P/ADR5	G16	DDR3_CLK_P
DIFFI_B1_16N/ADR4	G18	DDR3_CLK_N
DIFFI_B1_17P	J13	DDR3_A3
DIFFI_B1_17N	K14	DDR3_ODT
DIFFI_B1_18P/GCLK11/PLL0_CLK8/PLL1_CLK8	L12	DDR3_A5
DIFFI_B1_18N/GCLK10/PLL0_CLK9/PLL1_CLK9	L13	DDR3_A6
DIFFI_B1_19P/GCLK9/PLL0_CLK10/PLL1_CLK10	K15	DDR3_RAS_N
DIFFI_B1_19N/GCLK8/PLL0_CLK11/PLL1_CLK11	K16	DDR3_CAS_N
DIFFI_B1_21P/GCLK7/PLL2_CLK8/PLL3_CLK8	L15	DDR3_UDM
DIFFI_B1_21N/GCLK6/PLL2_CLK9/PLL3_CLK9	L16	DDR3_LDM
DIFFI_B1_22P/GCLK5/PLL2_CLK10/PLL3_CLK10	H17	DDR3_DQ4
DIFFI_B1_22N/GCLK4/PLL2_CLK11/PLL3_CLK11	H18	DDR3_DQ5
DIFFI_B1_23P/ADR3	J16	DDR3_DQ6
DIFFI_B1_23N/ADR2	J18	DDR3_DQ7
DIFFI_B1_24P/ADR1	K17	DDR3_DQS_P0
DIFFI_B1_24N/ADR0	K18	DDR3_DQS_N0
DIFFI_B1_25P/BFCS_N	L17	DDR3_DQ2
DIFFI_B1_25N/BFOE_N	L18	DDR3_DQ3
DIFFI_B1_26P/BFWE_N	M16	DDR3_DQ0
DIFFI_B1_26N/BLDC	M18	DDR3_DQ1
DIFFI_B1_28P/BHDC	N17	DDR3_DQ8
DIFFI_B1_28N	N18	DDR3_DQ9
DIFFI_B1_29P	P17	DDR3_DQ10
DIFFI_B1_29N	P18	DDR3_DQ11
DIFFI_B1_30P	N15	DDR3_DQS_P1
DIFFI_B1_30N	N16	DDR3_DQS_N1
DIFFI_B1_31P	T17	DDR3_DQ12
DIFFI_B1_31N	T18	DDR3_DQ13
DIFFI_B1_32P	U17	DDR3_DQ14
DIFFI_B1_32N	U18	DDR3_DQ15
DIFFI_B1_33P	M14	LED0
DIFFI_B1_33N/VREF_B1	N14	DDR3_VREF
DIFFI_B1_36P	L14	LED1
DIFFI_B1_36N	M13	R3 240R
DIFFI_B1_39P/WAKEUP	P15	LED2
DIFFI_B1_39N/DOUT_BUSY	P16	LED3

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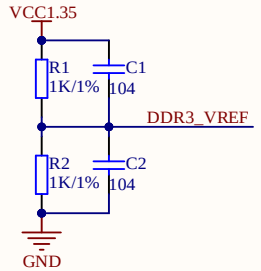

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Project: ATK-CFPGL25G_50GF.PrjPcb		
Size: A4	Author: ALIENTEK	
Date: 2024/2/5	Version: V1.2	Sheet: 1 of 7

U1C

DIFFIO_B2_0P/INIT_FLAG_N	U3		FPGA_INIT_FLAG_N
DIFFIO_B2_0N/CSO_N	V3		QSPI_CS
DIFFIO_B2_1P/D8	N5	B2_L1_P	KEY0
DIFFIO_B2_1N/D9	P6	B2_L1_N	KEY1
DIFFIO_B2_2P	T4	B2_L2_P	MIPI_CTP_RST
DIFFIO_B2_2N	V4	B2_L2_N	MIPI_CTP_INT
DIFFIO_B2_3P/D5	R3	B2_L3_P	MIPI_CTP_SDA
DIFFIO_B2_3N/D6	T3	B2_L3_N	MIPI_CTP_SCL
DIFFIO_B2_11P/D3	U5	B2_L11_P	REMOTE_IN
DIFFIO_B2_11N/D4	V5	B2_L11_N	BEEP
DIFFIO_B2_12P/D7	R5	B2_L12_P	
DIFFIO_B2_12N/RDWR_B/VREF_B2	T5	B2_L12_N	
DIFFIO_B2_13P	N6	B2_L13_P	
DIFFIO_B2_13N	P7	B2_L13_N	
DIFFIO_B2_14P	R7	B2_L14_P	KEY2
DIFFIO_B2_14N	T7	B2_L14_N	KEY3
DIFFIO_B2_15P	T6	B2_L15_P	
DIFFIO_B2_15N	V6	B2_L15_N	
DIFFIO_B2_16P	N7	B2_L16_P	
DIFFIO_B2_16N	P8	B2_L16_N	
DIFFIO_B2_17P	U7	B2_L17_P	
DIFFIO_B2_17N	V7	B2_L17_N	
DIFFIO_B2_19P	U8	B2_L19_P	
DIFFIO_B2_19N/VREF_B2	V8	B2_L19_N	
DIFFIO_B2_20P	M8	B2_L20_P	SDIO_D0
DIFFIO_B2_20N	N8	B2_L20_N	SDIO_D1
DIFFIO_B2_21P/GCLK29/PLL2_CLK1/PLL3_CLK1	T9	B2_L21_P	RS485_TX GBC_KEY
DIFFIO_B2_21N/GCLK28/PLL2_CLK0/PLL3_CLK0	V9		FPGA_PLL0_50MHz
DIFFIO_B2_22P/GCLK31/D14/PLL2_CLK3/PLL3_CLK3	R8	B2_L22_P	B2_L22_P
DIFFIO_B2_22N/GCLK30/D15/PLL2_CLK2/PLL3_CLK2	T8	B2_L22_N	B2_L22_N
DIFFIO_B2_23P/GCLK1/D13/PLL2_CLK5/PLL3_CLK5	U10	B2_L23_P	HDMI_FD0_P
DIFFIO_B2_23N/GCLK0/ECCLK/PLL2_CLK4/PLL3_CLK4	V10	B2_L23_N	HDMI_FD0_N
DIFFIO_B2_24P/GCLK3/PLL2_CLK7/PLL3_CLK7	R10	B2_L24_P	B2_L24_P
DIFFIO_B2_24N/GCLK2/PLL2_CLK6/PLL3_CLK6	T10	B2_L24_N	B2_L24_N
DIFFIO_B2_25P	U11	B2_L25_P	HDMI_FD1_P
DIFFIO_B2_25N	V11	B2_L25_N	HDMI_FD1_N
DIFFIO_B2_26P	M10	B2_L26_P	SDIO_D2
DIFFIO_B2_26N	N9	B2_L26_N	SDIO_D3
DIFFIO_B2_28P	N10	B2_L28_P	SDIO_SCK
DIFFIO_B2_28N	P11	B2_L28_N	SDIO_CMD
DIFFIO_B2_29P	T12	B2_L29_P	B2_L29_P
DIFFIO_B2_29N	V12	B2_L29_N	B2_L29_N 1WIRE_DQ
DIFFIO_B2_30P	R11	B2_L30_P	B2_L30_P
DIFFIO_B2_30N/VREF_B2	T11	B2_L30_N	B2_L30_N
DIFFIO_B2_31P	M11	B2_L31_P	B2_L31_P
DIFFIO_B2_31N	N11	B2_L31_N	B2_L31_N
DIFFIO_B2_32P/D11	U13	B2_L32_P	B2_L32_P
DIFFIO_B2_32N/D12	V13	B2_L32_N	B2_L32_N
DIFFIO_B2_33P/MODE_1	N12		FPGA_MODE1
DIFFIO_B2_33N/D10	P12	B2_L33_N	B2_L33_N RS485_RX GBC_LED
DIFFIO_B2_34P/D1	T14		QSPI_D2
DIFFIO_B2_34N/D2	V14		QSPI_D3
DIFFIO_B2_36P	U15	B2_L36_P	HDMI_FD2_P
DIFFIO_B2_36N	V15	B2_L36_N	HDMI_FD2_N
DIFFIO_B2_37P/D0	R13		QSPI_D1
DIFFIO_B2_37N/CS_N	T13		QSPI_D0
DIFFIO_B2_38P/CMPCLK	U16	B2_L38_P	HDMI_FCLK_P
DIFFIO_B2_38N/CMPMOSI	V16	B2_L38_N	HDMI_FCLK_N
DIFFIO_B2_39P/CFG_CLK	R15		QSPI_CLK
DIFFIO_B2_39N/MODE_0/CMPMISO	T15		FPGA_MODE0

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U1D

DIFFI_B3_0P	C2	B3_L0_P	UART1_RX
DIFFI_B3_0N/VREF_B3	C1	B3_L0_N	UART1_TX
DIFFI_B3_7P	F6	B3_L7_P	
DIFFI_B3_7N	F5	B3_L7_N	LCD_B6
DIFFI_B3_8P	E4	B3_L8_P	LCD_R3
DIFFI_B3_8N	D3	B3_L8_N	LCD_R2
DIFFI_B3_9P	H7	B3_L9_P	LCD_R5
DIFFI_B3_9N	G6	B3_L9_N	LCD_R4
DIFFI_B3_10P	D2	B3_L10_P	LCD_VSYNC
DIFFI_B3_10N	D1	B3_L10_N	LCD_HSYNC
DIFFI_B3_11P	F4	B3_L11_P	LCD_RST
DIFFI_B3_11N	F3	B3_L11_N	T_PEN
DIFFI_B3_12P	E3	B3_L12_P	LCD_G1
DIFFI_B3_12N	E1	B3_L12_N	LCD_G0
DIFFI_B3_13P	H6	B3_L13_P	T_SCK
DIFFI_B3_13N	H5	B3_L13_N	T_MISO
DIFFI_B3_14P	F2	B3_L14_P	LCD_B3
DIFFI_B3_14N	F1	B3_L14_N	LCD_B2
DIFFI_B3_15P	J7	B3_L15_P	LCD_BL
DIFFI_B3_15N	J6	B3_L15_N	LCD_DE
DIFFI_B3_16P	G3	B3_L16_P	LCD_R7
DIFFI_B3_16N	G1	B3_L16_N	LCD_R6
DIFFI_B3_17P	L7	B3_L17_P	LCD_G7
DIFFI_B3_17N	K6	B3_L17_N	LCD_G6
DIFFI_B3_18P/GCLK21/PLL0_CLK13/PLL1_CLK13	H4	B3_L18_P	LCD_B1
DIFFI_B3_18N/GCLK20/PLL0_CLK12/PLL1_CLK12	H3	B3_L18_N	LCD_B0
DIFFI_B3_19P/GCLK23/PLL0_CLK15/PLL1_CLK15	L5	B3_L19_P	LCD_CLK
DIFFI_B3_19N/GCLK22/PLL0_CLK14/PLL1_CLK14	K5	B3_L19_N	LCD_B7
DIFFI_B3_21P/GCLK25/PLL2_CLK13/PLL3_CLK13	K4	B3_L21_P	LCD_G5
DIFFI_B3_21N/GCLK24/PLL2_CLK12/PLL3_CLK12	K3	B3_L21_N	LCD_G4
DIFFI_B3_22P/GCLK27/PLL2_CLK15/PLL3_CLK15	H2	B3_L22_P	LCD_R1
DIFFI_B3_22N/GCLK26/PLL2_CLK14/PLL3_CLK14	H1	B3_L22_N	LCD_R0
DIFFI_B3_23P	J3	B3_L23_P	T_MOSI
DIFFI_B3_23N	J1	B3_L23_N	T_CS
DIFFI_B3_24P	L4	B3_L24_P	LCD_G3
DIFFI_B3_24N	L3	B3_L24_N	LCD_G2
DIFFI_B3_25P	K2	B3_L25_P	LCD_B5
DIFFI_B3_25N	K1	B3_L25_N	LCD_B4
DIFFI_B3_26P	L2	B3_L26_P	CMOS_PWDN
DIFFI_B3_26N	L1	B3_L26_N	CMOS_PCLK
DIFFI_B3_28P	M3	B3_L28_P	CMOS_D1
DIFFI_B3_28N	M1	B3_L28_N	CMOS_RESET
DIFFI_B3_29P	N2	B3_L29_P	CMOS_XCLK
DIFFI_B3_29N	N1	B3_L29_N	CMOS_D7
DIFFI_B3_30P	P2	B3_L30_P	CMOS_D6
DIFFI_B3_30N	P1	B3_L30_N	CMOS_D4
DIFFI_B3_31P	T2	B3_L31_P	CMOS_D5
DIFFI_B3_31N	T1	B3_L31_N	CMOS_D3
DIFFI_B3_32P	U2	B3_L32_P	CMOS_D2
DIFFI_B3_32N	U1	B3_L32_N	CMOS_D0
DIFFI_B3_33P	L6	B3_L33_P	CMOS_SDA
DIFFI_B3_33N/VREF_B3	M5	B3_L33_N	CMOS_HREF
DIFFI_B3_38P	P4	B3_L38_P	CMOS_VSYNC
DIFFI_B3_38N	P3	B3_L38_N	CMOS_SCL
DIFFI_B3_39P	N4	B3_L39_P	IIC_SDA
DIFFI_B3_39N/VREF_B3	N3	B3_L39_N	IIC_SCL EEPROM/RTC/6 AIXS

U-PGL25G-MBG324

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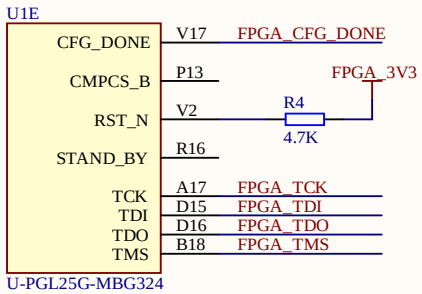
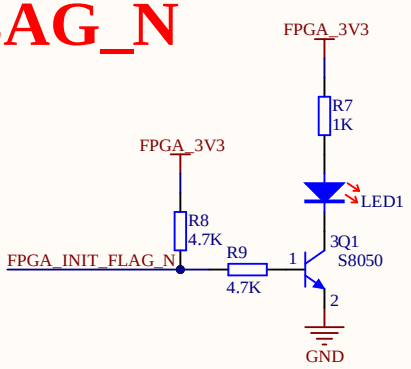
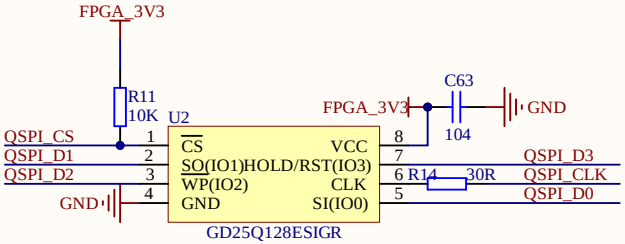
Project: ATK-CFPGL25G_50GF.PrjPcb		
Size: A4	Author: ALIENTEK	
Date: 2024/2/5	Version: V1.2	Sheet: 2 of 7



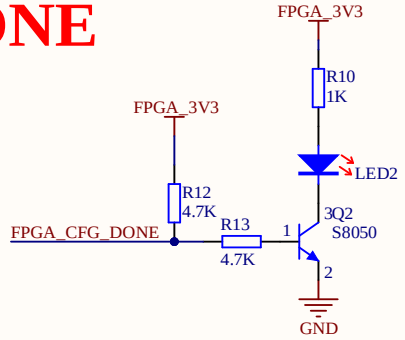
INIT_FLAG_N



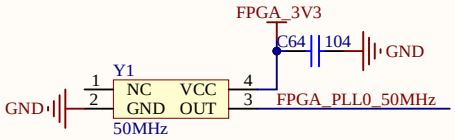
QSPI FLASH



CFG_DONE

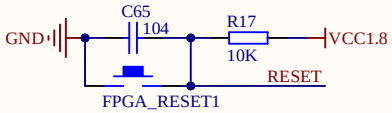


XTAL



IO_STATUS_C

RESET



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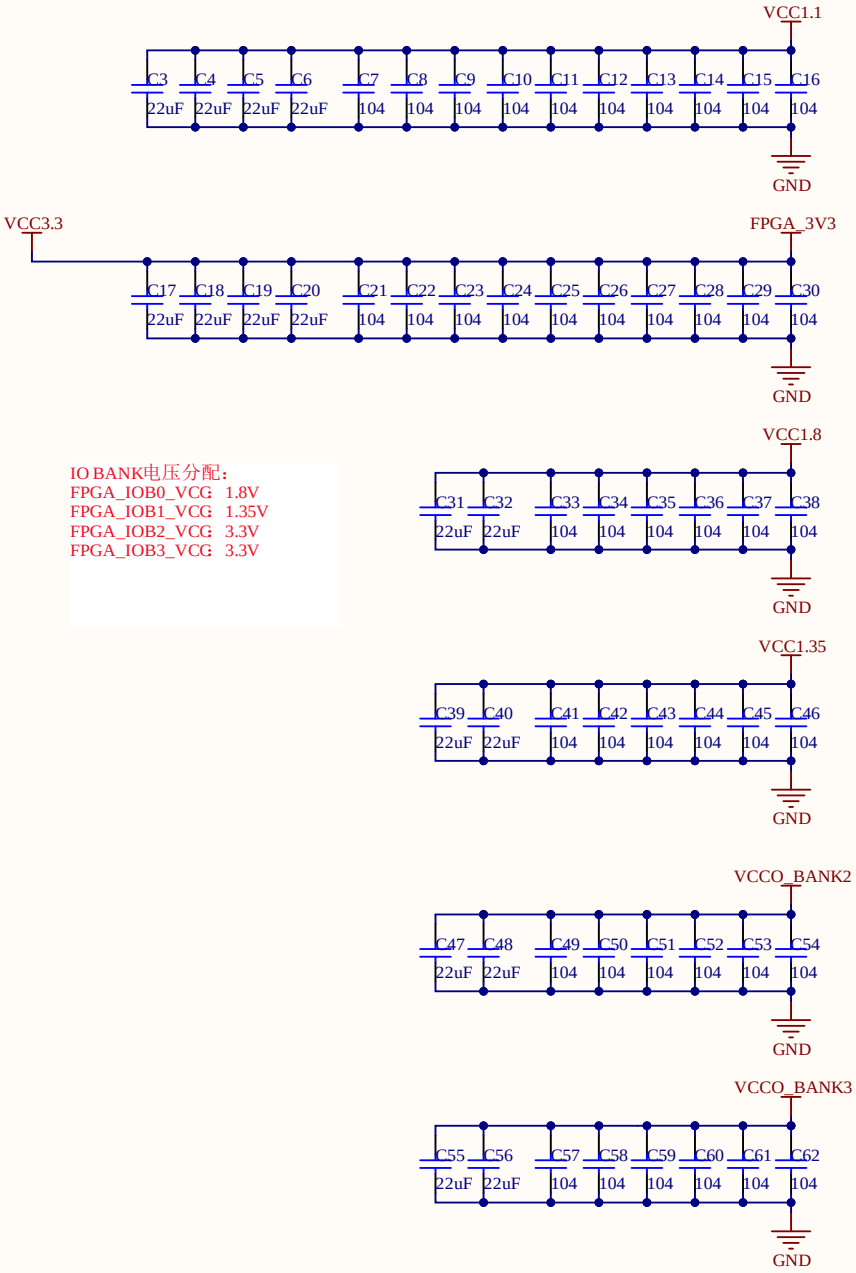
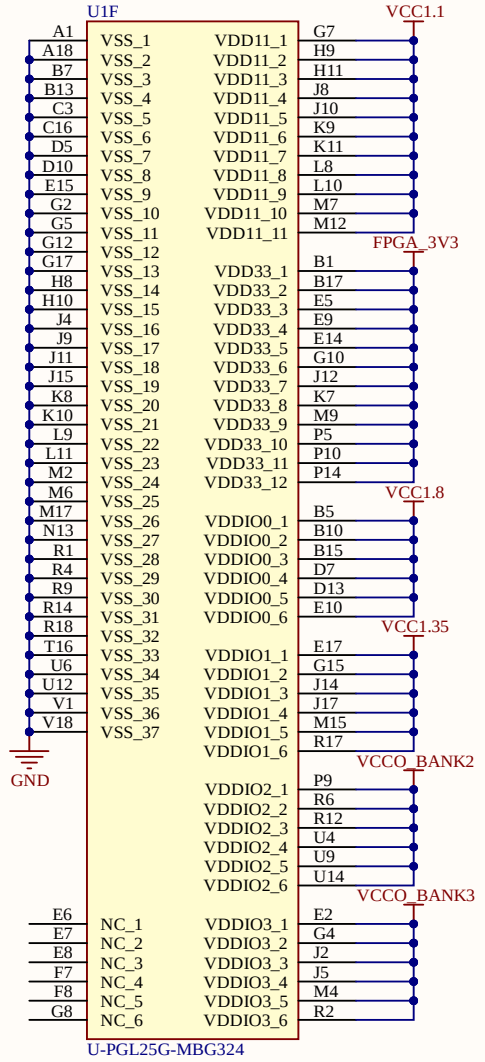
Project: ATK-CFPGL25G_50GF.PrjPcb			
Size: A4	Author: ALENTEK		
Date: 2024/2/5	Version: V1.2	Sheet: 3 of 7	

PWR



IO BANK电压分配：
FPGA_IOB0_VCC：1.8V
FPGA_IOB1_VCC：1.35V
FPGA_IOB2_VCC：3.3V
FPGA_IOB3_VCC：3.3V



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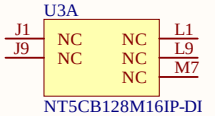
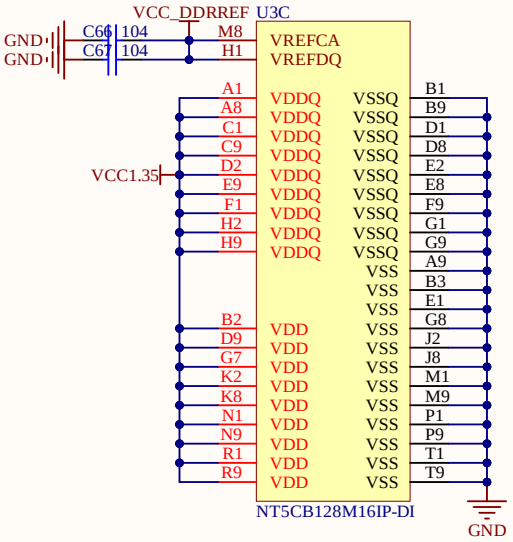
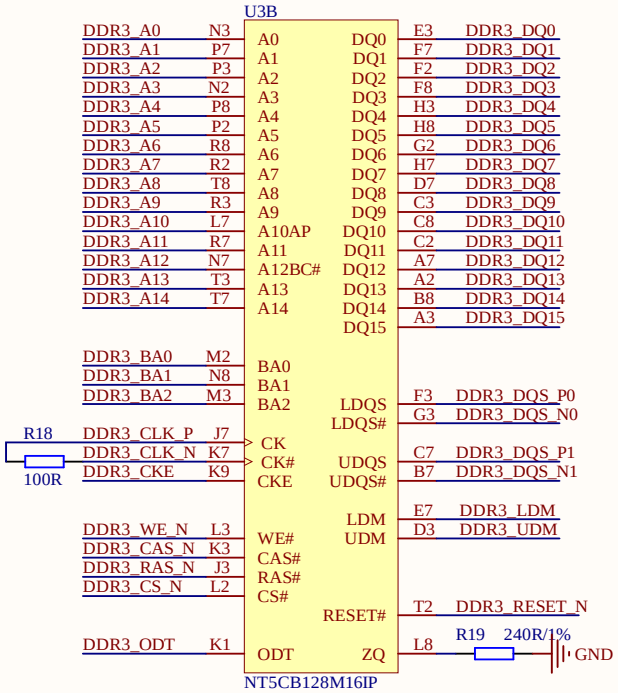
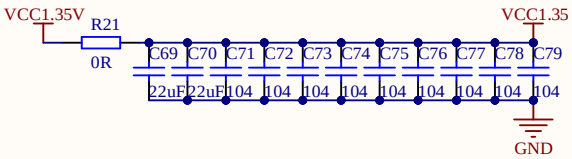
Size: A4	Author: ALIENTEK	
Date: 2024/2/5	Version: V1.2	Sheet: 4 of 7

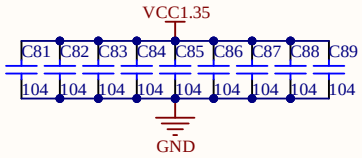
DDR

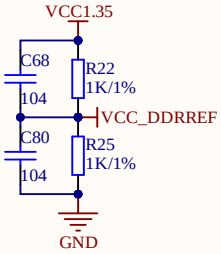


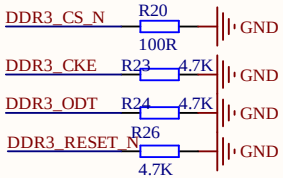






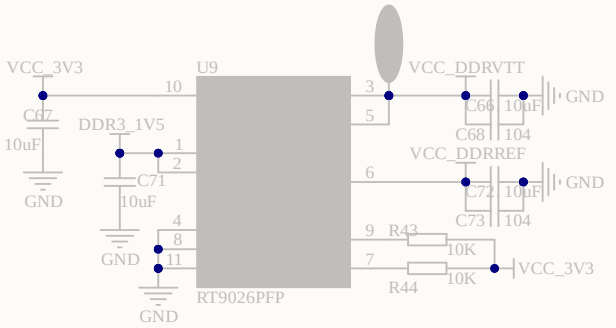


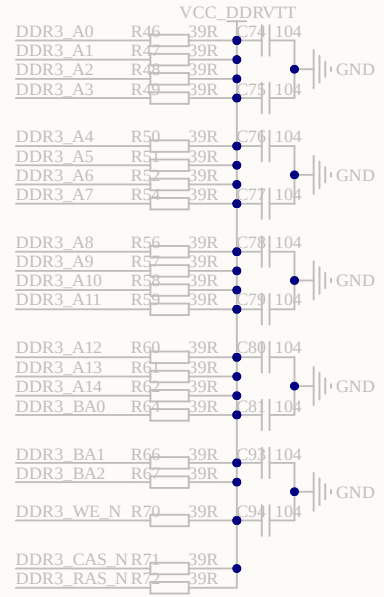




DDR_VTT

参考电源选择：VTT电源和电阻分压二选一





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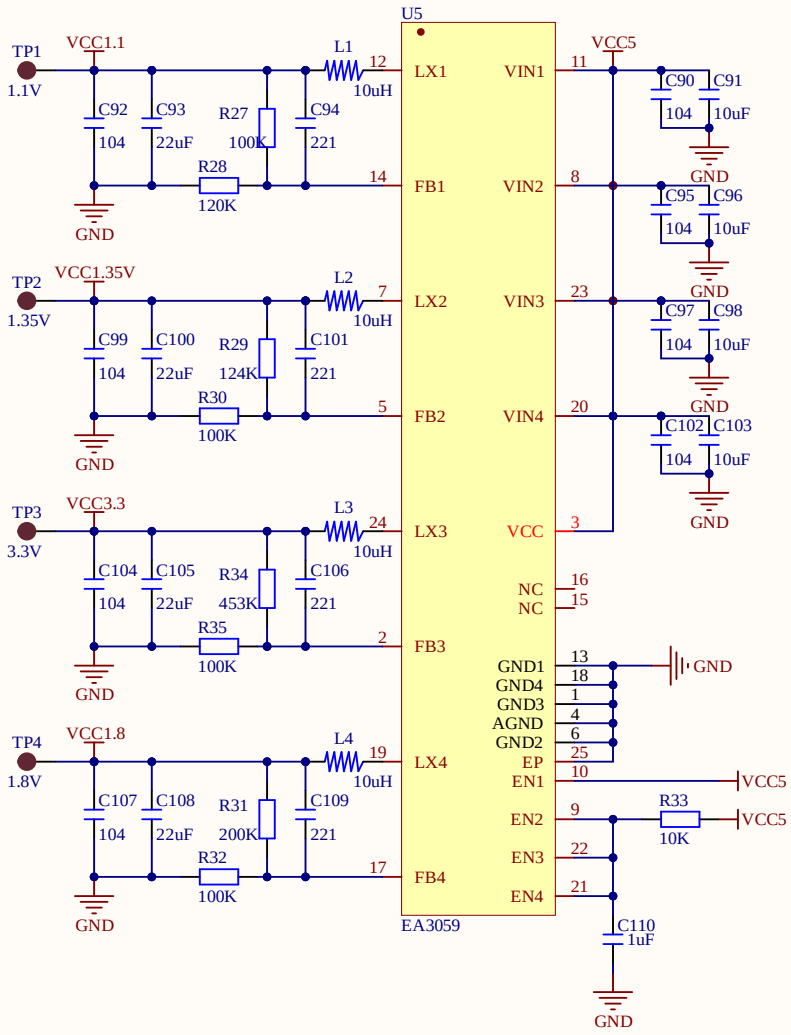
Project: ATK-CFPGL25G_50GF.PrjPcb			
Size: A4	Author: ALIENTEK		
Date: 2024/2/5	Version: V1.2	Sheet: 5 of 7	

PMIC



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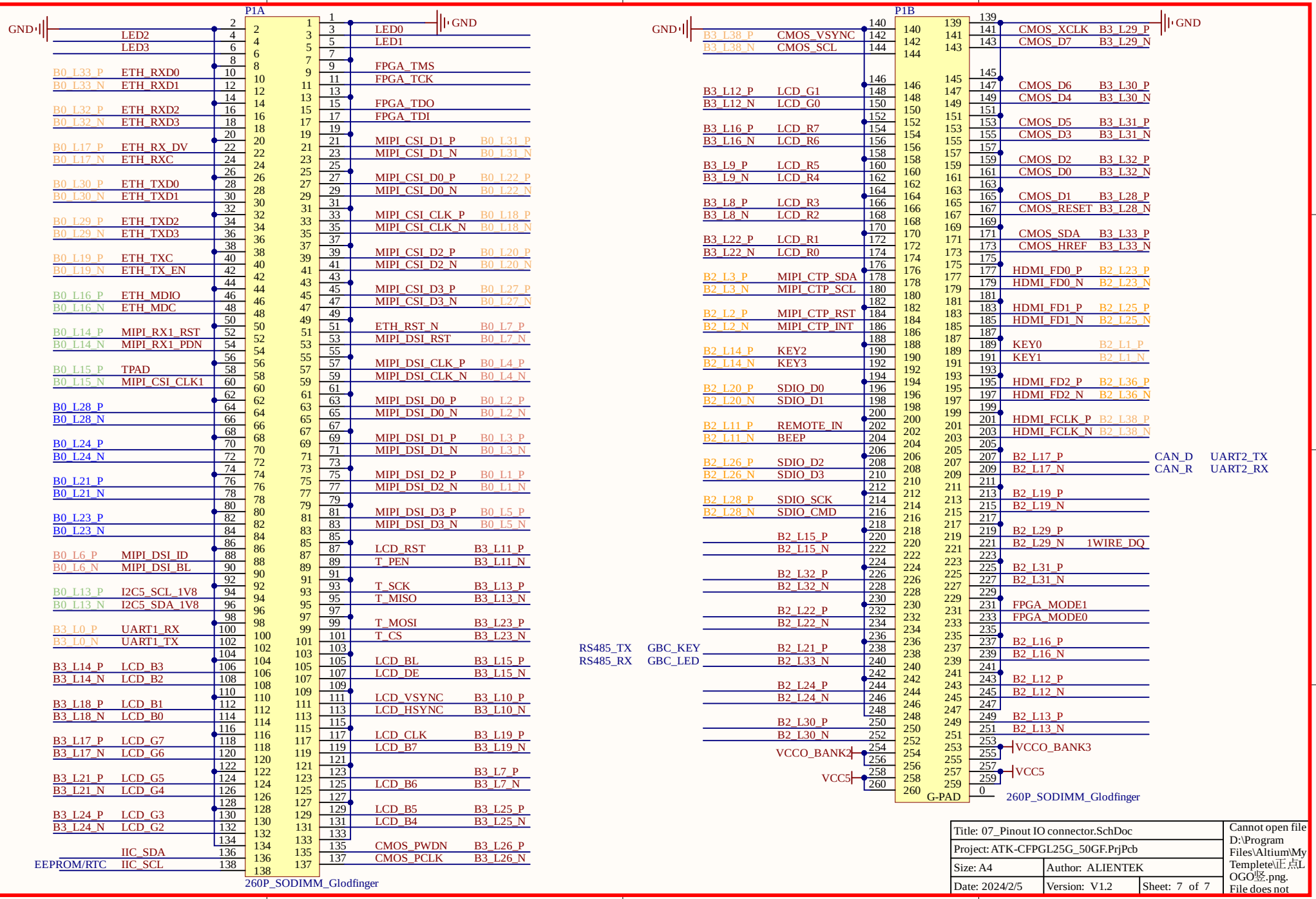
Project: ATK-CFPGL25G_50GF.PrjPcb			
Size: A4	Author: ALIENTEK		
Date: 2024/2/5	Version: V1.2	Sheet: 6 of 7	


P1A
GND
LED2
LED3
B0_L33_P ETH_RXD0
B0_L33_N ETH_RXD1
B0_L32_P ETH_RXD2
B0_L32_N ETH_RXD3
B0_L17_P ETH_RX_DV
B0_L17_N ETH_RXC
B0_L30_P ETH_TXD0
B0_L30_N ETH_TXD1
B0_L29_P ETH_TXD2
B0_L29_N ETH_TXD3
B0_L19_P ETH_TXC
B0_L19_N ETH_TX_EN
B0_L16_P ETH_MDIO
B0_L16_N ETH_MDC
B0_L14_P MIPI_RX1_RST
B0_L14_N MIPI_RX1_PDN
B0_L15_P TPAD
B0_L15_N MIPI_CSI_CLK1
B0_L28_P
B0_L28_N
B0_L24_P
B0_L24_N
B0_L21_P
B0_L21_N
B0_L23_P
B0_L23_N
B0_L6_P MIPI_DSI_ID
B0_L6_N MIPI_DSI_BL
B0_L13_P I2C5_SCL_1V8
B0_L13_N I2C5_SDA_1V8
B3_L0_P UART1_RX
B3_L0_N UART1_TX
B3_L14_P LCD_B3
B3_L14_N LCD_B2
B3_L18_P LCD_B1
B3_L18_N LCD_B0
B3_L17_P LCD_G7
B3_L17_N LCD_G6
B3_L21_P LCD_G5
B3_L21_N LCD_G4
B3_L24_P LCD_G3
B3_L24_N LCD_G2
IIC_SDA
EEPROM/RTC IIC_SCL
GND
LED0
LED1
FPGA_TMS
FPGA_TCK
FPGA_TDO
FPGA_TDI
MIPI_CSI_D1_P B0_L31_P
MIPI_CSI_D1_N B0_L31_N
MIPI_CSI_D0_P B0_L22_P
MIPI_CSI_D0_N B0_L22_N
MIPI_CSI_CLK_P B0_L18_P
MIPI_CSI_CLK_N B0_L18_N
MIPI_CSI_D2_P B0_L20_P
MIPI_CSI_D2_N B0_L20_N
MIPI_CSI_D3_P B0_L27_P
MIPI_CSI_D3_N B0_L27_N
ETH_RST_N B0_L7_P
MIPI_DSI_RST B0_L7_N
MIPI_DSI_CLK_P B0_L4_P
MIPI_DSI_CLK_N B0_L4_N
MIPI_DSI_D0_P B0_L2_P
MIPI_DSI_D0_N B0_L2_N
MIPI_DSI_D1_P B0_L3_P
MIPI_DSI_D1_N B0_L3_N
MIPI_DSI_D2_P B0_L1_P
MIPI_DSI_D2_N B0_L1_N
MIPI_DSI_D3_P B0_L5_P
MIPI_DSI_D3_N B0_L5_N
LCD_RST B3_L11_P
T_PEN B3_L11_N
T_SCK B3_L13_P
T_MISO B3_L13_N
T_MOSI B3_L23_P
T_CS B3_L23_N
LCD_BL B3_L15_P
LCD_DE B3_L15_N
LCD_VSYNC B3_L10_P
LCD_HSYNC B3_L10_N
LCD_CLK B3_L19_P
LCD_B7 B3_L19_N
B3_L7_P
LCD_B6 B3_L7_N
LCD_B5 B3_L25_P
LCD_B4 B3_L25_N
CMOS_PWDN B3_L26_P
CMOS_PCLK B3_L26_N
260P_SODIMM_Glodfinger
P1B
GND
B3_L38_P CMOS_VSYNC
B3_L38_N CMOS_SCL
B3_L12_P LCD_G1
B3_L12_N LCD_G0
B3_L16_P LCD_R7
B3_L16_N LCD_R6
B3_L9_P LCD_R5
B3_L9_N LCD_R4
B3_L8_P LCD_R3
B3_L8_N LCD_R2
B3_L22_P LCD_R1
B3_L22_N LCD_R0
B2_L3_P MIPI_CTP_SDA
B2_L3_N MIPI_CTP_SCL
B2_L2_P MIPI_CTP_RST
B2_L2_N MIPI_CTP_INT
B2_L14_P KEY2
B2_L14_N KEY3
B2_L20_P SDIO_D0
B2_L20_N SDIO_D1
B2_L11_P REMOTE_IN
B2_L11_N BEEP
B2_L26_P SDIO_D2
B2_L26_N SDIO_D3
B2_L28_P SDIO_SCK
B2_L28_N SDIO_CMD
B2_L15_P
B2_L15_N
B2_L32_P
B2_L32_N
B2_L22_P
B2_L22_N
RS485_TX GBC_KEY B2_L21_P
RS485_RX GBC_LED B2_L33_N
B2_L24_P
B2_L24_N
B2_L30_P
B2_L30_N
VCCO_BANK2
VCC5
GND
CMOS_XCLK B3_L29_P
CMOS_D7 B3_L29_N
CMOS_D6 B3_L30_P
CMOS_D4 B3_L30_N
CMOS_D5 B3_L31_P
CMOS_D3 B3_L31_N
CMOS_D2 B3_L32_P
CMOS_D0 B3_L32_N
CMOS_D1 B3_L28_P
CMOS_RESET B3_L28_N
CMOS_SDA B3_L33_P
CMOS_HREF B3_L33_N
HDMI_FD0_P B2_L23_P
HDMI_FD0_N B2_L23_N
HDMI_FD1_P B2_L25_P
HDMI_FD1_N B2_L25_N
KEY0 B2_L1_P
KEY1 B2_L1_N
HDMI_FD2_P B2_L36_P
HDMI_FD2_N B2_L36_N
HDMI_FCLK_P B2_L38_P
HDMI_FCLK_N B2_L38_N
B2_L17_P CAN_D UART2_TX
B2_L17_N CAN_R UART2_RX
B2_L19_P
B2_L19_N
B2_L29_P
B2_L29_N 1WIRE_DQ
B2_L31_P
B2_L31_N
FPGA_MODE1
FPGA_MODE0
B2_L16_P
B2_L16_N
B2_L12_P
B2_L12_N
B2_L13_P
B2_L13_N
VCCO_BANK3
VCC5
G-PAD
260P_SODIMM_Glodfinger
Title: 07_Pinout IO connector.SchDoc
Project: ATK-CFPGL25G_50GF.PrjPcb
Size: A4
Author: ALIENTEK
Date: 2024/2/5
Version: V1.2
Sheet: 7 of 7
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