Logos Family FPGAs Analog-to-Digital Converter (ADC) Module User Guide

(UG020009, V1.2)

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Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.2	22.01.2021	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
ADC	Analog to Digital Converter
SNR	Signal to Noise Ratio
DNL	Differential Nonlinearity
INL	Integral Nonlinearity
DRP	Dynamic Reconfiguration Port
MSPS	Mega sample per second
VFS	voltage full swing

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Chapter 1 General Introduction

The Logos Family FPGA products provide ADC resources, each with 12 channels, of which 10 are analog input pins multiplexed with GPIO and the other 2 are dedicated analog input pins. The scanning method of these 12 channels is flexibly controlled by the FPGA. Users can read and write the ADC control registers through User Logic, configure the ADC's working mode and channel selection, etc., and obtain the ADC channel conversion results and values for calibration such as offset and gain error by reading the ADC's status registers.

Below are some features of the ADC:

- Resolution: 10-bit;
- Sample rate: 1MSPS;
- 12 channels, of which 10 are analog input channels multiplexed with GPIO, and 2 are dedicated analog input channels;
- The internal and external reference voltage VREF for the ADC is 2.5V;
- The analog supply voltage is 3.3V;
- Integrated temperature sensor

Chapter 2 Detailed Introduction

2.1 ADC Schematic

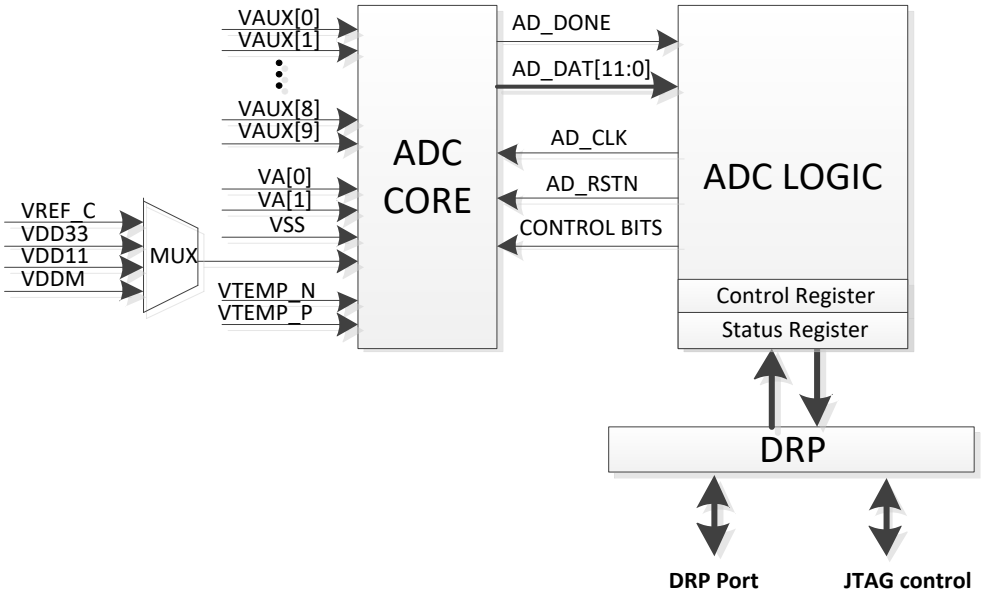

Figure2-1 ADC Schematic

The ADC includes 12 user-connectable analog input channels (where VAUX[9:0] is multiplexed with GPIO and VA[1:0] are dedicated analog input channels), with some channels used for on-chip voltage and temperature monitoring. Channel 12 is VSS, this signal is grounded; Channel 13 is MUX output, selectable for monitoring internal chip voltage; Channel 14 is VTEMP_N, and Channel 15 is VTEMP_P; Channels 14 and 15 form a differential pair to collect internal chip temperature signals.

In Figure2-1 above, the ADC_CORE module samples the analog input signal and converts it into 12-bit digital data transmitted to the ADC_LOGIC module. Users can read and write registers in ADC_LOGIC through the DRP interface to control the ADC's working mode and read the ADC's status and conversion values.

2.2 Features

Table 2-1 List of ADC Features

Function	Description
Access register through DRP	Users can access and operate registers via the DRP method
Error calibration	Calibrate the ADC conversion values, including offset calibration and gain calibration
Chip monitor	Monitor several on-chip power supply voltages and on-chip temperatures
Channel Scan	Sequentially scan and convert multiple ADC channels
Single-ended and differential mixed scanning	The channels scanned by the ADC can be arbitrarily selected as single-ended, differential, unipolar, or bipolar
Result averaging	The ADC can average the conversion results
User event driven	Users can manually control the conversion of the ADC event driven sampling
Single channel mode	Users can arbitrarily select a channel for individual operation

2.3 ADC Input Mode

There are three forms of ADC input signals: single-end for single-ended input, diff for differential input, and diff mode is divided into bipolar and unipolar.

The single-end diagram is shown in Figure2-2 below:

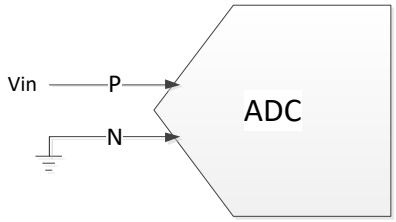

Figure2-2 Single-End Mode Input Diagram

Where Vin≥0V, the negative phase is connected to the internal ground.

The unipolar diagram is shown in Figure2-3 below:

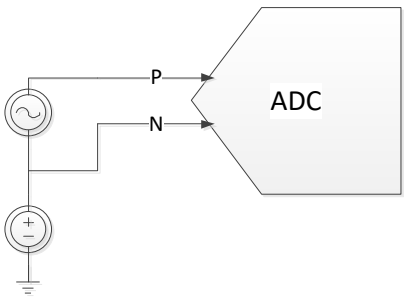

Figure2-3 Unipolar Mode Input Diagram

The positive phase's signal voltage must be higher than that of the negative phase.

The bipolar mode includes pseudo-differential and full-differential, each illustrated in Figure2-4 / Figure2-5 below:

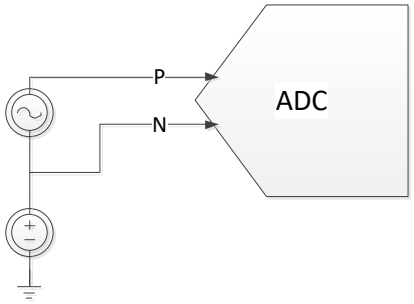

Figure2-4 Bipolar Mode Pseudo-Differential Input Diagram

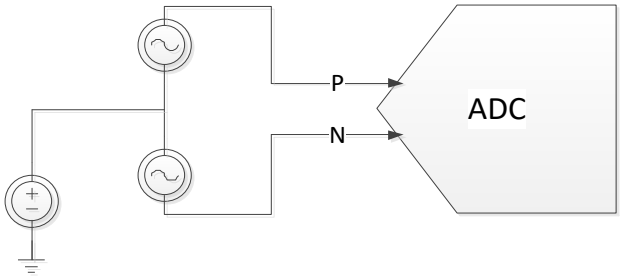

Figure2-5 Bipolar Mode Full-Differential Input Diagram

To ensure proper conversion, the signal requirements for each mode are as follows:

Table 2-2 ADC Input Analog Signal

Mode	**Vp**	**Vn**	**Vcm**		**Vp-Vn**
			Min	**Max**	
Single-end	[0,VFS]	N/A	N/A	N/A	[0,VFS]
Unipolar	$\frac{1}{2}$VFS + VCM − 0.3	$\frac{1}{2}$VFS + VCM − 2	N/A	N/A	[0,VFS]
Bipolar	N/A	N/A	$\frac{1}{2}$VFS + VCM − 2	$\frac{1}{2}$VFS + VCM − 0.3	[$-\frac{1}{2}$VFS, $\frac{1}{2}$VFS]

Where VFS is the full swing, and VCM is the common-mode voltage selected by the internal comparator (refer to VCM configuration in Control Registers section).

2.4 ADC Signal Conversion

The ADC can operate under different full swings (FS) and modes (unipolar, bipolar, and single-end). If various errors (including offset error and gain error) are not considered, the ADC conversion characteristic is as shown in the figure below:

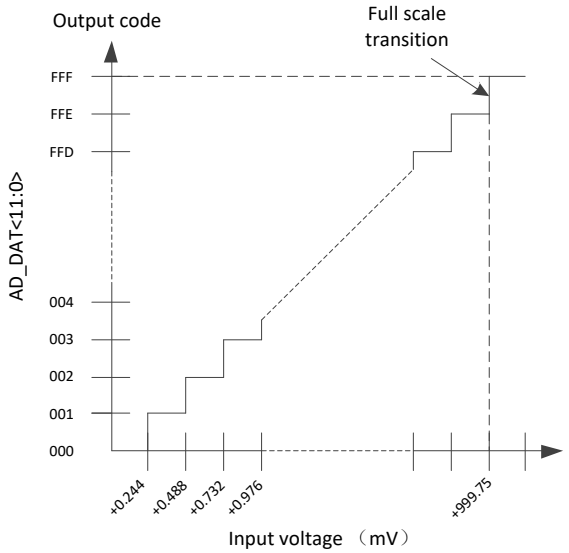

Figure2-6 ADC Analog-to-Digital Transfer Function in Unipolar and Single-End Mode

The figure above shows the transfer function when measuring in the range of 0 to +1V (FS=1V) for unipolar or single-end mode, where LSB=1V/4096=0.244mV. When the input voltage is 0V, the output code is 000 (if Vp<Vn, then the output is 000); when the input is 1V, the output code is FFF (if Vp-Vn>1V, the output is FFF, similar to other ranges).

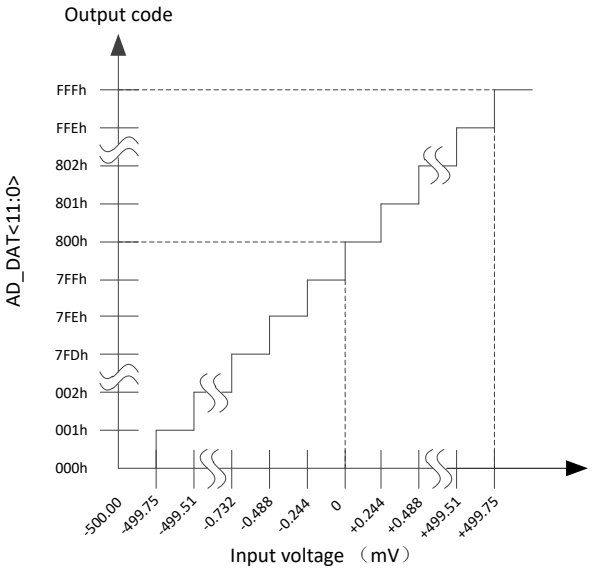

Figure2-7 ADC Digital Transfer Function in Bipolar Mode

Figure2-7 above shows the transfer function in bipolar mode with a measurement range of -0.5V to +0.5V (FS=1V), where the LSB=1V/4096=0.244mV. When the input voltage is -500mV, the output code is 000h (outputs 000 when less than -500mV, similar for other ranges); when the input voltage is 0V, the output code is 800h; when the input voltage is +500mV, the output code is FFFh (outputs FFF when greater than 500mV, similar for other ranges).

Below is the timing associated with the ADC's converting of analog signals into digital signals.

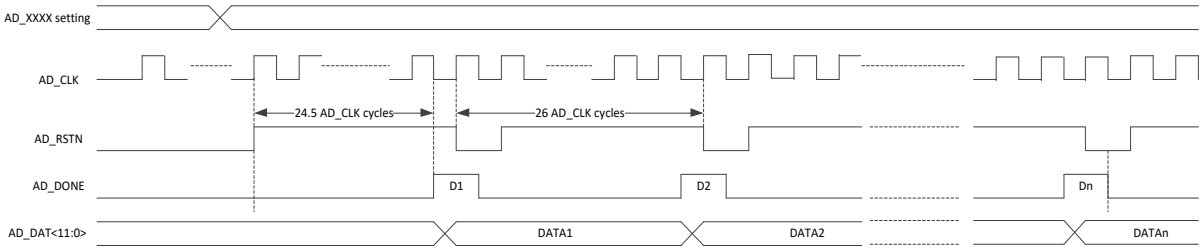

Figure 2-8 Timing Diagram of ADC Analog-to-Digital Conversion

As shown in, Figure 2-8 AD_CLK is a division clock of DCLK, with the division factor controlled by DIV3 to DIV0 (configuration register, 00h). AD_XXXX represents the data for the control register, AD_RSTN signal is the internal reset signal controlling the ADC conversion cycle, AD_DONE signal going high signifies the end of a conversion, as seen in Figure 2-8, a complete conversion cycle requires at least 26 AD_CLK cycles, AD_DAT is the 12-bit conversion result.

2.5 On-Chip Detection

The ADC provides monitoring functions for on-chip voltage and temperature, capable of monitoring the FPGA on-chip voltages of VDD33, VDD11, and VDDM with standard input values of 3.3V ±10%, 1.1V ±10%, and 1.18V ±10% respectively.

Temperature detection is achieved by measuring the voltage difference between two differently biased PN junctions, namely VTEMP_P and VTEMP_N.

Table 2-3 Typical Voltages Monitored by ADC

Item	Value Before Voltage Dividing (V)			Value After Voltage Dividing (V)			Voltage Divider Ratio	Best Range
	Min	Typical	Max	Min	Typical	Max		
VDD33	2.97	3.3	3.63	0.33	0.3667	0.403	1/9	0.5V
VDD11	0.99	1.1	1.21	0.248	0.275	0.303	1/4	0.5V
VDDM	1.062	1.18	1.298	0.266	0.295	0.325	1/4	0.5V

In single-channel mode, FS needs to be selected properly; in default mode, the 0.5V range is preselected.

2.6 Register Description

Figure2-9 shows the register access interface for the ADC. There are two types of registers in the ADC: control registers and status registers. All registers can be accessed through DRP or Jtag. The 25 16-bit registers (DADDR[7:0]=00h to 18h) can be operated through the address DADDR[7:0]. The first five addresses (DADDR[7:0]=00h to 04h) are control registers, which include various control operations for the ADC and can be read and written; the latter 20 addresses (DADDR[7:0]=05h to 18h) are status registers (with 05h being a reserved position without stored data), which store the results of the ADC conversion calculations and are read-only.

Upon entering user mode, the ADC automatically loads user configuration parameters into the corresponding control registers. Users can modify the relevant registers using DI[15:0] and address bits DADDR[7:0] through DRP, or access and modify them via Jtag.

After modifying the control registers, it is recommended to reset ADC.

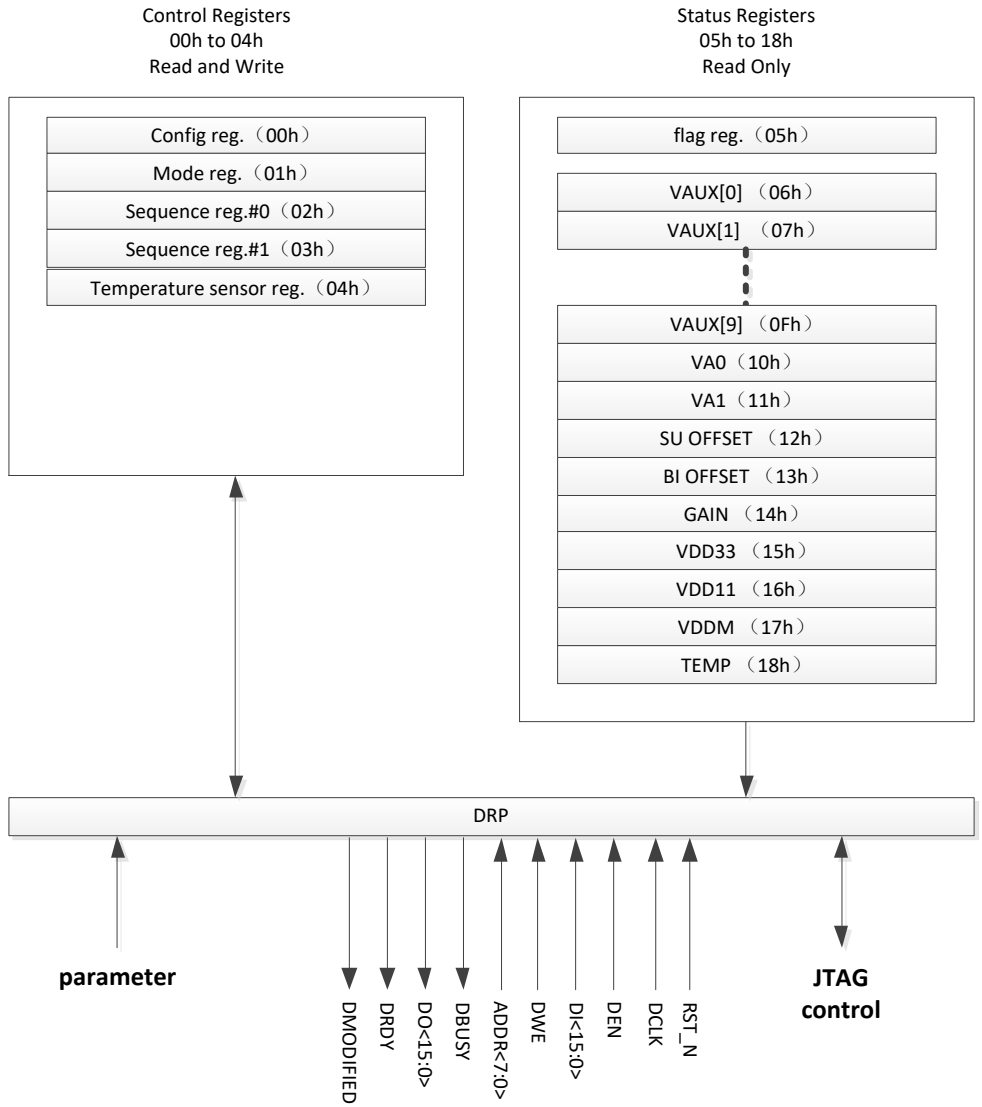

Figure2-9 Register Interface

2.6.1 Control Registers

The ADC has five 16-bit control registers with addresses ranging from 00h to 04h (see Figure2-9). These register configurations are used for specific operations of the ADC. All ADC functions are controlled through these registers.

Users can set the ADC to a specified mode through specific settings. Entering user mode will automatically load user configurations.

After reconfiguration of the control register (JTAG or DRP), it is recommended that the user reset the ADC once with RST_N.

After reconfiguring the control register, if the user wants to use the initial configuration again, they need to reset with LOADSC_N (low level for at least one AD_CLK cycle, with ADC_CLK being the clock divided from DCLK), and also reset the ADC with RST_N.

2.6.1.1 Configuration Register

The configuration register (00h) is used for configuring some internal modules of the ADC. The specific allocation of each bit is shown in Figure2-10 below.

The value of the configuration register can be modified through DRP or Jtag during the ADC operating. The specific definition of each bit is shown in Table 2-4.

Config Reg. ADDR[4:0]=00h	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
	AVG1	AVG0	CAL1	CAL0	REF	CREF	FS2	FS1	FS0	VCM2	VCM1	VCM0	DIV3	DIV2	DIV1	DIV0

Figure2-10 Configuration Register Bit Allocation

Table 2-4 Configuration Register 00h

Bit	Item	RW	Description
DI15 to DI14	AVG1 to AVG0	R/W	By configuring, set the amount of sample averaging of the ADC output CODE (refer to Table 2-5 for specific configurations)
DI13 to DI12	CAL1 to CAL0	R/W	Select the calibration application of the ADC (refer to Table 2-6 for details)
DI11	REF	R/W	Select reference source for ADC: 1'b0: Internal reference source (generated by BGP) 1'b1: External reference source
DI10	CREF	R/W	Select the reference source for ADC calibration 1'b0: Connect to ADC power supply VDD11 1'b1: External reference source (same as the external reference source selected by DI11)
DI9 to DI7	FS2 to FS0	R/W	Configure the full swing of the ADC (refer to Table 2-7 for specific configurations)
DI6 to DI4	VCM2 to VCM0	R/W	Configure the common-mode voltage of the ADC's internal comparator (refer to Table 2-8 for specific configurations)
DI3 to DI0	DIV3 to DIV0	R/W	Change the frequency of the ADC sampling clock by configuring different values to divide the input clock (refer to Table 2-9 for specific configurations)

Table 2-5 Averaging Control

AVG1	AVG0	Description
0	0	1
0	1	16
1	0	64
1	1	256

Table 2-6 Calibration Selection

CAL1	CAL0	Description
0	0	ADCs offset and gain calculation disable
0	1	ADCs offset calculation enable
1	X	ADCs offset and gain calculation enable

Table 2-7 Full Swing Control

FS2	FS1	FS0	Description
0	0	0	VFS=0.5V; Bipolar mode: ±0.25V; unipolar and single-end mode: 0~0.5V
0	0	1	VFS=0.6V; Bipolar mode: ±0.3V; unipolar and single-end mode: 0~0.6V
0	1	0	VFS=0.7V; Bipolar mode: ±0.35V; unipolar and single-end mode: 0~0.7V
0	1	1	VFS=0.8V; Bipolar mode: ±0.4V; unipolar and single-end mode: 0~0.8V
1	0	0	VFS=0.9V; Bipolar mode: ±0.45V; unipolar and single-end mode: 0~0.9V
1	0	1	VFS=1.0V; Bipolar mode: ±0. 5V; unipolar and single-end mode: 0~1V
1	1	0	VFS=1.1V; Bipolar mode: ±0.55V; unipolar and single-end mode: 0~1.1V
1	1	1	VFS=1.2V; Bipolar mode: ±0.6V; unipolar and single-end mode: 0~1.2V

Note: VFS indicates full swing.

Table 2-8 Common-Mode Voltage Control

VCM2	VCM1	VCM0	Common-Mode Voltage
0	0	0	VCM=0.8V
0	0	1	VCM=0.9V
0	1	0	VCM=1.0V
0	1	1	VCM=1.1V
1	0	0	VCM=1.2V
1	0	1	VCM=1.3V
1	1	0	VCM=1.4V
1	1	1	VCM=1.5V

Table 2-9 Sampling Clock Control

DIV3	DIV2	DIV1	DIV0	Division Ratio
0	0	0	0	2
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15

DIV3	DIV2	DIV1	DIV0	Division Ratio
1	1	1	1	16

2.6.1.2 Mode Register

The mode register (01h) is used to configure the working modes of the ADC, with the allocation of each bit as shown in Figure2-11 below.

Like the configuration register, the value of the mode register can be modified at any time during ADC operating through DRP. The definition of each bit is shown in Table 2-10.

	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Mode Reg. ADDR[4:0]=01h	SEQ1	SEQ0	CE	1M	clksw	0	0	0	MUX1	MUX0	CH3	CH2	CH1	CH0	BU	DS

Figure2-11 Mode Register Bit Allocation

Note: The bits configured to 0 in the figure above should always be configured as 0.

Table 2-10 Mode Registers 01h

Bit	Name	RW	Description
DI15 to DI14	SEQ1 to SEQ0	R/W	Sequence mode selection (see Table 2-11 for details)
DI13	CE	R/W	Continuous sampling mode and event-driven sampling mode 1’b0: continue 1’b1: event-drive
DI12	1M	R/W	1MSPS mode control bit: 1'b0: Working mode set by [SEQ1:SEQ0] 1'b1: Working mode is 1MSPS mode
DI11	clksw	R/W	Clock switch control bit, after entering user mode, if the control bit is: 1'b0: Select clk_osc as the ADC clock 1'b1: Select DCLK as the ADC clock
DI7 to DI6	MUX1 to MUX0	R/W	This control bit is valid in single channel mode and 1MSPS mode for selecting the channel 13 input signal, with [MUX1, MUX0] encoding as follows: 2'b0X: Select VDD33 2'b10: Select VDD11 2'b11: Select VDDM
DI5 to DI2	CH3 to CH0	R/W	This control bit is valid in single channel mode and 1MSPS mode for channel selection, to be used in conjunction with DS and BU (refer to Table 2-12 for details)
DI1 to DI0	BU and DS	R/W	This control bit is valid in single channel mode and 1MSPS mode (refer to definitions for SEQ1, SEQ0, and 1M) where DS selects either single-end or diff mode. Since diff mode includes bipolar and unipolar, the selection is made by BU, with [BU,DS] encoding as follows: 2’bX0: single-end; 2’b01: unipolar; 2’b11: bipolar

Table 2-11 Sequence Mode Selection

SEQ1	SEQ0	Description	Comment
0	0	Default sequence mode	Supports up to 0.5MSPS
0	1	Single pass sequence mode	Supports up to 0.5MSPS
1	0	Continuous sequence mode	Supports up to 0.5MSPS
1	1	Single channel mode (sequence mode off)	Supports up to 0.5MSPS

When CH3:CH0 values are from 0000 to 1011, the corresponding table is as follows:

Table 2-12 Channel Selection

[BU,DS]	CH3	CH2	CH1	CH0	Channel Number
X0 (single-end)	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
	1	0	0	1	9
	1	0	1	0	10
	1	0	1	1	11
01 (unipolar)	0	0	0	0	0/1
	0	0	0	1	
	0	0	1	0	2/3
	0	0	1	1	
	0	1	0	0	4/5
	0	1	0	1	
	0	1	1	0	6/7
	0	1	1	1	
	1	0	0	0	8/9
	1	0	0	1	
	1	0	1	0	10/11
	1	0	1	1	
11 (bipolar)	0	0	0	0	0/1
	0	0	0	1	
	0	0	1	0	2/3
	0	0	1	1	
	0	1	0	0	4/5

[BU,DS]	CH3	CH2	CH1	CH0	Channel Number
	0	1	0	1	
	0	1	1	0	6/7
	0	1	1	1	
	1	0	0	0	8/9
	1	0	0	1	
	1	0	1	0	10/11
	1	0	1	1	

Based on the table above, the summary is as follows:

When the BU/DS is set as single-end (00 or 10) mode, configure CH3–CH0 to select the corresponding channel, for example, when CH3–CH0 is set to 0000, channel 0 is selected, and when CH3–CH0 is set to 0001, channel 1 is selected.

When the BU/DS is set as unipolar/bipolar (01 or 11) mode, channels 0 and 1, channels 2 and 3, ..., and channels 10 and 11 will form pairs. For example, when CH3–CH0 is set to 0000 or 0001, the pair of channel 0 and channel 1 is selected, and so on.

When CH3:CH0 values are from 1100 to 1111, in this case, no selection will be made regardless of the BU/DS values.

2.6.1.3 Scan Control Registers (Sequence Registers)

The Scan Control Registers (02h to 03h) are used to configure and control the ADC in sequence mode. The sequence registers are used to select the channels for the sequence, while sequence register1 controls the channel's working mode (diff and single-end, unipolar and bipolar). The allocation of each bit of the register is shown in Figure2-12.

The values of the Scan Control Registers can be modified at any time during operating via DRP. The definitions of each bit are shown in Table 2-13, Table 2-14, Table 2-15.

	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Sequence Reg.#0 ADDR[4:0]=02h	0	0	0	0	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
Sequence Reg#1. ADDR[4:0]=03h	0	0	0	0	BU5	DS5	BU4	DS4	BU3	DS3	BU2	DS2	BU1	DS1	BU0	DS0

Figure2-12 Scan Control Register Bit Allocation

Note: DS (diff and single-end), BU (bipolar and unipolar)

Here, DS[0:5] is for selecting single-end and differential modes for VAUX[0]/VAUX[1],

VAUX[2]/VAUX[3], VAUX[4]/VAUX[5]...VAUX[8]/VAUX[9] respectively, 0: single-end; 1: diff.

On the premise of selection for differential mode, BU[0:5] is for selecting the form of diff for VAUX[0]/VAUX[1], VAUX[2]/VAUX[3], VAUX[4]/VAUX[5]...VAUX[8]/VAUX[9] respectively, 0: unipolar; 1: bipolar. (For the definitions of single-end, unipolar, and bipolar, refer to DS (diff and single-end) and BU (bipolar and unipolar)).

In single-end mode, a pair of channels such as VAUX[0] and VAUX[1] operate in single-end mode; in unipolar mode, VAUX[0] and VAUX[1] form a differential pair, with VAUX[0] as the N side and VAUX[1] as the P side; in bipolar mode, VAUX[0] and VAUX[1] form a differential pair.

Table 2-13 Channel Selection Register 02h in Single-End Mode

Bit	Item	RW	Description
DI0	C0	R/W	Control input channel VAUX[0] C0 controls whether to scan, 0: disable, 1: enable
DI1	C1	R/W	Control input channel VAUX[1] C1 controls whether to scan, 0: disable, 1: enable
DI2	C2	R/W	Control input channel VAUX[2] C2 controls whether to scan, 0: disable, 1: enable
DI3	C3	R/W	Control input channel VAUX[3] C3 controls whether to scan, 0: disable, 1: enable
DI4	C4	R/W	Control input channel VAUX[4] C4 controls whether to scan, 0: disable, 1: enable
DI5	C5	R/W	Control input channel VAUX[5] C5 controls whether to scan, 0: disable, 1: enable
DI6	C6	R/W	Control input channel VAUX[6] C6 controls whether to scan, 0: disable, 1: enable
DI7	C7	R/W	Control input channel VAUX[7] C7 controls whether to scan, 0: disable, 1: enable
DI8	C8	R/W	Control input channel VAUX[8] C8 controls whether to scan, 0: disable, 1: enable
DI9	C9	R/W	Control input channel VAUX[9] C9 controls whether to scan, 0: disable, 1: enable
DI10	C10	R/W	Control input channel VA0 C10 controls whether to scan, 0: disable, 1: enable
DI11	C11	R/W	Control input channel VA1 C11 controls whether to scan, 0: disable, 1: enable

Table 2-14 Channel Selection Register 02h in Diff Mode

Bit	Item	RW	Description
DI0/DI1	C0/C1	R/W	Control input channels VAUX[0]/VAUX[1] C0/C1 control whether to scan, 00/01/10: disable, 11: enable
DI2/DI3	C2/C3	R/W	Control input channels VAUX[2]/VAUX[3] C2/C3 control whether to scan, 00/01/10: disable, 11: enable
DI4/DI5	C4/C5	R/W	Control input channels VAUX[4]/VAUX[5] C4/C5 control whether to scan, 00/01/10: disable, 11: enable
DI6/DI7	C6/C7	R/W	Control input channels VAUX[6]/VAUX[7] C6/C7 control whether to scan, 00/01/10: disable, 11: enable
DI8/DI9	C8/C9	R/W	Control input channels VAUX[8]/VAUX[9] C8/C9 control whether to scan, 00/01/10: disable, 11: enable
DI10/DI11	C10/C11	R/W	Control input channels VA[0]/VA[1] C10/C11 control whether to scan, 00/01/10: disable, 11: enable

Table 2-15 Scan Mode Register 03h

Bit	Item	Controlled Channel	RW	Description
DI1/ DI0	BU0/ DS0	VAUX[0]/VAUX[1]	R/W	X0: single-end 01: unipolar (VAUX[0]/VAUX[1] form a pair) 11: bipolar (VAUX[0]/VAUX[1] form a pair)
DI3/DI2	BU1/ DS1	VAUX[2]/VAUX[3]	R/W	X0: single-end 01: unipolar 11: bipolar
DI5/ DI4	BU2/ DS2	VAUX[4]/VAUX[5]	R/W	X0: single-end 01: unipolar 11: bipolar
DI7/ DI6	BU3/ DS3	VAUX[6]/VAUX[7]	R/W	X0: single-end 01: unipolar 11: bipolar
DI9 /DI8	BU4/ DS4	VAUX[8]/VAUX[9]	R/W	X0: single-end 01: unipolar 11: bipolar
DI11/ DI10	BU5/ DS5	VA[0]/VA[1]	R/W	X0: single-end 01: unipolar 11: bipolar

2.6.1.4 Temperature Sensor Control Registers

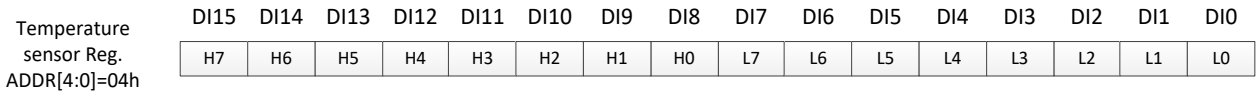

Figure2-13 Bit Allocation of Temperature Sensor Control Registers

The Temperature Sensor Control Register (04h) is used to configure and control the temperature detection thresholds (upper and lower limits). The upper 8 bits (DI15–DI8) set the upper limit for temperature detection, and the lower 8 bits (DI7–DI0) set the lower limit.

A setting of 0 corresponds to 0K (-273.15℃), the threshold setting step is 5.8K, allowing users to set their own detection thresholds through calculations:

$$Ttemp\_th=DIcode*16*0.364K-273.15℃$$

Common settings are as follows:

Table 2-16 Settings of Temperature Sensor Control Register

Bit	Item	RW	Value	Temperature
DI[15:8]	H[7:0]	R/W	8’b01000101	128℃
DI[7:0]	L[7:0]	R/W	8’b00111000	53℃

2.6.2 Status Registers

Status Registers (05h to 18h) are used to store the conversion results for each channel as well as the

offset and gain error values for calibration (while 05h is flag register). All status registers can only be read by the user through DRP and cannot be written to. Status registers 06h–11h are defined for both single-end and diff modes, with single-end mode showing in Table 2-16.

Table 2-17 Status Register Values in Single-End Mode

Address	RW	Description
06h to 0Fh	R	Stores the conversion values of VAUX[0:9]
10h	R	Stores the conversion value of VA0
11h	R	Stores the conversion value of VA1

Diff mode is shown in the following Table 2-17:

Table 2-18 Status Register Values in Diff Mode

Address	RW	Description
06h to 07h	R	Stores the differential conversion value of VAUX[1]/VAUX[0]
08h to 09h	R	Stores the differential conversion value of VAUX[3]/VAUX[2]
0Ah to 0Bh	R	Stores the differential conversion value of VAUX[5]/VAUX[4]
0Ch to 0Dh	R	Stores the differential conversion value of VAUX[7]/VAUX[6]
0Eh to 0Fh	R	Stores the differential conversion value of VAUX[9]/VAUX[8]
10h to 11h	R	Stores the differential conversion value of VA1/VA0

PS: In differential mode, paired address bits store the same value

Definitions of other registers:

Table 2-19 Definitions of Status Register Values for Addresses 12h–18h

Address	RW	Description
12h	R	Stores the offset calibration values of the ADC in single-end and unipolar modes
13h	R	Stores the offset calibration value of the ADC in bipolar mode
14h	R	Stores the calibration value of Gain error
15h	R	Stores the conversion value of power supply VDD33
16h	R	Stores the conversion value of power supply VDD11
17h	R	Stores the conversion value of power supply VDDM
18h	R	Stores the conversion value of the on-chip temperature sensor

The temperature conversion formula is as follows:

Temp=CODE(temp)*0.364K-273.15 ℃-7.5 ℃

Status registers can be read at any time; the pulse on LOGIC_DONE indicates an update has occurred.

The Offset Calibration Registers (12h and 13h) store the ADC's offset error calibration values, which have polarity with the most significant bit as the sign bit. For example, if the ADC has an offset of +10 LSBs, assuming a range of 1V, this would be about 10×250uV=2.5mV.

The Gain Calibration Register (14h) stores the ADC's Gain error calibration value, which also has polarity. Each bit represents an error of 1/2048 (approximately 0.05%), with the highest bit GAIN[11] of GAIN[11:0] being the sign bit.

2.7 ADC Working Modes

The operation of ADC working modes is primarily based on the configuration values of the control registers. Overall, the ADC working modes include default mode, single-pass mode, continuous scan mode, and single-channel mode. Additionally, users can enter the event driven mode by selecting event driven. ADC operation also includes temperature detection, calibration errors, etc.

2.7.1 Default Mode

The ADC will enter default mode under two circumstances:

One is during the programming phase, where the ADC operates in default mode, completely independent of register control.

The other is by setting the SEQ[1:0] in the mode register to 2'b00, which puts the ADC into default mode. In this mode, the ADC will automatically scan and convert the temperature and voltage on the chip, storing the conversion values in the status registers. The ADC will automatically perform calibration, which is obtained after averaging over 16 samples. In this mode, the ADC is not affected or controlled by most other register configuration values (except for SEQ, which allows selection of the reference source via REF and CREF, whether to switch to DCLK, and temperature detection threshold settings; all others are not controllable).

In the default mode, when reading with JTAG, the user must first write to a register (it is recommended to write to ADC Register 0x00, with the value 0x0000), then read from the register.

The scan list is shown in the table below.

Table 2-20 Default Mode Scan List

No.	Channel	Address	Description
1	Error calculation	12h/13h /14h	Calculate OFFSET and GAIN errors
2	VDD33	15h	Perform detection and conversion for VDD33 power supply
3	VDD11	16h	Perform detection and conversion for VDD11 power supply
4	VDDM	17h	Perform detection and conversion for VDDM

No.	Channel	Address	Description
			power supply
5	Temperature	18h	Convert on-chip temperature

The specific process is 1→2→3→4→5→2→3→..., where step 1 is only performed once initially, followed by a continuous loop between steps 2 to 5.

2.7.2 Single-Pass Mode

To enter single-pass mode, the SEQ[1:0] in the register must be written as 2'b01. In this mode, the ADC will scan from the lower channel bit to the higher channel bit once, and then stop scanning.
Upon entering this mode, if CAL1 and CAL0 (in the Configuration Register, 00h) are not 2'b00, a calibration value calculation (i.e., error calculation) will be performed first, and the offset error calibration value and gain error calibration value will be written into the corresponding status registers before starting the conversion of the selected channel signal.
Assuming the register configuration is shown in the table below:

Table 2-21 Single-Pass Mode Register Configuration

Register	Value
Configuration Register (00h)	7E8Fh
Mode Register (01h)	4000h
Sequence Register 0 (02h)	0FE4h
Sequence Register 1 (03h)	0D00h

The comparison diagram is as follows:

	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Config Reg. ADDR<4:0>=00h	AVG1	AVG0	CAL1	CAL0	REF	CREF	FS2	FS1	FS0	VCM2	VCM1	VCM0	DIV3	DIV2	DIV1	DIV0
	0	1	1	1	1	1	1	0	1	0	0	0	1	1	1	1
	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Mode Reg. ADDR<4:0>=01h	SEQ1	SEQ0	CE	0	0	0	0	0	MUX1	MUX0	CH3	CH2	CH1	CH0	BU	DS
	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Sequence Reg.#0 ADDR<4:0>=02h	0	0	0	0	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
	0	0	0	0	1	1	1	1	1	1	1	0	0	1	0	0
	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Sequence Reg#1. ADDR<4:0>=03h	0	0	0	0	BU5	DS5	BU4	DS4	BU3	DS3	BU2	DS2	BU1	DS1	BU0	DS0
	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0

Figure2-14 Single-Pass Mode Register Bit Configuration

For the aforementioned configuration values, the specific ADC process is to first perform error calculation, then sequentially scan channels 2→5→6→7→8→9→10→11, loop 16 times for the average, then perform error correction, and finally enter the values into the corresponding status registers. The ADC input clock frequency is F_{CLK}, and if the division ratio is N, then the ADC operating clock $F_{ADC}=F_{CLK}/N$, and in this mode, the ADC cannot support a 1M sampling rate.

2.7.3 Continuous Scanning Mode

Continuous scanning mode is similar to single-pass mode, where it will continuously cycle through scans until the scan mode is changed. The channel to be scanned can be selected at any time during ADC operation, and when changing the control register configuration values, the ADC will reset, and the values in the status registers will be cleared. Except for changing the SEQ[1:0] configuration to 2'b10, other configurations follow the values for the single-pass mode mentioned above.

2.7.4 Single-Channel Mode

To enter single-channel mode, SEQ[1:0] in the mode register (01h) must be set to 2'b11. In this mode, the user needs to select the channel for analog-to-digital conversion, and the channel selection is controlled through CH3 to CH0 in the mode register (01h), in conjunction with the DS and BU bits.

In single-channel mode, if channel 12/13/14/15 is selected, an appropriate range must be chosen. The ADC input clock frequency is F_{CLK}, and if the division ratio is N, then the ADC working clock $F_{ADC}=F_{CLK}/N$, and in this mode, the ADC cannot support a 1M sampling rate.

Without averaging, the LOGIC_DONE frequency can be calculated as follows:

Scanning channel-0/1/2/3/4/5/6/7/8/9:

$$F_{LOGIC\_DONE} = \frac{F_{ADC}}{51}$$

Scanning channel-10/11:

$$F_{LOGIC\_DONE} = \frac{F_{ADC}}{50}$$

Scanning channel-12/13/14/15:

$$F_{LOGIC\_DONE} = \frac{F_{ADC}}{43}$$

2.7.5 1MSPS Mode

The 1MSPS mode is controlled by register 1M (Mode Register, 01h), and when set to 1, it enters 1MSPS mode. Upon entering this mode, if CAL1 and CAL0 (in the Configuration Register, 00h) are not 2'b00, a calibration value calculation (i.e., error calculation) will be performed first, and the offset error calibration value and gain error calibration value will be written into the corresponding status registers before starting the conversion of the selected channel signal.

The data from the ADC conversion is directly stored in the corresponding register without averaging or calibration (the user is responsible for calculating and eliminating data errors). Once a pulse of LOGIC_DONE occurs, it indicates that the data update is complete, and the user can read the data through JTAG/DRP.

2.7.6 Event Driven Mode

Event driven mode is controlled by register CE (Mode Register, 01h); when set to 1, the device enters event driven mode. In event driven mode, the user controls it through the CONVST signal; each pulse triggers a conversion. When a pulse of LOGIC_DONE appears, it signifies that the data update is complete, which also indicates the completion of a user-controlled operation. In event driven mode, if the user opts for calibration, the ADC will automatically enter the calculation phase first; pulses of the CONVST signal input by the user are valid during this process, but the conversion will not occur until the calculation phase is complete.

Among the various modes, the default mode and the 1MSPS mode do not have event driven; the event driven in single-channel mode is identical to that in continuous scan mode.

2.7.7 Calibration

Calibration includes OFFSET and Gain calibration; when CAL1 and CAL0 are set to 00, no calibration calculation is performed. The entire calibration function is divided into two phases: error calculation and error correction.

For the ADC's OFFSET and Gain calibration process, it is worth noting that Gain calibration always follows OFFSET calibration. That is, during the error calculation phase, the offset is calculated first, followed by gain calculation; during the error correction phase, the offset is eliminated first, followed by gain calibration. Taking single channel mode as an example, ADC operation includes three stages: error calculation, conversion, and error correction. Among those, the error calculation stage is performed only once initially, followed by a continuous cycle of conversion, error correction, conversion, error correction, and so on.

Evrytime after error correction is completed, the LOGIC module outputs a pulse of the LOGIC_DONE signal (a high level lasting for one AD_CLK cycle), indicating that the status register has been updated (meaning the results of the previous conversion have been written to the register), and the latest conversion result can be read from the status register.

In single-end or unipolar mode, if the result after calibration exceeds 4095, the value stored in the channel register is fixed at 4095; if the result is less than 0, it is fixed at 0; if the result is in between, the value stored is the calibrated result.

In bipolar mode, if the result after calibration is greater than 2047, the value stored in the channel register is set to 2047; if the result is less than -2048, it is set to -2048; if the result is in between, the value stored is the calibrated result.

2.7.8 Temperature Sensing

Using the status register (18h) conversion results as the basis to judge the temperature sensing results. When the temperature exceeds the upper limit, it jumps high, and when it returns to the lower limit, it reverts to low. The judgment results are output through OVER_TEMP. This function is only effective in the default mode after programming, as shown in the example below:

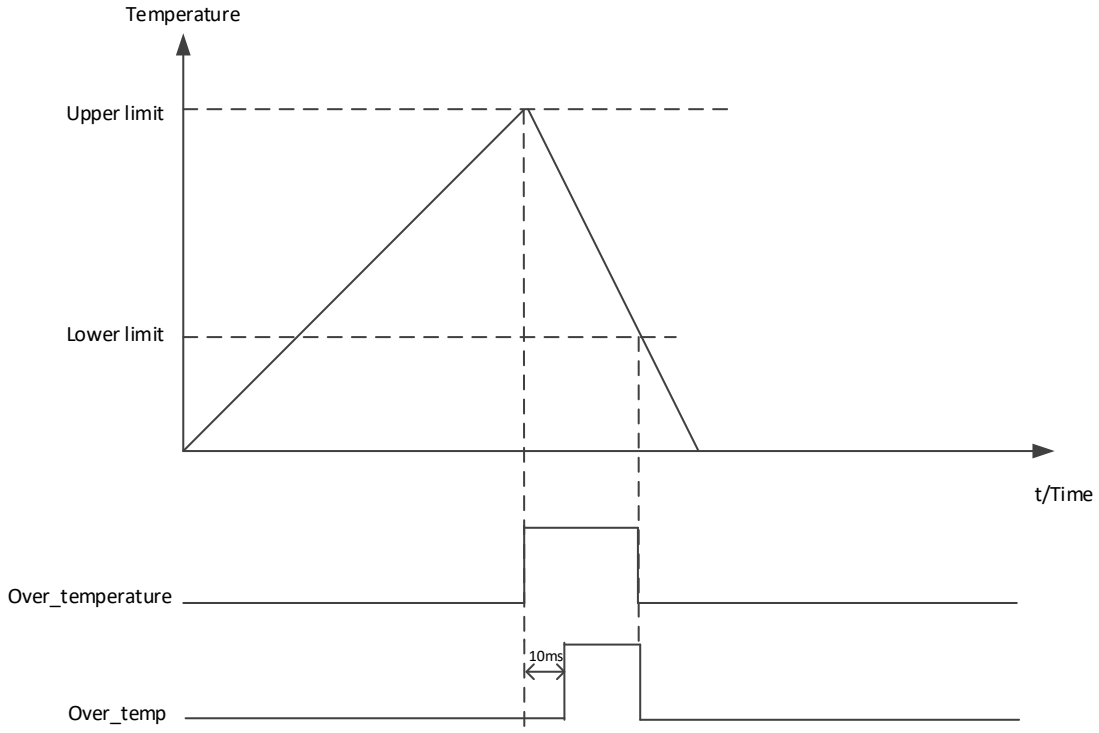

Figure2-15 Temperature Detection Analysis Chart

Users set the upper and lower thresholds for temperature detection through the temperature sensor control register. Refer to the configuration bit description for specific settings.

When the temperature status register value exceeds the threshold upper limit (status register value greater than H[7:0]), the internal register over_temperature is pulled high. When the temperature status register value falls below the threshold lower limit (status register value less than L[7:0]), the internal register over_temperature is pulled low.

To eliminate glitches in the over_temp output, after the internal register over_temperature is pulled high (maintaining a high level), an internal counter operating in the clk_osc clock domain begins counting. Only when it counts to 20'h80000 (approximately 10ms) output a high level OVER_TEMP. If the temperature changes within 10ms and the internal register over_temperature is pulled high and then low, the output signal over_temp will remain low.

The temperature conversion formula for status register 18h is as follows:

Temp=CODE(temp)*0.364K-273.15 ℃-7.5 ℃

Temperature threshold setting formula:

$$Ttemp\_th=DIcode*16*0.364K-273.15\ ℃$$

2.8 ADC GTP

The Logos Family products provide an ADC resource. Users can control the operation of the ADC by configuring the corresponding register parameters and registers can also be read/written through DRP.

2.8.1 ADC GTP Block Diagram

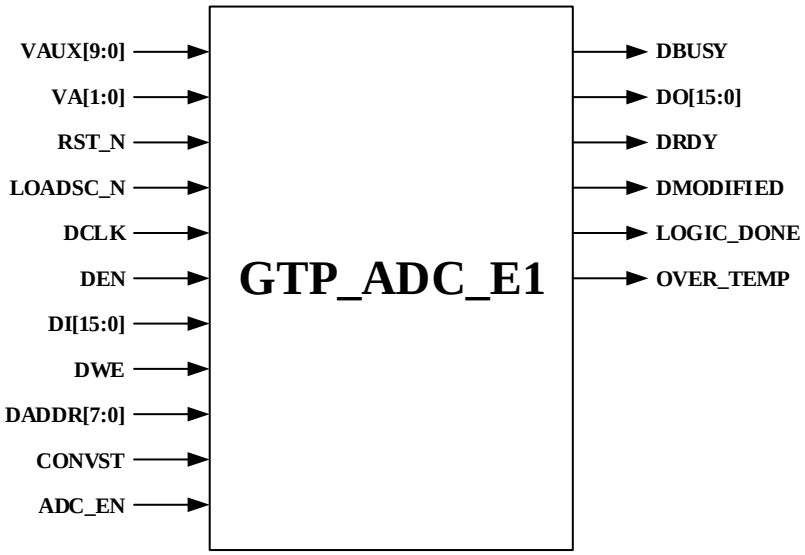

Figure2-16 GTP_ADC_E1 Block Diagram

2.8.2 ADC Port List

Table 2-22 GTP_ADC_E1 Port List

Port	Orientation	Function Description
VAUX[9:0]	Input	Multiplexed pin analog signal input
VA[1:0]	Input	Dedicated channel analog input
RST_N	Input	ADC system reset signal (active-low)
LOADSC_N	Input	ADC control register download static configuration value signal (active-low)
DCLK	Input	DRP clock
DEN	Input	Operation enable; initiates a read/write operation when active-high
DI[15:0]	Input	Data input
DWE	Input	Write enable, 1'b0: read operation; 1'b1: write operation;
DADDR[7:0]	Input	Address bits
CONVST	Input	Control signal for event driven mode, last at least 2 ADC_CLK cycles
ADC_EN	Input	ADC enable signal
DBUSY	Output	JTAG DRP operation flag, indicating that JTAG is performing DRP operation via JDRP instruction
DO[15:0]	Output	Data output
DRDY	Output	Operation completion flag (active-high)
DMODIFIED	Output	Control register modification flag, indicating that the control register has been written by JTAG DRP and the user has not yet performed DRP operation
LOGIC_DONE	Output	ADC status register update signal
OVER_TEMP	Output	ADC temperature alarm signal

2.8.3 Parameter List

Table 2-23 GTP_ADC_E1 Parameter List

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description	Mapped Register
AVERAGE	string	"1", "16", "64", "256"	"1"	Set the amount of ADC sample averaging	AVG0 to AVG1
CALIB	string	"NONE", "OFFSET", "OFFSET_GAIN"	"NONE"	ADC calibration setting "NONE": offset and gain calculation disable "OFFSET": offset calculation enable "OFFSET_GAIN": offset and gain calculation enable	CAL0 to CAL1
REFERENCE	string	"INTERNAL", "EXTERNAL"	"INTERNAL"	ADC reference source setting "INTERNAL": internal reference source "EXTERNAL": external reference source	REF
CALIB_ REFERENCE	string	"INTERNAL", "EXTERNAL"	"INTERNAL"	ADC calibration reference source setting "INTERNAL": internal reference source	CREF

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description	Mapped Register
				"EXTERNAL": external reference source	
FULL_ SWING	string	"0.5V", "0.6V", "0.7V", "0.8V", "0.9V", "1.0V", "1.1V", "1.2V"	"0.5V"	ADC full swing setting	FS0 to FS2
VCM	string	"0.8V", "0.9V", "1.0V", "1.1V", "1.2V","1.3V", "1.4V", "1.5V"	"0.8V"	ADC internal comparator input common-mode voltage setting	VCM0 to VCM2
DIVIDER	string	"2", "3", "4", "5", "6" ,"7", "8", 9" ,"10", "11" ,"12", "13", "14" , "15", "16"	"2"	Input clock division setting	DIV0 to DIV3
ADC_MODE	string	"DEFAULT", "SINGLE_PASS", "CONTINUE_SEQ", "SINGLE_CHANNEL"	"DEFAULT"	ADC Working Mode Selection "DEFAULT": default mode "SINGLE_PASS": single scan mode "CONTINUE_SEQ": continuous scan mode "SINGLE_CHANNEL": single-channel mode	SEQ0 to SEQ1
EVENT_ DRIVE	string	"FALSE", "TRUE"	"FALSE"	Sampling mode setting "FALSE": continuous sampling mode "TRUE": event-driven sampling mode	CE
ADC_MODE_ 1MSPS	string	"FALSE", "TRUE"	"FALSE"	1MSPS mode setting "FALSE": 1MSPS mode disabled "TRUE": 1MSPS mode enabled	1M
CLKSWITCH	string	"FALSE", "TRUE"	"FALSE"	Clock switching configuration "FALSE": select CLK_OSC "TRUE": select DCLK	clksw
INTERNAL_ VOL_SEL	string	"VDD33", "VDD11", "VDDM"	"VDD33"	channel 13 signal selection	MUX0 to MUX1
SINGLE_CH_ SEL	string	"0", "1", "2", "3", "4", "5", "6", "7", "8", "9", "10", "11", "12", "13", "14", "15"	"0"	Channel selection	CH0 to CH3
SINGLE_CH_ IN	string	"SINGLE_END", "UNIPOLAR", "BIPOLAR"	"SINGLE_END"	Input mode setting	DS and BU
SEQ_CH11_1 0_SEL	string	"NONE", "CH10", "CH11, "ALL"	"NONE"	Channels 11/10 scan setting "NONE": channels 11/10 not scanned	C10/C11

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description	Mapped Register
				"CH10": channel 10 scanned "CH11": channel 11 scanned "ALL": channels 11/10 scanned	
SEQ_CH9_8_SEL	string	"NONE", "CH8", "CH9, "ALL"	"NONE"	Channels 9/8 scan setting "NONE": channels 9/8 not scanned "CH8": channel 8 scanned "CH9": channel 9 scanned "ALL": channels 9/ 8 scanned	C8/C9
SEQ_CH7_6_SEL	string	"NONE", "CH6", "CH7, "ALL"	"NONE"	Channels 7/ 6 scan setting "NONE": channels 7/ 6 not scanned "CH6": channel 6 scanned "CH7": channel 7 scanned "ALL": channels 7/ 6 scanned	C6/C7
SEQ_CH5_4_SEL	string	"NONE", "CH4", "CH5, "ALL"	"NONE"	Channels 5/ 4 scan setting "NONE": channels 5/ 4 not scanned "CH4": channel 4 scanned "CH5": channel 5 scanned "ALL": channels 5/ 4 scanned	C4/C5
SEQ_CH3_2_SEL	string	"NONE", "CH2", "CH3, "ALL"	"NONE"	Channels 3/ 2 scan setting "NONE": channels 3/ 2 not scanned "CH2": channel 2 scanned "CH3": channel 3 scanned "ALL": channels 3/ 2 scanned	C2/C3
SEQ_CH1_0_SEL	string	"NONE", "CH0", "CH1, "ALL"	"NONE"	Channels 1/0 scan setting "NONE": channels 1/0 not scanned "CH0": channel 0 scanned "CH1": channel 1 scanned "ALL": channels 1/0 scanned	C0/C1
SEQ_CH11_10_IN	string	"SINGLE_END", "UNIPOLAR", "BIPOLAR"	"SINGLE_END"	Channels 11/10 input mode setting	BU5/DS5
SEQ_CH9_8_IN	string	"SINGLE_END", "UNIPOLAR", "BIPOLAR"	"SINGLE_END"	Channel 9/8 input mode setting	BU4/DS4
SEQ_CH7_6_IN	string	"SINGLE_END", "UNIPOLAR", "BIPOLAR"	"SINGLE_END"	Channels 7/ 6 input mode setting	BU3/DS3
SEQ_CH5_4_IN	string	"SINGLE_END", "UNIPOLAR", "BIPOLAR"	"SINGLE_END"	Channels 5/ 4 input mode setting	BU2/DS2
SEQ_CH3_2_IN	string	"SINGLE_END", "UNIPOLAR", "BIPOLAR"	"SINGLE_END"	Channels 3/ 2 input mode setting	BU1/DS1
SEQ_CH1_0_IN	string	"SINGLE_END",	"SINGLE_END"	Channels 1/0 input mode setting	BU0/DS0

Parameter Name	Parameter Type	Valid Values	Defaults	Function Description	Mapped Register
		"UNIPOLAR", "BIPOLAR"			
TEMP_SENSOR_HIGH	integer	0~255	0	Temperature sense upper threshold	H7:H0
TEMP_SENSOR_LOW	integer	0~255	0	Temperature sense lower threshold	L7:L0
ADC_EN_ENABLE	string	"FALSE", "TRUE"	"FALSE"	ADC_EN port enable setting "FALSE": ADC_EN port input invalid "TRUE": ADC_EN port input valid	

Parameter Design Rules:

1. The parameters INTERNAL_VOL_SEL, SINGLE_CH_SEL, and SINGLE_CH_IN are effective when the parameter ADC_MODE is set to "SINGLE_CHANNEL" or the parameter ADC_MODE_1MSPS is set to "TRUE", work together to select the corresponding channel and mode.
2. When the parameter ADC_MODE is set to "SINGLE_PASS" or "CONTINUE_SEQ", the parameters SEQ_CH11_10_SEL and SEQ_CH11_10_IN work together, as do the parameters SEQ_CH9_8_SEL and SEQ_CH9_8_SEL, and so on.
3. When the parameter ADC_MODE_1MSPS is set to "TRUE", the parameters INTERNAL_VOL_SEL, SINGLE_CH_SEL, and SINGLE_CH_IN work together to select the corresponding channel and mode.
4. After reconfiguring the control register, if wish to use the initial configuration again, need to reset with LOADSC_N (low level for at least one AD_CLK cycle), and concurrently reset the ADC with RST_N.
5. When the ADC operates in default mode, users are not allowed to turn off the oscillator (OSC), otherwise the temperature detection function will not operate properly.

2.8.4 ADC DRP Read/Write Timing

The dynamic reconfiguration port is an interface between the ADC and user logic, used for users to read and write the ADC's control and status registers. The read/write timing diagram is as follows:

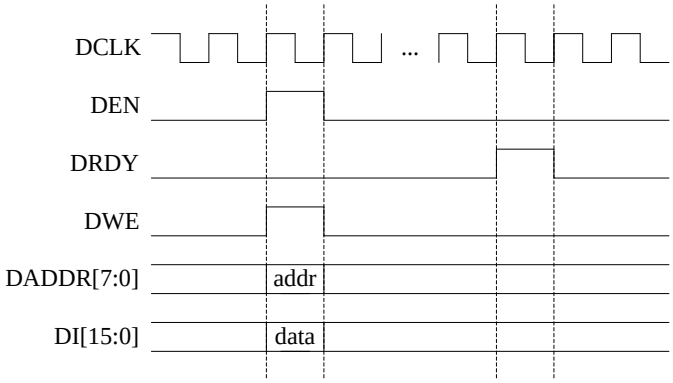

Figure2-17 Timing Diagram of DRP Write Register

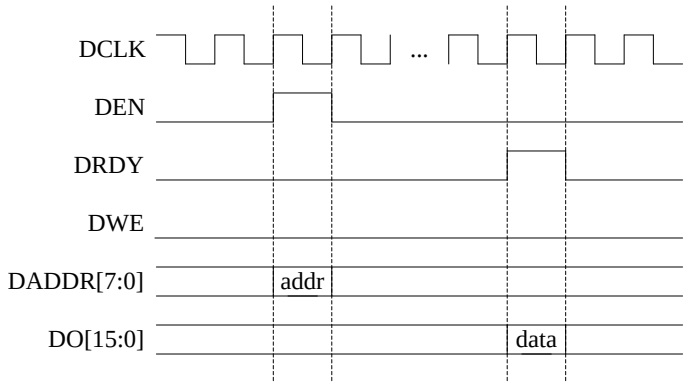

Figure2-18 Timing Diagram of DRP Read Register

DRP read and write operations also include burst mode, with the earliest next operation starting simultaneously upon completion of the previous one, as shown in the timing diagram below:

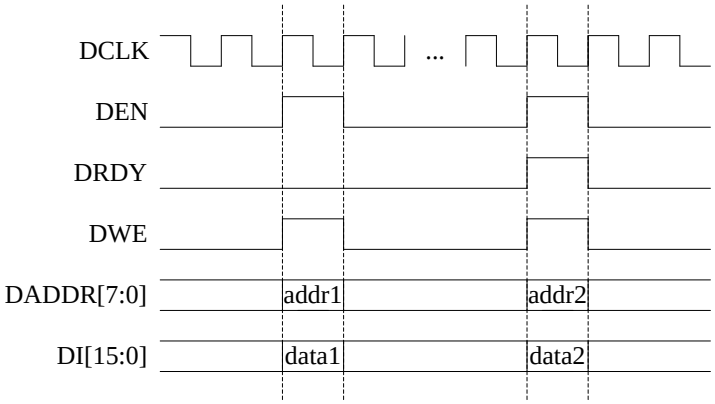

Figure2-19 Timing Diagram of DRP Burst Operation Continuous Write

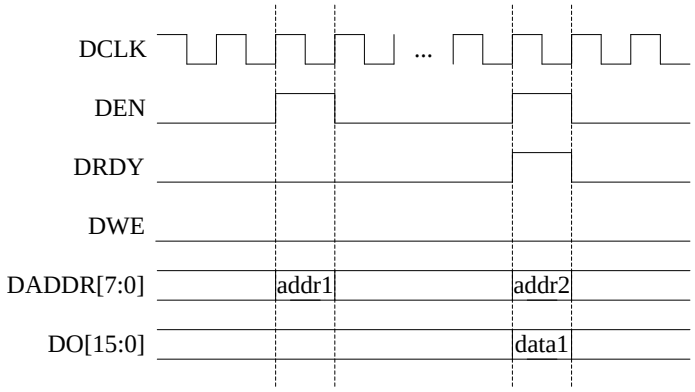

Figure2-20 Timing Diagram of DRP Burst Operation Continuous Read

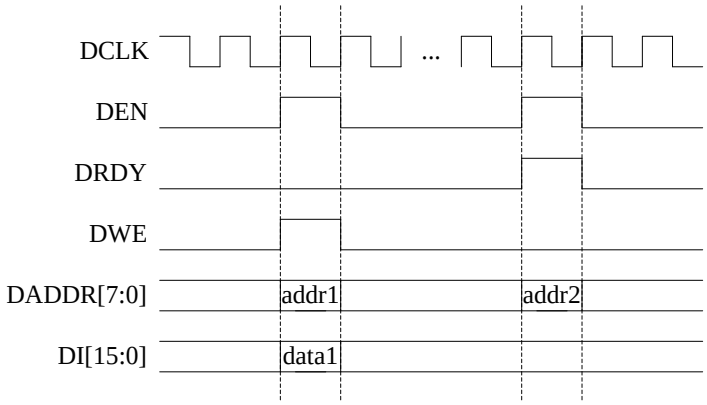

Figure2-21 Timing Diagram of DRP Burst Operation Write-Then-Read

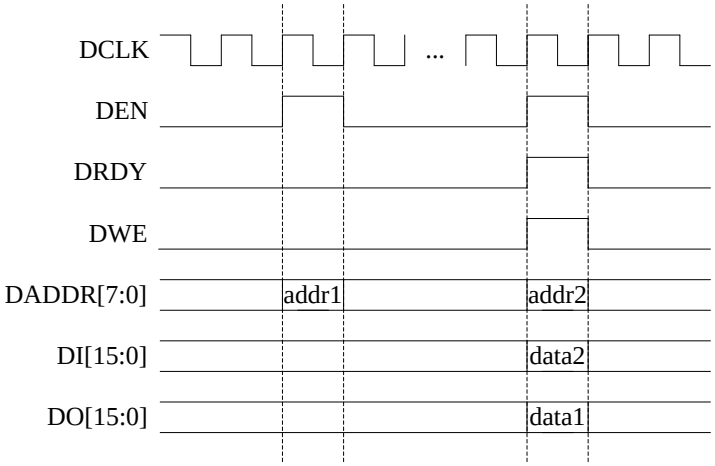

Figure2-22 Timing Diagram of DRP Burst Operation Read-Then-Write

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