Logos2 Family FPGAs High-Speed Serial Transceiver (HSSTLP) Common Functions Application Guide

(AN04004, V1.3)

(12.05.2021)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.3	12.05.2021	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
HSSTLP	High Speed Serial Transceiver Low Performance

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Chapter 1 Documentation

The Logos2 Family products have built-in high-speed serial interface modules with data rates ranging from 0.6 to 6.6 Gbps, namely HSSTLP. This document primarily introduces the basic operations of commonly used HSSTLP functions based on HSSTLP IP, including loopback, PRBS, TX de-emphasis, and output swing.

Chapter 2 Application Environment

Software version: Pango Design Suite 2020.1 and later versions

IP version: Logos2 HSSTLP v1.3 and above versions

Chapter 3 Application Description

3.1 Register Configuration Interface

The HSSTLP IP has 4 LANEs and 2 PLLs internally, each LANE and PLL has a separate set of configuration registers and address space. To facilitate user access, the IP has added an APB Bridge module, so users can access all LANEs and PLLs through a single APB bus interface.

The address bus width of LANE or PLL is 12 bits. The APB Bridge adds a 4-bit address as the Chip Select signal, so the address bus width is 16 bits. The mapping relationship is shown in Table 1.

Table 3-1 APB Address Mapping

Address Range	Register
0x0000~0x03FF	LANE0 PCS
0x0400~0x07FF	LANE0 PMA RX
0x0800~0x0BFF	LANE0 PMA TX
0x0C00~0x0FFF	Received
0x1000~0x13FF	LANE1 PCS
0x1400~0x17FF	LANE1 PMA RX
0x1800~0x1BFF	LANE1 PMA TX
0x1C00~0x1FFF	Received

Address Range	Register
0x2000~0x23FF	LANE2 PCS
0x2400~0x27FF	LANE2 PMA RX
0x2800~0x2BFF	LANE2 PMA TX
0x2C00~0x2FFF	Received
0x3000~0x33FF	LANE3 PCS
0x3400~0x37FF	LANE3 PMA RX
0x3800~0x3BFF	LANE3 PMA TX
0x3C00~0x3FFF	Received
0x4000~0x4FFF	PLL0
0x5000~0x5FFF	PLL1

For details about the offset address of each register, please refer to "UG040008_Logos2 Family FPGAs High-Speed Serial Transceiver (HSSTLP) User Guide"

In the IPC interface, users need to enable the APB interface, as shown in Figure 1.

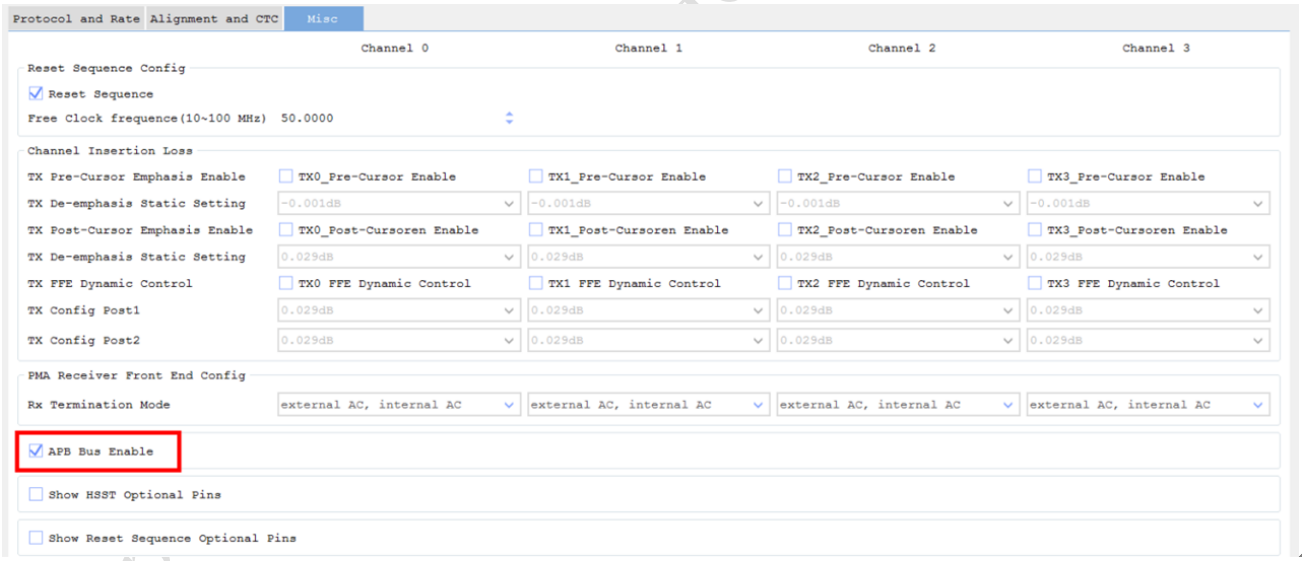

Figure 3-1 Enabling the APB Interface in the IPC Interface

3.2 Loopback Function

HSSTLP supports multiple loopback modes for testing, including PCS near-end loopback, PMA near-end parallel loopback, PMA near-end serial loopback, PMA far-end parallel loopback, and PCS far-end loopback.

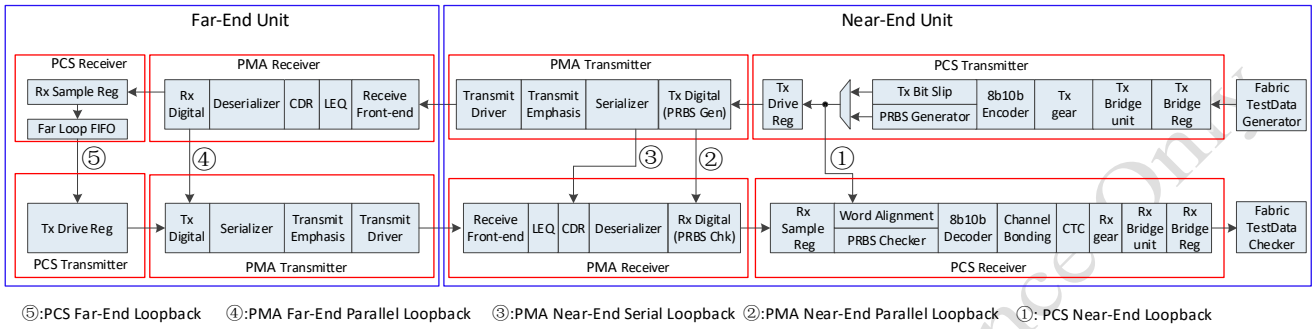

Figure 3-2 HSSTLP Loopback Mode Data Path Overview

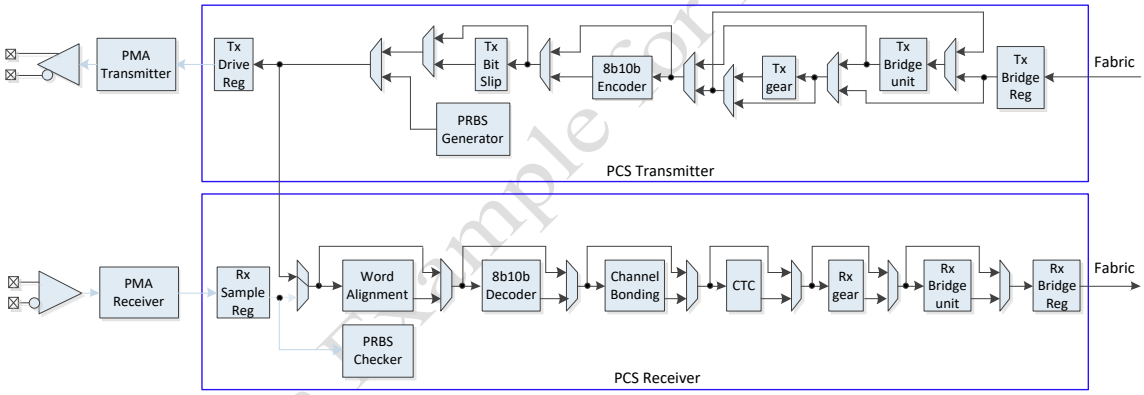

Figure 3-3 PCS Near-End Loopback Data Path Diagram

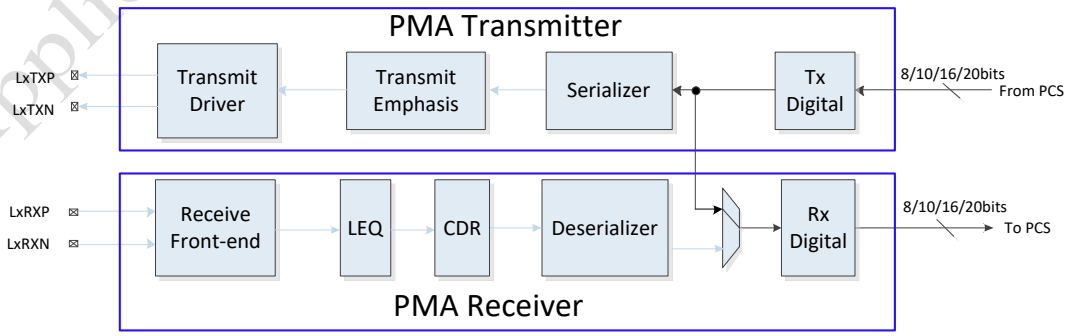

Figure 3-4 PMA Near-End Parallel Loopback Data Path Diagram

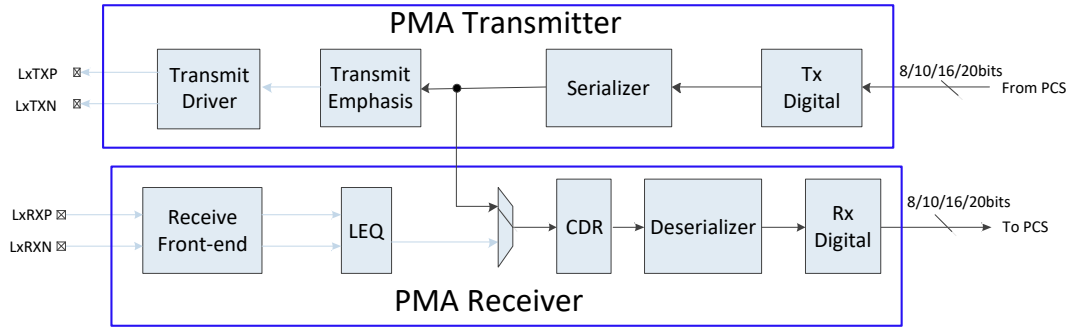

Figure 3-5 PMA Near-End Serial Loopback Data Path Diagram

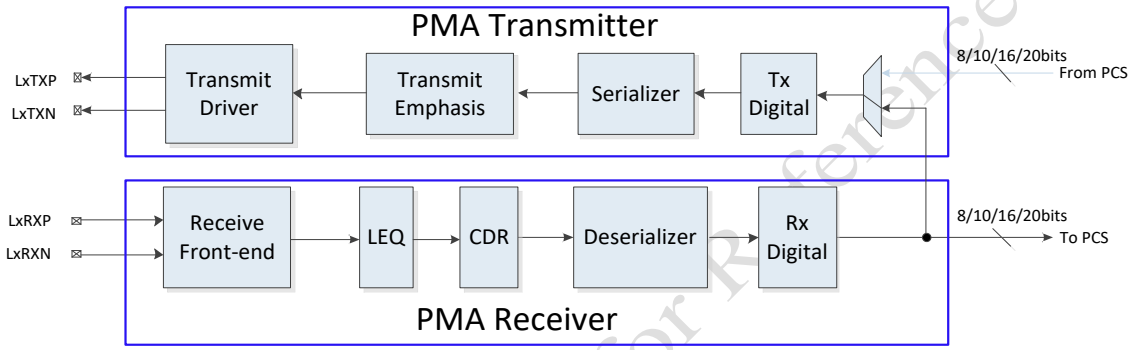

Figure 3-6 PMA Far-End Parallel Loopback Data Path Diagram

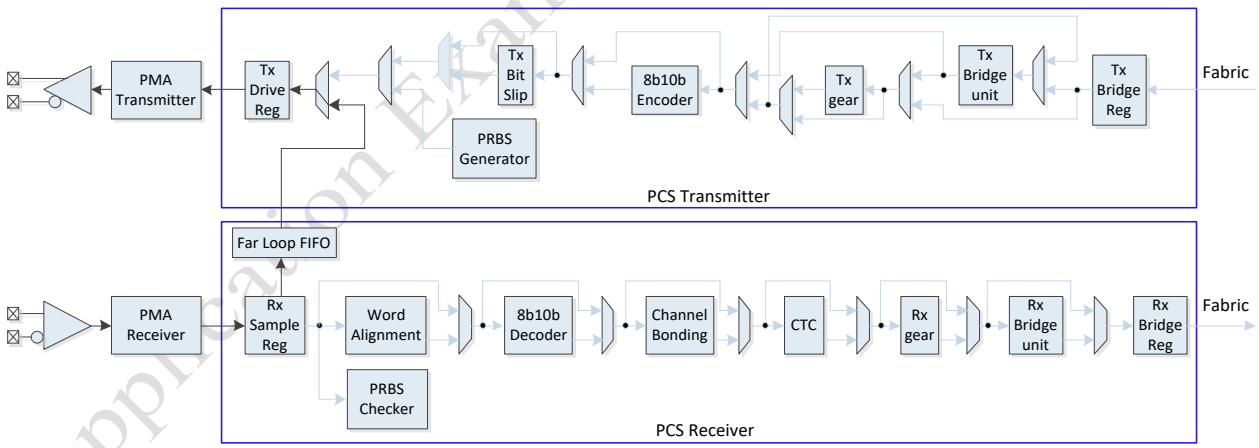

Figure 3-7 PCS Far-End Loopback Data Path Diagram

Users can configure the loopback mode via the registers or ports. These two methods are described below respectively.

Method 1: Via the Registers

On the third page of the IPC interface, check [Show Reset Sequence Optional Pins]. Then in the expanded reset options, check the [RX Debug Bus] for four channels as shown in Figure 8 below.

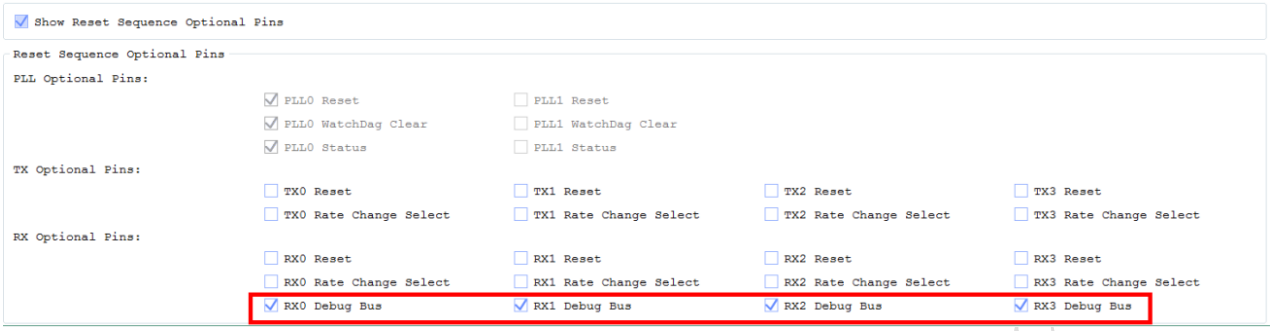

Figure 3-8 IPC Ports Required for Loopback via the Registers

Table 3-2 Loopback Mode Setting Via the Registers

Loopback Mode	**i_loop_dbg_x[2:0]**	**Register Settings**
PCS Near-End Loopback	3’b011	PCS_NEAR_LOOP=”TRUE” Corresponding to bit[1]=1 of PCS register 0x024
PMA Near-End Parallel Loopback	3’b011	PMA_REG_RX_TX2RX_PLPBK_EN=”TRUE” Corresponding to bit[6]=1 of PMA RX register 0x40C
PMA Near-End Serial Loopback	3’b000	PMA_REG_TX_TX2RX_SLPBACK_EN=”TRUE” Corresponding to bit[4]=1 of PMA TX register 0x818
PMA Far-End Parallel Loopback	3’b000	(1)PMA_REG_TX_DATA_MUX_SEL=3 Corresponding to bit[2:1]=2'b11 of PMA TX register 0x81D (2) PMA_REG_TX_FIFO_EN=”TRUE” Corresponding to bit[0] = 1 of PMA TX register 0x81D (3) PMA_REG_PLPBK_TXPCLK_EN=”TRUE” Corresponding to bit[2]=1 of PMA TX register 0x824
PCS Far-End Loopback	3’b000	(1)PCS_FAR_LOOP=”TRUE” Corresponding to bit[0]=1 of PCS register 0x024 (2) PMA_REG_PLPBK_TXPCLK_EN=”TRUE” Corresponding to bit[2]=1 of PMA TX register 0x824 (3) PCS_CB_RCLK_SEL =” PMA_TCLK” Corresponding to bit[4:3]=2'b01 of PCS register 0x00c
Note: During loopback testing, ensure the value of HSSTLP GTP port P_TDATA[45:44] is 2'b00, meaning that the TX LANE cannot be in electrical_idle state.		

When receiving or transmitting data in normal work mode, set the i_loop_dbg_x[2:0] and the value of corresponding loopback mode register to 0, and then reset the LANE.

Example:

Set LANE1 to PMA near-end serial loopback via the registers.

Steps

Step 1: First read the value of register 0x1818 (the bit[15:12]=1 of the corresponding address for LANE1)

Assume the default value read from 0x1818 is 0x80.

Step 2: According to the setting mode requirements, configure the value of the corresponding bits of register 0x1818 and the port i_loop_dbg_1.

This is the PMA near-end serial loopback, so

write the value 0x90 to register 0x1818 // Change bit[4] of 0x1818 from 0 to 1 to enable PMA near-end serial loopback

Port signal i_loop_dbg_1 =3'b000 // For PMA near-end serial loopback, this port value is 3'b000

Method 2: Via the ports

On the third page of the IPC interface, check [Show HSST Optional Pins] and in the expanded optional interfaces, check [Debug Bus]. Also check [Show Reset Sequence Optional Pins] and in the expanded reset options, check the [RX Debug Bus] for four channels as shown in Figure 9 below.

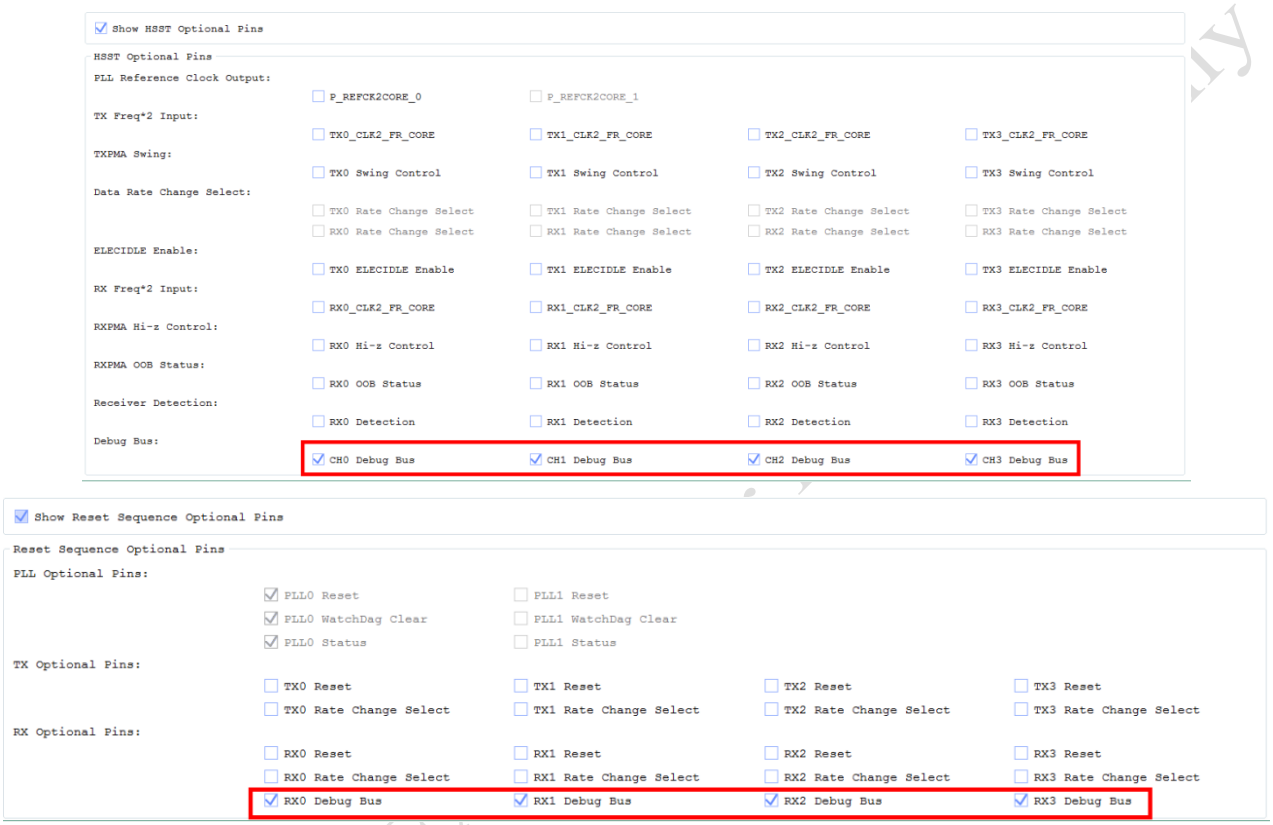

Figure 3-9 IPC Ports Required for Loopback Via the Ports

Table 3-3 Loopback Mode Setting Via the Ports

Loopback Mode	**i_loop_dbg_x[2:0]**	**Loopback Mode Port Enable Signal**
PCS Near-End Loopback	3’b011	i_p_pcs_nearend_loop_x=1’b1
PMA Near-End Parallel Loopback	3’b011	i_p_pma_nearend_ploop_x=1’b1
PMA Near-End Serial Loopback	3’b000	i_p_pma_nearend_sloop_x=1’b1
PMA Far-End Parallel Loopback	3’b000	i_p_pma_ farend_ploop_x=1'b0 (not via the ports)
PCS Far-End Loopback	3’b000	i_p_pcs_farend_loop_x=1'b1, and PCS_CB_RCLK_SEL =” PMA_TCLK” Corresponding to bit[4:3]=2'b01 of PCS register 0x00c
Note: During loopback testing, ensure the value of HSSTLP GTP port P_TDATA[45:44] is 2'b00, meaning that the TX LANE cannot be in electrical_idle state.		

When receiving or transmitting data in normal mode, set the i_loop_dbg_x[2:0] and the corresponding loopback mode port enables to 0, and then reset the LANE.

Example:

Set LANE1 to PMA near-end serial loopback via the ports.

Steps

Step 1: According to the setting mode requirements, configure i_p_pma_nearend_sloop_1 and the port i_loop_dbg_1.

This is the PMA near-end serial loopback, so

Port signal i_p_pma_nearend_sloop_1=1’b1 // Enable PMA near-end serial loopback.

Port signal i_loop_dbg_1 =3'b000 // For PMA near-end serial loopback, this port value is 3'b000

The loopback test via the ports or the registers is considered alternative options, meaning that either method can be used as long as it is valid.

In the near-end loopback mode, the TX data is also transmitted to the TX output port of the PMA.

In the far-end loopback mode, RX data is also transmitted to the RX user interface of the Fabric.

In the PCS near-end loopback mode, the RX data path goes through the Word align module block, bypassing the PRBS Check of PCS.

3.3 PMA PRBS Function

In the PMA digital section, there is also a PRBS Generator & Checker module supporting the data widths of 8BIT, 10BIT, 16BIT, and 20BIT, and four data patterns of PRBS7, PRBS15, PRBS23, and PRBS31.

Table 3-4 PMA PRBS Test Register Description

Register Address	Corresponding Parameter Name	Description
0x40d Bit[5]	PMA_REG_PRBS_CHK_EN	PMA RX PRBS check enable, with a default of 0 1'b0: corresponds to parameter value "FALSE": disabled **1'b1: corresponds to parameter value "TRUE": enabled**
0x40d Bit[4:3]	PMA_REG_PRBS_SEL	PMA RX PRBS mode selection, with a default of 2'b00 2'b00: PRBS7, corresponds to the parameter value "PRBS7" 2'b01: PRBS15, corresponds to the parameter value "PRBS15" 2'b10: PRBS23, corresponds to the parameter value "PRBS23" **2'b11: PRBS31, corresponds to the parameter value "PRBS31"**
0x40e Bit[2]	PMA_REG_CHK_COUNTER_EN	PRBS pattern error detection count enable/clear control, with a default of 0 1'b0: corresponds to parameter value "FALSE": disable, counter value clear **1'b1: corresponds to parameter value "TRUE": enable, counter count errors**
0x40e Bit[1]	PMA_REG_LOAD_ERR_CNT	PRBS pattern error detection counter hold control signal, with a default of 0 **1'b0: corresponds to Parameter value "FALSE", the counter always updates the cumulative error value detected by the current link** 1'b1: Corresponds to the parameter value "TRUE", the counter value holds and does not update even if the link has an error
0x436 Bit[7:0]	REG_RX_ERR_COUNTER	Checking error counter in PMA PRBS checker REG_RX_ERR_COUNTER[7:0]
0x437 Bit[7:0]		Checking error counter in PMA PRBS checker REG_RX_ERR_COUNTER[15:8]
0x438 Bit[7:0]		Checking error counter in PMA PRBS checker REG_RX_ERR_COUNTER[23:16]
0x439 Bit[7:0]		Checking error counter in PMA PRBS checker REG_RX_ERR_COUNTER[31:24], the counter resets to 0 after reaching the maximum value and then accumulates again.
0x819 Bit[4:3]	PMA_REG_TX_PRBS_SEL	PMA TX PRBS mode selection, with a default of 2'b00 2'b00: PRBS7 2'b01: PRBS15 2'b10: PRBS23 **2'b11: PRBS31**
0x819 Bit[0]	PMA_REG_TX_PRBS_GEN_EN	PMA TX PRBS generator enable, with a default of 0 1'b0: corresponds to parameter value "FALSE", disable **1'b1: corresponds to parameter value "TRUE":enable**
0x81d Bit[3]	PMA_REG_TX_ERR_INSERT	PRBS error code injection, with a default of 0 Triggered by the rising edge from 0 to 1, one error code is injected into the PRBS data. During regular transmission of PRBS test data, the value remains 0 **1'b0: Corresponds to the parameter value "FALSE"** 1'b1: Corresponds to the parameter value "TRUE"
0x81d	PMA_REG_TX_DATA_MUX_	Data selection control signal, with a default value of 2'b00

Register Address	Corresponding Parameter Name	Description
Bit[2:1]	SEL	2'b00: data from pcs **2'b01: prbs data** 2'b10: udp data 2'b11: rx loopback data
0x81d Bit[0]	PMA_REG_TX_FIFO_EN	Register configuration TX_fifo_en enable, with a default of 0 1'b0: Corresponds to parameter value "FALSE", disable **1'b1: Corresponds to parameter value "TRUE", enable** When TX PMA PRBS function or PMA far-end parallel loopback is used, set this value to 1. The default value under normal conditions is 0.

Register REG_RX_ERR_COUNTER is read-only, while other registers are readable/writable.

Example:

Set the PRBS Generator and PRBS Checker of PMA LANE0 to PRBS31 mode.

Steps

Step 1: First read the values of registers 0x040d, 0x040e, 0x0819, and 0x081d, assuming

the default value of register 0x040d is 0xC0,

the default value of register 0x040e is 0x38,

the default value of register 0x0819 is 0x06,

and the default value of register 0x081d is 0x00.

Step 2: Set the values of the corresponding bits in the registers 0x040d, 0x040e, 0x0819, and 0x081d as required by the setup mode.

Here is PRBS31 mode, then

write value 0xF8 to register 0x040d //Enable PRBS Checker, PRBS31 mode

write value 0x3C to register 0x040e //Prbs check count check errors

write value 0x1F to register 0x0819 //Enable PRBS Generator PRBS31

write value 0x03 to register 0x081d //When selecting the TX PMA PRBS function, set the value 0x03

Step 3: Read registers 0x0436, 0x0437, 0x0438, and 0x0439, and read the check results

If the check result read is a non-zero value, users can reset the check result to 0 by writing 0x38 to register 0x040e, and then write 0x3c to register 0x040e to recount errors.

For example, users can repeat the following command operations:

write 0x1F to register 0x0819 –>

write 0x03 to register 0x081d –>

write 0xF8 to register 0x040d –>

write 0x38 to register 0x040e –>

write 0x3C to register 0x040e –>

Read registers 0x0436, 0x0437, 0x0438, and 0x0439

3.4 PCS PRBS Function

The PCS PRBS Generator & Checker module can operate in 8bit, 10bit, 16bit, and 20bit only modes and generate multiple feature code streams (refer to "UG040008_Logos2 Family FPGAs High-Speed Serial Transceiver (HSSTLP) User Guide" for details). Users can dynamically insert error codes into the test code and perform error count.

Table 3-5 PCS PRBS Test Register Description

Register address	**Corresponding Parameter Name**	**Description**
0x01c Bit[5]	PCS_PRBS_ERR_LPBK	PRBS_ERR_LPBK enable, with a default of 0 **1'b0: Corresponds to parameter value "FALSE"**; 1'b1: Corresponds to the parameter value "TRUE";
0x01c Bit[4]	PCS_RX_ERRCNT_CLR	PCS_ERR_CNT counter clear, high level clear, with a default of 0 **1'b0: Corresponds to parameter value "FALSE";** 1'b1: Corresponds to parameter value "TRUE", counter clear
0x01c Bit[3:0]	PCS_RX_PRBS_MODE	PRBS Checker mode selection at the receive side, with a default of 0 4'd0: Corresponds to parameter value "DISABLE"; 4'd1: Corresponds to the parameter value "PRBS_7"; 4'd2: Corresponds to the parameter value "PRBS_15"; 4'd3: Corresponds to the parameter value "PRBS_23"; **4'd4: Corresponds to the parameter value "PRBS_31";**
0x01d Bit[5]	PCS_ENABLE_PRBS_GEN	PCS PRBS Generator enable, high level enable, with a default of 0 1'b0: Corresponds to parameter value "FALSE", Disable PRBS **1'b1: Corresponds to parameter value "TRUE", Enable PRBS**
0x01d	PCS_TX_INSERT_ER	PRBS error code injection, with a default of 0

Register address	Corresponding Parameter Name	Description
Bit[4]		Triggered by the rising edge from 0 to 1, one error code is injected into the PRBS data. During regular transmission of PRBS test data, the value remains 0 **1'b0: Corresponds to parameter value "FALSE";** 1'b1: Corresponds to the parameter value "TRUE";
0x01d Bit[3:0]	PCS_TX_PRBS_MODE	PCS PRBS Generator mode selection at the transmit side, with a default of 0 4'd0: Corresponds to parameter value "DISABLE" ; 4'd1: Corresponds to the parameter value "PRBS_7"; 4'd2: Corresponds to the parameter value "PRBS_15"; 4'd3: Corresponds to the parameter value "PRBS_23"; **4'd4: Corresponds to the parameter value "PRBS_31";** 4'd5: Corresponds to the parameter value "LONG_1"; 4'd6: Corresponds to the parameter value "LONG_0"; 4'd7: Corresponds to the parameter value "20UI"; 4'd8: Corresponds to the parameter value "D10_2"; 4'd9: Corresponds to the parameter value "PCIE";
0x01e Bit[7:0]	PCS_ERR_CNT	Checking error counter in PCS PRBS checker, which remains at 0xFF after reaching its maximum value 0xFF and will not increment with further link errors until the counter is cleared
0x822 Bit[0]	PMA_REG_TX_POLARITY	PMA TX polarity inversion, with a default of 0 1'b0: Corresponds to the parameter value "NORMAL" txpdata_out[19:0] = txpdata_in[19:0] 1'b1: Corresponds to the parameter value "REVERSE" txpdata_out[19:0] = ~txpdata_in[19:0] The polarity of the PRBS data difference between PCS and PMA is inverted. Therefore, when docking the PRBS of PMA and PCS, the PRBS data output from the PCS Generator needs to be polarity inverted at the PMA TX.
0x40d Bit[0]	PMA_REG_RX_DATA_POLARITY	PMA RX polarity inversion control signal, with a default of 0 1'b0: Corresponds to parameter value "NORMAL" 1'b1: Corresponds to parameter value "REVERSE", data inversion by bit The polarity of the PRBS data difference between PCS and PMA is inverted. Therefore, when docking the PRBS of PMA and PCS, the PCS Checker needs to be polarity inverted at the PMA RX.

Register PCS_ERR_CNT is read-only, while other registers are readable/writable.

Example:

Set the PRBS Generator and PRBS Checker of PCS LANE0 to PRBS31 mode.

Steps

Step 1: First, read the values of registers 0x001c and 0x001d,

assuming the default values read are 0x00 for register 0x001c and 0x00 for register 0x001d.

Step 2: Set the corresponding bit values of registers 0x001C and 0x001D according to the requirements of the set mode.

Here is PRBS31 mode, then

Write the value 0x24 to register 0x001d //Enable PRBS Generator, PRBS31 mode, no error code injection

Write the value 0x04 to register 0x001c //Enable PRBS Checker PRBS31 mode to count check errors

Step 3: Read register 0x001E to read the check result

If the check result read is a non-zero value, users can clear the check result by writing 0x14 to register 0x001c, then write 0x04 to register 0x001c to recount errors. i.e., users can repeat some command operations:

Write 0x24 to register 0x001d –>

Write 0x14 to register 0x001c –>

Write 0x04 to register 0x001c –>

Read register 0x001e

3.5 Dynamic Rate Switching

Dynamic rate switching can be performed via the registers or the ports.

Dynamic rate switching via the registers can be achieved by changing the values of the division ratio parameters N1, N2, M of the PLL and the value of the division ratio parameter D of the TX/RX LANE. It is ideal for scenarios where the reference clock and PLL frequency change.

Dynamic rate switching via the ports can only be achieved by changing the division ratio parameter D value of the TX/RX LANE. It is ideal for fast switching scenarios where the reference clock and PLL frequency do not change, but only the LANE rate changes, such as PCIe rate switching.

The TX and RX of the four LANEs in each HSSTLP share PLL0 and PLL1, and the TX or RX of each channel can independently select the clock source. The primary function of the PLL is

frequency synthesis, with the input clock and feedback clock passing through the Phase Frequency Detector (PFD), Charge Pump, and Loop Filter in sequence. The VCO frequency is locked between 1.6GHz and 6.6GHz. The PLL output frequency is determined by the input clock CLKIN frequency, input division factor M, and feedback division factors N1 and N2, with the calculation method as follows:

CLKOUT frequency = CLKIN frequency * N1 * N2 / M

The relationship between PMA line rate and PLL output is calculated as follows:

PMA line rate = CLKOUT frequency * 2 / D

Where D represents the division ratio on the TX or RX clock path.

Table 3-6 Supported Range for PLL Division Factors

Division Factor	**Supported Values**	**Register Definition**
M	1,2	Refer to the bit[4:0] definition of pma_pll_reg2
N1	4,5	Refer to the bit[5] definition of pma_pll_reg3
N2	1,2,3,4,5,6,8,10	Refer to the bit[4:0] definition of pma_pll_reg3
D	1,2,4,8	Tx: Refer to the definition of bits [3] and [1:0] of pma_rx_reg12
		Rx: Refer to the definition of bits [7] and [5:4] of pma_rx_reg4

Method 1: Via the Registers

The registers for the division factors M, N1, N2, and D are as shown in the table below.

For the allocation of PLL and LANE address ports, please refer to "Table 1 APB Address Mapping".

pma_pll_reg2 corresponds to the PLL register offset address 0x002;

pma_pll_reg3 corresponds to the PLL register offset address 0x003;

pma_rx_reg4 corresponds to the LANE register offset address 0x404;

pma_rx_reg12 corresponds to the LANE register offset address 0x40c.

Table 3-7 Description of PLL Configuration Registers Related to Dynamic Rate Switching

<table>
<tr><th>Register Address</th><th>Corresponding Parameter Name</th><th>Description</th></tr>
<tr><td>0x002
Bit[4:0]</td><td>PMA_PLL_REG_PLL_REFDIV</td><td>PLL reference clock divider M, related to IP configuration
5'b10000: Division Ratio 1 (default)
5'b00000: Division Ratio 2</td></tr>
<tr><td>0x003
Bit[5:0]</td><td>PMA_PLL_REG_PLL_FBDIV</td><td>Bit[5]:Pll feedback divider N1;
Bit[4:0],Pll feedback divider N2;
Related to IP configuration
<table>
<tr><th>Setting</th><th>N1</th><th>N2</th><th>Division Ratio</th></tr>
<tr><td>6’b010000</td><td>4</td><td>1</td><td>4</td></tr>
<tr><td>6’b000000</td><td>4</td><td>2</td><td>8</td></tr>
<tr><td>6’b000001</td><td>4</td><td>3</td><td>12</td></tr>
<tr><td>6’b000010</td><td>4</td><td>4</td><td>16</td></tr>
<tr><td>6’b000011</td><td>4</td><td>5</td><td>20</td></tr>
<tr><td>6’b000101</td><td>4</td><td>6</td><td>24</td></tr>
<tr><td>6’b000110</td><td>4</td><td>8</td><td>32</td></tr>
<tr><td>6’b000111</td><td>4</td><td>10</td><td>40</td></tr>
<tr><td>6’b110000</td><td>5</td><td>1</td><td>5</td></tr>
<tr><td>6’b100000</td><td>5</td><td>2</td><td>10</td></tr>
<tr><td>6’b100001</td><td>5</td><td>3</td><td>15</td></tr>
<tr><td>6’b100010</td><td>5</td><td>4</td><td>20</td></tr>
<tr><td>6’b100011</td><td>5</td><td>5</td><td>25</td></tr>
<tr><td>6’b100101</td><td>5</td><td>6</td><td>30</td></tr>
<tr><td>6’b100110</td><td>5</td><td>8</td><td>40</td></tr>
<tr><td>6’b100111</td><td>5</td><td>10</td><td>50</td></tr>
</table>
</td></tr>
</table>

Table 3-8 Description of LANE Configuration Registers Related to Dynamic Rate Switching

Register Address	Corresponding Parameter Name	Description
0x404 Bit[7]	PMA_REG_RX_RATE_EN	RX line rate division ratio control selection, 1'b0: Corresponds to the parameter value "FALSE" (default) Controlled by the port P_RX_RATE 1'b1: Corresponds to the parameter value "TRUE" Controlled by the register PMA_REG_RX_RATE
0x404 Bit[5:4]	PMA_REG_RX_RATE	RX line rate division ratio D control register 2’b00: The line rate is 1/4 of the PLL clock frequency; Corresponds to the parameter value "DIV4"; Corresponds to the division ratio of 8 2'b01: The line rate is 1/2 of the PLL clock frequency; Corresponds to the parameter value "DIV2"; Corresponds to the division ratio of 4 2'b10: Line rate and PLL clock frequency are equal (default); Corresponds to the parameter value "DIV1"; Corresponds to the division ratio of 2 2'b11: The line rate is 2 times the PLL clock frequency; Corresponds to the parameter value "MUL2"; Corresponds to the division ratio of 1

Register Address	Corresponding Parameter Name	Description
0x40c Bit[3]	PMA_REG_TX_RATE_EN	TX line rate division ratio control selection 1'b0: Corresponds to the parameter value "FALSE" (default) Controlled by the port P_TX_RATE 1'b1: Corresponds to the parameter value "TRUE", controlled by the register PMA_REG_TX_RATE
0x40c Bit[1:0]	PMA_REG_TX_RATE	TX line rate division ratio D control register 2'b00: The line rate is 1/4 of the PLL clock frequency; Corresponds to the parameter value "DIV4"; Corresponds to the division ratio of 8 2'b01: The line rate is 1/2 of the PLL clock frequency; Corresponds to the parameter value "DIV2"; Corresponds to the division ratio of 4 2'b10: The line rate is equal to the PLL clock frequency; Corresponds to the parameter value "DIV1" (default); Corresponds to the division ratio of 2 2'b11: The line rate is 2 times the PLL clock frequency; Corresponds to the parameter value "MUL2"; Corresponds to the division ratio of 1

Example:

Set the line rate of LANE0 via the registers; set the reference clock to 100MHz, and the TX and RX line rates to 5Gbps.

Step 1: Based on the relationship between the reference clock and the line rate, use the two formulas mentioned above to determine that M=1, N1*N2=50, i.e., N1=5, N2=10, and D=2. Also note that the VCO frequency should be within the range of 1.6GHz to 6.6GHz.

Step 2: Read the value of register 0x0002 and overwrite bit[4:0] to 5'b10000, then write the data, i.e., set M to 1;

Read the value of register 0x0003 and modify bit[5:0] to 6'b100111, then write the data, i.e., set N1 to 5 and N2 to 10;

Read the value of register 0x0404 and modify bit[7] to 1'b1, i.e., change the RX line rate division ratio control selection to be register-controlled and [5:4] to 2'b10, then write the data, i.e., change the D value to 2;

Read the value of register 0x040c and change bit[3] to 1'b1, i.e., change the TX line rate division ratio control selection to be register-controlled and [1:0] to 2'b10, then write the data, i.e., change the D value to 2.

Step 3: After completing parameter configuration, use the control port i_pll_rst_0 to perform a reset operation on HSSTLP (Do not control the APB interface reset, otherwise the configuration register will restore to default values).

Method 2: Via the Ports

Dynamic rate switching done via the ports already synchronizes the timing of RX/TX rate switching in the IP reset sequence. Users only need to set the TX/RX line rate division ratio ports and trigger enable signal.

The IP generates the N1, N2, and M values, as well as the initial values for i_txckdiv/i_rxckdiv, based on the set reference clock and line rate.

The PMA line rate is determined by the PLL output frequency and i_txckdiv/i_rxckdiv. Their correspondences are described in the following table.

Table 3-9 Dynamic Rate Switching Control Ports

Port	Input/Output	Description
i_tx_rate_chng_x	Input	TX dynamic rate switching is enabled, valid on the rising edge active, in the i_free_clk clock domain. With the i_txckdiv value set and stabilized, the enable is valid.
i_txckdiv_x[1:0]	Input	TX line rate control signal, i.e., P_TX_RATE[1:0] 2’b00: The line rate is 1/4 of the PLL clock frequency; 2'b01: The line rate is 1/2 of the PLL clock frequency; 2'b10: Line rate equals PLL output clock frequency; 2’b11: The line rate is 2 times the PLL clock frequency.
i_rx_rate_chng_x	Input	RX dynamic rate switching is enabled, valid on the rising edge active, in the i_free_clk clock domain. With the i_rxckdiv value set and stabilized, its enable is valid.
i_rxckdiv_x[1:0]	Input	RX line rate control signal, i.e., P_RX_RATE[1:0] 2’b00: The line rate is 1/4 of the PLL clock frequency; 2'b01: The line rate is 1/2 of the PLL clock frequency; 2'b10: The line rate is equal to the PLL clock frequency; 2'b11: The line rate is twice the PLL clock frequency.

IPC interface configuration is shown in Figure 10. After configuring the IP as above, related ports for dynamic rate switching will be added to the top-level module of the project.

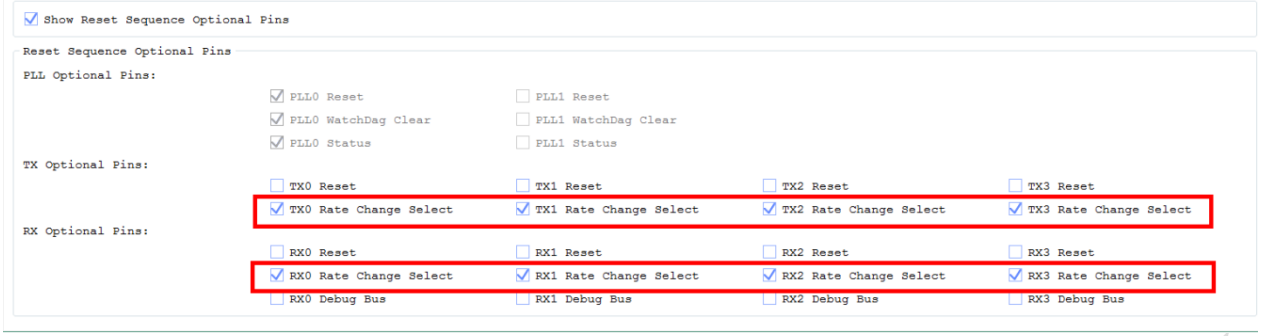

Figure 3-10 Dynamic Rate Switching IPC Interface Settings

3.6 Programmable TX Output Swing

Method 1: Via the Registers

First set HSSTLP GTP port signals P_TX_SWING_x=0 and P_TX_MARGIN_x=3'b000. The default setting values for these two port signal IPs are both 0, so they are controlled via the registers and no further modification is required.

TX output swing is achieved by controlling the PMA TX register offset address 0x811, as defined in the table below.

Table 3-10 TX Output Swing DAC0 Register Description

<table>
<tr><th>Register address</th><th>Corresponding Parameter Name</th><th>Description</th></tr>
<tr><td>0x811
Bit[7:6]</td><td></td><td>Reserved, fixed to value 0</td></tr>
<tr><td>0x811
Bit[5:0]</td><td>PMA_REG_TX_AMP_DAC0</td><td>TX output swing control DAC0 (default selection), bit[5] reserved, fixed value 0, bit[4:0] defined as follows
<table>
<tr><th>Setting</th><th>tx output swing(V)</th></tr>
<tr><td>5'b00000</td><td>0.193</td></tr>
<tr><td>5'b00001</td><td>0.229</td></tr>
<tr><td>5'b00010</td><td>0.269</td></tr>
<tr><td>5’b00011</td><td>0.305</td></tr>
<tr><td>5’b00100</td><td>0.344</td></tr>
<tr><td>5’b00101</td><td>0.383</td></tr>
<tr><td>5’b00110</td><td>0.416</td></tr>
<tr><td>5’b00111</td><td>0.453</td></tr>
<tr><td>5’b01000</td><td>0.486</td></tr>
<tr><td>5’b01001</td><td>0.519</td></tr>
<tr><td>5’b01010</td><td>0.552</td></tr>
<tr><td>5’b01011</td><td>0.582</td></tr>
<tr><td>5’b01100</td><td>0.615</td></tr>
</table></td></tr>
</table>

Register address	Corresponding Parameter Name	Description			
			5’b01101	0.646	
			5’b01110	0.679	
			5’b01111	0.706	
			5’b10000	0.736	
			5’b10001	0.760	
			5’b10010	0.787	
			5’b10011	0.815	
			5’b10100	0.839	
			5’b10101	0.860	
			5’b10110	0.884	
			5’b10111	0.905	
			5’b11000	0.923	
			5’b11001	0.941	
			5’b11010	0.959	
			5’b11011	0.974	
			5’b11100	0.987	
			5’b11101	0.996	
			5’b11110	1.008	
			5’b11111	1.011	

Method 2: Via the Ports

The output swing can also be controlled through the port-based method, and the required ports are described as follows.

Table 3-11 Output Swing Control Port Description

Port	Input/Output	Description
P_TX_SWING_x	Input	Transmitter output swing value for half-swing control 0: Full swing (default); 1: Half swing
P_TX_MARGIN_x[2:0]	Input	Transmitter output swing DAC source selection. 3’b000: Swing source register PMA_REG_TX_AMP_DAC0 (default); 3’b001: Swing source register PMA_REG_TX_AMP_DAC1; 3’b010: Swing source register PMA_REG_TX_AMP_DAC2; 3’b011: Swing source registerPMA_REG_TX_AMP_DAC3; Other values: Reserved

PMA_REG_TX_AMP_DAC0 Register Address: 0x811

PMA_REG_TX_AMP_DAC1 Register Address: 0x812

PMA_REG_TX_AMP_DAC2 Register Address: 0x813

PMA_REG_TX_AMP_DAC3 Register Address: 0x814

The register definitions are similar. Users can refer to Table 7 for the register definitions of PMA_REG_TX_AMP_DAC0.

Note: The set values of TX output swing correspond to the voltage amplitude values, subject to the updated parameter values in the "UG040008_Logos2 Family FPGAs High-Speed Serial Transceiver (HSSTLP) User Guide".

3.7 TX Pre-/Post-Cursor De-emphasis

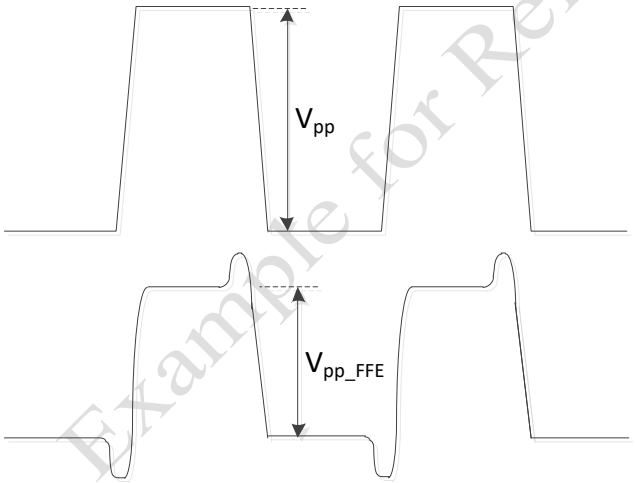

Figure 3-11 Pre-Cursor De-Emphasis Diagram

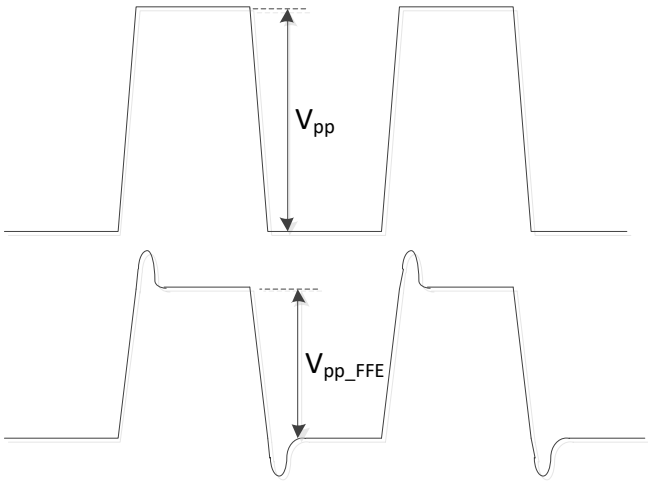

Figure 3-12 Post-Cursor De-Emphasis Diagram

Signal Attenuation Calculation: $\mathrm{deemp(dB)} = 20\log(V_{pp}/V_{pp\_FFE})$

The initial values of pre-/post-cursor de-emphasis can be dynamically set through the APB interface or set via the IPC interface (and can be dynamically set again via the APB interface). The two methods are described below respectively.

Method 1: Via the Registers (Dynamic Configuration via APB Interface)

Table 3-12 Pre-Cursor De-Emphasis Configuration Register

<table>
<tr><th>Register address</th><th>Corresponding Parameter Name</th><th>Description</th></tr>
<tr><td>0x829
Bit[1]</td><td>PMA_REG_PD_PRE</td><td>Pre-cursor de-emphasis enable
1’b0: Corresponds to parameter value "TRUE", enabled
1’b1: Corresponds to parameter value "FALSE", disable</td></tr>
<tr><td>0x826
Bit[4:0]</td><td>PMA_REG_TX_CFG_PRE</td><td>0x826 bit[7:5]: reserved, fixed value 0
Bit[4:0]: TX pre-cursor de-emphasis setting values, defined in the table below:
<table>
<tr><th>Setting</th><th>Gain (dB)</th></tr>
<tr><td>5'b00000</td><td>0</td></tr>
<tr><td>5'b00001</td><td>0.219</td></tr>
<tr><td>5'b00010</td><td>0.472</td></tr>
<tr><td>5’b00011</td><td>0.791</td></tr>
<tr><td>5’b00100</td><td>1.001</td></tr>
<tr><td>5’b00101</td><td>1.246</td></tr>
<tr><td>5’b00110</td><td>1.542</td></tr>
</table></td></tr>
</table>

Register address	Corresponding Parameter Name	Description
		5’b00111 1.871 5’b01000 2.109 5’b01001 2.460 5’b01010 2.714 5’b01011 3.053 5’b01100 3.446 5’b01101 3.871 5’b01110 4.215 5’b01111 4.619 5’b10000 5.043 5’b10001 5.438 5’b10010 5.958 Others reserved

Table 3-13 Post-Cursor De-Emphasis Configuration Register

Register address	Corresponding Parameter Name	Description
0x808 Bit[2]	PMA_REG_TX_PD_POST	Post-cursor de-emphasis enable **1'b0: Corresponds to parameter value "ON", enabled** 1’b1: Corresponds to parameter value "OFF", disable
0x828 Bit[4:0]	PMA_REG_CFG_POST	0x828 bit[7:5]: reserved, fixed value 0 Bit[4:0]: TX post-cursor de-emphasis setting values, defined in the table below: **Setting** / **Gain (dB)** 5'b00000 0 5'b00001 0.219 5'b00010 0.500 5’b00011 0.732 5’b00100 0.970 5’b00101 1.215 5’b00110 1.499 5’b00111 1.771 5’b01000 2.109 5’b01001 2.388 5’b01010 2.789 5’b01011 3.092 5’b01100 3.446 5’b01101 3.829 5’b01110 4.171 5’b01111 4.619 5’b10000 5.091 5’b10001 5.539

Register address	Corresponding Parameter Name	Description	
		5’b10010	5.904
		5’b10011	6.511
		5’b10100	7.001
		5’b10101	7.563
		5’b10110	8.095
		5’b10111	8.809
		5’b11000	9.588
		5’b11001	10.353
		5’b11010	11.325
		5’b11011	12.159
		5’b11100	13.205
		Others	reserved

Note: The set values of pre-/post-cursor correspond to the gain values, subject to the updated parameter values in the "UG040008_Logos2 Family FPGAs High-Speed Serial Transceiver (HSSTLP) User Guide".

Method 2: Via IPC Interface

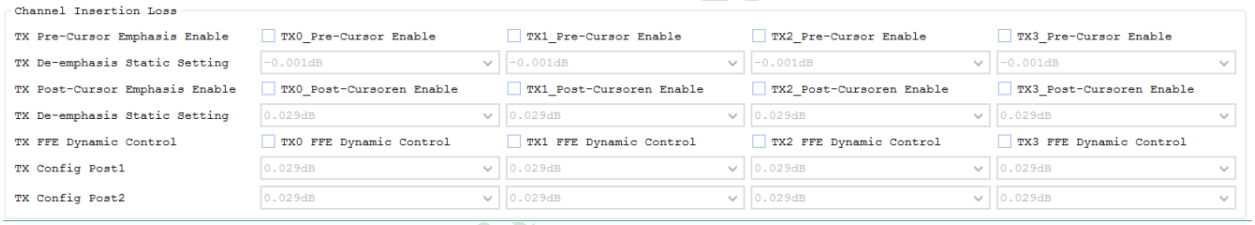

Figure 3-13 IPC Initial Value Settings for Pre and Post-Cursor De-Emphasis

1. Check [Pre-Cursor Enable] and configure the de-emphasis value to achieve pre-cursor de-emphasis
2. Check [Post-Cursor Enable] and configure the de-emphasis value to achieve post-cursor de-emphasis
3. Check [FFE Dynamic Control] and then dynamically select the post-cursor de-emphasis value through the port i_p_lx_deemp_ctl_x[1:0].

When i_p_lx_deemp_ctl_x[1:0]=00, check the [Post-Cursor] post-cursor de-emphasis value;

When i_p_lx_deemp_ctl_x[1:0]=01, check the [TX Config Post1] post-cursor de-emphasis value;

When i_p_lx_deemp_ctl_x[1:0]=10, check the [TX Config Post2] post-cursor de-emphasis value;
When i_p_lx_deemp_ctl_x[1:0]=11, reserve the value.

3.8 RX EQ Adjustment

The HSSTLP EQ module is an adaptive equalizer. By default, the adaptive function is enabled, and the EQ is automatically adapted to the channel attenuation. Manual EQ adjustment by the user is not required.

Users can also disable the adaptive function and choose to manually adjust the EQ by configuring the following registers.

Table 3-14 RX EQ Adjustment Register Description

Register address	Corresponding Parameter Name	Description
0x427 Bit[2]	PMA_REG_ANA_RX_EQ1_R_SET_FB_O_SEL	1'b0: Corresponds to the parameter value "FALSE", manually adjusts the EQ1 value using PMA_REG_RX_EQ1_R_SET_FB 1'b1: Corresponds to the parameter value "TRUE", auto-adjust the EQ1 value (default)
0x427 Bit[3]	PMA_REG_ANA_RX_EQ2_R_SET_FB_O_SEL	1'b0: Corresponds to the parameter value "FALSE", manually adjusts the EQ2 value using PMA_REG_RX_EQ2_R_SET_FB 1'b1: Corresponds to the parameter value "TRUE", auto-adjusts the EQ2 value (default)
0x428 Bit[3:0]	PMA_REG_RX_EQ1_R_SET_FB	EQ1 setting values, valid with manual adjustment, 0.5dB/step During the adjustment, EQ1 and EQ2 setting values must be equal, equivalent to an EQ value of 1dB/step
0x429 Bit[6:3]	PMA_REG_RX_EQ2_R_SET_FB	EQ2 setting values, valid with manual adjustment, 0.5dB/step During the adjustment, EQ1 and EQ2 setting values must be equal, equivalent to an EQ value of 1dB/step

3.9 CLK Aligner Function

3.9.1 RX clk aligner

After bypassing the RX Bridge FIFO, the clock phase of P_RCLK2FABRIC can be adjusted through the clk aligner module. This adjustment ensures that the phase of the user-side read data clock P_RX_CLK_FR_CORE is correspondingly adjusted, thereby guaranteeing that P_RX_CLK_FR_CORE can correctly read the P_RDATA data output by HSSTHP.

Related registers and ports for the RX clk aligner function are shown in Tables 3-15 and 3-16.

Table 3-15 RX CLK Aligner Register Description

Register Address	Corresponding Parameter Name	Description
0x000 Bit[7]	PCS_BYPASS_BRIDGE_FIFO	Bypass module Rx Bridge FIFO control, [7:6]=2'b10 bypass Rx Bridge FIFO [7] or [6]=1'b0: Corresponds to the parameter value "FALSE" [7] or [6]=1'b1: Corresponds to the parameter value "TRUE"
0x000 Bit[6]	PCS_BYPASS_BRIDGE	
0x029 Bit[2]	PCS_CA_DYN_DLY_SEL_RX	1'b1: Corresponds to parameter value "TRUE", enable CLK Aligner
0x029 Bit[1]	PCS_CA_DYN_DLY_EN_RX	1'b1: Corresponds to parameter value "TRUE", CLK Aligner delay step determined by register PCS_CA_RX or port P_CIM_CLK_ALIGNER_RX;
0x029 Bit[0]	PCS_CA_RSTN_RX	1'b1: Corresponds to the parameter value "TRUE", the Rx CLK Aligner releases the reset.
0x02a Bit[7:0]	PCS_CA_RX	Clock aligner delay value adjustment controlled by registers Bit[7]: reserved bit with invalid value; When Bit[6]=0: bit[5:0] is the delay adjustment value, the adjustment unit is 25ps, in Gray code format; When Bit[6]=1: bit[5:0] is the delay adjustment value, the adjustment unit is 50ps, in Gray code format; Gray code conversion formula: gray=((bin>>1)^ bin)

Table 3-16 RX CLK Aligner Port Description

Port	I/O	Clock Domain	Description
P_CIM_CLK_ALIGNER_RX[7:0]	I	Asynchronous Signal	Clock aligner delay value adjustment controlled by RX LANE port; Bit[7]: reserved bit with invalid value; When Bit[6]=0: bit[5:0] is the delay adjustment value, the adjustment unit is 25ps, in Gray code format; When Bit[6]=1: bit[5:0] is the delay adjustment value, the adjustment unit is 50ps, in Gray code format; Gray code conversion formula: gray=((bin>>1)^ bin)
P_CIM_DYN_DLY_SEL_RX	I	Asynchronous Signal	CLK Aligner delay step control selection 1'b0: Controlled by register PCS_CA_RX ; 1'b1: Controlled by port P_CIM_CLK_ALIGNER_RX

TX clk aligner

After bypassing the TX Bridge FIFO, the clock phase of P_TCLK2FABRIC can be adjusted through the clk aligner module. This adjustment ensures that the phase of the user-side read data clock P_TX_CLK_FR_CORE is correspondingly adjusted, thereby guaranteeing that P_TX_CLK_FR_CORE can correctly read the P_TDATA data output on the logic side.

Related registers and ports for the TX clk aligner function are shown in Tables 3-17 and 3-18.

Table 3-17 TX CLK Aligner Register Description

Register address	Corresponding Parameter Name	Description
0x010 Bit[2]	PCS_TX_BYPASS_BRIDGE_FIFO	Bypass module Tx Bridge FIFO control, [7:6]=2'b10 bypass Tx Bridge FIFO [2] or [1]=1'b0: Corresponds to the parameter value "FALSE" [2] or [1]=1'b1: Corresponds to the parameter value "TRUE"
0x010 Bit[1]	PCS_TX_BYPASS_BRIDGE_UINT	
0x2b Bit[2]	PCS_CA_DYN_DLY_SEL_TX	1'b1: Corresponds to the parameter value "TRUE", enables CLK Aligner
0x02b Bit[1]	PCS_CA_DYN_DLY_EN_TX	1'b1: Corresponds to parameter value "TRUE", CLK Aligner delay step determined by register PCS_CA_TX or port P_CIM_CLK_ALIGNER_TX;
0x02b Bit[0]	PCS_CA_RSTN_TX	1'b1: Corresponds to the parameter value "TRUE", Tx CLK Aligner releases the reset
0x02c Bit[7:0]	PCS_ CA_TX	Clock aligner delay value adjustment controlled by registers Bit[7]: reserved bit with invalid value; When Bit[6]=0: bit[5:0] is the delay adjustment value, the adjustment unit is 25ps, in Gray code format; When Bit[6]=1: bit[5:0] is the delay adjustment value, the adjustment unit is 50ps, in Gray code format; Gray code conversion formula: gray=((bin>>1)^ bin)

Table 3-18 TX CLK Aligner Port Description

Port	I/O/	Clock Domain	Description
P_CIM_CLK_ALIGNER_TX[7:0]	I	Asynchronous Signal	Clock aligner delay value adjustment controlled via TX LANE port; Bit[7]: reserved bit with invalid value; When Bit[6]=0: bit[5:0] is the delay adjustment value, the adjustment unit is 25ps, in Gray code format; When Bit[6]=1: bit[5:0] is the delay adjustment value, the adjustment unit is 50ps, in Gray code format; Gray code conversion formula: gray=((bin>>1)^ bin)
P_CIM_DYN_DLY_SEL_TX	I	Asynchronous Signal	CLK Aligner delay step control selection 1’b0: Controlled by register PCS_CA_TX; 1’b1: Controlled by port P_CIM_CLK_ALIGNER_TX.

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