Logos Series FPGA Clock Resources (Clock&PLL) User Guide

(UG020004, V1.8)

(2022.07.18)

Revisions History

Document Revisions

Version	Date of Release	Revisions
V1.8	18.07.2022	Initial release.

About this Manual

Terms and Abbreviations

Terms and Abbreviations	Meaning
USCM	User Select Clock Module
SRB	Signal Relay Block
GTP	General Technology Primitive

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Chapter 1 General Introduction

Logos series products are divided into different numbers of regions, offering extensive on-chip clock resources, including PLL, three types of clock networks: global clock, regional clock, and I/O clock. Among them, the I/O clock has the characteristics of high frequency, low clock skew, and short delay time. For details on the clock resources, see the table below:

Table 1-1 Clock Resources of Logos Series Products

Features	**PGL12G**	**PGL22G**	**PGL25G**	**PGL50H/ PGL50G**	**PGL100H**
Number of Regions	4	6	4	6	10
Number of Global Clocks	20	20	20	30	30
Number of global clocks supported by each region	16	12	16	16	16
Number of regional clocks supported by each region	4	4	4	4	4
Number of IO BANKs	4	6	4	4	6
Number of IO clocks supported by each IO BANK	2	2	4	The upper and lower BANKs each support four I/O clocks; the left and right BANKs each support six I/O clocks	The upper and lower BANKs each support four I/O clocks; the left and right BANKs each support ten I/O clocks
Total Number of IO Clocks	8	12	16	20	28
Number of PLLs	4	6	4	5	8

Furthermore, to enhance clock performance, the Logos series products also provide specialized clock-related IOs, including three types: clock input pins, PLL reference clock input pins, and PLL feedback input clock pins. Compared to normal I/O, these clock input pins utilize the FPGA's dedicated clock network, thus achieving better clock performance. When not used as clock inputs, these clock input pins can be configured for use as normal I/O.

Chapter 2 Detailed Introduction

2.1 Clock Input

The clock input pins can use dedicated clock routing to directly input into the internal clock network, including global, regional, or I/O clocks, reducing interference and improving clock quality. Clock input pins can be a pair of differential input ports or a single-ended input port, with both P side and N side usable as single-ended. When not used as clock inputs, dedicated clock pins can still be used as normal I/O. The figure below shows a diagram of differential time input.

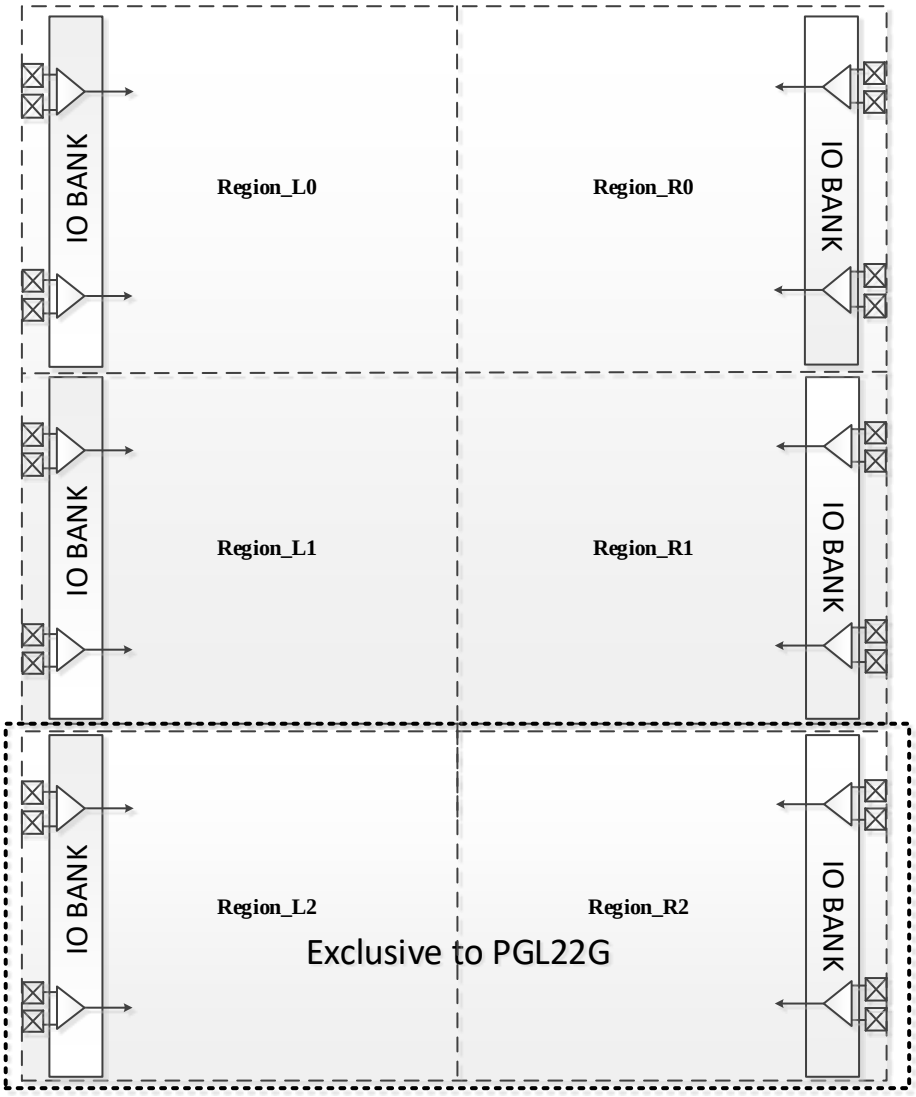

Figure 2-1 Diagram of Clock Input Distribution for Logos Series PGL12G and PGL22G

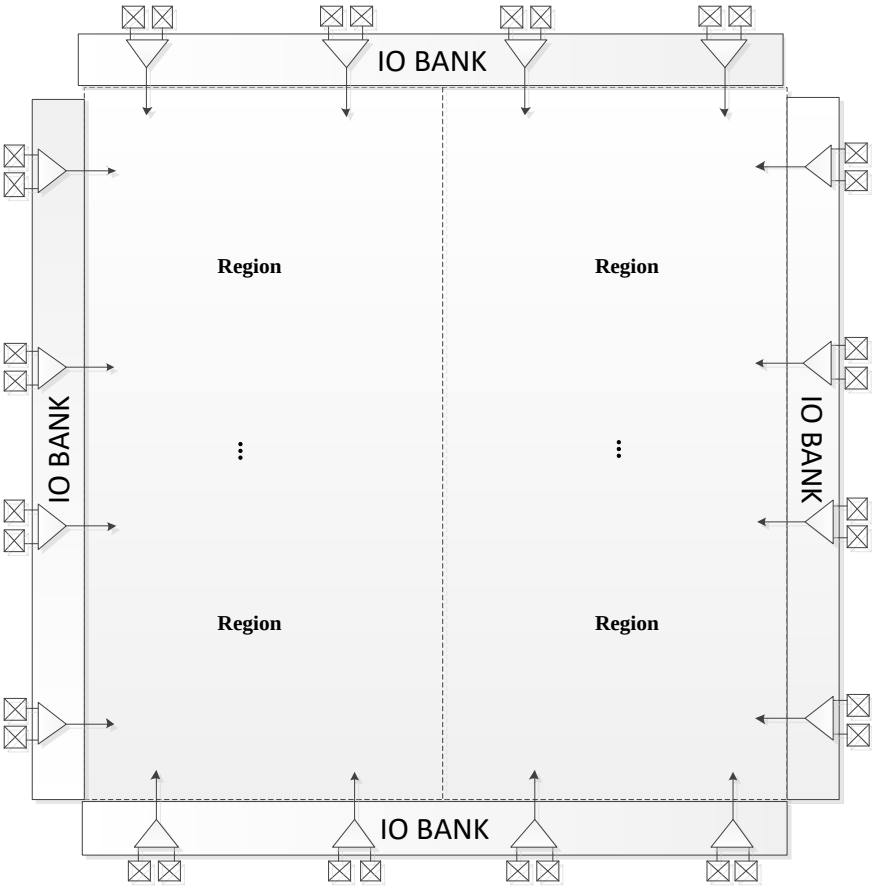

Figure 2-2 Diagram of Clock Input Distribution for Logos Series PGL25G, PGL50H, PGL50G, and PGL100H

To meet the need to adjust the input clock phase in some applications, the clock input pins of the Logos series products offer an optional time delay function. The time delay of the input clock is directly achieved through GTP_IOCLKDELAY, the schematic of which is shown in the figure below, with port and parameter descriptions in the table below.

Users can statically configure the delay step (adjust the number of delay chains, with each step delaying by 25ps, the minimum delay count is 0, and the maximum is 127 (8'b0–8'b0111_1111)), or dynamically obtain the delay step using the on-chip DLL. Furthermore, dynamic fine-tuning of the delay step can be performed through user control logic at on the basis of dynamic/static configuration. In static configuration adjustment mode, MOVE and DIRECTION are not working.

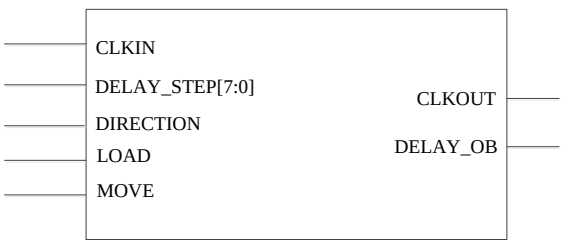

Figure 2-3 Diagram of GTP_IOCLKDELAY

Table 2-1 Port Description of GTP_IOCLKDELAY

Port Signal	Input/Output	Description
CLKIN	Input	Clock input from pin
DELAY_STEP [7:0]	Input	Delay step from DLL
DIRECTION	Input	Set to 0 to dynamically increase the delay step, set to 1 to dynamically decrease the delay step
LOAD	Input	Active high, loading static parameter configuration or delay step value from DLL, when LOAD=1'b0, the delay time can be dynamically adjusted
MOVE	Input	Falling edge triggers dynamic fine-tuning, increasing or decreasing a step depending on the DIRECTION.
CLKOUT	Output	Delayed clock output
DELAY_OB	Output	Dynamic fine-tuning overflow flag of delay step; it goes high when internal DELAY STEP is 127 with DIRECTION set to 0; it goes high when internal delay step is 0 with DIRECTION set to 1

Table 2-2 Parameter Description of GTP_IOCLKDELAY

Parameter	Description
DELAY_STEP_VALUE	Static delay step, effective when DELAY_STEP_SEL is set to "PARAMETER"
DELAY_STEP_SEL	When set to "PORT", it selects the delay step from DLL; When set to "PARAMETER", it selects the delay step from the static parameter configuration

The use of GTP_IOCLKDELAY can be instantiated directly with source code, taking Verilog instantiation as an example:

```
GTP_IOCLKDELAY
#(
.DELAY_STEP_VALUE     (8'd10          ),    //Used for static DELAY STEP setting, 0~127
.DELAY_STEP_SEL       ("PARAMETER")     // "PARAMETER" or "PORT"
)
I_IOCLKDELAY (
.CLKIN                (CLKIN          ),
.DELAY_STEP           (DELAY_STEP     ),
.CLKOUT               (CLKOUT         ),
.DIRECTION            (DIRECTION      ),
.LOAD                 (LOAD           ),
.MOVE                 (MOVE           ),
.DELAY_OB             (DELAY_OB       )
);
```

In the above example, with the CLKIN period being 2000ps and the CLKDLY_STEP_VALUE parameter set to 10, CLKOUT is delayed by 250ps relative to CLKIN. The timing diagram is as follows. The LOAD is set to 1, and DIRECTION and MOVE are set to 0.

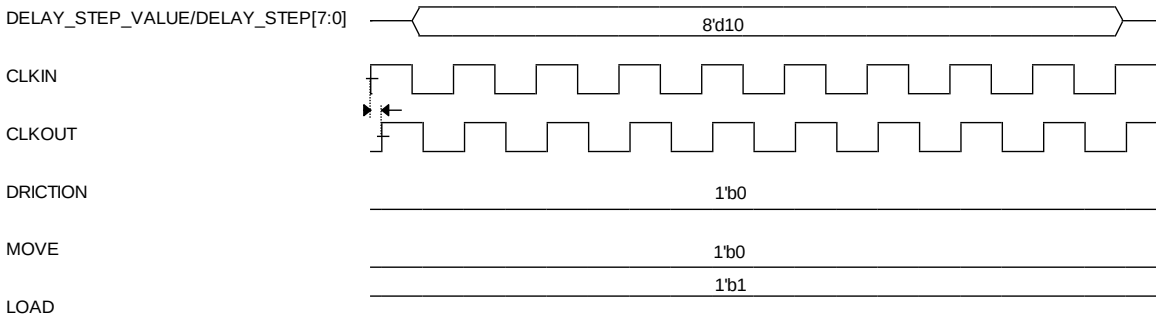

Figure 2-4 Timing Diagram for Static Configuration of GTP_IOCLKDELAY

When adjusting in manual mode, LOAD=1'b0, MOVE acts as the trigger clock for manual mode, triggered on the falling edge. With each trigger, the input clock is increased or decreased by one step. DIRECTION controls the direction of the step, decreasing the step when DIRECTION=1'b1; and increasing the step when DIRECTION=1'b0. The corresponding timing diagram is as follows, with each increase or decrease in time being T1.

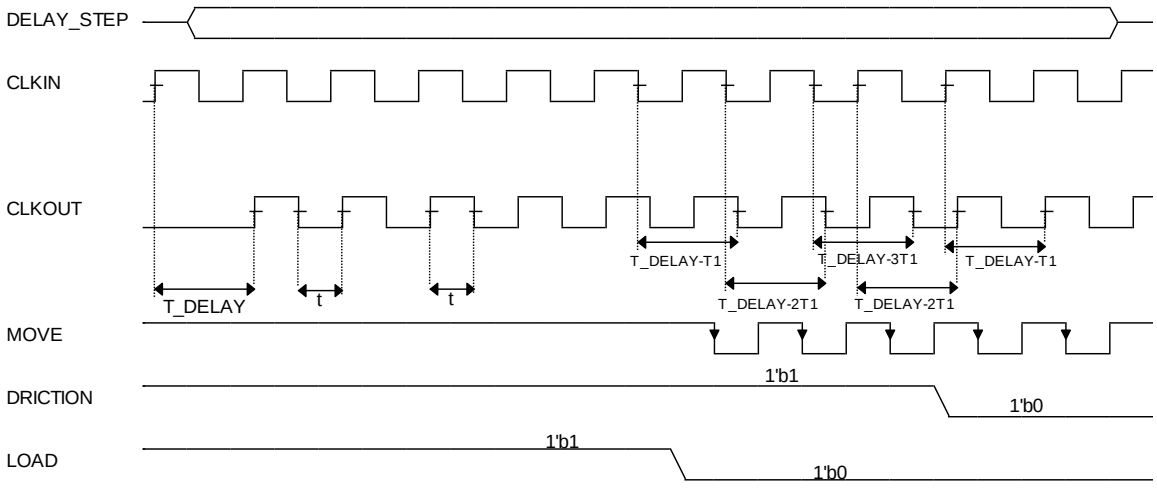

Figure 2-5 Timing Diagram for Manual Delay Example of GTP_IOCLKDELAY

For DELAY_OB, as described in the diagram below, after the moment t_0, DIRECTION=1'b0; if the count M of MOVE falling edges plus the value of DELAY_STEP_VALUE set or the DELAY_STEP value x from DLL reaches 127, then DELAY_OB transitions to a high level, indicating that the maximum adjustable DELAY TIME has been reached and no further steps can be added; when DELAY_STEP_VALUE or DELAY_STEP is set to 8'd0, if DIRECTION=1'b1, then DELAY_OB transitions to a high level, indicating that the minimum adjustable DELAY TIME has been reached and no further steps can be reduced.

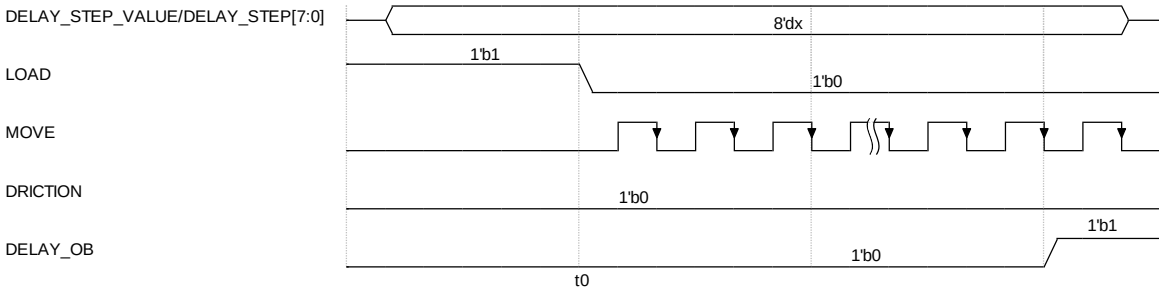

Figure 2-6 Example Timing Diagram for GTP_IOCLKDELAY Signal DELAY_OB Transitioning to High Level

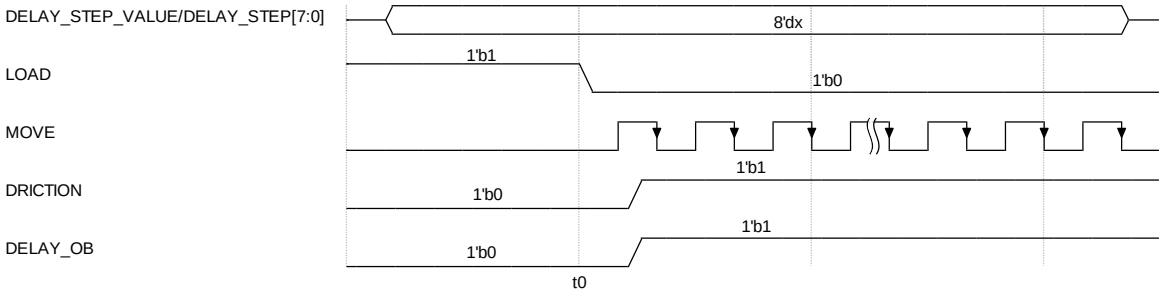

Figure 2-7 Example Timing Diagram for GTP_IOCLKDELAY Signal DELAY_OB Transitioning to High Level

2.2 Global Clock

The global clock input sources for Logos series products are shown in the table below, and the input path diagram is shown in the figure:

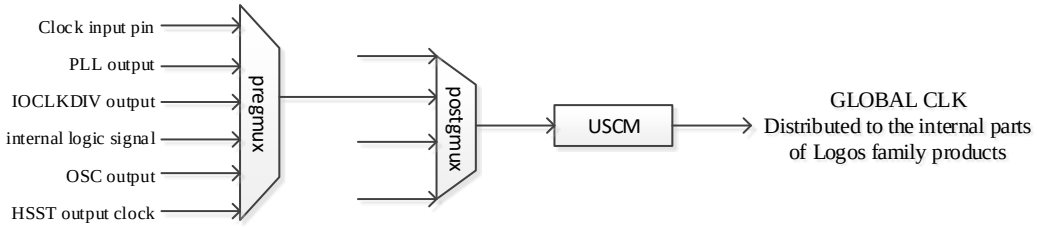

Figure 2-8 Diagram of Global Clock Source Paths for Logos Series Products

Table 2-3 Global Clock Input Sources for Logos Series Products

Global Clock Input Sources	Description
Clock input pin	Clock entered from the clock input pin
PLL output	The PLL's output clock corresponds to the PLL output clocks CLKOUT0/CLKOUT1/CLKOUT2/CLKOUT3/CLKOUT4/CLKOUT5
IOCLKDIV output	Divided clock output by IOCLKDIV
OSC output	Clock output from the internal oscillator
Internal logic signal	Internal logic signal, generally not recommended for use, as it can easily affect the quality of the input clock
HSST output (devices with HSST)	The HSST's 10 output clocks (RCLK2FABRIC[3:0], TCLK2FABRIC[3:0], REFCK2CORE_0, REFCK2CORE_1); PGL50H has one HSST, PGL100H has two HSSTs

USCM is a intelligent 2-to-1 clock signal selector that controls the selection signal, allowing output of the desired signal regardless of where it is triggered in the clock, and without glitches. It provides enable and selection functions for the global clock, supporting three modes: CLKBUFG, CLKBUFGCE, and CLKBUFGMUX. CLKBUFG provides a simple clock BUFFER function, usually automatically inserted by software; CLKBUFGCE is a clock BUFFER with clock enable, implemented by instantiating GTP directly in RTL; CLKBUFGMUX is a clock selector with selection functionality.

The diagram of GTP_CLKBUFGCE is shown in the figure below, with the corresponding descriptions of ports and parameters in the tables below:

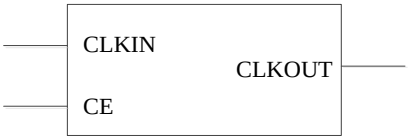

Figure 2-9 Block Diagram of GTP_CLKBUFGCE

Table 2-4 Port Description of GTP_CLKBUFGCE

Port Signal	Direction	Description
CLK	Input	Input Clock
CE	Input	Synchronous enable signal, CE is effective only when there is a clock at CLKIN. When CE=1'b1, CLKOUT=CLKIN; when CE=1'b0, CLKOUT=1'b0
CLKOUT	Output	Output clock

Table 2-5 Parameter Description of GTP_CLKBUFGCE

Parameter	Description
DEFAULT_VALUE	This parameter only supports configured to 0, when configured to 1, the CLKOUT output is consistent with the configuration to 0. When CE=0, output DEFAULT_VALUE; When CE=1, output CLKIN;

Taking Verilog as an example, the instantiation of GTP_CLKBUFGCE is as follows:

```
GTP_CLKBUFGCE
#(
.DEFAULT_VALUE  (1'b0            ) //1'b0;
) I_GTP_CLKBUFGCE (
.CLKIN                (CLKIN      ),
.CE                   (CE         ),
.CLKOUT               (CLKOUT     ));
```

When CE is high, CLKOUT=CLKIN; when CE is low, CLKOUT output is low level, with the timing diagram shown in the figure below:

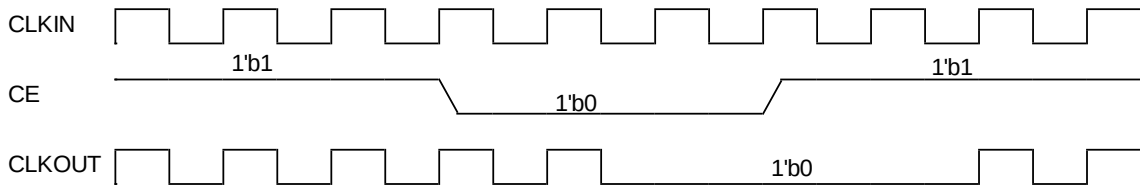

Figure 2-10 Timing Diagram of GTP_CLKBUFGCE

The Diagram of GTP_CLKBUFG is as shown in the figure below, with its port descriptions in the table below:

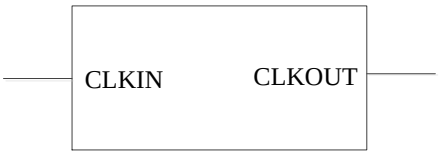

Figure 2-11 Block Diagram of GTP_CLKBUFG

Table 2-6 Port Description of GTP_CLKBUFG

Port Signal	**Direction**	**Description**
CLKIN	Input	Input Clock
CLKOUT	Output	Output clock

GTP_CLKBUFG can be used by directly instantiating the module, taking Verilog instantiation as an example:

```
GTP_CLKBUFG
    I_ GTP_CLKBUFG (
    .CLKOUT          (CLKOUT),
    .CLKIN           (CLKIN    ));
```

The timing diagram of GTP_CLKBUFG is shown in the figure below:

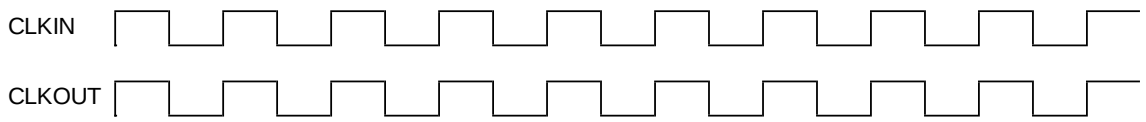

Figure 2-12 Timing Diagram of GTP_CLKBUFG

GTP_CLKBUFGMUX can be used for dynamic switching between two clock sources, allowing users to choose forced switching (corresponding to TRIGGER_MODE="NORMAL"), which may lead to glitches; it can also reduce the glitches by synchronous switching function, which should be configured to clock falling edge trigger mode (corresponding to TRIGGER_MODE="NEGEDGE"), synchronous switching requires both input clocks to be normal, with neither constantly at 0 nor 1.

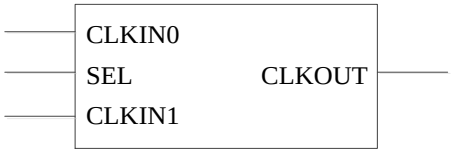

Figure 2-13 Block Diagram of GTP_CLKBUFGMUX

Table 2-7 Port Description of GTP_CLKBUFGMUX

Port Signal	**Direction**	**Description**
CLKIN0	Input	Input clock 0
CLKIN1	Input	Input clock 1
SEL	Input	Clock selection signal, 0 selects CLK0; 1 selects CLK1;
CLKOUT	Output	Output clock

Table 2-8 Parameter Description of GTP_CLKBUFGMUX

Parameter	**Description**
TRIGGER_MODE	Modes "NEGEDGE", "NORMAL"

GTP_CLKBUFGMUX can be used by directly instantiating modules, taking Verilog instantiation as an example:

```
GTP_CLKBUFGMUX
#(
.TRIGGER_MODE              ("NEGEDGE"      ) //    "NEGEDGE",
) I_CLKBUFGMUX (
    .CLKIN0                (CLK0           ),
```

```
.CLKIN1          (CLK1          ),
.SEL             (SEL           ),
.CLKOUT          (CLKOUT        ))
```

Its timing diagram is shown below:

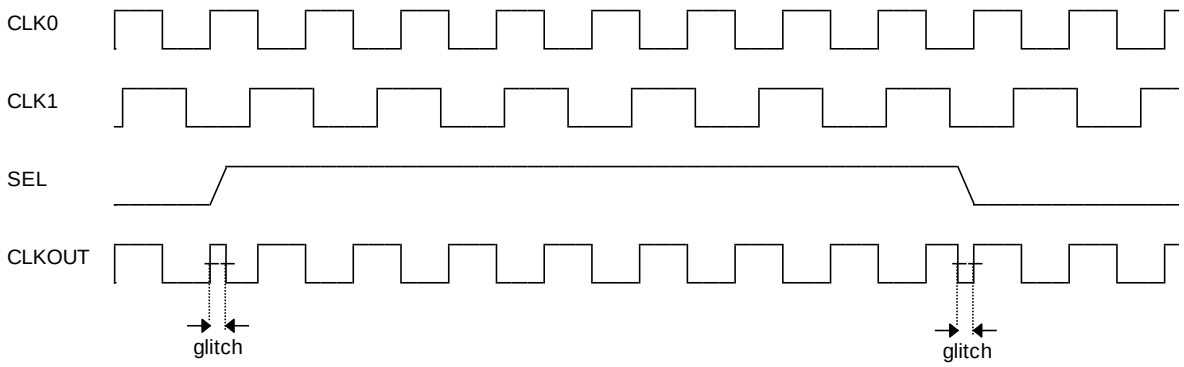

Figure 2-14 USCM's CLKBUFGMUX Mode Timing Diagram (TRIGGER_MODE="NORMAL")

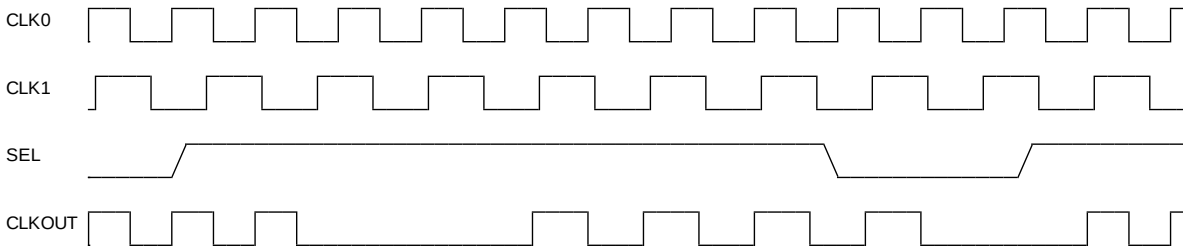

Figure 2-15 USCM's CLKBUFGMUX Mode Timing Diagram (TRIGGER_MODE="NEGEDGE")

2.3 Regional Clock

The internal logic resources of the Logos series products are distributed by region, consisting of multiple regions, as shown in the figure below. Each region is composed of a variable number of CLMs, DRMs, ADCs, IOs, and APM columns.

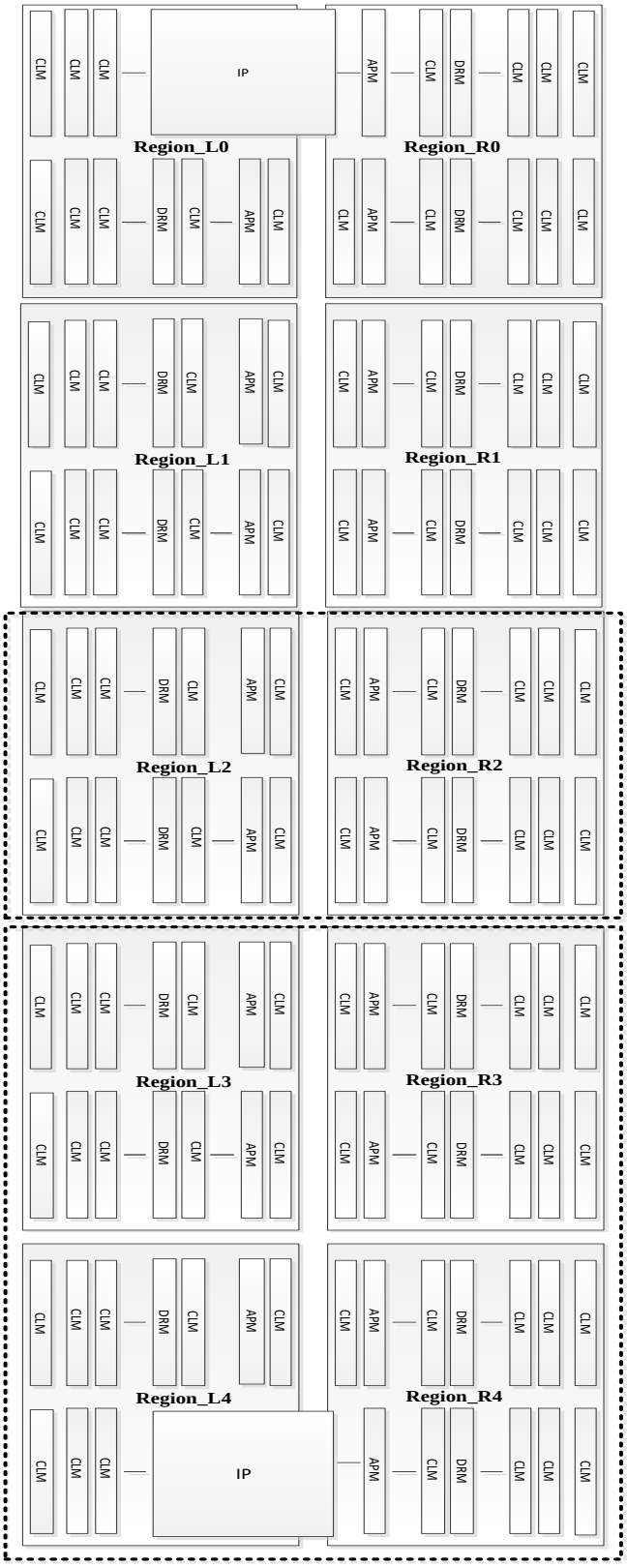

Figure 2-16 Diagram of Regional Distribution for Logos Series

Notes:

1. The IP in the figure refers to ADC (PGL12G and PGL22G) or HSST (PGL50H and PGL100H)

2. The regions Region_L2 and Region_R2 enclosed by the dashed line in the diagram are specific to PGL22G, PGL50H, PGL50G

3. The regions Region_L3, Region_R3, Region_L4, and Region_R4 enclosed by the dashed line in the diagram are specific to PGL100H

Each region supports four regional clocks, which have the advantage of lower delay and skew compared to the global clock but have a limited distribution range. The source paths for the regional clocks are as shown in the figure below, and the input sources for the regional clocks are listed in the table below:

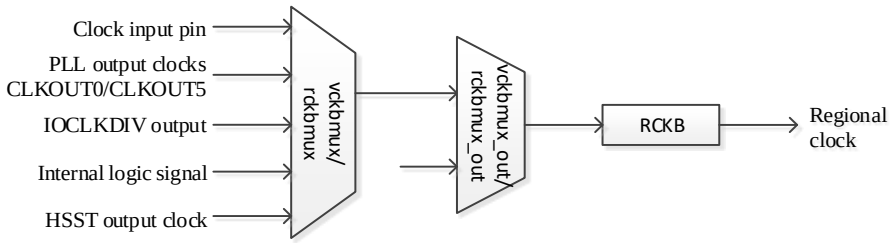

Figure 2-17 Diagram of Regional Clock Source Path

Table 2-9 Logos Regional Clock Sources

Regional Clock Input Source	**Description**
Clock input pin	The clock input from the clock pins within each region can only serve as the input source for that regional clock
PLL outputs CLKOUT0/CLKOUT5	PGL12G: PLL0's CLKOUT5 can drive the Region CLOCK of L0 and R0. PLL1's CLKOUT5 can drive the Region CLOCK of L0, R0, L1, and R1. PLL2's CLKOUT5 can drive the Region CLOCK of L0, R0, L1, and R1. PLL3's CLKOUT5 can drive the Region CLOCK of L2 and R2. PGL22G: PLL0's CLKOUT5 can drive the Region CLOCK of L0 and R0. PLL1's CLKOUT5 can drive the Region CLOCK of L0, R0, L1, and R1. PLL2's CLKOUT5 can drive the Region CLOCK of L0, R0, L1, and R1. PLL3's CLKOUT5 can drive the Region CLOCK of L1, R1, L2, and R2. PLL4's CLKOUT5 can drive the Region CLOCK of L1, R1, L2, and R2. PLL5's CLKOUT5 can drive the Region CLOCK of L2 and R2. PGL25G: PLL0's CLKOUT5 can drive the Region CLOCK of L0 and R0. PLL1's CLKOUT5 can drive the Region CLOCK of L0, R0, L1, and R1. PLL2's CLKOUT5 can drive the Region CLOCK of L0, R0, L1, and R1. PLL3's CLKOUT5 can drive the Region CLOCK of L1 and R1. PGL50H/ PGL50G: PLL0's CLKOUT0 can drive the Region CLOCK of L0 and R0. PLL0's CLKOUT5 can drive the Region CLOCK of L0, R0, L1, and R1. PLL1's CLKOUT0 can drive the Region CLOCK of L1 and R1. PLL1's CLKOUT5 can drive the Region CLOCK of L0, R0, L1, and R1. PLL2's CLKOUT0 can drive the Region CLOCK of L1 and R1. PLL2's CLKOUT5 can drive the Region CLOCK of L1, R1, L2, and R2. PLL3's CLKOUT0 can drive the Region CLOCK of L2 and R2. PLL3's CLKOUT5 can drive the Region CLOCK of L1, R1, L2, and R2. PLL4's CLKOUT0/CLKOUT5 can drive the Region CLOCK of L2 and R2. PGL100H: PLL0's CLKOUT0 can drive the Region CLOCK of L0 and R0. PLL0's CLKOUT5 can drive the Region CLOCK of L0, R0, L1, and R1. PLL1's CLKOUT0 can drive the Region CLOCK of L1 and R1. PLL1's CLKOUT5 can drive the Region CLOCK of L0, R0, L1, and R1. PLL2's CLKOUT0 can drive the Region CLOCK of L1 and R1. PLL2's CLKOUT5 can drive the Region CLOCK of L1, R1, L2, and R2. PLL3's CLKOUT0 can drive the Region CLOCK of L2 and R2.

Regional Clock Input Source	Description
	PLL3's CLKOUT5 can drive the Region CLOCK of L1, R1, L2, and R2. PLL4's CLKOUT0 can drive the Region CLOCK of L2 and R2. PLL4's CLKOUT5 can drive the Region CLOCK of L2, R2, L3, and R3. PLL5's CLKOUT0 can drive the Region CLOCK of L3 and R3. PLL5's CLKOUT5 can drive the Region CLOCK of L2, R2, L3, and R3. PLL6's CLKOUT0 can drive the Region CLOCK of L3 and R3. PLL6's CLKOUT5 can drive the Region CLOCK of L3, R3, L4, and R4. PLL7's CLKOUT0 can drive the Region CLOCK of L4 and R4. PLL7's CLKOUT5 can drive the Region CLOCK of L3, R3, L4, and R4.
IOCLKDIV output	The divided clock output by IOCLKDIV within each region can only serve as the input source for that regional clock
internal logic signal	Internal logic signal, generally not recommended for use, as it can easily affect the quality of the input clock
HSST output (devices with HSST)	The output clocks RCLK2FABRIC[1] and RCLK2FABRIC[3] from PGL50H's HSST can drive the Region CLOCK of L0 and R0 The output clocks RCLK2FABRIC[1] and RCLK2FABRIC[3] from the upper HSST of PGL100H can drive the Region CLOCK of L0 and R0, and The output clocks RCLK2FABRIC[1] and RCLK2FABRIC[3] from the lower HSST can drive the Region CLOCK of L4 and R4

Users can drive logic units within the region by instantiating the GTP_CLKBUFR, which is shown in the figure below, with its port description provided in the table below:

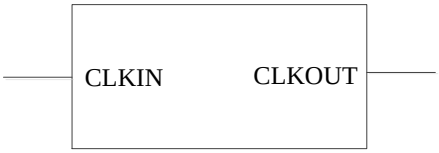

Figure 2-18 Block Diagram of GTP_CLKBUFR

Table 2-10 Port Description of GTP_CLKBUFR

Port Signal	Direction	Description
CLKIN	Input	Input Clock
CLKOUT	Output	Output clock

GTP_CLKBUFR can be used by directly instantiating the module, taking Verilog instantiation as an example:

```
GTP_CLKBUFR
    I_ GTP_CLKBUFR (
    .CLKOUT         (CLKOUT     ),
    .CLKIN          (CLKIN      ))
```

The timing diagram of GTP_CLKBUFR is shown in the figure below:

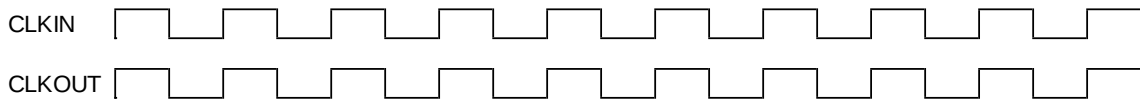

Figure 2-19 Timing Diagram of GTP_CLKBUFR

2.4 I/O Clock

The I/O clock provides the high-speed and low-skew clock to I/O logic, and the I/O clock in each region can only directly drive the I/O logic resources of that region. By using the global clock network, it can drive all FPGA resources. The distribution of the I/O clocks in the Logos series FPGA is shown in the figure below:

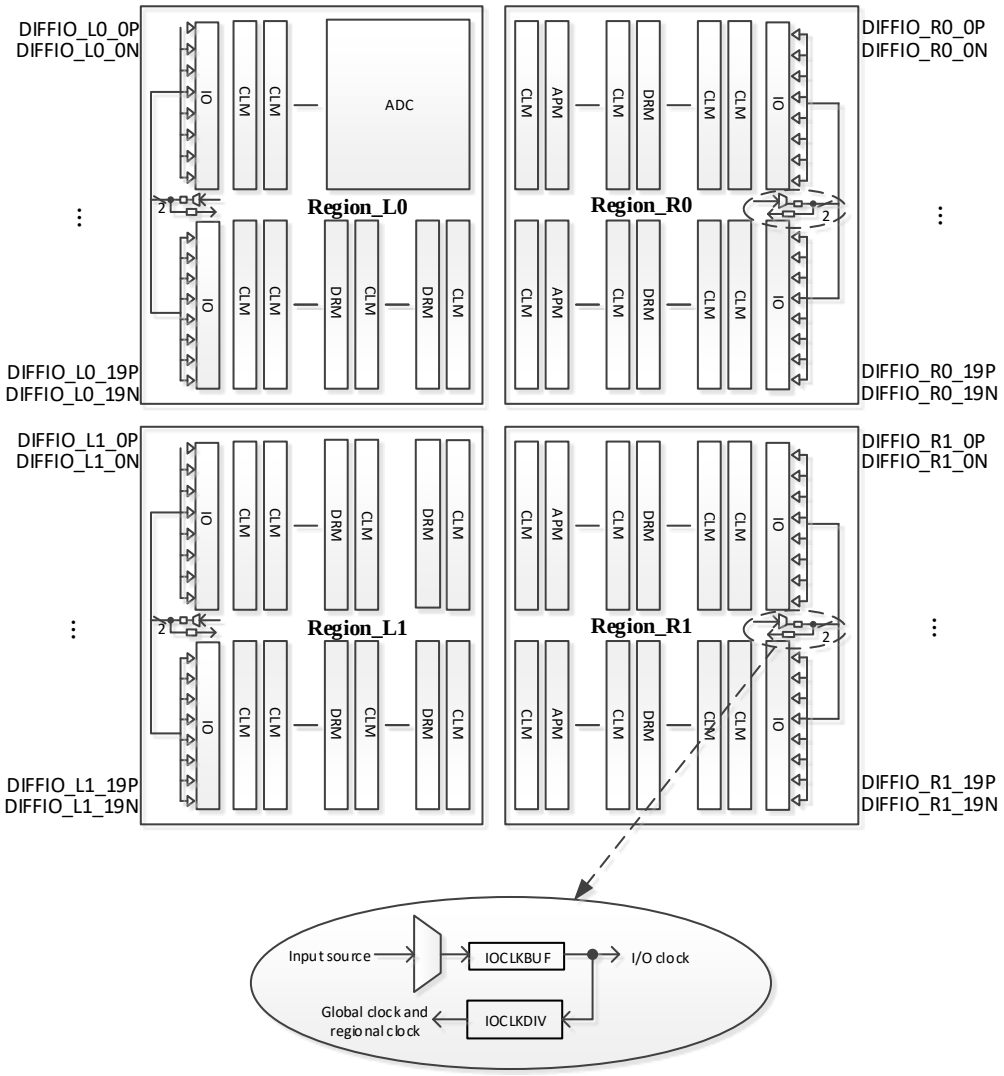

Figure 2-20 Diagram of the I/O Clock Distribution for the Logos Series PGL12G

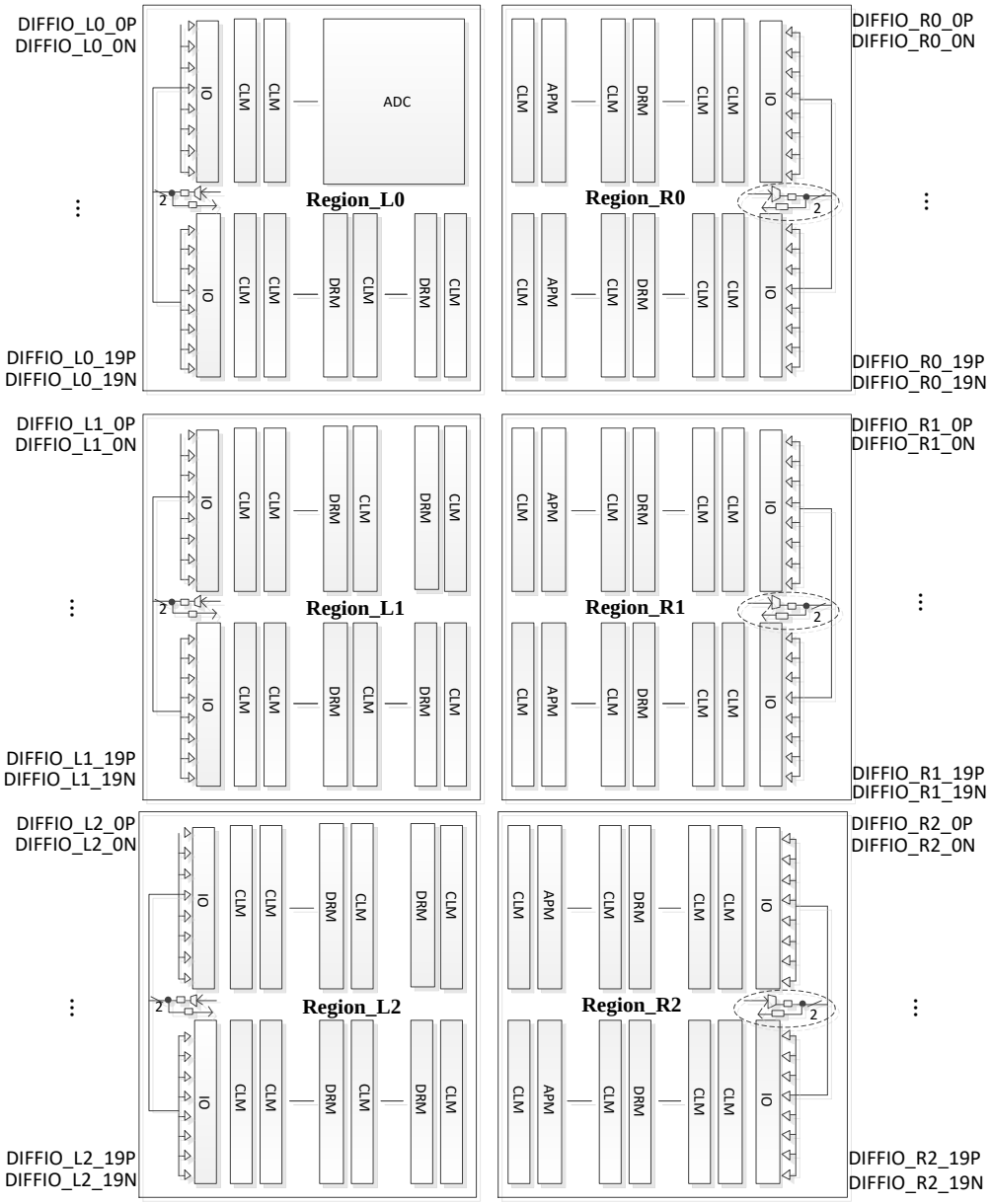

Figure 2-21 Diagram of the I/O Clock Distribution for the Logos Series PGL22G

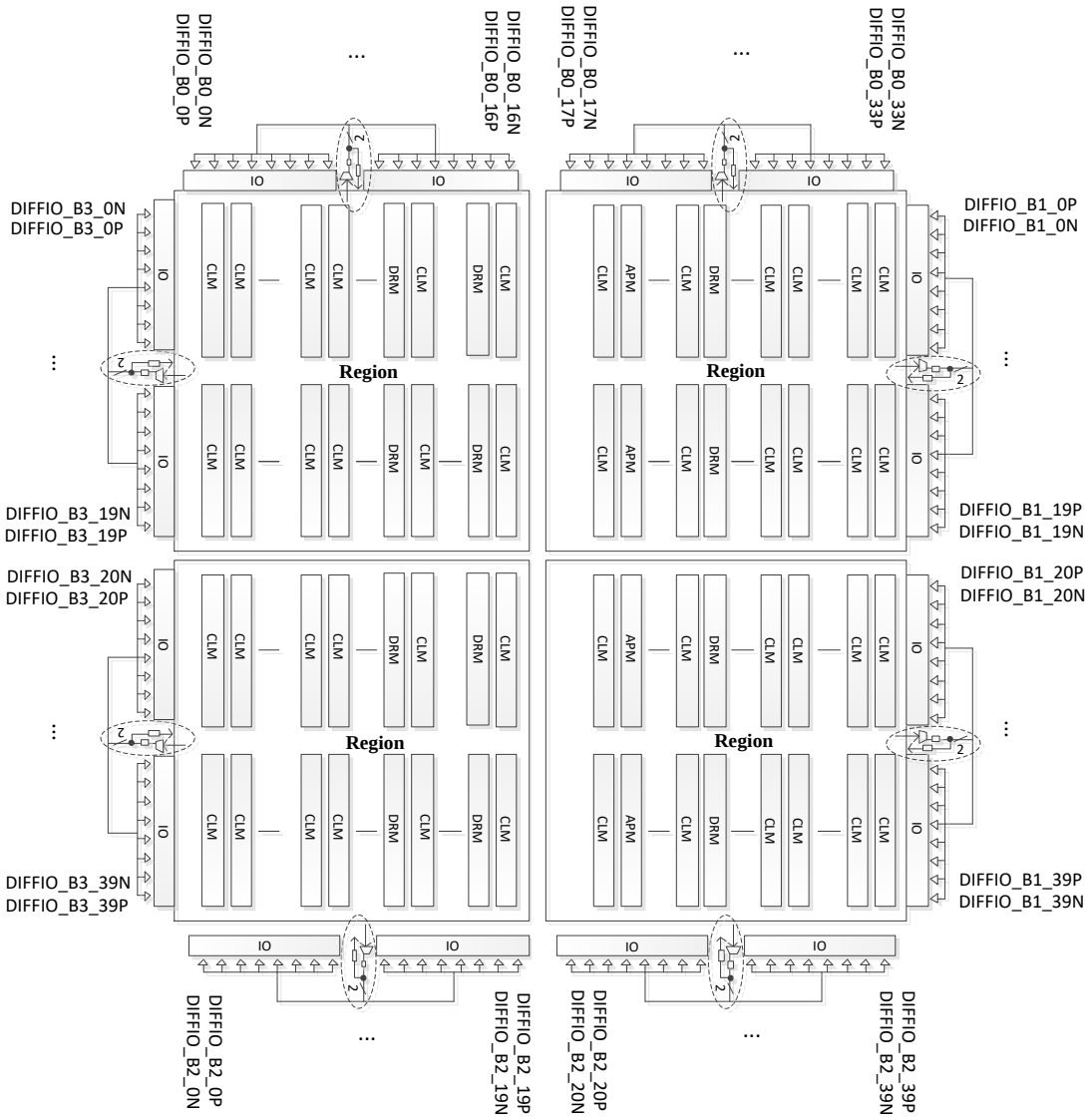

Figure 2-22 Diagram of the I/O Clock Distribution for the Logos Series PGL25G

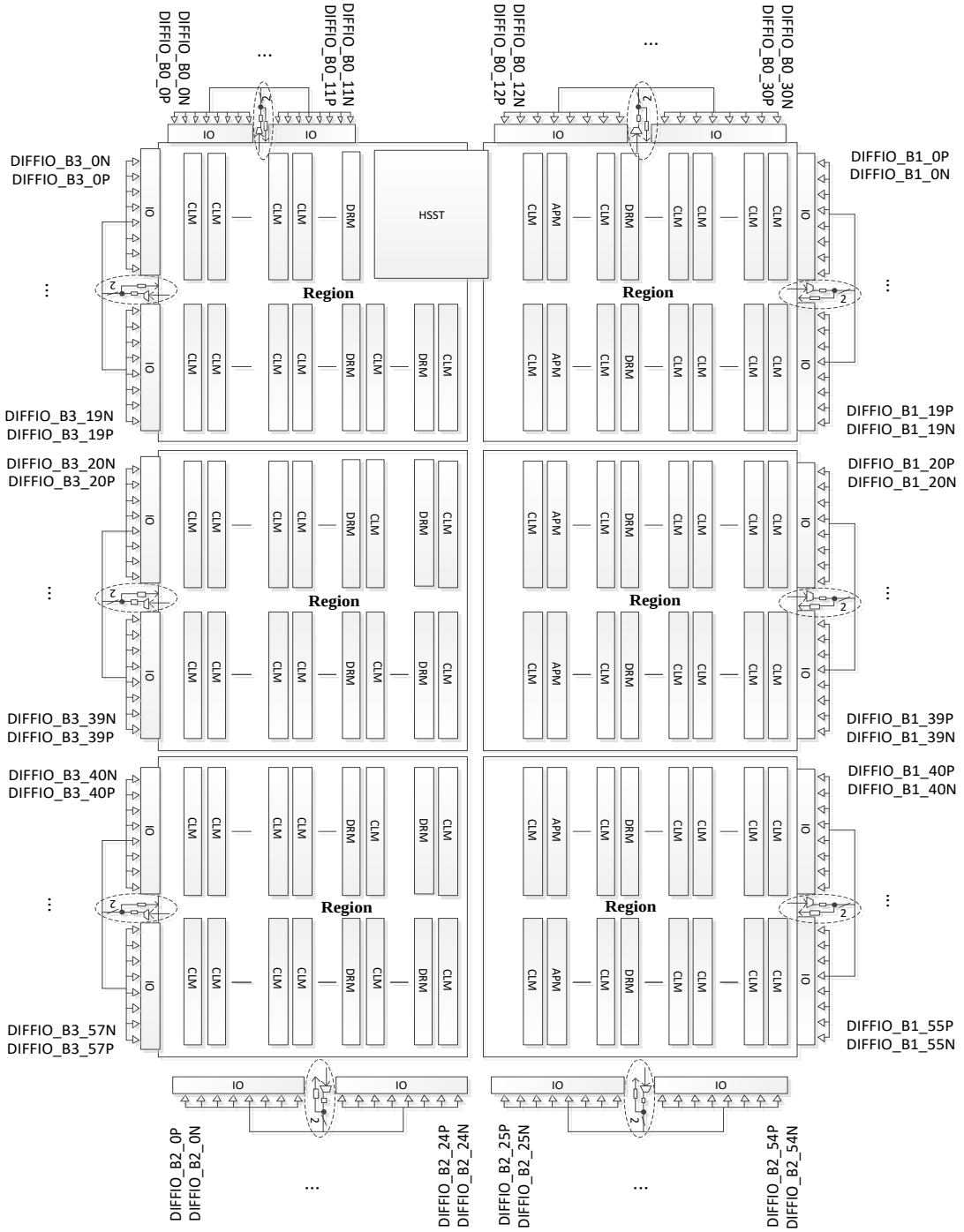

Figure 2-23 Diagram of the I/O Clock Distribution for the Logos Series PGL50H and PGL50G

Note: The PGL50G device does not have the HSST shown in the figure

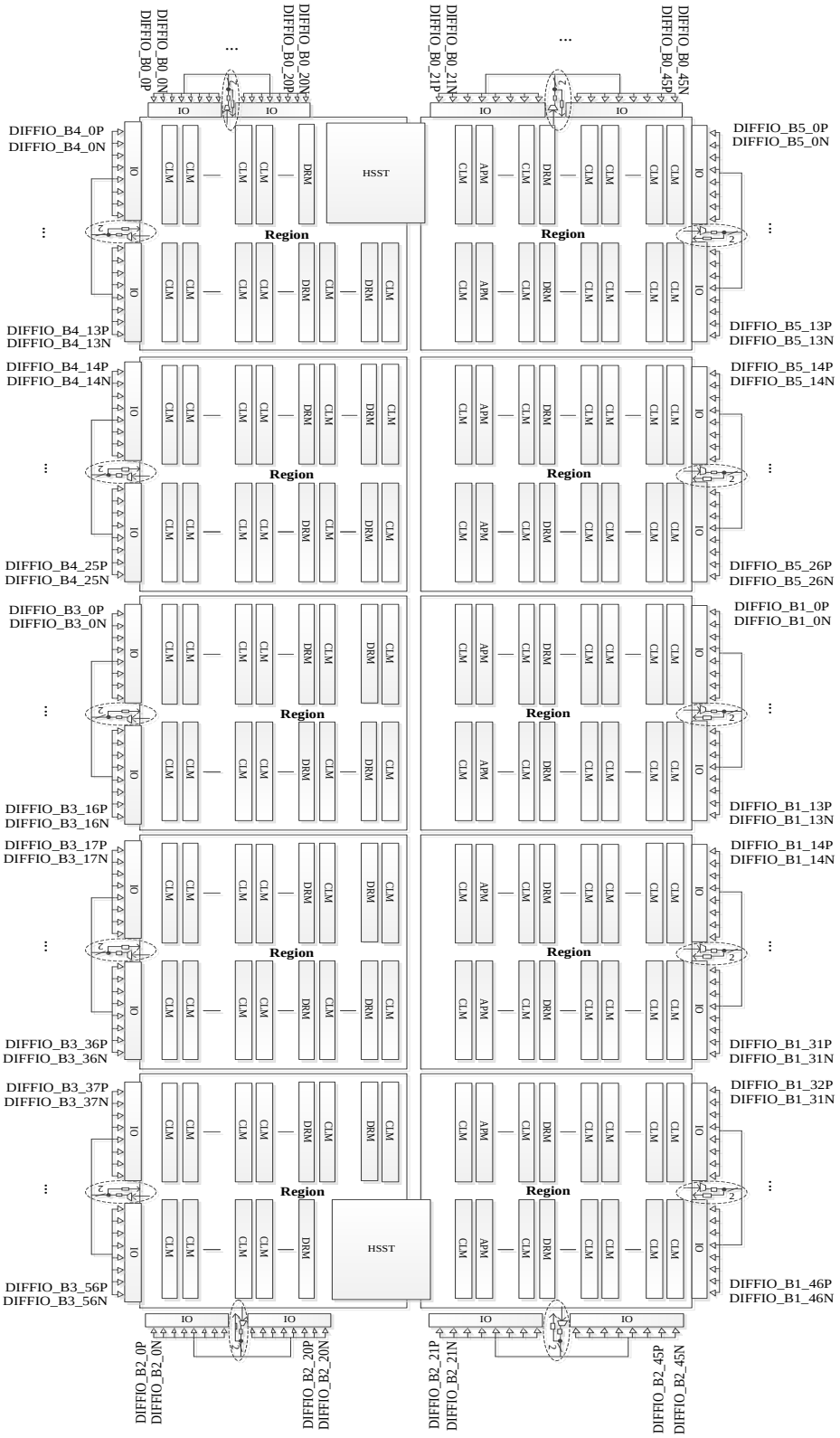

Figure 2-24 Diagram of the I/O Clock Distribution for the Logos Series PGL100H

In the architectures of PGL25G, PGL50H, PGL50G, and PGL100H, the clock IO pins of the upper and lower IO BANKs cannot directly drive the regional clocks of their respective REGIONS, but

they can drive the regional clock networks through the global clock network.

Within each region, the input sources for the I/O clock include the clock input from the clock pins in the region, PLL output clocks CLKOUT0 and CLKOUT5, and internal logic signals as shown in the figure below, with specific I/O clock input sources detailed in the table below:

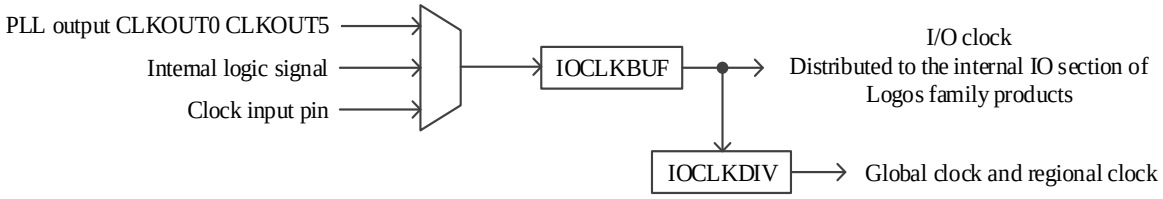

Figure 2-25 Diagram of the Paths into the I/O Clock Network

Table 2-11 Input Sources for the Logos I/O Clock Network

IO Clock Input Source	**Description**
Clock input pin	The clock input from the clock pins within each region can only serve as the input source for the I/O clock of that region, and the N-ends of PGL12G and PGL22G cannot serve as input sources for the I/O clock
PLL outputs CLKOUT0/CLKOUT5	PGL12G: PLL0's CLKOUT0/CLKOUT5 can drive the IO CLOCK of L0 and R0. PLL1's CLKOUT0/CLKOUT5 can drive the IO CLOCK of L0, R0, L1, and R1. PLL2's CLKOUT0/CLKOUT5 can drive the IO CLOCK of L0, R0, L1, and R1. PLL3's CLKOUT0/CLKOUT5 can drive the IO CLOCK in L2 and R2. PGL22G: PLL0's CLKOUT0/CLKOUT5 can drive the IO CLOCK of L0 and R0. PLL1's CLKOUT0/CLKOUT5 can drive the IO CLOCK of L0, R0, L1, and R1. PLL2's CLKOUT0/CLKOUT5 can drive the IO CLOCK of L0, R0, L1, and R1. PLL3's CLKOUT0/CLKOUT5 can drive the IO CLOCK in L1, R1, L2, and R2. PLL4's CLKOUT0/CLKOUT5 can drive the IO CLOCK in L1, R1, L2, and R2. PLL5's CLKOUT0/CLKOUT5 can drive the IO CLOCK in L2 and R2. PGL25G: PLL0's CLKOUT0/CLKOUT5 can drive the IO CLOCK of L0 and R0. PLL1's CLKOUT0/CLKOUT5 can drive the IO CLOCK of L0, R0, L1, and R1. PLL2's CLKOUT0/CLKOUT5 can drive the IO CLOCK of L0, R0, L1, and R1. PLL3's CLKOUT0/CLKOUT5 can drive the IO CLOCK in L1 and R1. PGL50H/PGL50G: PLL0's CLKOUT0/CLKOUT5 can drive the IO CLOCK in L0, R0, L1, and R1. PLL1's CLKOUT0/CLKOUT5 can drive the IO CLOCK of L0, R0, L1, and R1. PLL2's CLKOUT0/CLKOUT5 can drive the IO CLOCK in L1, R1, L2, and R2. PLL3's CLKOUT0/CLKOUT5 can drive the IO CLOCK in L1, R1, L2, and R2. PLL4's CLKOUT0/CLKOUT5 can drive the IO CLOCK in L2 and R2. PGL100H: PLL0's CLKOUT0/CLKOUT5 can drive the IO CLOCK in L0, R0, L1, and R1. PLL1's CLKOUT0/CLKOUT5 can drive the IO CLOCK of L0, R0, L1, and R1. PLL2's CLKOUT0/CLKOUT5 can drive the IO CLOCK in L1, R1, L2, and R2. PLL3's CLKOUT0/CLKOUT5 can drive the IO CLOCK in L1, R1, L2, and R2. PLL4's CLKOUT0/CLKOUT5 can drive the IO CLOCK in L2, R2, L3, and R3. PLL5's CLKOUT0/CLKOUT5 can drive the IO CLOCK in L2, R2, L3, and R3. PLL6's CLKOUT0/CLKOUT5 can drive the IO CLOCK in L3, R3, L4, and R4. PLL7's CLKOUT0/CLKOUT5 can drive the IO CLOCK in L3, R3, L4, and R4.
Internal logic signal	Internal logic signal, generally not recommended for use, as it can easily affect the quality of the input clock

The use of IOCLKBUF can be implemented by instantiating GTP_IOCLKBUF, as shown in the figure below, with port and parameter descriptions in the table below:

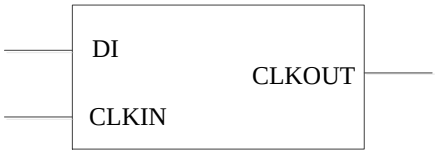

Figure 2-26 Block Diagram of GTP_IOCLKBUF

Table 2-12 Port Description of GTP_IOCLKBUF

Port Signal	**Direction**	**Description**
CLKIN	Input	Input Clock
DI	Input	Synchronous enable signal and falling edge, requires two clock cycles of input synchronization
CLKOUT	Output	Output clock

Table 2-13 Parameter Description of GTP_IOCLKBUF

Parameter	**Description**
GATE_EN	When "TRUE", the enable signal DI is valid; when "FALSE", the enable signal DI is invalid;

Instantiation of GTP_IOCLKBUF, taking Verilog instantiation as an example:

```
GTP_IOCLKBUF
    #(
    .GATE_EN    ("FALSE"      )    //FALSE; TRUE
    ) I_GTP_IOCLKBUF (
    .CLKOUT  (CLKOUT      ),
    .CLKIN         (CLIN          ),
    .DI            (DI            ));
```

When the parameter GATE_EN is "TRUE" or "FALSE", the corresponding timing diagram is as follows:

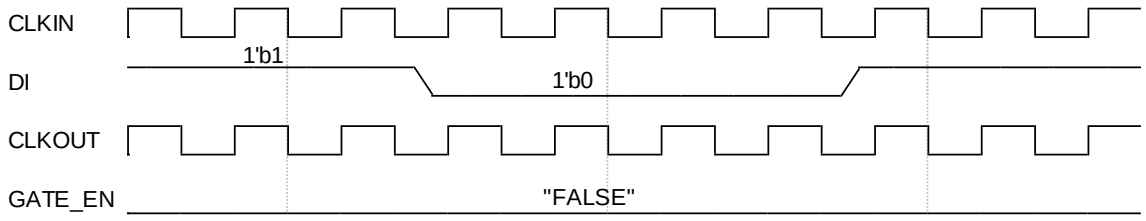

Figure 2-27 Timing Diagram of GTP_IOCLKBUF with GATEN="FALSE"

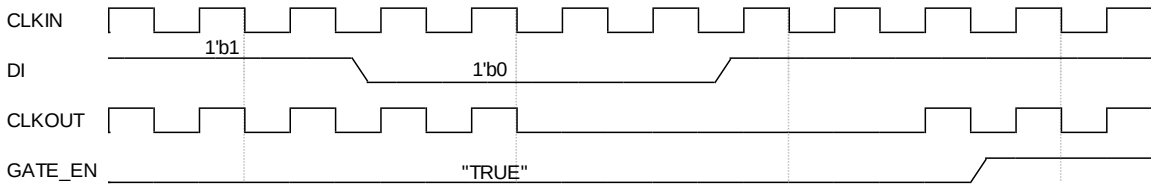

Figure 2-28 Timing Diagram of GTP_IOCLKBUF with GATEN="TRUE"

IOCLKDIV divides the clock from IOCLKBUF, and the divided clock can serve as an input source for global and regional clocks. The use of IOCLKDIV is implemented by directly instantiating the corresponding GTP in RTL, taking Verilog instantiation as an example:

```
GTP_IOCLKDIV #(
.DIV_FACTOR     ("2"          ), //"2"; "3.5"; "4"; "5";
.GRS_EN         ("FALSE"      ) //"TRUE"; "FALSE"
)I_IOCLKDIV(
.CLKIN          (CLKIN        ),
.RST_N          (RST_N        ),
.CLKDIVOUT      (CLKDIVOUT    ));
```

Table 2-14 Port Description of GTP_IOCLKDIV

Port Signal	**Direction**	**Description**
CLKIN	Input	Input Clock
RST_N	Input	Low-Active. The internal circuit of this port uses asynchronous reset and synchronous release. When the input changes from 1 to 0, the CLKDIVOUT port may output a clock glitch; when the input changes from 0 to 1, the CLKDIVOUT port will not output a clock glitch.
CLKDIVOUT	Output	Divided output clock

Table 2-15 Parameter Description of GTP_IOCLKDIV

Parameter	**Description**
DIV_FACTOR	For division ratios of "2", "3.5", "4", and "5"
GRS_EN	Global enable signal, "TRUE" means the global enable signal is valid; "FALSE" means the global enable signal is invalid

2.5 PLL

The Logos series products have varying numbers of PLLs, as shown in the figure below:

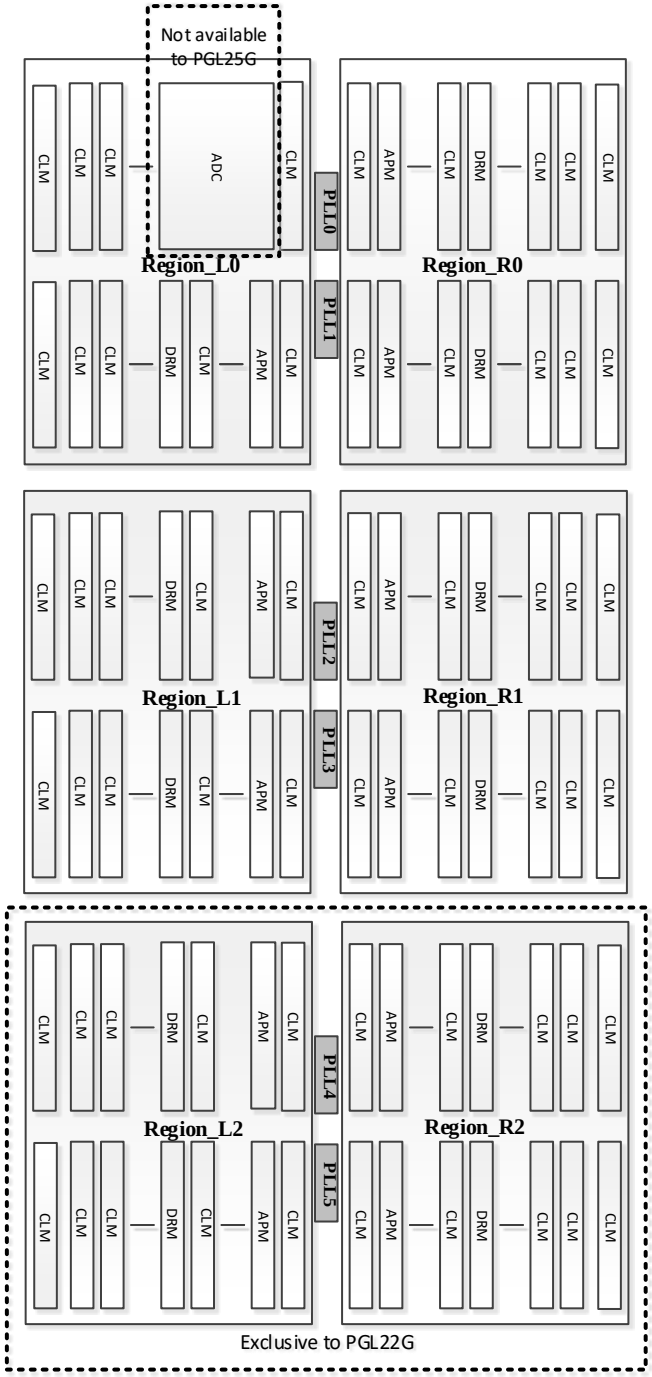

Figure 2-29 Diagram of PLL Location Distribution for Logos Series PGL12G, PGL22G, and PGL25G Devices

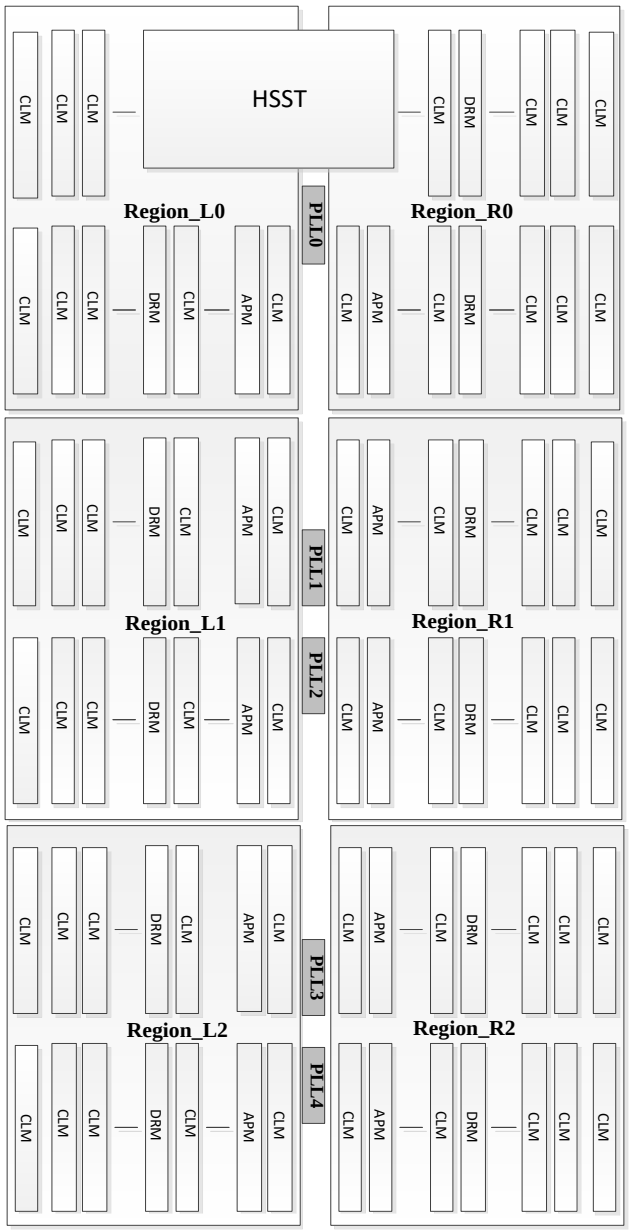

Figure 2-30 Diagram of PLL Location Distribution for Logos Series PGL50H and PGL50G Devices

Note: The PGL50G device does not have the HSST shown in the figure

Figure 2-31 Diagram of PLL Location Distribution for Logos Series PGL100H Devices

The distribution diagram of the PLL for Logos series products is shown in the figure above, with

the main characteristics of the PLL as follows:

- Frequency synthesis, phase adjustment;
- Optional input clock dynamic selection;
- Supporting two feedback modes: external feedback and internal feedback;
- Supporting dynamic configuration of PLL;
- Optional output clock gate function;
- Optional programmable phase shift;

2.5.1 Top Layer Block Diagram of PLL

The PLL model block diagram for Logos series PGL12G, PGL25G, PGL50H, PGL50G, and PGL100H products is as follows:

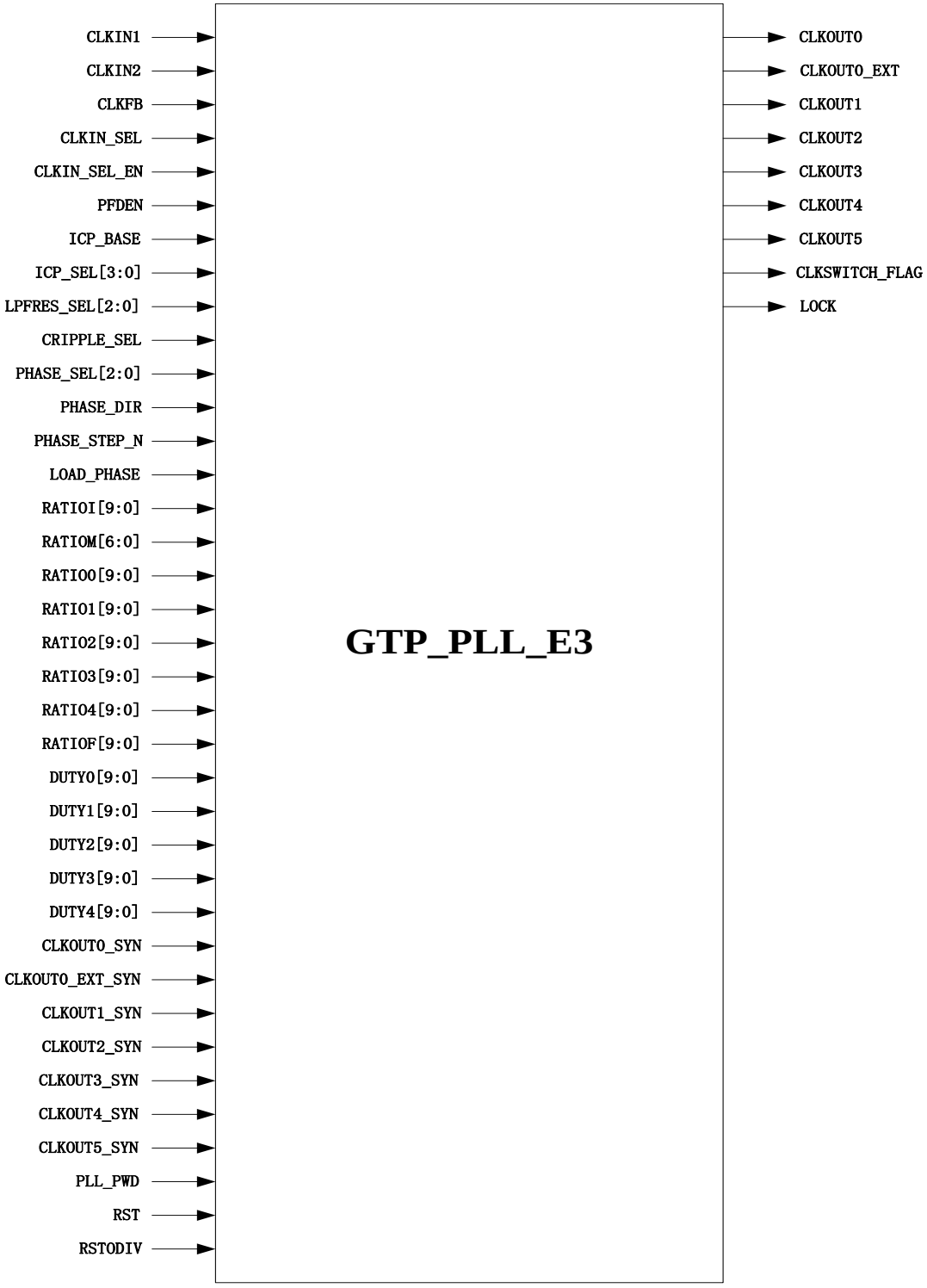

Figure 2-32 PLL Model Block Diagram for PGL12G, PGL25G, PGL50H, PGL50G, and PGL100H Devices

The PLL model block diagram for Logos series PGL22G product is shown in the figure below:

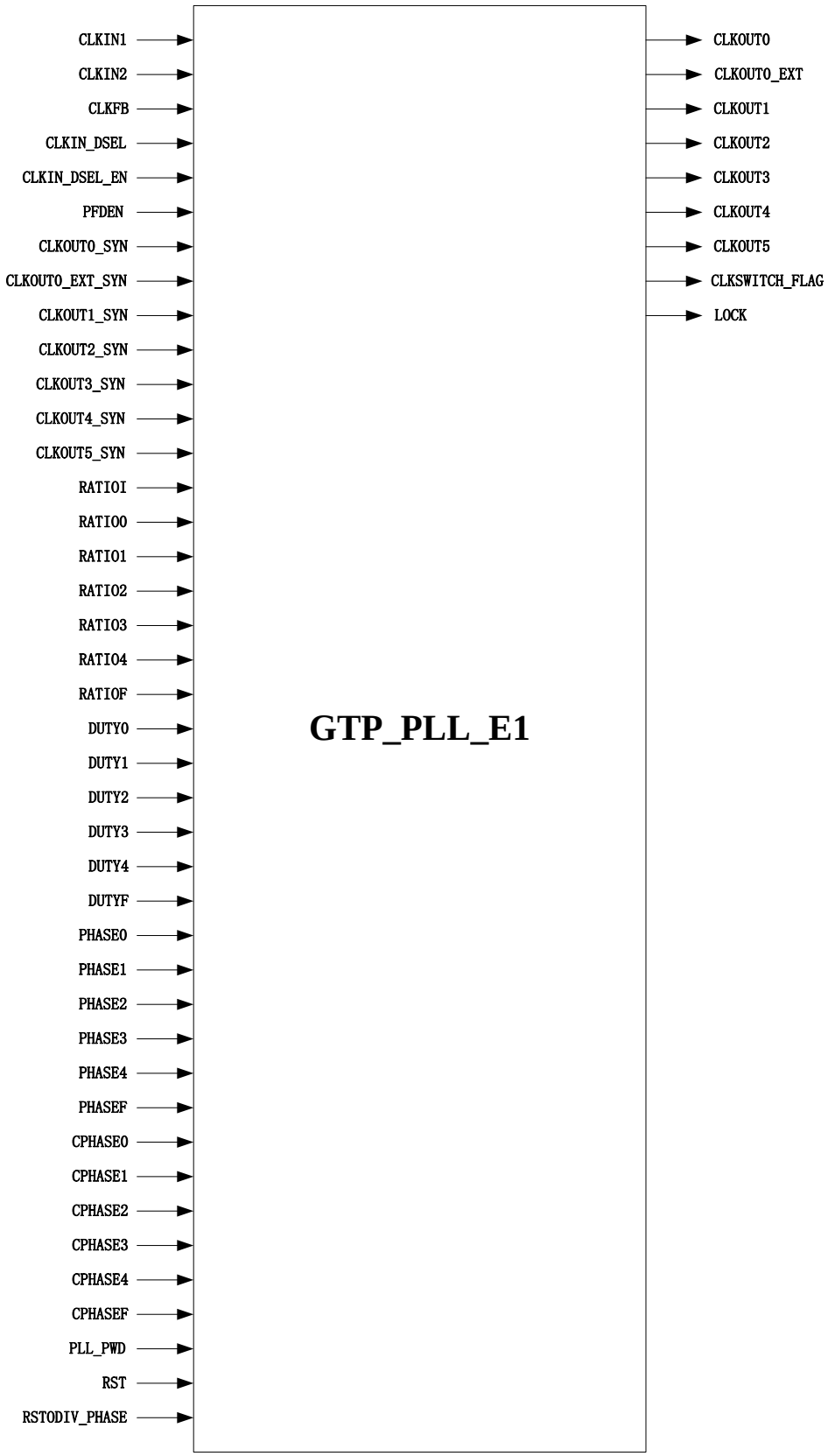

Figure 2-33 Model Block Diagram of GTP_PLL_E1 for PGL22G

2.5.2 Port List

The PLL port signals for Logos series PGL12G, PGL25G, PGL50H, PGL50G, and PGL100H products are shown in the table below:

Table 2-16 Port Description of GTP_PLL_E3

Port	Direction	Feature Description
CLKOUT0	Output	The divided output clock from ODIV0;
CLKOUT0_EXT	Output	The divided output clock from ODIV0, which shares the same source with CLKOUT0;
CLKOUT1	Output	The divided output clock from ODIV1;
CLKOUT2	Output	The divided output clock from ODIV2;
CLKOUT3	Output	The divided output clock from ODIV3;
CLKOUT4	Output	The divided output clock from ODIV4 or bypass output of the input clock;
CLKOUT5	Output	Output divider0–4, one out of five divided clocks is selected by static configuration CLKOUT5_SEL, CLKOUT5 and CLKOUT0-4 phase default misalignment;
CLKSWITCH_FLAG	Output	Clock auto-switching flag, in the automatic mode of dynamic clock selection: A value of 0 indicates CLKIN1 is selected as the PLL reference clock; A value of 1 indicates CLKIN2 is selected as the PLL reference clock;
LOCK	Output	The lock output signal of PLL; 0 indicates PLL is not locked; 1 indicates PLL is locked;
CLKIN1	Input	Input clock 1;
CLKIN2	Input	Input clock 2;
CLKFB	Input	Feedback clock;
CLKIN_SEL	Input	The selection port for input clock, asynchronous control signal. A value 0 of indicates CLKIN1 is selected; a value of 1 indicates CLKIN2 is selected;
CLKIN_SEL_EN	Input	CLKIN_SEL port enable: A value of 0 renders the CLKIN_SEL port input invalid, automatic mode; A value of 1 renders the CLKIN_SEL port input valid, with the input clock selected by CLKIN_SEL;
PFDEN	Input	PLL PFD enable, active high;
ICP_BASE	Input	The current reference setting for Charge Pump;
ICP_SEL[3:0]	Input	The current dynamic setting for Charge Pump;
LPFRES_SEL[2:0]	Input	The resistance dynamic setting for Loop Filter;
CRIPPLE_SEL	Input	The capacitance dynamic setting for Loop Filter;
PHASE_SEL[2:0]	Input	Select the corresponding PLL output clock for phase adjustment; 3'b000: Select CLKOUT0, 3'b001: Select CLKOUT1, 3'b010: Select CLKOUT2, 3'b011: Select CLKOUT3; 3'b100: Select CLKOUT4; 3'b101: Select internal feedback clock;
PHASE_DIR	Input	Select the direction for dynamic phase fine-tuning; 1'b0: lag, 1'b1: lead;
PHASE_STEP_N	Input	Dynamic phase fine-tuning adjustment toggle signal; Each toggle adjusts the output clock phase by 1/8Tvco;
LOAD_PHASE	Input	Load signal for the current phase fine-tuning value of the selected

Port	Direction	Feature Description
		channel, is a pulse signal, active high;
RATIOI[9:0]	Input	The divider ratio dynamic setting for input divider;
RATIOM[6:0]	Input	The divider ratio dynamic setting for feedback M divider;
RATIO0[9:0]	Input	The divider ratio dynamic setting for ODIV0;
RATIO1[9:0]	Input	The divider ratio dynamic setting for ODIV1;
RATIO2[9:0]	Input	The divider ratio dynamic setting for ODIV2;
RATIO3[9:0]	Input	The divider ratio dynamic setting for ODIV3;
RATIO4[9:0]	Input	The divider ratio dynamic setting for ODIV4;
RATIOF[9:0]	Input	The divider ratio dynamic setting for feedback F divider;
DUTY0[9:0]	Input	The duty cycle dynamic setting for ODIV0;
DUTY1[9:0]	Input	The duty cycle dynamic setting for ODIV1;
DUTY2[9:0]	Input	The duty cycle dynamic setting for ODIV2;
DUTY3[9:0]	Input	The duty cycle dynamic setting for ODIV3;
DUTY4[9:0]	Input	The duty cycle dynamic setting for ODIV4;
CLKOUT0_SYN	Input	Output clock CLKOUT0 GATE control, active high;
CLKOUT0_EXT_SYN	Input	Output clock CLKOUT0_EXT GATE control, active high;
CLKOUT1_SYN	Input	Output clock CLKOUT1 GATE control, active high;
CLKOUT2_SYN	Input	Output clock CLKOUT2 GATE control, active high;
CLKOUT3_SYN	Input	Output clock CLKOUT3 GATE control, active high;
CLKOUT4_SYN	Input	Output clock CLKOUT4 GATE control, active high;
CLKOUT5_SYN	Input	Output clock CLKOUT5 GATE control, active high;
PLL_PWD	Input	Power Down, active high; the PLL can be turned off to save power when not in use.
RST	Input	Global reset signal, active high;
RSTODIV	Input	Output reset signal for divider0–4 and FDIV, active high;

PLL port signals for the Logos series PGL22G product are shown in the table as follows:

Table 2-17 Port Description of GTP_PLL_E1

Port	Direction	Feature Description
CLKOUT0	Output	The divided output clock from ODIV0;
CLKOUT0_EXT	Output	The divided output clock from ODIV0, which shares the same source with CLKOUT0;
CLKOUT1	Output	The divided output clock from ODIV1;
CLKOUT2	Output	he divided output clock from ODIV2;
CLKOUT3	Output	The divided output clock from ODIV3;
CLKOUT4	Output	The divided output clock from ODIV4 or bypass output of the input clock;
CLKOUT5	Output	Output divider0–4, one out of five divided clocks is selected by static configuration CLKOUT5_SEL;

Port	Direction	Feature Description
CLKSWITCH_FLAG	Output	Clock auto-switching flag, in the automatic mode of dynamic clock selection: A value of 0 indicates CLKIN1 is selected as the PLL reference clock; A value of 1 indicates CLKIN2 is selected as the PLL reference clock;
LOCK	Output	The lock output signal of PLL; 0 indicates PLL is not locked; 1 indicates PLL is locked;
CLKIN1	Input	Input clock 1;
CLKIN2	Input	Input clock 2;
CLKFB	Input	Feedback clock;
CLKIN_DSEL	Input	Manual selection port for input clock dynamic selection;
CLKIN_DSEL_EN	Input	CLKIN_DSEL port enable: A value of 0 renders the CLKIN_DSEL port input invalid, automatic mode for dynamic selection; A value of 1 renders the CLKIN_DSEL port input valid, manual mode for dynamic selection;
PFDEN	Input	PLL PFD enable, active high;
CLKOUT0_SYN	Input	Output clock CLKOUT0 GATE control, active high;
CLKOUT0_EXT_SYN	Input	Output clock CLKOUT0_EXT GATE control, active high;
CLKOUT1_SYN	Input	Output clock CLKOUT1 GATE control, active high;
CLKOUT2_SYN	Input	Output clock CLKOUT2 GATE control, active high;
CLKOUT3_SYN	Input	Output clock CLKOUT3 GATE control, active high;
CLKOUT4_SYN	Input	Output clock CLKOUT4 GATE control, active high;
CLKOUT5_SYN	Input	Output clock CLKOUT5 GATE control, active high;
RATIOI	Input	The divider ratio dynamic setting for input divider;
RATIO0	Input	The divider ratio dynamic setting for IDIV0;
RATIO1	Input	The divider ratio dynamic setting for IDIV1;
RATIO2	Input	The divider ratio dynamic setting for IDIV2;
RATIO3	Input	The divider ratio dynamic setting for IDIV3;
RATIO4	Input	The divider ratio dynamic setting for IDIV4;
RATIOF	Input	The divider ratio dynamic setting for feedback divider;
DUTY0	Input	The duty cycle dynamic setting for IDIV0;
DUTY1	Input	The duty cycle dynamic setting for IDIV1;
DUTY2	Input	The duty cycle dynamic setting for IDIV2;
DUTY3	Input	The duty cycle dynamic setting for IDIV3;
DUTY4	Input	The duty cycle dynamic setting for IDIV4;
DUTYF	Input	The duty cycle dynamic setting for feedback divider;
PHASE0	Input	The fine phase dynamic setting for ODIV0;
PHASE1	Input	The fine phase dynamic setting for ODIV1;
PHASE2	Input	The fine phase dynamic setting for ODIV2;
PHASE3	Input	The fine phase dynamic setting for ODIV3;
PHASE4	Input	The fine phase dynamic setting for ODIV4;
PHASEF	Input	The fine phase dynamic setting for the feedback divider;
CPHASE0	Input	The coarse phase dynamic setting for ODIV0;

Port	Direction	Feature Description
CPHASE1	Input	The coarse phase dynamic setting for ODIV1
CPHASE2	Input	The coarse phase dynamic setting for ODIV2;
CPHASE3	Input	The coarse phase dynamic setting for ODIV3;
CPHASE4	Input	The coarse phase dynamic setting for ODIV4;
CPHASEF	Input	The coarse phase dynamic setting for feedback divider;
PLL_PWD	Input	Power Down, active high;
RST	Input	Global reset signal, active high;
RSTODIV_PHASE	Input	When the phase adjustment function is enabled, the output reset signal for divider0–4, active high; When the phase adjustment function is disabled, the output for divider0–4 is controlled by the RST reset signal;

2.5.3 Parameter List

PLL parameters for Logos series PGL12G, PGL25G, PGL50H, PGL50G, and PGL100H products are shown in the table below:

Table 2-18 Parameter Description of GTP_PLL_E3

Parameter Name	Valid Values	Feature Description
CLKIN_FREQ	5~625	Input Clock Frequency
PFDEN_EN	"FALSE","TRUE"	PLL PFDEN signal enable;
VCOCLK_DIV2	1’b0-1’b1	PLL VCO output clock 2 division enable;
DYNAMIC_RATIOI_EN	"FALSE","TRUE"	Dynamic control enable for input divider frequency division;
DYNAMIC_RATIOM_EN	"FALSE","TRUE"	Dynamic control enable for feedback M divider frequency division;
DYNAMIC_RATIO0_EN	"FALSE","TRUE"	Dynamic control enable for ODIV0 frequency division;
DYNAMIC_RATIO1_EN	"FALSE","TRUE"	Dynamic control enable for ODIV1 frequency division;
DYNAMIC_RATIO2_EN	"FALSE","TRUE"	Dynamic control enable for ODIV2 frequency division;
DYNAMIC_RATIO3_EN	"FALSE","TRUE"	Dynamic control enable for ODIV3 frequency division;
DYNAMIC_RATIO4_EN	"FALSE","TRUE"	Dynamic control enable for ODIV4 frequency division;
DYNAMIC_RATIOF_EN	"FALSE","TRUE"	Dynamic control enable for feedback F divider frequency division;
STATIC_RATIOI	1~512	Static setting for input divider frequency division;
STATIC_RATIOM	1~64	Static setting for feedback M divider frequency division;
STATIC_RATIO0	1~512	Static setting for ODIV0 frequency division;
STATIC_RATIO1	1~512	Static setting for ODIV1 frequency division;
STATIC_RATIO2	1~512	Static setting for ODIV2 frequency division;

Parameter Name	Valid Values	Feature Description
STATIC_RATIO3	1~512	Static setting for ODIV3 frequency division;
STATIC_RATIO4	1~512	Static setting for ODIV4frequency division;
STATIC_RATIOF	1~512	Static setting for feedback F divider frequency division;
DYNAMIC_DUTY0_EN	"FALSE","TRUE"	Dynamic control enable for ODIV0 duty;
DYNAMIC_DUTY1_EN	"FALSE","TRUE"	Dynamic control enable for ODIV1 duty;
DYNAMIC_DUTY2_EN	"FALSE","TRUE"	Dynamic control enable for ODIV2 duty;
DYNAMIC_DUTY3_EN	"FALSE","TRUE"	Dynamic control enable for ODIV3 duty;
DYNAMIC_DUTY4_EN	"FALSE","TRUE"	Dynamic control enable for ODIV4 duty;
STATIC_DUTY0	2~1022	The duty static setting for ODIV0;
STATIC_DUTY1	2~1022	The duty static setting for ODIV1;
STATIC_DUTY2	2~1022	The duty static setting for ODIV2;
STATIC_DUTY3	2~1022	The duty static setting for ODIV3;
STATIC_DUTY4	2~1022	The duty static setting for ODIV4;
STATIC_PHASE0	0~7	The fine phase static setting for ODIV0;
STATIC_PHASE1	0~7	The fine phase static setting for ODIV1;
STATIC_PHASE2	0~7	The fine phase static setting for ODIV2;
STATIC_PHASE3	0~7	The fine phase static setting for ODIV3;
STATIC_PHASE4	0~7	The fine phase static setting for ODIV4;
STATIC_PHASEF	0~7	The fine phase static setting for feedback divider;
STATIC_CPHASE0	0~511	The coarse phase static setting for ODIV0;
STATIC_CPHASE1	0~511	The coarse phase static setting for ODIV1;
STATIC_CPHASE2	0~511	The coarse phase static setting for ODIV2;
STATIC_CPHASE3	0~511	The coarse phase static setting for ODIV3;
STATIC_CPHASE4	0~511	The coarse phase static setting for ODIV4;
STATIC_CPHASEF	0~511	The coarse phase static setting for feedback divider;
CLK_CAS1_EN	"FALSE","TRUE"	ODIV1 clock cascade enable;
CLK_CAS2_EN	"FALSE","TRUE"	ODIV2 clock cascade enable;
CLK_CAS3_EN	"FALSE","TRUE"	ODIV3 clock cascade enable;
CLK_CAS4_EN	"FALSE","TRUE"	ODIV4 clock cascade enable;
CLKOUT5_SEL	0~4	Output clock CLKOUT5 selection setting;
CLKIN_BYPASS_EN	"FALSE","TRUE"	Input clock bypass enable;
CLKOUT0_SYN_EN	"FALSE","TRUE"	CLKOUT0_SYN port enable;
CLKOUT0_EXT_SYN_EN	"FALSE","TRUE"	CLKOUT0_EXT_SYN port enable;
CLKOUT1_SYN_EN	"FALSE","TRUE"	CLKOUT1_SYN port enable;
CLKOUT2_SYN_EN	"FALSE","TRUE"	CLKOUT2_SYN port enable;

Parameter Name	Valid Values	Feature Description
CLKOUT3_SYN_EN	"FALSE","TRUE"	CLKOUT3_SYN port enable;
CLKOUT4_SYN_EN	"FALSE","TRUE"	CLKOUT4_SYN port enable;
CLKOUT5_SYN_EN	"FALSE","TRUE"	CLKOUT5_SYN port enable;
INTERNAL_FB	"DISABLE","ENABLE"	Internal feedback divider selection setting;
EXTERNAL_FB	"CLKOUT0","CLKOUT1" "CLKOUT2","CLKOUT3" "CLKOUT4","DISABLE"	External feedback divider selection setting;
DYNAMIC_LOOP_EN	"FALSE","TRUE"	PLL loop bandwidth parameter dynamic enable;
LOOP_MAPPING_EN	"FALSE","TRUE"	PLL loop bandwidth parameter automatic mapping enable;
BANDWIDTH	"LOW", "HIGH" "OPTIMIZED"	Bandwidth selection settings;

The PLL parameters for the Logos series PGL22G product are shown in the table below:

Table 2-19 Parameter Description of GTP_PLL_E1

Parameter Name	Valid Values	Feature Description
DYNAMIC_CLKIN_EN	"FALSE","TRUE"	Input clock dynamic selection enable;
CLKIN_SSEL	1’b0-1’b1	Input clock static selection setting;
DYNAMIC_RATIOI_EN	"FALSE","TRUE"	Dynamic control enable for input divider frequency division;
STATIC_RATIOI	1~512	Static setting for input divider frequency division;
PFDEN_EN	"FALSE","TRUE"	PLL PFDEN signal setting
VCOCLK_DIV2	1’b0-1’b1	PLL VCO output clock 2 division enable;
DYNAMIC_RATIO0_EN	"FALSE","TRUE"	Dynamic control enable for ODIV0 frequency division;
DYNAMIC_RATIO1_EN	"FALSE","TRUE"	Dynamic control enable for ODIV1 frequency division;
DYNAMIC_RATIO2_EN	"FALSE","TRUE"	Dynamic control enable for ODIV2 frequency division;
DYNAMIC_RATIO3_EN	"FALSE","TRUE"	Dynamic control enable for ODIV3 frequency division;
DYNAMIC_RATIO4_EN	"FALSE","TRUE"	Dynamic control enable for ODIV4 frequency division;
DYNAMIC_RATIOF_EN	"FALSE","TRUE"	Dynamic control enable for feedback divider frequency division;
STATIC_RATIO0	1~512	Static setting for ODIV0 frequency division;
STATIC_RATIO1	1~512	Static setting for ODIV1 frequency division;
STATIC_RATIO2	1~512	Static setting for ODIV2 frequency division;
STATIC_RATIO3	1~512	Static setting for ODIV3 frequency division;
STATIC_RATIO4	1~512	Static setting for ODIV4 frequency division;
STATIC_RATIOF	1~512	Static setting for feedback divider frequency division;
DYNAMIC_DUTY0_EN	"FALSE","TRUE"	Dynamic control enable for ODIV0 duty;
DYNAMIC_DUTY1_EN	"FALSE","TRUE"	Dynamic control enable for ODIV1 duty;
DYNAMIC_DUTY2_EN	"FALSE","TRUE"	Dynamic control enable for ODIV2 duty;

Parameter Name	Valid Values	Feature Description
DYNAMIC_DUTY3_EN	"FALSE","TRUE"	Dynamic control enable for ODIV3 duty;
DYNAMIC_DUTY4_EN	"FALSE","TRUE"	Dynamic control enable for ODIV4 duty;
DYNAMIC_DUTYF_EN	"FALSE","TRUE"	Dynamic control enable for feedback divider duty;
STATIC_DUTY0	1~1022	The duty static setting for ODIV0;
STATIC_DUTY1	1~1022	The duty static setting for ODIV1;
STATIC_DUTY2	1~1022	The duty static setting for ODIV2;
STATIC_DUTY3	1~1022	The duty static setting for ODIV3;
STATIC_DUTY4	1~1022	The duty static setting for ODIV4;
STATIC_DUTYF	1~1022	The duty static setting for feedback divider;
PHASE_ADJUST0_EN	"FALSE","TRUE"	The phase adjustment enable for ODIV0;
PHASE_ADJUST1_EN	"FALSE","TRUE"	The phase adjustment enable for ODIV1;
PHASE_ADJUST2_EN	"FALSE","TRUE"	The phase adjustment enable for ODIV2;
PHASE_ADJUST3_EN	"FALSE","TRUE"	The phase adjustment enable for ODIV3;
PHASE_ADJUST4_EN	"FALSE","TRUE"	The phase adjustment enable for ODIV4;
DYNAMIC_PHASE0_EN	"FALSE","TRUE"	Dynamic control enable for ODIV0 phase;
DYNAMIC_PHASE1_EN	"FALSE","TRUE"	Dynamic control enable for ODIV1 phase;
DYNAMIC_PHASE2_EN	"FALSE","TRUE"	Dynamic control enable for ODIV2 phase;
DYNAMIC_PHASE3_EN	"FALSE","TRUE"	Dynamic control enable for ODIV3 phase;
DYNAMIC_PHASE4_EN	"FALSE","TRUE"	Dynamic control enable for ODIV4 phase;
DYNAMIC_PHASEF_EN	"FALSE","TRUE"	Dynamic control enable for feedback divider phase;
STATIC_PHASE0	0~7	The fine phase static setting for ODIV0;
STATIC_PHASE1	0~7	The fine phase static setting for ODIV1;
STATIC_PHASE2	0~7	The fine phase static setting for ODIV2;
STATIC_PHASE3	0~7	The fine phase static setting for ODIV3;
STATIC_PHASE4	0~7	The fine phase static setting for ODIV4;
STATIC_PHASEF	0~7	The fine phase static setting for feedback divider;
STATIC_CPHASE0	2~513	The coarse phase static setting for ODIV0;
STATIC_CPHASE1	2~513	The coarse phase static setting for ODIV1;
STATIC_CPHASE2	2~513	The coarse phase static setting for ODIV2;
STATIC_CPHASE3	2~513	The coarse phase static setting for ODIV3;
STATIC_CPHASE4	2~513	The coarse phase static setting for ODIV4;
STATIC_CPHASEF	2~513	The coarse phase static setting for feedback divider;
CLK_CAS0_EN	"FALSE","TRUE"	ODIV0 clock cascade enable;
CLK_CAS1_EN	"FALSE","TRUE"	ODIV1 clock cascade enable;
CLK_CAS2_EN	"FALSE","TRUE"	ODIV2 clock cascade enable;
CLK_CAS3_EN	"FALSE","TRUE"	ODIV3 clock cascade enable;
CLK_CAS4_EN	"FALSE","TRUE"	ODIV4 clock cascade enable;
INTERNAL_FB	"FALSE","TRUE"	Internal feedback divider selection setting;

Parameter Name	Valid Values	Feature Description
EXTERNAL_FB	"ODIV0","ODIV1" "ODIV2","ODIV3" "ODIV4","FALSE"	External feedback divider selection setting;
BANDWIDTH	"LOW", "HIGH" "OPTIMIZED"	Bandwidth selection settings;
CLKOUT5_SEL	0~4	Output clock CLKOUT5 selection setting;
CLKIN_BYPASS_EN	"FALSE","TRUE"	Input clock bypass enable;
CLKOUT0_SYN_EN	"FALSE","TRUE"	CLKOUT0_SYN port enable;
CLKOUT0_EXT_SYN_EN	"FALSE","TRUE"	CLKOUT0_EXT_SYN port enable;
CLKOUT1_SYN_EN	"FALSE","TRUE"	CLKOUT1_SYN port enable;
CLKOUT2_SYN_EN	"FALSE","TRUE"	CLKOUT2_SYN port enable;
CLKOUT3_SYN_EN	"FALSE","TRUE"	CLKOUT3_SYN port enable;
CLKOUT4_SYN_EN	"FALSE","TRUE"	CLKOUT4_SYN port enable;
CLKOUT5_SYN_EN	"FALSE","TRUE"	CLKOUT5_SYN port enable;
RST_INNER_EN	"FALSE","TRUE"	RST reset signal enable;
RSTODIV_PHASE_EN	"FALSE","TRUE"	RSTODIV_PHASE reset signal enable;

2.5.4 PLL Clock Input

PLL reference clock input sources include the input clock from clock input pins or PLL reference clock input pins, global clocks, regional clocks or I/O clocks, and signals from internal logic. Among these, the PLL reference clock input pins are highly recommended which can make the PLL getting best performance. Signals originating which from internal logic are prone to interference from other internal signals, and it is recommended that users are advised to use them with caution.

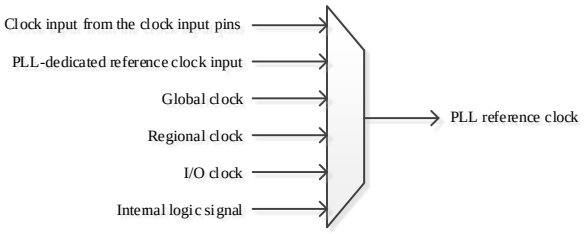

Figure 2-34 PLL Reference Clock Selection Diagram

The PLL feedback clock input sources can be divided into two types: PLL internal feedback and PLL external feedback. And the PLL internal feedback clock source consists of the dedicated internal clock.

For the PGL12G and PGL22G PLLs, the external feedback clock sources include clocks from clock input pins, PLL feedback clock pin input, global clocks, regional clocks, and signals from internal logic; for other device PLLs, the external feedback clock sources include clocks from clock input pins, PLL feedback clock pin input, global clocks, regional clocks, I/O clocks and signals from internal logic. Among these, signals which from internal logic are prone to interference from other

internal signals, and it is recommended that users employ the PLL dedicated feedback clock.

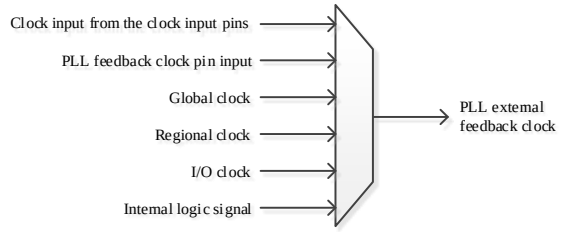

Figure 2-35 PLL External Feedback Clock Selection Diagram

The following points should be noted regarding the PLL input clock:

- If the input clock is lost and then recovered, or is unstable causing the PLL to lose lock, a reset of the PLL is required;
- In the absence of a clock source, the PLL may output an invalid clock signal which will lead the LOCK signal to become a low level. If the PLL does not output clock signal, the PLL's gate signal can be set or the PLL_PWD signal can be configured to 1.

2.5.5 Input Clock Switch

In clock automatic switching mode, the PLL has two clock inputs (CLKIN1 and CLKIN2). In automatic mode, CLKIN1 is selected by default as the input; if the CLKIN1 clock no longer toggles, it will automatically switch to CLKIN2; in manual mode, users can switch between CLKIN1 and CLKIN2 using logic. Note that the frequency difference between the two clock inputs during automatic switching should not exceed 5%, and the maximum frequency for automatic switching is 320MHz. The timing diagram of clock automatic switching is shown below:

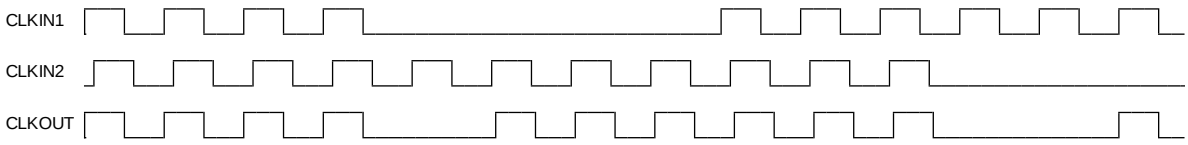

Figure 2-36 Automatic Clock Switching Timing

During clock switching, the lock signal is pulled low, and after the PLL relocks, it needs to be reset.

2.5.6 PLL Output Clock Frequency Programming

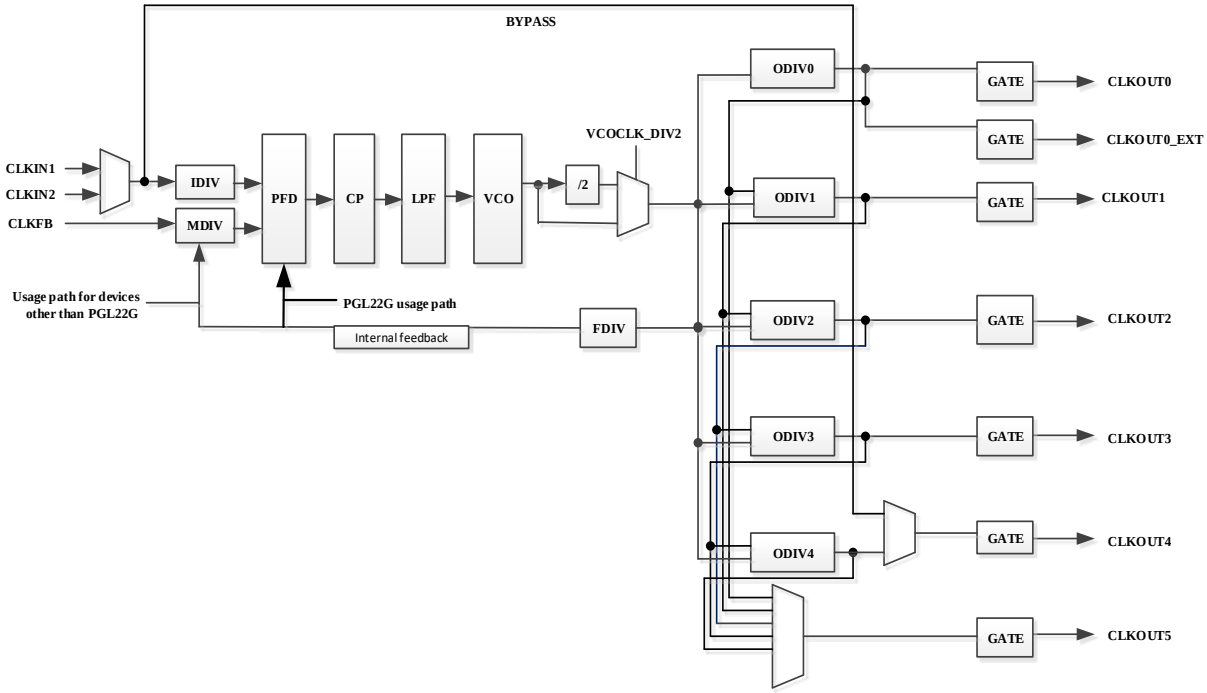

Figure 2-37 Diagram of PLL Structure in Logos Series Products

One of the main functions of the PLL is frequency synthesis. As shown in the figure above, after the input clock and feedback clock pass through the Phase Frequency Detector (PFD) and Charge Pump (CP), then through the Loop Filter (LPF) and the Voltage Controlled Oscillator (VCO). When the parameter "VCOCLK_DIV2" is 0, N=1; when it is 1, N=2. The frequency of the VCO and the output clock frequency are calculated as follows:

Internal feedback:

$$F_{VCO}= F_{ref}*F_{DIV}*M_{DIV}*N/I_{DIV}$$

$$F_{clkout0\sim4}= F_{ref}*F_{DIV}*M_{DIV}/(I_{DIV}*O_{DIVx})$$

External feedback:

$$F_{VCO}= F_{ref}*M_{DIV}*O_{DIVF}*N/I_{DIV}$$

$$F_{clkout0\sim4}= F_{ref}* M_{DIV}*O_{DIVF}/(I_{DIV}*O_{DIVx})$$

Table 2-20 Available Range of PLL Input and Output Frequencies and Dividers

Parameter	**Description**
F_{VCO}	VCO frequency
$F_{clkout0\sim4}$	The frequency of the PLL output clocks CLKOUT0–4
F_{ref}	Frequency of the reference input clock
F_{DIV}	The division ratio of the divider F_{DIV} on the feedback path, only on the internal feedback path
M_{DIV}	The division ratio of the divider M_{DIV} on the feedback path
I_{DIV}	The division ratio of the input divider I_{DIV}

Parameter	Description
O_{DIVx}	The division ratio of the output divider O_{DIVx}, where x is from 0 to 4
O_{DIVF}	The output divider ratio on the feedback path is one of O_{DIVx}

2.5.7 PLL Phase Shift Function

- Phase adjustment includes two methods: fine-tuning and coarse-tuning. Fine-tuning has two control modes: static configuration and dynamic adjustment, while coarse-tuning has only static configuration. The final phase adjustment is determined by both fine-tuning and coarse-tuning.

Phase adjustment method:

- **Phase fine-tuning**

  With respect to the input VCO clock, the minimum step for phase fine-tuning of the output clocks CLKOUT0/1/2/3/4 is $T_{VCO}/8$, with an adjustment range of 0–7/8Tvco.

- **Phase coarse-tuning**

  With respect to the input VCO clock, when VCOCLK_DIV2 = 1'b0, the minimum step for phase coarse-tuning of the output clocks CLKOUT0/1/2/3/4 is T_{VCO}, with an adjustment range of $[0\sim O_{DIVX}-1]*T_{VCO}$; when VCOCLK_DIV2 = 1'b1, the minimum step for phase coarse-tuning of the output clocks CLKOUT0/1/2/3/4 is $2*T_{VCO}$, with an adjustment range of $[0\sim O_{DIVX}-1]*2*T_{VCO}$.

Phase adjustment modes:

- **Static phase adjustment**

  The PLL output clock's phase shift function includes both fine-tuning and coarse-tuning methods. The static configuration for phase fine-tuning of the output clocks CLKOUT0/1/2/3/4 is controlled by parameters STATIC_PHASE0/1/2/3/4 respectively; the static configuration for phase coarse-tuning is controlled by STATIC_CPHASE0/1/2/3/4 respectively. The diagram below is a timing diagram obtained by configuring parameters according to the table below.

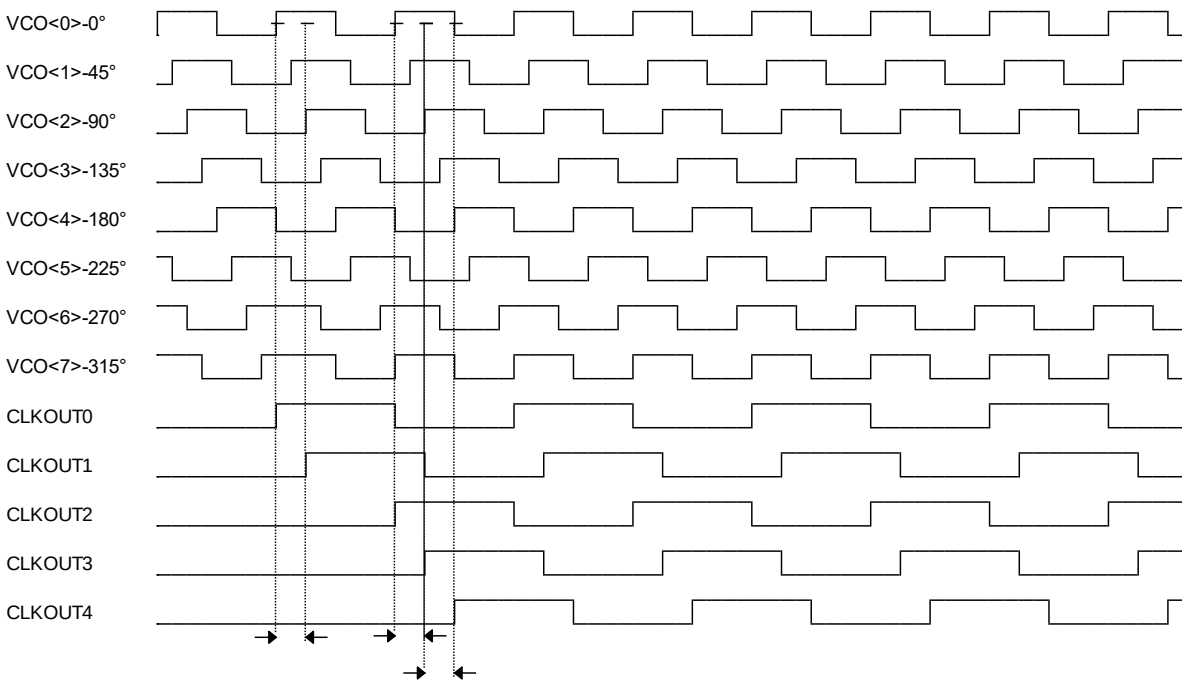

Figure 2-38 PLL Static Phase Adjustment

Table 2-21 Static Phase Adjustment Parameter Configuration

Phase Parameter	**Configuration Value**
STATIC_PHASE0	0
STATIC_PHASE1	2
STATIC_PHASE2	0
STATIC_PHASE3	2
STATIC_PHASE4	4
STATIC_CPHASE0	0
STATIC_CPHASE1	0
STATIC_CPHASE2	1
STATIC_CPHASE3	1
STATIC_CPHASE4	1
VCOCLK_DIV2	0

- **Dynamic phase adjustment**

  Logos series products support dynamic phase adjustment function; the PGL22G dynamic phase adjustment method differs from other model products.

  PGL22G dynamic phase adjustment feature:

  The PGL22G dynamic phase adjustment ports are dyn_phase0/1/2/3/4, with each corresponding to a clock output port, allowing for simultaneous dynamic phase adjustment of the clock outputs CLKOUT0/1/2/3/4;

Supports phase fine-tuning and coarse-tuning, dyn_phase[2:0] are the fine-tuning control bits with a parameter range of 0–7, and dyn_phase[12:3] are the coarse-tuning control bits with a parameter range of 2–513. Refer to the phase adjustment methods section for the minimum step and range. After phase adjustment, the PLL needs to be reset.

Dynamic phase adjustment feature of other products:

The ports for dynamic phase adjustment in other Logos series products include PHASE_SEL, PHASE_DIR, PHASE_STEP_N, and LOAD_PHASE. All the output clocks CLKOUT0/CLKOUT1/ CLKOUT2/CLKOUT3/CLKOUT4 have dynamic phase adjustment capabilities, but only one output clock can be adjusted at a time.

PHASE_SEL and PHASE_DIR must remain stable before the LOAD_PHASE signal is triggered. LOAD_PHASE must be released before triggering the PHASE_STEP_N signal. Phase adjustment is achieved by triggering PHASE_STEP_N, with each trigger adjusting the phase by one step (T_{VCO}/8). The PHASE_STEP_N signal must start from logic 1 and phase adjustment will start at the rising edge. When switching phase adjustment channels or directions, the current phase fine-tuning value of the selected channel must be loaded with the LOAD_PHASE signal. The timing requirements are shown in the figure below:

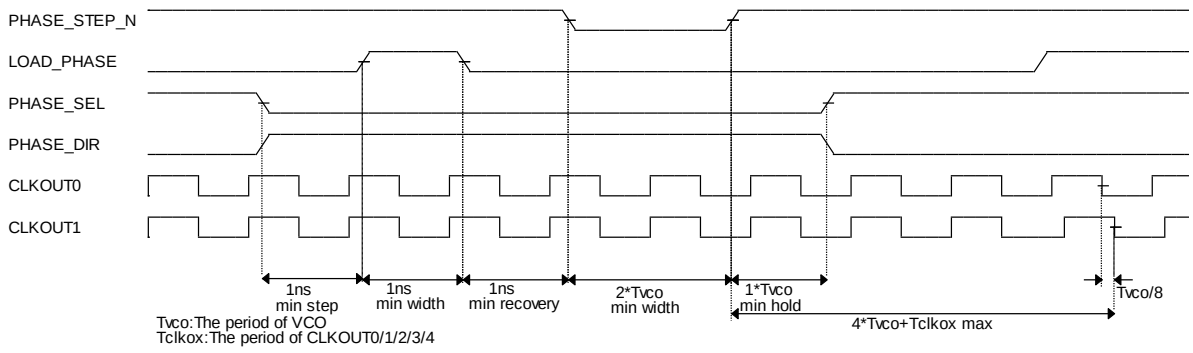

Figure 2-39 Timing Requirements of Dynamic Phase Fine-Tuning

2.5.8 PLL Programmable Duty Cycle

The PLL supports a programmable duty cycle with a minimum step of 50%/$ODIV_X$, where $ODIV_X$ is the division factor of the output divider. The duty is the value configured for the duty cycle can come from static parameters STATIC_DUTY0, STATIC_DUTY1, STATIC_DUTY2, STATIC_DUTY3, STATIC_DUTY4, or from ports DUTY0, DUTY1, DUTY2, DUTY3, DUTY0. The valid range for the Duty value is from 2 to 1022 and is also limited by the division ratio of the output divider.

duty cycle = (50%/odiv)*duty

The setting value of duty is limited by the $ODIV_X$ value (division), as expressed below,

$ODIV_X$>1 2=< duty <= 2* $ODIV_X$ -2.

$ODIV_X$=1 duty is invalid and does not function. The default output is 50%.

2.5.9 PLL Output Clock Gate Function

Before the clock CLKOUT0/0_EXT/1/2/3/4/5 outputs, it passes through the GATE module, which is controlled by static parameters.

When CLKOUT0/0_EXT/1/2/3/4/5_SYN_EN = "TRUE", the clock GATE function is enabled;

When CLKOUT0/0_EXT/1/2/3/4_SYN_EN = "FALSE", the clock GATE function is disabled, and the clock passes through directly;

After the GATE function of the clock CLKOUT0/0_EXT/1/2/3/4 is enabled, the clock output is controlled by the corresponding dynamic control signal. Taking CLKOUT0 as an example, the timing relationship is as follows:

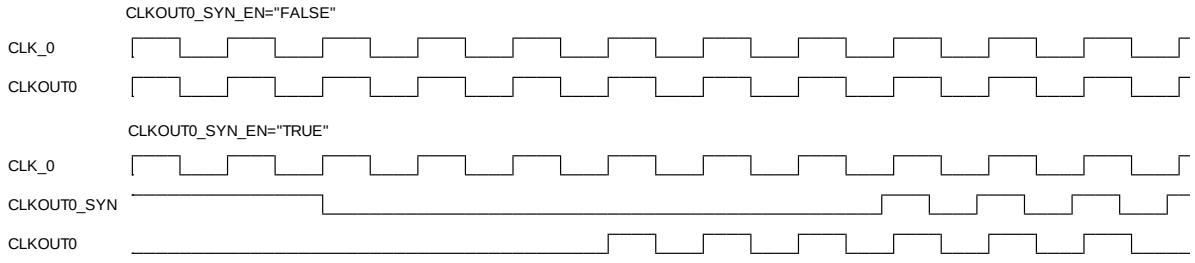

Figure 2-40 The Timing Diagram of Output Clock GATE

2.5.10 Divider Output Cascading

The PLL static configuration divider cascading schematic is as shown below, CLK_CAS_EN (where x is 1, 2, 3, or 4) controls the clock selection for divider 0–4. When statically configured to "TRUE", it selects the cascaded clock, and when "FALSE", it selects the VCO output clock.

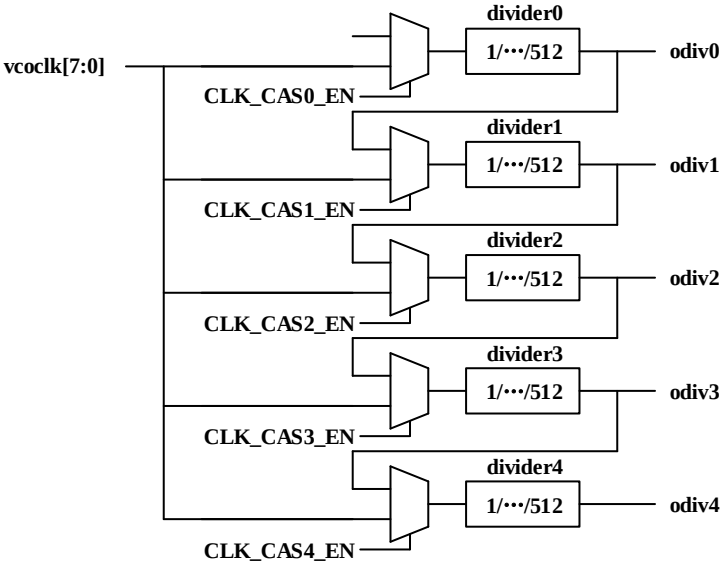

Figure 2-41 PLL Divider Output Cascading

2.6 Internal Oscillator (OSC)

The Logos series chips provide an internal oscillator (OSC), which can be used as a clock source, but with poor precision. The clock output from the internal oscillator can be used as a global clock input source, but not as a regional clock or I/O clock input source. The OSC can be instantiated directly as GTP_OSC_E3, with its structural diagram shown below, the port and parameter descriptions are in the table below:

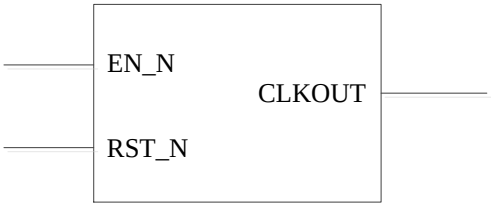

Figure 2-42 Block Diagram of GTP_OSC_E3

Table 2-22 Port Description of GTP_OSC_E3

Port Name	Types	Description
CLKOUT	Output	Output clock, frequency can be changed according to the parameter value settings.
EN_N	Input	OSC shutdown signal, high level turns off OSC, low level turns on OSC.
RST_N	Input	OSC reset signal, active low

Table 2-23 Parameter Description of GTP_OSC_E3

Parameter	**Description**
CLK_DIV	Clock division ratio setting, valid values are 0–127

When CLK_DIV is set to 0, a 128 division is achieved, and the corresponding relationships for other values are as shown in the table below:

Table 2-24 Clock Frequency Configuration

CLK_DIV	**CLKOUT(MHz)**
0	200/128
1	200/1
2	200/2
3	200/3
…	…
125	200/125
126	200/126
127	200/127

Instantiation of GTP_OSC_E3, taking Verilog instantiation as an example:

```
GTP_ OSC_E3
#(
    .CLK_DIV        (2              )//0-127
    ) u_OSC_E3 (
    .CLKOUT         (CLKOUT         ),
    .RST_N          (RST_N          ),
    .EN_N           (EN_N           ));
```

When the parameter CLK_DIV is set to 2, the timing diagram is shown in the figure below:

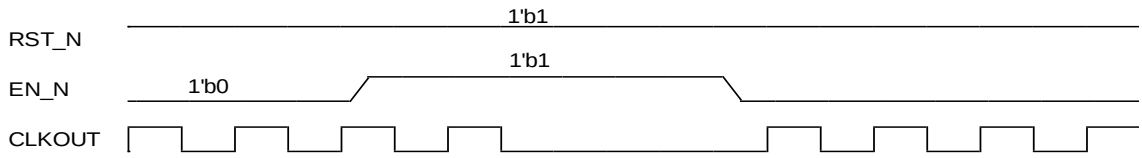

Figure 2-43 Timing Diagram of GTP_OSC_E3

Chapter 3 Appendix

Appendix primarily describes a solution to the issue of clock phase misalignment when the PGL22G PLL uses a feedback clock from the dedicated input pin for the FPGA feedback clock (external feedback).

Issue description:

When using external feedback with PGL22G, the PLL outputs multiple clocks, and the phase of the output clocks (other output clock expect the feedback clock) is not fixed after each reset.

PGL22G is one of the earliest products in the Logos series, designed to only support phase synchronization among all output dividers outside the loop. There is no phase bonding between the feedback divider inside the PLL loop and the output dividers outside; since the synchronous reset signals for dividers outside the loop and dividers inside the loop come from different signal sources that lead to phase synchronization cannot be achieved. For example, if a developer sets CLKOUT0 as the external feedback clock in the IP Compiler, expecting to use ODIV0 as the feedback divider for source synchronization, then the phase between CLKOUT1 and CLKOUT0 cannot be synchronized. As explained above, ODIV0 is inside the loop and ODIV1 is outside, with their reset signals coming from different sources.

Solutions for using external feedback mode:

If phase bonding is required between dividers inside the loop and dividers outside the loop, then the reset source for the feedback divider must be chosen to be consistent with that of the external loop dividers. The following solution can be employed: When instantiating PGL22G PLL using IP Compiler, set CLKOUT2 as the external feedback clock, so both ODIV0 and ODIV1 are considered as dividers outside the loop; when using the PLL, the external feedback clock input is actually still connected to CLKOUT0. This achieves a common source for the reset signals of ODIV0 and ODIV1, thereby accomplishing phase synchronization.

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