FPGA implementation of Digital Down Converter using CORDIC algorithm

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ABSTRACT

In radio receivers, Digital Down Converters (DDC) are used to translate the signal from Intermediate Frequency level to baseband. It also decimates the oversampled signal to a lower sample rate, eliminating the need of a high end digital signal processors. In this paper we have implemented architecture for DDC employing CORDIC algorithm, which down converts an IF signal of 70MHz (3G) to 200 KHz baseband GSM signal, with an SFDR greater than 100dB. The implemented architecture reduces the hardware resource requirements by 15 percent when compared with other architecture available in the literature due to elimination of explicit multipliers and a quadrature phase shifter for mixing.

Keywords: CORDIC, Digital Down Converter, FPGA, CIC filter

1. INTRODUCTION

Software Defined Radio (SDR) Communication systems are driving analog to digital converters (ADCs) to move as close as possible towards the antenna. DDC takes band limited digitized RF/IF signal which is sampled at a very high rate as its input, mixes to obtain low frequency signal and decimates the sample rate without losing information. The frequency down conversion task is computationally intensive. To illustrate, if the IF frequency is 70MHz, frequency down conversion on two channels, one in-phase and one quadrature channel, needs around 3000MIPS. This requires two high end DSP processors on receive path which is hardware inefficient solution. FPGAs, not only offer efficiency in hardware but they also offer design flexibility, high precision computing and performance improvement[2].

The COordinate Rotation DIgital Computer (CORDIC) is a fast technique, first developed by J.E. Volder in 1959, for computing trigonometric functions using shift and add operations and conversion from rectangular to polar conversion[3]. Later in 1971 it was generalized by J.S. Walther to circular, linear and hyperbolic coordinate systems to compute multiplication, division, logarithmic and exponential functions apart from trigonometric computations[4]. CORDIC algorithm can be realized using bit serial architecture and word parallel/pipelined architecture. The choice of architecture depends on the required throughput, frequency of operation of a target application, area constraints etc.[5].

The implementation of DDC requires quadrature waveforms to be generated. There are two methods for generation of quadrature waveforms viz., look up table method and CORDIC method. In look up table method, ROM of size MXN is used, where M represents the number of bits used to represent phase resolution and N represents the amplitude resolution. The locations of the ROM have to be filled with the required cosine/sine values and they are accessed with the phase address (M). The disadvantages of this method are exponential increase in the size of ROM with increase in phase/amplitude resolution and either needs a phase shifter or another ROM to generate the quadrature waveform. A phase shifter introduces delay distortions where as ROM occupies lot of area on the chip. On the other hand, CORDIC implementation overcomes the above disadvantages.

In this present work, we propose a prototype architecture for DDC based on CORDIC algorithm suitable for down conversion of a GSM IF signal to a baseband signal of 200 KHz. We have employed pipelined CORDIC architecture to implement the proposed architecture on VIRTEX-4 XC4vSX35-10ff668 device operating at a maximum operating frequency of 100MHz. The CORDIC architecture implemented is configured to produce quadrature waveforms, with a frequency of 35MHz [6].

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2. DIGITAL DOWN CONVERTER

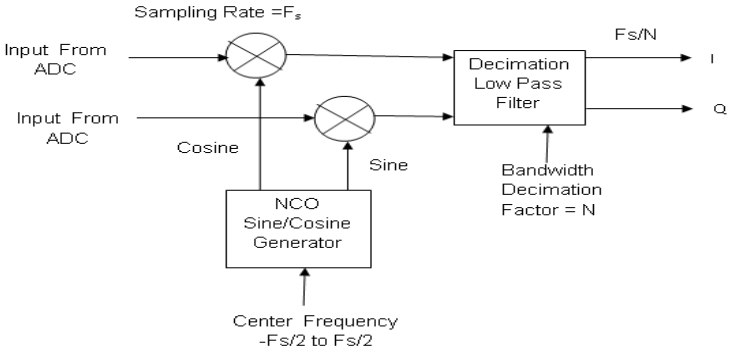
The basic architecture of DDC shown in figure 1 contains on chip Numerically Controlled Oscillators (NCO). NCOs generate precise quadrature waveforms, mixes with the incoming IF signal producing the sum and difference components. This mixer translates the intermediate frequency signal to the baseband. Frequency translation in frequency domain is given by equation (1). The difference component is filtered out and then decimated.

$$\cos\omega_c t\, x(t) \leftrightarrow 0.5\left[X(\omega-\omega_c)+X(\omega+\omega_c)\right]$$

$$\sin\omega_c t\, x(t) \leftrightarrow j0.5\left[X(\omega-\omega_c)+X(\omega+\omega_c)\right] \qquad (1)$$

where x (t) is the input signal, X (ω) is its Fourier transform and ω_c is the carrier frequency of the signal.

Figure 1: Block diagram of Digital Down Converter



2.2 CORDIC algorithm

CORDIC algorithm was first developed by Volder[3] in 1959 to compute the value of trigonometric functions iteratively using shift and add/subtract operations, which is suitable for VLSI implementation due to its regular structure. The iteration equations of radix-2 CORDIC algorithm for vector rotation of coordinates in Cartesian coordinate system is given as :

$$\begin{aligned} x_{i+1} &= x_i - \sigma_i y_i 2^{-i} \\ y_{i+1} &= y_i + \sigma_i y_i 2^{-i} \\ z_{i+1} &= z_i - \sigma_i \tan^{-1}(2^{-i}) \end{aligned} \qquad (2)$$

where σ_i represents the direction of rotation in each iteration and $\tan^{-1}(2^{-i})$ is an elementary rotation angle. The realization of above equations increases the length of the vector, to preserve the norm of the vector the final coordinates must be multiplied by K^{-1}, the scale factor.

$$K^{-1} = \prod_{i=1}^{n} \sqrt{1+\sigma_i^2 2^{-2i}} \qquad (3)$$

As the scale factor is constant in radix-2 CORDIC algorithm, scale factor compensation can be achieved with constant multipliers using canonic signed digit representation. However, for implementation of DDC this scale factor can be adjusted in the automatic gain control unit of the receiver.

2.3 Digital Filters

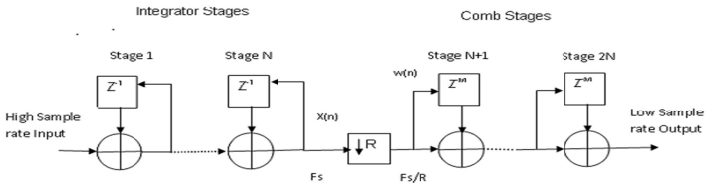
Among digital filters, Cascaded integrator comb filters are a special class of multiplier less digital FIR filters[9]. These filters are highly suitable for frequency down conversion or up conversion due to their multiplier less architectures. CIC

filters have N integrators operating at a high sampling rate and the same no of differentiators operating at a lower sampling rate as shown in figure 2. Equation (4) represents the transfer function of CIC filter. Though the CIC filter structure is simple in design, integrators are highly instable due to bit growth. These filters have a large pass band droop which has to be compensated. Hence a compensation FIR filter has to be designed to restore the pass band droop in accordance with the required specification. Also another low pass FIR filter is used to attain the required attenuation characteristics.

$$H(z)=\left\{\frac{1-z^{-RM}}{1-z^{-1}}\right\}^{N} \tag{4}$$

Where R = Decimation Factor, M = Differential delay (1 or 2), N = No of Integrators/Combs

Figure 2 Structure of a CIC decimation Filter



2.4 GSM Specifications

The proposed architecture is designed for GSM specifications[7]. The intermediate frequency of signal in Global System for Mobile communications is 70MHz. This signal is digitized with high speed analog to digital converters and has to be passed through a DDC. DDC performs the required frequency translation to produce a baseband signal of 200 KHz. The baseband signal is filtered to decimate a signal with decimation factor of 256 and pass band ripple of 0.01dB when high decimation rate is required and a narrow band signal has to be extracted from a wide band signal.

3. ARCHITECTURE

In order to address the problems related to the phase distortions due to phase synchronization and errors due to mixing operations, CORDIC algorithm is used to generate quadrature waveforms and multiplier-less mixing operation. CORDIC based DDCs have good SFDR when compared with the conventional Look up table approach[8]. The pipelined CORDIC architecture is implemented with 16-bit precision using carry save adders and carry look ahead adders with a maximum operating clock frequency of 190MHz and 205MHz respectively.

3.1 Numerically Controlled Oscillator

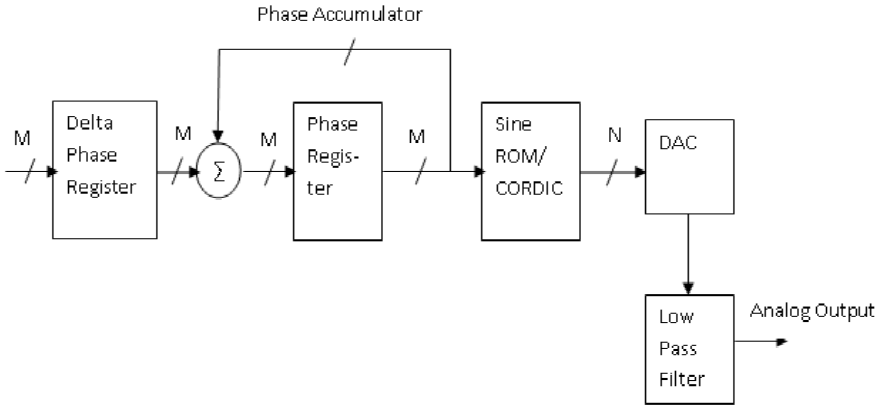
The structure of the numerically controlled oscillator shown in figure 3 consists of two blocks viz, phase accumulator and phase to amplitude (sine/cosine) generator. The digital output of the phase to amplitude generator is fed to Digital to Analog Converter and then passed through a low pass filter to remove the unwanted frequency components. The frequency of the NCO is controlled by the frequency control word f_{cw}, which is nothing but the phase increment given to the phase accumulator. In each clock cycle the phase accumulator increments itself by that value until it overflows and wraps around. Thus the frequency of NCO is given by

$$f_c = F_{clk} * \frac{f_{cw}}{2^{M-1}} \tag{5}$$

where F_{clk} is Clock Frequency, f_c is required local oscillator frequency, f_{cw} is Frequency control word.

We have configured the frequency control word such that the numerically controlled oscillator frequency is tuned to 70MHz for simulation and it is tuned to 35MHz for implementation on FPGA.

Figure 3 Block diagram of Numerically Controlled Oscillator



3.2 Digital Down Converter

As stated earlier, equations (3) and (4) describe the rotation of the vectors by an angle θ. The CORDIC module is configured in the circular rotation mode with inputs being $x_0 = x_{if} \cos(\omega_{if} n)$, y0 = 0, z0 = $\omega_c n$ as shown in figure. The output of the CORDIC module is given by the equation (6), generating the in phase and quadrature phase mixer outputs.

$$x_{out} = x_{if} \cos(\omega_{if} n)\cos(\omega_c n)$$

$$y_{out} = x_{if} \cos(\omega_{if} n)\sin(\omega_c n)$$

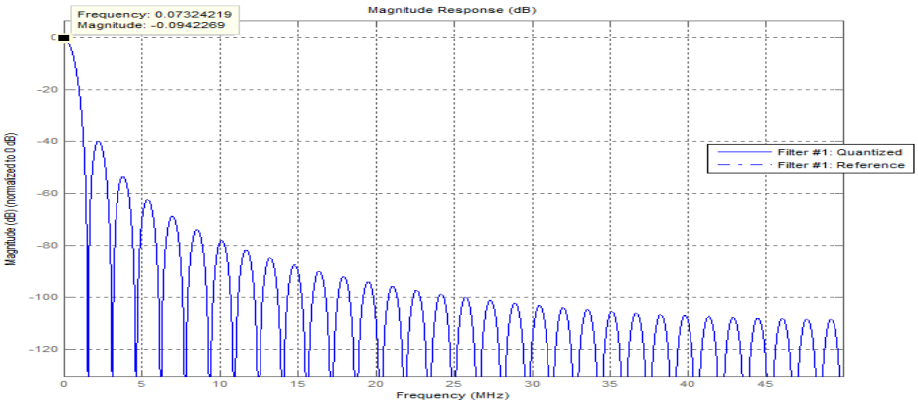
$$z_{out} = 0 \qquad (6)$$

According to the trigonometric identities, the output of the CORDIC module has two frequency components viz, $\omega_{if} + \omega_c$ and $\omega_{if} - \omega_c$. We have implemented a CORDIC algorithm using pipelined architecture with 16-bit precision in x/y datapath. We have chosen ω_{if} = 34.8MHz, ω_c = 35MHz to generate a difference component of 200 KHz with 100MS/s, which has to be decimated by a factor of 256 for Nyquist sampling rate.

3.3 Filtering and Decimation

We have implemented a CIC filter with a decimation rate of 64 to down sample satisfying Nyquist sampling rate. CIC filters are the best choice to decimate a signal when high decimation rate is required and a narrow band signal has to be extracted from a wide band signal. We have implemented a pipelined architecture for CIC filters in two stages using three integrators and three differentiators, a decimation factor of R=8 per stage. This is done to overcome the bit growth requirements as suggested in [6]. As the second stage CIC filter is clocked at a frequency of $f_{clk}/8$ power dissipation is also reduced. The gain of the CIC filter is normalized to unity so that the bit width of the integrators is reduced. The frequency response of the implemented CIC filter is shown in figure 4.

Figure 4 Frequency Response of implemented CIC Filter



4. RESULTS

The simulation setup for testing prototype DDC is shown in figure 5 uses three CORDIC based digital synthesizers/mixers generate message signal of 200KHz, Amplitude modulated wave with a carrier frequency of 35MHz and a mixer respectively. CIC filters as stated in section 3.3 are implemented to extract the inphase and quadrature component of the baseband signal at a lower sampling rate. The design is implemented on VIRTEX-4 XC4vSX35-10ff668 FPGA and the baseband signal is observed on CRO as shown in figure 6.

Figure 5

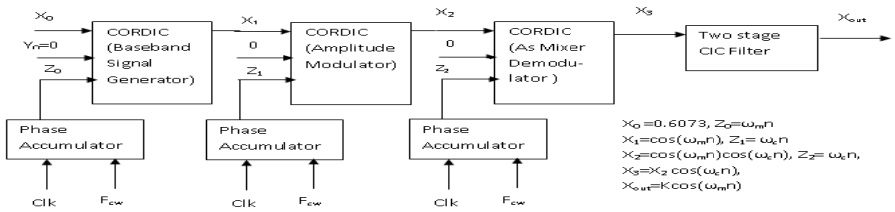
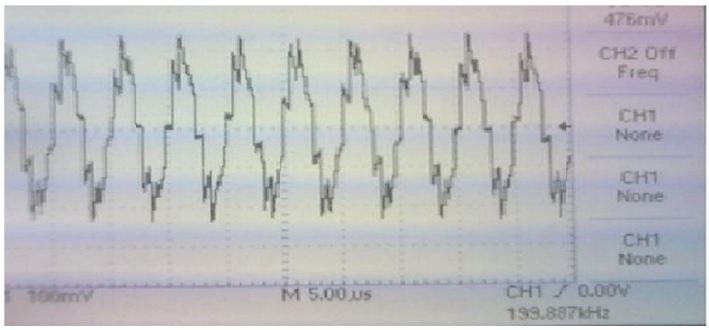


Figure 5 Digital Down Converted output observed on Oscilloscope



The proposed architecture for DDC is implemented employing Carry save adder and carry look-ahead adder. The comparison of device utilization summary for Digital Down Conversion of the inphase and the quadrature channel is shown in Table 1. From the results presented in Table 1, it is clear that the implemented carry save and carry look-ahead architecture utilises less hardware resources when compared with architecture in[1].

Table 1 Comparison of Hardware resource utilization for DDC (Device: XC4vSX35-10FF668)

S.No	Hardware Resources	Carry Save Architecture	Carry look ahead Architecture	Other Architecture [1]
1	No of Slice Flip-Flops	2320	1717	3373
2	No of four input LUTs	5414	4650	3575
3	No of DSP48s	0	0	60
4	Frequency of Operation	190 MHz	205 MHz	92.16 MHz

5. CONCLUSIONS

We have implemented architectures of digital down converter for GSM specifications on VIRTEX-4 XC4vSX35-10ff668 FPGA using carry save adders and carry look-ahead adders. The implemented architecture eliminates the need of explicit multipliers in the mixing stage and phase distortion due to synchronization issues. The CIC filter is a multiplier less filter which can be operated at a high frequency where as other filters in the filter chain can be designed using multipliers because the sample rate is decimated by a factor of 64. As compared with the other architecture in[1], carry save architecture can operate with a frequency of 190MHz and carry look-ahead architecture with a frequency of 205MHz with significant reduction in hardware resources. Further, a programmable triple mode down converter for down converting GSM, CDMA2000 and WCDMA signals, a 3G/4G Software Defined Radio application can be implemented.

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