數位電路設計 (Digital Circuit Design)
Lab2：組合電路之 HDL 模組撰寫與測試
(Writing and Testing the HDL Modules of Combinational Circuits)

1. 目標 (Goal)

在這次 Lab 中，我們希望同學們可以熟悉組合電路的設計原理，以 **gate-level modeling**、**dataflow modeling**、**behavioral modeling** 等不同方式撰寫其 HDL 電路模組，並撰寫測試模組。我們以減法器及乘法器為設計實例，分別模擬後，繳交模組檔案與波形圖。

The main purpose of this Lab Unit is to be familiar with the design of Combinational Circuits. Please write their HDL circuit modules by gate-level modeling, dataflow modeling, and behavioral modeling, and write the testbench for these circuit modules. We take binary subtractor and binary multiplier for practice. After simulation, upload the files of the modules and the waveforms of the simulation results.

2. 撰寫 HDL 電路模組與測試模組 (Design of the HDL Circuit Modules and Testbench)

A. 二元減法器之設計 (Design of Binary Subtractor)

(a) **半減器(Half Subtractor)**：設計一個具有延遲的半減器(half subtractor, HS)，有兩個輸入變數及兩個輸出變數。輸入變數為被減數 ***x*** 與減數 ***y***；輸出變數為差值 ***D*** 與借位輸出 ***B***。

Design a half subtractor (HS) with propagation delay which has 2 input variables and 2 output variables. The input variables are the minuend (被減數) ***x*** and the subtrahend (減數) ***y***, and the output variables produce the difference ***D*** and the borrow-out ***B***.

i. 請以 **gate-level modeling** 方式撰寫其 HDL 電路模組，其中 AND 與 OR 邏輯閘之延遲設為 5 個單位時間，XOR 與 XNOR 邏輯閘之延遲設為 10 個單位時間，NOT 邏輯閘之延遲則忽略之。模組名稱與 port list 請訂為 Lab2_half_sub_gatelevel(output D, B, input x, y)，檔案則命名為 Lab2_half_sub_gatelevel.v。

Please write the Verilog circuit module in **gate-level modeling**. Assume that the propagation delay of AND and OR gates is 5 time units, the propagation delay of XOR and XNOR gates is 10 time units, and the propagation delay of NOT gates is ignored. The circuit module and port list should be named as Lab2_half_sub_gatelevel(output D, B, input x, y), and its file should be named as Lab2_half_sub_gatelevel.v .

ii. 請撰寫一測試模組來完整測試此半減器電路模組；請將此測試模組命名為

t_Lab2_half_sub，檔案則命名為 t_Lab2_half_sub.v

Please write a testbench to test the half-substractor circuit module thoroughly. The testbench module should be named as t_Lab2_half_sub, and its file should be named as t_Lab2_half_sub.v .

(b) **全減器(Full Substractor)：**設計一個全減器(full subtractor, FS)，有三個輸入變數及兩個輸出變數。輸入變數為被減數 ***x***、減數 ***y***、及借位輸入 ***z***；輸出變數為差值 ***D*** 與借位輸出 ***B***。

Design a full subtractor (FS) which has 3 input variables and 2 output variables. The input variables are the minuend (被減數) ***x***, the subtrahend (減數) ***y***, and the borrow-in ***z***, and the output variables produce the difference ***D*** and the borrow-out ***B***.

i. 請利用**(a)**中的 gate-level 半減器來建構全減器。電路中 AND 與 OR 邏輯閘之延遲設為 5 個單位時間，XOR 與 XNOR 邏輯閘之延遲設為 10 個單位時間，NOT 邏輯閘之延遲則忽略之。請撰寫出全減器之 HDL 電路模組，模組名稱與 port list 請訂為 Lab2_full_sub(output D, B, input x, y, z)，檔案則命名為 Lab2_full_sub.v。

Please use the gate-level half-substractor designed in **(a)** to construct the full-substractor. Assume that the propagation delay of AND and OR gates is 5 time units, the propagation delay of XOR and XNOR gates is 10 time units, and the propagation delay of NOT gates is ignored. Plase write the HDL circuit module of the full-substractor. The circuit module and port list should be named as Lab2_full_sub(output D, B, input x, y, z), and its file should be named as Lab2_full_sub.v.

ii. 請撰寫一測試模組來完整測試此全減器電路模組；請將此測試模組命名為 t_Lab2_full_sub，檔案則命名為 t_Lab2_full_sub.v。

Please write a testbench to test the full-substractor circuit module thoroughly. The testbench module should be named as t_Lab2_full_sub, and its file should be named as t_Lab2_full_sub.v.

(c) **四位元漣波借位減法器(4-bit Ripple Borrow Subtractor, RBS)：**設計一個四位元漣波借位減法器，以產生兩個四位元二進位數字相減之結果。其輸入變數為四位元二進位被減數 ***X***、四位元二進位減數 ***Y***、及借位輸入 ***Bin***，輸出變數為四位元二進位差值 ***Diff*** 與借位輸出 ***Bout***。

Design a 4-bit binary subtractor which may produce the arithmetic difference of two 4-bit binary numbers. The input variables are the 4-bit binary minuend (被減數) ***X*** , the 4-bit subtrahend (減數) ***Y*****,** and the borrow-in ***Bin***, and the output variables produce the 4-bit difference ***Diff*** and the borrow-out ***Bout***

i. 利用**(b)**中之全減器來建構此 4-bit Ripple Borrow Subtractor (RBS)。請撰寫出此 RBS 之 HDL 電路模組，模組名稱與 port list 請訂為 Lab2_4_bit_RBS (output [3:0] Diff, output Bout, input [3:0] X, Y, input Bin)，檔案命名為 Lab2_4_bit_RBS.v。

Please use the full substractor designed in **(b)** to construct the 4-bit Ripple Borrow Subtractor (RBS). Please write the HDL circuit module of the RBS. The circuit module and port list should be named as Lab2_4_bit_RBS (output [3:0] Diff, output Bout, input [3:0] X, Y, input Bin), and its file should be named as Lab2_4_bit_RBS.v .

ii. 請撰寫此 RBS 之測試模組，至少以下述八組測資測試之。請將此測試模組命名為 t_Lab2_4_bit_sub，檔案則命名為 t_Lab2_ 4_bit_sub.v。

Please write the testbench of the RBS in which at least eight test data showed in the following figure should be included. The testbench module should be named as t_Lab2_4_bit_sub, and its file should be named as t_Lab2_4_bit_sub.v .

X	Y	Bin
1111	1111	1
0000	1111	0
0101	1010	1
1000	1100	1
0101	0101	0
1011	1011	1
0011	1100	1
1001	0110	1

(d) **四位元前看借位減法器(4-bit Borrow Lookahead Subtractor, BLS)：**設計一個四位元前看借位減法器，以產生兩個四位元二進位數字相減之結果。其輸入變數為四位元二進位被減數 ***X***、四位元二進位減數 ***Y***、及借位輸入 ***Bin***，輸出變數為四位元二進位差值 ***Diff*** 與借位輸出 ***Bout***。(Hint: 作法請參考課堂練習題說明。)

Design a **4-bit Borrow Lookahead Subtractor,** which may produce the arithmetic difference of two 4-bit binary numbers. The input variables are the 4-bit binary minuend (被減數) ***X*** , the 4-bit subtrahend (減數) ***Y,*** and the borrow-in ***Bin***, and the output variables produce the 4-bit difference ***Diff*** and the borrow-out ***Bout***. (Hint: Refer to the description in the class exercise.)

i. 請以 **gate-level modeling** 方式撰寫此 BLS 之 HDL 電路模組。AND 與 OR 邏輯閘之延遲設為 5 個單位時間，XOR 與 XNOR 邏輯閘之延遲設為 10 個單位時間，NOT 邏輯閘之延遲則忽略之。模組名稱與 port list 請訂為 Lab2_4_bit_BLS_gatelevel (output [3:0] Diff, output Bout, input [3:0] X, Y, input Bin)，檔案則命名為 Lab2_4_bit_BLS_gatelevel.v。

Please write the HDL circuit module of the BLS in **gate-level modeling**. Assume that the propagation delay of AND and OR gates is 5 time units, the propagation delay of XOR and XNOR gates is 10 time units, and the propagation delay of NOT gates is ignored. The circuit module and port list should be named as Lab2_4_bit_BLS_gatelevel (output [3:0] Diff, output Bout, input [3:0] X, Y, input Bin), and its file should be named as Lab2_4_bit_BLS_gatelevel.v

ii. 請以 **dataflow modeling (assign)**方式撰寫此 BLS 之 HDL 電路模組。無需考慮電路延遲。模組名稱與 port list 請訂為 Lab2_4_bit_BLS_dataflow (output [3:0] Diff, output Bout, input [3:0] X, Y, input Bin)，檔案則命名為 Lab2_4_bit_BLS_dataflow.v。

Please write the HDL circuit module of the BLS in **dataflow modeling** (**assign**) without considering the propagation delay. The circuit module and port list should be named as Lab2_4_bit_BLS_dataflow (output [3:0] Diff, output Bout, input [3:0] X, Y, input Bin), and its file should be named as Lab2_4_bit_BLS_dataflow.v

iii. 請以 **behavioral modeling** (**always**)方式撰寫此 BLS 之 HDL 電路模組。無需考慮電路延遲。模組名稱與 port list 請訂為 Lab2_4_bit_BLS_behavioral (output [3:0] Diff, output Bout, input [3:0] X, Y, input Bin)，檔案則命名為 Lab2_4_bit_BLS_behavioral.v。

Please write the HDL circuit module of the BLS in **behavioral modeling** (**always**) without considering the propagation delay. The circuit module and port list should be named as Lab2_4_bit_BLS_behavioral (output [3:0] Diff, output Bout, input [3:0] X, Y, input Bin), and its file should be named as Lab2_4_bit_BLS_behavioral.v

iv. 請以 2A(c) ii 所撰寫之測試模組(t_Lab2_4_bit_sub)測試此 BLS 之三個不同的電路模組。

Simulate the three different circuit modules of this 4-bit BLS by the same testbench of 2A(c) ii (t_Lab2_4_bit_sub).

B. 四位元乘四位元二進制乘法器之設計 (Design of a 4-bit by 4-bit binary multiplier)

設計一個二進制乘法器，以產生兩個四位元二進位數字相乘之結果。其輸入變數為四位元二進位被乘數 ***X***、四位元二進位乘數 ***Y***，輸出變數為八位元二進位積 ***Product***。無需考慮電路延遲。無需考慮電路延遲。Design a 4-bit by 4-bit binary multiplier, which may produce the product of two 4-bit binary numbers. The input variables are the 4-bit binary multiplicand (被乘數) ***X*** and the 4-bit binary multiplier (乘數) ***Y***, and the output variables produce the 8-bit product (積) , ***Product***. No need to consider the propagation delay of the circuit.

i. 請利用給定之四位元加法器電路模組(binary_adder.v)，以 **gate-level** 或 **dataflow** modeling 方式來建構此二進制乘法器，模組名稱與 port list 請訂為 Lab2_4_bit_multiplier_adder (output [7:0] Product, input [3:0] X, input [3:0] Y)，檔案則命名為 Lab2_4_bit_multiplier_adder.v。不可使用 Verilog operator “+” 或 “*”。

Please use the given 4-bit parallel adders (binary_adder.v) to construct the 4-bit by 4-bit binary multiplier. Do not use the Verilog operators “+” and “*”. The circuit module and port list of the multiplier should be named as Lab2_4_bit_multiplier_adder (output [7:0] Product, input [3:0] X, input [3:0] Y), and its file should be named as Lab2_4_bit_multiplier_adder.v .

ii. 請利用「+」運算子以 **behavioral modeling** (**always**) 來撰寫此四位元乘法器之電路模組，模組名稱與 port list 請訂為 Lab2_4_bit_multiplier_op (output [7:0] Product, input [3:0] X, input [3:0] Y)，檔案則命名為 Lab2_4_bit_multiplier_op.v。

不可使用 Verilog operator “*”。

Please use operator “+” to write the Verilog circuit module of the multiplier in **behavioral modeling** (**always**). Do not use the Verilog operators “*”. The circuit module and port list should be named as Lab2_4_bit_multiplier_op (output [7:0] Product, input [3:0] X, input [3:0] Y), and its file should be named as Lab2_4_bit_multiplier_op.v.

iii. 請撰寫此乘法器之測試模組，至少以下述八組測資測試之。請將此測試模組命名為 t_Lab2_4_bit_multiplier，檔案則命名為 t_Lab2_4_bit_multiplier.v。

Please write the testbench of this multiplier in which at least eight test data showed in the following figure should be included. The testbench module should be named as t_Lab2_4_bit_multiplier, and its file should be named as t_Lab2_4_bit_multiplier.v .

X	Y
1111	1111
0000	1111
1111	0000
1010	0101
0101	0101
0011	1110
1011	0111
1001	0110

C. 注意事項 ：(Notes)

- 請用 Icarus Verilog 作為編譯器，以 vvp 執行，並以 GTKWave 觀察波形圖。

  Please compile your Verilog code by Icarus Verilog, execute the compiled code by vvp, and then observe the waveform by GTKWave.
- 請務必依照上述各項目之規定命名模組及檔案。

  Be sure to name the modules and files as described above.
- 禁止抄襲，違者(抄襲者與被抄襲者)以 0 分計算。

  Any assignment work by fraud will get a zero point.
- 助教會使用不同的測試模組來驗證同學的電路模組正確性。

  After you hand in your code, TA will use similar TestBench modules with different test data to verify the correctness of your design of the Verilog circuit modules.

3. 作業及 HDL 模組繳交(Hand in)

A. 作業報告繳交：word 檔，命名為 Lab2_學號_姓名

包含下列項目：配分含隱藏測資之測試及 Demo 狀況

(1) 詳述半減器之電路設計流程，包括：真值表、布林代數式、邏輯電路圖。附上 2A(a)ii (半減器) 之模擬結果波形圖，並說明波形圖是否正確及所需之延遲時間。(10%)

(2) 詳述如何以半減器建構全減器，畫出電路方塊圖。附上 2A(b)ii (全減器) 之模擬結果波形圖，並說明波形圖是否正確及所需之延遲時間。(10%)

(3) 詳述如何以全減器建構四位元漣波借位減法器，畫出電路方塊圖。附上 2A(c)ii (4-bit RBS) 之模擬結果波形圖，並說明波形圖是否正確及所需之延遲時間。(10%)

(4) 詳述四位元前看借位減法器之電路設計流程，如：列出相關布林代數式(如：Pi、

Gi、Bi、Di 等)。附上 2A(d)iv (4-bit BLS) 之模擬結果波形圖，說明三個不同電路模組之波型圖是否正確，以及 gate-level modeling 電路模組所需的延遲時間。(40%)

(5) 詳述四位元乘四位元二進制乘法器之設計，畫出電路圖。附上 2B. iii 之模擬結果波形圖，並說明兩個不同電路模組之波型圖是否正確。(20%)

(6) 心得與感想、及遭遇到的問題或困難 (10%)

Hand in a word file, named Lab2_StudentID_Name , including the following items:

(Scores include answering problems in demo and the testing of extra data.)

(1) Describe the design process of the half substructor, including the truth table, the derived Boolean expressions, and the logic diagram. Attach the waveforms of the simulation results for the module of the half subtractor tested in 2A(a)ii, describe the propagation delay of the circuit, and determine whether the waveforms are correct or not. (10%)

(2) Describe how do you construct the full substructor by using half subtractors as basic blocks and draw the block diagram of the circuit. Attach the waveform of the simulation results for the module of the full subtractor tested in 2A(b)ii, describe the propagation delay of the circuit, and explain whether the waveforms are correct or not. (10%)

(3) Describe how do you construct the 4-bit ripple-borrow subtractor by using full subtractors as basic blocks and draw the block diagram of the circuit. Attach the waveform of the simulation results for the module of the 4-bit RBS tested in 2A(c)ii, describe the propagation delay of the circuit, and explain whether the waveforms are correct or not. (10%)

(4) Describe the design process of the 4-bit borrow lookahead subtractor (BLS), for examples, deriving the Boolean expressions of P_i, G_i, B_{i+1}, and D_i for i = 0~3. Attach the waveforms of the simulation results for the three different modules of the 4-bit BLS tested in 2A(d)iv, describe the propagation delay of the module written in gate-level modeling, and explain whether the waveforms of the three modules are correct or not. (40%)

(5) Describe the design process of the 4-bit by 4-bit binary multiplier and draw the block diagram of the circuit. Attach the waveforms of the simulation results for the two different modules of the multiplier 2B iii, and explain whether the waveforms are correct or not. (20%)

(6) Describe what you have learned from this lab unit and discuss the problems or difficulties encountered in this lab. (10%)

B. Verilog modules 檔案繳交：13 files

Hand in the following Verilog modules: 13 files

Lab2_half_sub_gatelevel.v、t_Lab2_half_sub.v、
Lab2_full_sub.v、t_Lab2_full_sub.v、
Lab2_4_bit_RBS.v、
Lab2_4_bit_BLS_gatelevel.v、Lab2_4_bit_BLS_dataflow.v、
Lab2_4_bit_BLS_behavioral.v、t_Lab2_4_bit_sub.v、
Lab2_4_bit_multiplier_adder.v、Lab2_4_bit_multiplier_op.v、
t_Lab2_4_bit_multiplier.v、binary_adder.v

4. DEADLINE

- 本實驗單元為一人一組， 作業請上傳至 E3 平台。
  This lab unit is one student per group. Please upload your Lab Report (word file) and the corresponding HDL code (.v files) onto e-Campus platform.

- 請將上述作業報告及 Verilog 電路模組與測試模組檔案(.v)全部壓縮成一個 **zip 檔** 或是 **rar 檔**(禁止上傳其他檔案格式)，並以「Lab2_學號_姓名」的方式命名，如：「Lab2_0816000_王大明」。
  Please compress the word file of lab report and the Verilog circuit modules and testbench described above all into one **zip** file or **rar** file (other format is not accepted), and name the zip file as "Lab2_StudentID_Name" , for example, "Lab2_0816000_Kent Chang".

- 作業繳交截止日期為 **2020/8/11 (二) 23:55**，**不接受逾期繳交。**
  The deadline for handing in lab report and Verilog files is **Aug. 11 (Tuesday) 23:55. No late hand-in is allowed.**

- **Demo** 時間暫定為 **8/12 (三)**、**8/13 (四) 4:30pm~9:00pm**，之後會再發公告通知大家上網填寫 Demo 時間表。未繳交作業者，將無法參加 Demo；雖有繳交作業但未 Demo 者，亦不予計分。
  The **demo time** is arranged at **2020/8/12 (Wednesday)** and **8/13 (Thursday) 4:30PM~9:00PM** tentatively, and we will send an announcement to inform you to fill the Demo schedule online. Those who have not hand-in their lab reports and Verilog files will not be able to demo their work, and those who have not demo their lab units will get zero score.

- 程式碼請勿抄襲別人或讓別人抄襲，經查證後此次 lab 總分一律以 0 分計算。
  Any assignment work by fraud will get a zero point