Microprocessor Systems: Principles and Implementation

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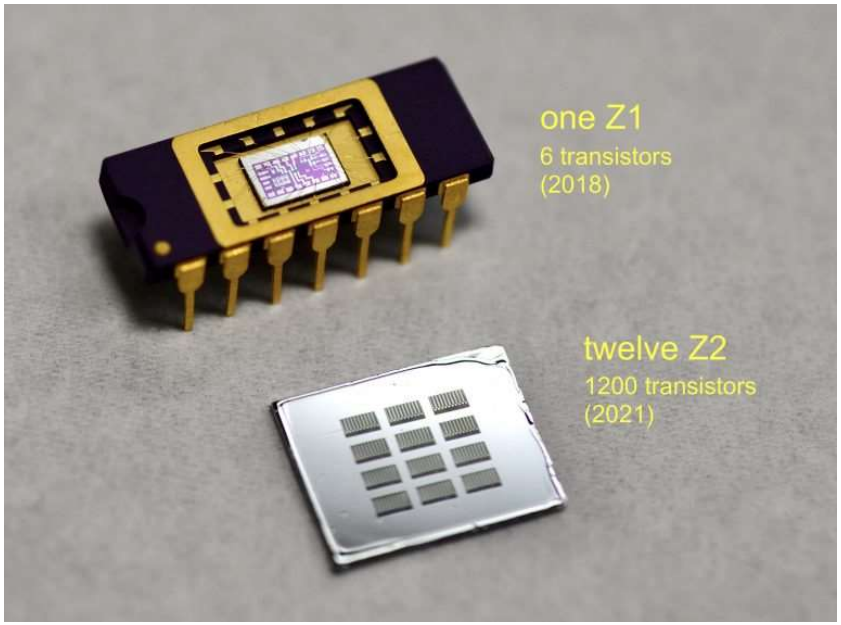
Before We Start …

- What is “hacker spirit?”
- Jargon File: a hacker is a person who enjoys exploring the details of programmable systems and stretching their capabilities, as opposed to most users, who prefer to learn only the minimum necessary.
- RFC-1392: a hacker is a person who delights in having an intimate understanding of the internal workings of a system, computers and computer networks in particular.

A Human Being Has No Limit

- A senior high school student in the USA built a 5-micron IC (an OP AMP) in a garage in 2018
- In 2021, he made an IC with transistor counts similar to Intel's 4004 CPU



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Introduction to the Course

- Lecture outline
  - Introduction to the Course, Tools, and Platform
  - RISC-V Instruction Set Architecture
  - Microprocessor Design: History and Review
  - Microarchitecture of the Aquila Core
  - Memory Subsystem of Microprocessors
  - I/O Subsystem of Microprocessors
  - Operating System Support of Microprocessors
  - Multicore Organization of Microprocessors

Homework & Grading

- Homework is based on an open-source RISC-V processor
- Homework labs:
  - 0: Simulation of a HW-SW Platform
  - 1: Real-time Debugging of a HW-SW Platform
  - 2: Branch Predictor Analysis and Improvement
  - 3: Memory Controller & Cache Improvement
  - 4: Communication with an I/O Device
  - 5: Running an RTOS
- Grading
  - HW 1 ~ 5 account for 70%
  - One online test account for 30%

The Open-Source Aquila SoC

- In this course, our homework will be based on the open-source Aquila SoC:

  http://github.com/eisl-nctu/aquila

- The Aquila SoC is an open-source processor core:
  - Developed at the EISLab, Dept. of CS, NYCU (NCTU)
  - RISC-V RV32-IMA compliant
  - In-order five-stage pipeline
  - Capable of running multi-threading RTOS
  - 0.9x Dhrystone MIPS/MHz

A Short Table of DMIPS/MHz

- Dhrystone is one of the oldest CPU benchmarks:

Computer/CPU	Year	Clock (MHz)	DMIPS/MHz
UNIVAC I (first ISA computer)	1951	2.25	0.0008
Intel 4004 (first microprocessor)	1971	0.74	0.124
IBM PC/Intel 8088 (begins the fall of mainframes)	1979	4.77	0.145
PDP-11/70 (where UNIX & C were created)	1970	? (~ 10)	0.15
Apple II (origin of Taiwan's PC industry)	1977	1	0.43
Alpha 21064 (descendent used in SunWay)	1993	150	0.675
ARM 7 (popular for 2G mobile phones)	1994	45	0.889
ARM Cortex M4 (intended for microcontrollers)	2010	200	1.25
Cray I (first super computer)	1975	80	2.0
ARM Cortex A53 (popular in 4G smartphones)	2014	1500	2.24
ARM Cortex A9 (popular for 3G feature phones)	2009	1500	2.5
ARM Cortex A76 (popular in 4G smartphones)	2018	3000	12.4
Intel i9-9900K	2018	4700	10.96

← Aquila (0.9)

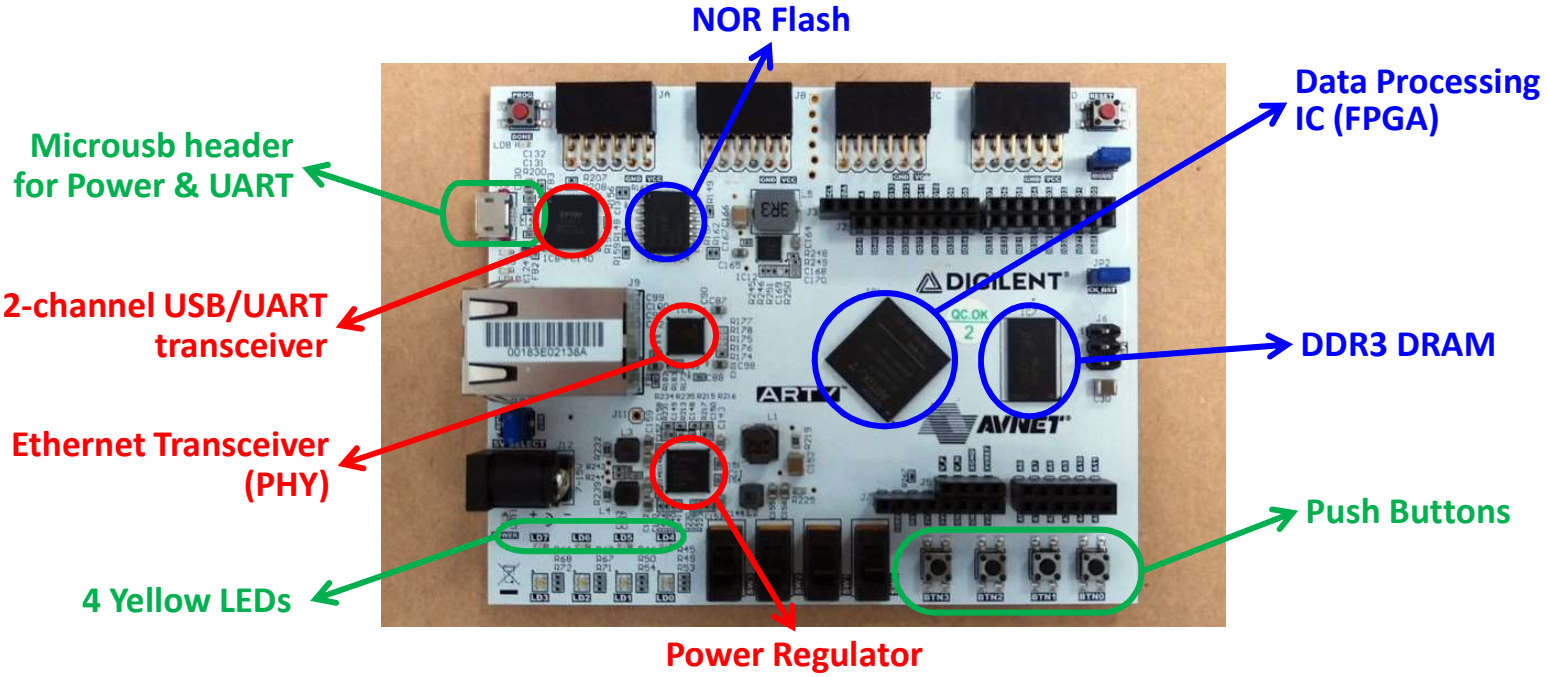
← Falco (1.75)

Skill Requirement

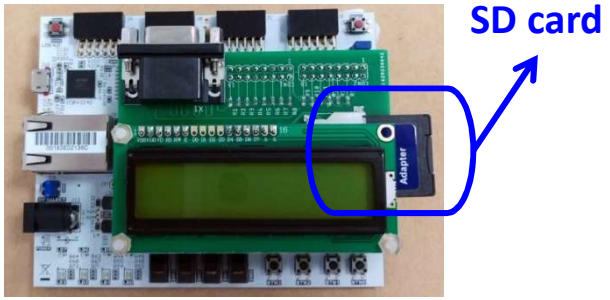
- Verilog programming for HW design
  - Using FPGA as digital design target
  - Using waveform simulator for functional debugging
  - Using embedded logic analyzer for live debugging
- C programming for SW design
  - Using GCC toolchain for SW development
  - Using linker script usage for SW memory organization
  - Tracing assembly code for SW debugging

The Development Board

- In this course, Arty A7-35 is used for experiments:



- We have designed an I/O daughter board for Arty:



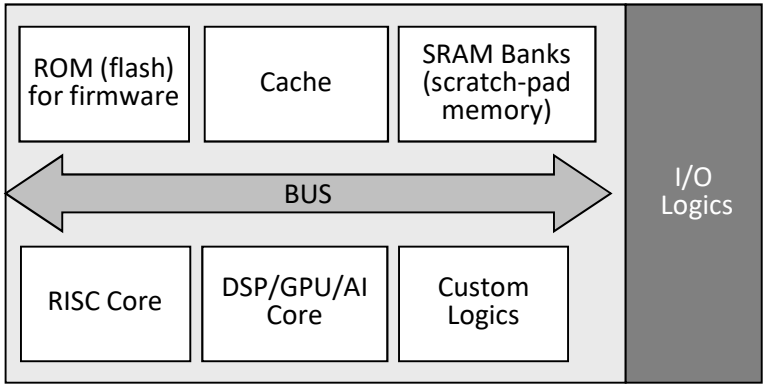
A Computing System

- All computing systems are used to compute functions
  - Input → Compute → Output
  - In this course, we have: UART/SD → FPGA → UART
- For board-level implementation, we integrate different ICs on a printed circuit board (PCB):
  - A PCB has multiple layers
    - Trace layers: connecting IC ports to other IC ports
    - Power layers: supply power to circuit components on the PCB
    - Ground layers: provide electrical grounds for signals
  - ICs implement analog functions and digital functions
    - Digital: data processing, buffering, signal arbitration and bridging
    - Analog: voltage regulation, AD/DA, signal amplification

System-on-Chip (SoC)

- SoC: Complex IC that integrates the major functional elements of a computing system into a single chip

- The SoC design typically incorporates
  - Embedded processor cores (RISC/DSP/GPU/AI)
  - On-chip memory blocks
  - Custom Accelerator Logic blocks
  - I/O logic blocks
  - Embedded software

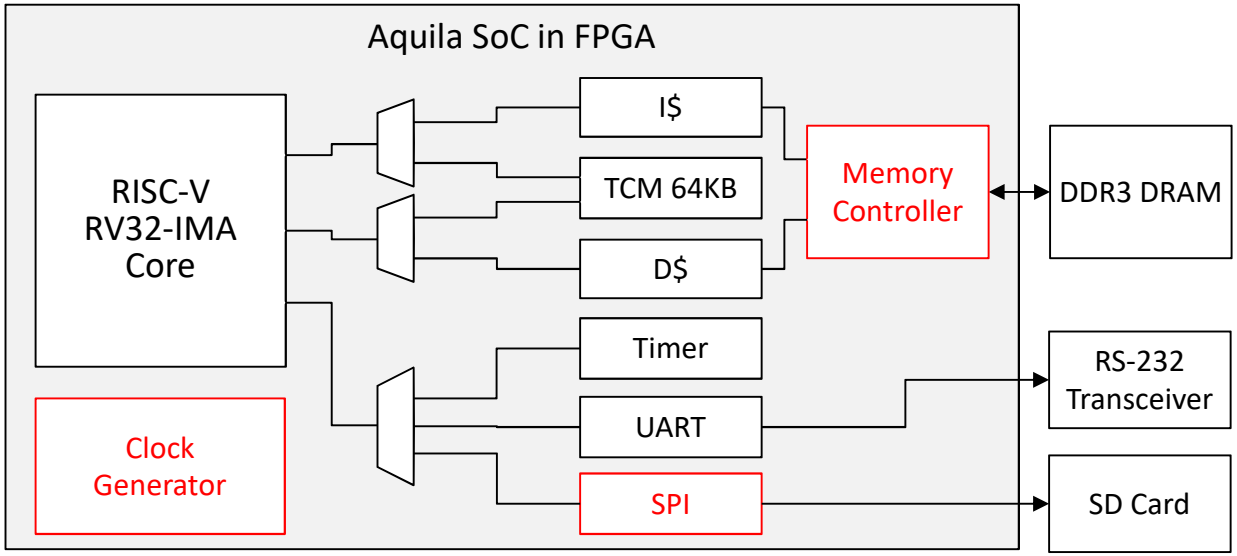


“Board-level” vs. “Chip-level” Design

- Board-level Design
  - More flexibility in development cycle
  - High manufacturing cost for large quantities
  - High power consumption
  - Bad for small form factor products
- Chip-level Design (i.e. SoC)
  - Difficult in design, debug, and verification
  - Design constrained by manufacturing process
  - Low cost for large quantities
  - Low power consumption
  - Excellent for small devices

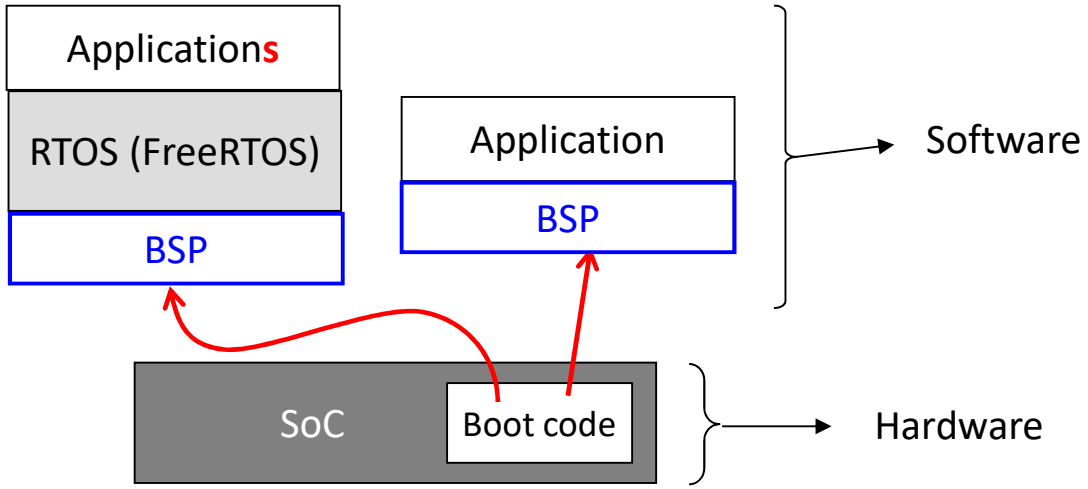
The Architecture of the Aquila SoC

- The Aquila SoC specification on Arty A7-35:
  - A 32-bit RISC-V core @ 50MHz
    - L1 4-way set associative I/D-caches
  - 64KB on-chip tightly-coupled memory (TCM)
  - 256MB DDR3 DRAM
  - Integrated UART, Timer, and SPI controllers



The System HW-SW Layers

- The layered structure of the HW-SW in this course:
  - BSP stands for Board Support Package, it contains a basic set of I/O routines, usually for C programs (similar to BIOS for PC)



- The layers can split or merge, depending on the cost, design expertise, market time constraints, etc.

System Platform Convergence

- Today, smart devices have many things in common:
  - Powerful processors and accelerators
  - Sensor integrations
  - Audio/video recording and/or playback
  - Complex feedback control of motors
  - Wireless communication capabilities
- One platform for all devices (Drones, ADAS, etc.)?
  - Application Processor
  - GPS
  - AV codecs
  - Motor control
  - Wi-Fi and BT

Discussions

- This course tries to teach you the entire HW-SW system, with almost all source code exposed to you
- Taiwan has an IT industry today because back in 1977, the co-funder of Apple, Steve Wozniak, insisted that the entire source code and the schematics of the Apple II computer should be available to users