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| Software Developer’s Guide  for the  **Core Flight SystemSP0-VxWorks6.9 Platform Support Package – Version 1.5.1.0** |
| Engineering Directorate  Software, Robotics, and Simulation Division |
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| National Aeronautics and  Space Administration  **Lyndon B. Johnson Space Center**  Houston, Texas |

Software Developer’s Guide

for the

Core Flight SystemTime-Triggered Ethernet Library

Version 1.5.1.0

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# INTRODUCTION

## Scope

This Software Developer’s Guide is for the Core Flight System (cFS) SP0-VxWorks6.9 Platform Support Package (PSP). From here on, the software product will be referred to as the SP0-VxWorks6.9 PSP.

## Purpose

This document describes how to install, configure, build, execute and troubleshoot the SP0-VxWorks6.9 PSP within the context of a cFS-based software system. The software was developed specifically as a software component of a cFS system, and hence, can only be built and executed within the cFS development and run-time environments. For additional information on cFE/cFS software framework, see documentation building and running included with the cFE software release. A copy can be obtained at <https://github.com/nasa/cfe>.

## Audience

The intended audience of this document are the cFS software developers. It is assumed that the developers are familiar with the general infrastructure of the cFS and its ecosystem as well as the general build and run of cFS applications and libraries. New cFS developers can start with CFS-101 as the initial cFS training. A copy can be obtained at <https://github.com/nasa/cfs-101>.

Note that this is not the standard Software User’s Guide for the Crew and Ground to command and control the target system. That would be a separate document to be produced by the project that uses this application.

## Document Status and Schedule

This Software Developer’s Guide is part of the documentation that comes with the software release of the SP0-VxWorks6.9 PSP.

# RELATED DOCUMENTATION

## Applicable Documents

The following documents, of the exact issue and revision shown, form a part of this Software Developer’s Guide to the extent specified herein.

Table ‑: Applicable Documents

| ***Document***  ***Number*** | ***Document Title*** | ***Revision /***  ***Release Date*** |
| --- | --- | --- |
| NPR 7150.2 | NASA Software Engineering Procedural Requirements | Rev C / Aug 2019 |
| EA-WI-025 | GFE Flight Project Software and Firmware Development | Rev D / Sep 2013 |
| GP-10021 | Core Flight Software Certification Software Development Plan | Baseline / May 2020 |

## Reference Documents

The following documents are reference documents utilized in the development of this Software Developer’s Guide. These documents do not form a part of this document and are not controlled by their reference herein.

Table ‑: Reference Documents

| ***Document***  ***Number*** | ***Document Title*** | ***Revision /***  ***Release Date*** |
| --- | --- | --- |
| GSFC 582-2008-012 | cFS Deployment Guide | Rel. 3.0 / Sep 2014 |
| GSFC 582-2007-001 | cFE Application Developer’s Guide | Rel. 5.4 / Sep 2014 |
| GSFC 582-2007-00 | OSAL Configuration Guide | Rel. 4.2.1 / Aug 2016 |
| TBD | SP0-VxWorks6.9 PSP Software Design Document | TBD |

# OVERVIEW

The SP0-VxWorks6.9 PSP is an abstraction layer of the processor’s Board Support Package (BSP), similar to how the OSAL is the abstraction layer of the Operating System. A PSP provides a common set of Application Programming Interfaces (APIs) that can be used by the cFE, the OSAL and any cFS application/library.

The SP0-VxWorks6.9 PSP is implemented specifically for the AiTech SP0-S processor running VxWorks v6.9 operating system.

# INSTALLATIOn

The SP0-VxWorks6.9 PSP requires no custom installation. It is packaged for distribution and installation just like any other PSP product, along with all the necessary documentation and artifacts. To install the SP0-VxWorks6.9 in a typical cFS workspace layout, the developer can add its source code to the “***psp***” directory. See <https://github.com/nasa/cfs> for a recommended cFS workspace layout.

Note that a project can opt to customize its own cFS workspace layout. When that is the case, the project’s custom installation process supersedes the cFS default installation process.

# BUILD

The SP0-VxWorks6.9 PSP requires no custom build. Adding the SP0-VxWorks6.9 PSP to the build is the same as adding any typical PSP implementation to an existing cFS build. See cFS Deployment Guide for information on cFS build process with CMake.

Note that if a project opts to use its own workspace layout, the cFS build steps will change to accommodate that custom workspace layout. When that is the case, the project’s build process supersedes the cFS default build process.

The SP0-VxWorks6.9 PSP is developed to build, load and executed out-of-box with the defined default values of its configurable parameters.

# CONFIGURATION

The SP0-VxWorks6.9 PSP can be configured for a project. To customize the configuration parameters, edit the C header file, “***psp/fsw/sp0-vxworks6.9/inc/cfe\_psp\_config.h***”.

# Application Programming Interfaces

This section includes the seven groups of SP0-VxWorks6.9 PSP APIs.

## Common APIs

Table 7.1 lists the SP0-VxWorks6.9 PSP APIs associated with common APIs for a cFE PSP.

Table ‑: [SP0-VxWorks6.9 PSP Common APIs](PSP_sp0-vxworks6.9_common.pdf)

## Startup APIs

Table 7.2 lists the SP0-VxWorks6.9 PSP APIs associated with PSP startup.

Table ‑: [SP0-VxWorks6.9 PSP Startup APIs](PSP_sp0-vxworks6.9_startup.pdf)

## FLASH APIs

Table 7.3 lists the SP0-VxWorks6.9 PSP APIs associated with FLASH-related IO.

Table ‑: [SP0-VxWorks6.9 PSP FLASH APIs](PSP_sp0-vxworks6.9_cdsflash.pdf)

## Exception Storage APIs

Table 7.2 lists the SP0-VxWorks6.9 PSP APIs associated with exception storage.

Table ‑: [SP0-VxWorks6.9 PSP Exception Storage APIs](PSP_sp0-vxworks6.9_exceptionstorage.pdf)

## Memory APIs

Table 7.3 lists the SP0-VxWorks6.9 PSP APIs associated with memory.

Table ‑: [SP0-VxWorks6.9 PSP Memory APIs](TTE_LIB_port.pdf)

## Memory Scrubbing APIs

Table 7.4 lists the SP0-VxWorks6.9 PSP APIs associated with memory scrubbing.

Table ‑: [SP0-VxWorks6.9 PSP Memory Scrubbing APIs](PSP_sp0-vxworks6.9_memoryscrub.pdf)

## Module APIs

Table 7.5 lists the SP0-VxWorks6.9 PSP APIs associated with module.

Table ‑: [SP0-VxWorks6.9 PSP Module APIs](PSP_sp0-vxworks6.9_module.pdf)

## SP0 Info APIs

Table 7.6 lists the SP0-VxWorks6.9 PSP APIs associated with SP0 statistical data.

Table ‑: [SP0-VxWorks6.9 PSP SP0 APIs](PSP_sp0-vxworks6.9_sp0.pdf)

## NTP Time Synchronization APIs

Table 7.7 lists the SP0-VxWorks6.9 PSP APIs associated with NTP time synchronization.

Table ‑: [SP0-VxWorks6.9 PSP NTP Time Synchronization APIs](PSP_sp0-vxworks6.9_timesync.pdf)

# Assumptions, dependencies and constraints

## Assumptions

1. The SP0-VxWorks6.9 PSP contains the implementation of the common PSP APIs, as well as the additional custom APIs that are specific to the SP0 processor. The custom APIs are dictated by the software system’s requirements, and hence, will vary from PSP to PSP.
2. The SP0-VxWorks6.9 PSP’s platform-specific configuration parameters are defined in the header file, ***psp/fsw/sp0-vxworks6.9/inc/cfe\_psp\_config.h***.
3. Aitech Bootloader seems to delete the Reserved Memory after reboot. Since Reserved Memory will get erased at each reboot, Critical Data Storage (CDS), Reset Memory, Volatile Disk Memory, and User Reserved Memory are synchronized on FLASH memory.
   * The Reserved Memory on RAM is the Gold copy.
   * The Reserved Memory sections on FLASH are used to recover data after a PROCESSOR reset. A POWERON reset will result in each Reserved Memory section being erased.
   * There is no process by which a user can disable a Reserved Memory section.

## Dependencies

1. The SP0-VxWorks6.9 PSP is dependent on the Wind River development tools (cross compiler, loader, etc.) for the VxWorks v6.9 operating system for the PowerPC processor family.

## Constraints

1. The SP0-VxWorks6.9 PSP is developed specifically for cFS, and hence, can only be used within the cFS development and run-time environments. For additional information on cFS, see documentation included with the cFE software release.

# LIMITATIONS AND WARNINGS

## Limitations

1. The SP0 exception handling is currently defaulted to the Kernel’s default exception handling.
2. Direct Memory Access (DMA) is not yet supported.
3. When running the SP0-VxWorks6.9 PSP’s unit tests on the SP0 platform, the SPE-based functions are currently stubbed out due to issues with the Wind River’s code coverage tool.

## Warnings

None.

# Known Problems

The SP0-VxWorks6.9 PSP’s known problems and known changes are documented in the SP0-VxWorks6.9 PSP’s Version Description Document (VDD).

# TroubleShoot

## Verifying successful startup

When the SP0-VxWorks6.9 PSP is successfully loaded and executed by the cFE Executive service, look for outputs similar to those below from the FSW execution output. Note that

1. the expected outputs might not immediately follow one another; and
2. the actual timestamps or will not be the same as the ones listed below; and
3. certain values relating to kernel configurations, such as memory addresses could be different.

. . .

CFE\_PSP\_Main()

. . .

CFE\_PSP: Set up VxWorks timebase, 50000000 ticks/sec, OS\_time\_t ratio=1/5

CFE\_PSP: Using DIRECT memory mapped EEPROM implementation

CFE\_PSP: Using DIRECT memory mapped RAM implementation

CFE\_PSP: Using DIRECT memory mapped PORT implementation

PSP SP0: Collecting Data

PSP MEMORY: SetupReservedMemoryMap Info:

RESET: Block Ptr: 0x3ffce090 Block Size: 0x000264e8

CDS: Block Ptr: 0x3fbe0000 Block Size: 0x00020000

VoDi: Block Ptr: 0x3fc00000 Block Size: 0x00200000

UsRe: Block Ptr: 0x3fa00000 Block Size: 0x00100000

PSP NTP SYNC: Task Initialized

PSP: Reset Register = 08

PSP: POWERON Reset: Power Switch ON.

CFE\_PSP: Clearing Processor Reserved Memory.

PSP MEM SCRUB: Starting Active Memory Scrubbing

PSP: Setting system tasks' priorities for 10 tasks.

PSP: Setting tLogTask priority from 0 to 0

PSP: Setting tShell0 priority from 0 to 201

PSP: Setting tWdbTask priority from 0 to 203

PSP: Setting tVxdbgTask priority from 0 to 200

PSP: Setting tNet0 priority from 0 to 25

PSP: Setting ipftps priority from 0 to 202

PSP: Setting ipcom\_syslogd priority from 0 to 205

PSP: Setting ipcom\_telnetd priority from 0 to 204

PSP: Could not find task ipcom\_egd

PSP: Setting FTCMP00 priority from 0 to 253

PSP: At least one vxWorks task priority set failed. System may have degraded performance.

PSP: PROCESSOR rst Source = 0x8 = (RESET\_SRC\_POR) Safe mode = 0, sbc = LOCAL, reason = 0, cause = 0x00000000

PSP: POST Test - PASSED - Marching Address Test(L) .

PSP: POST Test - Not Run - Marching Address Test(W).

PSP: POST Test - Not Run - Marching Address Test(B).

PSP: POST Test - Not Run - Walk a Bit Test(L).

PSP: POST Test - Not Run - Walk a Bit Test(W).

PSP: POST Test - Not Run - Walk a Bit Test(B).

PSP: POST Test - PASSED - Refresh Test(L) .

PSP: POST Test - Not Run - Refresh Test(W).

PSP: POST Test - Not Run - Refresh Test(B).

PSP: POST Test - PASSED - Random Data Test(L) .

PSP: POST Test - Not Run - Random Data Test(W).

PSP: POST Test - Not Run - Random Data Test(B).

PSP: POST Test - PASSED - Clear Memory Test(L) .

PSP: POST Test - Not Run - Clear Memory Test(W).

PSP: POST Test - Not Run - Clear Memory Test(B).

PSP: POST Test - Not Run - N/D Marching Bit Test(L).

PSP: POST Test - Not Run - N/D Marching Bit Test(W).

PSP: POST Test - Not Run - N/D Marching Bit Test(B).

PSP: POST Test - PASSED - ECC Read Test on SDRAM .

PSP: POST Test - Not Run - Boot Flash Fail Over.

PSP: POST Test - PASSED - EEPROM CRC Test .

PSP: POST Test - PASSED - User Flash CRC Test .

PSP: POST Test - Not Run - User Flash Retention Test.

PSP: POST Test - PASSED - CPU Test .

PSP: POST Test - Not Run - L1 Cache Test.

PSP: POST Test - Not Run - L2 Cache Test.

PSP: POST Test - PASSED - PCI Bridge Test .

PSP: POST Test - PASSED - cPCI Bridge Test .

PSP: POST Test - Not Run - Watchdog Reset Test.

PSP: POST Test - PASSED - Interrupt Test .

PSP: POST Test - PASSED - Timer Test .

PSP: POST Test - Not Run - Serial I/O External Loopback Test.

PSP: POST Test - PASSED - Memory Interface Test .

PSP: POST Test - Not Run - Combined Timer Test.

PSP: POST Test - PASSED - ECC Error Injection Test .

PSP: POST Test - PASSED - Serial I/O Internal Loopback Test - UART .

PSP: POST Test - Not Run - Watchdog Timer Test.

PSP: POST Test - Not Run - FPGA Watchdog Reset Test.

PSP: POST Test - PASSED - FPGA Watchdog Timer Test .

. . .

PSP: PSP Application Startup Complete

. . .

PSP EXC: Attached cFE Exception Handler.

PSP SetDefaultExceptionEnvironment not implemented

PSP NTP SYNC: CFE TIME Service is ready - Starting NTP Sync

. . .

# Appendices

## Abbreviations and Acronyms

| **Term** | **Definition** |
| --- | --- |
| API | Application Programming Interface |
| BSP | Board Support Package |
| CCDD | CFS Command and Data Dictionary tool |
| CCSDS | Consultative Committee for Space Data Systems |
| cFE | Core Flight Executive |
| cFS | Core Flight System |
| CI | Command Ingest cFS application |
| COTS | Commercial Off-the-Shelf |
| CSC | Computer Software Component |
| CSCI | Computer Software Configuration Item |
| CSU | Computer Software Unit |
| EA | JSC Engineering Directorate Organization Code |
| ES | cFE Executive Services |
| EVS | cFE Event Services |
| GFE | Government Furnished Equipment |
| GSFC | Goddard Space Flight Center |
| HK | Housekeeping cFS application |
| JSC | Johnson Space Center |
| MDT | Message Definition Table (for SCH\_TT application) |
| MID | Message Identifier |
| NASA | National Aeronautics and Space Administration |
| NPR | NASA Procedural Requirements |
| OS | Operating System |
| OSAL | Operating System Abstraction Layer |
| PSP | Platform Support Package |
| SB | cFE Software Bus |
| SBNg | Software Bus Network for Gateway cFS application |
| SCH | Scheduler cFS application |
| SCH\_TT | Time-Triggered Ethernet Scheduler cFS application |
| SDD | Software Detailed Design |
| SDT | Schedule Definition Table (for SCH\_TT application) |
| SRS | Software Requirements Specification |
| TBD | To Be Determined |
| TDM | Time-Division Multiplexer |
| TO | Telemetry Output cFS application |
| TTE | Time-Triggered Ethernet |
| TTE ES | Time-Triggered Ethernet End System |
| TTE\_LIB | Time-Triggered Ethernet cFS Library |
| TTE\_MGR | Time-Triggered Ethernet Manager cFS application |
| VDD | Version Description Document |

## Definition of Terms

None.

# Notes

None.