Week 05 Final Report

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The Seven Step Process:

1. *Complete the Plan of Record (POR):*

- Understanding the circuit step by step made it easier for us to draw the 'Back of the Napkin' Schematic and carry out the calculations for nodal voltages and currents required in the later stage of the project.
- We estimated the total budget of the board to be $25, but the PCB alone cost us $30 and $5-10 additionally for the components making it a total of $40.
- For the next design, we should take into account the shipping cost of the PCB as well.

2. *Complete the initial Bill of Materials (BOM):*

- Ordering components in a set of either 10 or 20, is sometimes cheaper than buying components in non-regular quantities (e.g. 22uF Capacitors)
- For 1K and 50-ohm resistors, we only looked up parts with 1/4-watt power rating as the I^2R losses through the resistors were far less than the power rating.
- For the next design, we could perhaps put a filter on DIgikey for the lowest prices and not on the power rating of the components because sometimes the higher rating components can be cheaper.

3. *Complete the Schematic Capture and Final BOM:*

- As we had a well scoped out POR, it made easier to create the schematic as we knew the board functionality pretty well and we also didn't miss out on any passive components. Also referring the data sheets for the ICs made it easier to map out the pin configuration on the schematic.
- Having similar names for the nets such as 5V and 5V_J is sometimes confusing, as a small error in the net names can cause incorrect connections between the components.
- For the next design, the net names could be kept as distinct as possible to avoid any unforced human error.

4. *Complete the Layout and order all parts:*

- The component on the PCB were well spaced out (within the std. board size), making it easier to route the traces in between the components. Similarly, soldering was also simplified as there was minimum interference of the components with the soldering iron.
- A well-planned project schedule during the POR phase, made it possible to order the PCB well in time.
- For the Power Jack footprint there were rectangular slots on the GKO layer as well as circular holes for the leads. The overlapping of these two features, caused confusion at the manufacturing end over which feature to go ahead with.
- For the next design, we can make sure that all the component footprints are aligned correctly with its mounting holes.
- We could also provide polarity dots for correctly orienting the LEDs and the ICs without the need to refer datasheets while assembly.

5. *Complete the Assembly:*

- Keeping the thermal relief pads around the solder pads in copper plane, made it easier to solder components onto them.
- As there were no polarity indicators on the silkscreen of the board, we unnecessarily spent time figuring out the orientation of ICs and LEDs.

- For the next design, we will keep in mind to make liberal use of flux, as it makes soldering easier (dissolves Tin Oxide layer on the pads and reflows the solder onto the pad) and at the same time does not have any side-effects.
- Always make sure the tip of your soldering iron is clean and shiny (free from tin oxide).

6. Complete the Bring up, Troubleshoot and Final Test:

- Having the isolation switches on the board, made it easier to isolate different parts of the board and test them separately.
- Setting the oscilloscope trigger mode to auto, sometimes makes the signal shaky and difficult to read through. Instead using the single shot triggering on oscilloscope, makes the signal clear and distinct for easy reading.
- Also, the probe needs to be compensated correctly each and every time, before making any of the readings on oscilloscope.
- While testing in future, first step would always be to compensate the probe well, check in the oscilloscope if the appropriate probe has been detected (1x or 10x) as it causes ambiguity in the reading. Wherever necessary the single shot triggering mode of oscilloscope will be used. And, the isolation switches will be added to the circuit while bringing up the board for the ease of debugging.

7. Complete the Documentation:

- Maintaining success and failure records after each and every step, made it easier to track the progress and document it well at the end of the project.
- While we were only monitoring success and failures, from the next design, we should have a risk register through which we anticipate issues based on our experience, before the start of all the above mentioned 6 steps.

Readings from the week 01 Timer 555 board (Layout done by us):

1) *3.3 V Power Rail:*

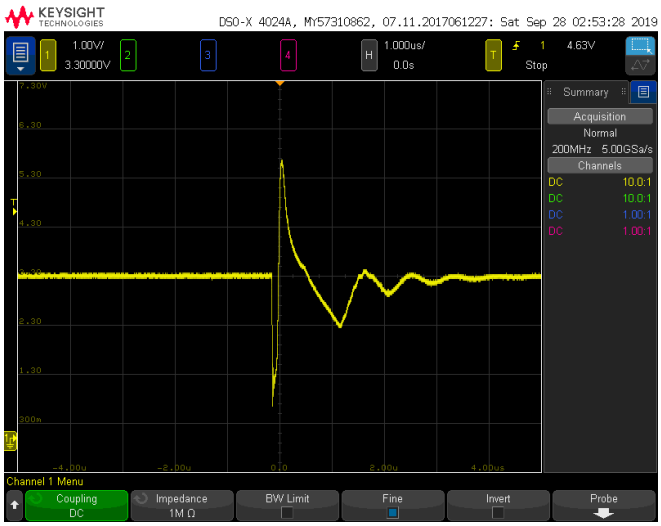

Figure 1: 3.3 V rail signal noise (Without Decoupling Capacitor)

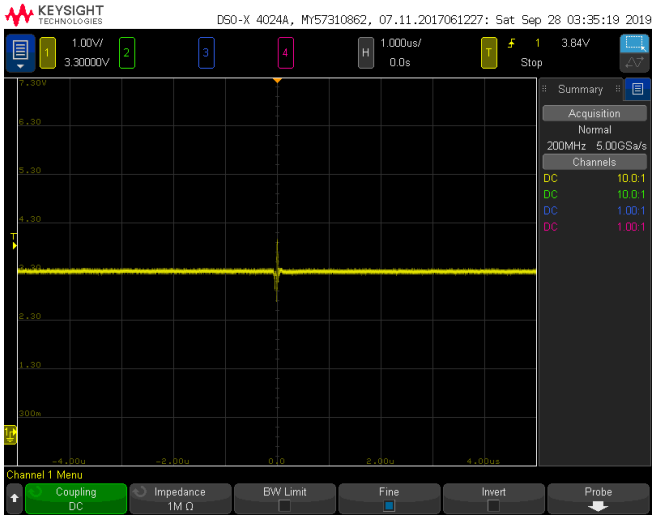

Figure 2: 3.3 V rail signal noise (With Decoupling Capacitor)

We expected to see a voltage of 3.3 V after the LDO (as per the POR), along with some noise in the circuit. A decoupling capacitor of 22 uF was added to reduce the rail-noise.
As we can see, there is a huge difference in the voltage levels of the 3.3V rail before and after adding the decoupling capacitors. Without the decoupling capacitor, the peak to peak noise in the signal was observed to be around 5 V whereas after adding the decoupling capacitor, the peak to peak noise reduced to around 1 V.

2*) 555 Timer Output:*

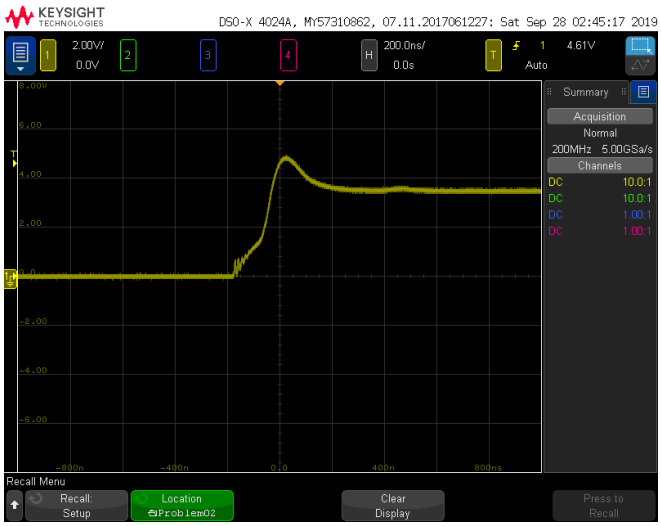

Figure 3: 555 timer output signal rising edge (Without Decoupling Capacitor)

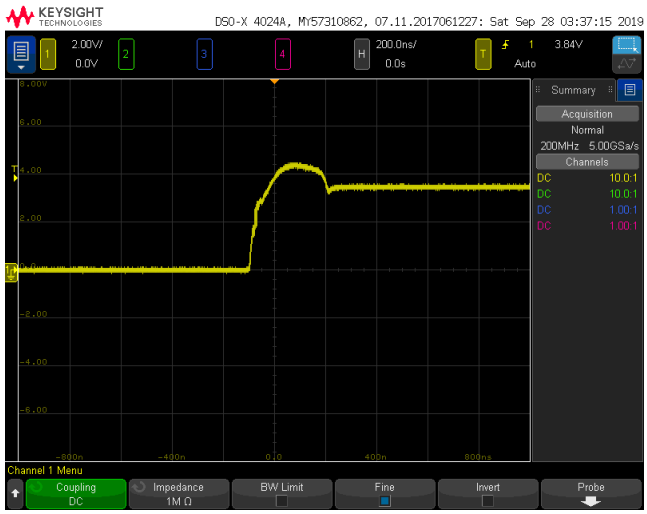

Figure 4: 555 timer output signal rising edge (With Decoupling Capacitor)

We are using a SA555 timer which operates at 100 kHz frequency. The rise time is 125 nsec without the decoupling capacitor whereas after adding the decoupling capacitor, the rise time reduced to 50 nsec.

3) *Hex Inverter Output:*

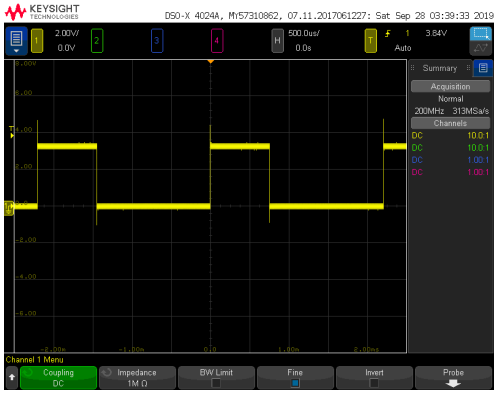

Figure 5: Hex Inverter Trigger output signal (Duty Cycle Measurement)

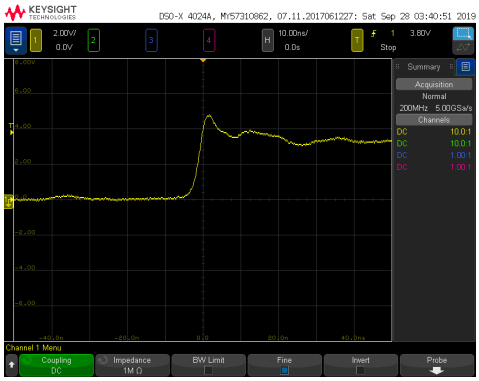

Figure 6: Hex Inverter Trigger output signal (Rising Edge) Rise time ≈ 2.5 nsec

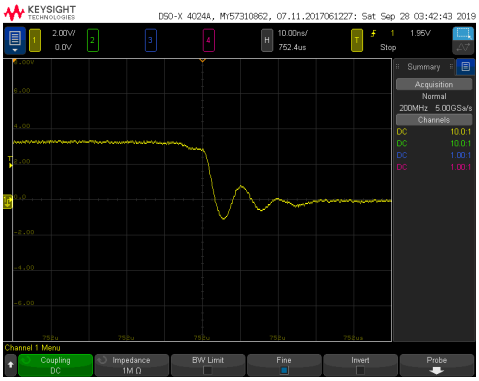

Figure 7: Hex Inverter Trigger output signal (Falling Edge)

Q4) *Quite High and Quite Low signals **with Decoupling Capacitor:***

Figure 8: Hex Inverter Quite High signal (Spring Return Tip)

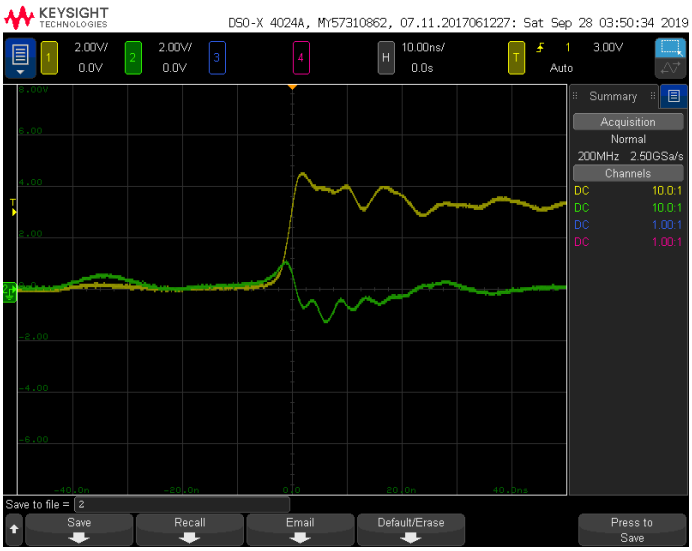

Figure 9: Hex Inverter Quite Low signal (Spring Return Tip)

Conclusion: As the switching occurs at a greater frequency inside the hex inverter, we can see significant switching noises at its output. After adding the decoupling capacitors, we can see there is sufficient reduction in the noise levels.

(EXTRA PICTURE):

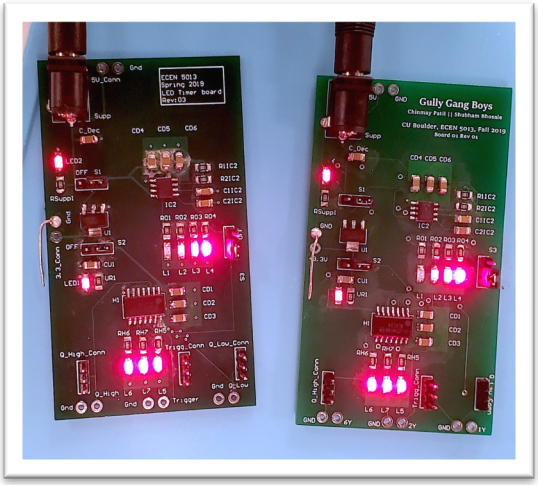

Figure 10: Both boards functioning at the same time