Generating 25% Duty Cycle Clock with 50% Frequency

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Objective - To design a synchronous 25% duty-cycle clock generator with 50% frequency that produces a clock HIGH for exactly one input cycle and LOW for three cycles, using Verilog in eSim. Applications include clock gating, sampling systems, and power-efficient designs.

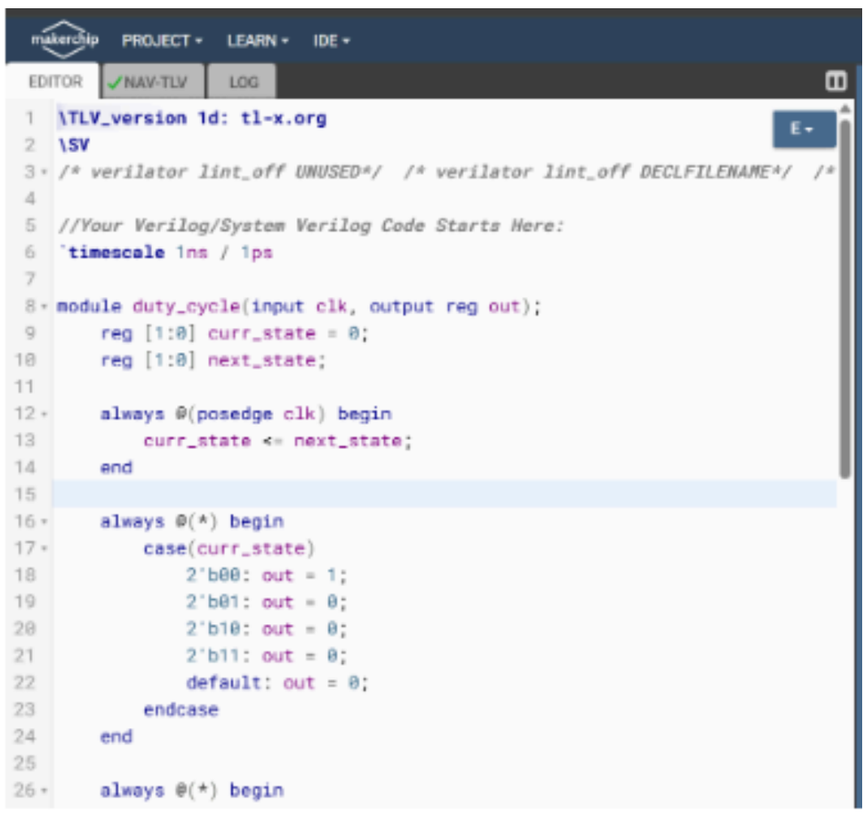
I. Circuit Details

The circuit is based on a 2-bit counter implemented with two D flip-flops. The outputs of the flip-flops represent the current state, and combinational logic generates the next state. A 4-to-1 multiplexer is used to produce the output HIGH for state 00 and LOW for all other states.

- Sequential block: 2-bit counter using D flip-flops with asynchronous reset.

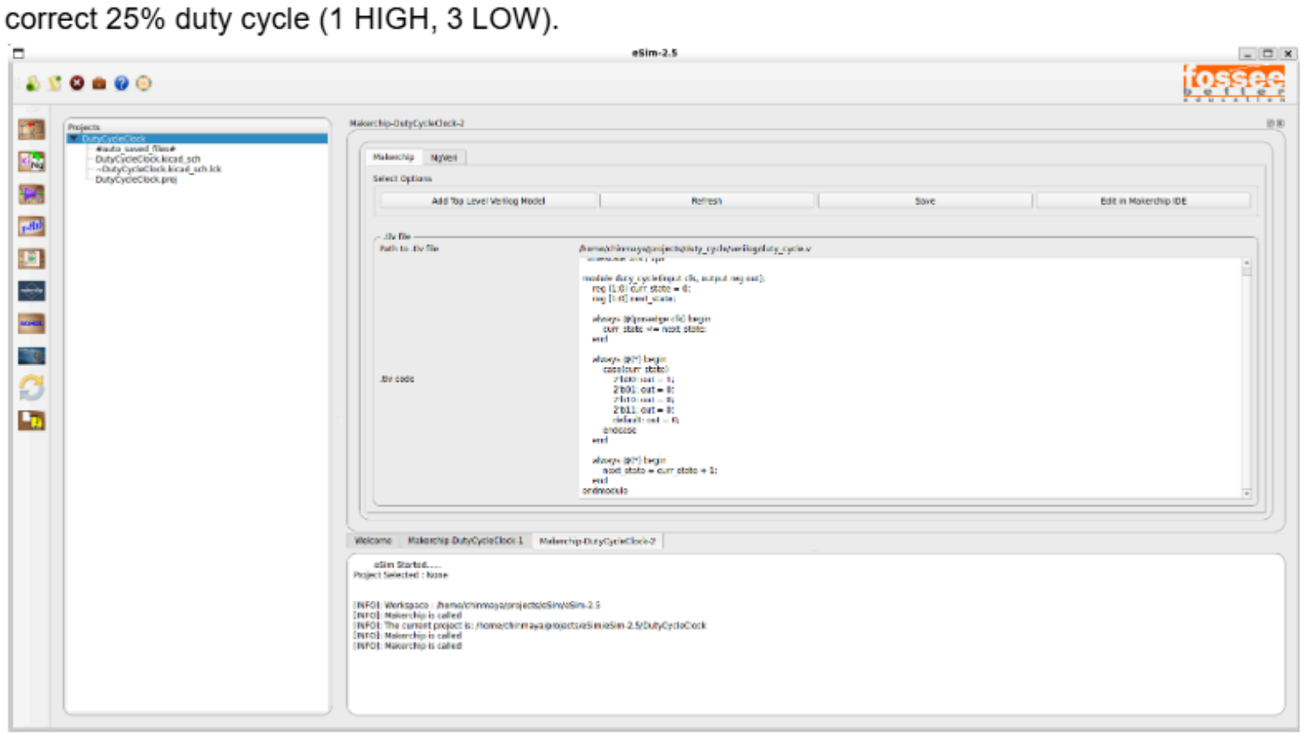
- Combinational block: Next-state logic using addition.

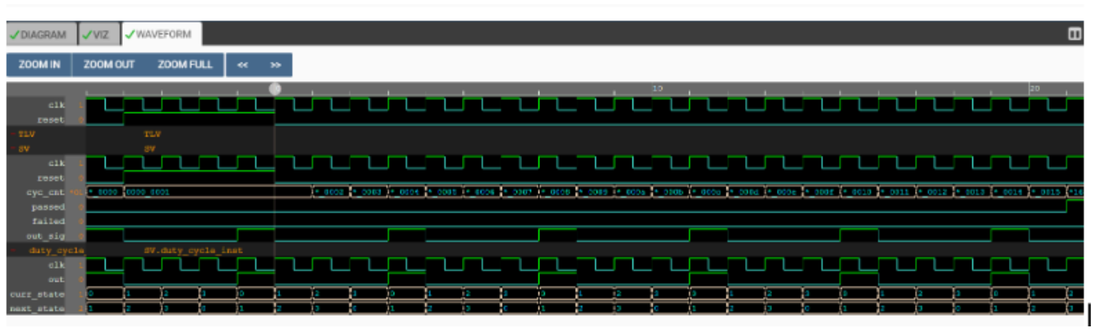
- Output block: 4-to-1 multiplexer generating the 25% duty-cycle output.



II. Simulation Results

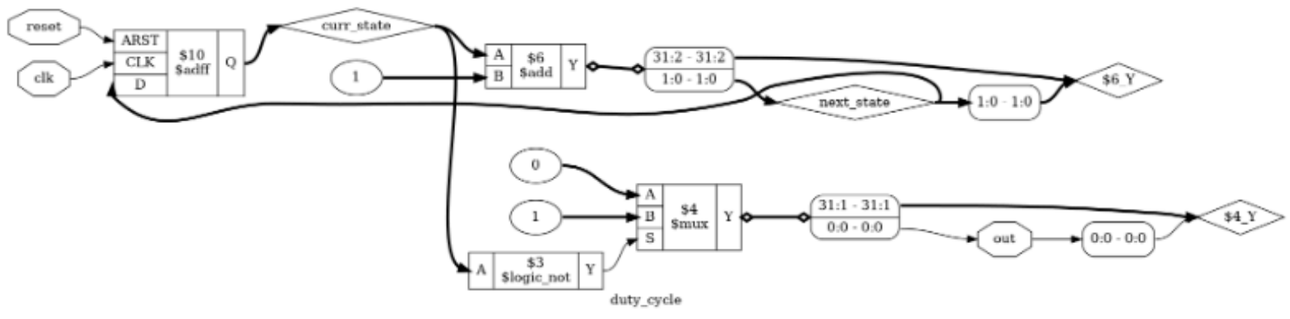
Simulation performed using Makerchip IDE using eSim. Output waveform demonstrates the correct 25% duty cycle (1 HIGH, 3 LOW).

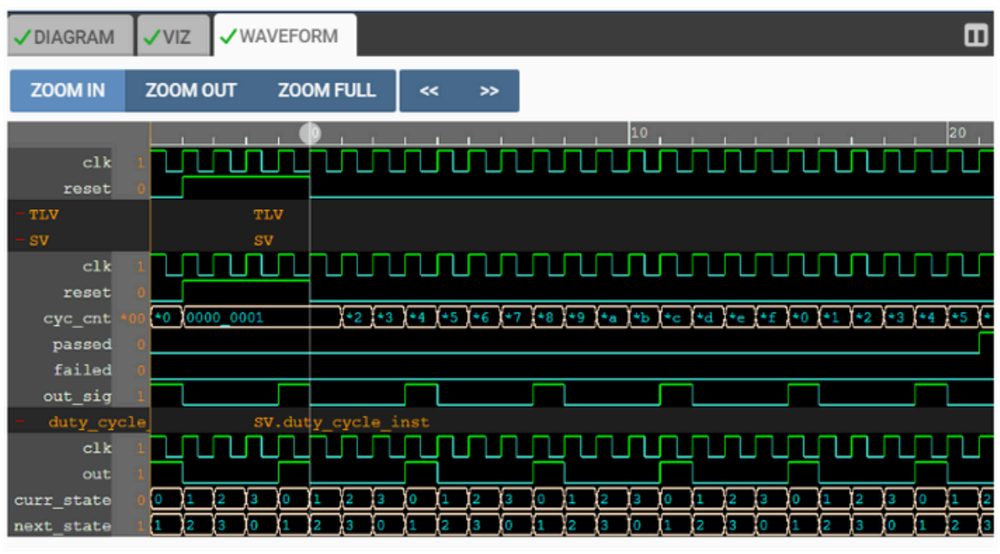




III. Netlist

Synthesis done using Yosys.





IV. Conclusion

The design successfully implements a 25% duty-cycle clock generator with 50% frequency. Simulation results match expected outputs, and the design is verified using Yosys synthesis. The circuit is compact and suitable for integration in larger digital systems requiring precise timing control.

GitHub Repository:
https://github.com/chinmaya24163/duty_cycle

README.md:
https://github.com/chinmaya24163/duty_cycle/blob/main/README.md

REFERENCES

https://patents.google.com/patent/US8442472B2/en