# Generating 25% Duty Cycle Clock with 50% Frequency

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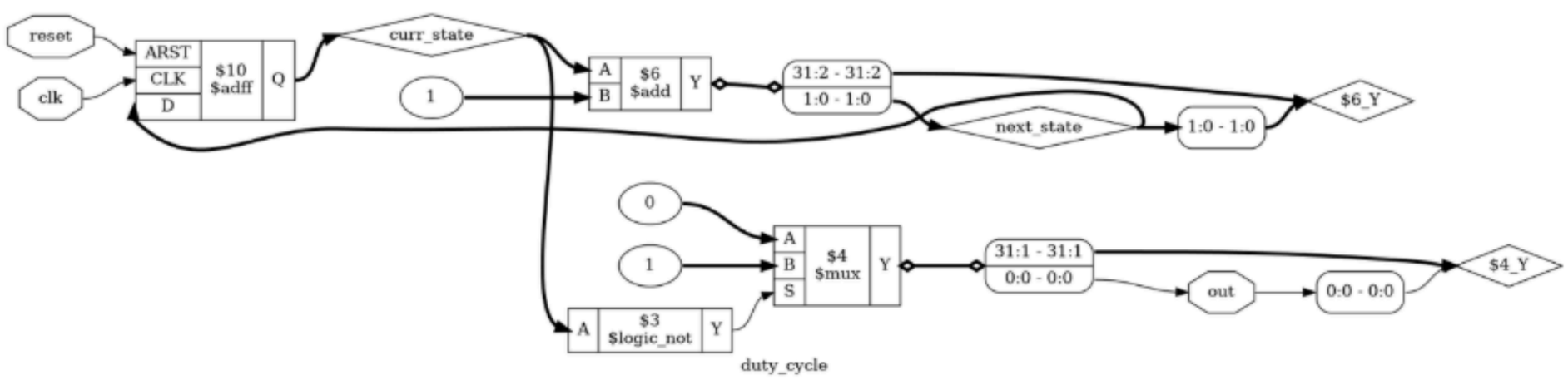
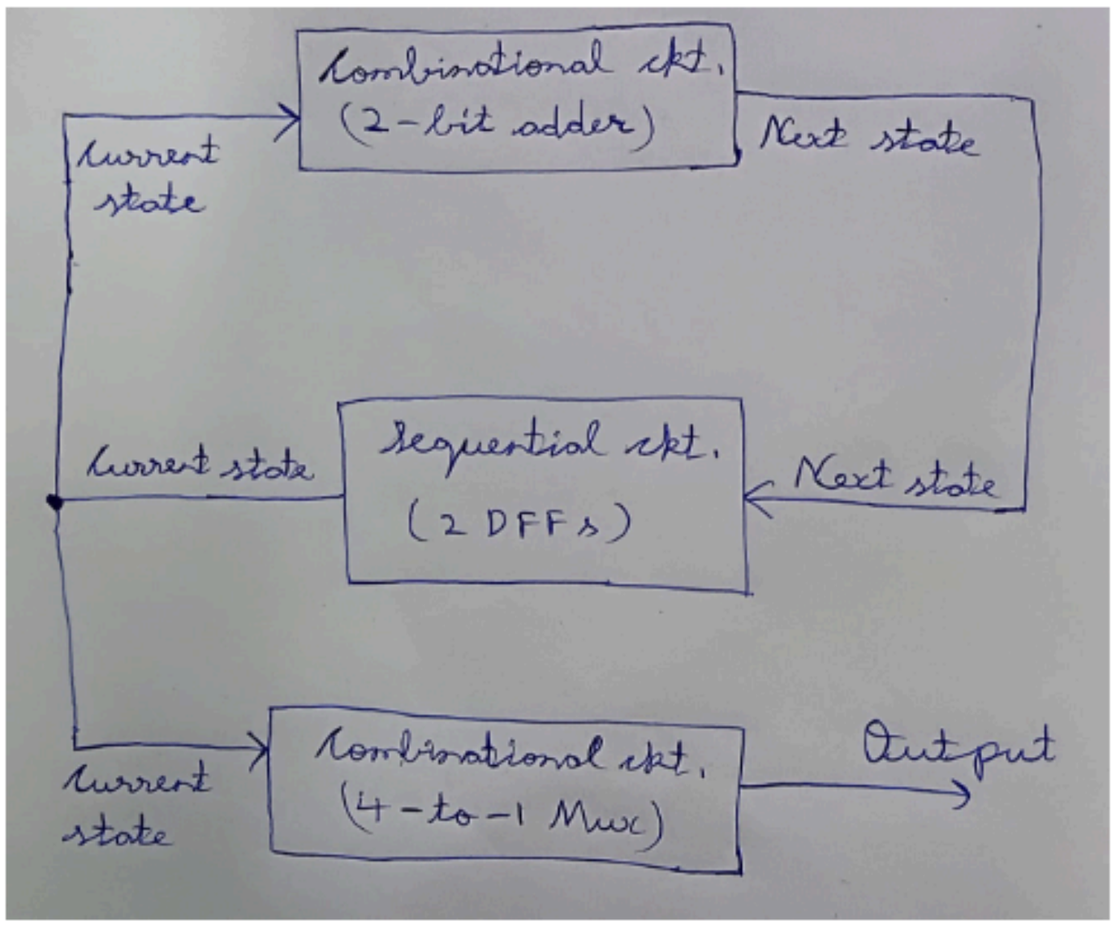
**Abstract —** This paper presents an implementation to generate a synchronous 25% duty-cycle clock with 50% frequency to the input clock, that is HIGH for exactly one input clock cycle and then LOW for three cycles. It finds application in clock gating, sampling systems, power management, and communication protocols.

## I. Circuit Details

The overall circuit is a combination of a sequential circuit and two combinational circuits. The circuit can be treated as that of a 2-bit counter with 4 states, and so the sequential part consists of two edge-triggered D flip-flops, clocked by the input clock, used to form the 2-bit counter, with their outputs forming the MSB and LSB digits of the 4 states. The DFFs also have an asynchronous active high reset signal which forces the current state to the state “01”. The sequential part thus passes the next state on to the current state. A combinational block consisting of a 2-bit adder is responsible for the transition of the current state to the next state in the order - 00→01→10→11→00 and so on. The output of the circuit is delivered by a combinational block, consisting of a 4-to-1 multiplexer, that depends on the current state. The output is HIGH only for the state 00.




## II. Block Diagram




## III. Waveform


## REFERENCES

https://patents.google.com/patent/US8442472B2/en