POWER REDUCTION IN 8T SRAM USING POWER GATING

1. Introduction

Memory elements play a crucial role in modern integrated circuit (IC) design, significantly influencing system performance, area efficiency, and power consumption. Among various memory technologies, Static Random-Access Memory (SRAM) is widely used due to its high speed and low standby power characteristics. SRAM forms an essential component in processors, cache memories, and embedded systems.

However, as CMOS technology continues to scale down, conventional six-transistor (6T) SRAM cells face challenges related to read stability, leakage power, and reliability. These limitations become more severe at lower supply voltages and advanced technology nodes.

To overcome these issues, the eight-transistor (8T) SRAM architecture has been introduced. By decoupling the read and write operations through a dedicated read path, the 8T SRAM cell significantly improves read stability and noise margins. This project focuses on the design, simulation, and power optimization of an 8T SRAM cell using NMOS footer-based power gating.

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2. 8T SRAM Cell Architecture

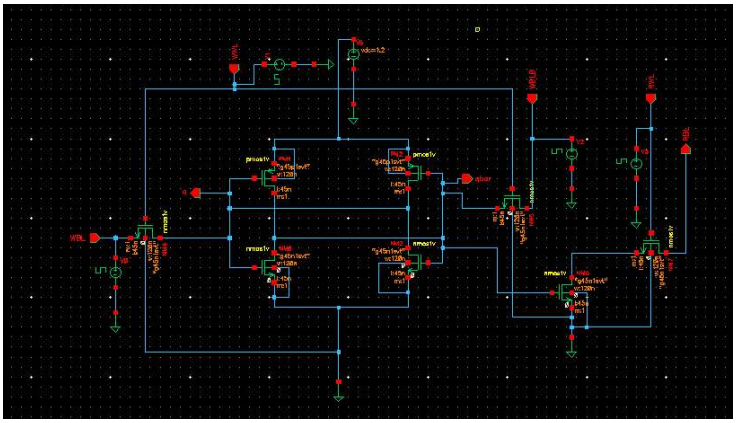

Fig 1: 8T SRAM

The 8T SRAM cell consists of eight MOS transistors organized into two functional blocks:

2.1 Storage Core (6T)

The storage core is formed using two cross-coupled CMOS inverters, consisting of:

- Two PMOS transistors
- Two NMOS transistors

This configuration allows the cell to store one bit of data (0 or 1) reliably as long as power is supplied.

Two additional NMOS access transistors connect the storage nodes to the write bitlines (WBL and WBLB). These access transistors are controlled by the **Write Word Line (WWL)**, enabling write operations.

2.2 Read Buffer (2T)

The read buffer is implemented using two NMOS transistors controlled by the **Read Word Line (RWL)**. The read bitline (RBT) is isolated from the internal storage nodes, preventing read disturbances and enhancing stability.

This separation of read and write paths is the key advantage of the 8T SRAM architecture.

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3. Operation of 8T SRAM Cell

3.1 Write Operation

During a write operation:

- The WWL is asserted high.
- The access transistors connect the internal storage nodes to the write bitlines.
- Data from WBL and WBLB overwrites the stored value.

3.2 Read Operation

During a read operation:

- The read bitline (RBT) is precharged to a high voltage.
- RWL is asserted high.

- Depending on the stored data, RBT either remains high or discharges to ground.

Since the storage node is isolated from the read path, the stored data is not disturbed during read operations.

NOTE: Pre-charge circuitry ensures RBT is initially set high before read operations, enabling correct sensing without disturbing the memory state

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4. Simulation of Conventional 8T SRAM

The 8T SRAM cell was designed and simulated using CMOS technology in a schematic-based environment.

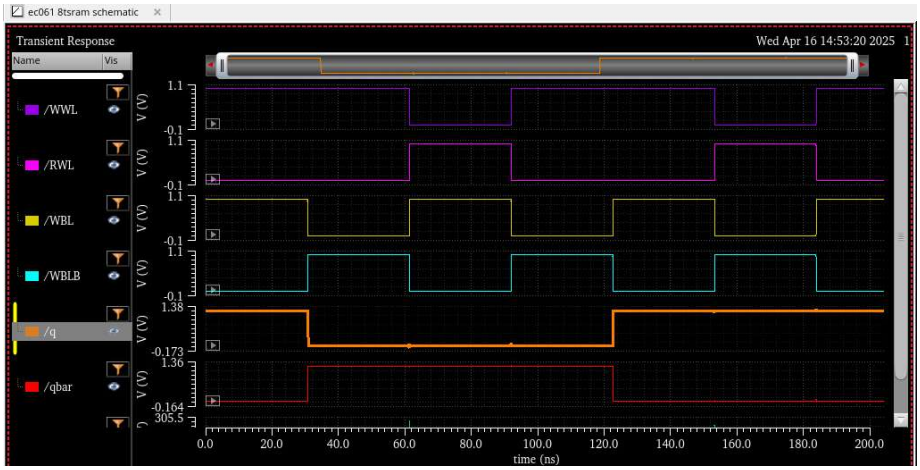

Fig 2: Simulation Results

4.1 Simulation Results

Parameter	Value
Voltage	659.9×10^{-3} V
Current	9.588×10^{-9} A
Power	6.328×10^{-9} W

These results indicate that while the 8T SRAM provides improved stability, leakage current still contributes significantly to power consumption.

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5. Power Optimization Using NMOS Footer

To reduce leakage power, an **NMOS footer transistor** is introduced in the ground path of the 8T SRAM cell.

5.1 Working Principle

- **Footer ON:** SRAM operates normally.
- **Footer OFF:** Ground path is disconnected, significantly reducing leakage current.

This technique is known as **power gating**, and it is particularly effective during standby or idle modes.

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6. Simulation of Optimized 8T SRAM

The optimized 8T SRAM with NMOS footer was simulated under the same conditions as the conventional design.

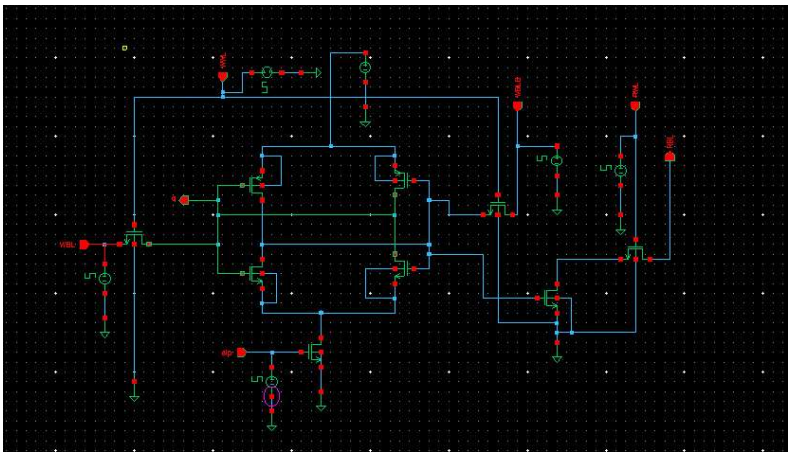

Fig 3: Optimised 8T SRAM

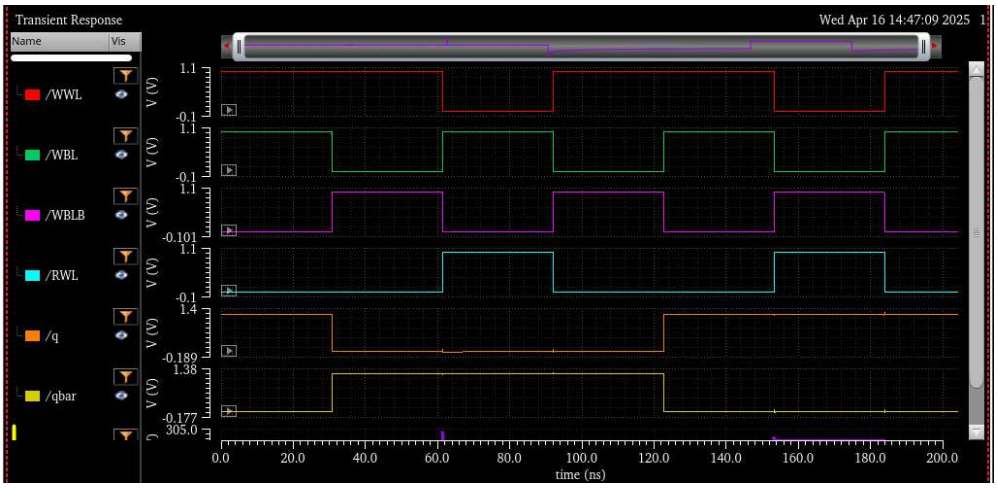

Fig 4: Simulation Results

6.1 Simulation Results

Parameter	Value
Voltage	655.5×10^{-3} V
Current	906.3×10^{-15} A
Power	6.026×10^{-13} W

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7. Result Comparison

Parameter	Normal 8T SRAM	Optimized 8T SRAM
Voltage	659.9 mV	655.5 mV
Current	9.588 nA	906.3 fA
Power	6.328 nW	0.6026 pW

The optimized design achieves approximately **10^4× reduction in power consumption**, with minimal impact on operating voltage.

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8. Conclusion

This project presented the design and power optimization of an 8T SRAM cell. Compared to conventional 6T SRAM, the 8T architecture provides improved read stability and robustness due to its decoupled read and write paths.

By introducing NMOS footer-based power gating, leakage power is significantly reduced, especially during idle conditions. Simulation results confirm a substantial reduction in power consumption from the nanowatt range to the sub-picowatt range.

The optimized 8T SRAM design is therefore well suited for low-power VLSI systems, embedded applications, and energy-efficient memory architectures.

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9. Future Scope

- Analysis of read/write delay impact due to power gating
- Extension to SRAM array-level design
- Use of multi-threshold devices for further leakage reduction
- Comparison with header-based power gating techniques
