

Chinmay Rozekar

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OBJECTIVE

Seasoned Silicon Validation Engineer aiming to leverage 4+ years of experience in physical design, signoff processes, and cross-functional team leadership to drive silicon learning and PPA optimization for premium mobile GPUs as a Senior Silicon Learning Lead at Samsung SARC/ACL, utilizing a strong background in problem-solving, technical mentorship, and global collaboration.

PROFESSIONAL SUMMARY

- Versatile engineer with 4+ years in Silicon Validation, adept in both Pre-Silicon and Post-Silicon environments, specializing in system-level testing and product quality enhancement.
- Committed to leveraging technical expertise for reducing operational costs and enhancing product specifications.
- Excels in cross-functional team collaboration, test automation with Python, C/C++, and Java, and innovative problem-solving.

EXPERIENCE

Product Development Engineer

July 2020 – Present

Advanced Micro Devices (AMD)

Austin, TX

System Level Testing (SLT)

- Led system-level testing for AMD's Ryzen 8040 'Hawkpoint' series, Accelerated Processing Units (APUs), ensuring adherence to customer environment standards.
- Spearheaded Test Time Reduction (TTR), eliminated redundant tests, for reducing operational costs through DPPM Yield Analysis in Production.
- Experienced in monitoring production yield and debugging/root cause analysis of high-Pareto items in production fallout.
- Experienced in performing SoC Characterization for Product Definition by setting Test-Program flows on volume testing.
- Maintained the test program codebase repository using Atlassian BitBucket, overseeing the development and release of test content throughout the product roadmap.
- Collaborated with Diagnostic, BIOS, and Design teams to enhance CPU performance features, contributing to product specification improvements.
- Experienced in Customer RMA Debug issues through secure fuse unlocking during Field Return Analysis (FRA).
- Established and managed an in-house server farm and APU client board setup, ensuring robust testing environments and streamlining development.

Product Engineering Co-Op

Jan. 2019 – Dec.2019

Advanced Micro Devices (AMD)

Austin, TX

- Designed and automated test programs for Human Body Model Testing, reducing Engineering time by 90%.
- Reverse-engineered and redesigned a 20-year-old robotic graphical user interface in Python, reducing engineering time by 95%.
- Conducted stress tests on AMD products according to industry standards, qualifying products for production.
- Performed scheduled calibration and waveform verification for preventive maintenance as per ISO 9000 standards
- Conducted Design of Experiments on AMD products for Capacitive Modeling to optimize protection circuitry

Graduate Research Assistant

Jan 2020 – May 2020

Rochester Institute of technology

Rochester, NY

- Developed a process flow for thin film IC development, covering various fabrication steps
- Designed and simulated NMOS devices to determine sub-threshold voltages and model leakage current
- Conducted electrical device characterization to optimize gate oxide thickness on NMOS devices.

TECHNICAL SKILLS

Process Engineering: Thin Films, PVD, CVD, Sputtering, Dry Etch, Metrology, Characterization
Languages: Java, Python, BASH, C/C++, SQL, HTML/CSS, XML, Markdown, MATLAB, Perl
Libraries: Matplotlib, Pandas, Numpy, Scikit-learn, Selenium
Developer Tools: Git, Jira, Confluence, Linux, CI/CD, IntelliJ Idea, VS Code, PyCharm, Eclipse, Jupyter, Anaconda, JSON, Notepad++, LaTeX
Protocols: JTAG, PCIE, DFT, Boundry SCAN, ATPG
Simulation: KiCAD, SolidWorks, COMSOL Multiphysics, Silvaco-Athena, Pyxis(Mentor Graphics)
Data Analysis: Excel, Power-BI, JMP, Python

PROJECTS

- Review of Thin Film Technologies for Flexible Electronics** Jan 2020 – May. 2020
- Designed a simulation model for growing a 1 μm layer of flexible crystalline Si substrate on top of Tungsten metal layer using SOI method in Silvaco Athena.
- A Thermally actuated four-legged MEMS based Silicon Micro-robot** May 2018 – Dec. 2018
- Designed and fabricated a thermally actuated MEMS based Silicon micro-robot. Modeled design in CAD / Solidworks and Heat Transfer using COMSOL multi-physics FEA.

EDUCATION

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| Rochester Institute of Technology | Rochester, NY |
| <i>Master of Science, Electrical Engineering</i> | <i>Aug. 2017 – May 2020</i> |
| Bharati Vidyapeeth University | Pune, India |
| <i>Bachelor of Technology, Electrical Engineering</i> | <i>Aug. 2012 – June 2016</i> |