

Chinmay Rozekar

Hillsboro, OR | chinmay.rozekar@gmail.com | linkedin.com/in/chinmayrozekar | github.com/chinmayrozekar

Lead QA Engineer · Automation Strategy · Python · CI/CD · Cloud and Desktop Testing

PROFILE

Lead-level QA engineer with 6 years of experience designing automation frameworks, defining validation strategy, and enabling cross-team quality processes across semiconductor and software domains. Skilled in Python, CI/CD, and test infrastructure for complex desktop and cloud environments. Known for data-driven quality metrics, reproducible pipelines, and mentoring engineers to accelerate release readiness.

TECHNICAL SKILLS

Languages: Python, Tcl, Bash, Perl, C/C++, SQL

Automation and QA: Test framework design, regression infrastructure, API and functional testing, KPI dashboards

Tools: Jenkins, Docker, Git, Jira, Confluence, Power BI, Siemens Calibre PERC, DRC/LVS

Domains: Desktop application testing, cloud automation, reliability verification, post-silicon validation

OS: Linux (RHEL/SLES), macOS, Windows

EXPERIENCE

Software QA Engineer Calibre PERC

2024 – 2025

Siemens EDA (Mentor Graphics)

Wilsonville, OR

- Led QA automation for the Calibre PERC reliability verification platform, guiding strategy for ESD, EOS, and multi-voltage validation flows used by global design teams.
- Developed Python and Tcl pipelines for nightly regression and configuration checks, reducing setup time by 20 percent and improving stability by 15 percent.
- Collaborated with R&D and CAD groups to align rule sequencing QA and electrical topology coverage across hierarchical SoC designs.
- Built Power BI dashboards tracking runtime and defect metrics to support data-driven release decisions and improve visibility across teams.
- Authored QA runbooks and onboarding documentation that reduced new engineer ramp-up time by 30 percent and standardized validation procedures.

System Level Test Engineer Product Development

2019 – 2024

Advanced Micro Devices (AMD)

Austin, TX

- Owned post-silicon validation for Ryzen 8040 APU SoCs across 14 IP blocks to ensure functional, power, and reliability qualification before production.
- Automated data capture and yield analysis in Python and Perl, reducing manual debug effort by 40 percent and improving correlation accuracy across lots.
- Developed Power BI dashboards for real-time KPI visualization and triage tracking that shortened defect turnaround by 25 percent.
- Mentored junior engineers on test data pipelines and analysis tools and standardized debug processes across multiple teams.
- Collaborated with firmware and diagnostics teams to reproduce and resolve BIOS and system-level failures during qualification.

SELECTED PROJECTS

HelmNet AI Safety Helmet Detection

- Developed a VGG16 transfer learning model to detect PPE compliance in industrial images with 91.8 percent validation accuracy and 0.92 F1-score. Deployed with Streamlit and Docker for real-time use.

SuperKart Retail Forecasting Workflow

- Built a Gradient Boosting forecasting model on 8,763 transactions achieving $R^2 = 0.86$ and $MAE = 0.43$ and deployed via a Dockerized Flask API with a dashboard for cloud prediction.

RAG-based Medical Assistant

- Implemented a Retrieval Augmented Generation system using Mistral-7B and ChromaDB on a 4000 page medical corpus that improved retrieval accuracy by 23 percent versus baseline search.

EDUCATION

University of Texas at Austin <i>Post Graduate Program in Artificial Intelligence and Machine Learning</i>	2025 <i>Online</i>
Rochester Institute of Technology <i>Master of Science, Electrical Engineering</i>	2020 <i>Rochester, NY</i>
Bharati Vidyapeeth University <i>Bachelor of Technology, Electrical Engineering</i>	2016 <i>Pune, India</i>