CHINMAY ROZEKAR

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Sr. Software QA Engineer

Physical Verification | New Product NPI | System Level Testing | Test Engineering | QA and Automation

AI first Software Engineer with 5+ years across semiconductor validation, fab-adjacent automation, and cleanroom experience (RIT SMFL). Adept in Automation, Python tooling and dashboards for trend detection and change-point triage. Practical AI experience (LLMs, RAG) used to accelerate data analysis and QA automation.

Skills

Python | Bash Scripting | TCL | AWK | SVRF | C ++ | Perl | Java | Unix | Calibre PERC | DRC | LVS | RVE | TensorFlow | PyTorch | Scikit-learn | LLMs | RAG | Hugging Face | Transformers | GitHub | CVS | GitLab | Jira | Confluence | Docker | Bitbucket | Agile | Scrum | Waterfall | Test Program Development | JTAG | RMA | Customer Escalations | Data Analysis | Clean Room Experience | Wafer Probe | Oscilloscope

Experience

SIEMENS EDA (MENTOR GRAPHICS), Wilsonville, OR **July 2024 - October 2025**

Software QA Engineer

Validated Calibre PERC 3DIC rule decks by developing and executing QA test cases to ensure accurate topology, ESD, and reliability checks across semiconductor designs.

- Owned QA reliability verification for Calibre PERC (LDL, topology, voltage propagation, point-to-point resistance, current density), maintaining reproducible testcases and baselines across single and multi-threaded modes.
- Collaborated with developers to debug MTFlex issues (turbo/EV mismatches, rule-group sequencing); enhanced pre-run environment validation to ensure PERC LOAD options and LDL scopes are consistently honored.
- Automated regression setup using Bash/Tcl and Python covering testcase checkout, configuration validation, and log analysis to cut setup/debug effort by **20%** and improve nightly stability by **15%**.
- Upgraded the internal *perc checkIn script* to include broader validation scenarios and output checks, reducing configuration errors and streamlining regression submissions.
- Implemented distributed job-submission workflows (Terra) for multi-configuration regressions with priority tuning and automated post-run KPI reporting, improving visibility into runtime and memory performance.
- Expanded test coverage with new edge case and baseline suites for 3DIC and hierarchical verification, improving regression accuracy and reducing false negatives.
- Analyzed large scale regression data to track runtime, memory, and testcase reliability; generated KPI dashboards used in release-readiness reviews.
- Reproduced and validated customer-reported issues on internal builds, supplying detailed testcase evidence and configuration documentation to assist R&D triage.
- Validated sequential and distributed execution flows to confirm consistent rule sequencing and tool behavior across software versions.
- Developed infrastructure utilities, including a grid-monitoring prototype for resource-usage tracking and an automated disk-space notifier to prevent job interruptions.
- Authored QA runbooks, grid execution guidelines, and onboarding documentation, reducing new-hire ramp-up time by approximately **30%**.

ADVANCED MICRO DEVICES (AMD), Austin, TX **July 2020 - March 2024**

Product Development Engineer (System-Level Test)

Validated SoCs at the System Level Test stage by developing and executing production test programs to characterize power, voltage, and thermal behavior, ensuring silicon reliability and performance compliance.

- Led post-silicon SLT for Ryzen 8040 APUs across 14+ IPs and multiple platforms, coordinating bring-up through qualification.
- Developed production test programs for electrical/thermal characterization (IR drop, current draw, power margins) to meet spec.
- Automated data capture in Python Jupiter Notebook, cutting manual analysis by **40%** and speeding yield feedback.
- Executed SIDD, margin, and stress screens to flag borderline parts and tighten early screening. Applied DOE to isolate parametric drift; stabilized ramp by optimizing test sequencing for **10%** throughput gain.
- Built Power BI dashboards for KPI tracking; reduced triage and time to completion by **30%**.

RIT SMFL, Rochester, NY **January 2020 - May 2020**

Graduate Research Assistant - Process Engineering
Developed and evaluated semiconductor fabrication processes on Lux Semiconductors's crystalline thin-film substrates, integrating device structures and performing electrical characterization to assess process feasibility.

- Developed a complete thin-film IC process flow within the SMFL cleanroom, covering lithography, deposition, and etch steps.
- Simulated NMOS devices to analyze subthreshold slope and leakage.
- Performed electrical characterization to optimize gate oxide growth and achieve desired device threshold profiles.

ADVANCED MICRO DEVICES (AMD), Austin, TX **July 2019 - December 2019**
Product Engineering Co-Op
Designed and implemented Python-based automation frameworks for ESD characterization systems, integrating equipment control, data acquisition, and GUI interaction to support product qualification and reliability testing.

- Automated Human Body Model ESD test programs; reduced engineering time by **90%**.
- Reverse-engineered the Charge Device Model (CDM) test system GUI and developed Python automation to replace manual test execution, enabling fully automated control and data collection for ESD characterization.
- Performed calibration and waveform verification for preventive maintenance per ISO 9000 procedures.
- Designed DOE for capacitive modeling to optimize protection circuitry and improve first-pass yield.

Key Projects

FOODHUB - DELIVERY BUSINESS INTELLIGENCE SYSTEM

- Analyzed 1,898 food delivery orders from 178 NYC restaurants using Python, identifying $6,166 in commission revenue and proposing insights to cut delivery time by 21% and boost feedback rates to 85%.

ML PIPELINE PROJECT

- Deployed production-ready MLOps solution for SuperKart retail forecasting using Flask REST API backend and Streamlit frontend, containerized with Docker and hosted on Hugging Face Spaces.
- Served real-time sales predictions through scalable microservices architecture processing 8,763+ transaction records with 66.8% model accuracy, supporting quarterly inventory planning.

NATURAL LANGUAGE PROCESSING RAG-POWERED MEDICAL AI ASSISTANT

- Built a RAG-based medical AI assistant using Mistral-7B and a 4,000-page medical manual, leveraging embeddings and ChromaDB to improve accuracy and reduce hallucinations in healthcare decision support.

HELMNET: AI POWERED HELMET DETECTION SYSTEM

- Developed a computer vision safety monitoring system using VGG-16 and CNNs on 631 workplace images, achieving high accuracy in automated helmet detection to improve safety compliance.

PREDICTIVE ANALYTICS PORTFOLIO (LOAN, VISA, AND CHURN MODELS)

- Developed and trained machine learning models using Python on 40,000+ financial and immigration records, applying Gradient Boosting, Decision Trees, and DNNs with SMOTE to achieve 99.3% recall and 81.1% F1-score.

MEMS SILICON MICRO-ROBOT

- Designed and fabricated thermally actuated MEMS micro-robot inside the Semiconductor & Microsystems Fabrication Laboratory (SMFL) cleanroom at RIT, following Class-100/1000 contamination-control procedures.
- Utilized CAD/SolidWorks for device layout and COMSOL Multiphysics for heat-transfer and actuation simulation, validating design feasibility prior to fabrication.

Education And Certifications

Post Graduate Program Artificial Intelligence, Machine Learning **January 2025 - September 2025**
University of Texas at Austin, Online

Master of Science Electrical Engineering **July 2017 - December 2020**
Rochester Institute of Technology, Rochester, NY

Bachelor of Technology Electrical Engineering **July 2012 - May 2016**
Bharati Vidyapeeth University, Pune, India