Chinmay Rozekar

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Professional Summary

Process-oriented engineer with 5+ years across semiconductor validation, fab-adjacent automation, and cleanroom device work (RIT SMFL). Strong with SPC, Cp/Cpk, DOE, tool readiness, and ESD protocol. Builds Python tooling and dashboards for trend detection and change-point triage. Practical AI experience (LLMs, RAG) used to accelerate data analysis and QA automation.

Technical Skills

Languages: Python, Tcl/Tk, Shell, SVRF, C/C++, Perl, Java
Fabrication & Lab Experience: Cleanroom protocol compliance (Class 100/1000), ESD handling, wafer-level diagnostics, probe station and handler operation
EDA/Verification: Calibre PERC, DRC/LVS, LDL, RVE
QA: Regression automation, coverage tracking, rule sequencing/debug, Grid job scheduling (Terra)
Infrastructure & Automation: RHEL/SLES, grid scheduling, queue/priority tuning
AI/ML: TensorFlow, PyTorch, Scikit-learn, Transformers, LLMs, RAG, Embedding Models, Hugging Face
CI/CD: GitHub, CVS, GitLab, Bitbucket, Jira, Confluence, Docker, Jenkins
Development Methodologies: Agile, Scrum, Kanban, Waterfall
Hardware Validation: SoC validation, JTAG, system-level testing, RMA diagnostics
Statistical Analysis: SPC, Cp/Cpk, box plots, parametric yield analysis
Certifications: Calibre PERC (2024), Advanced PERC Rule Writing (2025)

Experience

Software QA Engineer — July 2024 – October 2025

Siemens EDA (Mentor Graphics) — *Wilsonville, OR*

- Execute reliability-verification QA for Calibre PERC (LDL, topology, voltage propagation, point-to-point resistance, current density), maintaining reproducible testcases and baselines across single- and multi-threaded modes.
- Automated regression setup using Bash/Tcl and Python—covering testcase checkout, configuration validation, and log analysis—to cut setup/debug effort by **20%** and improve nightly stability by **15%**.
- Upgraded the internal *perc_checkIn_script* to include broader validation scenarios and output checks, reducing configuration errors and streamlining regression submissions.
- Implemented distributed job-submission workflows (Terra) for multi-configuration regressions with priority tuning and automated post-run KPI reporting, improving visibility into runtime and memory performance.
- Expanded test coverage with new edge-case and baseline suites for 3DIC and hierarchical verification, improving regression accuracy and reducing false negatives.
- Analyzed large-scale regression data to track runtime, memory, and testcase reliability; generated KPI dashboards used in release-readiness reviews.
- Reproduced and validated customer-reported issues on internal builds, supplying detailed testcase evidence and configuration documentation to assist R&D triage.
- Validated sequential and distributed execution flows to confirm consistent rule sequencing and tool behavior across software versions.
- Developed infrastructure utilities, including a grid-monitoring prototype for resource-usage tracking and an automated disk-space notifier to prevent job interruptions.
- Authored QA runbooks, grid-execution guidelines, and onboarding documentation, reducing new-engineer ramp-up time by approximately **30%**.

Product Development Engineer (System-Level Test) — July 2020 – March 2024

Advanced Micro Devices (AMD) — *Austin, TX*

- Led post-silicon SLT for Ryzen 8040 APUs across 14+ IPs and multiple platforms, coordinating bring-up through qualification.
- Developed production test programs for electrical/thermal characterization (IR drop, current draw, power margins) to meet spec.
- Automated data capture and STDF parsing with Python/Perl, cutting manual analysis by **40%** and speeding yield feedback.

- Executed SIDD, margin, and stress screens to flag borderline parts and tighten early screening.
- Applied DOE to isolate parametric drift; stabilized ramp by optimizing test sequencing for **10%** throughput gain.
- Built Power BI dashboards for KPI tracking; reduced triage and time to completion by **30%**.

Product Engineering Co-Op July 2019 – December 2019
Advanced Micro Devices (AMD) *Austin, TX*

- Automated Human Body Model ESD test programs; reduced engineering time by **90%**.
- Performed calibration and waveform verification for preventive maintenance per ISO 9000 procedures.
- Designed DOE for capacitive modeling to optimize protection circuitry and improve first-pass yield.

Graduate Research Assistant — Process Engineering January 2020 – May 2020
RIT Semiconductor & Microsystems Fabrication Laboratory (SMFL) *Rochester, NY*

- Developed a complete thin-film IC process flow within the SMFL cleanroom, covering lithography, deposition, and etch steps.
- Simulated NMOS devices to analyze subthreshold slope and leakage.
- Performed electrical characterization to optimize gate oxide growth and achieve desired device threshold profiles.

Projects

MEMS Silicon Micro-robot

- Designed and fabricated thermally actuated MEMS micro-robot inside the Semiconductor & Microsystems Fabrication Laboratory (SMFL) cleanroom at RIT, following Class-100/1000 contamination-control procedures.
- Utilized CAD/SolidWorks for device layout and COMSOL Multiphysics for heat-transfer and actuation simulation, validating design feasibility prior to fabrication.

FoodHub - Delivery Business Intelligence System

- Conducted comprehensive data analysis of 1,898 food delivery orders across 178 NYC restaurants using Python (pandas, matplotlib, seaborn), identifying $6,166 in commission revenue and delivering 8 specific business recommendations that could reduce average delivery time by 21% (from 28.34 to 22.47 minutes) and potentially increase customer feedback rates from 61% to 85% through targeted engagement strategies

ML Pipeline Project

- Deployed production-ready MLOps solution for SuperKart retail forecasting using Flask REST API backend and Streamlit frontend, containerized with Docker and hosted on Hugging Face Spaces.
- Served real-time sales predictions through scalable microservices architecture processing 8,763+ transaction records with 66.8% model accuracy, supporting quarterly inventory planning.

Natural Language Processing RAG-powered medical AI assistant

- Developed RAG-based medical AI assistant using Mistral-7B LLM and 4,000+ page medical manual, implementing document chunking, vector embeddings (SentenceTransformers), and ChromaDB to achieve high accuracy and reduced hallucinations for healthcare decision support, with LLM-as-judge evaluation showing superior performance over baseline models

HelmNet: AI Powered Helmet Detection System

- Developed computer vision safety monitoring system using VGG-16 transfer learning and CNN architectures on 631 workplace images, implementing data augmentation and achieving high accuracy for automated helmet detection to enhance workplace safety compliance in construction and industrial environments

Predictive Analytics Portfolio (Loan, Visa, and Churn Models)

- Developed multiple machine learning models using Python (scikit-learn, TensorFlow, pandas) across financial and immigration datasets totaling over 40,000 records. Implemented Gradient Boosting, Decision Tree, and Deep Neural Networks with SMOTE oversampling to achieve up to 99.3% recall and 81.1% F1-score. Identified key predictors such as income, education, and wage level for improved targeting, retention, and process optimization.

Education

University of Texas at Austin Online
Post Graduate Program in Artificial Intelligence and Machine Learning *2025*

Rochester Institute of Technology Rochester, NY
Master of Science, Electrical Engineering *2020*

Bharati Vidyapeeth University Pune, India
Bachelor of Technology, Electrical Engineering *2016*