

Chinmay Rozekar

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OBJECTIVE

Post Silicon Validation engineer seeking to apply semiconductor expertise in SPC, MRB, and process optimization towards achieving zero defects and enhancing fab operations.

PROFESSIONAL SUMMARY

- Leveraging 4+ years in Post-Silicon Validation to excel in Defect Metrology, aiming to advance recipe optimization and equipment functionality for superior defect detection.
- Experienced in Fab Technology Process Flow, Device Characterization, and Data Analysis through both coursework and applied projects at RIT's Semiconductor Microsystems Fabrication Laboratory (SMFL).
- Demonstrated expertise in project leadership, effectively reducing costs and enhancing product designs through analytical rigor and proactive equipment oversight.
- Skilled in fostering teamwork across functions, driving advancements in testing methodologies, and ensuring equipment reliability to uphold stringent industry norms.

EXPERIENCE

Product Development Engineer <i>Advanced Micro Devices (AMD)</i>	July 2020 – Present Austin, TX
<ul style="list-style-type: none">• Led system-level testing for AMD's Ryzen 8040 'Hawkpoint' series, Accelerated Processing Units (APUs), ensuring adherence to customer environment standards.• Collaborated with Diagnostic, BIOS, and Design teams to enhance CPU performance features, contributing to product specification improvements.• Spearheaded Test Time Reduction (TTR) analysis, eliminating redundant tests, significantly shortening test cycles, and reducing operational costs.• Innovated a JTAG protocol-based solution for debugging returned parts RMA, enhancing product quality and customer satisfaction.• Established and managed an in-house server farm and APU client board setup, ensuring robust testing environments and streamlining development.• Maintained the test program codebase repository using BitBucket/GIT, overseeing the development and release of test content.	
Product Engineering Co-Op <i>Advanced Micro Devices (AMD)</i>	Jan. 2019 – Dec. 2019 Austin, TX
<ul style="list-style-type: none">• Designed and automated test programs for Human Body Model Testing, reducing Engineering time by 90%.• Reverse-engineered and redesigned a 20-year-old robotic graphical user interface in Python, reducing engineering time by 95%.• Conducted stress tests on AMD products according to industry standards, qualifying products for production.• Performed scheduled calibration and waveform verification for preventive maintenance as per ISO 9000 standards• Conducted Design of Experiments on AMD products for Capacitive Modeling to optimize protection circuitry	
Graduate Research Assistant <i>Rochester Institute of technology</i>	Jan 2020 – May 2020 Rochester, NY
<ul style="list-style-type: none">• Developed a process flow for thin film IC development, covering various fabrication steps such as Dry Etch, Wet Etch, Ion Implantation, PVD and CVD.• Designed and simulated NMOS devices to determine sub-threshold voltages and model transistor leakage current• Conducted electrical device characterization and Meterology to optimize gate oxide thickness on NMOS devices.	

TECHNICAL SKILLS

Languages: Java, Python, BASH, C/C++, SQL, HTML/CSS, XML, Markdown, MATLAB, Perl

Libraries: Matplotlib, Pandas, Numpy, Scikit-learn, Selenium

Developer Tools: Git, Jira, Confluence, Linux, CI/CD, IntelliJ Idea, VS Code, PyCharm, Eclipse, Jupyter, Anaconda, JSON, Notepad++, LaTeX

Protocols: JTAG, PCIE, DFT, Boundary SCAN, ATPG

Simulation: KiCAD, SolidWorks, COMSOL Multiphysics, Silvaco-Athena, Pyxis(Mentor Graphics)

Data Analysis: Excel, Power-BI, JMP, Python

PROJECTS

Review of Thin Film Technologies for Flexible Electronics	Jan 2020 – May. 2020
• Designed a simulation model for growing a 1 μm layer of flexible crystalline Si substrate on top of Tungsten metal layer using SOI method in Silvaco Athena.	
A Thermally actuated four-legged MEMS based Silicon Micro-robot	May 2018 – Dec. 2018
• Designed and fabricated a thermally actuated MEMS based Silicon micro-robot. Modeled design in CAD / Solidworks and Heat Transfer using COMSOL multi-physics FEA.	

EDUCATION

Rochester Institute of Technology	Rochester, NY
<i>Master of Science, Electrical Engineering</i>	<i>Aug. 2017 – May 2020</i>
Bharati Vidyapeeth University	Pune, India
<i>Bachelor of Technology, Electrical Engineering</i>	<i>Aug. 2012 – June 2016</i>