Chinmay Rozekar

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Professional Summary

- Versatile engineer with 4+ years in Silicon Validation, adept in both Pre-Silicon and Post-Silicon environments, specializing in system-level testing and product quality enhancement.
- Committed to leveraging technical expertise for reducing operational costs and enhancing product specifications.
- Excels in cross-functional team collaboration, test automation with Python, C/C++, and Java, and innovative problem-solving.

Experience

Product Development Engineer July 2020 – March 2024

Advanced Micro Devices (AMD) *Austin, TX*

System Level Testing (SLT)

- Led system-level testing for AMD's Ryzen 8040 'Hawkpoint' series Acclerated Processing Units (APU's) in Java and Linux, designing and overseeing 100+ test scenarios to test and validate 14 SoC IPs.
- Spearheaded Test Time Reduction (TTR) initiative, eliminating 10% of redundant tests and reducing operational costs by 5% through detailed DPPM Yield Analysis in Production.
- Generated detailed test reports, collected parametric data for voltage, frequency, and thermal plots, leading to a 10% improvement in product reliability over 3 release cycles.
- Analyzed failure logs and debugged issues, creating and tracking JIRA tickets and leveraging Confluence for documentation. Timely escalated critical issues and collaborated with cross-functional teams across different time zones to ensure swift resolutions.
- Collaborated in SoC design changes and dynamically revised test plan strategies, identifying early-stage software bugs. Proactive contributions led to significant refinements in test content, boosting overall quality and reliability
- Led defect management efforts, categorizing low Sidd (Static Idd) marginal units from Typical-Typical (TT)/ fast units, and conducted SoC characterization on marginal units to pinpoint stress tests that caused IP failures. Utilized box plots to verify if VF values met product specifications.
- Effectively managed customer RMA issues by diagnosing and resolving the majority of hardware failures in-house, minimizing escalations. Contributed to root cause analyses and documentation in RMA meetings, enhancing product reliability and customer trust.

Product Engineering Co-Op Jan. 2019 – Dec.2019

Advanced Micro Devices (AMD) *Austin, TX*

- Designed and automated test programs for Human Body Model Testing, reducing Engineering time by 90%.
- Reverse-engineered and redesigned a 20-year-old robotic graphical user interface in Python, reducing engineering time by 95%.
- Conducted ESD High Voltage stress tests on over 50 AMD GPU server products to verify latchup events, ensuring compliance with JEDEC standards and securing their qualification for mass production.
- Performed scheduled calibration and waveform verification for preventive maintenance as per ISO 9000 standards
- Conducted Design of Experiments on AMD products for Capacitive Modeling to optimize protection circuitry

Graduate Research Assistant Jan 2020 – May 2020

Rochester Institute of technology *Rochester, NY*

- Developed a process flow for thin film IC development, covering various fabrication steps
- Designed and simulated NMOS devices to determine sub-threshold voltages and model leakage current
- Conducted electrical device characterization to optimize gate oxide thickness on NMOS devices.

Technical Skills

Process Engineering: Thin Films, PVD, CVD, Sputtering, Dry Etch, Metrology, Characterization
Languages: Verilog, Python, Java, BASH, C/C++, SQL, HTML/CSS, XML, Markdown, MATLAB, Perl
Libraries: Matplotlib, Pandas, Numpy, Scikit-learn, Selenium
Developer Tools: Git, Jira, Confluence, Linux, CI/CD, IntelliJ Idea, VS Code, PyCharm, Eclipse, Jupyter, Anaconda, JSON, Notepad++, LaTeX
Protocols: JTAG, PCIE, DFT, Boundry SCAN, ATPG
Simulation: ModelSim, KiCAD, SolidWorks, COMSOL Multiphysics, Silvaco-Athena, Pyxis(Mentor Graphics)
Data Analysis: Statistical Process Control (SPC), Cp, Cpk, R, Excel, Power-BI, Python

Projects

Review of Thin Film Technologies for Flexible Electronics Jan 2020 – May. 2020

- Designed a simulation model for growing a 1 µm layer of flexible crystalline Si substrate on top of Tungsten metal layer using SOI method in Silvaco Athena.

A Thermally actuated four-legged MEMS based Silicon Micro-robot May 2018 – Dec. 2018

- Designed and fabricated a thermally actuated MEMS based Silicon micro-robot. Modeled design in CAD / Solidworks and Heat Transfer using COMSOL multi-physics FEA.

Education

Rochester Institute of Technology Rochester, NY
Master of Science, Electrical Engineering *Aug. 2017 – May 2020*

Bharati Vidyapeeth University Pune, India
Bachelor of Technology, Electrical Engineering *Aug. 2012 – June 2016*