Micron Interview Prep

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1 DDR Memory

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2 questions based on my Resume

1. **Can you walk us through your role in system-level testing for AMD's Ryzen 'Hawkpoint' series and how it prepared you for a role at our company?**

   (a) I work as a Product Development Engineer at in System Level Test (SLT) and it is my job to successfully oversee the entire lifecycle of the product from Tape out to Production.

   (b) In my Role as a Product Development Engineer, I wear various hats. During Tape out and Bring up I am responsible for Characterization activities which include figuring the baseline curves and values for Vmin and Fmax for the product in the IRM spec thus aiding Product Defination.

   (c) I am responsinble for performaing LAE (Limiting Application Experiment) Charz to figure out the most limiting diagnostic tests / stressors on the product IP and characterize them.

   (d) Basically at SLT/ Prod Def. we test our Chips in mission mode as a customer would run our parts out in the field, but we test them aggressively

   (e) All our parts are Tested in a Linux Environment and we utilize software stacks like BIOS, device drivers, and firmware that are released to the custonmer

   (f) basically if you see it this way, ATE tests for scan, MBIST, CREST, ATPG and a few other tests to insure that 99.5% of the test coverage is covered in the test.

   (g) At SLt we catch that 0.5% of the failures before the parts go out in the field

   (h) I am also responsible for continuous yield monitoring and Data Analysis, monitoring yield drops package by package per product, rootcausing / debugging any issues that are repponsible for a yield fallout by making Pareto charts.

   (i) And lastly I am responsinle for TTR (Test Time reduction) activities in our software Testprogram suite, scavenging for any seconds I can save to bring down testter time because time is money.

(j) I believe this experience has trained me think methodically and always look for the bigger picture in terms of product Def. I also gained a lot of ecperience working with crossfunctional teams in differnt timezones defining mission critical deadlines which I believe would be a great asset in this role as well.

2. **How did you achieve test time reduction (TTR) and what impact did this have on operational costs and DPPM yield analysis?**

   (a) Thanks for the question Tete, So the purpose of TTR is to reduce the Test time in the software stack by weeding out tests that either have a test time of < 1 sec. or had a DPPM value of 0

   (b) The way I do this is I look up Production data from last 60 days of our products across all packages. This data is arounf 50,000 units.

   (c) Then I look at what are the commonn low DPPM diagnostic test across all packages and present it to the SoC IP owners. If I get a confirmation from Design team and Leadership that removing them from the stack will not have any impact on the coverage, I remove them from the SLT Test flow.

   (d) These Tests are usually some redundant tests that are targetting the same IP or have been in the software stack from previous products.

   (e) We have a DPPM calculator that does the DPPM calculation for us but iDPPM calculation is pretty simple, I mean its :

$$\text{DPPM} = \left(\frac{\text{Defects Observed}}{\text{Total Size of the Sample or Population}} \right) \times 10^6 \tag{1}$$

   Example, In a total of 500 units, 5 objects were rejected for some reasons. Hence,

$$\text{DPPM} = \left(\frac{5}{500} \right) \times 10^6 \tag{2}$$

$$= \left(\frac{1}{100} \right) \times 10^6 \tag{3}$$

$$= 10,000. \tag{4}$$

3. **Describe a challenging production yield issue you faced and how you performed root cause analysis to resolve it.**

   (a) Excellent Question Tete, In the last quarter we had 2 APU products Phoenix and Hawkpoint (This is public so I can talk about it) which are from the same SoC family and same FP7r2 package respectively

   (b) So basically they were the same package.

   (c) But what happened was there was a sudden 40% yield gap between the two test programs that were in the production.

   (d) First I ran a control group of 50 HPT units as baseline and did a bios/ FW regression between all the recent FWs that were released

(e) This proved my hypothesis that one of the FW that was causing this as it was impacting control and power delivery

(f) Next I set up meetings with Design team and IP architects and designed few experiments where I turned off features in the IP one by one like changing the limits on EDC, AFLL, CLDO etc and played around with the Latch up voltage limits,

(g) Next I did a temperature study and fixed some Temperature issues where we were understesting or Overtesting our parts in the flow. Basically I had to do a deep dive into our codebase for this.

(h) Basically, it turned out that the test on which we were seeing failures was running too aggressively and hence throttling, which is why we had to switch to a low CaC workload and relax some of our guardbands and this fixed our issue.

4. **Can you explain the process of SoC Characterization for Product Definition and how it influenced product specifications**

(a) When it comes to Characterization, In the entire Product Development, Chracterization happens on both ATE as well as SLT

(b) ATE charz is quick as it has a shorter run time but SLT charz takes a bit longer.

(c) In Both Charz we do Freq/ Voltage sweep search. On ATE charz it is scan, Bist, Func/ IO. On SLT Charz we do F/V searches on most limiting tests and applications

(d) First we identify IP / Voltage rail and the clock domain to characterized based on prod spec. eg. CoreClk runs on V_{dd}CPU rail.. GFXCLK runs on V_{dd}GFX rail and FCLK runs on V_{dd}SOC rail.

(e) Next we we need to take into account that we characterize for a whole range for temperatures that we have guranteed to the both hot and cold. cold is 25C and hot is 95C

(f) The next step is to figure out the applications that we are going to run in the Charz based on the IP

(g) The most imp thing is to determine what material you are using for charz, these coud be TT, FF SS, FS, SF material baseed on the wafer

(h) Next thing is we disable some parameters in BIOS/ FW such as Thermal Slew rate for faster thermal response, we disable DFLL for Droop mitigation and enable DFLL for better Freq control

(i) The next step is to run these application in a form aof a burst flow to calculate Vmin and Fmax data points to form a curve or a bounding box.

(j) This bounding box serves as a skeleton for Product Defination

5. **Discuss your experience with Atlassian BitBucket and how you used it to manage the test program codebase repository.**

(a) At AMD, I used BitBucket to oversee our test program codebase, ensuring streamlined development and timely release processes across the product lifecycle.

(b) My role involved maintaining the repository, managing code reviews, and integrating changes.

(c) I audited thesoftware stack, and made sure misssion critical S/W and F/W updates were checked into the codebase during major product milestones

(d) This experience sharpened my skills in version control and team collaboration, facilitating efficient and error-free updates to our testing protocols

(e) It was crucial for enhancing CPU performance features and supporting cross-functional team efforts, demonstrating my capability to manage complex codebases in a dynamic development environment

6. **Detail a customer RMA debug issue you encountered and how you resolved it through secure fuse unlocking.**

(a) We recently encountered an RMA issue from customer which has multiple problems. We had 3 customer returns.

(b) The first issue was that the prefrred cores were failing in the customer systems and the second issue was that the customer was facing a GFX hang which resulted in a BlueScreen of Death.

(c) We ususally handle RMA issues through our TestPrograms, but since it was an unrgent issue, I had to mannuly debug it

(d) First I unlocked the part using a Wombat and JTAG interface, overriding the secure fuses

(e) I ran our n Threaded performance workload and GFX workload in mission mode settings to see if there is a problem with our workload or F/W.

(f) Next I ran our n threaded CPU workloads with our GFX workloads concurrently to see if that replicates the issue since running it concurrently would stress the part even more, but that was not the case

(g) Next I replaced our N Threaded workload for a lower Cac workload and ran GFX workload concurrently, to see if the workload itself was the problem but that wasnt the problem either

(h) Next I synced with the GFX DLDO team to change the DLDO tuning and to see if lowering the voltage can help us

(i) we went back and forth trying differnt voltage settings between previous products and ultimatly figured out that GFX DLDO tuning was not updated from previous process nodes which led to GFX hang issues.

(j) And we also discovered that one of the units had a metal speedpath issue.

7. **What was your approach to establishing and managing an in-house server farm and APU client board setup?**

(a) So our Team's SLT server which hosted our files and OSLT environmet was reaching its end of life

(b) So I made a server rack local to our team so that multiple SLT test beches can be stacked anf hosted together thus saving space

(c) we had a AMD EPYC server CPU's lying around from server team so I synced with my lab manager and ordered a Super Micro ATX board and built a server and installed Linux on it.

(d) I installed Virtual Box for VM environment for each SLT Testbenches and installed OSLT RedHat OS on it.

(e) The challenging part was to figure out the correct Network IP's and to setup DCHP for each bench.

(f) Once that was done, I installed Dediprog on the main server and wrote anautomation script that would automatically flash bios on all the Test bench, This enabled remote bios flashing for my team which previously someone has to manually go into the lab to do so.

(g) This improved team productivity.