Chinmay Rozekar

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Professional Summary

Software QA Engineer with 5+ years in semiconductor design validation (Siemens EDA, AMD). Experienced in regression automation, SoC validation, and data-driven QA optimization using Python, TCL, and Linux.

Technical Skills

Languages: Shell, Python, TCL/TK, SVRF, C/C++, Perl
AI/ML: TensorFlow, PyTorch, Scikit-learn, Pandas, NumPy, OpenCV, Transformers, RAG Pipelines
CI/CD: GitHub, CVS, Gitlab, Atlassian BitBucket, Jira, Confluence, Docker
Development Methodologies: Agile, Scrum, Kanban, Waterfall
QA & Verification: Test Automation, DRC, LVS, Calibre PERC, Regression Validation, Rule Debugging
Hardware Validation: SoC Validation, JTAG, PCIe, System-Level Testing
Statistical Analysis: SPC, Cp/Cpk, Box Plots, Parametric Yield Analysis
Certifications: *Calibre PERC (Siemens Software, 2024)*; *Advanced PERC Rule Writing (Siemens Software, 2025)*

Experience

Software QA Engineer July 2024 – Present
Siemens EDA (Mentor Graphics) *Wilsonville, OR*

- Validated Calibre PERC features for reliability verification (ESD, EOS, and topology-based checks) across customer-scale IC designs, ensuring consistent rule behavior and deterministic sign-off results.
- Developed and maintained SVRF-based testcases to verify Logic-Driven Layout (LDL) functionality including current-density, point-to-point resistance, and device-topology checks.
- Created regression validation designs to verify cell recognition accuracy and rule consistency across PERC feature updates.
- Analyzed runtime and memory performance of Calibre PERC under single-threaded, multi-threaded, and MTFlex (distributed) execution modes; identified scaling bottlenecks and supported performance optimization.
- Automated repetitive QA tasks (testcase cloning, export management, log parsing) to reduce manual validation time by ˜20% and improve reproducibility across monthly regression runs.
- Collaborated with developers to diagnose rule-sequencing and execution anomalies, validating correctness of sequential and parallel rule groups in the PERC framework.
- Delivered clean regression baselines with more than 90% testcase coverage, directly supporting quarterly Calibre PERC product releases and customer reliability decks.
- Created a Python tool to compare Calibre PERC output files using regex parsing, enabling structured validation of rule attributes, improving traceability, and reducing manual QA effort across regression cycles.

Product Development Engineer July 2020 – March 2024
Advanced Micro Devices (AMD) *Austin, TX*

- Led system-level testing for AMD's Ryzen 8040 'Hawkpoint' series Accelerated Processing Units (APUs), designing and overseeing 100+ test scenarios to test and validate 14 SoC IPs.
- Spearheaded Test Time Reduction (TTR) initiative, eliminating 10% of redundant tests and reducing operational costs by 5% through detailed DPPM Yield Analysis in Production.
- Generated detailed test reports, collected parametric data for voltage, frequency, and thermal plots, leading to a 10% improvement in product reliability over 3 release cycles.
- Analyzed failure logs and debugged issues, creating and tracking JIRA tickets and leveraging Confluence for documentation. Promptly escalated critical issues and collaborated with cross-functional teams across different time zones to ensure swift resolutions.
- Collaborated in SoC design changes and dynamically revised test plan strategies, identifying early-stage software bugs. Proactive contributions led to significant refinements in test content, boosting overall quality and reliability.
- Led defect management efforts, categorizing low Sidd (Static Idd) marginal units from Typical-Typical (TT)/ fast units, and conducted SoC characterization on marginal units to pinpoint stress tests that caused IP failures. Utilized box plots to verify if VF values met product specifications.
- Effectively managed customer RMA issues by diagnosing and resolving the majority of hardware failures in-house, minimizing escalations. Contributed to root cause analyses and documentation in RMA meetings, enhancing product reliability and customer trust.

PROJECTS

EasyVisa - US Visa Approval Prediction

- Developed ensemble machine learning models for US visa approval prediction using 25,480 applications with 12 features, implementing Gradient Boosting with SMOTE oversampling to achieve 73.6% accuracy and 81.1% F1-score, identifying education level and prevailing wage as key approval factors for OFLC certification process optimization
- **Repository:** github.com/chinmayrozekar/PGPAIML_UT_Austin

Neural Network-Based Customer Churn Prediction

- Built deep neural network models for bank customer churn prediction using TensorFlow on 10,000 customer records, implementing SMOTE oversampling and comparing SGD vs Adam optimizers to achieve optimal recall performance for early churn detection and proactive customer retention strategies
- **Repository:** github.com/chinmayrozekar/PGPAIML_UT_Austin

Natural Language Processing RAG-powered medical AI assistant

- Developed RAG-based medical AI assistant using Mistral-7B LLM and 4,000+ page medical manual, implementing document chunking, vector embeddings (SentenceTransformers), and ChromaDB to achieve high accuracy and reduced hallucinations for healthcare decision support, with LLM-as-judge evaluation showing superior performance over baseline models
- **Repository:** github.com/chinmayrozekar/PGPAIML_UT_Austin

HelmNet: AI Powered Helmet Detection System

- Developed computer vision safety monitoring system using VGG-16 transfer learning and CNN architectures on 631 workplace images, implementing data augmentation and achieving high accuracy for automated helmet detection to enhance workplace safety compliance in construction and industrial environments
- **Repository:** github.com/chinmayrozekar/PGPAIML_UT_Austin

ML Pipeline Project

- Deployed production-ready MLOps solution for SuperKart retail forecasting using Flask REST API backend and Streamlit frontend, containerized with Docker and hosted on Hugging Face Spaces.
- Served real-time sales predictions through scalable microservices architecture processing 8,763+ transaction records with 66.8% model accuracy, supporting quarterly inventory planning.
- **Repository:** github.com/chinmayrozekar/PGPAIML_UT_Austin

Thin Film Technologies for Flexible Electronics

- Conducted comprehensive review of thin film materials and fabrication techniques for next-generation flexible electronic devices, focusing on material properties and integration challenges.

MEMS Silicon Micro-robot

- Designed and fabricated thermally actuated MEMS micro-robot using CAD/SolidWorks design and COMSOL multi-physics simulation for heat transfer analysis.

RESEARCH & CLEANROOM EXPERIENCE

Graduate Researcher – Semiconductor & Microsystems Fabrication Laboratory (SMFL)
Rochester Institute of Technology *Rochester, NY*

- Executed microfabrication processes in a Class 100/1000 cleanroom environment, adhering to contamination control and safety standards.
- Operated CVD, PVD, photolithography, and etching equipment for thin-film deposition and MEMS prototyping.
- Performed wafer cleaning, mask alignment, and metrology (profilometry, ellipsometry) for process characterization and yield analysis.
- Gained comprehensive exposure to fab protocols, vacuum systems, and preventive maintenance procedures applicable to production fabs.

EDUCATION

University of Texas at Austin Online
Post Graduate Program in Artificial Intelligence and Machine Learning (Part-Time) *2025*
Rochester Institute of Technology Rochester, NY
Master of Science, Electrical Engineering *2020*
Bharati Vidyapeeth University Pune, India
Bachelor of Technology, Electrical Engineering *2016*