CHINMAY ROZEKAR (valid H1-B visa, **Authorized to Work in USA, Available to start Immediately**)
7216 GRAY CATBIRD DR. AUSTIN TX 78744 | (646) 510-5699 | chinmay.rozekar@gmail.com | www.linkedin.com/in/chinmayrozekar

EDUCATION

Rochester Institute of Technology, *Rochester, NY* ***Aug 2017 - May 2020***
Master of Science in Electrical Engineering*Microelectromechanical Systems (MEMS)*
Courses taken: Microelectronic Fabrication, Microelectromechanical Systems, Thin Films, Principles of Robotics
BHARATI VIDYAPEETH UNIVERSITY, Pune, India ***Aug 2012 – June 2016***
Bachelor of Technology Electrical Engineering

SKILLS:

Hardware Description and programming languages: Verilog, Java, Python, MATLAB, C C++, Bash Scripting, Perl, SQL, XML
Tools: GitHub, Linux, Confluence, JIRA, COMSOL, SolidWorks, Silvaco Athena, Power BI, JMP
Protocols: JTAG, I2C, PCIE, HBM, DDR PHY, Post Si Validation

WORK EXPERIENCE

Product Development Engineer 2 | ADVANCED MICRO DEVICES, AUSTIN, TX ***July 2020 – Present***

- Led product SoC bring-up, test program development, and hardware debug, including pattern generation using HDT and JTAG, built inhouse server farm for APU client team, which involved inventory management, network configuration, and hardware/software installation for AMD APU client boards.
- Managed product data analysis for yield improvement, developed test programs for customer return and RMA validation with BKM strategies, and designed experiments to enhance yield, ensuring comprehensive data analysis and automation tool development for efficient reporting.
- Coordinated closely with cross-functional teams during silicon bring-up to boost IP yield, served as the point of contact between diagnostic teams in Asia and PDG in Austin for test content management, and maintained active involvement in system level production test program updates.
- Oversaw program releases for key product milestones, handled test program checkout throughout the product cycle via rigorous hardware and software validation, and ensured the resolution of debug tickets during test program integration and testing.
- Maintained the test program codebase repository using BitBucket/GIT, was responsible for the development and release of test content throughout product roadmap.

Product Engineering Co-Op Engineer | ADVANCED MICRO DEVICES, AUSTIN, TX ***Jan. 2019 – Dec. 2019***

- Designed and developed test programs, and patterns for reliability testing and reduced Engineering time for Human Body Model Testing for Electrostatic Discharge Tests (ESD) by 90% by automating manual test program development in Python.
- Reduced engineering time on ESD, Charged Device Model (CDM) testing by 95 % by reverse engineering and redesigning a 20-year-old robotic graphical user interface in Python and conducted stress tests on AMD products for HBM, CDM and Latch up tests according to JDEC and JS002 industry standards to qualify AMD products to the SLT, sustaining teams and production.
- Performed scheduled calibration and waveform verification for preventive maintenance as per ISO 9000 standards and Conducted Design of Experiments on AMD products for Capacitive Modeling to find the rise in peak currents to design better protection circuitry.

Graduate Student Researcher | ROCHESTER INSTITUTE OF TECHNOLOGY, Rochester, NY ***Jan. 2020 – May. 2020***

- Created a process flow for developing thin film IC which included photolithography, metal deposition, wet and dry etching, ion implant, and diffusion for an industry research project to develop integrated circuits for Flexible Electronics technology
- Designed and simulated 10 µm, 1 µm and 0.5 µm channel long NMOS devices to determine sub-threshold voltages and model leakage current for the NMOS devices to determine the thickness of the oxide layer in the fabrication process.
- Designed and performed electrical device characterization to decide on the thickness of the gate oxide on NMOS devices.

PROJECTS

- Review of Thin Film Technologies for Flexible Electronics : Designed a simulation model for growing a 1 µm layer of flexible crystalline Si substrate on top of Tungsten metal layer using SOI method in Silvaco Athena.
- A Thermally actuated four-legged MEMS based Silicon Micro-robot : Designed and fabricated a thermally actuated MEMS based Silicon micro-robot

CERTIFICATION

Computer Architecture with Industrial RISC-V Core (RVfpga), edX