. E. Cumbery Module - 1 Assignment -1 A 297 Hdl Bids \* Learned the Basics of HDLs like Verilag . & untitand how Holls are used to digital circuits at various levels of abstraction. \* Explaned methodologies like I stanchoal Adea book on the 21 Behavioural

21 RTU (Register Transfer level) \* Simulation and ventication Synthesis and Implementation Timing and constraints Some Real world Examples 712-hour cluck Understand waiting test Bench. JERM SITAG - 1 Day fuse sin France.

Assignment - 2 Jodule -1 F PG A Issignmend -1 classification of Ic's & Lecaned the Beside of the Visity in believed to deside to desided to desided to desided to desided to deside to spram spational bacalque & why were need FPGIA Prouds we to 12 Basics of PLD Location of Les fred - All possible commercion article program and after program pagam't wer pagam passed unwited signals were Blown off Blode Diagram of PPGA; sons bous prinit To Block and -> CLB ( ) Ilo Blocke ) Inforcement sold -> SRAM -> JTAG -) Andifuse -> Flash FIDGA.

-> La Jancyo -> Throughput. alli-Learned what was the difference of Asics 7 Fmax Finally: > From have different process of waitings codes and dest terch. -> understand the Design flow of FPGLAS. Design Enlay
Design Syndhesis Simulation Functional smuleton Implementation J. Bbcle Annotation -) Implemented Different Examples from HDL bits and understand In FPGA Design and Utilization.