Module 2

Axi stream Interface

→ consists different signals

↳ mainly Read and write transactions

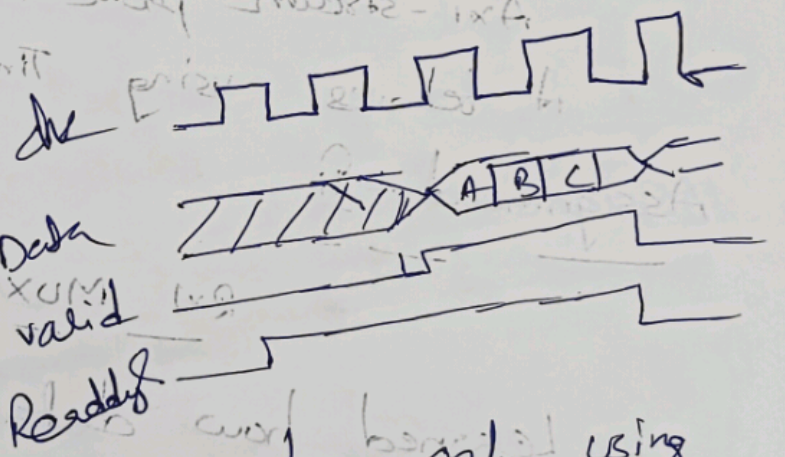
* Data
* valid
* Ready (optional)

↳ other signals

* Last
* keep
* USER
* DEST
* SRTB
* TID

Hand shaking :-

→ understand different hand shaking mechanism



→ Implement different examples only using Data, valid, Ready and Last signals.

→ when valid is low, Data is not transfer because Data is not valid data.

Assignment - I

Register

↳ data storage element can receive data from Axi master provide to Axi slave.

↳ used to minimize propation delay

↳ understand the how Latency should work.

↳ Implement small example based on Axi-stream protocal. understand how it behaves. using Timing circuits/schematic and utilization report.

Assignment - II

2x1 MUX

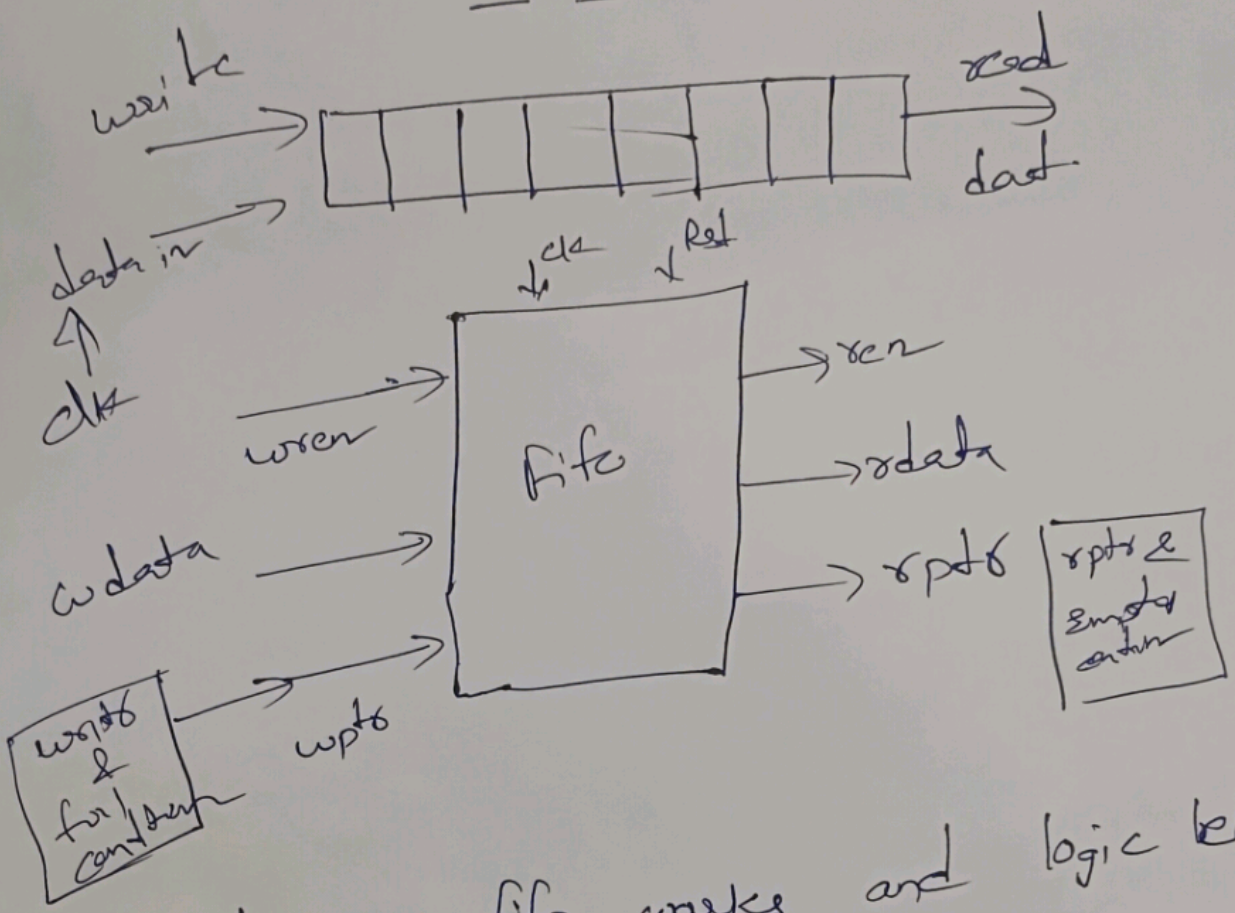
↳ Learned how data differs based on selection lines. and additionally dealt with Axis protocal.

↳ writing testbench based on posedge/negedge clks.

↳ understand what errors will get if we use #delay. in module design.

Assignment - III

Fifo (fisrt input fisrt out)



→ Learned how fifo works and logic behind the fifo design.

→ Added Axi-stream signals to normal fifo and tested.

→ constructed 1-fifo using 2-fifos.

→ understand when B-RAM takes place in FPGA utilization.

→ In test Benches, how files access for input and comparing output data with sim original output understand.