Module - 1

Assignment - 1

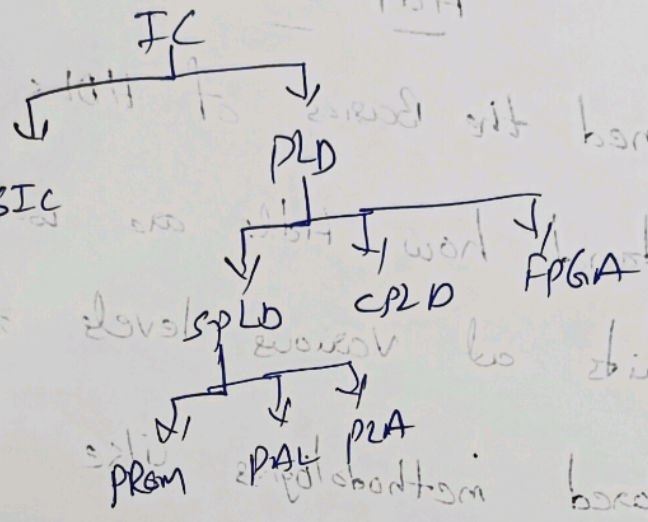
Hdl Bits

* Learned the Basics of HDLs like Verilog
* understand how Hdls are used to digital circuits at various levels of abstraction.
* Explored methodologies like
  1] structural
  2] Behavioural
  3] RTL (Register Transfer level)
* Simulation and verification
* Synthesis and Implementation
* Timing and constraints
* Some Real world Examples → 12-hour clock
* Understand writing test Bench.

Assignment - 2

FPGA

classification of Ic's



why we need FPGA ?

Basics of PLD

fixed :- All possible connection available before program and after program

program :- when program passed unwanted signals are blown off

Block Diagram of FPGA :

→ I/O Blocks
→ CLB
→ Interconnects / pip

→ SRAM
→ Antifuse
→ Flash FPGA

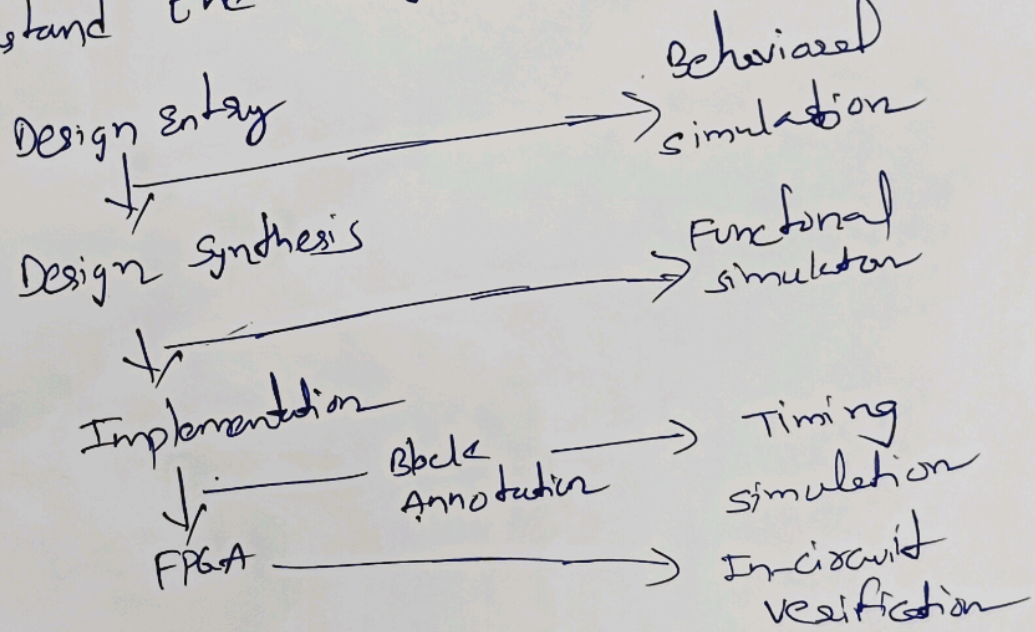
→ JTAG

→ Latency
→ Throughput.
→ Fmax.

Finally:
Learned what was the difference of Asics and FPGAs.

→ FPGAs have different process of writing codes and test bench.

→ understand the Design flow of FPGAs.



→ Implemented Different examples from HDL bits and understand the FPGA Design and utilization.