Multiprocessors

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Interconnection Structure

Introduction

- The components that form a multiprocessor system are CPUs, IOPs connected to input-output devices, and a memory unit.
- The interconnection between the components can have different physical configurations, depending on the number of transfer paths that are available
  - Between the processors and memory in a shared memory system
  - Among the processing elements in a loosely coupled system

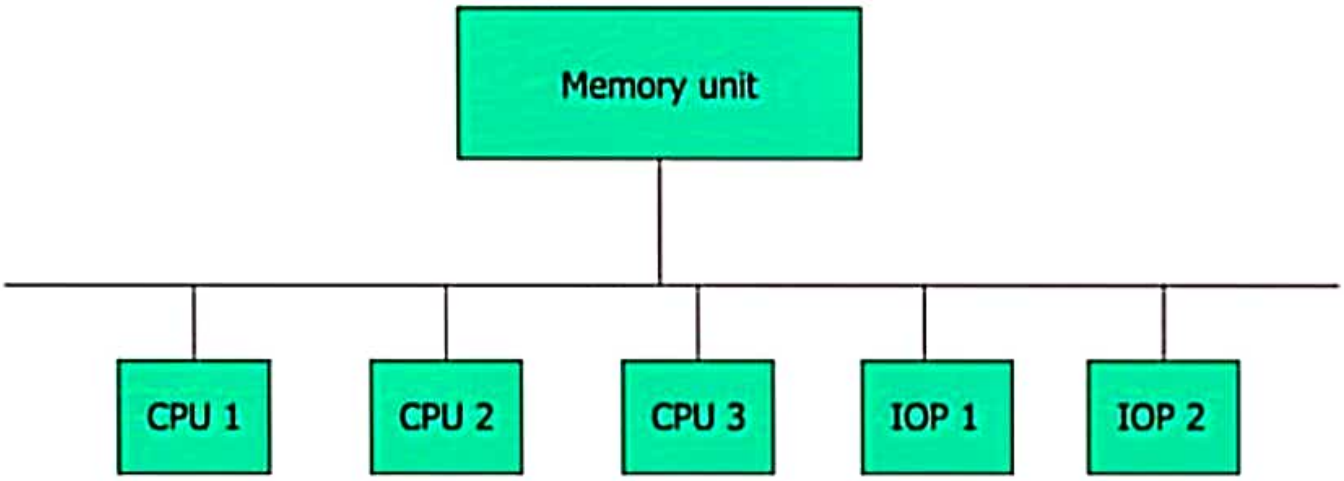
Introduction(*cont.*)

- There are several physical forms available for establishing an interconnection network.
  - Time-shared common bus
  - Multiport memory
  - Crossbar switch
  - Multistage switching network
  - Hypercube system

Time-shared common bus

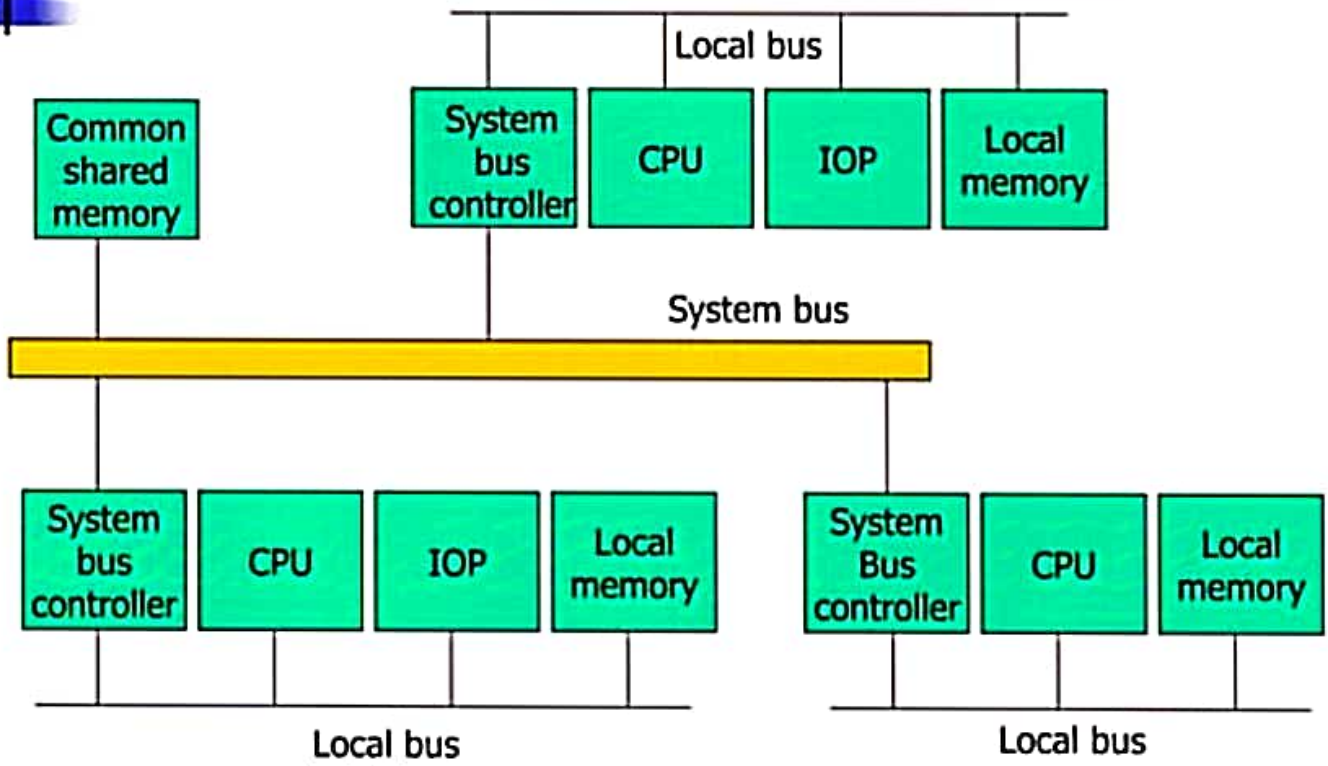
- A common-bus multiprocessor system consists of a number of processors connected through a common path to a memory unit.
- *Disadv.*:
  - Only one processor can communicate with the memory or another processor at any given time.
  - As a consequence, the total overall transfer rate within the system is limited by the speed of the single path
- A more economical implementation of a dual bus structure is depicted in Fig. 2.
- Part of the local memory may be designed as a *cache memory* attached to the CPU.

Time-shared common bus organization



System bus structure for multiproces

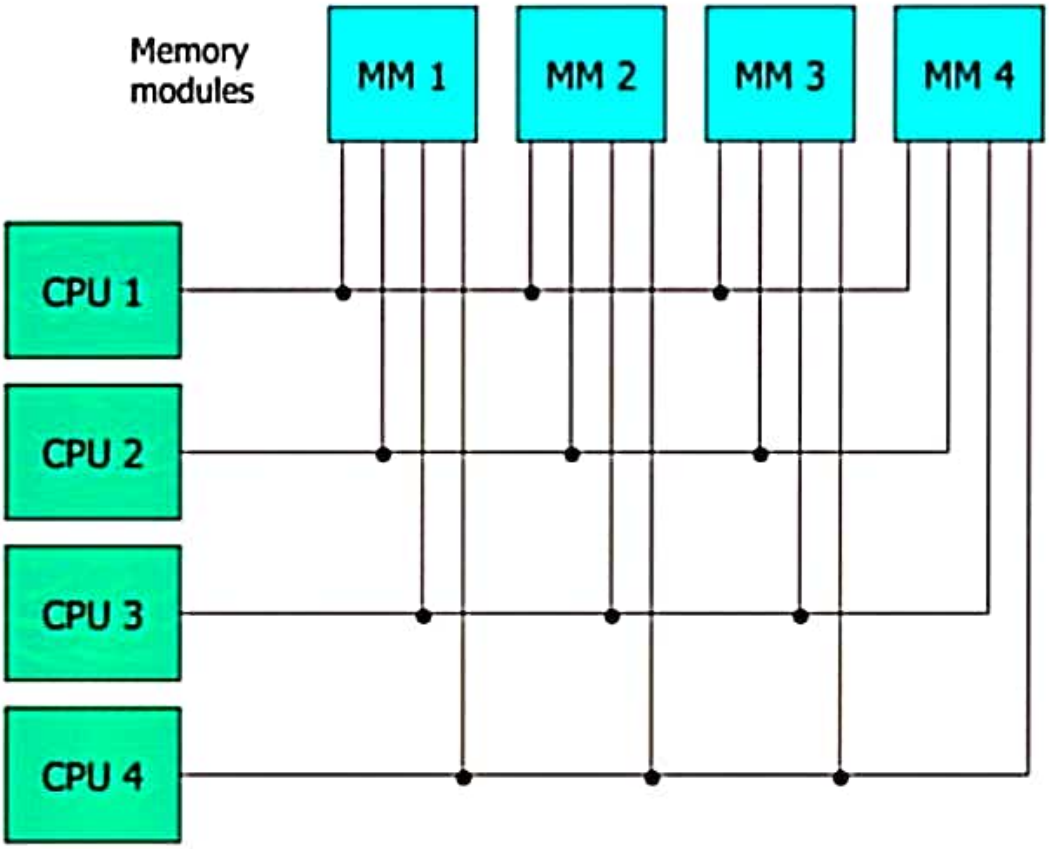
Fig. 2



Multiport memory

- A multiport memory system employs separate buses between each memory module and each CPU.
- The module must have internal control logic to determine which port will have access to memory at any given time.
- Memory access conflicts are resolved by assigning fixed priorities to each memory port.
- *Adv.*:
  - The high transfer rate can be achieved because of the multiple paths.
- *Disadv.*:
  - It requires expensive memory control logic and a large number of cables and connections

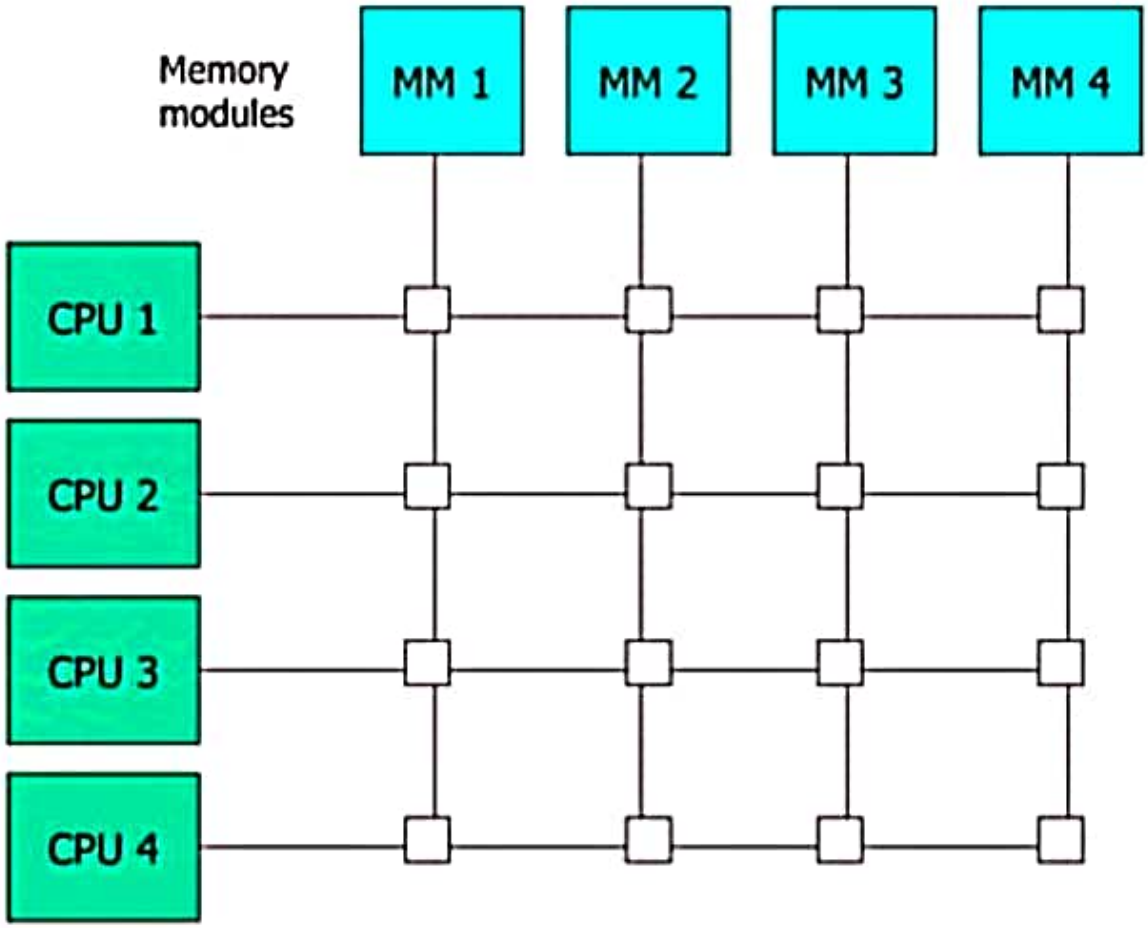
Multiport memory organization



Crossbar switch

- Consists of a number of *crosspoints* that are placed at intersections between processor buses and memory module paths.
- The small square in each crosspoint is a *switch* that determines the path from a processor to a memory module.
- Adv.:
  - Supports simultaneous transfers from all memory modules
- Disadv.:
  - The hardware required to implement the switch can become quite large and complex.
- Fig. 5 shows the functional design of a crossbar switch connected to one memory module.

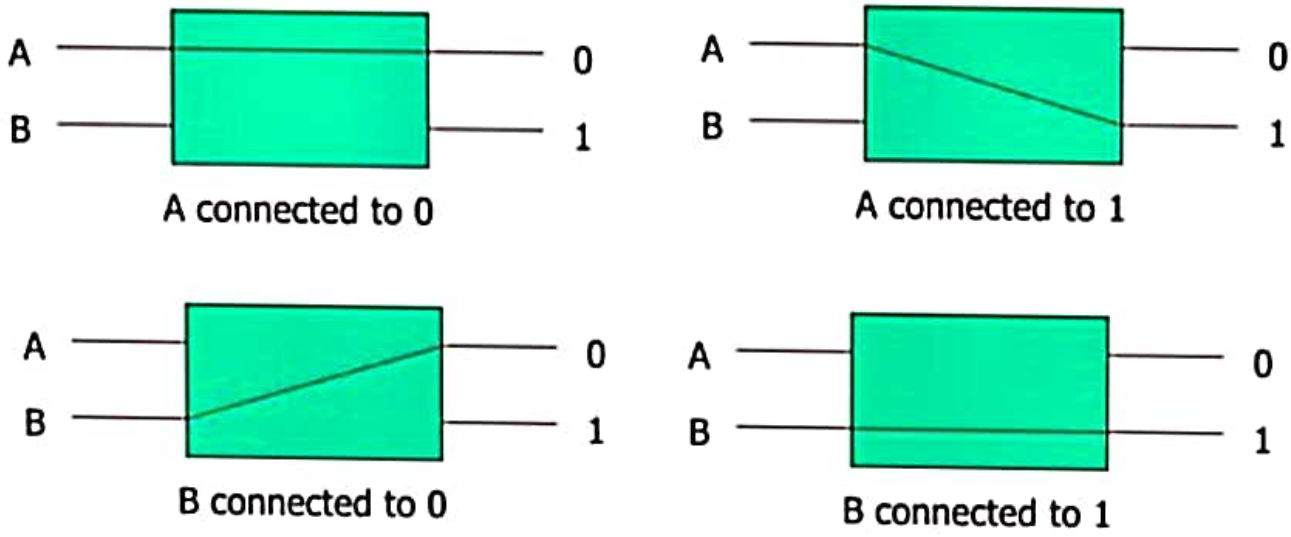
Crossbar switch



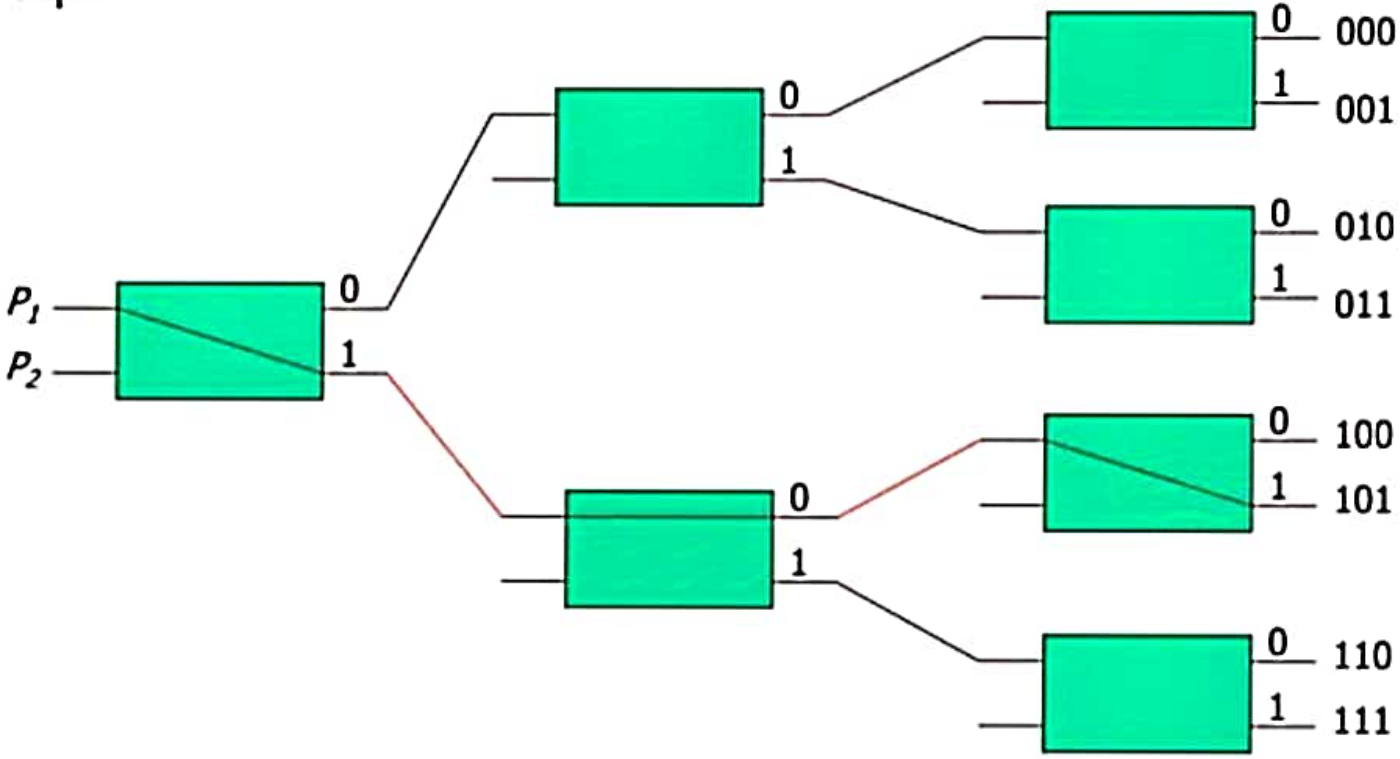
Multistage switching network

- The basic component of a multistage network is a two-input, two-output interchange switch as shown in Fig. 6.
- Using the 2x2 switch as a building block, it is possible to build a multistage network to control the communication between a number of sources and destinations.
  - To see how this is done, consider the binary tree shown in Fig. 13-7.
  - Certain request patterns cannot be satisfied simultaneously. i.e., if $P_1 \rightarrow$ 000~011, then $P_2 \rightarrow$ 100~111

Operation of a 2 x 2 interchange sv
Fig. 6

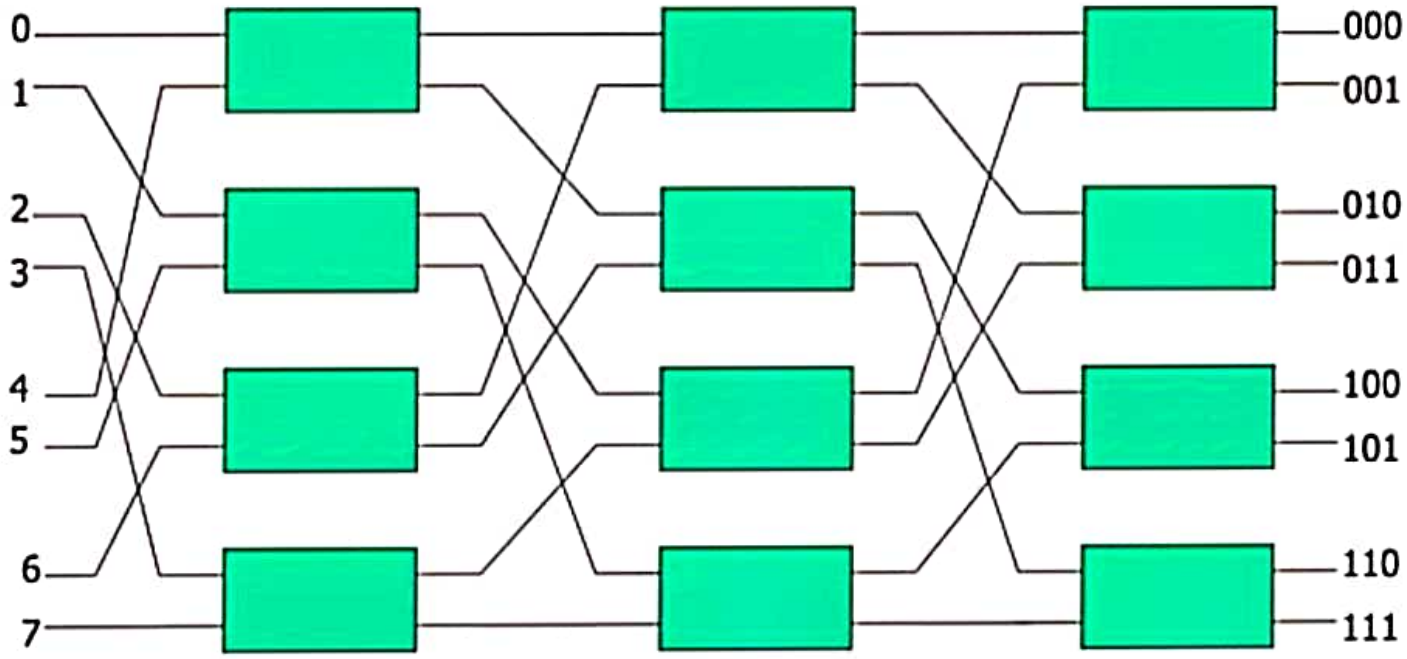


Binary tree with 2 x 2 switches



8 x 8 omega switching networki

Fig. 8



Hypercube system

- The hypercube or binary n-cube multiprocessor structure is a loosely coupled system composed of $N=2^n$ processors interconnected in an n-dimensional binary cube.
  - Each processor forms a node of the cube, in effect it contains not only a CPU but also local memory and I/O interface.
  - Each processor address differs from that of each of its n neighbors by exactly one bit position.
- Fig. 9 shows the hypercube structure for n=1, 2, and 3.

Hypercube structures for n=1, 2
Fig. 9