1. Description

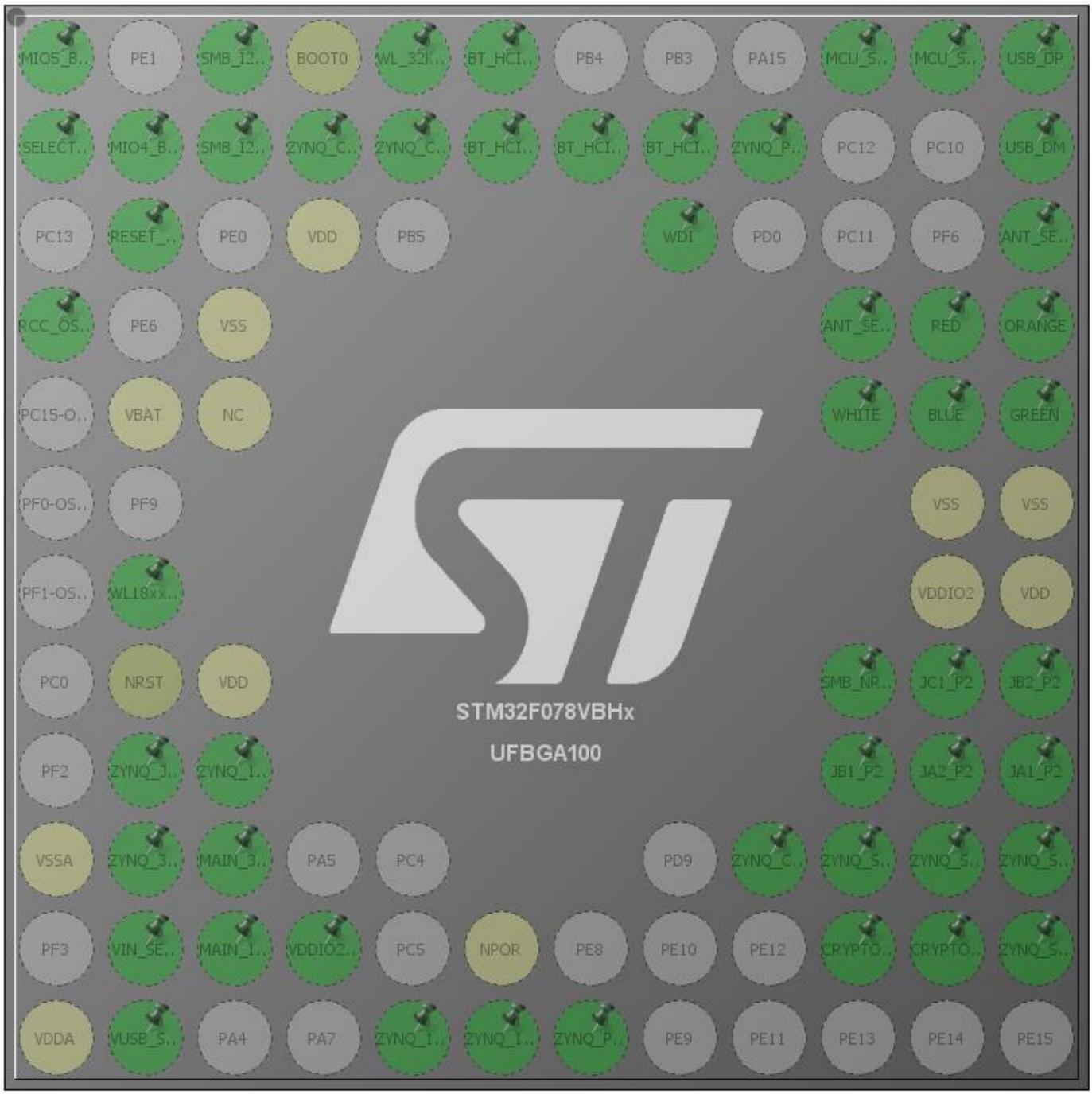
1.1. Project

Project Name	platform-controller
Board Name	platform-controller
Generated with:	STM32CubeMX 4.12.0
Date	05/18/2016

1.2. MCU

MCU Series	STM32F0
MCU Line	STM32F0x8
MCU name	STM32F078VBHx
MCU Package	UFBGA100
MCU Pin number	100

2. Pinout Configuration



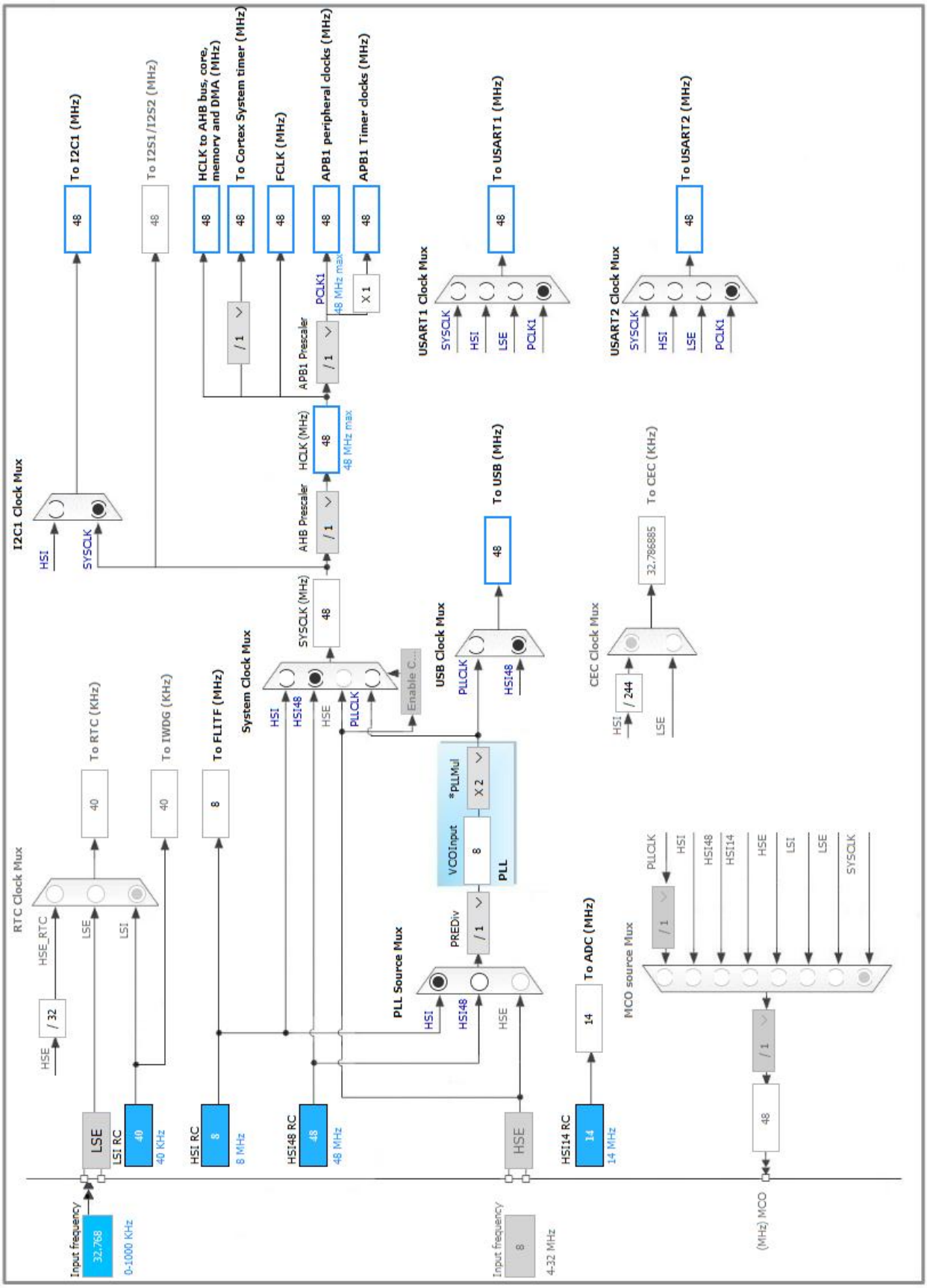
3. Pins Configuration

Pin Number UFBGA100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	PE3 *	I/O	GPIO_Output	MIO5_BOOT_SELECT
A3	PB8	I/O	I2C1_SCL	SMB_I2C_SCL
A4	BOOT0	Boot		
A5	PD7 *	I/O	GPIO_Output	WL_32KHZ_CLK_EN
A6	PD5	I/O	USART2_TX	BT_HCI_RX
A10	PA14	I/O	SYS_SWCLK	MCU_SWCLK
A11	PA13	I/O	SYS_SWDIO	MCU_SWDIO
A12	PA12	I/O	USB_DP	USB_DP
B1	PE4 *	I/O	GPIO_Input	SELECT_BUTTON
B2	PE2 *	I/O	GPIO_Output	MIO4_BOOT_SELECT
B3	PB9	I/O	I2C1_SDA	SMB_I2C_SDA
B4	PB7	I/O	USART1_RX	ZYNQ_CONSOLE_TX
B5	PB6	I/O	USART1_TX	ZYNQ_CONSOLE_RX
B6	PD6	I/O	USART2_RX	BT_HCI_TX
B7	PD4	I/O	USART2_RTS	BT_HCI_CTS
B8	PD3	I/O	USART2_CTS	BT_HCI_RTS
B9	PD1 *	I/O	GPIO_Output	ZYNQ_POWER_EN
B12	PA11	I/O	USB_DM	USB_DM
C2	PE5 *	I/O	GPIO_Input	RESET_BUTTON
C4	VDD	Power		
C8	PD2 *	I/O	GPIO_Output	WDI
C12	PA10 *	I/O	GPIO_Output	ANT_SELECT_2
D1	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
D3	VSS	Power		
D10	PA9 *	I/O	GPIO_Output	ANT_SELECT_1
D11	PA8	I/O	TIM1_CH1	RED
D12	PC9	I/O	TIM3_CH4	ORANGE
E2	VBAT	Power		
E3	NC	Power		
E10	PC8	I/O	TIM3_CH3	WHITE
E11	PC7	I/O	TIM3_CH2	BLUE
E12	PC6	I/O	TIM3_CH1	GREEN
F11	VSS	Power		
F12	VSS	Power		
G2	PF10 *	I/O	GPIO_Output	WL18xx_BT_EN
G11	VDDIO2	Power		

Pin Number UFBGA100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
G12	VDD	Power		
H2	NRST	Reset		
H3	VDD	Power		
H10	PD15 *	I/O	GPIO_Output	SMB_NRESET
H11	PD14	I/O	GPIO_EXTI14	JC1_P2
H12	PD13	I/O	GPIO_EXTI13	JB2_P2
J2	PC1 *	I/O	GPIO_Output	ZYNQ_JTAG_NRST
J3	PC2	I/O	ADC_IN12	ZYNQ_1V2_SENSE
J10	PD12	I/O	GPIO_EXTI12	JB1_P2
J11	PD11	I/O	GPIO_EXTI11	JA2_P2
J12	PD10	I/O	GPIO_EXTI10	JA1_P2
K1	VSSA	Power		
K2	PC3	I/O	ADC_IN13	ZYNQ_3V3_SENSE
K3	PA2	I/O	ADC_IN2	MAIN_3V3_SENSE
K9	PD8 *	I/O	GPIO_Output	ZYNQ_CLK_EN
K10	PB15	I/O	SPI2_MOSI	ZYNQ_SPI_MOSI
K11	PB14	I/O	SPI2_MISO	ZYNQ_SPI_MISO
K12	PB13	I/O	SPI2_SCK	ZYNQ_SPI_CLK
L2	PA0	I/O	ADC_IN0	VIN_SENSE
L3	PA3	I/O	ADC_IN3	MAIN_1V8_SENSE
L4	PA6	I/O	ADC_IN6	VDDIO2_3V3_SENSE
L6	NPOR	Power		
L10	PB10	I/O	I2C2_SCL	CRYPTO_I2C_SCL
L11	PB11	I/O	I2C2_SDA	CRYPTO_I2C_SDA
L12	PB12	I/O	SPI2_NSS	ZYNQ_SPI_NSS
M1	VDDA	Power		
M2	PA1	I/O	ADC_IN1	VUSB_SENSE
M5	PB0	I/O	ADC_IN8	ZYNQ_1V0_SENSE
M6	PB1	I/O	ADC_IN9	ZYNQ_1V8_SENSE
M7	PE7 *	I/O	GPIO_Input	ZYNQ_POWER_GOOD

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC

mode: IN0

mode: IN1

mode: IN2

mode: IN3

mode: IN6

mode: IN8

mode: IN9

mode: IN12

mode: IN13

5.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Forward
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled
Low Power Auto Power Off	Disabled

ADC_Regular_ConversionMode:

Sampling Time	1.5 Cycles
External Trigger Conversion Edge	None

WatchDog:

Enable Analog WatchDog Mode	false

5.2. I2C1

I2C: I2C

5.2.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20303E5D ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.3. I2C2

mode: I2C

5.3.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20303E5D ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.4. RCC

Low Speed Clock (LSE) : BYPASS Clock Source

5.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	1.8
Instruction Cache	Disabled
Prefetch Buffer	Enabled
Data Cache	Disabled
Flash Latency(WS)	1 WS (2 CPU cycle)

RCC Parameters:

HSI14 Calibration Value	16

5.5. SPI2

Mode: Full-Duplex Slave
mode: Hardware NSS Signal

5.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Input Hardware

5.6. SYS

mode: Serial-WireDebug

5.7. TIM1

Channel1: PWM Generation CH1

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1919 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	**Low ***
CH Idle State	Reset

5.8. TIM3

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1919 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	**Low ***

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	**Low ***

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	**Low ***

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	**Low ***

5.9. TIM7

mode: Activated

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0

Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**47999 ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Update Event ***

5.10. USART1

Mode: Asynchronous

5.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.11. USART2

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

5.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.12. USB

mode: Device (FS)

5.12.1. Parameter Settings:

Basic Parameters:

Speed	Full Speed 12MBit/s
Endpoint 0 Max Packet size	8 Bytes
Physical interface	Internal Phy

Power Parameters:

Low Power	Disabled
Battery Charging	Disabled

5.13. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

5.13.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SUPPORT_USER_STRING (Enable user string descriptor)	Disabled
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message

Class Parameters:

USBD_CDC_INTERVAL (Number of micro-frames interval)	1000

5.13.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	**STMMicroelectronics ***

Device Descriptor FS:

PID (Product IDentifier)	22336
PRODUCT_STRING (Product Identifier)	**STMicroelectronics Virtual COM Port ***
SERIALNUMBER_STRING (Serial number)	00000000001A
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC	PC2	ADC_IN12	Analog mode	n/a	n/a	ZYNQ_1V2_SENSE
	PC3	ADC_IN13	Analog mode	n/a	n/a	ZYNQ_3V3_SENSE
	PA2	ADC_IN2	Analog mode	n/a	n/a	MAIN_3V3_SENSE
	PA0	ADC_IN0	Analog mode	n/a	n/a	VIN_SENSE
	PA3	ADC_IN3	Analog mode	n/a	n/a	MAIN_1V8_SENSE
	PA6	ADC_IN6	Analog mode	n/a	n/a	VDDIO2_3V3_SENSE
	PA1	ADC_IN1	Analog mode	n/a	n/a	VUSB_SENSE
	PB0	ADC_IN8	Analog mode	n/a	n/a	ZYNQ_1V0_SENSE
	PB1	ADC_IN9	Analog mode	n/a	n/a	ZYNQ_1V8_SENSE
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	n/a	**High ***	SMB_I2C_SCL
	PB9	I2C1_SDA	Alternate Function Open Drain	n/a	**High ***	SMB_I2C_SDA
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	n/a	**High ***	CRYPTO_I2C_SCL
	PB11	I2C2_SDA	Alternate Function Open Drain	n/a	**High ***	CRYPTO_I2C_SDA
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
SPI2	PB15	SPI2_MOSI	Alternate Function Push Pull	n/a	**High ***	ZYNQ_SPI_MOSI
	PB14	SPI2_MISO	Alternate Function Push Pull	n/a	**High ***	ZYNQ_SPI_MISO
	PB13	SPI2_SCK	Alternate Function Push Pull	n/a	**High ***	ZYNQ_SPI_CLK
	PB12	SPI2_NSS	Alternate Function Push Pull	n/a	**High ***	ZYNQ_SPI_NSS
SYS	PA14	SYS_SWCLK	n/a	n/a	n/a	MCU_SWCLK
	PA13	SYS_SWDIO	n/a	n/a	n/a	MCU_SWDIO
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	n/a	Low	RED
TIM3	PC9	TIM3_CH4	Alternate Function Push Pull	n/a	Low	ORANGE
	PC8	TIM3_CH3	Alternate Function Push Pull	n/a	Low	WHITE
	PC7	TIM3_CH2	Alternate Function Push Pull	n/a	Low	BLUE
	PC6	TIM3_CH1	Alternate Function Push Pull	n/a	Low	GREEN
USART1	PB7	USART1_RX	Alternate Function Push Pull	n/a	**High ***	ZYNQ_CONSOLE_TX
	PB6	USART1_TX	Alternate Function Push Pull	n/a	**High ***	ZYNQ_CONSOLE_RX
USART2	PD5	USART2_TX	Alternate Function Push Pull	n/a	**High ***	BT_HCI_RX
	PD6	USART2_RX	Alternate Function Push Pull	n/a		BT_HCI_TX

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					High *	
	PD4	USART2_RTS	Alternate Function Push Pull	n/a	**High ***	BT_HCI_CTS
	PD3	USART2_CTS	Alternate Function Push Pull	n/a	**High ***	BT_HCI_RTS
USB	PA12	USB_DP	n/a	n/a	n/a	USB_DP
	PA11	USB_DM	n/a	n/a	n/a	USB_DM
GPIO	PE3	GPIO_Output	Output Push Pull	n/a	Low	MIO5_BOOT_SELECT
	PD7	GPIO_Output	Output Push Pull	n/a	Low	WL_32KHZ_CLK_EN
	PE4	GPIO_Input	Input mode	n/a	n/a	SELECT_BUTTON
	PE2	GPIO_Output	Output Push Pull	n/a	Low	MIO4_BOOT_SELECT
	PD1	GPIO_Output	Output Push Pull	n/a	Low	ZYNQ_POWER_EN
	PE5	GPIO_Input	Input mode	n/a	n/a	RESET_BUTTON
	PD2	GPIO_Output	Output Push Pull	n/a	Low	WDI
	PA10	GPIO_Output	Output Push Pull	n/a	Low	ANT_SELECT_2
	PA9	GPIO_Output	Output Push Pull	n/a	Low	ANT_SELECT_1
	PF10	GPIO_Output	Output Push Pull	n/a	Low	WL18xx_BT_EN
	PD15	GPIO_Output	Output Push Pull	n/a	Low	SMB_NRESET
	PD14	GPIO_EXTI14	External Interrupt Mode with Rising edge trigger detection	n/a	n/a	JC1_P2
	PD13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	n/a	n/a	JB2_P2
	PC1	GPIO_Output	**Output Open Drain ***	n/a	Low	ZYNQ_JTAG_NRST
	PD12	GPIO_EXTI12	External Interrupt Mode with Rising edge trigger detection	n/a	n/a	JB1_P2
	PD11	GPIO_EXTI11	External Interrupt Mode with Rising edge trigger detection	n/a	n/a	JA2_P2
	PD10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	n/a	n/a	JA1_P2
	PD8	GPIO_Output	Output Push Pull	n/a	Low	ZYNQ_CLK_EN
	PE7	GPIO_Input	Input mode	n/a	n/a	ZYNQ_POWER_GOOD

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
System tick timer	true	0	0
EXTI line 4 to 15 interrupts	true	0	0
TIM7 global interrupt	true	0	0
SPI2 global interrupt	true	0	0
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	true	1	0
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	true	0	0
USB global interrupt / USB wake-up interrupt through EXTI line 18	true	1	0
Non maskable interrupt	unused		
Hard fault interrupt	unused		
VDDIO2 supply comparator interrupt through EXTI line 31	unused		
Flash global interrupt	unused		
RCC and CRS global interrupts	unused		
ADC and COMP interrupts (COMP interrupts through EXTI lines 21 and 22)	unused		
TIM1 break, update, trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
I2C1 event global interrupt / I2C1 wake-up interrupt through EXTI line 23	unused		
I2C2 global interrupt	unused		

*** User modified value**

7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F0
Line	STM32F0x8
MCU	STM32F078VBHx
Datasheet	026006_Rev2

7.2. Parameter Selection

Temperature	25
Vdd	1.8

8. Software Project

8.1. Project Settings

Name	Value
Project Name	platform-controller
Project Folder	\\vmware-host\Shared Folders\Software\snickerdoodle-STM32-firmware
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F0 V1.4.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	No
Set all free pins as analog (to optimize the power consumption)	No