Advance MCU Lab3

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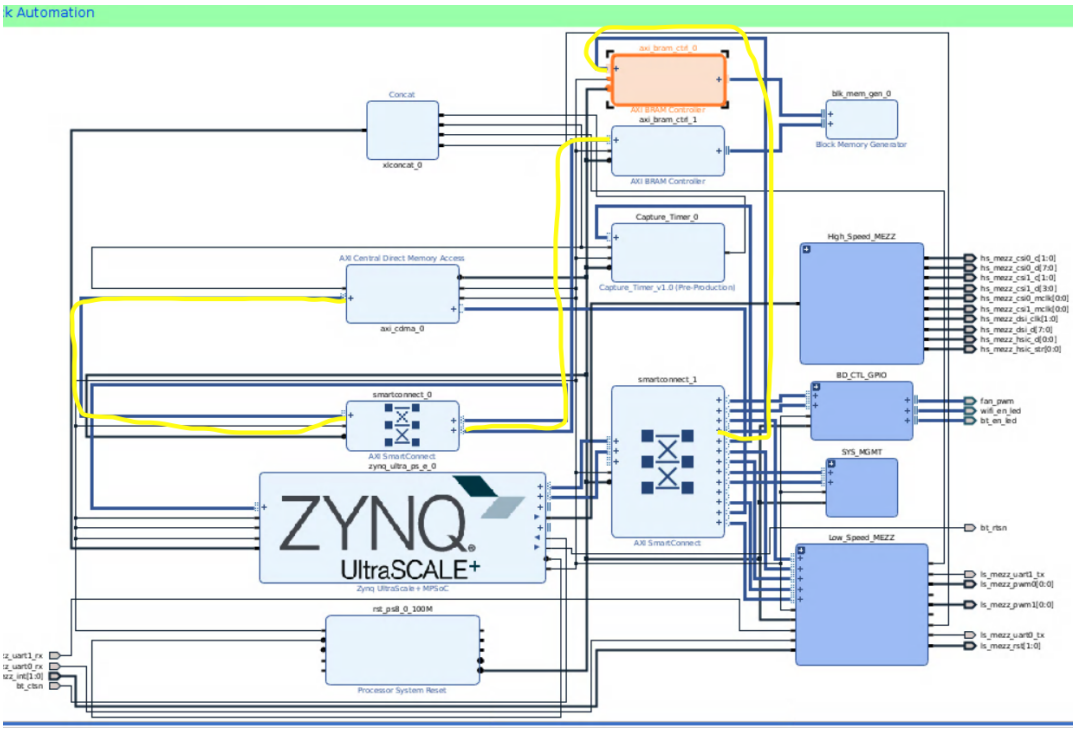
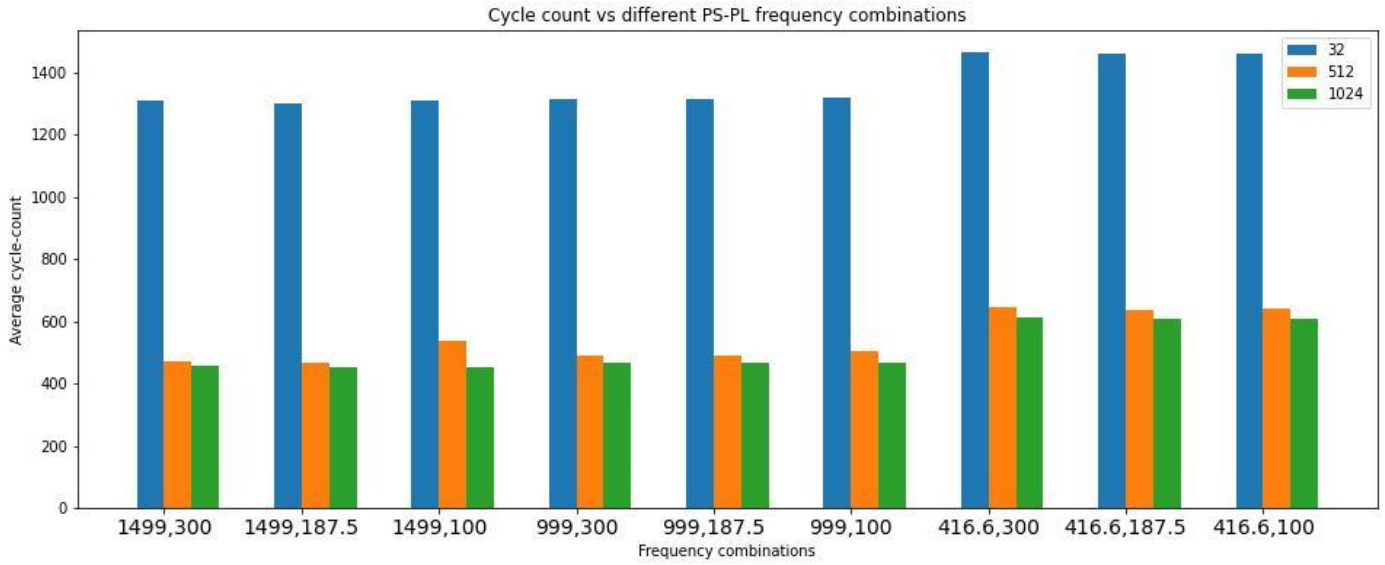
1. Determine which busses to maximize between the PS-PL. Explain how and why?
   a. 

   b. PS to Smart connect bus is configured to its maximum width by default. As specified in the lab doc, we configured PS AXI Master HPM1 FPD data width to 128. This is set to 128 by default.
2. If necessary, change the SmartConnect configuration. Explain why?
   a. I have not modified SmartConnect.
3. Determine which busses to maximize in the PL to the point where there are no timing issues. Explain how and why?
   a. Bus widths have less impact on timing issues. From my experiments, I didn't face any issues with timing while changing the bus widths on the PL side.
4. Determine which busses to maximize in the PL to the point where there are still some FPGA resources available (i.e., >3%)
   a. The data flows from PS to smart connect, smart connect to DMA, DMA to smart connect, smart connect to BRAM controller in the specified order.
   b. The BRAM to Smartconnect1 can be increased too. But, Vivado allows it to a maximum of ¼ that of the other port of the BRAM — 1024. Hence, we configured our BRAM controller0 bus width to 256.
   c. The DMA bus width can be increased. Here, we increased it to 1024 and reduced the burst size accordingly.

5. Maximize the PL synthesis clock frequency in Vivado to the point where there are no timing issues. Explain how and why?
    a. The clock frequency for which the Worst Negative Slack and Total Negative slacks are positive — a design still functions — is 250 MHz. I got the TNS and WNS to be negative for 300 MHz.
    b. However, this has not caused any issues in the software when the PL frequency is configured to 300 MHz. We also observed this in the previous labs where we synthesized the design to 100MHz and configured the clock to 300MHz. We can explain this by the hypothesis that Vivado chooses the best possible BRAMS blocks. Furthermore, I observed that the TNS and WNS were not that bad during the Synthesis with 300 MHz constraints. This observation strengthens our claim that we can run the software at 300 MHz PL frequency.
6. Run Lab_2 Test #1 using the new PS and PL configurations to determine the baseline performance improvements.
    a. Graph the performance improvements versus what you got in Lab_2.



    b. If there are performance improvements explain where they are coming from. If not explain why there was no improvement. You may need to generate additional instrumentation blocks to help determine what is going on.
    c. I have plotted the average cycle count vs different frequency combinations for DMA transfers. In our previous lab, we see that the cycle count is around 1300 for various frequency combinations. After changing the bus widths to the above-mentioned configurations, we can see the average count reduced to 500.
        i. DMA data widths = 1024
        ii. BRAM controller = 1024, 256 respectively
    d. They are coming from the increment of DMA data width from 32 to 1024. Keeping DMA width the same, the BRAM's data width change from 1024 to 512 did not degrade the performance that much. We can observe this from the graph too.

    e. I did not instrument any modules since we can see the performance improvement from the graphs.
    f. Note: Our 300MHz PL clock frequency did not create any issues. Hence, it was possible for us to compare all the frequencies as for the previous lab.
7. Determine if should now modify your application software and kernel module to take advantage of the new hardware configuration.
    a. Graph the performance improvements with the new software changes.
    b. If there are performance improvements explain where they are coming from. If not explain why there was no improvement. You may need to generate additional instrumentation blocks to help determine what is going on.
    c. We have not made any changes to the software.