Spring 2023

EE 382N-4: Advanced Embedded Systems

Classroom: EER 1.512

Time: Tue/Thu 14:00 - 15:15

Last updated: Tuesday, April 04, 2023

Course Overview:

This course focuses on the HW/SW architectures of “System-on-a-Chip (SoC) implementations. The SoC’s are composed of hardware and software components which must be seamlessly integrated together to produce working SOCs. These systems are becoming increasingly complex utilizing micro-architectural features from high performance computing platforms and from operating systems such as Linux and Android.

Topics covered:

Hardware and software co-design of an SOC on a ARM multi-core based FPGA
Linux drivers/handlers, kernel modules and interrupt handlers
Flash based file systems
Embedded Linux debugging
Hardware accelerators, dataflow processing
Intelligent & cognitive sensor systems, sensor fusing
I/O subsystems
Power aware software
Networking-on-chip (NOC).

There will be 3 lab assignments, 1 exam and a class project.

The class project focuses building a hardware accelerator that is coupled to an ARM multi-core system via the AXI bus on the Ultra96V2 board. The Lab assignments focus on learning how to design, synthesize, debug and test using various components of the Xilinx ZYNQ SOC.

Course prerequisites:

- An undergrad or grad Computer Architecture course similar to **EE460N/EE382N.1** or an equivalent Computer Architecture course.
- **EE445L** or **EE445M** undergraduate Embedded Systems, or similar courses.
- Basic high level language programming skills such as C or C++
- Basic VERILOG or VHDL programming skills
- Some familiarity with assembly language programming (ARM)
- Some familiarity with Linux programming

Instructor:

Mark McDermott
Office: EER 5.826,
Phone: (512) 471-3253
Office hours: **See Canvas**
Or by appointment.
E-Mail: *mcdermot at ece.utexas.edu*

Course outline and schedule:

Week	Date	Lecture Topic	Lecture Notes	LAB Assignments
1	Jan 10 Jan 12	Course Overview Xilinx Development Environment **Lab #1 Overview**	Lecture 1 Lecture 2	LAB #1 ~~Due Feb 2nd~~ Due Feb 6th
2	Jan 17 Jan 19	Zynq UltraScale+ Architecture	Lecture 3	
3	Jan 24 Jan 26	Debugging ZynqMP Hardware Debugging Embedded Linux	Lecture 4a Lecture 4b	
4	Jan 31 Feb 2	**Classes Cancelled**		
5	Feb 7 Feb 9	Interrupts, Interrupt Handlers & Signals **Lab # 2 Overview**	Lecture 5	LAB #2 Due: Feb 27th
6	Feb 14 Feb 16	Linux Device Drivers	Lecture 6	
7	Feb 21 Feb 23	Embedded Linux **Lab #3 Overview**	Lecture 7	

8	Feb 28	Boot Loaders & Device Tree Blobs	Lecture 8	LAB #3 Due: Mar 24th
	Mar 2	Linux File Systems	Lecture 9	
9	Mar 7	Software Optimization for Power Reduction	Lecture 10	
	Mar 9	Dataflow Processing	Lecture 11	
	Mar 13-18	Spring Break		
10	Mar 21	Sensor Systems	Lecture 12	
	Mar 23			
11	Mar 28	Accelerators & Co-Processors	Lecture 13	**Work on Final Project**
	Mar 30	Exam	Previous Exams	
12	Apr 4	ARM v8 Processor Architecture ARM v8 ISA ARM v7 Processor Architecture ARM v7 ISA	Lecture 14a Lecture 14b Lecture 14c Lecture 14d	
	Apr 6	Network-on-Chips (NOC)	Lecture 15	
13	Apr 11	**NO lectures -- Work on Final Project** **NOTE: Project Reviews will be held in person during Final Exam Period May 1st No exceptions**		
	Apr 13			
14	Apr 18			
	Apr 20			

Grading:	
Lab #1	5%
Lab #2	15%
Lab #3	20%
Exam	20%

Project	40%

Late Submission Penalties:

Penalty for late submission of Labs and Class Project: 25% per working day (Maximum: 100%)

Lab Facilities:

EER 1.806/1.810

Getting Started Tutorials:

Setting up Baseline Ultra96 Xilinx Environment

BIT File Generation Flow

Ultra-96 Documentation:

Setting up Ultra-96 Board

Getting Started

Ultra-96 HW User Guide

Ultra-96 Base TRD

Ultra-96 Building the Base TRD

Ultra-96 Schematic

Ultra96 Assembly Drawings

Xilinx Zynq UltraScale+ Tutorials and Documentation

ZYNQ UltraScale+ White Papers

ZYNQ UltraScale+ Register Map

ZYNQ UltraScale+ MPSoC Base Targeted Reference Design

ZYNQ UltaScale+ Documentation

ZYNQ UltraScale+ Video Tutorials

Zynq UltraScale+ All Programmable SoC Technical Reference Manual

Exploring Zynq MPSoC

FPGAs for SW Programmers

AXI Infrastructure Intellectual Property

Creating an AXI Peripheral

Using Xilinx SDK

Repository of useful Vivado, Zynq & Petalinux Documentation

Vivado Tutorials and Documentation

Vivado Video Tutorials

Vivado Design Suite User Guide: Getting Started (UG910)

Vivado Design Suite Tutorial (UG940)

Vivado Design User Guide: Design Flows Overview (UG892)

Vivado Design Suite Tutorial: Design Flows Overview (UG888)

Vivado Design Suite Tutorial: Programming and Debugging (UG936)

Vivado Design Suite User Guide: High-Level Synthesis (UG902)

Vivado Design Suite User Guide: Synthesis (UG901)

Vivado Design Suite User Guide: Implementation (UG904)

Introduction to FPGA Design with Vivado High-Level Synthesis

Vivado Design Suite User Guide: Using Tcl Scripting (UG894)

Vivado Design Suite Tcl Command Reference Guide (UG835)

Vivado Design Suite User Guide: Designing with IP (UG896)

Vivado Design Suite User Guide: Designing IP Subsystems Using IP Integrator (UG994)

Vivado Design Suite User Guide: Logic Simulation (UG900)

Vivado Design Suite User Guide: Using Constraints (UG903)

Vivado Design Suite User Guide: Design Analysis and Closure Techniques (UG906)

Vivado Design Suite User Guide: Design Analysis and Closure Techniques (Design HUB)

Vivado Design Suite User Guide: Programming and Debugging (UG908)

Vivado Design Suite User Guide: System-Level Design Entry (UG895)

Vivado Design Suite Properties Reference Guide (UG912)

Vivado Design Suite User Guide: I/O and Clock Planning (UG899)

Vivado Design Suite User Guide: Model-Based DSP Design Using System Generator (UG897)

Vivado Design Suite User Guide: Power Analysis and Optimization (UG907)

Xilinx Wiki

Main page

Zynq 7000 Wiki

Zynq UltraScale+MPSoc Wiki

Linux

U-Boot

Technical Articles

Installing Ubuntu

Zynq Base Targeted Reference Design (TRD)

Zynq UltraScale+ MPSoC Base Targeted Reference

Digilent Zedboard Tutorials and Documentation

Embedded Linux Development Guide

Getting Started with Embedded Linux - ZedBoard

Embedded Linux Hands-on Tutorial - ZedBoard

Creating a Custom IP core using the IP Integrator

Getting Started with Zynq

Using Pmod IPs

Zedboard DMA Audio Demo

Zedboard LED Demo

Zedboard OLED Demo
Zedboard Programming Guide in SDK

Forums

Xilinx

Avnet

Digilent

Miscellaneous Websites

Zynq Design from Scratch

bootlin (Free Electrons)

Zynq Training

An FPGA Tutorial using the ZedBoard

References

Sreekrishnan Venkateswaran Essential Linux Device Drivers (Prentice Hall Open Source Software Development Series)

Karim Yaghmour Building Embedded Linux Systems

Jonathon Corbet Linux Device Drivers

Richard Zurawski Embedded Systems Handbook: Networked Embedded Systems

L.H. Crockett, R.A. Elliot, M.A. Enderwitz, and R.W. Stewart, The Zynq Book: Embedded Processing with the ARM Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC, PDF copy available for free at http://www.zynqbook.com

L.H. Crockett, R.A. Elliot, M.A. Enderwitz, and R.W. Stewart, The Zynq Book Tutorials, available for free at http://www.zynqbook.com/download-tuts.html

Academic dishonesty:

Oral discussion of homework problems is encouraged. However, be sure to submit your own individual and independent solution. Labs and final projects can be done in teams. Collaboration on projects is encouraged. Copying of any part of a homework/lab solution or project report without explicit reference to its source is plagiarism and considered cheating.

Electronic Mail Notification Policy:

In this course e-mail will be used as a means of communication with students. You will be responsible for checking your e-mail regularly for class work and announcements. The complete text of the University electronic mail notification policy and instructions for updating your e-mail address are available at http://www.utexas.edu/its/policies/emailnotify.html

Use of Canvas and Class Web Site

This course uses the class web page and Canvas to distribute course materials, to communicate and collaborate online, to submit assignments and to post solutions and grades. You will be responsible for checking the class web page and the Canvas course site regularly for class work and announcements. As with all computer systems, there are occasional scheduled downtimes as well as unanticipated disruptions. Notification of disruptions will be posted on the Canvas login page.

Scheduled downtimes are not an excuse for late work. However, if there is an unscheduled downtime for a significant period of time, I will make an adjustment if it occurs close to the due date.

Students with disabilities

The University of Texas at Austin provides upon request appropriate academic accommodations for qualified students with disabilities. For more information, contact the Services for Students with Disabilities (SSD) at 471-6259, http://ddce.utexas.edu/disability/.

Religious Holidays

Religious holy days sometimes conflict with class and examination schedules. If you miss an examination, work assignment, or other project due to the observance of a religious holy day you will be given an opportunity to complete the work missed within a reasonable time after the absence. It is the policy of The University of Texas at Austin that you must notify each of your instructors at least fourteen days prior to the classes scheduled on dates you will be absent to observe a religious holy day.

Classroom Evacuation and Emergency Preparedness

Every member of the university community must take appropriate and deliberate action when an emergency strikes a building, a portion of the campus, or entire campus community. Emergency preparedness means we are all ready to act for our own safety and the safety of others during a crisis. It takes an effort by all of us to create and sustain an effective emergency preparedness system. Your support is important to achieving the best possible outcomes during a crisis event. As a University faculty member, you are responsible for pointing out your classrooms building emergency evacuation routes and for reviewing emergency procedures with students at the beginning of each semester. This review should include a mention of the monthly emergency communications test (every first Wednesday at 11:50 a.m.) and the list of communications channels the university uses during emergencies. It should also include a review of the attached document outlining emergency terms (e.g., the difference between “shelter-inplace” and “lockdown”) and instructions for faculty and students to follow during emergencies. As a matter of convenience, we recommend including this information in your syllabus along with the phone number for the Behavior Concerns Advice Line (BCAL: **512-232-5050**). This is the number to call if you have concerns regarding the attitude or actions of students, staff, or other faculty. Finally, at the end of your emergency preparedness review, request that students requiring assistance in evacuation inform you in writing of their needs during the first week of class. This information must then be provided to the Fire Prevention Services office by fax (**512-232-2759)**, with "Attn. Mr. Roosevelt Easley" written in the subject line. Thank you in advance for taking the time to ensure the safety of your classroom. I assure you this small effort can yield much greater rewards should the unthinkable happen. If you would like more information regarding emergency preparedness, visit http://www.utexas.edu/safety/preparedness/.

Emergency Communications

Emergencies may range from inclement weather, to building evacuations, to campus closures, and the university has a variety of tools to communicate with the public in the event of these and other possible emergencies. Depending on the type of emergency, we may use some or all of the following tools to communicate with faculty, staff and students:

Siren System

This system is tested around noon on the first Wednesday of every month, and delivers a siren warning and public address in the event of certain outdoor emergencies. Read more about the siren system.

Emergency Web Site

You may want to bookmark the emergency Web site because it is updated with information during actual emergencies or campus closures.

Local Press and Social Media

University Communications staff send emergency information to the press and update social media with public safety messages. Because of the transient nature of our population, the university depends a great deal on the press and social media to keep students, faculty, and staff informed during campus emergencies.

Pager System

Our campus first responders, resident advisors, and some building managers are part of the AWACS paging system. The pagers send text messages about emergencies on campus and alert city responders (APD, AFD, EMS, Office of Emergency Management, etc.) to campus crisis situations.

Text Alerts

The university collects cell phone numbers from members of the campus community for emergency text messages. Sign up for campus text alerts online.

University Group E-mail

During emergencies, UT Safety Alert sends an “urgent” group e-mail to every student, faculty and staff member. The e-mail directs individuals to the emergency Web site for additional information and instruction.

Public Safety Patrol Car Announcements

UTPD patrol cars are equipped with PA systems, which officers can use to provide instructions to pedestrians during emergencies.

University Emergency Information Line: 512-232-9999

Students, faculty, and staff can call this main number for information about campus closures. The implementation of each tool described above is assigned to an individual who has at least two backups who can also carry out the communications task. Individuals with electronic communication tools assigned to them have remote access (from their homes, etc.) to those tools. The police department and the associate vice president for Campus Safety and Security are typically the ones who deliver emergency information to university administration. Upon considering this information, administration develops the messages and activates campus-wide communications. The only exceptions to this are the sirens and pager system, which are activated directly by UTPD in extremely urgent situations where immediate action is required.

Last updated: Tuesday, April 04, 2023
