


Section A (A1)

1. Write Verilog code to describe the following functions $f_1 = ac' + bc + b'c'$ $f_2 = (a+b+c)(a+b+c')(a'+b+c')$ Check whether f_1 and f_2 in question 1 are functionally equivalent or not.

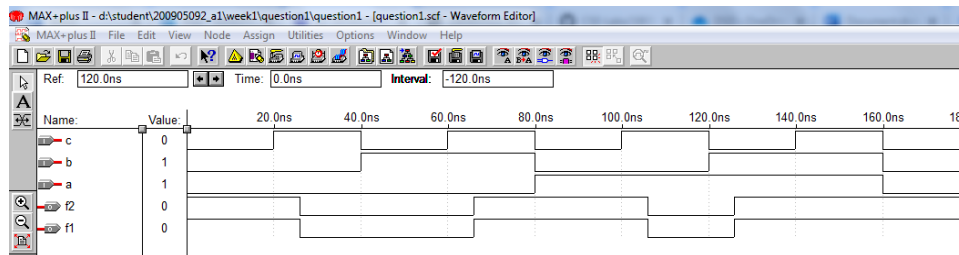


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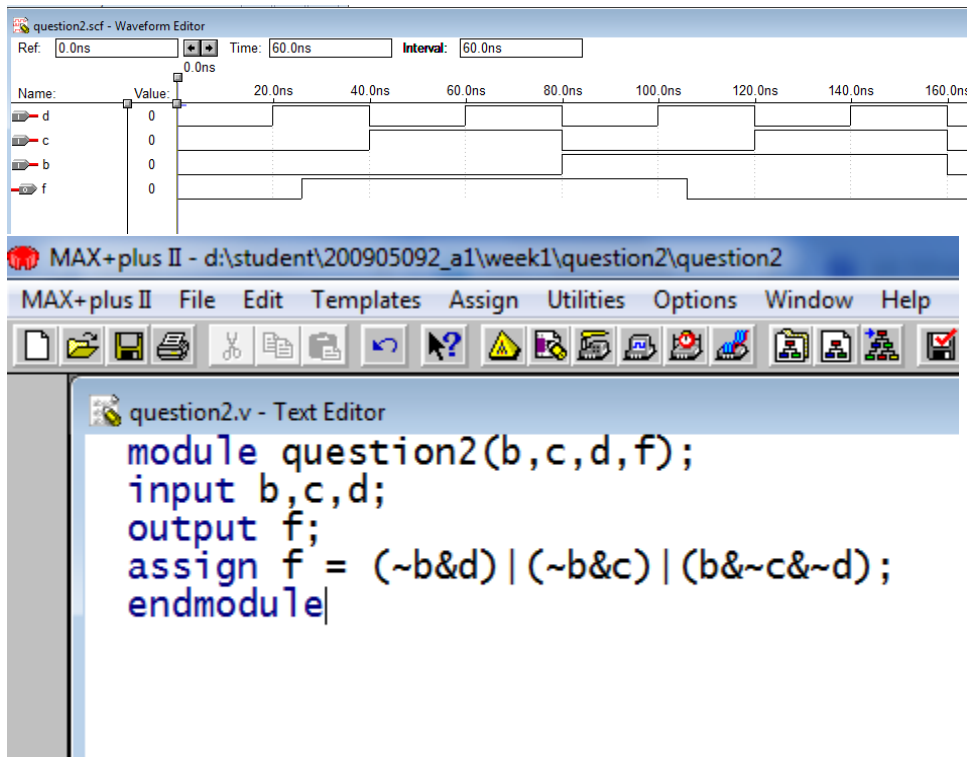
question1.v - Text Editor

```
module
question1 (a,b,c,f1,f2);
input a,b,c;
output f1,f2;
assign f1=(a&~c)|(b&c)|(~b&~c);
assign f2=(a|~b|c)&(a|b|~c)&(~a|b|~c);
endmodule
```

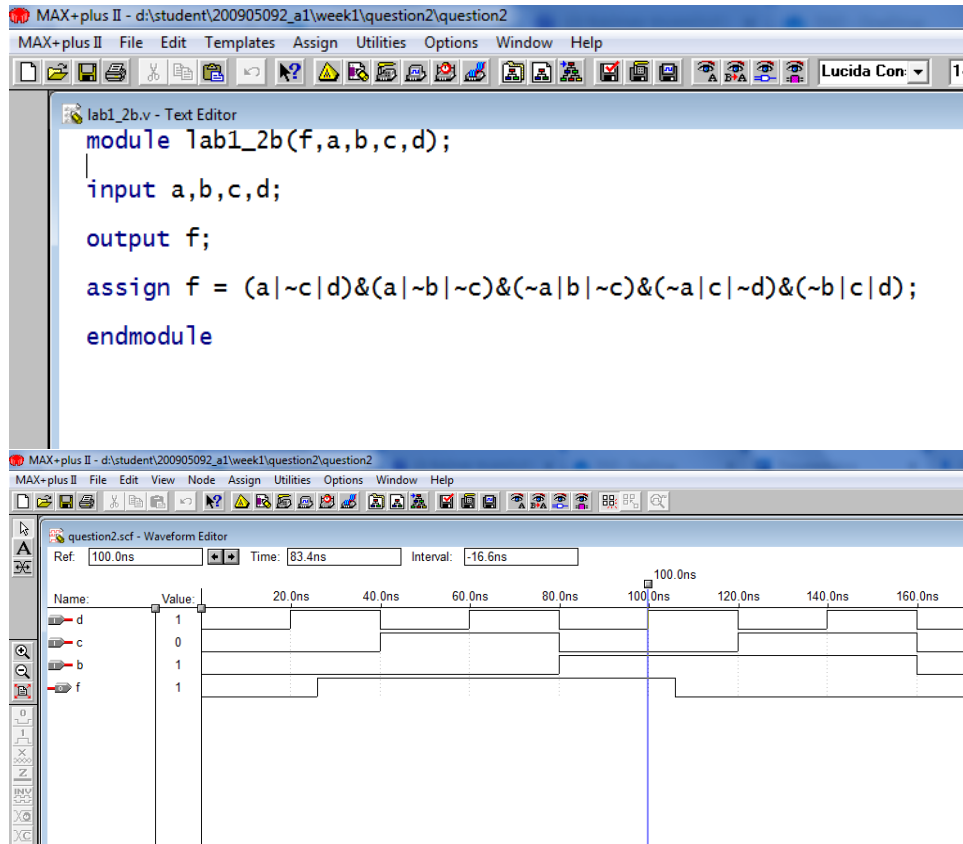


2. Simplify the following functions using K-map and implement the circuit using logic gates. Write Verilog code and simulate the circuit

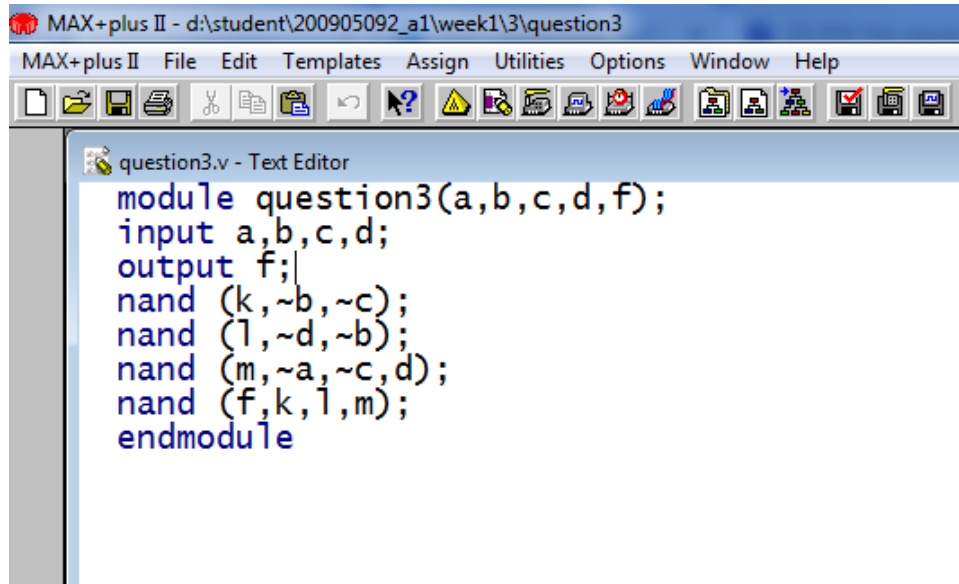
a) $f(A,B,C,D) = \sum m(1,3,4,9,10,12) + D(0,2,5,11)$



$$b)f(A,B,C,D) = \prod M(6,9,10,11,12) + D(2,4,7,13)$$



3. Minimize the following expression using K-map and simulate using only NAND gates.
 $f(A,B,C,D) = \pi M(2,6,8,9,10,11,14)$



```
module question3(a,b,c,d,f);
input a,b,c,d;
output f;
nand (k,~b,~c);
nand (l,~d,~b);
nand (m,~a,~c,d);
nand (f,k,l,m);
endmodule
```

