200905092

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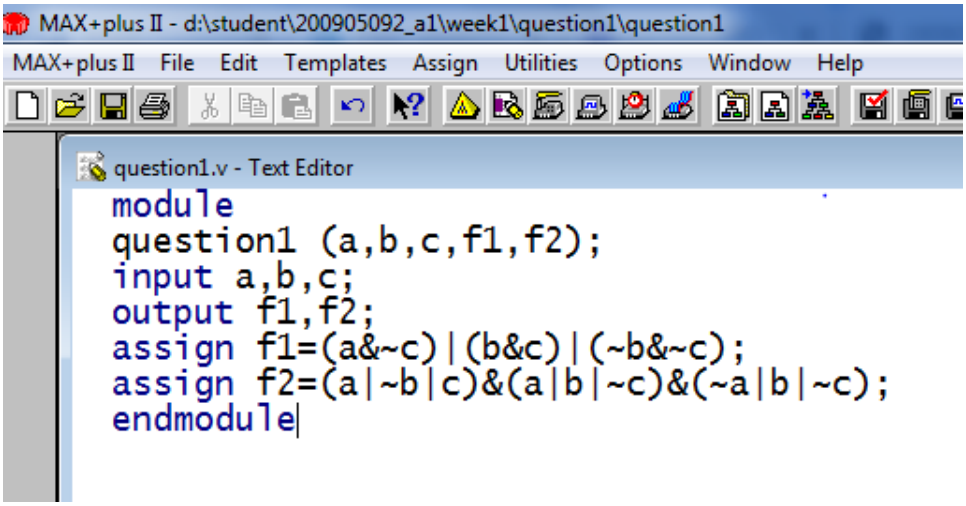
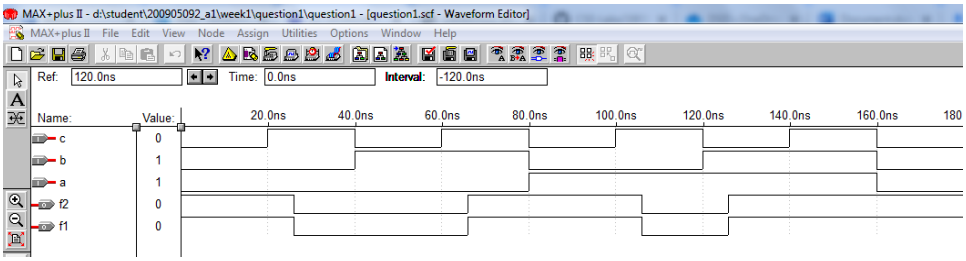
Roll NO 15

Section A (A1)

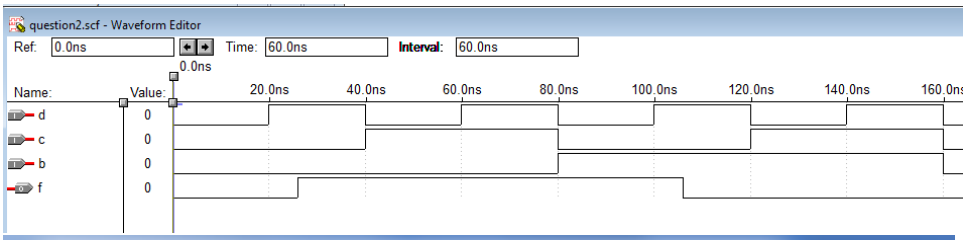
1.Write Verilog code to describe the following functions f1 =ac'+bc+b'c'f2 = (a+b'+c)(a+b+c')(a'+b+c')Check whether f1 and f2 in question 1 are functionally equivalent or not.

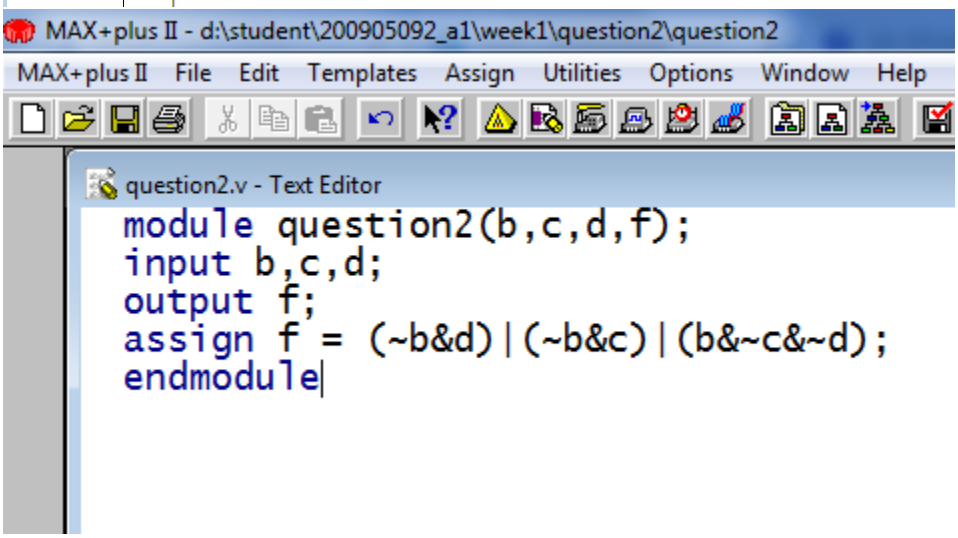




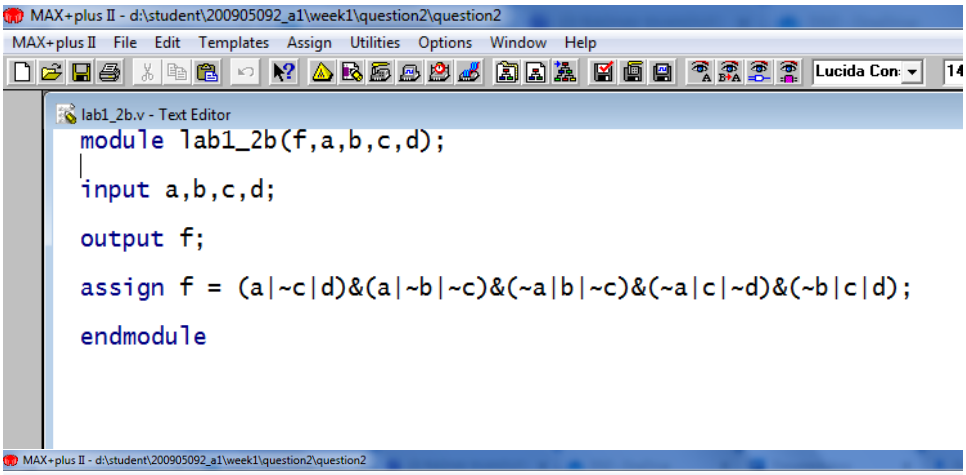
2.Simplify the following functions using K-map and implement the circuit using logic gates.Write Verilog code and simulate the circuit

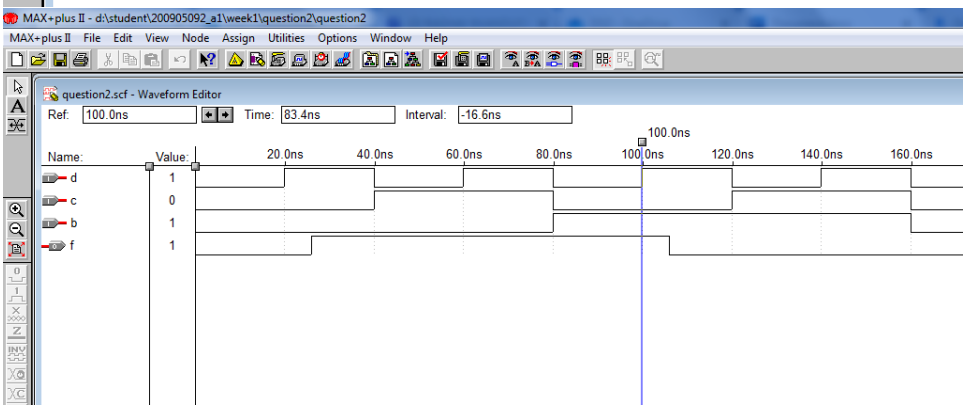
a)f(A,B,C,D) = ∑m(1,3,4,9,10,12) + D(0,2,5,11)





b)f(A,B,C,D) = ∏M(6,9,10,11,12) + D(2,4,7,13)





3.Minimize the following expression using K-map and simulate using only NAND gates.f(A,B,C,D)=πM(2,6,8,9,10,11,14)