CA INNOVATIVE ASSIGNMENT

TWO NEW INSTRUCTION EXUCUTION OF BASIC COMPUTER ARCHITECTURE

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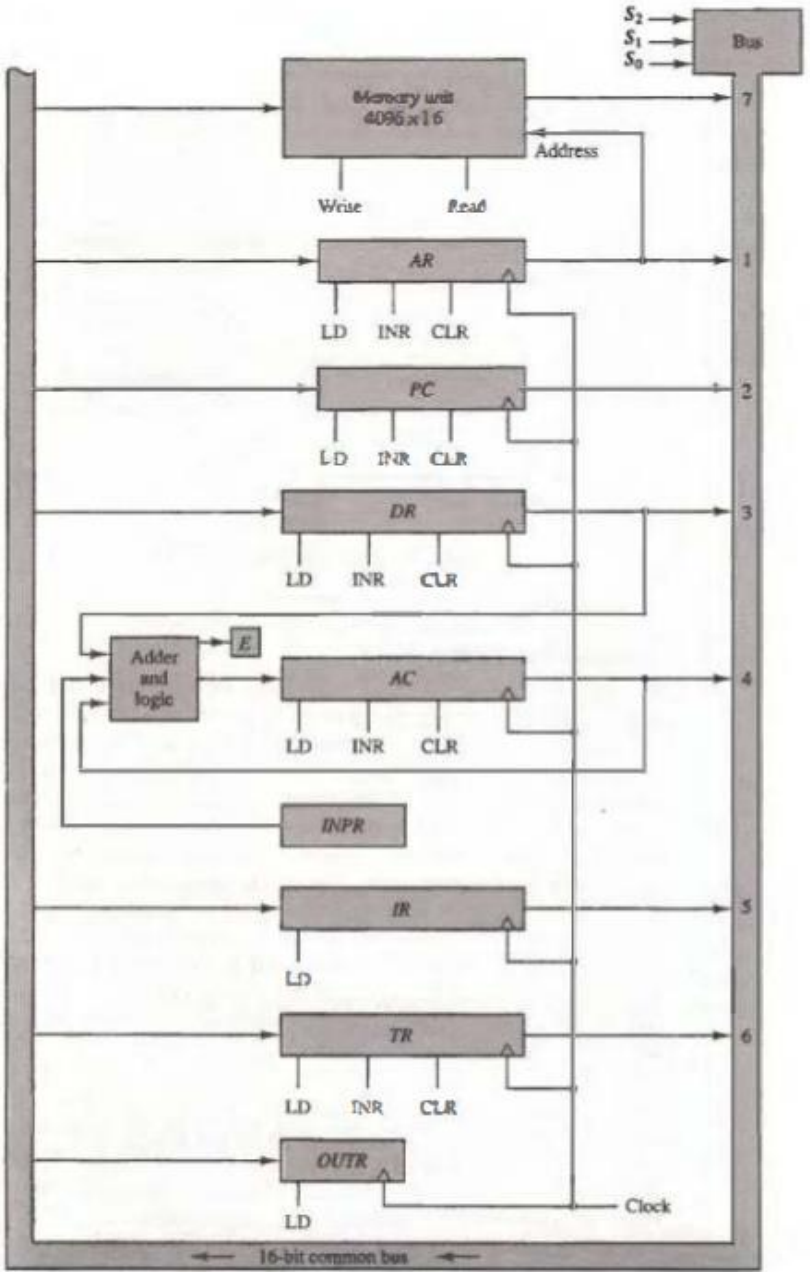
BASIC COMPUTER ARCHITECTURE

The basic computer has eight registers, a memory unit, and a control unit. Paths must be provided to transfer information from one register to another and between memory and registers.
The number of wires will be excessive if connections are made between the outputs of each register and the inputs of the other registers.



TWO NEW INSTRUCTION

1. Exchange - (Swap value of AC and memory[AR])

- Exchange is a **memory reference instruction** which swap value of AC and m[AR].
- Required clock cycle : 6 (T0 – T5)
- INSTRUCTION :

T0 : AR <- PC

T1 : IR <- M[AR] , PC <- PC +1

T2 : DECODE <- IR(12-14), I <- IR(15), AR <- IR(0-11)

D7'IT3 : AR <- M[AR]

D0T4 : DR <- M[AR]

D0T5 : M[AR] <- AC, AC <- DR, SC <- 0

2. Shift right AC :

- Shift right is register reference instruction which shift contect of AC and E.
- OPCODE of this instruction is 7003.
- Required clock cycle : 4 (T0 – T3)
- INSTRUCTION :

T0 : AR <- PC

T1 : IR <- M[AR] , PC <- PC +1

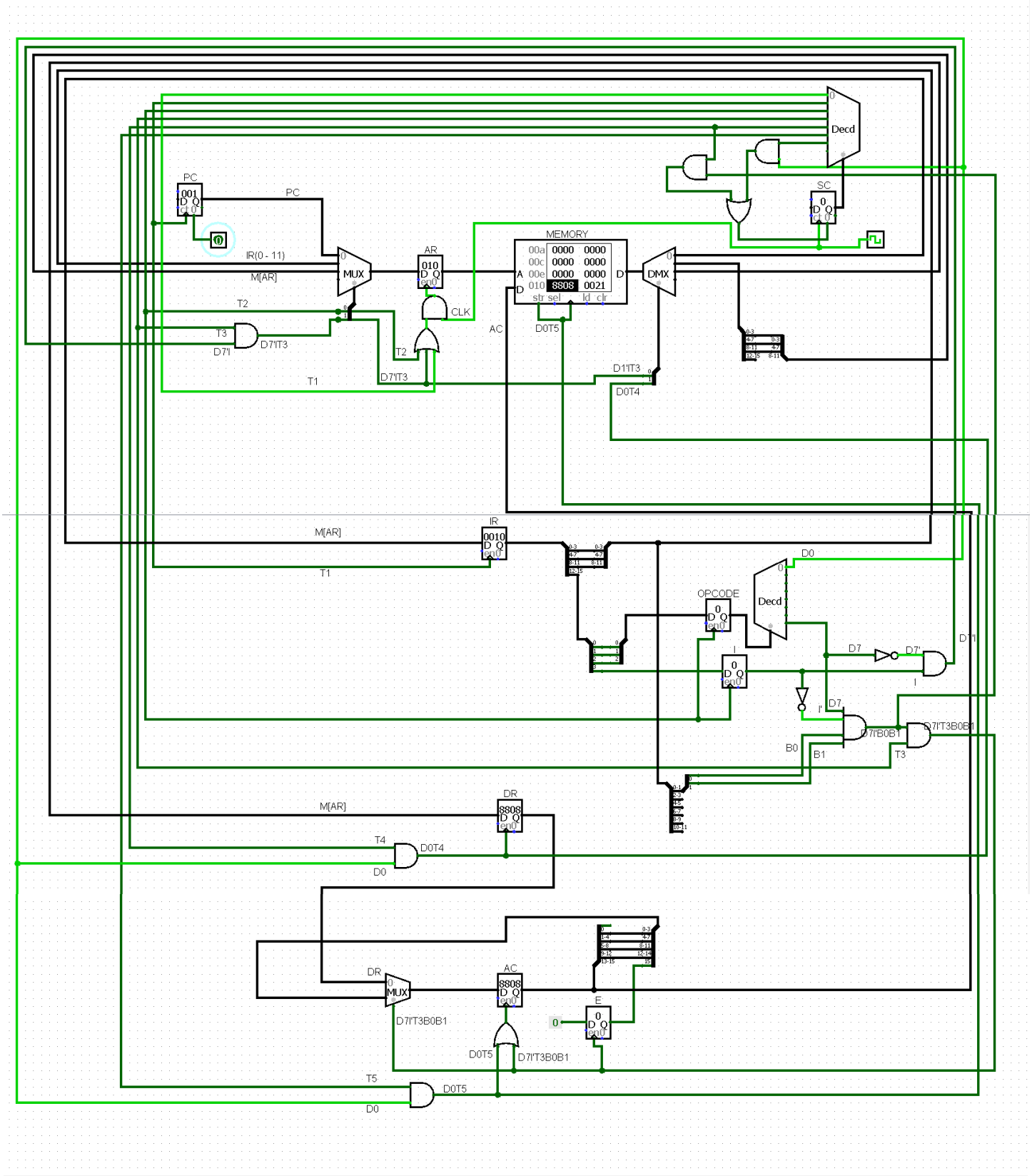
T2 : DECODE <- IR(12-14), I <- IR(15), AR <- IR(0-11)

D7I'T3B0B1 : shift right AC & E

SIZE OF ALL REQUIRED REGISTER, COUNTER AND MEMORY

- MEMORY :
    - RAM – 4094x16 bit
- REGISTER :
    - AR – 12 bits
    - IR – 16 bits
    - DR – 16 bits
    - AC – 16 bits
    - OPCODE – 3 bits
    - I – 1 bit
    - E – 1 bit
- COUNTER :
    - PC – 12 bits
    - SC – 3 bits

CIRCUIT


PC
001
PC
IR(0 - 11)
M[AR]
MUX
AR
010
CLK
MEMORY
00a 0000 0000
00c 0000 0000
00e 0000 0000
010 8808 0021
str sel ld clr
DMX
Decd
SC
T2
T3
D7'I
D7'IT3
T1
D7'IT3
AC
D0T5
D1'IT3
D0T4
IR
0010
M[AR]
T1
OPCODE
Decd
D0
I
D7
D7'
D7'I
I'
D7
D7'IB0B1
D7'IT3B0B1
B0
B1
T3
DR
8808
M[AR]
T4
D0T4
D0
DR
MUX
AC
8808
E
D7'IT3B0B1
D0T5
D7'IT3B0B1
T5
D0T5
D0