

# CA INNOVATIVE ASSIGNMENT

## TWO NEW INSTRUCTION EXUCUTION OF BASIC COMPUTER ARCHITECTURE

24<sup>TH</sup> April 2023

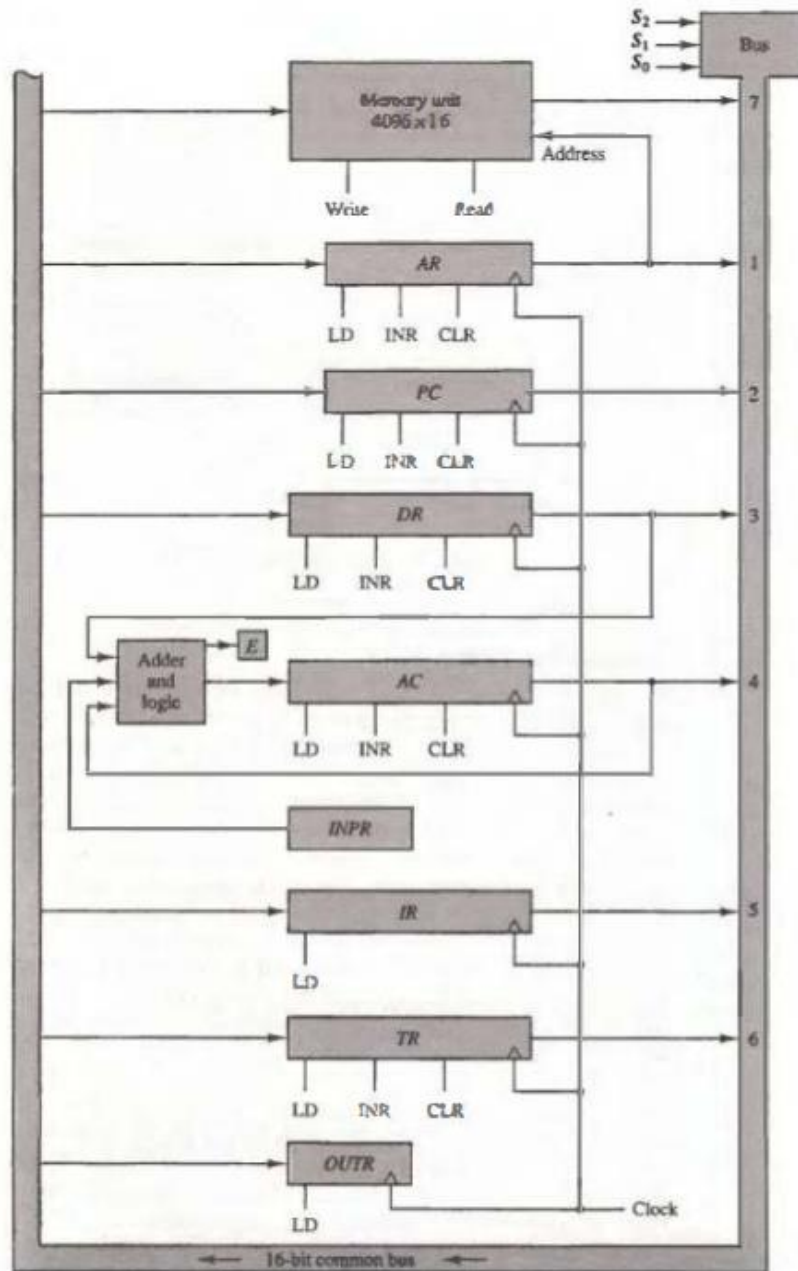
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21BCE047 – CHINTAN DETROJA  
21BCE049 – DEV BACHANI  
21BCE052 – SHYAM DHAMECHA

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# BASIC COMPUTER ARCHITECTURE

The basic computer has eight registers, a memory unit, and a control unit. Paths must be provided to transfer information from one register to another and between memory and registers.

The number of wires will be excessive if connections are made between the outputs of each register and the inputs of the other registers.



# TWO NEW INSTRUCTION

## 1. Exchange - (Swap value of AC and memory[AR])

- Exchange is a **memory reference instruction** which swap value of AC and m[AR].
- Required clock cycle : 6 ( T0 – T5 )
- INSTRUCTION :

T0 : AR <- PC

T1 : IR <- M[AR] , PC <- PC + 1

T2 : DECODE <- IR(12-14), I <- IR(15), AR <- IR(0-11)

D7'T3 : AR <- M[AR]

D0T4 : DR <- M[AR]

D0T5 : M[AR] <- AC, AC <- DR, SC <- 0

## 2. Shift right AC :

- Shift right is register reference instruction which shift content of AC and E.
- OP CODE of this instruction is 7003.
- Required clock cycle : 4 ( T0 – T3 )
- INSTRUCTION :

T0 : AR  $\leftarrow$  PC

T1 : IR  $\leftarrow$  M[AR] , PC  $\leftarrow$  PC + 1

T2 : DECODE  $\leftarrow$  IR(12-14), I  $\leftarrow$  IR(15), AR  $\leftarrow$  IR(0-11)

T3 : shift right AC & E

# SIZE OF ALL REQUIRED REGISTER, COUNTER AND MEMORY

- MEMORY :

- RAM – 4096x16 bit

- REGISTER :

- AR – 12 bits
- IR – 16 bits
- DR – 16 bits
- AC – 16 bits
- OP CODE – 3 bits
- I – 1 bit
- E – 1 bit

- COUNTER :

- PC – 12 bits
- SC – 3 bits

The diagram illustrates a 16-bit computer architecture with the following components and connections:

- PC (Program Counter):** A 16-bit register (001) that outputs IR(0-11) to the MUX and M[AR] to the Memory.
- IR (Instruction Register):** A 16-bit register (0010) that outputs to the MUX and the DMX.
- Memory:** A 16x16 memory array (00a) that outputs to the DMX and the AC.
- AC (Accumulator):** A 16-bit register (8808) that outputs to the DMX and the E register.
- AR (Address Register):** A 16-bit register (010) that outputs to the MUX and the DMX.
- DMX (Data Multiplexer):** A 16-to-1 decoder (0) that outputs to the AC and the E register.
- Decd (Decoder):** A 4-to-1 decoder (0) that outputs to the DMX and the E register.
- OPCODE (Operation Code):** A 4-bit register (0) that outputs to the DMX and the E register.
- DR (Data Register):** A 16-bit register (8808) that outputs to the DMX and the E register.
- E (Enable Register):** A 16-bit register (0) that outputs to the DMX and the E register.
- Logic Gates:** AND, OR, NOT, XOR, and MUX gates are used to control the flow of data between registers and memory.
- Shift Registers:** Two 16-bit shift registers (00a) are used to shift data between registers and memory.