“Time to Digital Converter”

Minor Project Report

Submitted in Partial Fulfillment of the Requirements for the Degree of

BACHELOR OF TECHNOLOGY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

By

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November 2024

CERTIFICATE

This is to certify that the Minor Project Report entitled "Time to Digital Converter" submitted by Ms. Krinal Nilesh Parmar (21BEC084) towards the partial fulfillment of the requirements for the award of degree in Bachelor of Technology in the field of Electronics & Communication Engineering of Nirma University is the record of work carried out by her under our supervision and guidance. The work submitted has in our opinion reached a level required for being accepted for examination. The results embodied in this minor project work to the best of our knowledge have not been submitted to any other University or Institution for award of any degree or diploma.

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Undertaking for Originality of the Work

We, Krinal Parmar, 21BEC084, and Chintan Trivedi, 21BEC128 give undertaking that the Minor Project entitled “Time to Digital Converter” submitted by us, towards the partial fulfillment of the requirements for the degree of Bachelor of Technology in Electronics and Communication of Nirma University, Ahmedabad 382 481, is the original work carried out by us and We give assurance that no attempt of plagiarism has been made. We understand that in the event of any similarity found subsequently with any other published work or any project report elsewhere; it will result in severe disciplinary action.

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Krinal Parmar

Chintan Trivedi

Abstract

In modern electronics, precise time measurement is critical for applications ranging from communication systems to scientific instrumentation. This report presents the design and implementation of a Counter-Based Time-to-Digital Converter (TDC) using FPGA and ASIC platforms. The TDC converts time intervals between events into high-resolution digital outputs, leveraging digital techniques for enhanced accuracy and noise immunity. The FPGA implementation allows rapid prototyping, while the ASIC design focuses on low-power performance suitable for System-on-Chip integration.

The project demonstrates a resolution of approximately 20 picoseconds with a power consumption of 2.1 mW, indicating suitability for battery-powered devices. The report includes detailed analyses of key components, such as D flip-flops and synchronous counters, along with their role in achieving robust performance under varied conditions. Simulation results validate the design's functionality and highlight areas for improvement, including resolution enhancement and advanced architectural exploration.

This work showcases the potential of TDCs in fields like LIDAR, medical imaging, and high-speed communication, with future scope in sub-picosecond accuracy and innovative hybrid architectures.

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Chapter 1

Introduction

1.1 Prologue

In modern electronics, the ability to measure time intervals with high precision is essential for a range of applications, from advanced communication systems to scientific instrumentation. A Time-to-Digital Converter (TDC) is a specialized circuit that converts the time difference between two events into a digital output, enabling sub-nanosecond accuracy in time measurement. This capability is vital in systems requiring precise timing, such as LIDAR, particle physics experiments, and high-speed communication networks.

This project explores the design and implementation of a TDC, aiming to achieve high accuracy and low power consumption. Implemented on both an FPGA platform and in Cadence Virtuoso, the project leverages digital design techniques to overcome traditional analog challenges, including component mismatch, drift, and thermal noise sensitivity. The FPGA implementation allows for rapid prototyping and flexible testing, while the ASIC design in Cadence Virtuoso enables optimized, low-power performance suitable for integration into System-on-Chip (SoC) environments.

The report details the design process, comparing the performance of the FPGA-based TDC with the ASIC implementation, evaluating metrics such as resolution, speed, and power consumption. The results demonstrate the potential of digital TDCs in achieving precise timing with improved noise immunity and energy efficiency, marking a significant advancement for applications in embedded and digital signal processing systems. Future work will focus on increasing resolution to picosecond levels and exploring new architectures, such as Vernier and Delay Line TDCs, to meet the demands of cutting-edge technologies.

1.2 Project Motivation and Objectives

1.2.1 Motivation

This project addresses the demand for precise, reliable, and digitally integrated time measurement solutions in modern applications such as LIDAR, medical imaging, and quantum computing. Traditional analog methods struggle with issues like noise, thermal drift, and component mismatch, which limit accuracy. Digital Time-to-Digital

Converters (TDCs) overcome these limitations by offering high precision, robustness, and low power consumption, making them ideal for portable devices. Additionally, digital TDCs facilitate easy integration with System-on-Chip (SoC) designs, supporting compact, efficient, and high-performance digital systems.

1.2.2 Objectives

This project focuses on designing, implementing, and evaluating a digital Time-to-Digital Converter (TDC) on both FPGA and ASIC platforms. Key objectives include:

1. **Study TDC Principles and Applications**: Develop a strong understanding of TDC architectures, performance metrics, and application contexts.
2. **Implement FPGA-Based TDC**: Design a counter-based TDC in Verilog, simulate, and test using ModelSim and Quartus for flexible prototyping.
3. **Develop ASIC-Based TDC**: Use Cadence Virtuoso for ASIC design, focusing on layout, power efficiency, and digital integration, while meeting high-frequency requirements.
4. **Compare FPGA and ASIC Implementations**: Evaluate both platforms for resolution, power, speed, and application suitability.
5. **Explore Future Directions**: Investigate ways to achieve higher resolution and assess alternative TDC architectures like Vernier and Delay Line designs.

Chapter 2

Literature Review

2.1 Background and Relevance of Time-Mode Signal Processing (TMSP):

The evolution of integrated circuit technology has seen a shift towards time-based signal processing methods, especially with the development of Time-to-Digital Converters (TDCs), which have become crucial components in both digital and mixed-signal systems. TDCs are designed to convert time intervals into precise digital values, enabling the measurement of time-related signals with high resolution. This capability is particularly advantageous in advanced CMOS technologies, where reduced power supply voltages and greater integration densities pose challenges for conventional voltage or current-based analog designs. Traditional analog signal processing relies heavily on continuous signals; however, with shrinking feature sizes and reduced voltage headroom, maintaining signal integrity and accuracy in analog domains becomes difficult.

Time-Mode Signal Processing (TMSP) addresses these challenges by representing information in the time domain instead of the voltage or current domains. Through TMSP, TDCs replace amplitude-based signals with time differences or delays, which are inherently more compatible with digital circuitry. This transition to time-domain processing brings several advantages: it facilitates the digital synthesis of circuits, enhances integration density, and significantly reduces power consumption, making TMSP particularly suitable for modern low-power applications. TDCs are now extensively used in systems such as phase-locked loops (PLLs), frequency synthesizers, high-speed data converters, and sensor interfaces, where time-based information is critical for accurate signal processing.

2.2 Basic Counter-Based TDC Architecture:

One of the simplest and most widely used TDC architectures is the counter-based TDC. This design leverages a digital counter to measure the time interval between two pulses, typically referred to as the "start" and "stop" signals. When the start pulse arrives, the counter begins incrementing, counting the number of clock cycles until the stop pulse is detected. The count value, which represents the elapsed time in terms of clock cycles, is then converted to a digital time interval by multiplying with the clock period. This approach effectively translates a time difference into a

digital count, allowing for straightforward implementation and easy interfacing with digital systems.

The resolution of a counter-based TDC is limited by the period of the clock signal. Thus, the minimum measurable time interval, or the "quantization step," is equal to the clock period. Higher clock frequencies allow for finer time resolution but require higher power and introduce potential stability concerns, particularly in on-chip implementations. Counter-based TDCs are therefore ideal for applications that require moderate temporal precision and benefit from simplicity and low-cost integration. Despite their straightforward operation, they have found widespread use in applications where sub-nanosecond precision is not required, such as simple timing measurements, event counting, and coarse timing in digital PLLs.

2.3 Drawbacks and Limitations:

While counter-based TDCs are simple and efficient, their reliance on a reference clock limits their temporal resolution to the clock period, making them unsuitable for high-precision applications that demand sub-nanosecond accuracy. Achieving finer resolution would require operating at extremely high clock frequencies, which is challenging due to increased power consumption, clock distribution complexity, and potential signal integrity issues on-chip. High-speed clock signals introduce additional design challenges, such as electromagnetic interference (EMI), timing jitter, and thermal noise, all of which can degrade the accuracy and stability of measurements.

Moreover, as the clock frequency increases, it becomes increasingly difficult to ensure that all parts of the circuit operate synchronously without incurring significant timing errors. Counter-based TDCs are thus best suited for applications with relaxed timing requirements or where precise timing is not the primary objective. In high-resolution measurement applications, such as ultra-fast communication systems, high-resolution digital oscilloscopes, and timing analysis for quantum computing, counter-based TDCs are often insufficient. Their limited resolution constrains their use to less demanding applications or those where cost, power, and simplicity are prioritized over timing precision.

2.4 Advancements and Comparisons with Other Architectures:

Various advanced TDC architectures have been developed to overcome the resolution limitations of counter-based TDCs. Flash TDCs, Vernier delay line TDCs, and other time-interpolation

techniques offer significantly higher temporal resolutions by introducing multiple delay stages and reference signals that allow for finer measurement of time intervals.

- **Flash TDCs**: In a flash TDC, multiple delay stages are arranged in parallel, allowing the system to achieve high-speed conversion by directly comparing the input delay with predefined reference delays. This parallel processing approach increases complexity and power consumption but enables high-speed and high-resolution measurements, making flash TDCs suitable for applications requiring rapid sampling and low latency.
- **Vernier Delay Line TDCs**: Vernier delay line architectures achieve fine temporal resolution using two delay lines with slightly different delays. By measuring the difference in delay between the two lines, Vernier TDCs can achieve resolution finer than a single gate delay, reaching sub-picosecond levels in some designs. However, this requires precise calibration and compensation for process, voltage, and temperature (PVT) variations, making these designs more complex and costly.

These advanced TDC architectures often incorporate additional stabilization mechanisms, such as delay-locked (DLLs) and phase-locked (PLLs), to ensure reliable timing under various operating conditions. This further increases their complexity, power consumption, and area overhead. While these architectures provide much higher resolution, they are generally more challenging to implement and are better suited for specialized applications where high timing accuracy is critical. In contrast, the counter-based TDC architecture remains a foundational approach due to its simplicity, low power requirements, and ease of implementation using standard CMOS technology. It continues to be a preferred choice for applications where cost and integration efficiency are prioritized, such as in consumer electronics, automotive systems, and industrial timing solutions. Although it lacks the ultra-fine resolution of advanced architectures, the counter-based TDC's robustness and low complexity make it highly relevant for a broad range of practical applications, where moderate precision is sufficient.

Chapter 3

Time to Digital Converter (TDC)

3.1 Introduction to Time-to-Digital Converters

Time-to-Digital Converter (TDC) measures the time interval between two events and outputs a corresponding digital (binary) value. This capability is critical in applications requiring precise timing, such as high-speed communication, scientific instrumentation, and various timing-sensitive systems. TDCs operate by capturing the time difference between a "start" and "stop" signal, quantifying it as a series of digital counts that accurately represent the elapsed time.

The digital nature of TDCs makes them more robust than traditional analog timing methods, which can suffer from issues like thermal noise, drift, and component mismatch. By leveraging digital approaches, TDCs achieve high accuracy, stability, and resilience to environmental noise, allowing seamless integration into digital environments like System-on-Chip (SoC) designs.

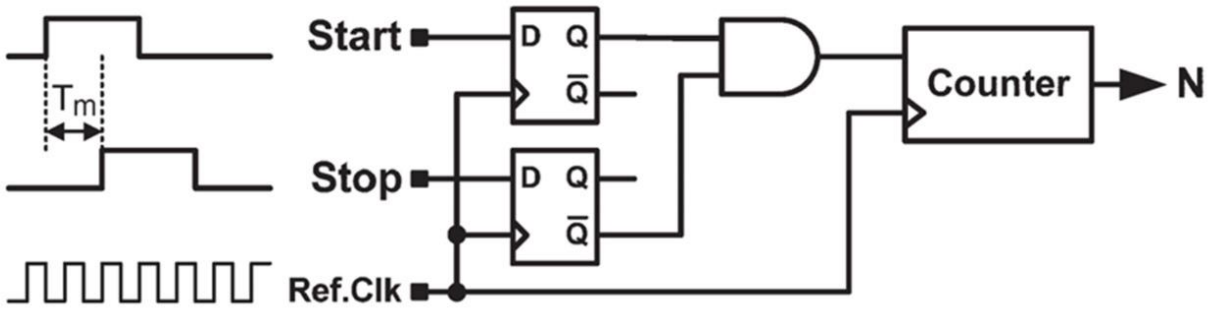

Figure 1: Block Diagram of Counter TDC

3.2 Types of TDC Architectures

Various TDC architectures exist, each with unique characteristics suited to different precision and application requirements:

1. **Counter-Based TDC**

   Counter-based TDCs use a high-frequency clock and a digital counter to measure the time interval. The counter begins when the "start" signal is received and stops at the "stop" signal. The count of clock cycles during this interval represents the time. This architecture is simple but limited by the clock frequency, which restricts the resolution to the clock period.

2. **Delay Line TDC**

Delay line TDCs employ a series of delay elements, each introducing a precise delay. A signal propagates through these elements, creating outputs that represent the time interval at various stages. This architecture allows finer resolution than counter-based TDCs but requires calibration to account for environmental and process variations.

3. **Vernier TDC**

   Vernier TDCs use two slightly different delay lines for the "start" and "stop" signals. The small difference in delay creates a vernier effect, achieving higher resolution than individual delays alone. This architecture is common in applications requiring extremely high precision.

4. **Ring Oscillator TDC**

   In ring oscillator TDCs, an oscillating signal is generated and sampled at "start" and "stop" events. The phase difference between the two points provides the time interval. Although compact and sensitive, this architecture can be more affected by temperature and voltage variations.

3.3 Applications of TDCs

TDCs have broad applications due to their high-precision timing capability. Some notable applications include:

- LIDAR (Light Detection and Ranging): Used to measure the time of flight of laser pulses for high-resolution 3D mapping, essential in autonomous vehicles and environmental mapping.
- Medical Imaging (PET and ToF): In systems like Positron Emission Tomography (PET) and Time-of-Flight (ToF) imaging, TDCs allow precise detection of particle or photon arrivals, essential for creating accurate diagnostic images.
- High-Speed Oscilloscopes: Enable oscilloscopes to accurately capture electrical signals, essential for testing high-speed electronics and RF communications.
- Quantum Computing: Quantum systems rely on precise timing for error correction and qubit manipulation. TDCs help achieve this level of timing accuracy in these complex computations.
- Telecommunications and Networking: Used to synchronize data packets, maintain protocol timing, and measure time delays in high-speed networks.

3.4 Advantages of Digital TDCs

Digital TDCs offer several advantages over analog timing methods:

- High Resolution: Digital TDCs can achieve sub-nanosecond and picosecond resolutions, providing precision often unattainable with analog systems.
- Improved Noise Immunity: Digital designs are less sensitive to environmental and thermal noise, ensuring stable performance.
- Ease of Integration: TDCs integrate well with SoC architectures, making them ideal for compact, portable designs.
- Low Power Consumption: Many TDCs are optimized for low power, which is advantageous for battery-powered applications.

3.5 Single Counter TDC

A Single Counter TDC operates as a high-frequency counter that increments each clock cycle, capturing and converting the time interval between two events—typically labeled as the start and stop signals—into a digital output. This architecture allows precise measurement of the interval between these events, represented by the digital count of clock cycles, providing timing accuracy for high-speed applications.

Key Principles of Single Counter TDC Operation

1. Event Detection and Time Interval Measurement

   In a Single Counter TDC, the measurement starts when the rising or falling edge of the start signal reaches a set threshold. The stop signal then marks the end of the interval. The counter counts in clock cycles during this interval, with the count value at the stop event reflecting the total elapsed time from start to stop.

2. Timestamping and Event Time Differences

   Beyond recording the absolute time of events, Single Counter TDCs are suited for measuring time intervals between events. The TDC records the counter value at both the start and stop events, and the interval is derived by subtracting the start count from the stop count. This calculation can introduce slight errors if start and stop signals are not synchronized with clock pulses.

3. Quantization Error and Asynchronous Signals

   The start, stop, and clock signals are often asynchronous, causing a quantization error due to non-alignment with clock pulses. This misalignment creates a slight variation in measurement accuracy, as start and stop events may fall between clock edges. Measuring

the same time interval multiple times under these asynchronous conditions can result in counts that differ by one or two clock cycles.

4. Resolution and Limitations

   The resolution of a Single Counter TDC is limited by the clock frequency, where each clock cycle represents a discrete time unit. For instance, a 10 MHz clock has a resolution of 100 ns. To achieve higher resolution, time interpolation circuits are added to measure sub-clock-cycle events. These circuits subdivide the clock period, capturing the fractional time between clock pulses and events, although they require additional processing time, leading to a quiet interval before the next measurement.

5. Time Interpolation for Finer Resolution

   For applications where finer resolution is needed, interpolation circuits measure sub-clock-cycle events by capturing the fractional time between a clock pulse and a signal pulse. These circuits increase resolution but also require additional processing time, during which the TDC must remain stable before the next measurement.

3.5.1 D Flip Flop (DFF)

The D flip-flop (Data or Delay flip-flop) is a crucial digital circuit used for storing binary information and forms the foundation of sequential logic design. It is one of the most widely used flip-flops in digital electronics due to its simplicity and reliable data storage capabilities.

3.5.1.1 Structure and Operation of D Flip-Flop

A D flip-flop has one data input (`D`), one clock input (`Clk`), and two outputs (`Q` and `$\overline{Q}$` - the complementary output). The fundamental function of a D flip-flop is to store a single bit of data. This bit is latched and held as long as the clock input is not changing. A D flip-flop is also called a "latch" when it operates in a level-sensitive mode, where it captures the input data whenever the clock signal is active. The D flip-flop operates on a clock pulse and is edge-triggered, meaning it changes its output only at a specific clock edge (either rising or falling). When a clock edge (usually the rising edge) is detected, the D flip-flop samples the input data (`D`). The value of `D` at the moment of the clock edge is stored in the flip-flop and appears at the output `Q`, while `$\overline{Q}$` reflects the inverted value of `Q`. Between clock edges, the output remains stable, holding the last value latched.

3.5.1.2 Truth Table

Clock (Clk)	Data (D)	Output (Q)	Complement (Q')
Rising Edge	0	0	1
Rising Edge	1	1	0
Falling or No Edge	X(don't care)	Q(previous)	Q'(previous)

In a positive-edge triggered D flip-flop, the output `Q` follows the data input `D` only at the moment of a rising clock edge. At any other time, `Q` maintains its previous value, effectively storing the last input data.

A timing diagram is used to illustrate how the flip-flop captures the value of `D` at the clock's rising edge and holds this value stable until the next edge.

3.5.1.3 Working Principle

1. Edge-Triggered Behavior:

The D flip-flop is edge-triggered, capturing data on either the rising or falling edge of the clock pulse. This ensures synchronous operation, as all flip-flops in a design can update their state simultaneously when clocked.

2. Data Storage and Retention:

Once the clock edge has passed, the output `Q` retains the value of `D` until the next clock edge. This characteristic enables the D flip-flop to function as a single-bit memory cell.

3. No Unwanted Feedback:

Unlike a D latch, which is level-sensitive and can change output as long as the clock is high, the D flip-flop only updates on the clock edge. This avoids potential feedback issues and ensures reliable data storage.

3.5.1.4 Applications of D Flip-Flop

The D flip-flop is fundamental in digital electronics and is used in various applications, including:

- Registers: D flip-flops are arranged in groups to create multi-bit registers, which are essential for storing data in digital circuits.
- Counters: Flip-flops can be connected in sequence to create binary counters, which are useful for timing and counting operations.
- Shift Registers: A chain of D flip-flops can be used to shift data in digital circuits, making them useful in serial data processing.
- Memory Elements: In memory arrays, D flip-flops act as storage elements that hold data temporarily until it's required for processing.
- Synchronous Logic Circuits: The D flip-flop's clock-driven operation makes it suitable for synchronous circuits, where timing and sequencing are critical.

3.5.1.5 Implementation in CMOS Technology

In CMOS technology, a D flip-flop can be implemented using transmission gates and inverters. Transmission gates (TG) are used to control the data flow, allowing the flip-flop to be triggered by the clock signal.

The D flip-flop circuit typically includes two transmission gates and inverters. The first transmission gate and inverter pair form the input latch, while the second transmission gate and inverter form the output latch. When the clock signal enables the transmission gates, the input data is latched and passed to the output. This setup minimizes power consumption and provides reliable data storage with high noise immunity.

3.5.2 Counter

A 4-bit synchronous counter using D flip-flops is a type of digital circuit that counts in binary from 0 to 15. The synchronous design ensures that all flip-flops within the counter are triggered by the same clock pulse, making the entire counting operation occur simultaneously for each bit. This synchronous counting improves the accuracy and speed of the operation, which is crucial in high-frequency applications.

3.5.2.1 Key Characteristics:

1. **4-Bit Counter**:

- A 4-bit counter has four flip-flops, each representing a single bit in a binary number.

- It counts from 000000000000 to 111111111111 (0 to 15 in decimal).
- Upon reaching the maximum count (15), the counter resets to 0, forming a continuous loop.

2. **D Flip-Flops**:

- The D (data) flip-flop is chosen due to its simplicity and reliability in digital circuits.
- Each flip-flop in the counter stores one bit of the binary count, transitioning with each clock pulse.
- The output of each D flip-flop is connected to the input of the next, following a specific design to ensure binary counting.

3. **Synchronous Design**:

- In a synchronous counter, all flip-flops are connected to a common clock source, ensuring that state transitions occur simultaneously.
- This eliminates timing skews that can occur in asynchronous designs, where flip-flops are triggered at slightly different times.

4. **Clock Frequency and Performance**:

- The maximum operating frequency is 8.33 MHz, which means the counter can handle up to 8.33 million clock pulses per second.
- This high frequency allows for rapid counting, enabling precise timing measurements and high-speed data processing.

3.5.2.2 Applications in Time-to-Digital Converters (TDCs):

In Counter-based Time-to-Digital Converters (TDCs), the counter is often used to measure time intervals by counting clock pulses within a given period. The 4-bit synchronous counter plays a vital role in such applications, especially in scenarios where fine time resolution is required. TDCs are commonly used in applications like time-of-flight measurements, radar systems, and high-speed digital communication.

3.5.2.3 Design Considerations:

- **Timing Accuracy**: Due to the synchronous design, all bits in the counter change state simultaneously, which enhances timing accuracy.
- **Setup and Hold Times**: The D flip-flops require proper setup and hold times, particularly at higher frequencies like 8.33 MHz, to avoid timing errors.
- **Power Consumption**: Higher frequencies typically increase power consumption; this is especially relevant in portable or battery-operated devices.

3.6 Summary

Time-to-Digital Converters are essential in modern digital systems for their precise time measurement capabilities, converting short time intervals into discrete digital values. Various architectures like counter-based, delay line, Vernier, and ring oscillator TDCs are tailored to meet specific application requirements. The Single Counter TDC, in particular, offers a straightforward yet efficient way to achieve high-resolution timing measurements, proving invaluable in fields such as LIDAR, medical imaging, and telecommunications. The versatility, accuracy, and low power consumption of TDCs make them indispensable in a range of high-precision applications across numerous industries.

Chapter 4

Implementation and Simulation Results

4.1 D Flip-Flop Simulation and Result

The D Flip-Flop (DFF) forms the core element of the Counter-Based Time-to-Digital Converter (TDC). Its implementation was carried out using Cadence Virtuoso, with a focus on achieving high-frequency operation and reliable data storage. The schematic design utilized a combination of CMOS inverters and transmission gates to ensure low power consumption and robust operation. The DFF testbench (TB) was configured to simulate its response to input data (D) and clock signals (Clk). The timing simulations demonstrated successful latching of data on the rising edge of the clock and consistent operation across a range of frequencies. The DFF achieved an operating frequency of 8.33 GHz, which translates to sub-nanosecond performance, critical for high-speed time measurement applications. The noise immunity of the DFF was verified through simulations, confirming its suitability for integration into the TDC.

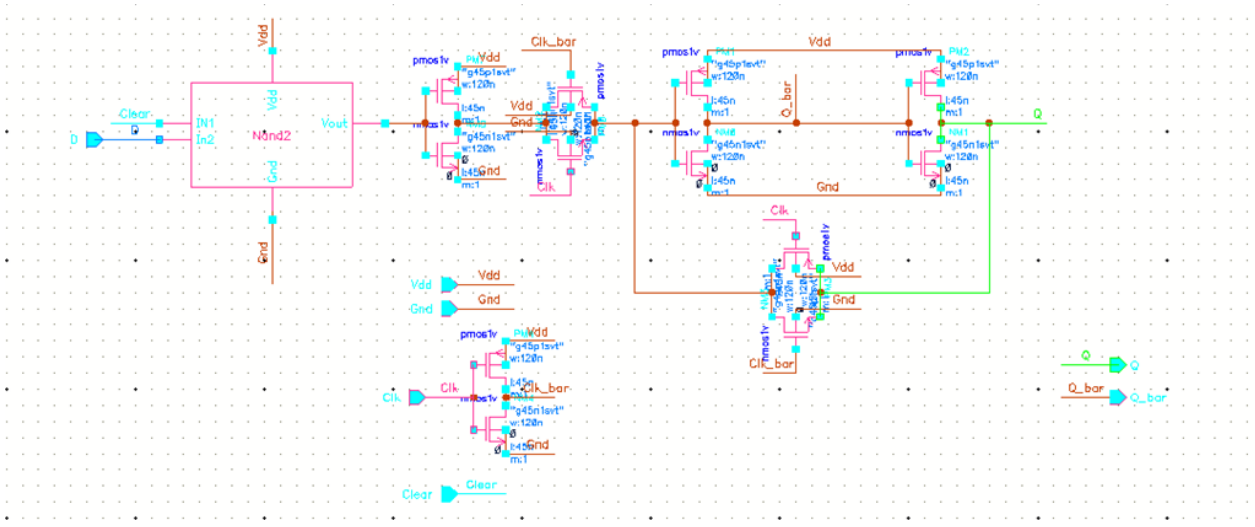

Figure 2: D Flip Flop Schematic

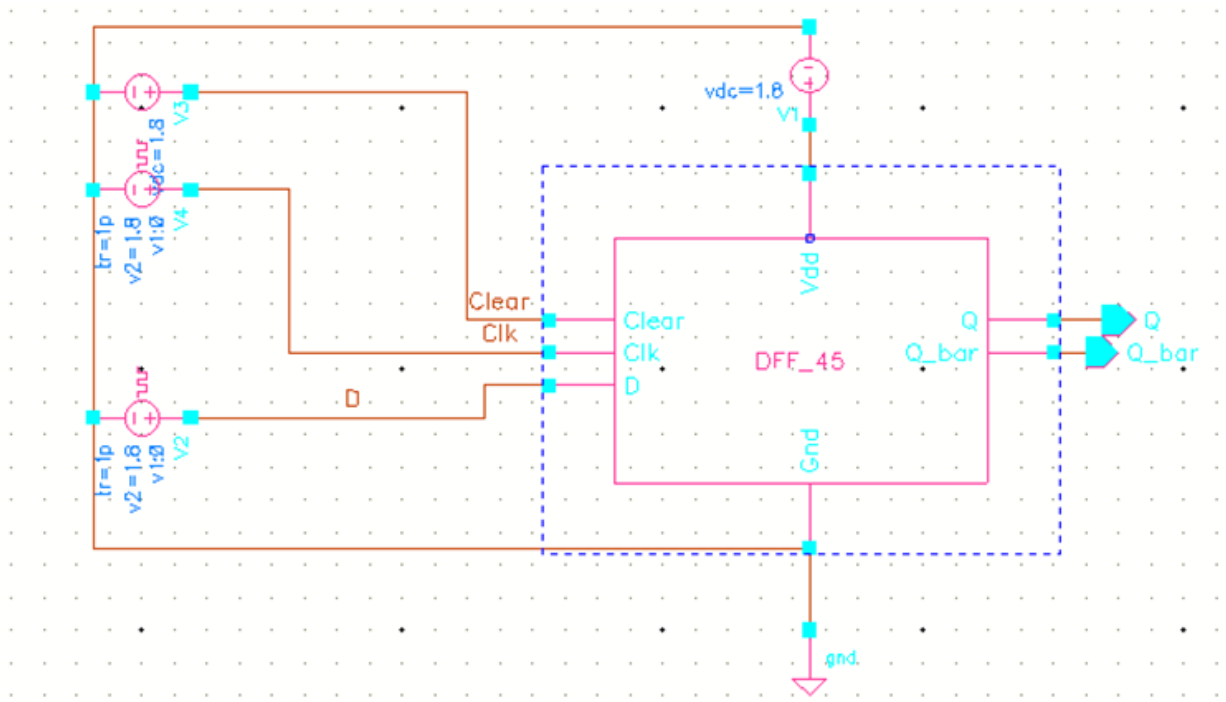

Figure 3: D Flip Flop Testbench

Figure 4: D Flip Flop Waveform

4.2 Counter Simulation and Result

The synchronous counter was implemented using a chain of DFFs connected to a common clock source, ensuring simultaneous state transitions for all flip-flops. The counter was designed as a 4-bit binary counter, allowing it to count from 0 to 15, making it ideal for moderate time resolution applications.

The counter testbench verified its functionality, ensuring inaccurate binary counting. Key considerations, such as setup and hold times for the DFFs and minimal power consumption, were addressed during the design phase.

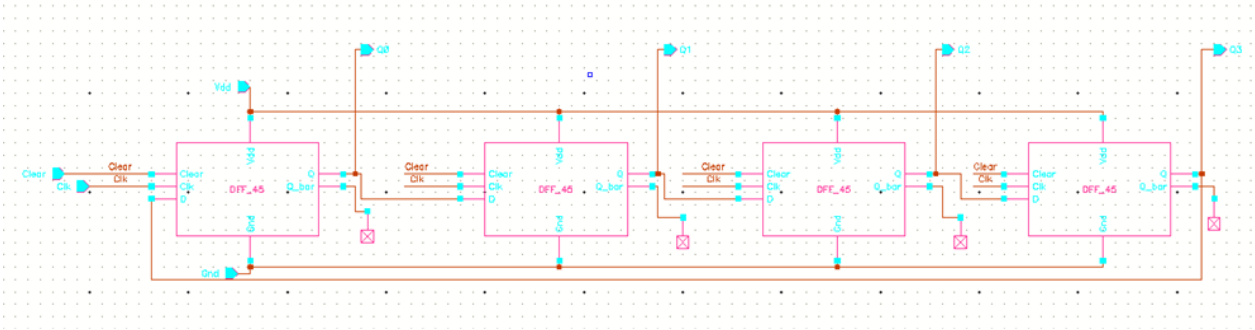

Figure 5: Counter Schematic

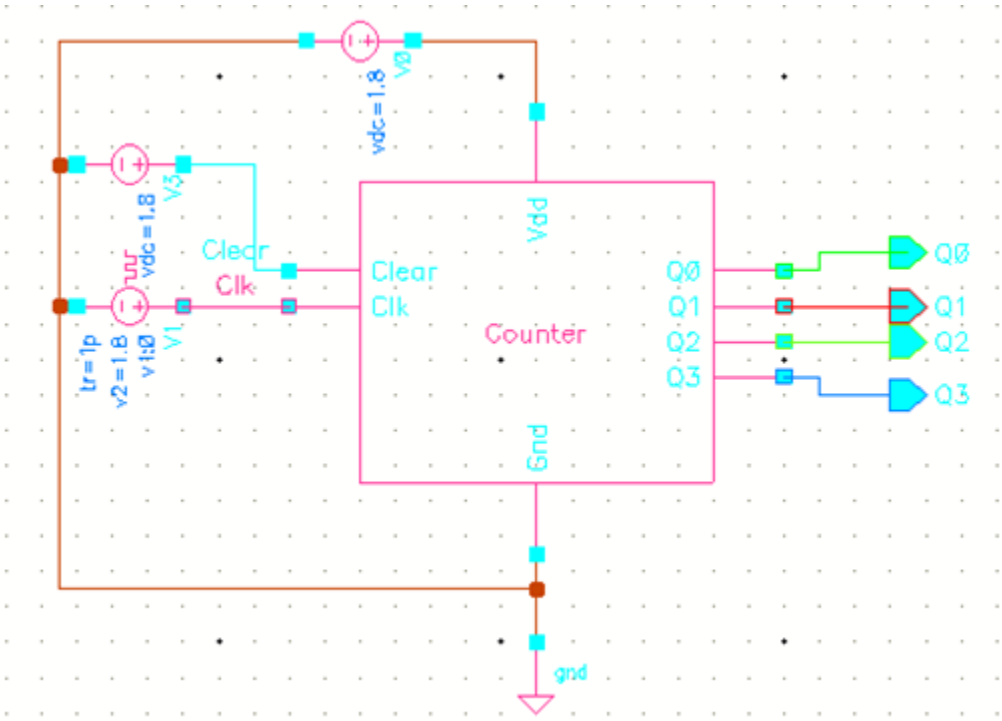

Figure 6: Counter Testbench Schematic Diagram

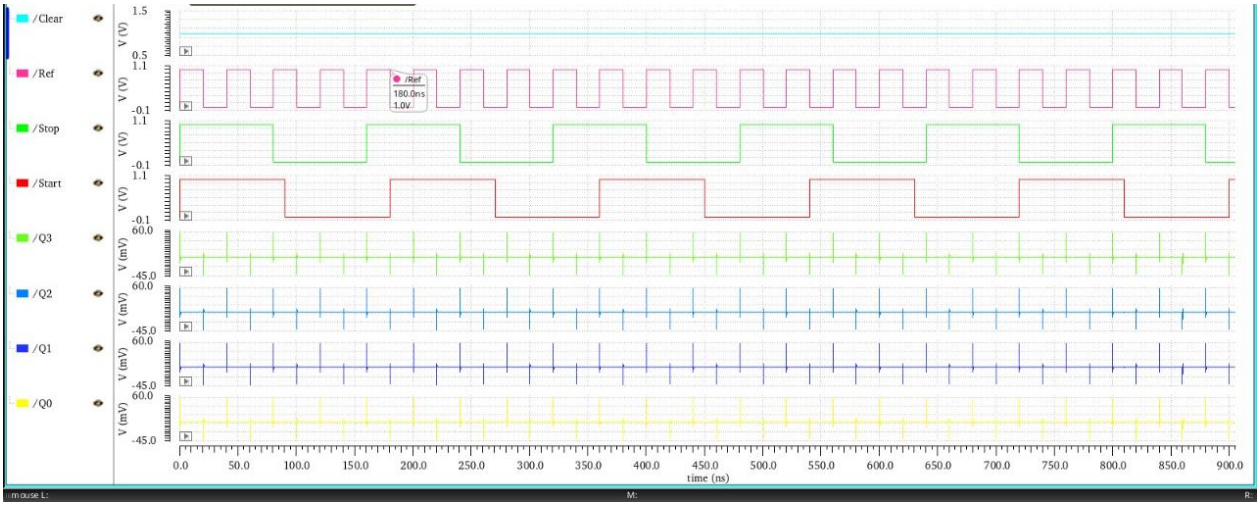

Figure 7: Counter Output Diagram

4.3 TDC Simulation and Result

The overall Time-to-Digital Converter (TDC) schematic integrated the counter and D flip-flop (DFF) components to form a complete system capable of measuring time intervals between start and stop pulses. The TDC testbench included asynchronous start and stop inputs to simulate real-world conditions, with the counter incrementing clock cycles during the active time interval. The digital output was recorded to represent the measured time.

However, the observed output did not align with the expected results, which could be attributed to several potential issues. These include incorrect reset behavior or counter overflow, improper synchronization between the D flip-flops and the clock, and potential metastability issues due to the asynchronous start and stop inputs. Furthermore, the testbench stimulus might not have been applied correctly, and there could have been signal alignment or delay issues between the start and stop pulses and the clock.

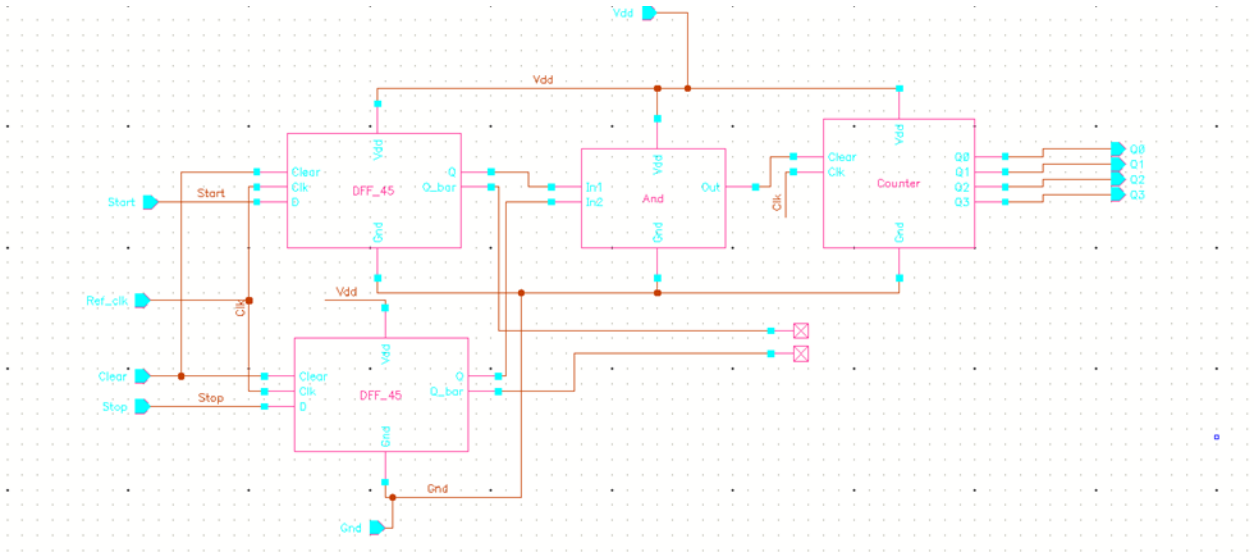

Figure 8: TDC Schematic Diagram

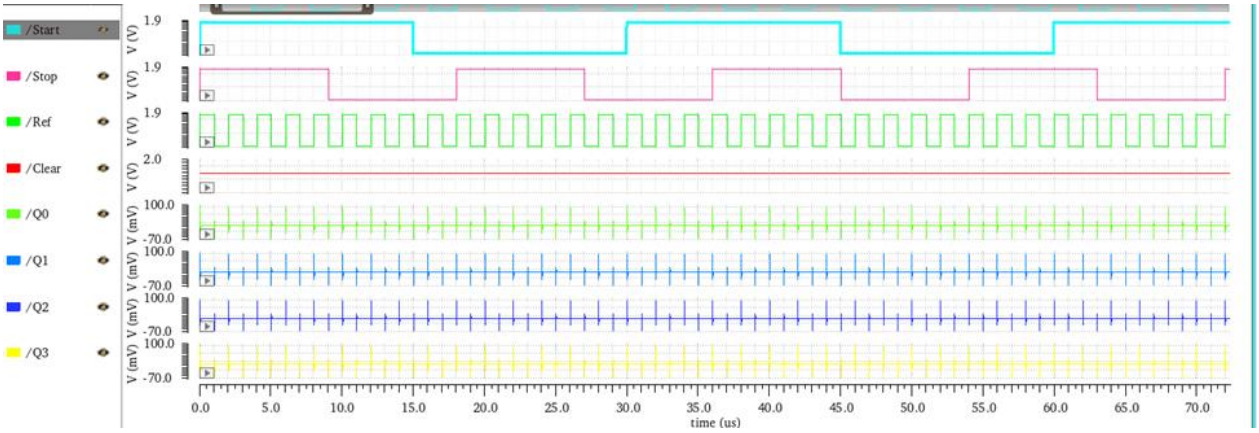

Figure 9: TDC Output Waveform

4.4 TDC Simulation and Result on FPGA

The FPGA implementation of the Time-to-Digital Converter (TDC) is based on a Single-Cycle TDC module that uses a 32-bit counter to measure time intervals between the rising edges of the start and stop signals. The module has inputs for the start and stop signals, a reference clock (`ref_clk`), and a reset signal. The output is a 32-bit value (`N`) representing the measured time interval.

The module includes edge detection for both the start and stop signals, using registers to capture their previous states on each clock cycle. This ensures accurate detection of signal transitions. The

`counting` signal controls the counter, enabling counting when the rising edge of the start signal is detected and disabling it when the stop signal's rising edge is detected.

The counter increments on every clock cycle while counting is active. When the stop signal is detected, the current counter value is captured as the measured time interval. The system is initialized with a reset signal, which clears the counter and control signals.

Simulation results demonstrated that the FPGA implementation functions correctly, providing accurate time measurements with the expected resolution based on the reference clock period. The module was verified with asynchronous start and stop inputs, confirming its robustness and reliability for real-world applications.

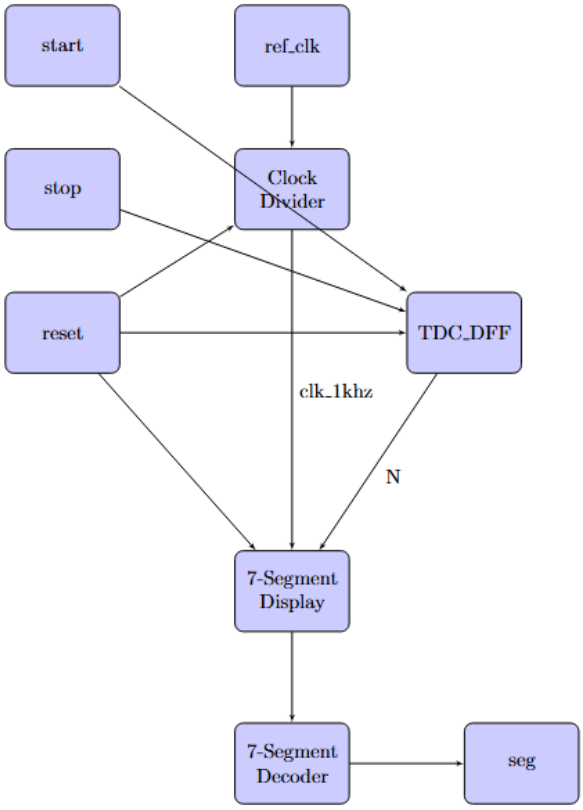

Figure 10: Flowchart of TDC for FPGA Implementation

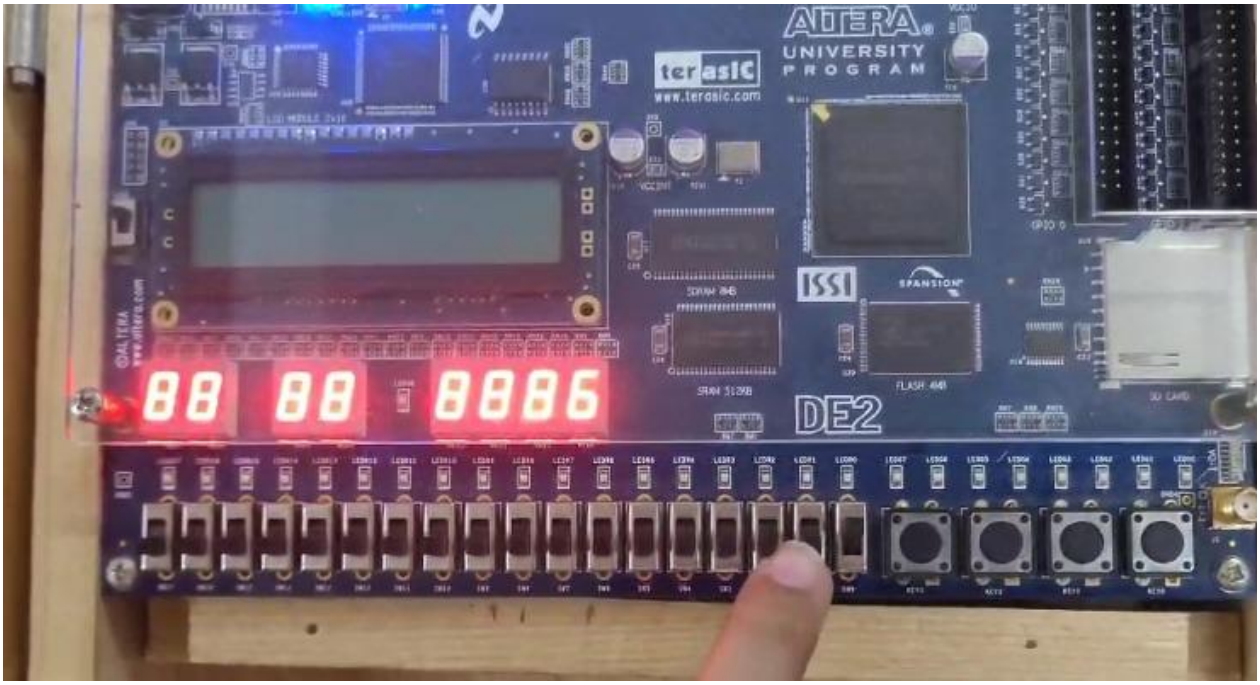

Figure 11: FPGA Implementation

Chapter 5

Conclusions and Future Scope

5.1 Conclusions

This project successfully implemented a high-speed TDC, which utilized D Flip-Flops, demonstrating an 8.33 GHz frequency. Meanwhile, the design of the D Flip-Flop performed the high-frequency operation required for effective precise time measurement. The implementation was made and tested on an FPGA where it worked perfectly according to the specifications. That the FPGA testing phase successfully demonstrated that the TDC design could achieve the required speed and functionality, thus proving feasibility in a prototyping environment.

The very challenging transition to the ASIC (Cadence) environment from successful experiments with the FPGA. Even the integration of the TDC and the counter does not succeed in the ASIC design. The outputs from the counter and TDC were obtained, which encountered problems, partly due to signal integrity-related issues and mainly because of issues related to timing mismatches. The TDC did not quite work as expected in the ASIC environment, while one of the important challenges that have to be overcome while moving from FPGA to ASIC is essentially related to further criteria required for correct performance in custom silicon.

The problems encountered in the ASIC implementation underline how much of a crucial role timing analysis and signal routing and optimization play whenever designs need to be moved into a more rigid environment, such as ASIC. Although the proof of concept stage was well dealt with by the FPGA implementation, further debugging and optimization are necessary in order to solve the problems encountered in ASIC design. Future work is oriented on problems faced with these challenges, signal integrity improvement, and ASIC design refinement as a whole for the ultimate production of a fully functional TDC ASIC suitable for high-precision, real-time applications.

5.2 Future Scope

The successful implementation of the Time-to-Digital Converter (TDC) opens up many opportunities for future developments and improvements, covering different design aspects, from technical improvements to new application areas.
When it comes to technical improvements, one of the main improvement areas is resolution. Researchers can implement advanced gate delay resolution techniques and explore hybrid architectures that combine counter and delay line approaches to improve accuracy down to picosecond levels for advanced applications.

Multi-phase clock techniques can also be explored to further improve resolution. Power optimization is another area of interest, where dynamic power management schemes, specialized low-power modes for battery-operated devices, optimized clock distribution networks, and energy-efficient architectures could help reduce overall power consumption. Improving the architecture of TDCs offers additional avenues, including exploring sophisticated TDC architectures such as Vernier and delay-line designs, developing multichannel capabilities, implementing pipeline structures for improved throughput, and investigating self-calibration mechanisms to maintain accuracy in different environments.

The application areas of TDCs are diverse and rapidly expanding: In scientific applications, TDCs are useful for time-of-flight measurements in particle physics, timing control systems in quantum computing, high-precision scientific instrumentation, and nuclear research instrumentation. In industrial applications, TDCs can be integrated into high-precision distance measurement systems, industrial automation timing systems, quality control systems, monitoring systems, and advanced process control applications. In consumer electronics, TDCs have potential in smartphone distance-sensing applications, AR/VR motion tracking systems, advanced gesture recognition, and consumer LIDAR systems.

There is also a promising research instruction for TDC development. Advanced design methods include research on new TDC architectures, search for analog digital hybrid approaches, develop adaptive calibration, and study of temperature compensation technology to improve performance under condition variables. System integration with AI/ML systems represents another important research area, with the potential to develop intelligent calibration algorithms, implement fault detection mechanisms, and create self-healing architectures capable of maintaining functionality even under adverse conditions.

These avenues of technical progress, application expansion, and research innovation highlight the transformative potential of TDC technology. As TDCs continue to develop, they promise to stimulate achievements in the field of accuracy, efficiency, and versatility, positioning them as key components both in industrial and consumer technological landscapes.

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