EE 5323

Fall 2024, Yu (Kevin) Cao

Project 1

Due Friday, October 10, 6:00pm, submitted to Canvas.

Submission: Prepare a concise report (**< 5 pages**) with important results only. You don't have to include the entire set of your circuit schematics or layout plots. Place the report in Assignment at Canvas with the filename as: EE5323_Project_1_your name.

The objective of this software lab is to exercise SPICE circuit simulations with Cadence tools. The technology used in this course is TSMC 16nm. V_{DD}=0.8V.

0. SPICE startup

Get familiar with the tools and the simulation environment. No submission needed for this problem.

1. Technology characteristics

Figure 1 shows a single NMOS and PMOS. In this problem, we calibrate the IV characteristics of this 16nm technology. Each transistor has 8 fins.

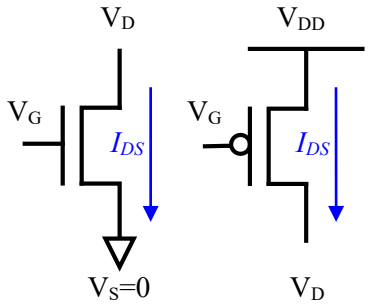

Figure 1. Single transistors

a. For the NMOS,
(1) Plot out I_{DS} vs. V_{DS} in one figure, for V_{GS}=0.05V-V_{DD}, at the step size of **150mV**; V_{DS}=0-V_{DD}, at the step size of 1mV;
(2) Plot out log(I_{DS}) vs. V_{GS}, for V_{DS}=0.15V and V_{DD}; V_{GS}=0-V_{DD}, at the step size of 1mV.

b. Repeat Step (1) for the PMOS transistor.

2. CMOS inverter design

Figure 2 shows the design of a CMOS inverter. Both PMOS and NMOS FinFETs have 8 fins. **C_L=10fF, which is added in the test bench, not in the schematic**.

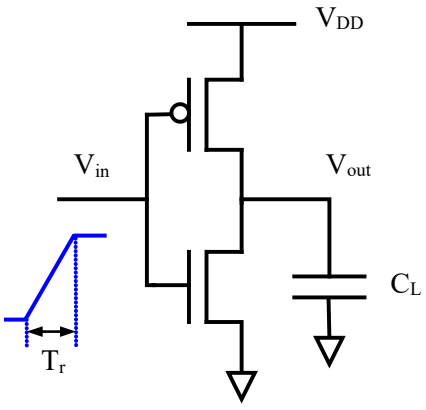

Figure 2. The schematics of a CMOS inverter

a. Plot out the voltage transfer characteristic (VTC), which is the curve of V_{out} vs. V_{in}, when V_{in} sweeps from 0 to V_{DD}.

b. Apply a ramp input to V_{in}, which is a 0 to V_{DD} switching, with the transition time T_r=20ps (as shown in Figure 2). Plot out the waveform of V_{out}. Measure the 50% V_{DD} delay (i.e., time difference from the 50% point of input to the 50% point of output) and the time for V_{out} to transit from 90%-10% V_{DD}.

3. A NMOS only inverter

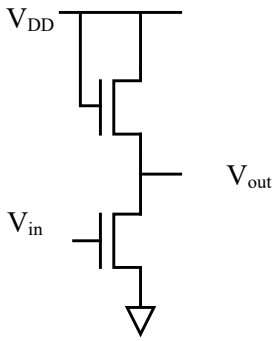

Figure 3. A NMOS only inverter

Figure 3 shows the design of an inverter with NMOS only. Both NMOS transistors have 8 fins.

a. Simulate the maximum and minimum voltages at V_{out}. What's the corresponding V_{in} for them?
b. Similar to a. in Prob. 2, plot out the VTC.
c. Compare this design with the CMOS inverter. What are the main disadvantages?