UNIVERSITY OF MINNESOTA

5327 VLSI DESIGN LAB (Section 004)

Project 1

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VLSI DESIGN PROJECT 1

1.1 Objectives

The objective of this project is to exercise SPICE circuit simulations using Cadence tools to study the characteristics of 16nm FinFET technology. The focus is on understanding the behavior of NMOS and PMOS transistors, designing a CMOS inverter, and comparing it with an NMOS-only inverter.

1.2 Report

1 Figure 1 shows a single NMOS and PMOS. In this problem, we calibrate the IV characteristics of this 16nm technology. Each transistor has 8 fins.

a) Plot out IDS vs. VDS in one figure, for VGS =0.05V-VDD , at the step size of 150mV; VDS =0-VDD, at the step size of 1mV;

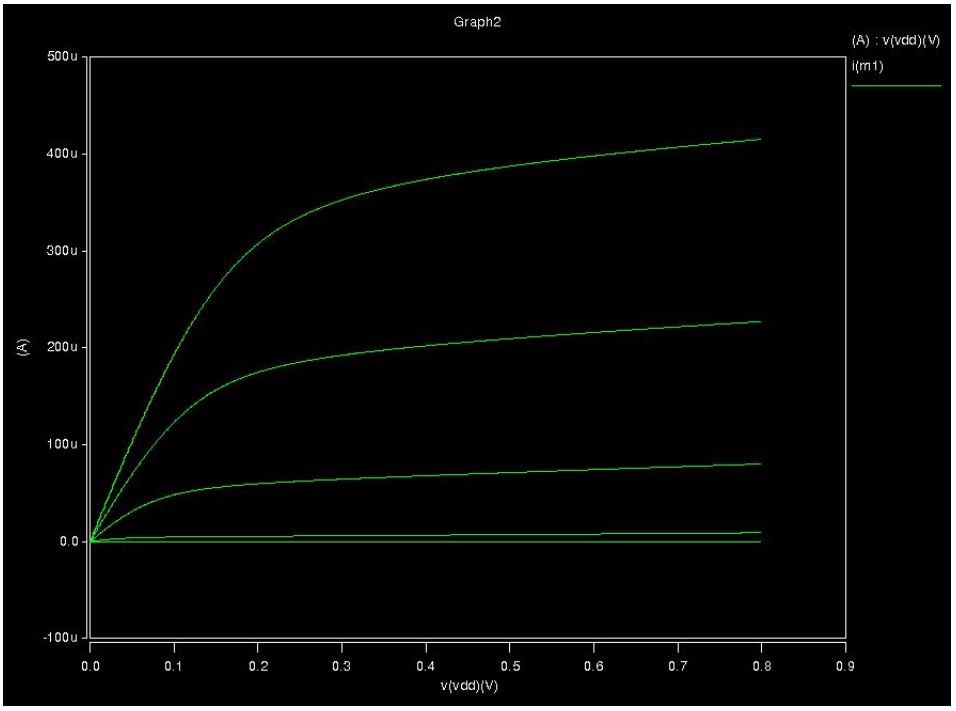

Figure 1: 1(a) $I_{ds} vs V_{ds}$

b) Plot out log(IDS) vs. VGS , for VDS =0.15V and VDD ; VGS =0-VDD , at the step size of 1mV.

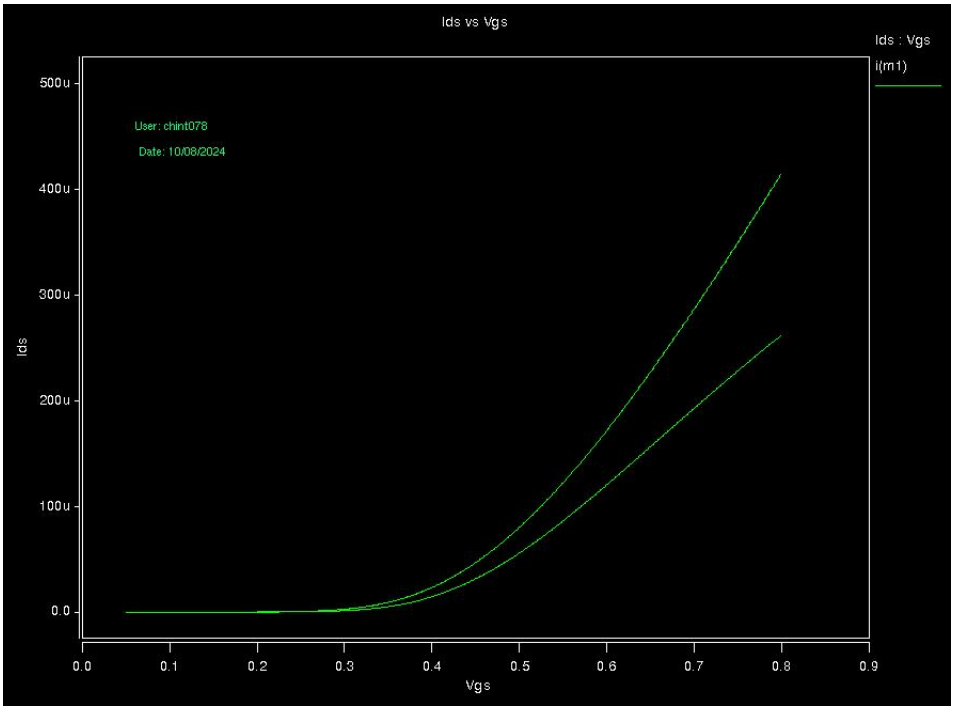

Figure 2: $I_{ds} vs V_{gs}$

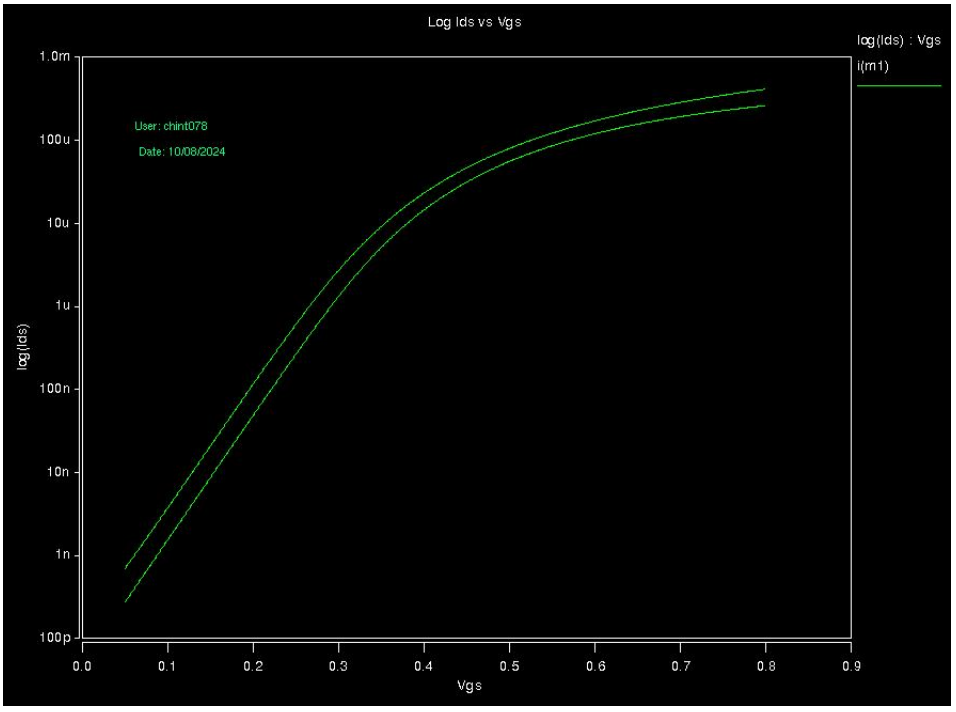

Figure 3: $\log(I_{ds}) vs V_{gs}$

b)Repeat
Step (1) for the PMOS transistor

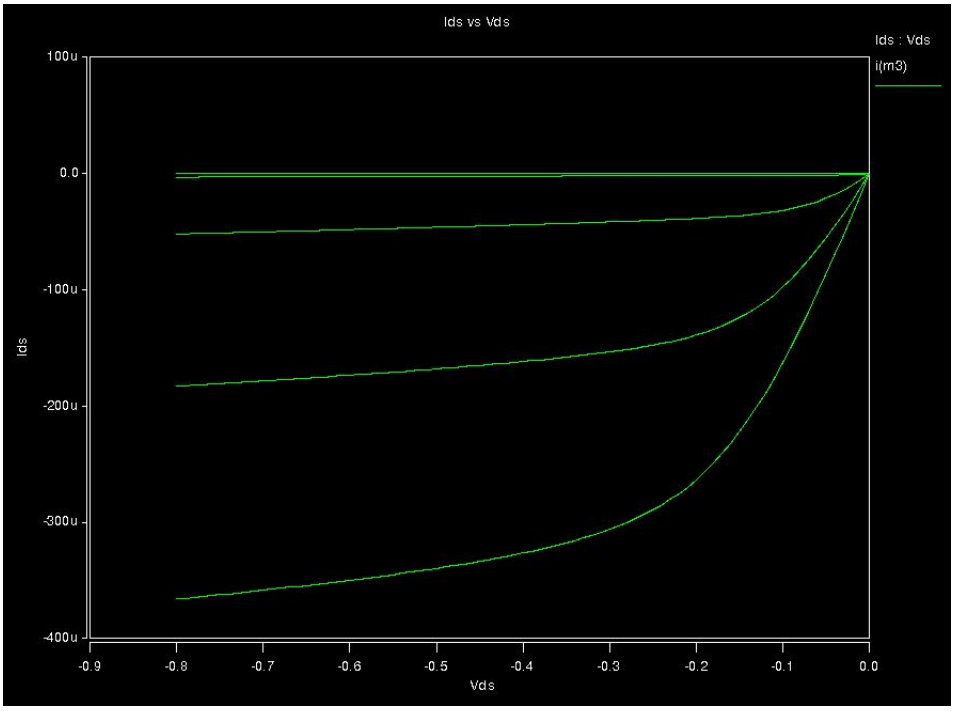

Figure 4: $I_{ds} vs V_{ds}$

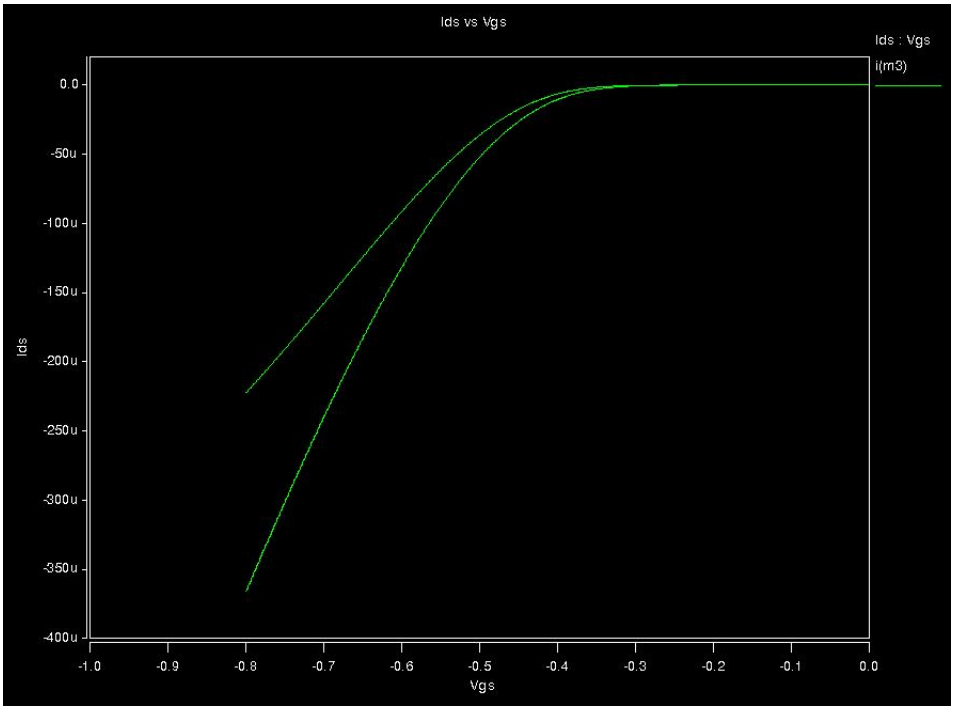

Figure 5: $I_{ds} vs V_{gs}$

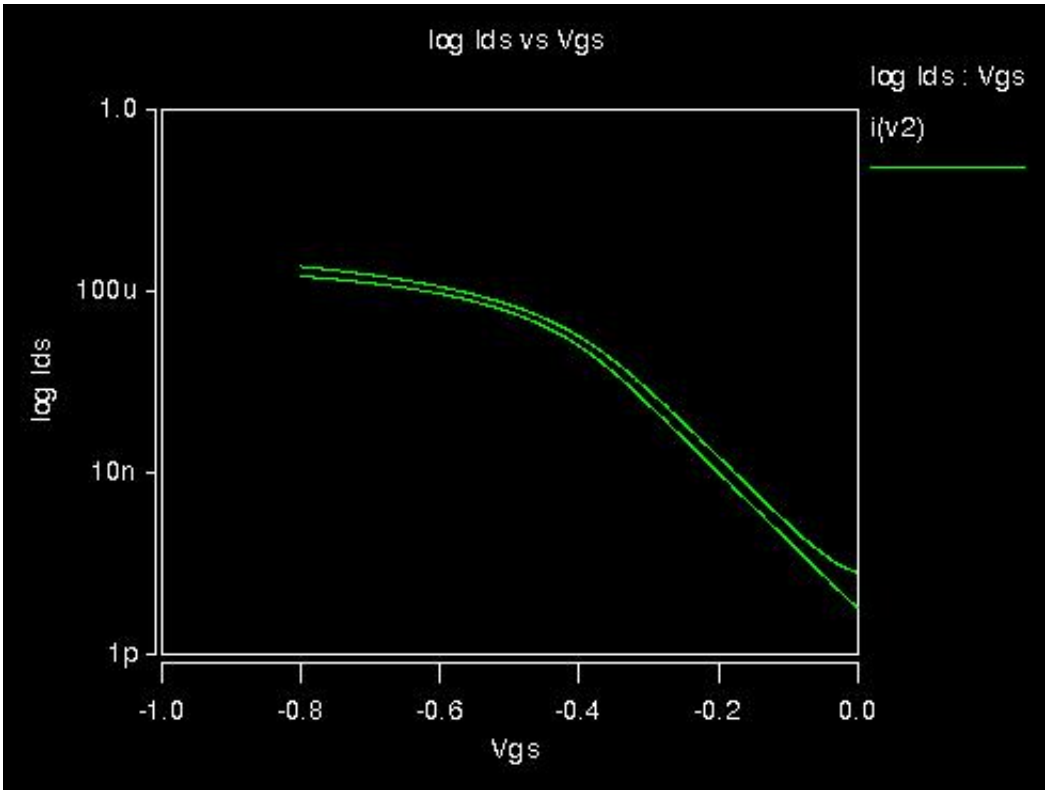

Figure 6: $\log(I_{ds}) vs V_{gs}$

2) CMOS inverter design Figure 2 shows the design of a CMOS inverter. Both PMOS and NMOS FinFETs have 8 fins. CL=10fF, which is added in the test bench, not in the schematic a)Plot out the voltage transfer characteristic(VTC), which is the curve of Vout vs. Vin , when Vin sweeps from 0 to V DD

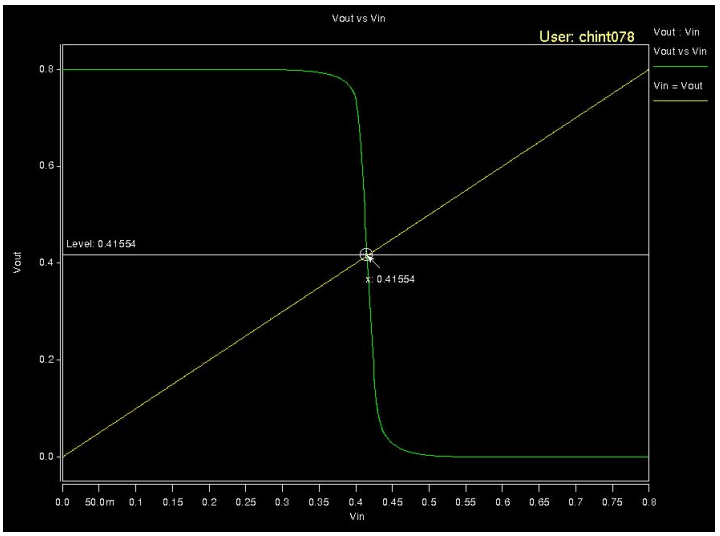

Figure 7: $V_{out} vs V_{in}$

b) a ramp input to V in , which is a 0 to VDD switching, with the transition timeTr =20ps (as shown in Figure 2). Plot out the waveform of Vout . Measure the 50% VDD delay (i.e., time difference from the 50% point of input to the 50% point of output) and the time for Vout to transit from 90%-10% VD

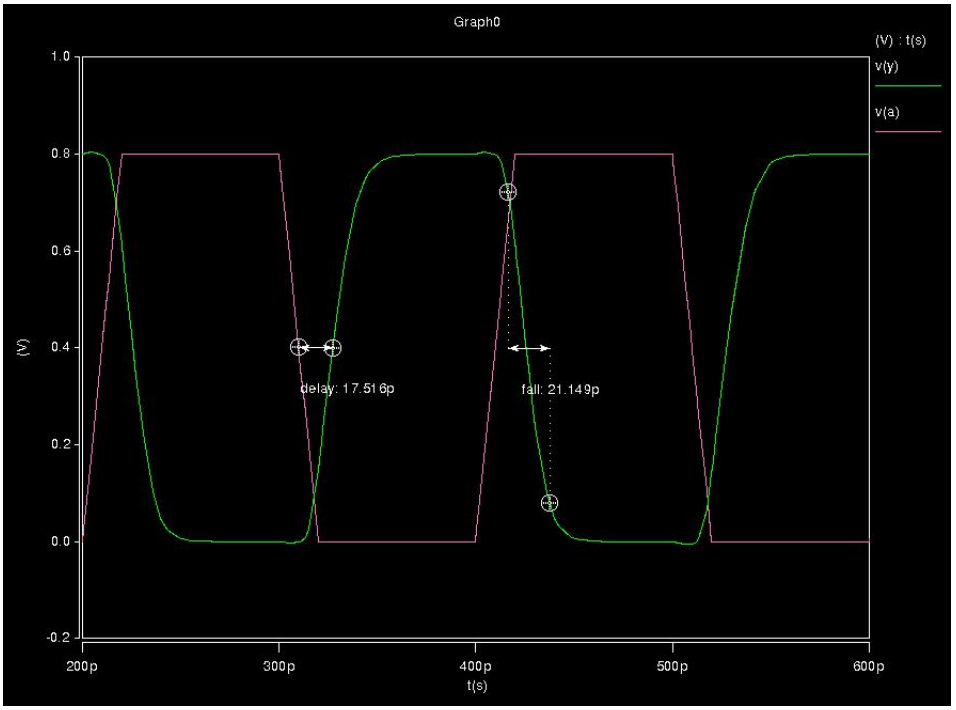

Figure 8: Voltages VS Time

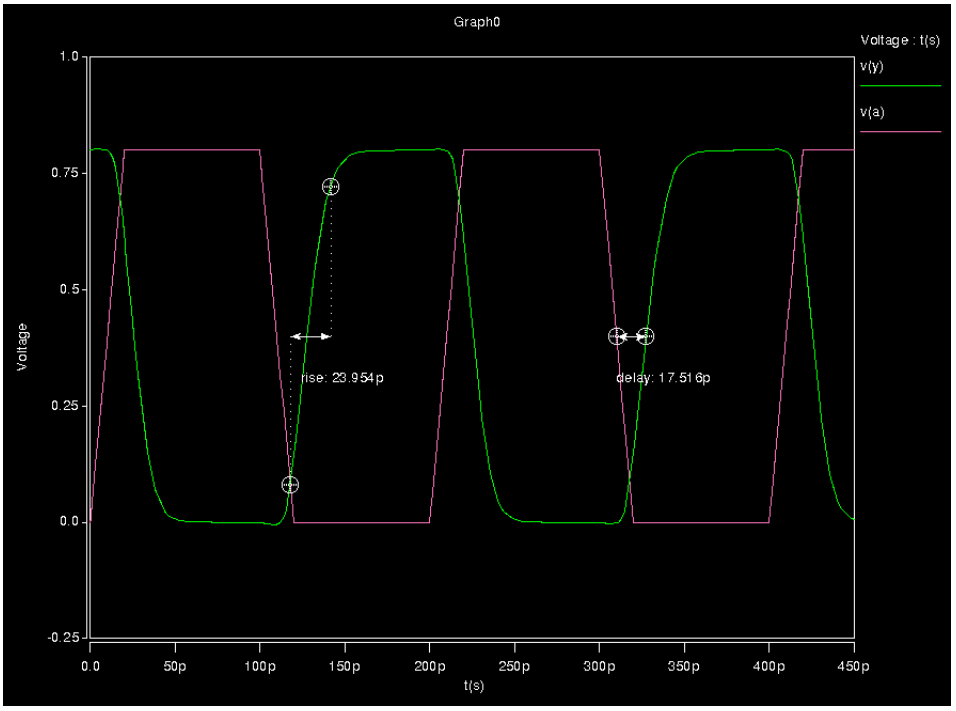

Figure 9: Voltages vs Time

A NMOS only inverter Figure 3 shows the design of an inverter with NMOS only. Both NMOS transistors have 8 fins. a. Simulate the maximum and minimum voltages at Vout . What's the corresponding Vin for them?

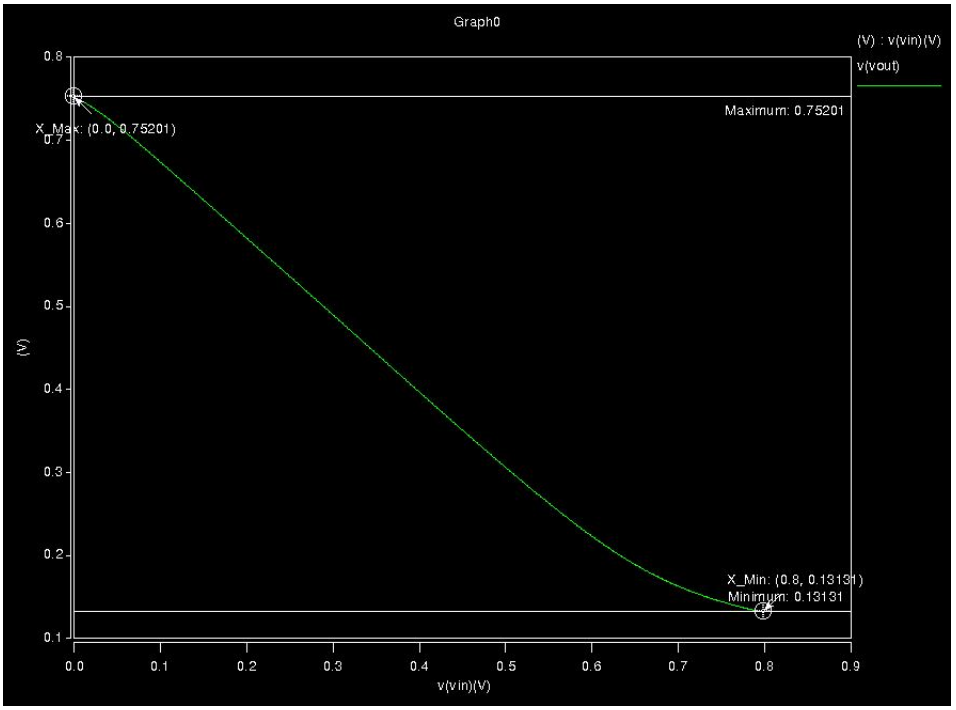

Figure 10: 3(a) NMOS Inverter $V_{out} vs V_{in}$

b. Similar to a. in Prob. 2, plot out the VTC.

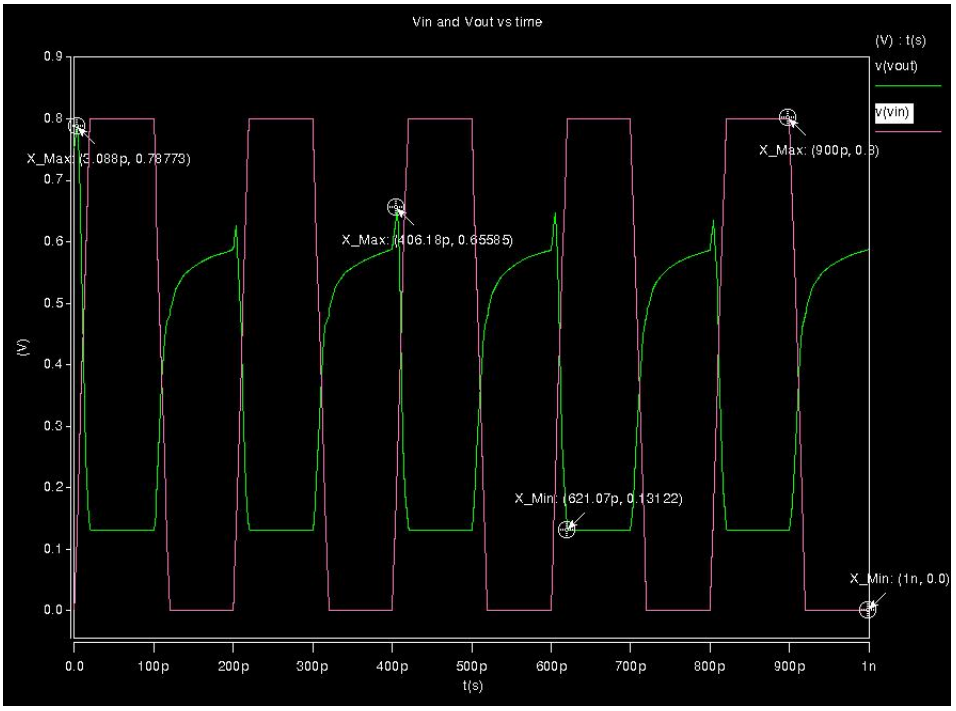

Figure 11: 3(b) NMOS Inverter-Transient Analysis

c. Compare this design with the CMOS inverter. What are the main disadvantages?

1) The Curve of NMOS Looks more softer than CMOS Inverter (Which is more steeper) Indicates the Less Noise margin . THe VOH(Ideally Should be VDD 0.8V) and VOL points(Ideally Should be GND OV)of The graph moved towards Vm point making less stable even at low noise .
2)One of the biggest disadvantages of the NMOS-only inverter is that it consumes static power even when the input is held constant.When the input is low (Vin = 0), the output is high (VOH), but due to the weak pull-up mechanism, a direct current path exists between VDD and ground through the NMOS transistor. This causes a constant static power dissipation.
3)The CMOS inverter is generally faster than an NMOS-only inverter because of its complementary nature, where an NMOS transistor pulls the output down and a PMOS transistor pulls the output up.
4)Symmetric Drive Strength: CMOS has symmetic Drive Strength making it ideal ,NMOS has Threshold Drop Making it Non ideal for Pull UP
5)Low Capacitance : NMOS-only design have a higher intrinsic capacitance .Charging the output node capacitance takes longer due to the weaker pull-up, increasing the rise time.
6)Asymetric Rise and Fall signals due to difference in Drive Strengths This results in longer rise times and increased propagation delays, particularly in the transition from low to high, making it slower overall than the CMOS inverter.