EE 5323

Fall 2024, Yu (Kevin) Cao

Project 2

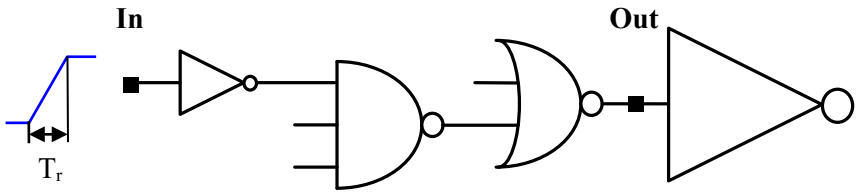
Due Friday, November 8, 11:59pm, submitted to Canvas.

Submission: Prepare a concise report (<5 pages) with key steps to find the answer and important results. Please include layout view with DRC and LVS pass screenshots, and the simulation results with both schematic and extracted view. Place the report in Assignment at Canvas with the filename as: EE5323_Project_2_your name.

The objective of this lab is to practice of logic circuit design, optimization, and layout.

Delay optimization and implementation of a logic path

The figure below shows a 3-stage logic path. V_{DD} = 0.8V. The input signal is a linear ramp input with $T_r = T_f$ = 20ps (between 0% and 100% V_{DD}). The load capacitance at the final output node is an inverter which is 25 times the size of the first inverter. Note: this final inverter is the load when you do the simulation. It is NOT included in the layout.



W_{N1} = 8 Fins W_{N2} = X Fins W_{N3} = Y Fins W_{N4} = 120 Fins

a. All four gates are implemented with complementary static logic, with PUN and PDN having the same drive capability (i.e., PMOS and NMOS are appropriately sized) – please appropriately size the ratio of PMOS/NMOS first. Describe your ratio of the transistors in the report.

b. Use logical efforts to estimate the size W_{N2} and W_{N3}, such that the delay from In to Out is minimized. Please include your hand calculation in the report.

c. Create the HSPICE testbench to simulate the schematic from In to Out, and monitor the delay. What's the value of t_{pHL} and t_{pLH} from In to Out?

d. **Use the standard cells from TSMC 16 library to make the layout of the entire path in Virtuoso. Verify DRC with Calibre.** Tune the size W_{N2} and W_{N3}, calculated in (b), to the available sizes of standard cells. Please include the layout view, DRC and LVS pass screenshots in your report.

e. Extract the netlist and simulate the delay again in HSPICE. What's the value of t_{pHL} and t_{pLH} now?