UNIVERSITY OF MINNESOTA

5327 VLSI DESIGN LAB (Section 004)

Project 2

conducted on : *08th Nov 2024*

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VLSI DESIGN PROJECT 1

1.1 Objectives

The objective of this lab is to practice logic circuit design, optimization, and layout techniques. Specifically, this project aims to minimize delay in a 3-stage logic path by appropriately sizing transistors, implementing the design in a layout tool, and validating the design through simulations.

1.2 Report

1.3 Introduction Theory

In digital circuits, delay optimization is crucial for enhancing performance. The delay between the input and output of a logic path is influenced by factors such as transistor sizing, load capacitance, and the logical effort of the stages. The logical effort method is used to size transistors in such a way that the propagation delay is minimized. This involves calculating the appropriate PMOS to NMOS width ratio and adjusting subsequent stages based on logical effort principles to reduce overall delay.

For this project: VDD is set to 0.8V. The input signal has a linear ramp with a rise and fall time of 20ps.

a. All four gates are implemented with complementary static logic, with PUN and PDN having the same drive capability (i.e., PMOS and NMOS are appropriately sized) – please appropriately size the ratio of PMOS/NMOS first. Describe your ratio of the transistors in the report.

In CMOS technology, complementary static logic gates are implemented with pull-up networks (PUN) and pull-down networks (PDN) that have equal drive strengths. To maintain balance and proper functioning of the circuit, the PMOS and NMOS transistors are sized proportionally. A commonly used ratio for achieving similar rise and fall times in Finfet circuits is approximately 1:1 for PMOS to NMOS width ratios.

Transistor Sizes: WN1 = 8 Fins, WN2 = 42 Fins, WN3 = 33 Fins, WN4 = 120 Fins

Part B: Delay Optimization with Logical Effort Use logical efforts to estimate the size WN2 and W N3 , such that the delay from In to Out is minimized. Please include your hand calculation in the report. Theory

Logical effort is a method used to determine the optimal sizes of transistors in a multi-stage logic path to achieve minimal delay. The delay of a stage is proportional to its logical effort and the load it drives. By using logical effort, we can estimate the appropriate sizing for each stage (WN2 and WN3) based on the load presented by WN4.

Calculations

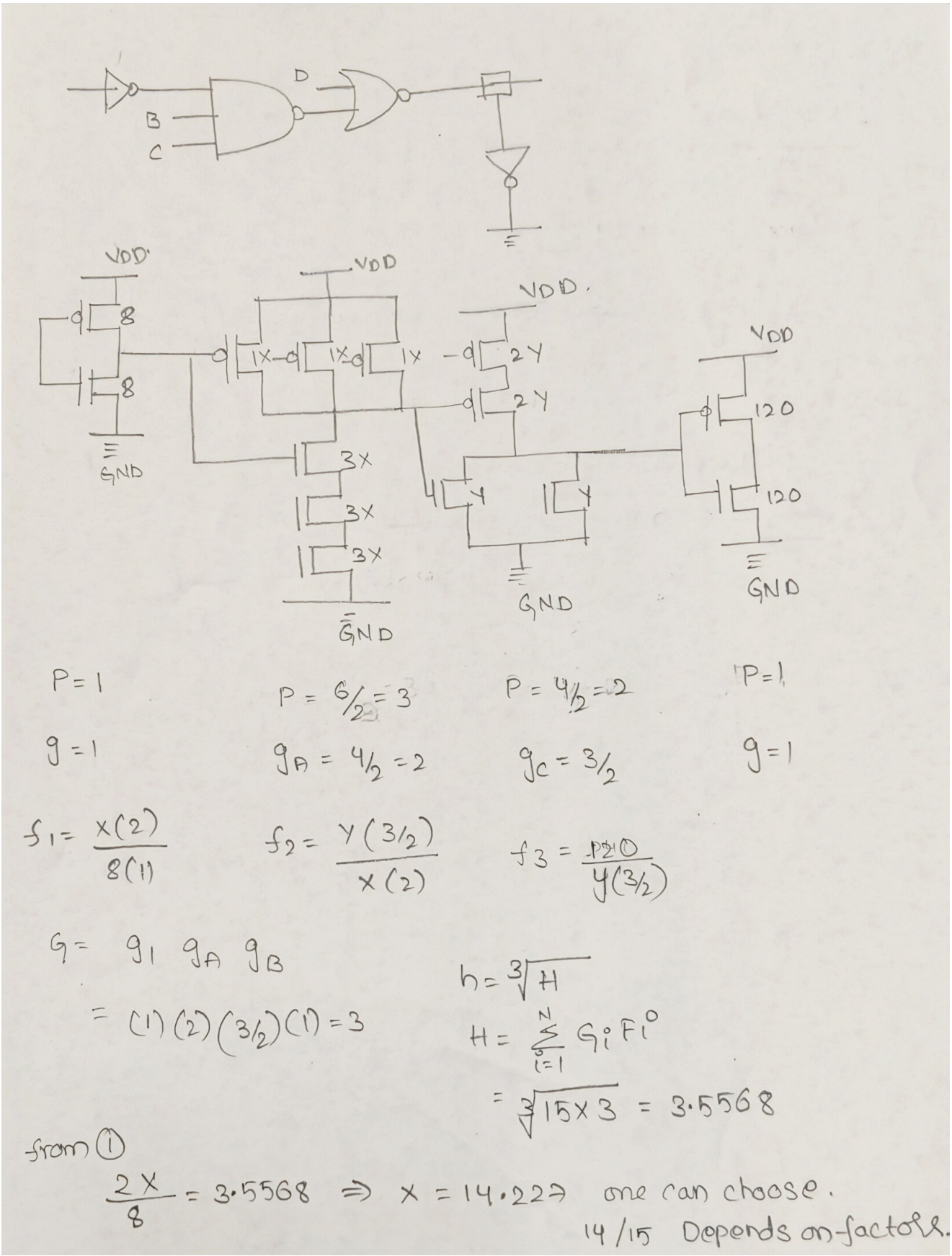

Figure 1: Calculation 1

From (2)

$$\frac{2 \times Y\,(3/2)}{X(2)} = 3.5568$$

$$Y = \frac{2 \times 3.5568 \times 14.2272}{3}$$

$$= 33.9328. \longrightarrow 33/34 \text{ varies}$$

Min delay =) $t_p = \sum_{i=1}^{N} P_i + N h$

$$1+3+2+3 \times 3.5568$$

$$T_p = 16.65 \text{ ps.}$$

Inverter 1 $\Rightarrow$ $w_N = 8$ Ratio = 1

$w_{PMOS} = 8$

NAND => $w_{NMOS} = 3 \times 14 = 42.$ Ratio = $\frac{PMOS}{NMOS} = 1/3.$

$w_{PMOS} = 14 = 42$

NOR => kl_{NMOS}

kl_{PMOS} ratio = $\frac{2}{1}$

Figure 2: calcuation 2

Results Hand Calculations: for Optimal delay All the Gates should have samme effort delay which is equal to 3.5568 ps .

So the optimal delay That can be optained is (1+3+2)+3*3.5568 ps =16.65ps . for Both TPhl and TPlh . This is the calculated result . To obtain this All the stages should be sized appropiately to X=14.227, y= 33.7328. which will be make Wnmos in NAND to 42 approximately . Wnmos of NOR to 33 approximated . We Doesnt favour any Node in this calculation and this the min delay we can achieve for this circuit when there is switching from 0 to 1 .

Part C: HSPICE Schematic Simulation

1. Create an HSPICE testbench simulating the 3-stage logic path from input to output.

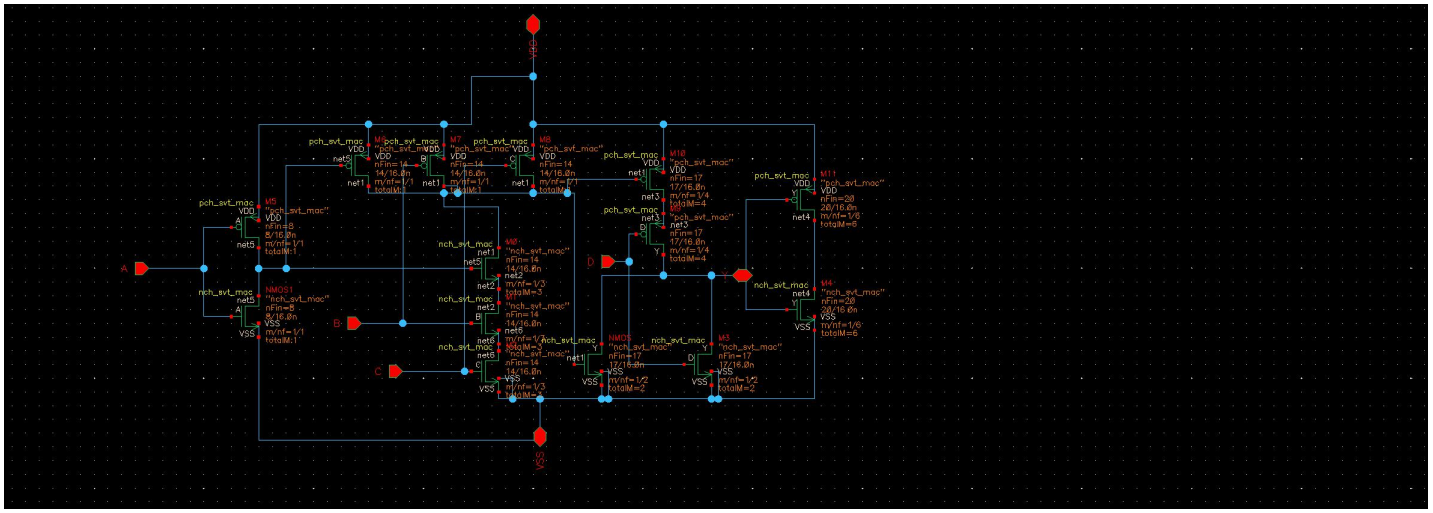

Figure 3: Schematic

2. Measure the high-to-low (tpHL) and low-to-high (tpLH) propagation delays from In to Out.

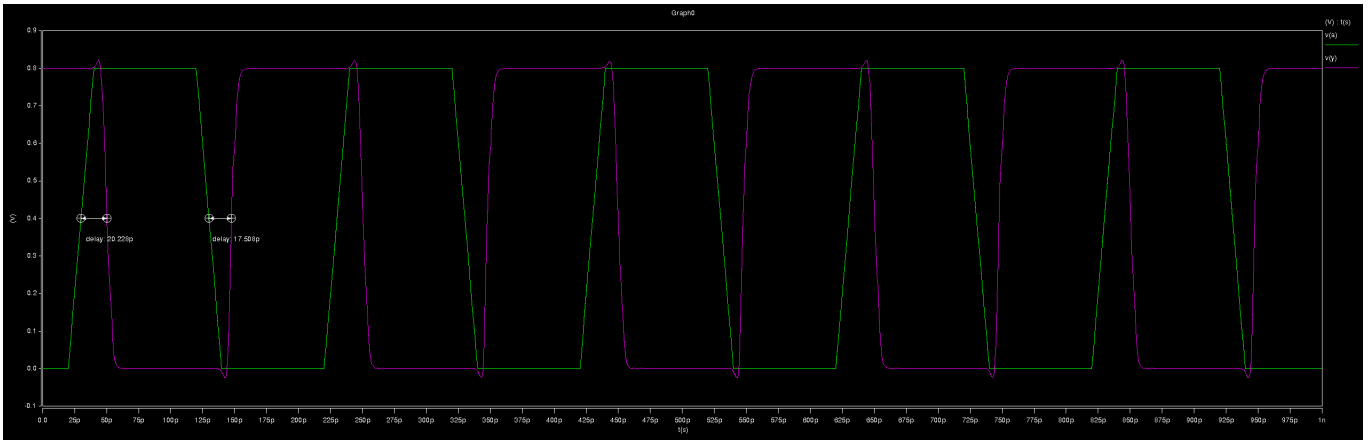

Figure 4: Medium Delay

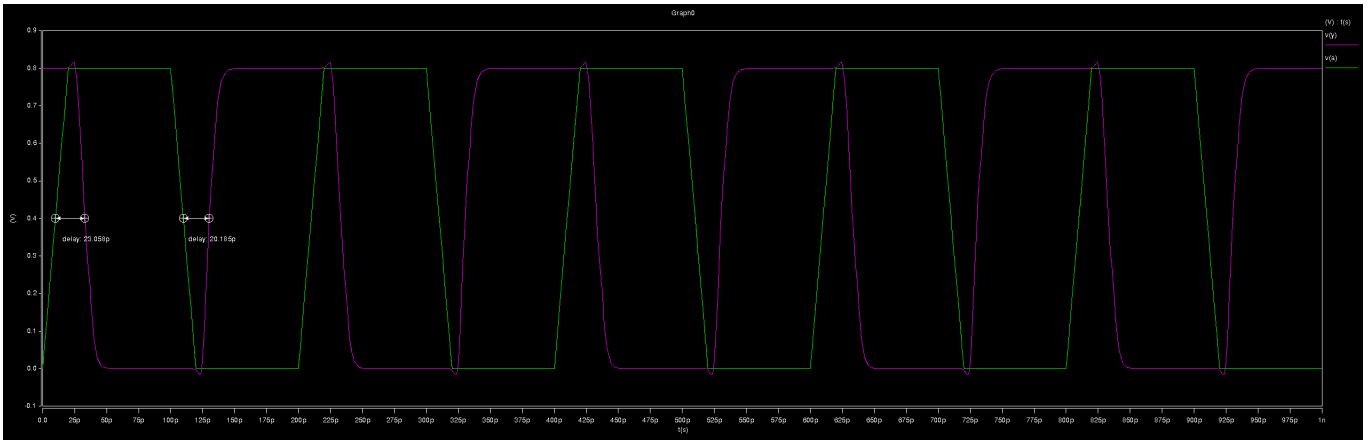

Figure 5: More Delay

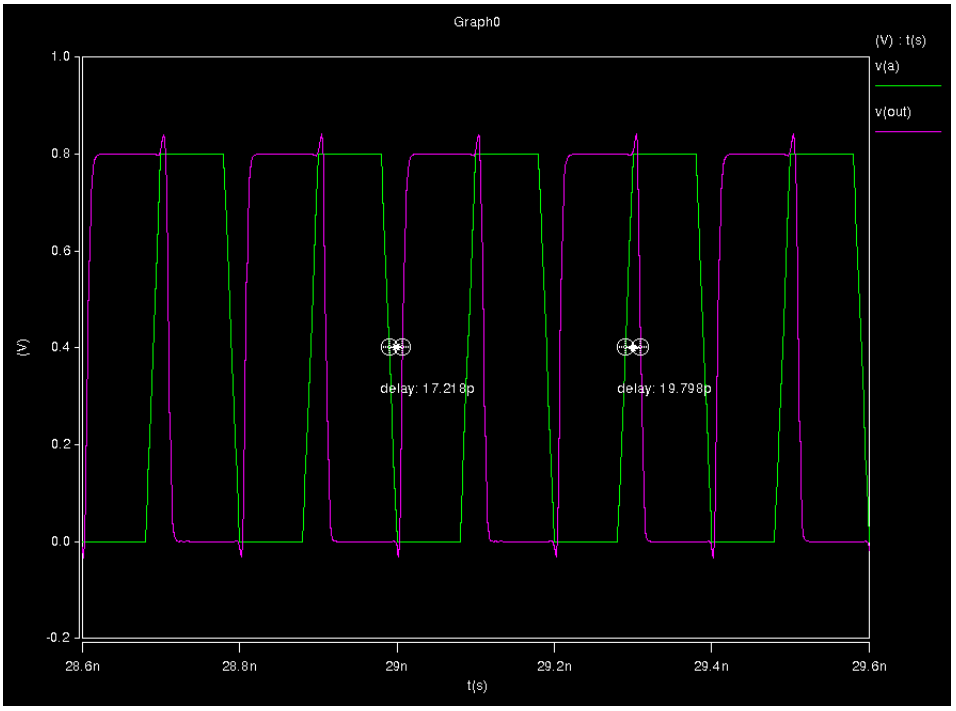

Figure 6: Most Least Design

Results Most least Design

tpHL (In to Out): 17.218 ps

tpLH (In to Out): 19.782 ps

Conclusion

1)The delay of a multi-stage logic path was successfully minimized by applying transistor sizing based on logical effort and implementing an optimized Simulations.As we can see depending on the sizing combinations we can really find difference in Delay values . If the switching node is closer to the output we will get the least delay values as shown. If the Switching node is far from output node the values vary a bit due to the capacitab=nce in the path.

2The Values of Tphl and TPlh are not same in the graph due to stacking effect and difference in Mobility of Electrons and holes .

3)The combination of of approximating Up and Approximating Down also decides the delay values .