DATA SHEET

Ethernet IP Core

Introduction

The Ethernet IP Core is a 10/100 Media Access Controller (MAC). It consists of a synthesizable Verilog RTL core that provides all features necessary to implement the Layer 2 protocol of the Ethernet standard. It is designed to run according to the IEEE 802.3 and 802.3u specifications that define the 10 Mbps and 100 Mbps Ethernet standards, respectively.

Features

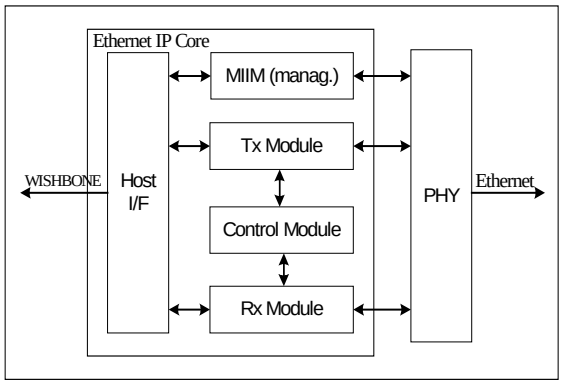

Figure 1: Core Architecture Overview

The core provides the following features:

- Flow control and automatic generation of control frames in full duplex mode (IEEE 802.3x)
- Collision detection and auto re-transmission on collisions in half duplex mode (CSMA/CD protocol)
- Automatic 32-bit CRC generation and checking
- Preamble generation and removal
- Complete status for TX/RX packets
- IEEE 802.3 Media Independent Interface (MII)
- WISHBONE SoC Interconnection Rev. B compliant interface

General Description

Architecture

Adjoining figure shows the general architecture of the Ethernet IP core. It consists of several building blocks:

- TX Ethernet MAC (transmit function) block with the CRC generator
- RX Ethernet MAC (receive function) block with the CRC generator
- MAC control block
- Management block (MIIM)
- Host interface

TX and RX Modules

The TX and RX modules provide full transmit and receive functionality. CRC generators are incorporated in both modules for error detection purposes. The modules also handle preamble generation and removal. Padding occurs automatically (when enabled) in compliance with the IEEE 802.3 standard. When enabled, packets greater than the standard can be transmitted.

Control Module

The control module provides full duplex flow control, according to the IEEE 802.3u standard. Flow control is achieved by transfering the PAUSE control frames between the communicating stations.

Management Module (MIIM)

The management module provides the standard IEEE 802.3 Media Independent Interface (MII) that defines the connection between the PHY and link layers. Using this interface, the device (RISC) connected to the host interface can force PHY to run at 10 Mbps versus 100 Mbps or to

configure it to run at full versus half duplex mode.

WISHBONE Interface

The WISHBONE interface connects the Ethernet core to the RISC and to external memory. The core is WISHBONE SoC Interconnection specification Rev. B compliant. The implementation realizes a 32-bit bus width and does not support other bus widths.

Utilization

The following table lists the core's intended applications.

Technology	FPGA Size	Silicon Area	Speed	Power Consumption
Xilinx Virtex	2600 slices	100000 gates	60 MHz	